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60 GHz IMPATT DIODE DEVELOPMENT

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16. Abstract

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ABSTRACT

The objective of this program is to develop 60 GHz IMPATT diodes suitable for communications applications. The performance goals of the 60 GHz IMPATT is 1W CW output power with a conversion efficiency of 15 percent and 10-year lifetime.

The final design of our 60 GHz IMPATT structure evolved from computer simulations performed at the University of Michigan. The initial doping profile, involving a hybrid double-drift (HDD) design, was derived from a drift-diffusion model that used the static velocity-field characteristic for GaAs. Unfortunately, the model did not consider the effects of velocity undershoot and delay of the avalanche process due to energy relaxation. Consequently, our initial devices were oscillating at a much lower frequency than anticipated. With a revised simulation program that included the two effects given above, a second HDD profile was generated and was used as a basis for our fabrication efforts.

In the area of device fabrication, significant progress was made in epitaxial growth and characterization, wafer processing, and die assembly. During the early part of this program, two epitaxial growth techniques were employed in the preparation of the 60 GHz HDD structures, namely: (a) halide-vapor phase epitaxy (H-VPE), and (b) organo-metallic chemical vapor deposition (OMCVD). Due to the advantages involved, it was agreed that efforts would only be focused on the OMCVD approach during the approved extension to the original 24-month duration of this program.

Starting with a baseline X-Band IMPATT technology, appropriate processing steps were modified to satisfy the device requirements at V-Band. In terms of efficiency and reliability, the device requirements dictate a reduction in its series resistance and thermal resistance values. Qualitatively, we were able to reduce the diodes' series resistance by reducing the thickness of the N+ GaAs substrate used in its fabrication. Additional improvement in the device performance was achieved by using diamond as a heat sink. In this case the conventional

50-65 microns of gold plated heat sink (PHS) was reduced to 2-5 microns, thereby allowing the junction of the bonded device to be positioned closer to the diamond heat sink.

To evaluate the RF performance of our 60 GHz double-drift IMPATTs, a V-Band top hat cavity was designed and fabricated. This design was chosen over a coaxial-waveguide circuit because of its broad band nature. Impedance matching between the diode and its circuit was achieved by trying various top hat structures and diode heat sink holders. Additionally, optimum device performance was obtained by using a sliding short.

As a result of the approach outlined above, hybrid double-drift IMPATTs were fabricated with the following RF characteristics:

Frequency range:	54-58.7 GHz
CW Output Power	
Average	505mW
Best	600mW
Conversion Efficiency	
Average	10.2%
Best	15.3%

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SECTION 1
INTRODUCTION AND SUMMARY

This is the final report for work performed under Contract No. NAS3-23339, sponsored by NASA-Lewis Research Center. The objectives of this program were to design, fabricate, test and deliver 60 GHz Gallium Arsenide Double-Drift IMPATT diodes. The goal in device performance was 1 watt CW output power with a DC to RF conversion efficiency of 15% or greater.

The final design of our 60 GHz IMPATT structure evolved from computer simulations performed at the University of Michigan. The initial doping profile, involving a hybrid double-drift (HDD) design, was derived from a drift-diffusion model that used the static velocity-field characteristic for GaAs. Unfortunately, the model did not consider the effects of velocity undershoot and delay of the avalanche process due to energy relaxation. Consequently, our initial devices were oscillating at a much lower frequency than anticipated. With a revised simulation program that included the two effects given above, a second HDD profile was generated and was used as a basis for our fabrication efforts.

In the area of device fabrication, significant progress was made in epitaxial growth and characterization, wafer processing, and die assembly. During the early part of this program, two epitaxial growth techniques were employed in the preparation of the 60 GHz HDD structures, namely: (a) halide-vapor phase epitaxy (H-VPE) as described in Section 2, and (b) organo-metallic chemical vapor deposition (OMCVD), as described in Section 3. Due to the advantages involved, it was agreed that efforts would only be focused on the OMCVD approach during the approved extension to the original 24-month duration of this program.

Some of the major accomplishments achieved from the epitaxial growth efforts include:

1) A thorough characterization of growth parameters for uniform sub-micron epitaxial layers (of high electrical quality) on large area substrates.
2) The development of a highly predictable N-type doping technology using silane.
3) Demonstration of extremely sharp doping transitions.
4) Reproducible growth of P-type layers using dimethylzinc and diethylzinc as P-type dopants.
5) The growth of single and double-drift IMPATT structures for 60 GHz applications.

Starting with a baseline X-Band IMPATT technology, appropriate processing steps were modified to satisfy the device requirements at V-Band. In terms of efficiency and reliability, the device requirements dictate a reduction in its series resistance and thermal resistance values. Qualitatively, we were able to reduce the diodes' series resistance by reducing the thickness of the N+ GaAs substrate used in its fabrication. For example, by thinning the 60 GHz IMPATT substrate to 10-15 microns (from the conventional 25-30 microns employed at 10 GHz), we were able to increase the device efficiency by a factor of 2. Additional improvement in the device performance was achieved by using diamond as a heat sink. In this case, the conventional 50-65 microns of gold plated heat sink (PHS) was reduced to 2-5 microns, thereby allowing the junction of the bonded device to be positioned closer to the diamond heat sink. The processing sequence and techniques used to fabricate these thin, 60 GHz, IMPATT devices is given in Section 4.

For preliminary RF evaluations, chips from 60 GHz epitaxial wafers were thermocompression bonded (TCB) onto threaded ODS-138 copper packages. Promising candidates (those that yielded approximately 300mW on copper) were later TCB onto diamond heat sink packages. These packages were manufactured in-house and consisted of threaded copper bases into which cylindrical diamonds were hand-pressed. Subsequent to the embedding process, ceramic spacers (32 mils OD; 16 mils ID; 8 mils high - typically used on ODS-138 packages) were bonded onto the diamond packages.

As an aid in impedance matching of the IMPATT device to its external circuit, the strap inductance was varied by using different gold ribbon (strap) configurations, namely: single, double (crossed), and triple. From this experiment, the highest output power and operating frequency were obtained using the double strap configuration. Additional efforts to reduce the parasitics associated with the ODS-138 package involved the fabrication of very small ceramic spacers (OD = 16 mils; ID = 8 mils, H = 4 mils). While the small spacers were successfully fabricated, devices assembled with them proved difficult to operate in our top hat cavity.

To evaluate the RF performance of our 60 GHz double-drift IMPATTs, a V-Band top hat cavity was designed and fabricated. This design was chosen over a coaxial-waveguide circuit because of its broad band nature. Impedance matching between the diode and its circuit was achieved by trying various top hat structures and diode heat sink holders. Additionally, optimum device performance was obtained by using a sliding short.

SECTION 2

HALIDE VAPOR PHASE EPITAXY (H-VPE)

2.0 INTRODUCTION

As indicated earlier, 60 GHz hybrid double-drift (HDD) IMPATT structures were initially prepared using H-VPE and Organo-Metallic Chemical Vapor Deposition (OMCVD) systems. After the first two years of this contract, H-VPE efforts were discontinued and more emphasis was placed on the OMCVD approach because of its advantages in growing millimeter-wave device structures. While Section 3 describes the OMCVD approach, this section of the final report will discuss the progress made in growing 60 GHz HDD structures using a H-VPE system.

At the initiation of this program a specially designed computer controlled H-VPE system was constructed and dedicated towards the growth of double-drift structures. Since then the epitaxial growth techniques in the new system evolved in stages which finally culminated in the production of HDD structures. The systems and techniques used for the growth and characterization of 60 GHz HDD epitaxial material are outlined below.

2.1 H-VPE ($AsCl_3$-GaAs-H_2) System

In the open tube H-VPE system, hydrogen is bubbled through $AsCl_3$ which is maintained at a constant temperature. As hydrogen and $AsCl_3$ vapor enter the upstream side of the reactor tube, the following reaction occurs:

$$AsCl_3 + 3/2\ H_2 \rightleftharpoons 1/4\ As_4 + 3HCl \qquad (2.1)$$

The created HCl gas reacts with an undoped GaAs source which is maintained at approximately 800°C. Here,

$$GaAs + HCl \rightleftharpoons GaCl + 1/2\ H_2 + 1/4\ As_4 \qquad (2.2)$$

The above reaction is driven from left to right causing the decomposition of GaAs at 800°C. A seed, or GaAs wafer, is positioned

downstream of the source and is maintained at 700°C. At the seed location, reaction (2.2) is driven in the opposite direction causing the deposition of GaAs on a wafer that is positioned on a carriage. In summary, this VPE process involves the transport of GaAs from a source, where it is formed, to a GaAs wafer, on which it is deposited.

The main features of the H-VPE system used for this program to grow 60 GHz HDD epitaxial material are as follows:

(i) A 4" diameter reactor tube positioned in a 6-zone furnace.
(ii) A multi-channel (tier) seed carriage.
(iii) Separate N and P dopant networks.
(iv) Two $AsCl_3$ bubblers maintained at a constant temperature by means of circulator baths.
(v) An HP1000 computer system for automatic control.
(vi) An electronic console to interface the HP1000 with the VPE system. Features include automatic/manual control of all growth parameters.
(vii) A Pd-diffused hydrogen purifier to supply the VPE system with high purity hydrogen.

Some of the above features are pictured in Figure 2.1.

A schematic of the reactor tube is shown in Figure 2.2. The tube consists of three inlets. The 1st inlet is connected to the $AsCl_3$ growth bubbler and is used to transport hydrogen and $AsCl_3$ vapor necessary for the source reaction. The 2nd inlet is connected to the N-dopant network and allows a flow of silane (SiH_4) to enter the reactor when growing N-type layers. For in-situ etching prior to epitaxial growth, the 2nd inlet is also used to transport $AsCl_3$ from the etch bubbler. The 3rd inlet is located further downstream of the 2nd inlet and is used as a conduit for dimethylzinc (DMZ)/diethylzinc (DEZ) when growing P-type layers.

The furnace that accommodates the 4" diameter tube consists of six zones with each zone independently controlled by a temperature

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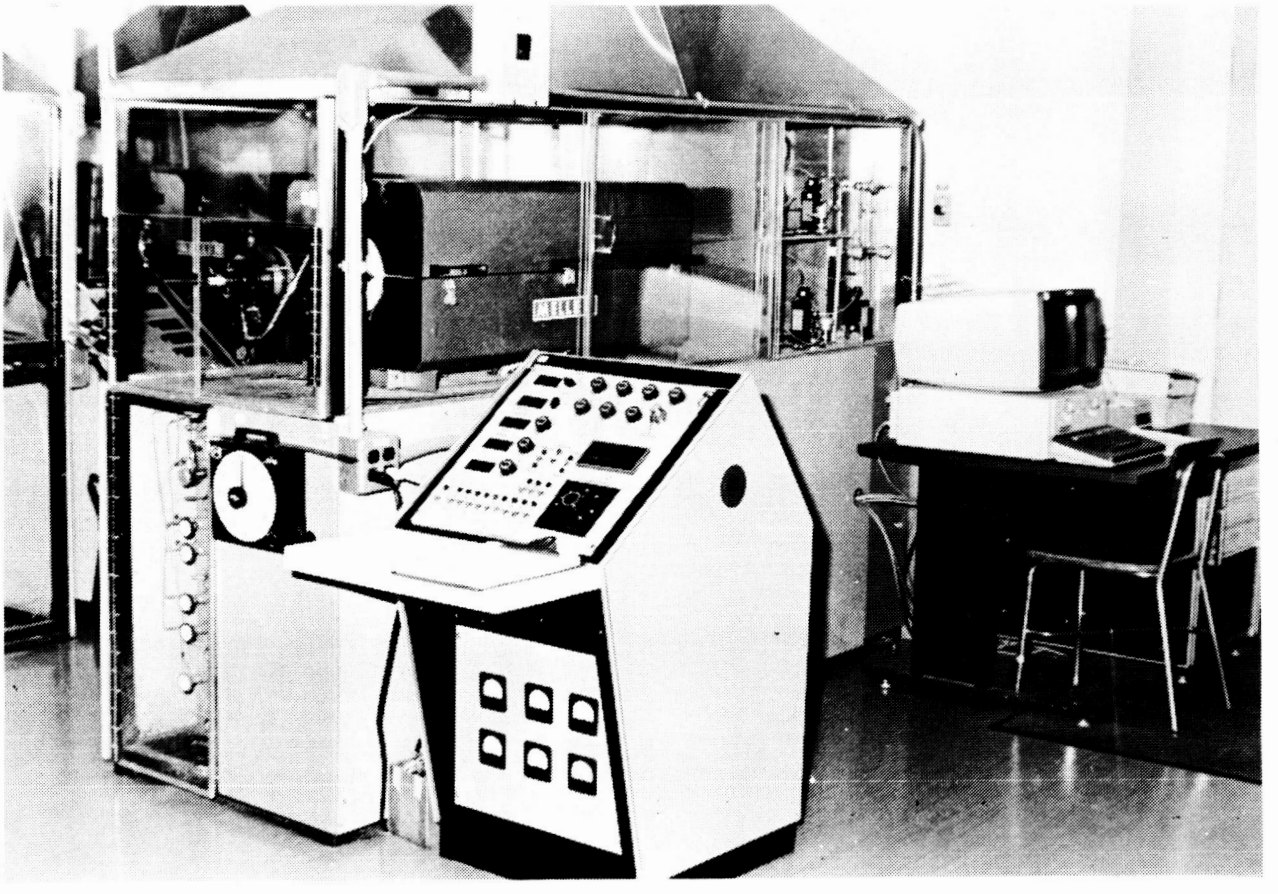

FIGURE 2.1 NEW LARGE BORE (4" DIA.) COMPUTER CONTROLLED $AsCl_3$ - GaAs - H_2 SYSTEM.

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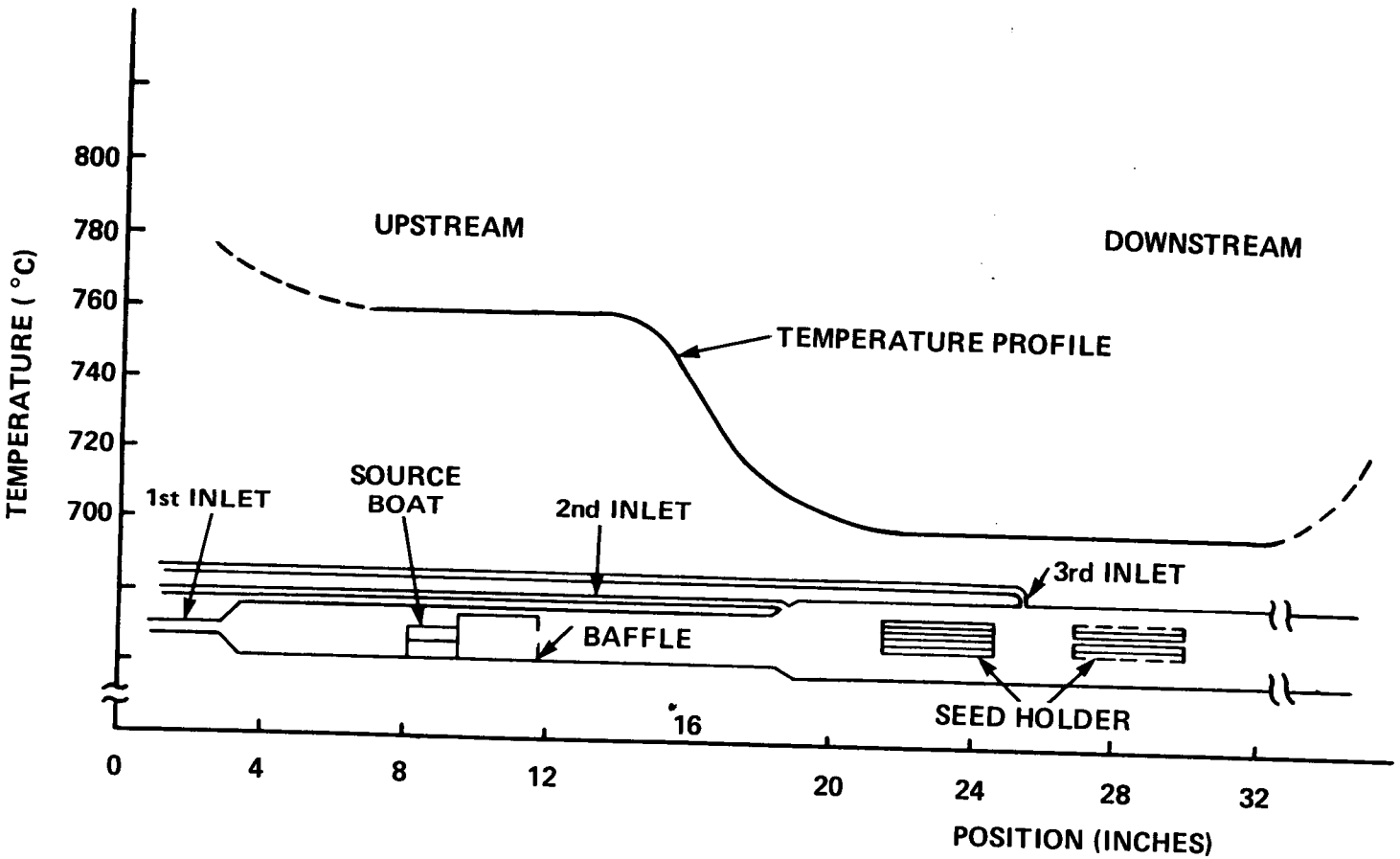

FIGURE 2.2 SCHEMATIC OF 4" DIAMETER REACTOR TUBE POSITIONED WITH RESPECT TO TEMPERATURE PROFILE.

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controller and SCR power supply. Twenty-three thermocouples are positioned along the length of the furnace with six of them being control thermocouples. The others are used for measuring temperature along the furnace. With a total heated length of 36 inches, the furnace was profiled to yield a 6" constant temperature source zone (760°C) and 12" flat deposition zone (700°C).

The location of the source boat within the reactor tube is shown in Figure 2.2. Adjacent to the source boat is a quartz baffle so as to allow for thorough mixing of the components resulting from the source reaction. During the growth of N-type layers, the seed carriage is positioned between the 2nd and 3rd inlets. Subsequently, the carriage is moved into a region downstream of the 3rd inlet in preparation for the growth of P-type layers. A diagram of the seed carriage used throughout this program is shown in Figure 2.3.

A schematic of the plumbing arrangement is shown in Figure 2.4. This arrangement consist of mass flow controllers, normally opened and normally closed valves, and $AsCl_3$ bubblers. The upper section of the flow diagram in Figure 2.4 that includes MFC 1, 2, and 3 is a representation of the P-dopant network. A separate N-dopant network is also represented and includes MFC 4, 5, and 6. The N and P dopant networks are assembled separately so as to avoid the cross contamination of impurities when growing P-N junctions.

The N-dopant network is configured so as to allow for the growth of N-type layers with a wide range of carrier concentration. For example, when growing highly doped (>2 X $10^{18}/cm^3$) N-type layers, such as buffer layers, a high concentration of silane (100ppm in H_2) bypasses MFC4 and enters the 2nd inlet of the reactor via MFC6 (see Figure 2.5). For this dilution bypass procedure, the configuration of valves 2 and 3 in Figure 2.5 are reversed instantaneously. For moderately doped (10^{15} - $10^{17}/cm^{-3}$) N-type layers, silane is diluted with hydrogen. In this case, MFC4 controls the amount of the concentrated silane that enters the dilution system. This concentrated flow of silane is diluted by a hydrogen flow that is controlled by MFC5. The flow of the diluted silane into the reactor is controlled by MFC6.

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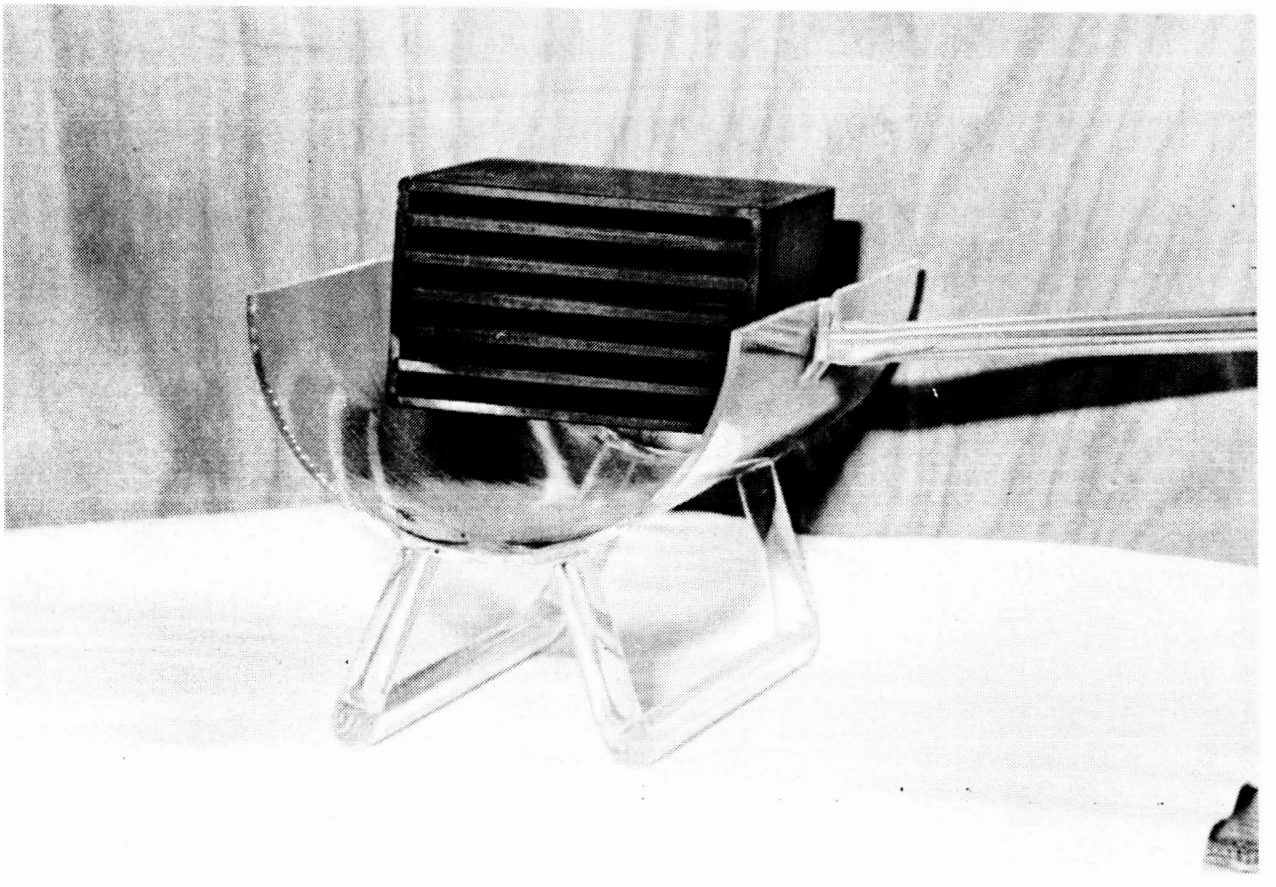

FIGURE 2.3 MULTI-TIER SEED CARRIAGE.

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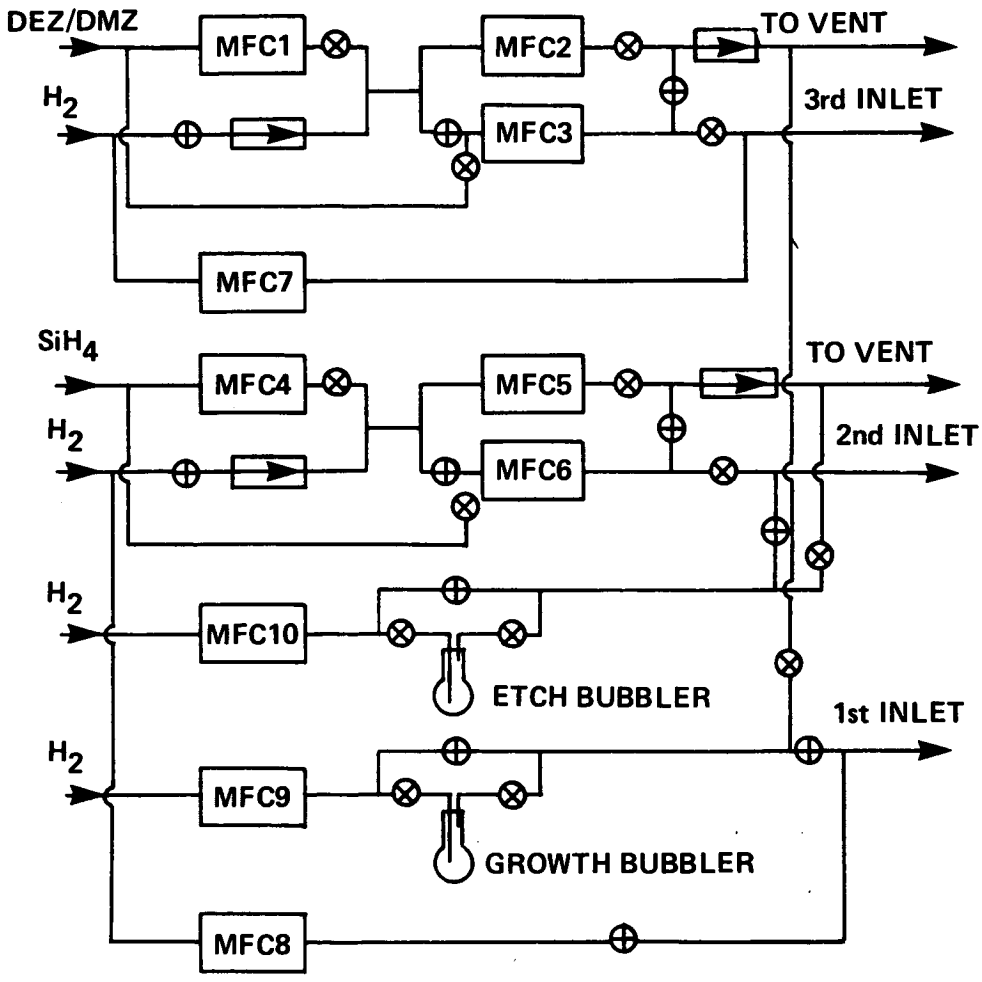

FIGURE 2.4 GAS FLOW CONTROL FOR LARGE BORE DOUBLE-DRIFT REACTOR.

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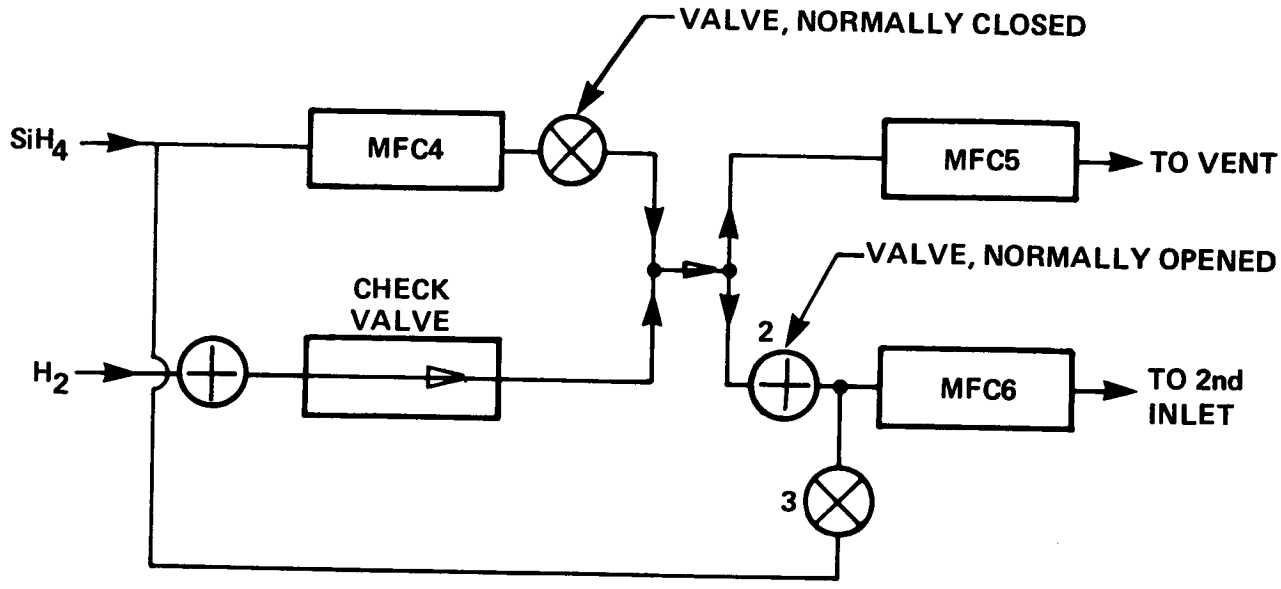

FIGURE 2.5 GAS FLOW CONTROL FOR DOPANT DILUTION SYSTEM.

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The P-dopant network has the same arrangement and capabilities as that used for growing N-type layers. In order to grow highly doped P++ contact layers (~1 X $10^{19}/cm^3$), a concentrated flow of DMZ is routed directly from the tank, via MFC3, to the 3rd inlet of the tube. Dilution of concentrated DMZ/DEZ is achieved in a similar manner as that outlined above for silane. In this case, MFC1, 2 and 3 are employed in the dilution system.

2.2 Computer Control

The new double-drift IMPATT reactor was designed for automatic/manual modes of operation. For automatic control, an HP1000 system was interfaced with the reactor via an electronic console. If computer control is lost, the reactor can be controlled manually from the electronic console.

Due to the complexity of the doping profile required by 60 GHz double-drift structures, it was found necessary to use a computer controlled epitaxial system for growing these structures. The computer was configured so as to accomplish the following:

a) Set and monitor mass flow controllers for each phase.
b) Control the opening and closing of valves during phase transition.
c) Monitor elapsed time for each phase.
d) Set and control thermal set-points on six furnace controllers.
e) Create and store a run data output file that contains requested and monitored parameters. These parameters include run time, flow rates and thermocouple readings for each phase. This data is very useful in troubleshooting the system whenever irregularities in the grown wafer are encountered.

The important advantage of the computer controlled epitaxial system is that it ensures reproducibility of growth runs, assuming

constant source concentrations. Furthermore, sharp doping transitions are achieved since mass flow controllers are instantaneously reset in sychronization with valve switching during phase transition.

2.3 Design of 60 GHz HDD IMPATT Diodes

The theoretical design of the doping profile, required to give optimum device performance at 60 GHz, was done under the direction of Dr. George Haddad at the University of Michigan. A comprehensive computer simulation program was used to generate the desired doping profile. This program is based on the drift-diffusion model and can accommodate any doping profile, velocity-electric field characteristic, ionization rates, and diffusion coefficients.

The hybrid double-drift structure shown in Figure 2.6 represents the initial 60 GHz design generated by the computer simulation program.

Using the doping profile of Figure 2.6 as a guideline for epitaxial growth, we observed that our fabricated diodes oscillated at a much lower frequency (35 GHz) than that predicted by the design (60 GHz). At that time there was speculation that the drift-diffusion model may not be adequate at mm-wave frequencies. The rationale for such speculation is as follows. The bulk material parameters (drift velocity, diffusion coefficient, and ionization rates) are regarded as functions of the local instantaneous electric field. Since the electric field changes very rapidly in mm-wave devices, the transient behavior may dominate and the material parameters may not settle down to the bulk values given by static relations. Also, since the material parameters are more properly functions of carrier energy rather than the electric field, tabulation of material parameters versus electric field is not strictly correct even with slowly varying electric field. Finally, important transport phenomena such as the transport of carrier thermal energy are not included in the conventional drift-diffusion model.

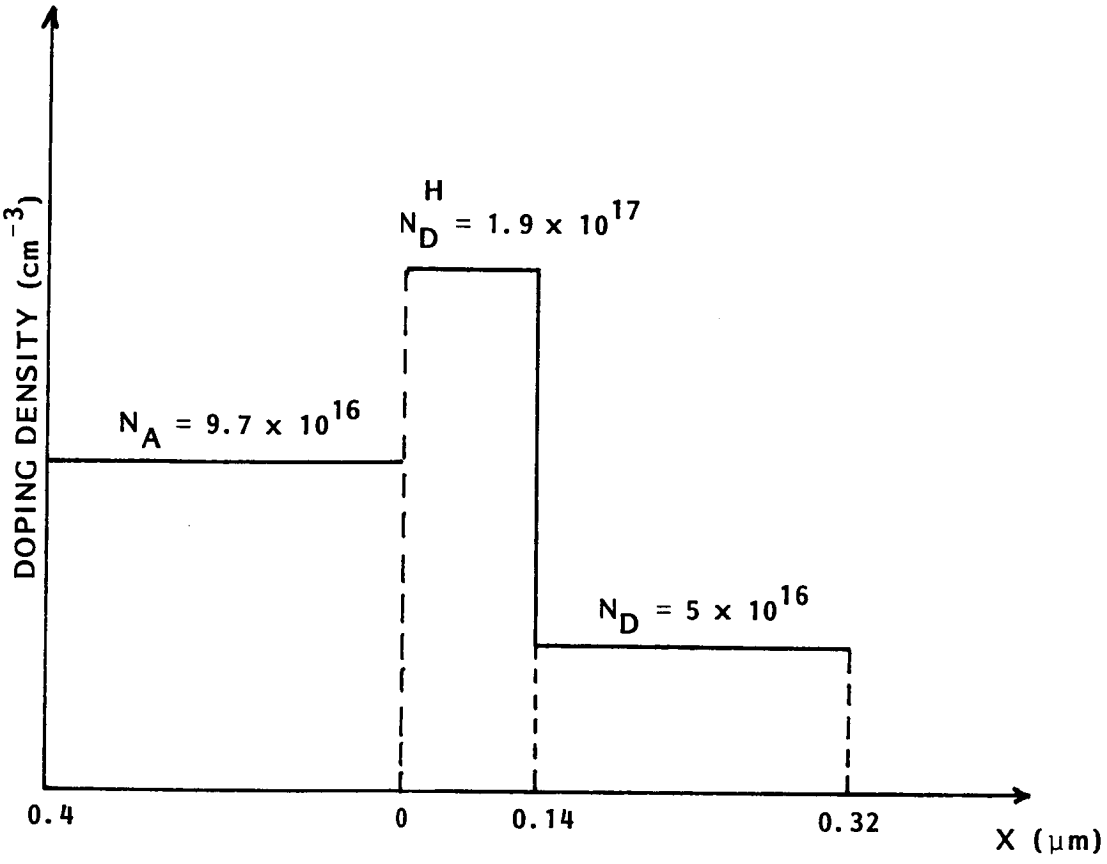

FIGURE 2-6: INITIAL DESIGN OF 60 GHz HDD STRUCTURE

Subsequent to the initial 60 GHz design, Haddad and Mains, at the University of Michigan, developed a more complete model to overcome the deficiencies described above. Using the new model, a revised doping profile (Figure 2.7) for 60 GHz HDD IMPATT diodes was generated. The revised doping profile was received during the early part of 1984.

2.4 Epitaxial Growth Procedure

Substrates used for this program to produce 60 GHz hybrid double-drift HDD IMPATT structures were Si doped N+ GaAs, grown by the horizontal Bridgman technique. They were oriented 2° off the (100) towards the (110) plane with a resistivity of <0.002 ohm-cm. The measured etch pit density on these D-shaped substrates was approximately $5000/cm^2$. The substrates were lapped and chemically polished to a final thickness of 17 mils.

Prior to epitaxial growth, the substrates were etched in 5:1:1 (H_2SO_4:H_2O:H_2O_2), rinsed in DI water, and cleaned in acetone and alcohol. Once cleaned, the substrate was loaded into the multi-tier seed carriage and the latter was positioned in the appropriate growth zone.

Before attempting to grow the entire 60 GHz HDD structure (P^{++}-P-N^{+}-N-N^{++}) in a single growth run, it was necessary to develop growth techniques through several stages, simulating growth parameters for each section of the structure. The parameters of interest included growth time and concentration of injected impurity (ppm) for each layer. The evolutionary stages for N-type growth included the following steps:

a) The growth of an N^{++} buffer layer with a carrier concentration of $2 \times 10^{18}/cm^3$.
b) The sequential growth of an N^{++} buffer/N-active structure.
c) The sequential growth of an N^{++} buffer/N-active/N^{+} avalanche structure.

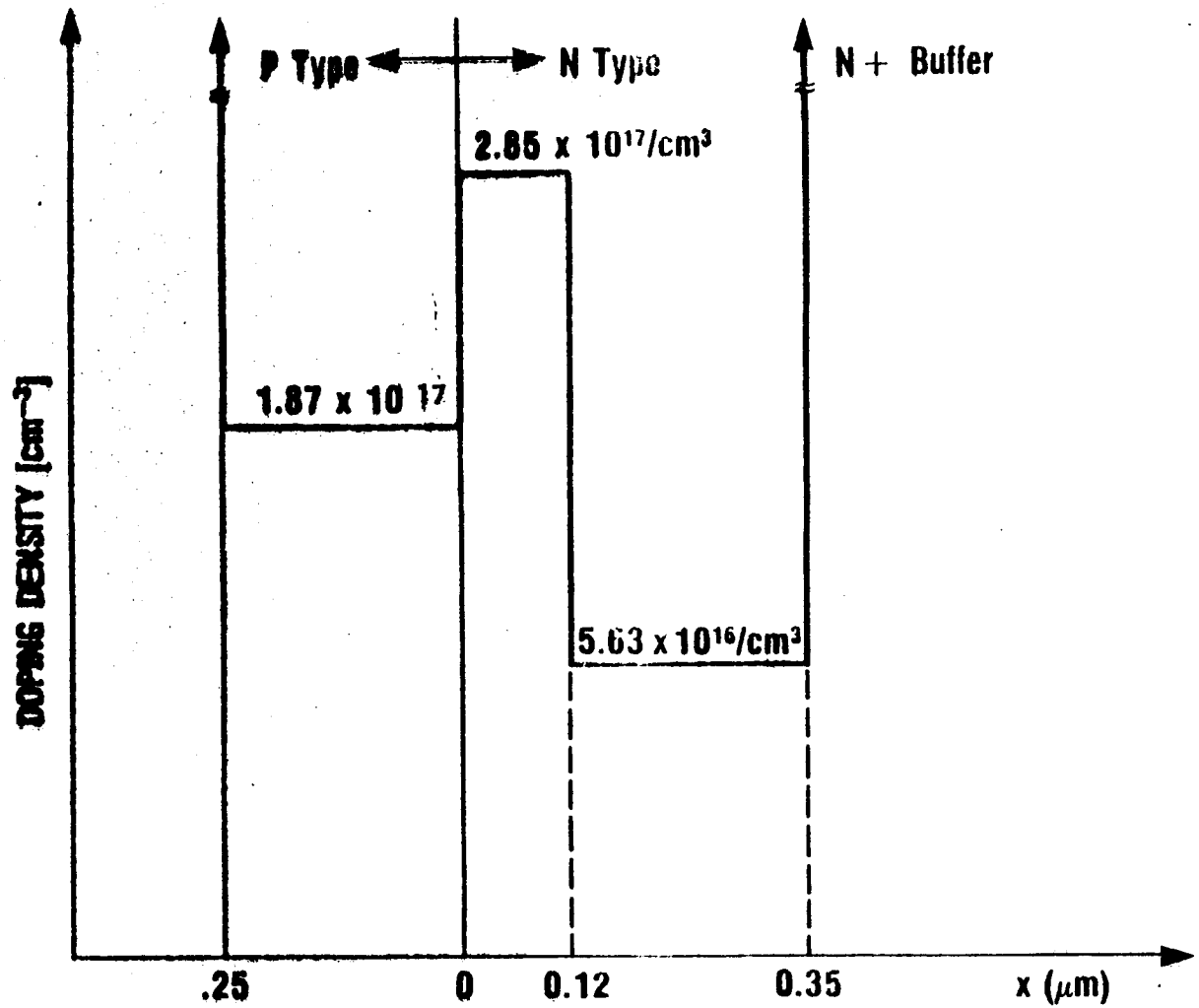

FIGURE 2-7: REVISED DESIGN OF 60 GHz HDD STRUCTURE

As the above stages of epitaxial growth techniques were developed, growth parameters were adjusted so as to achieve uniform doping profiles.

The predictable growth of HI-LO (N^+-N) doping profiles requires an understanding of the relationship between injected silane concentration (ppm) and the resulting epilayer carrier concentration (cm^{-3}). This relationship was determined by performing an N-type calibration growth run. For such a growth run, several layers were deposited sequentially on an N^+ substrate. During the growth of each layer a controlled amount of silane was injected into the reactor.

The multi-layer structure resulting from the N-type calibration growth run was characterized by the conventional differential capacitance-voltage method using a mercury probe. Access to each of the N-layers was made possible by using a 3:1:1 (H_2SO_4:H_2O:H_2O_2) etch. Since the injected concentration of SiH_4 was computed for each of the layers, it was possible to empirically determine the dependence of SiH_4 concentration (ppm) on the doping density of the epilayer. As shown in Figure 2.8, it was possible to grow N-type layers with donor densities ranging from 2 X $10^{15}/cm^3$ to 2.5 X $10^{18}/cm^3$.

After establishing the N-type calibration curve, experimental growth runs were made to fine-tune the growth parameters needed for the N^+-N-N^{++} section of the profiles shown in Figures 2.6 and 2.7. An example of the results obtained from such experimental growth runs is presented in Figure 2.9. The continuous plot of the doping profile shown in Figure 2.9 gives the total thickness of the N^+-N(HI-LO) structure. It also indicates the good N^+-N-N^{++} doping transitions which have been routinely achieved in the new VPE system.

The growth of P-type layers was not as simple and straightforward as that of N-type layers. Unlike the ease in using silane as the source of silicon for the reproducible growth of N-type layers, the contrary was observed with dimethylzinc. Initial experimental growth runs to produce P-type layers centered around the use of DMZ as the source for

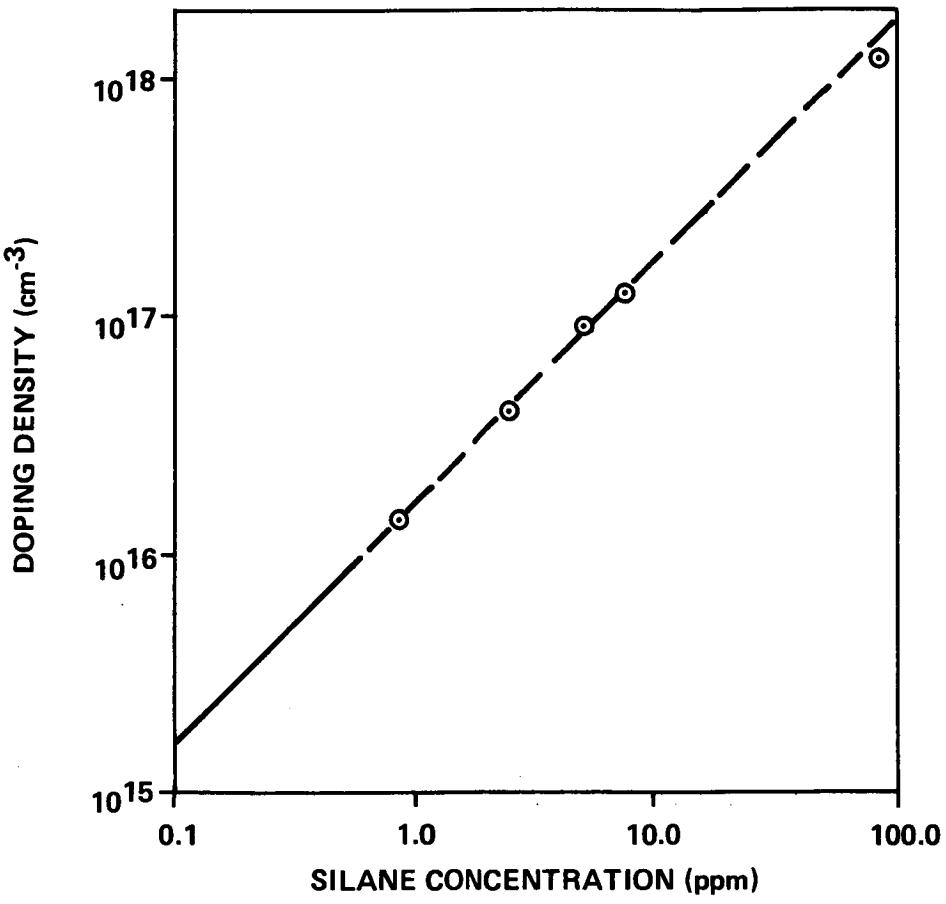

FIGURE 2.8 DONOR DENSITY (cm^{-3}) VERSUS INJECTED SILANE CONTRATION (ppm).

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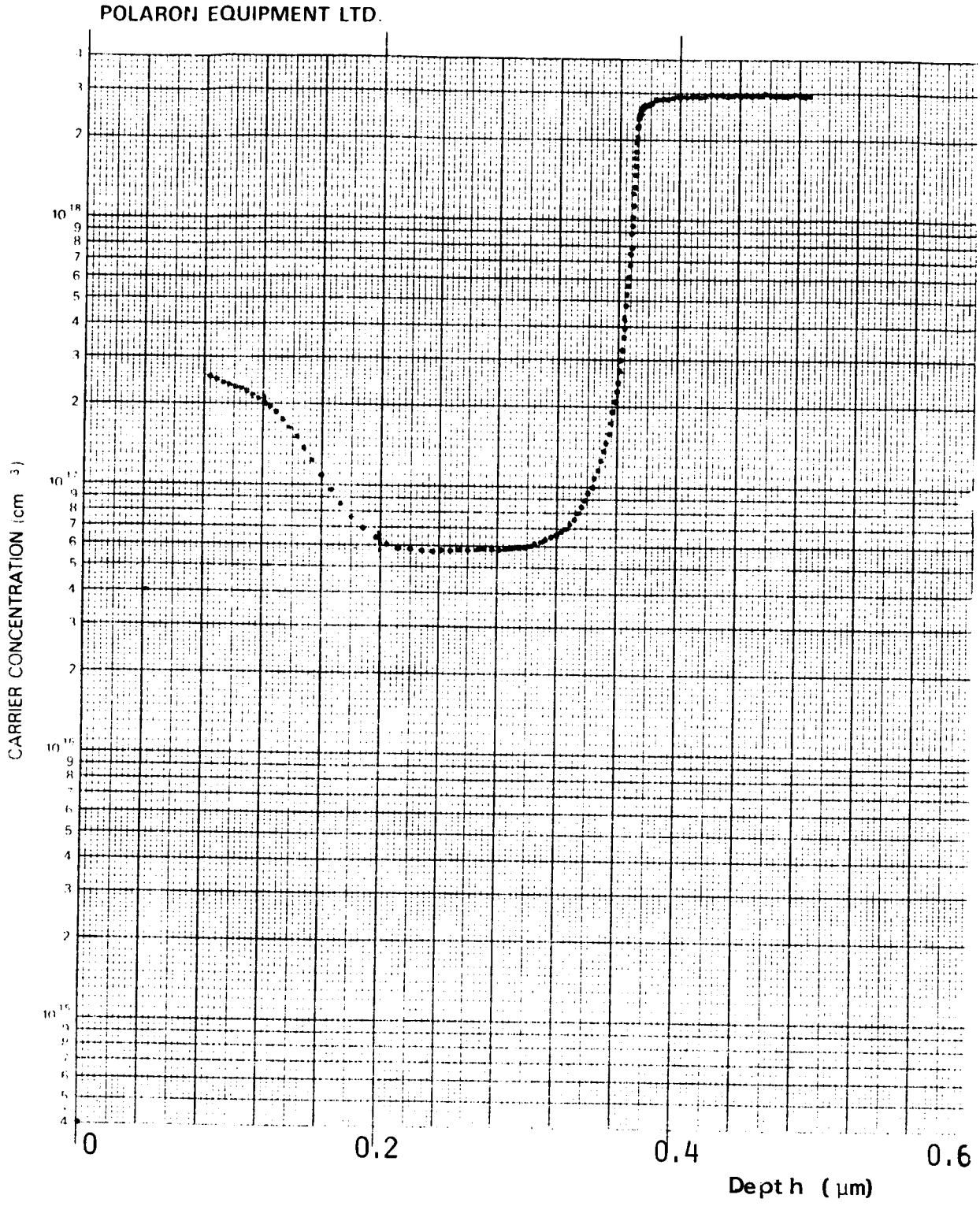

FIGURE 2.9: POLARON PLOT OF N^+ N N^+ STRUCTURE

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P-type dopant. DMZ, diluted with high purity grade hydrogen to a resultant concentration of 210 ppm, was employed during these growth runs. The major successful application of DMZ was towards the reproducible growth of highly doped P^{++} contact layers. These layers were consistently grown with a carrier concentration of 1 X $10^{19}/cm^3$ and a room temperature mobility of 78 cm^2/V-sec. To a lesser extent, the application of DMZ for the growth of lower doped P-type layers was not as successful with respect to reproducibility.

The growth of low doped P-type layers ($<10^{16}/cm^3$) required significant dilution of the as purchased 210 ppm DMZ. The achievement of very low ppm of DMZ (<1 ppm) required mass flow controller (MFC) no. 1, in the P-dilution network (see Figure 2.4), to function in the very low end of its operating range. In this range of operation, MFC no. 1 was unable to allow a controlled amount of concentrated DMZ to enter into the dilution system. Consequently the reproducible growth of low doped N-type layers was impaired.

In order to relax the constraint imposed on MFC no. 1 by the 210 ppm DMZ tank, the latter was replaced by a 55 ppm DMZ tank. With the lower ppm tank, successful attempts were made to grow P-type layers with hole concentration in the 10^{15}-$10^{18}/cm^3$ range. The calibration curve for P-type doping, using the 55 ppm DMZ tank, is shown in Figure 2.10.

While it was possible to generate a P-calibration curve, the results were short lived. Later attempts to grow low doped P-type layers and, furthermore, to reproduce the curve shown in Figure 2.10 were unsuccessful. The "low doped P-type" layers were actually compensated N-type layers. At that time all indications were pointing in the direction of DMZ as being the source of the problem since the reactor system was not disturbed. Furthermore, the growth parameters remained unchanged from those that gave reproducible results.

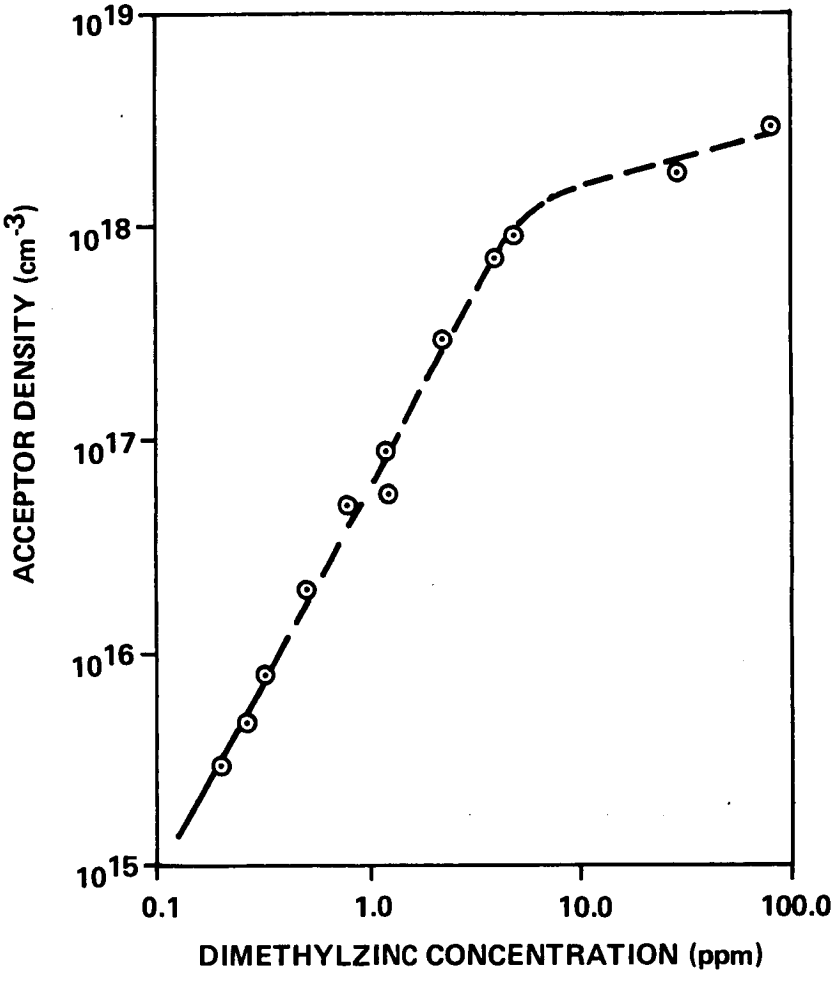

FIGURE 2.10 ACCEPTOR DENSITY (cm^{-3}) VERSUS INJECTED DIMETHYLZINC (DMZ) CONCENTRATION (ppm).

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The nature of the problem encountered with the 55 ppm DMZ tank was thought to be affiliated with its shelf life. The tank was successfully used for approximately two months. Thereafter, a consistent decline in the hole concentration in the epilayer was observed from run to run, while maintaining a constant ppm of injected DMZ. Newer DMZ tanks were explored with unsuccessful results. It was not possible to reproduce any of the initial results achieved with the old tank. Furthermore, most of the attempts resulted in N-type compensated layers.

Based on the results achieved from the first tank of DMZ (low ppm) employed in growing P-type layers, it is apparent that the composition of the gas mixture in the tank was constantly changing and becoming depleted of zinc. This was evidenced by the decline in hole concentration of consecutive growth runs using the same ppm of injected DMZ. The reason for zinc depletion is not understood. However, it is suggested that as DMZ decomposes in the tank, zinc atoms attach themselves to the inner walls of the stainless steel cylinder. As the process continues, more zinc atoms "disappear" leaving behind a cylinder of ethane formed by the combination of methyl radicals.

After recognizing that DMZ was unsuitable for the reproducible growth of P-type layers, a compatible alternate was immediately implemented. The substitute for DMZ was a tank of 66 ppm Diethylzinc (DEZ) to be used as the source for P-type dopant. The success with DEZ was a significant breakthrough in realizing the growth of hybrid double-drift structures. Unlike the case with DMZ, no major problem has been encountered with DEZ since its implementation as a source for zinc.

Immediately after the 66 ppm DEZ tank was installed, several experimental P-type growth runs were made so as to generate a P-calibration curve. The experimental results from such growth runs are presented in Figure 2.11 where hole concentration (cm^3) is plotted against injected concentration of DEZ (ppm). Based on these results, further experimental growth runs were made so as to fine tune the growth parameters necessary to achieve the P-active region of the profiles shown

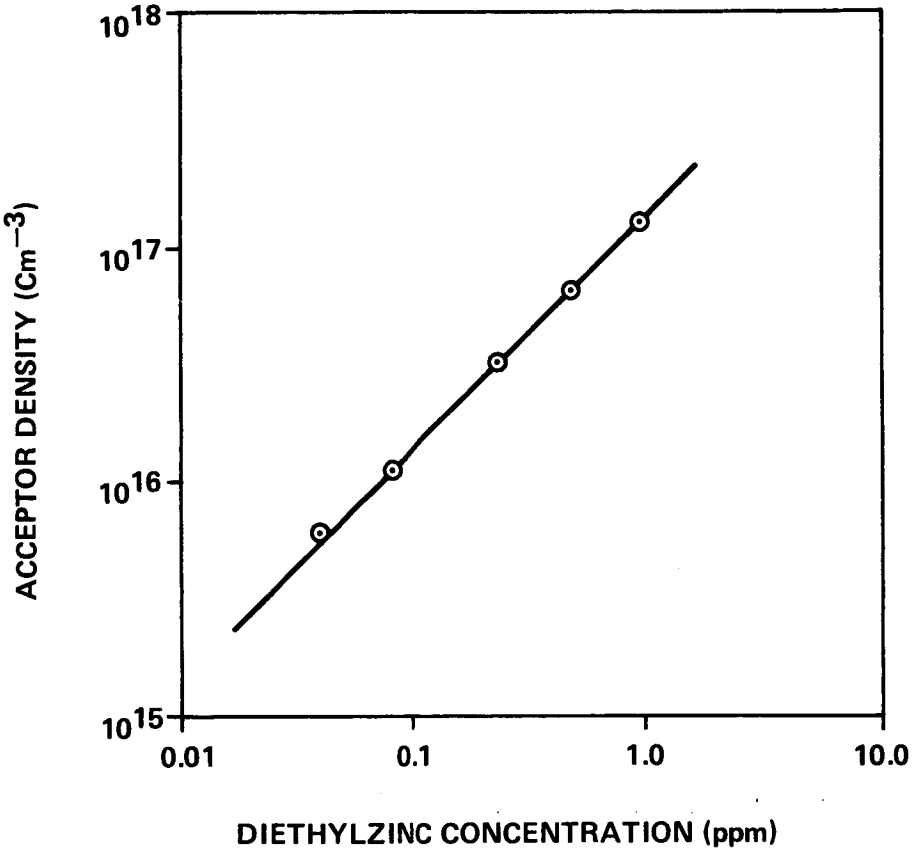

FIGURE 2.11 ACCEPTOR DENSITY (cm^{-3}) VERSUS INJECTED DIETHYLZINC (DEZ) CONCENTRATION (ppm).

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in Figures 2.6 and 2.7. One example of the results from such growth runs is shown in Figure 2.12. The P-layer was intentionally grown thicker than that required so as to observe the flatness of the P-type doping profile and, also, to achieve a more accurate value for its growth rate.

2.5 Growth of 60 GHz HDD Structures

The hybrid double-drift profile of Figures 2.6 and 2.7 consists of five distinct layers, namely: N^+buffer, LO-N active, HI-N avalanche, P-active, and P^{++} contact. The growth of these layers was done sequentially in the order listed above. The preprogrammed steps used for the sequential growth of the five layers are listed in Table 2.1. In order to realize sharp doping transitions, additional steps were incorporated in the automatic growth schedule. Some of these steps included in-situ etch back, purge, and dope-up. The purpose of the first two steps was basically to remove residual dopant gases, while the third was used to condition the reactor tube at the doping level required by the subsequent layer. The positive effects of these additional steps are reflected in the sharp doping transitions as is shown in Figures 2.9.

Subsequent to the separate N and P type simulated growth runs, attempts were made to integrate their calibrated growth parameters so as to achieve a hybrid double-drift structure. After loading a pre-cleaned N^+ substrate into the VPE reactor, the HP1000 system was engaged for automatic control of the entire growth procedure, as listed in Table 2.1. Following the initialize phase, the $AsCl_3$ etch bubbler was switched on so as to vapor etch (in-situ etch) the substrate prior to epitaxial growth.

The third sequence involved the growth of a 2-3um thick N^+ buffer having a carrier concentration of 2-3 X $10^{18}/cm^3$. This high doping density was achieved by directing concentrated silane (80 ppm) into the reactor via the bypass dilution network (see Figure 2.5). During the growth of the N^+ layer, the dilution network was activated, with MFC no. 4 and 5 set at the values required for the subsequent growth of the LO-N

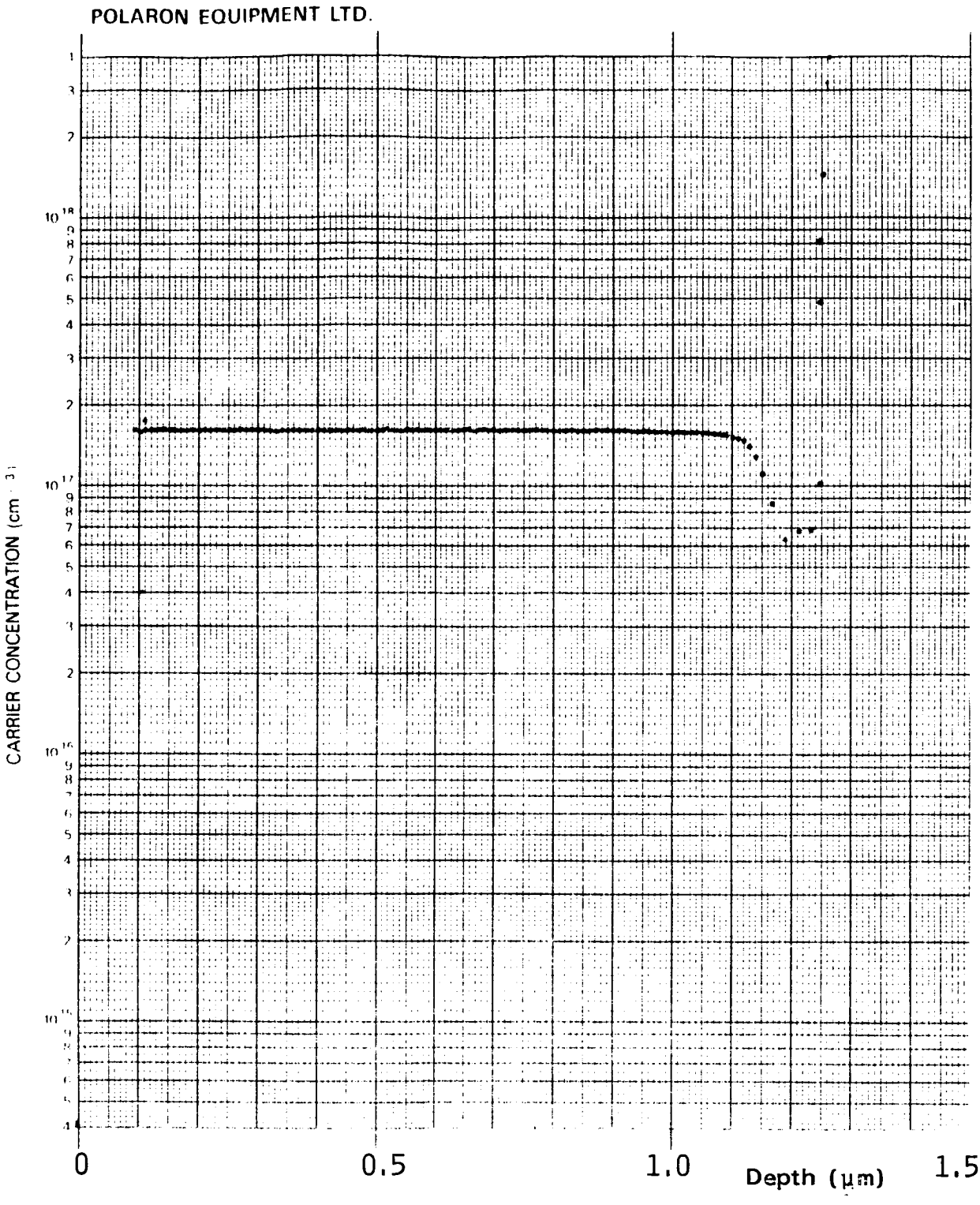

FIGURE 2.12: POLARON PLOT OF P-TYPE LAYER (GROWN ON AN N+ SUBSTRATE)

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TABLE 2.1: AUTOMATIC GROWTH SEQUENCE FOR HDD STRUCTURES

1. INITIALIZE
2. IN-SITU ETCHING
3. N^+ BUFFER
4. N (LO)
5. N (HI)
6. N-TERMINATE
7. P-DOPE UP
8. P-ACTIVE
9. P^+ CONTACT
10. TERMINATE

layer. The established flow in the dilution network was exchanged with that used for the N^+ buffer growth. The advantage of this approach was to minimize the interface width between the N^+ buffer and the LO-N layer. In order to further improve the doping transition between these layers, an in-situ etch back of the N^+ buffer layer was employed.

Following the N-side growth of the HDD structure, a large flow of hydrogen was admitted into the tube, thereby purging it of residual silane. Before growing the P-active layer, DEZ was allowed into the tube so as to condition the region downstream of the 3rd inlet. At the termination of the P-dope up phase, the seed carriage was pulled into the doped region and the growth bubbler switched on. The growth of the P-active layer was followed sequentially by that of the P^{++} contact layer. Finally, the system was purged and the wafer unloaded for characterization.

2.6 Characterization of 60 GHz HDD Structures

2.6.1 Evaluation of Carrier Concentration

The characterization of epitaxial material is an integral part of the epitaxial growth process. A knowledge of the epitaxial doping profile provides a feedback loop which constantly updates the functional characteristics of the growth system. Based on the acquired information, growth parameters can be tailored to meet the specifications of the subsequent doping profile. Additionally, epilayer characterization is essential for selecting material to be submitted for device fabrication.

The characterization of an epitaxial layer begins with an investigation of its impurity distribution. The technique frequently employed for such an investigation is the differential capacitance-voltage (C-V) method on a Schottky diode structure. In certain cases the depth that can be explored by the C-V method is limited by the applied voltage (breakdown voltage) that the depletion layer can

withstand. For these cases, the entire doping profile can be determined by performing a series of step etching in conjunction with C-V measurements. If the step etching process is controlled, the thickness of the epilayer can be determined from a knowledge of the etch rate. Otherwise, the epilayer thickness can be determined by the cleave and stain technique.

In addition to the step etching technique mentioned above, an automatic electrochemical profiler was used to characterize P-type layers. Basically, the automatic system combined electrochemical dissolution with simultaneous differential capacitance measurement in order to provide direct plotting of the doping profile. An example of such direct plotting is shown in Figure 2.12. The structure consist of a P-type layer grown on an N^+ substrate. The continuous profile of Figure 2.12 could not have been obtained by the more conventional solid Schottky barrier method without resorting to a laborious procedure of measurement and chemical step etching.

The automatic electrochemical system was used exclusively for the characterization of N and P-type doping profiles resulting from calibration growth runs. The application of this system for the evaluation of an entire HDD structure was never successful. Most attempts resulted in very distorted profiles in the vicinity of the P-N junction. This distortion can possibly be due to a non-uniform etch rate of the P-type material, causing some to remain as the HI-N layer is profiled.

All HDD doping profiles were investigated using the conventional step etching technique on evaluation pieces that were cleaved from the original epitaxial wafers. From an evaluation piece, the P^+ contact layer (~1um) was chemically removed using a 3:1:1 etch. The etch rate was typically 3um/min. As the P-N junction was approached, a slower etch was employed so as to safeguard against excessive removal of the N-type material. The composition of the slower etch was 2.8 H_2O_2:8NH_4OH:400H_2O and its etch rate was determined to be 0.2um/min.

The main objective of the above step etching procedure was to determine accurately the N-type HI-LO doping profile. Using another evaluation piece from the original epitaxial wafer, single mesa test diodes were defined and C-V measurements were taken so as to yield an effective doping profile of the HDD structure (see Figure 2.13). Based on the effective doping profile (from mesa evaluation) and a knowledge of the HI-LO doping profile (via step etching), it was possible to determine the carrier concentration of the P-active layer using the relationship:

$$1/N_{eff} = 1/P + 1/N$$

where

N_{eff} = effective carrier concentration (cm^{-3})
N = Net donor carrier concentration (cm^{-3})
P = Net acceptor carrier concentration (cm^{-3})

Using the growth and characterization techniques described above, several 60 GHz HDD structures were grown in the large bore H-VPE system. The HDD structures that were fully evaluated and submitted for processing are listed in Table 2.2 (see Section 6.2 for RF test results). The tabulation presented in Table 2.2 was acquired via C-V/step etching measurements and mesa diode evaluation.

2.6.2 Thickness Evaluation

As shown in the design profiles of Figures 2.6 and 2.7, the thickness of the individual layers involved in a 60 GHz HDD structure are sub-micron in nature. In order to accurately determine the thickness of each grown layer, it was necessary to use a scanning electron microscope (SEM). The latter provided much high resolution and magnification when compared with an optical microscope.

Samples from each 60 GHz epitaxial wafer were cleaved and the layers were delineated using the following formulation:

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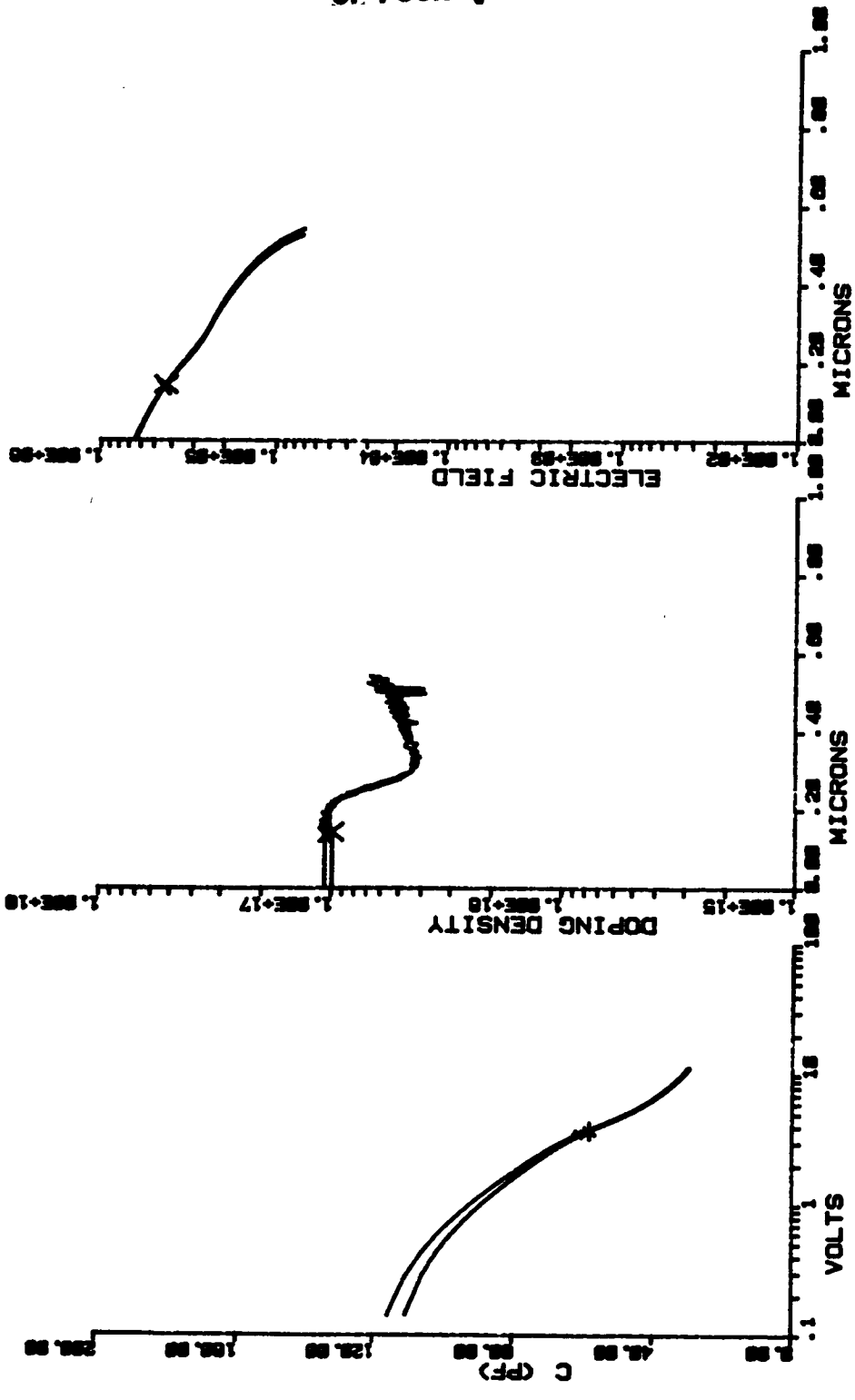

FIGURE 2.13: Composite Doping Profile for 60 GHz HDD Structure.

TABLE 2.2: 60 GHz HYBRID DOUBLE-DRIFT WAFERS.

Wafer No.	CV Measurement Via Step Etching+ N-LO(cm^{-3})	CV Measurement Via Step Etching+ N-HI(cm^{-3})	Effective Doping* From Mesa Evaluation HI(cm^{-3})	Effective Doping* From Mesa Evaluation LO(cm^{-3})	Calculated Doping of P-Layer (cm^{-3})	Breakdown Voltage (Volts)
I10292	8.6×10^{16}	3.2×10^{17}	9×10^{16}	3.5×10^{16}	$1,2 \times 10^{17}$	13
I10293	1.0×10^{17}	3.4×10^{17}	1.5×10^{17}	7×10^{16}	2.6×10^{17}	11
I10294	5.4×10^{16}	1.7×10^{17}	8×10^{16}	3×10^{16}	1.5×10^{17}	16
I10296	3.8×10^{16}	1.4×10^{17}	6×10^{16}	2.3×10^{16}	1×10^{17}	19
I10297	3.7×10^{16}	1.5×10^{17}	7.5×10^{16}	2.3×10^{16}	1.5×10^{17}	18
I10298	7×10^{16}	1.9×10^{17}	1×10^{17}	4.2×10^{16}	2×10^{17}	14
I10300	5.2×10^{16}	1.5×10^{17}	9×10^{16}	5.5×10^{16}	2.2×10^{17}	13
I10301	5.2×10^{16}	1.6×10^{17}	1×10^{17}	5×10^{16}	2.6×10^{17}	14
I10304	5.1×10^{16}	1.9×10^{17}	1×10^{17}	4.3×10^{16}	2×10^{17}	16
I10305	6×10^{16}	1.9×10^{17}	9×10^{16}	4.7×10^{16}	1.7×10^{17}	15
I10306	4.6×10^{16}	1.7×10^{17}	9×10^{16}	4×10^{16}	1.9×10^{17}	16
I10307	4.5×10^{16}	1.8×10^{17}	9.5×10^{16}	5×10^{16}	2×10^{17}	16
I10396	5.6×10^{16}	2.8×10^{17}	1.0×10^{17}	3.6×10^{16}	1.6×10^{17}	---

+ Etch Composition

(1) slow etch (approx. 0.2 m/min)- 2.8:008:400 (H_2O_2:NH_4OH; H_2O)

(2) fast etch (approx. 3 m/min)- 5:1:1 (H_2SO_4:H_2O_2:H_2O)

*: $1/N_{eff} = 1/N + 1/P$

1 g $K_2Fe(CN)_6$ in 50ml H_2O
12ml NH_4OH in 36ml H_2O

mixed in a 2:1 ratio before use.

Initially, samples were mounted in the SEM and raster scan measurements were done with the samples positioned at 90° with respect to the electron beam (no tilt angle). Using this mode of operation, it was often difficult to identify the individual layers. This situation was resolved by inclining the sample to the electron beam. The optimum tilt angle was determined to be 35°. Photomicrographs of a sample measured with no tilt and a tilt angle of 35° are shown in Figures 2.14 and 2.15, respectively. The latter case, where the individual layers are distinguishable, can be attributed to an increase in the yield of secondary electrons when the sample is inclined to the electron beam.

The micrograph shown in Figure 2.15 was obtained by raster scanning the sample with the electron beam. Using this scanning technique, errors resulted in epilayer thickness due to the width of the lines separating the layers. To minimize these errors, a line scan was performed on the same sample. This technique gave sharp peaks that corresponded to doping transitions (see Figure 2.16). The distance between any two peaks corresponded to the thickness of the epilayer. Figure 2.17 shows the relationship between the line and raster scans.

Using the above techniques, it was possible to evaluate epilayer thickness for all 60 GHz HDD epitaxial wafers. Table 2.3 gives the thickness for N, P, and P^+ layers as measured using a scanning electron microscope.

2.7 Doping and Thickness Uniformity

The large bore H-VPE system was designed and characterized to grow very uniform epilayers on several large area substrates per growth run. The advantage of establishing such a system is

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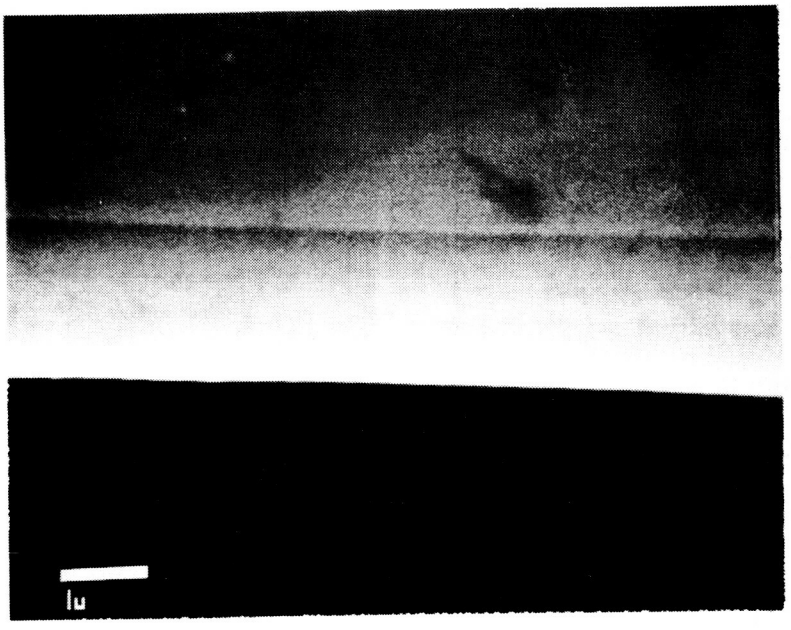

FIGURE 2.14 SEM RASTER SCAN OF 60 GHz HDD CLEAVED CROSS-SECTION. NO TILT ANGLE.

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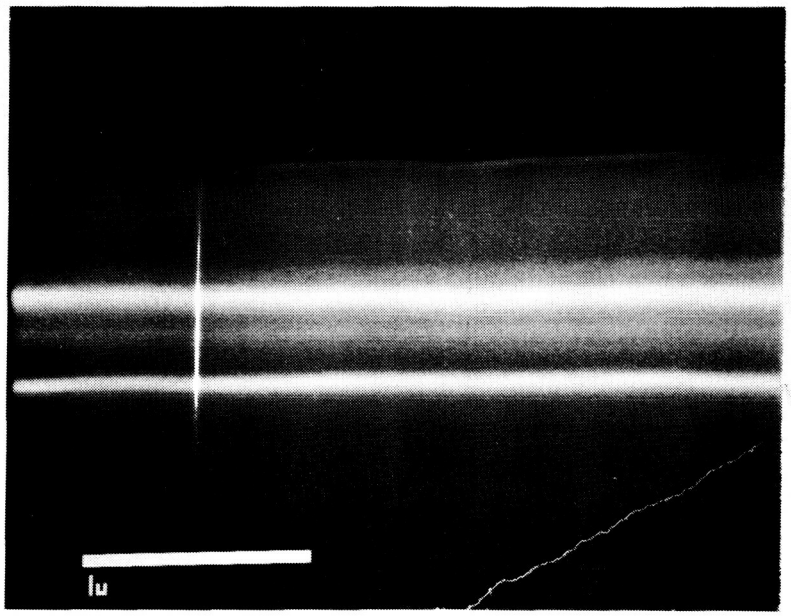

FIGURE 2.15 SEM PHOTOMICROGRAPH OF 60 GHz HDD CLEAVED CROSS-SECTION. TILT ANGLE = 35°

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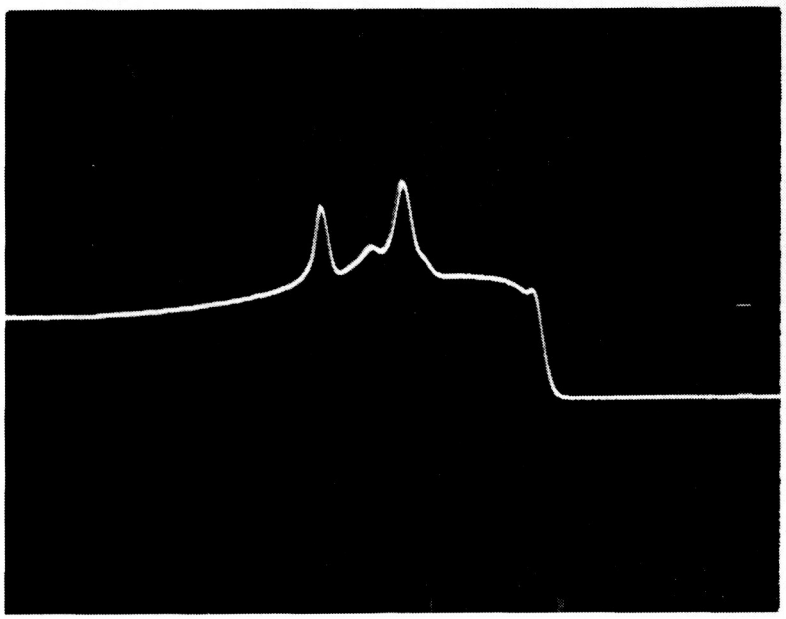

FIGURE 2.16 SEM LINE SCAN OF 60 GHz HDD CLEAVED CROSS-SECTION.

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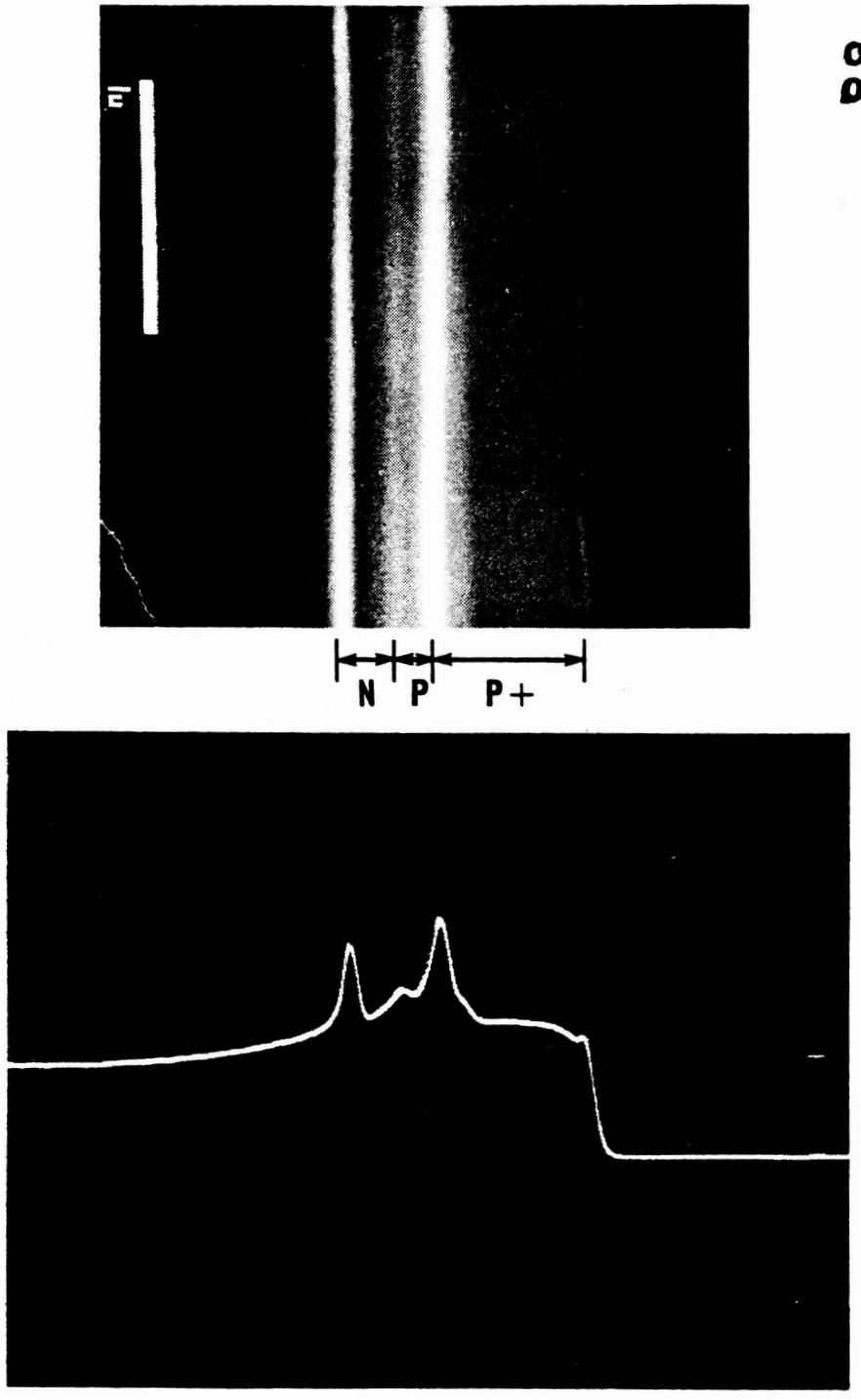

Figure 2.17 RELATIONSHIP BETWEEN SEM RASTER AND LINE SCANNING

TABLE 2.3: SEM THICKNESS DATA FOR 60 GHz HDD EPITAXIAL WAFERS GROWN IN LARGE BORE H-VPE SYSTEM.

	THICKNESS (μm)		
RUN NO.	N(HI/LO)	P-ACTIVE	P+ CONTACT
I10292	0.35	0.18	0.96
I10293	0.42	0.28	1.0
I10294	0.27	0.18	1.2
I10296	0.34	0.21	1.0
I10297	0.38	0.35	1.0
I10298	0.30	0.15	1.2
I10300	0.36	0.24	1.0
I10301	0.32	0.21	1.0
I10304	0.34	0.26	1.2
I10305	0.57	0.36	1.02
I10306	0.28	0.16	0.84
I10307	0.27	0.29	1.07
I10396	0.36	0.26	1.0

very significant for a development program like 60 GHz Hybrid Double-Drift IMPATTs. Because the 60 GHz HDD epitaxial structure is very complex, much of the original sample can be consumed in the process of evaluating the individual layers. Growing very uniform HDD structures on large area substrates (or several substrates per growth run) allows for a reasonable amount of material to be processed. Furthermore, various processing techniques can be applied to individual pieces from a growth run so as to determine their impact on device performance.

In order to produce highly uniform epitaxial layers on large area substrates it is necessary to adopt a growth process such that the deposition mechanism is kinetically controlled. For growth in the kinetically controlled region, a low deposition temperature (<700°C) is employed and the growth process is controlled by some slow surface process such as absorption and desorption. Depending on the deposition temperature, an optimum $AsCl_3$ mole fraction exists where high epitaxial uniformity can be achieved.

For the large bore H-VPE system, a deposition temperature of 700°C was chosen. The flow conditions were established by extrapolating those that proved successful in M/A-COM's small bore (2" dia.) reactors. The range of $AsCl_3$ mole fraction that was explored for optimum doping and thickness uniformities was 4.1×10^{-3}-5.4×10^{-3}. The value of the $AsCl_3$ mole fraction was varied by adjusting the temperature of the growth bubbler. The optimum $AsCl_3$ mole fraction was determined to be 4.6×10^{-3}.

Using the multi-tier seed carriage and optimized growth parameters such as:

Source temperature	= 760°C
Seed temperature	= 700°C
Total flow rate	= 1140 sccm
$AsCl_3$ mole fraction	= 4.6×10^{-3}

we have repeatedly demonstrated very good doping and thickness uniformity in the large bore H-VPE system.

With respect to across-slice (20 cm^2) uniformity, we have consistently grown layers with doping and thickness uniformity of 4 percent and 8 percent, respectively. The doping uniformity was determined by C-V profiling, and the layer thickness was evaluated on cleaved and stained cross-sections.

The results for slice-to-slice doping variations are shown in Figures 2.18(a) thru 2.18(f). Based on the results presented there (for 6 wafers at $20cm^2$ each per growth run), the doping variation was determined to be 10 percent. The thickness distributions on $120cm^2$ of epitaxial material per growth run are tabulated in Table 2.4. Using the tabulated results of Table 2.4, the total thickness variation was determined to be 16 percent.

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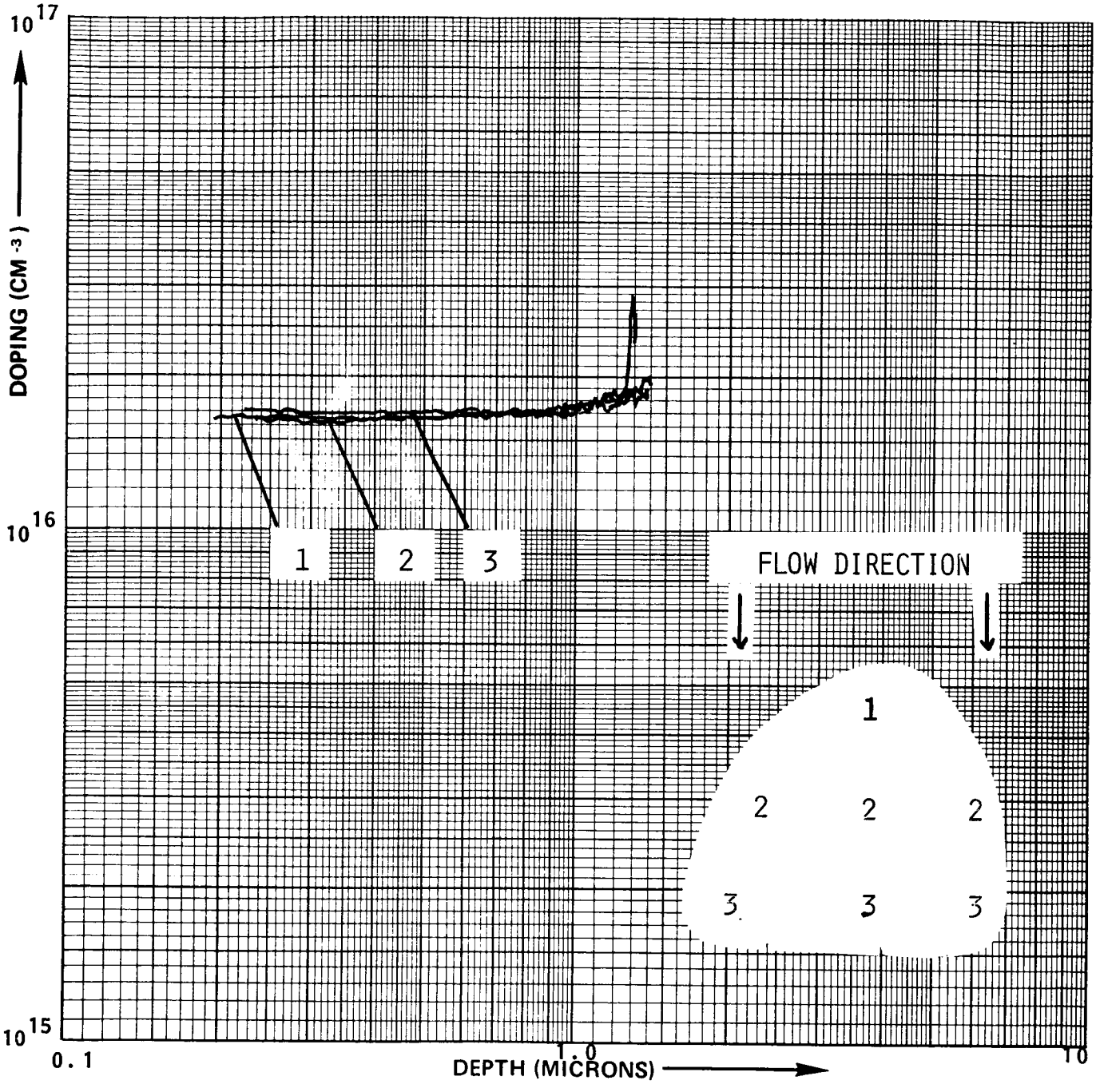

FIGURE 2.18(a) THE DOPING DISTRIBUTION OF EPITAXIAL LAYER GROWN IN TIER #1 OF MULTI TIER SEED CARRIAGE.
AREA OF EPITAXIAL WAFER $\approx 20 cm^2$.

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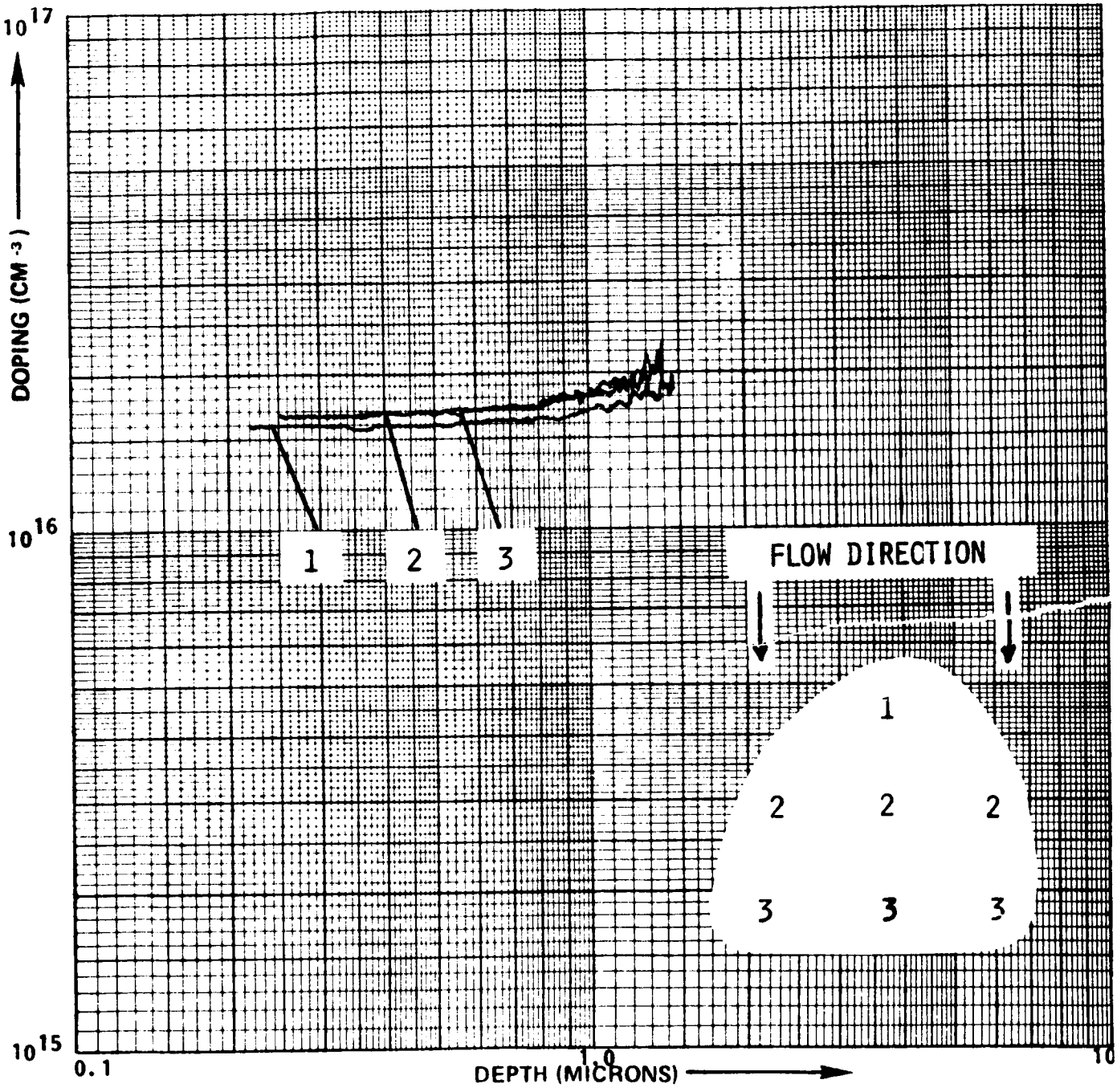

FIGURE 2.18 (b) THE DOPING DISTRIBUTION OF EPITAXIAL LAYER GROWN IN TIER #2 OF MULTI TIER SEED CARRIAGE.
AREA OF EPITAXIAL WAFER $\approx 20 cm^2$.

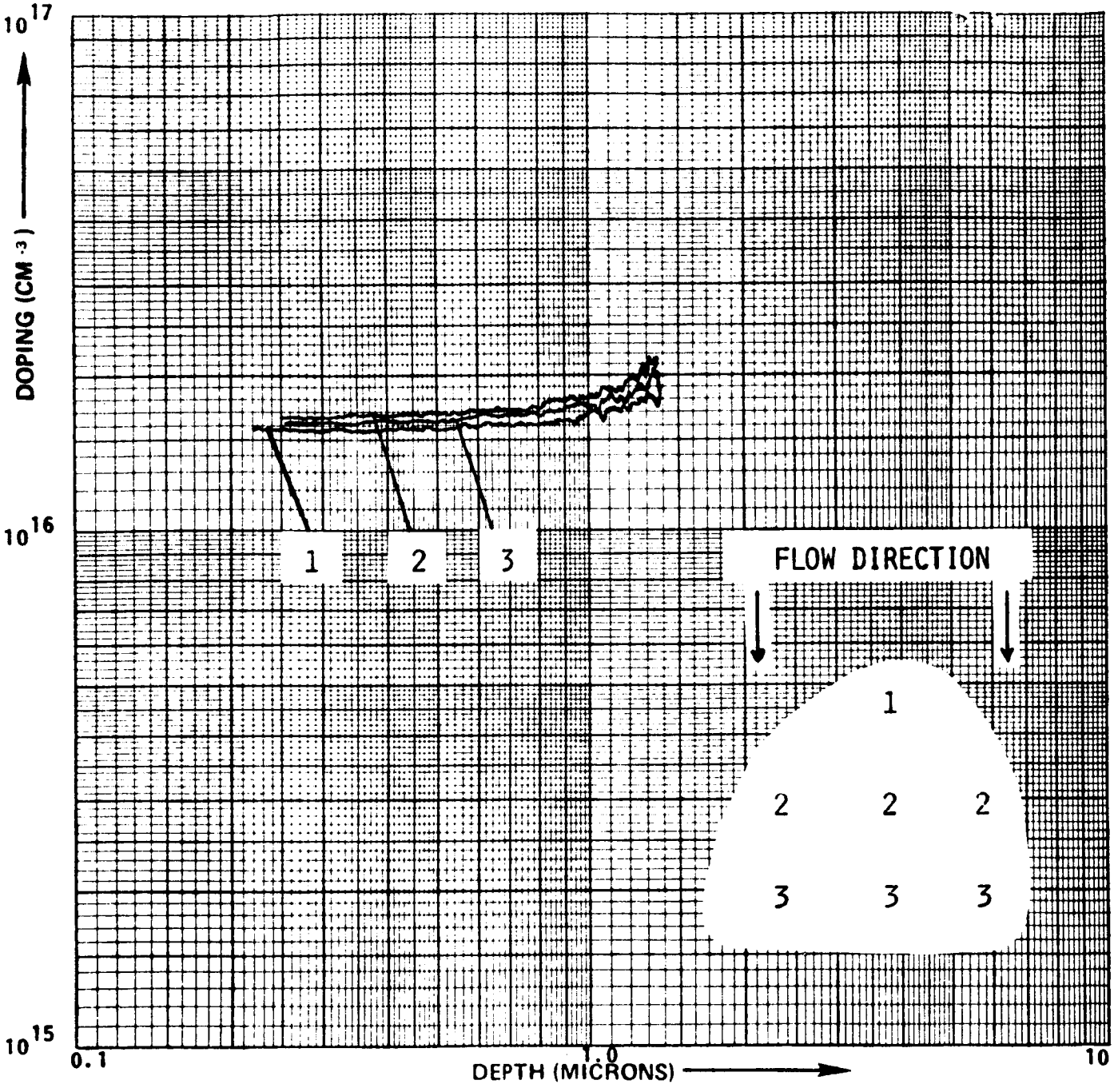

FIGURE 2.18(c) THE DOPING DISTRIBUTION OF EPITAXIAL LAYER GROWN IN TIER #3 OF MULTI TIER SEED CARRIAGE.
AREA OF EPITAXIAL WAFER ≈20cm^2.

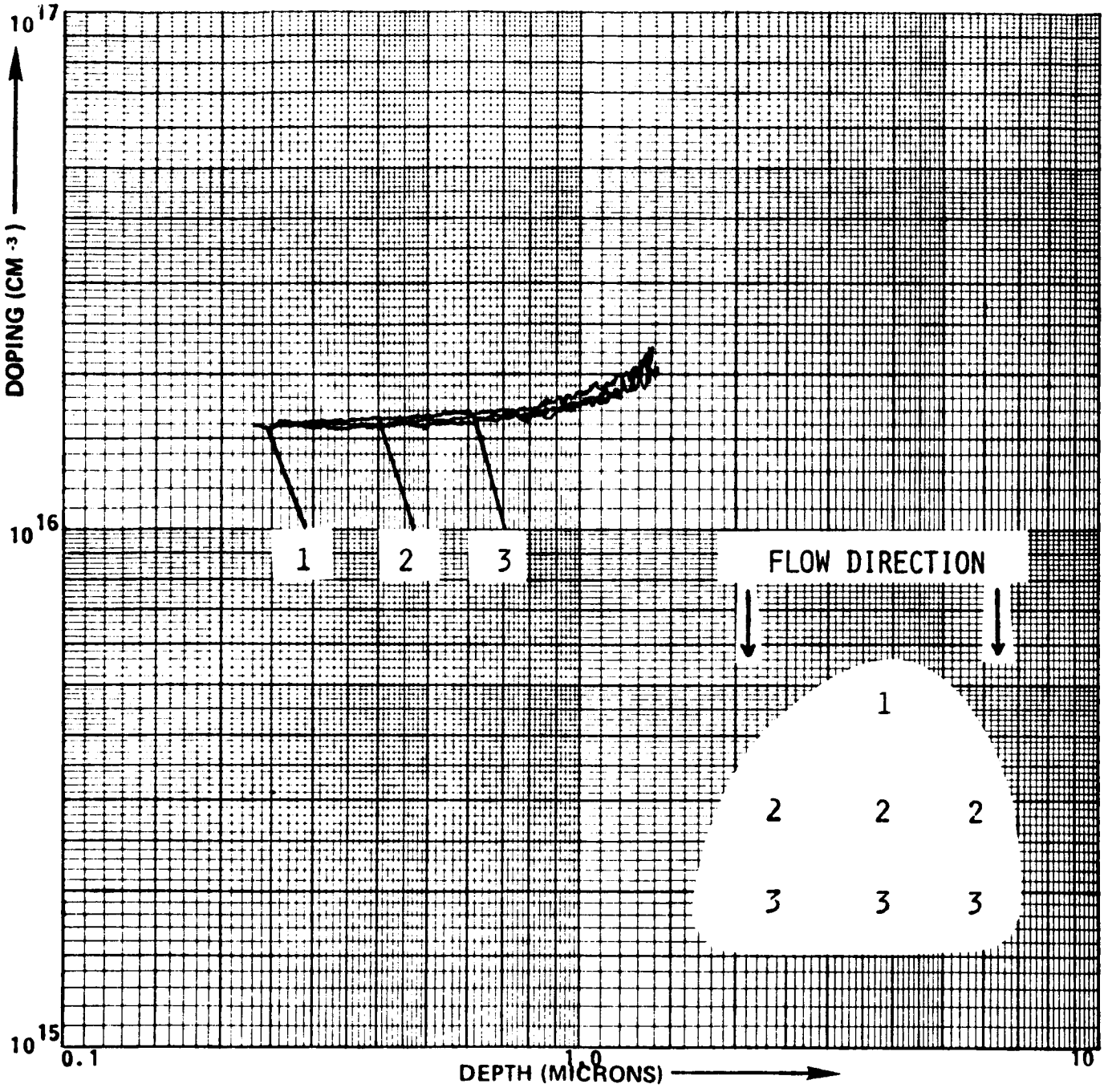

FIGURE 2.18(d) THE DOPING DISTRIBUTION OF EPITAXIAL LAYER GROWN IN TIER #4 OF MULTI TIER SEED CARRIAGE.
AREA OF EPITAXIAL WAFER ≈20cm^2.

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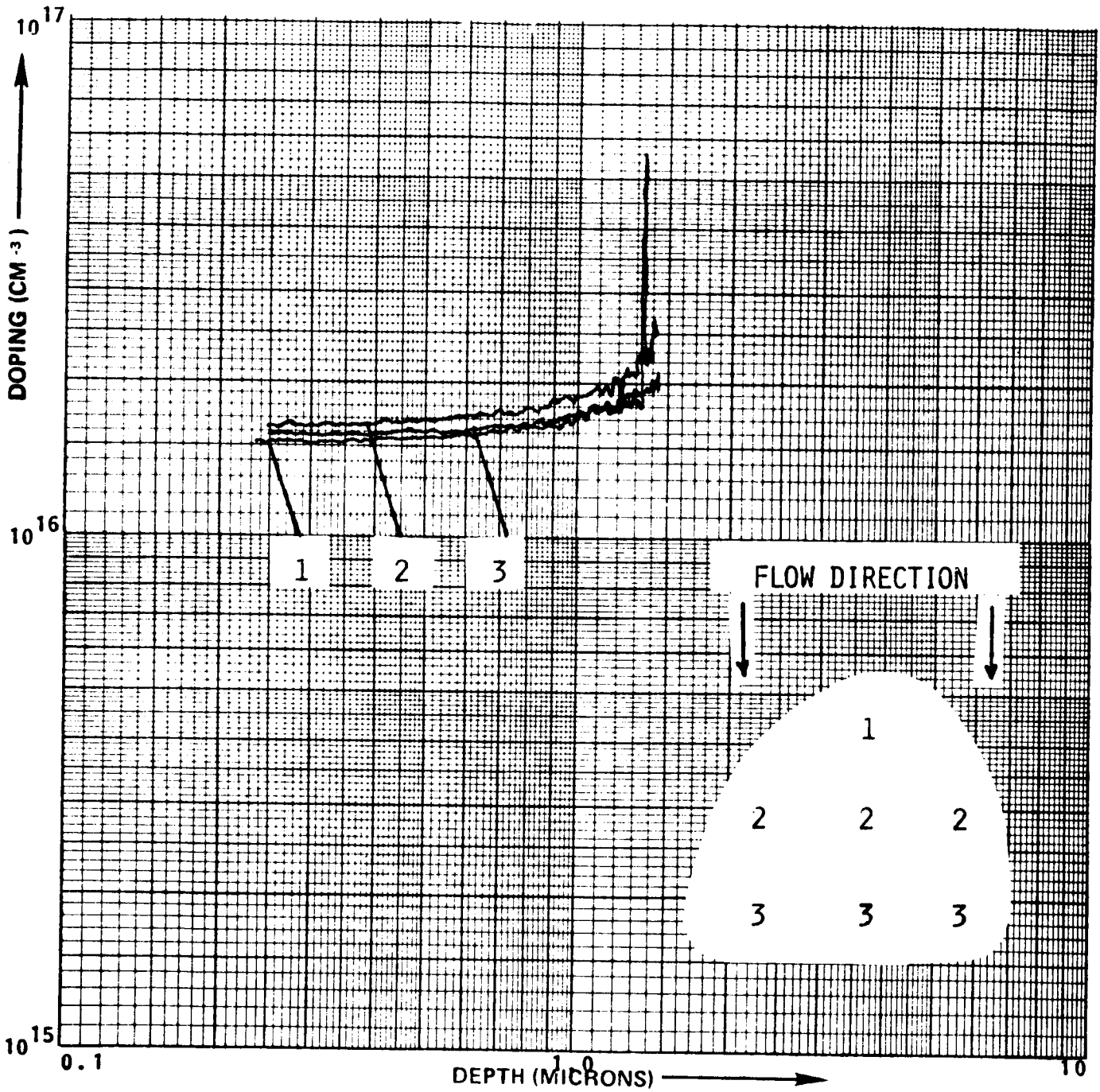

FIGURE 2.18.(e) THE DOPING DISTRIBUTION OF EPITAXIAL LAYER GROWN IN TIER #5 OF MULTI TIER SEED CARRIAGE.
AREA OF EPITAXIAL WAFER ≈20cm^2.

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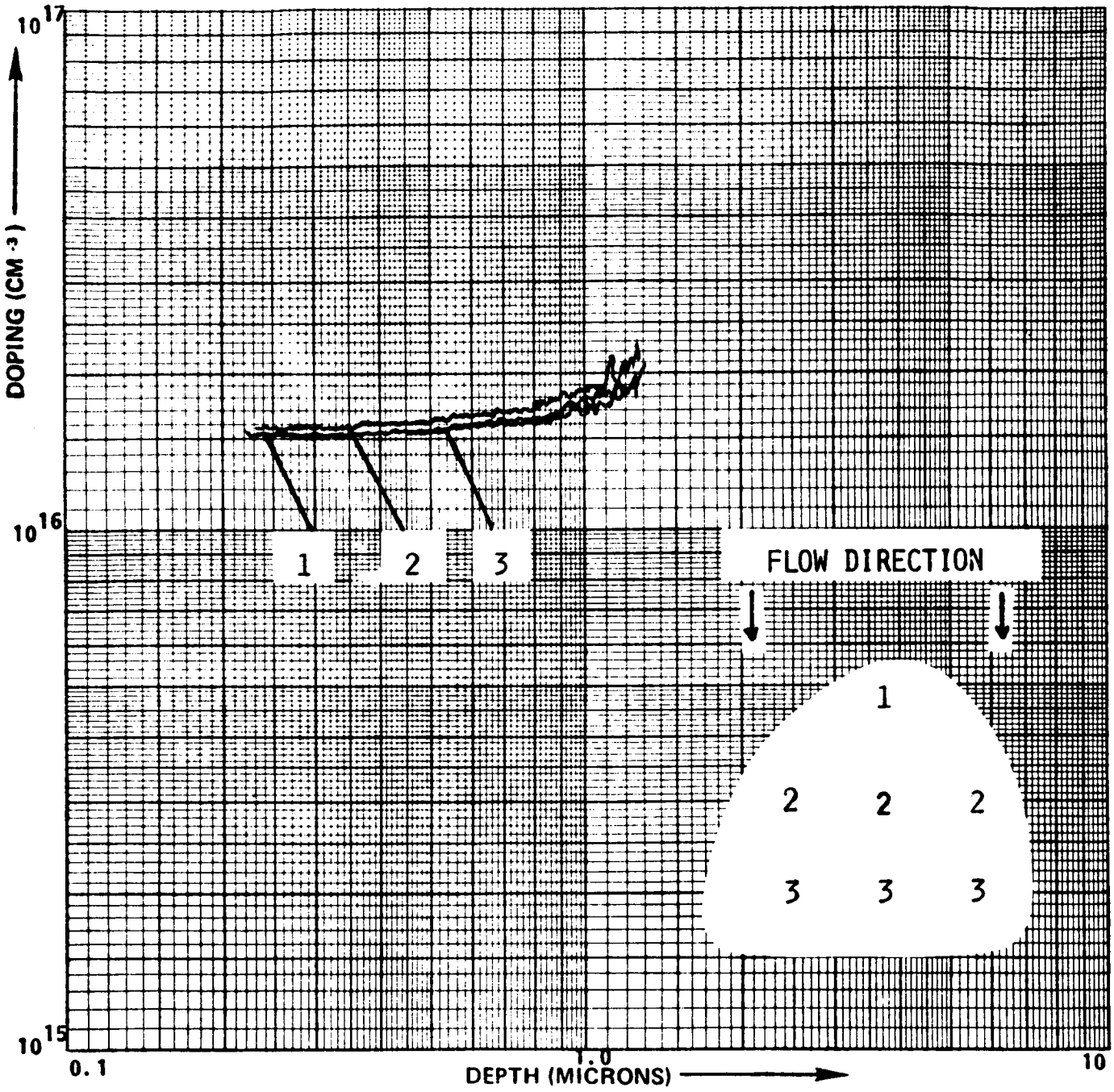


FIGURE 2.18(f) THE DOPING DISTRIBUTION OF EPITAXIAL LAYER GROWN IN TIER #6 OF MULTI TIER SEED CARRIAGE.
AREA OF EPITAXIAL WAFER $\approx 20 cm^2$

TABLE 2.4: THICKNESS DATA FOR EPILAYERS GROWN IN THE SIX-TIER SEED CARRIAGE.

	THICKNESS (μm)				
Tier#	Position 1 (or upstream)	Position 2 (or center)	Position 3 (or downstream)	Mean Thickness	Δt/ tier %
1	2.99	2.87	2.74	2.87	8.7
2	2.85	2.66	2.60	2.70	9.2
3	2.77	2.55	2.61	2.64	8.3
4	2.77	2.57	2.63	2.66	7.5
5	2.76	2.56	2.62	2.65	7.5
6	2.84	2.64	2.70	2.73	7.3

SECTION 3

ORGANO-METALLIC CHEMICAL VAPOR DEPOSITION (OMCVD or MOCVD)

3.0 INTRODUCTION

During the term of this contract, considerable progress was made toward the realization of OMCVD as an epitaxial growth technology capable of producing structures for 60 GHz Double-drift IMPATT diodes. Many epitaxial growth experiments were performed during this period under a wide variety of conditions, including: different reactor geometries, flow rates, material concentrations and temperatures. In addition, several important modifications and design improvements were incorporated into the OMCVD system. The current OMCVD system had evolved from two geometric reconfigurations and one complete reconstruction which finally contributed to its usefulness in relation to the growth of millimeter wave structures in GaAs. Several of the device structures, which were grown during this period, were determined to be sufficiently close to the theoretical model so as to merit processing into functional diodes. Results based on these diodes, although encouraging, fell short of the ultimate goals of this program. The best RF performance results were obtained from devices fabricated from material grown in the OMCVD system.

3.1 Background

In recent years, the interest in OMCVD as an epitaxial growth technology has increased at an unprecedented rate. Since the first reported growth of GaAs by OMCVD, dating back as far as 1968, considerable progress has been made in the development of this growth technology. OMCVD has received wide recognition as having the capacity to grow high quality device oriented epitaxial structures with background carrier concentrations of 1E14 cm^{-3} and liquid nitrogen mobilities in excess of 135,000 $cm^2/V\text{-}Sec$. This technology has demonstrated the potential of being a viable alternative to the more widely used halide VPE systems.

As an epitaxial growth technology for GaAs devices, OMCVD has several unique and inherent advantages over the more established

halide vapor phase epitaxy, (H-VPE), and liquid phase epitaxy, (LPE), technologies. Presently, the microwave performance of advanced devices such as GaAs MESFET's as well as conventional millimeter wave devices have evidenced comparable or even superior electrical properties to those grown by the H-VPE systems.

In comparison, the appeal to OMCVD over H-VPE, is due to its straight forward chemistry and availability of a vapor phase source of gallium and arsenic reactants to be readily transported in the gas stream. The flux of gallium and arsenic reactants from the trimethylgallium, (TMGa), and arsine, (AsH3), sources require no in-situ formation reaction. It is precisely for these reasons that OMCVD is considered to be extremely attractive as a production tool.

A common design for an OMCVD reactor typically uses a lower growth temperature, a significantly higher gas flow velocity and the growth reaction occurs in an inductively coupled RF heated cold wall system. A system configuration of this type would inhibit the premature decomposition of transport reactants as well as minimize the presence of outgassing impurities from the quartz walls of the reaction chamber. The growth reaction in OMCVD is commonly viewed as an irreversible, surface catalyzed pyrolisis that is relatively independent of growth temperature and substrate orientation. The dynamics of the growth reaction in the 600°C-800°C temperature range occurs in the mass-transport-limited region where the concentration of gallium flux is the limiting specie for growth. The degree of precision in controlling the thickness of each grown layer is dependent upon the linear nature of the growth rate as a function of the mole fraction of TMGa. The sharpness of an interface, or the abruptness of a transition between varying doping levels, is largely influenced by the manner in which a system is configured and operated.

One of the major limitations in achieving high quality epilayers has been the inconsistent purity of the starting materials. Empirically, it has been shown that the electrical properties of the GaAs epilayers will vary when source materials from different vendors are used.

Even from the same vendor, the lot to lot variations of the arsine and trimethylgallium quality has evidenced strong effects on the baseline background doping of the unintentionally doped epilayers. This problem, in time, will be addressed. As the interest in this technology increases so will the need for higher quality materials.

3.2 System Design, Growth Experiments, and Material Characterization

The initial experiments were conducted in a small bore reaction chamber with a susceptor which was sharply angled with respect to the gas stream. A schematic of this reaction chamber is shown in Figure 3.1. The susceptor in this reactor was capable of holding a sample approximately 3cm X 4.5cm. However, due to its shape, uniform heating could only be obtained over an area of about 2cm X 2.5cm which was located near the downstream end. Due to these effects, it was determined that all further work with this reactor should be done using only the area of the susceptor which was evenly heated so as to eliminate the effects of a non-uniform temperature distribution.

In order to gain experience with the growth parameters of the reactor, relatively thick (1 to 3 microns) layers were grown without any intentional impurity doping. The results of these experiments indicated that for a wide range of total flow rates (3 slm to 10 slm of hydrogen), there remained a large degree of non-uniformity in layer thickness over the limited area used. Non-uniformities of up to +/- 70% were observed with the thickest portion of the layer always occurring in the center of the wafer. This result suggested that a jet of high velocity gas was forming in the reactor causing a hydrodynamically uneven distribution of reactant flux.

In order to remedy this situation a baffle was constructed and placed immediately downstream from the reactant entry port. This baffle, shown schematically in Figure 3.2, served to break up the flow stream lines and helped to form a laminar flow condition upstream of the susceptor. With the baffle installed in the reactor, layers grown under the same conditions used previously now exhibited much better uniformity in thickness; on the order to +/- 20%. All further experiments were

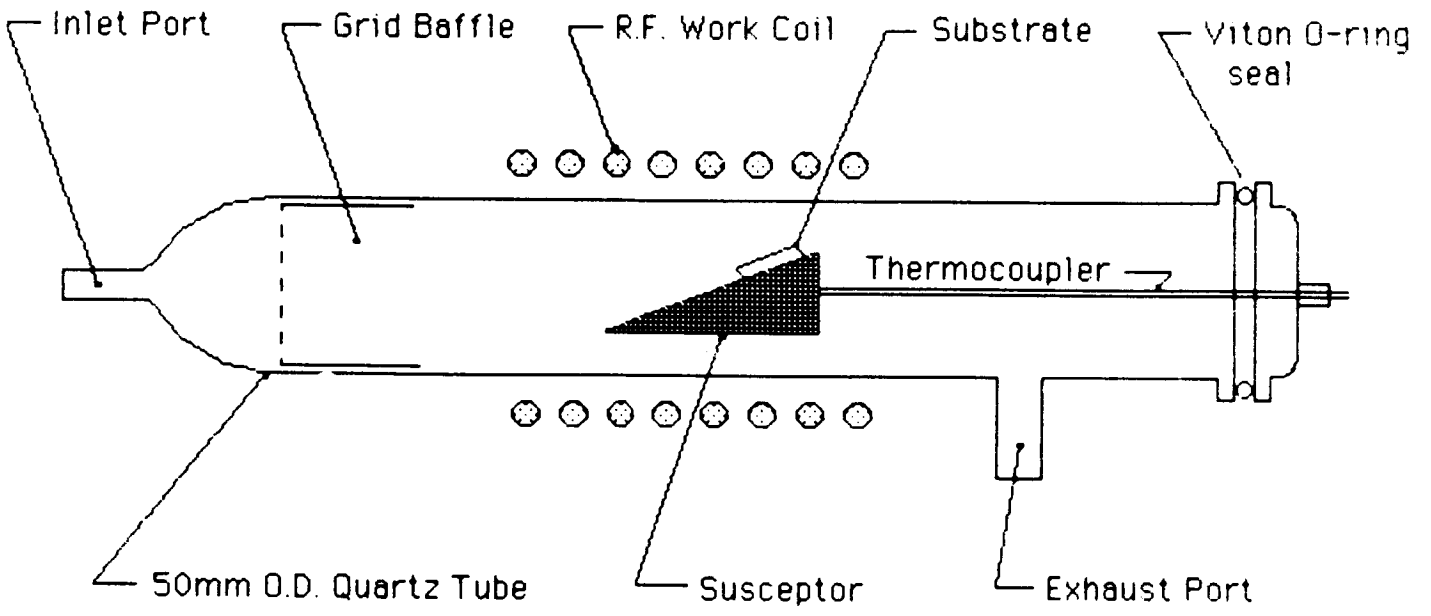


Figure 3.1 - Schematic of the Original Reaction Chamber used for the initial experiments in OMCVD for 60GHz Double Drift Impatts.

conducted with a total hydrogen flow of 9.5 standard liters per minute (slm) and with this baffle in place, since these conditions yielded the best uniformity and surface morphology. An example of the results obtained for an undoped layer grown under these conditions is given in Figure 3.3.

The growth of thin layers (less than 1.0 micron thick) which are required for high frequency devices, has not been treated extensively in the published literature for MOCVD. Therefore, a series of experiments was conducted in order to investigate the growth of sub-micron layers, as well as to calibrate the properties of the reactor. As shown in Figure 3.4, layers of between 0.1 micron and 0.5 micron can be controllably grown in reasonable time spans. It is important to use a growth rate which yields such time intervals so that high accuracy can be obtained in the control of the layer thickness using either manual or automatic control of the trimethylgallium (TMG) injection valves. The conditions which were used to grow these layers were:

Temperature	= 700°C
TMG partial pressure	= 7.0×10^{-5} atm
Arsine partial pressure	= 4.5×10^{-3} atm

The data closely fits a linear relationship between layer thickness and growth interval, with an effective growth rate of 0.056 microns/minutes. Extrapolation of the data to zero layer thickness yielded a period over which little or no growth occurred. This phenomenon has not been reported previously in MOCVD, but has been found to exist in other forms of epitaxy. This "induction period", as it has been termed, probably exists due to non-equilibrium effects associated with nucleation and transient effects in the boundary layer above the susceptor. This effect is not expected to cause a problem since the required time interval appears to be highly repeatable and uniform.

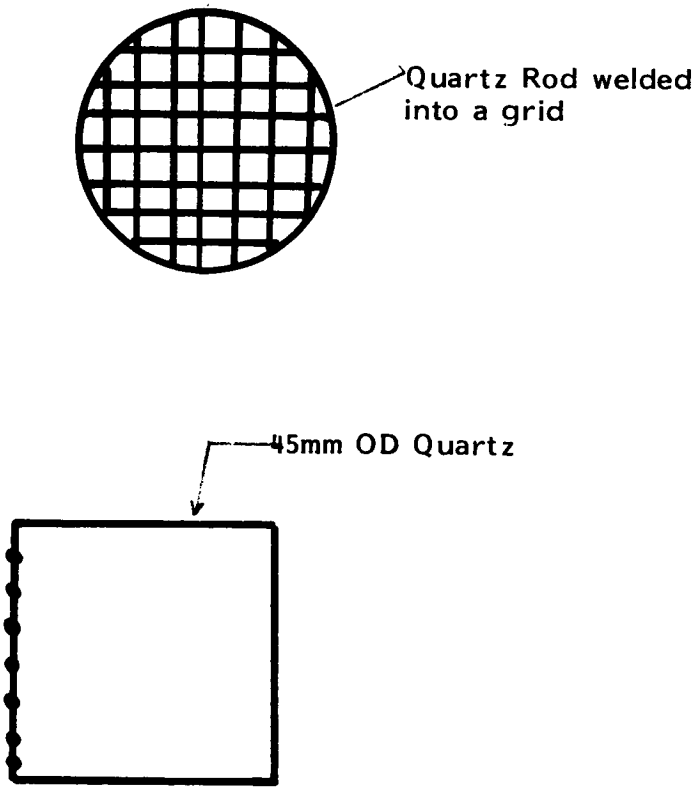


Figure 3.2 - Baffle for MOCVD Reaction Tube

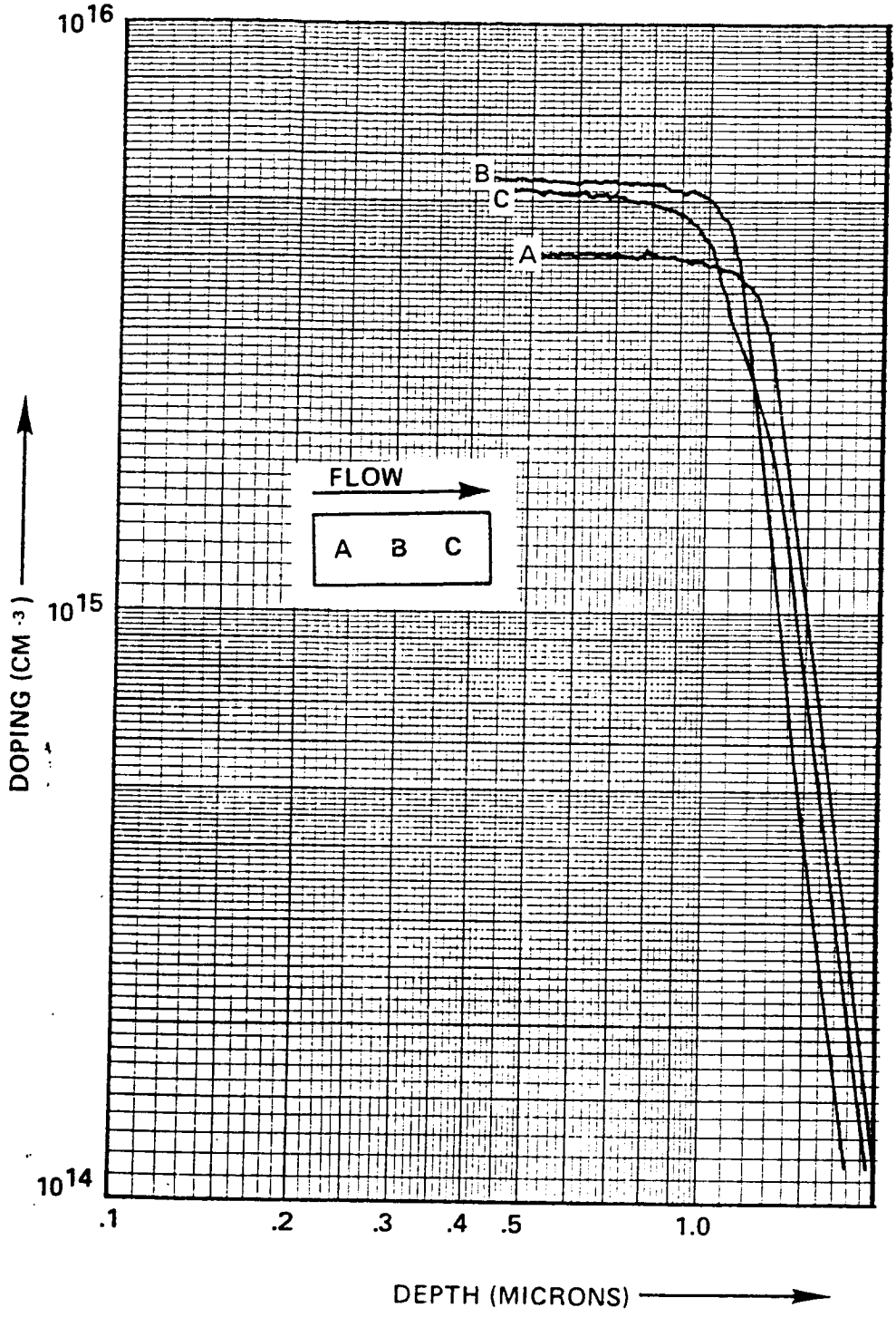


Figure 3.3 - Example of typical uniformity achieved in undoped MOCVD epi-layers using a baffle

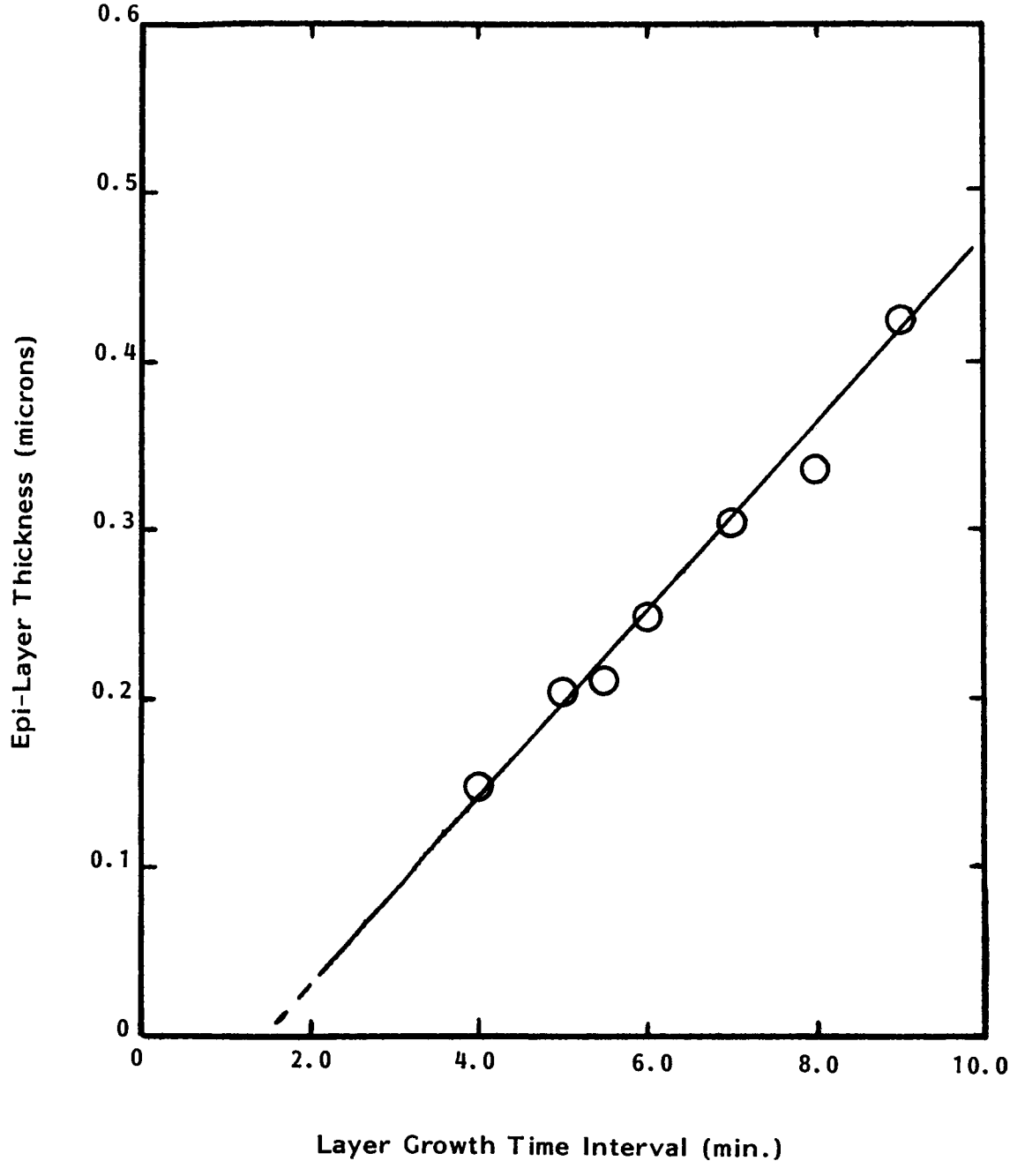


Figure 3.4 - Relationship between Growth Time Interval and resulting Layer Thickness for MOCVD

Another set of experiments was performed to characterize the doping behavior of silane (SiH_4) in MOCVD grown epilayers. The results of this set of growth runs are demonstrated in Figure 3.5. Silane was chosen as the N-type dopant impurity because it is known to be highly stable as a mixture with hydrogen at high pressure; thus, it would not demonstrate a degradation in activity which is commonly found when other N-type dopants (such as H_2Se or H_2S) are used. The partial pressure of silane in the reactant stream was controlled by a dilution network, shown in Figure 3.6, and was calculated using a mass balance equation given in this Figure.

Several important points should be noted from these doping experiments. First, as shown in Figure 3.5, the free electron concentration is linearly proportional to the concentration of silane present in the reactant stream indicating that the incorporation process for silicon from silane is most likely a straightforward decomposition/absorption reaction. The linearity also indicates that the large majority of silicon atoms incorporated into the GaAs lattice occupy gallium sites and are therefore donors; otherwise, significant curvature would be expected since the acceptor/donor ratio would be a function of doping level. A second interesting point can be observed by comparing the silane concentration required to produce a given electron concentration observed in MOCVD with that found in halide VPE. The result of this comparison indicates that silicon, from silane, is incorporated between 10 and 100 times more effectively in MOCVD that in halide VPE. Although not shown on the graph, it was also possible to obtain high doped ($N = 2 \times 10^{18} cm^{-3}$) layers which are commonly used in microwave devices as a buffer between the substrate and the active layers.

Electrical measurements were made on epitaxial layers grown on semi-insulating substrates using the Hall effect. Films grown without any intentional doping typically were N-type with carrier concentrations of about $2.5 \times 10^{15} cm^{-3}$ and electron mobilities of 5,900 $cm^2/V\text{-Sec}$ at 300K. With silicon doping, films doped to $N = 3.5 \times 10^{16} cm^{-3}$ had mobilities of about 4800 $cm^2/V\text{-sec}$. These high electron mobilities

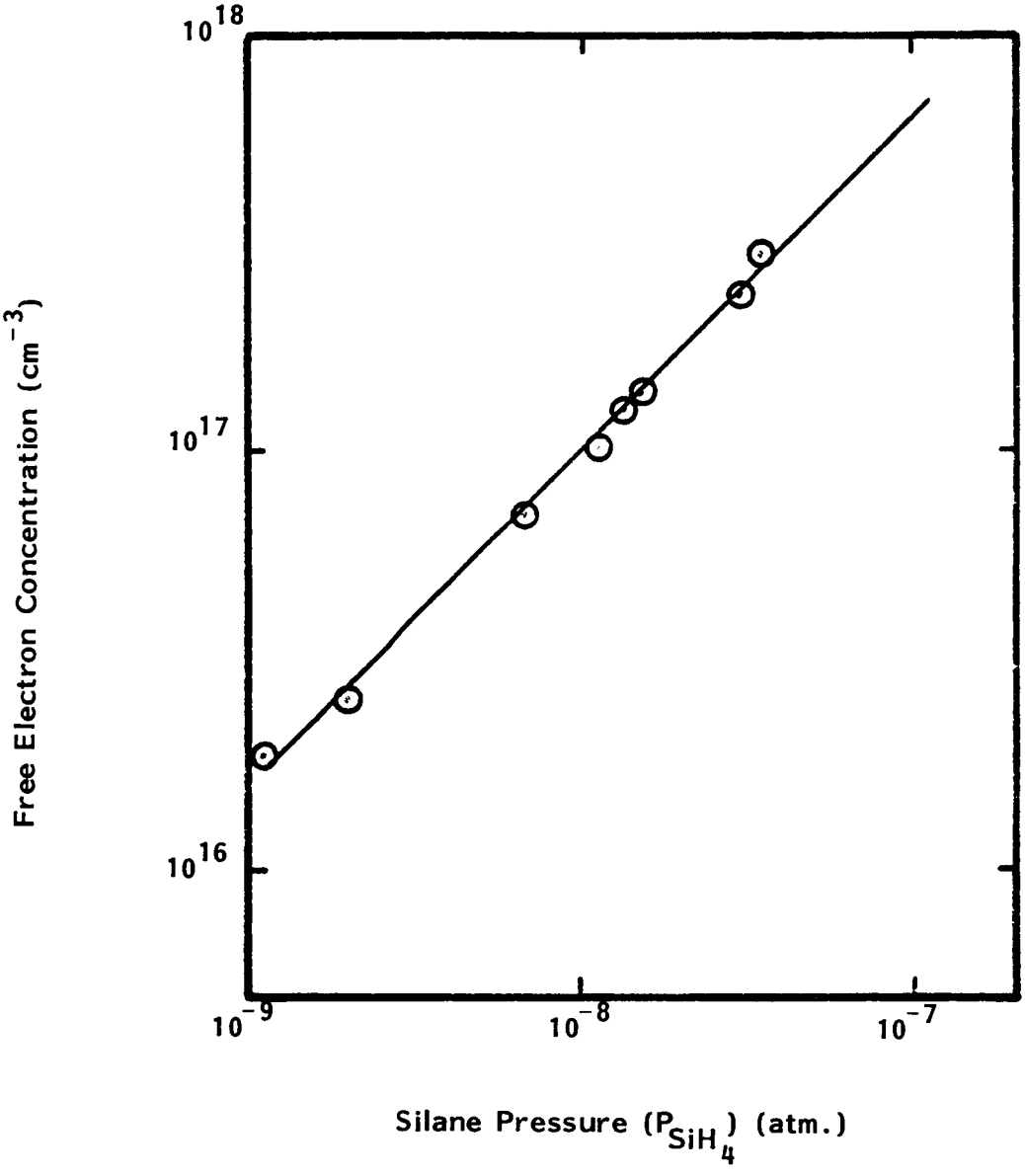
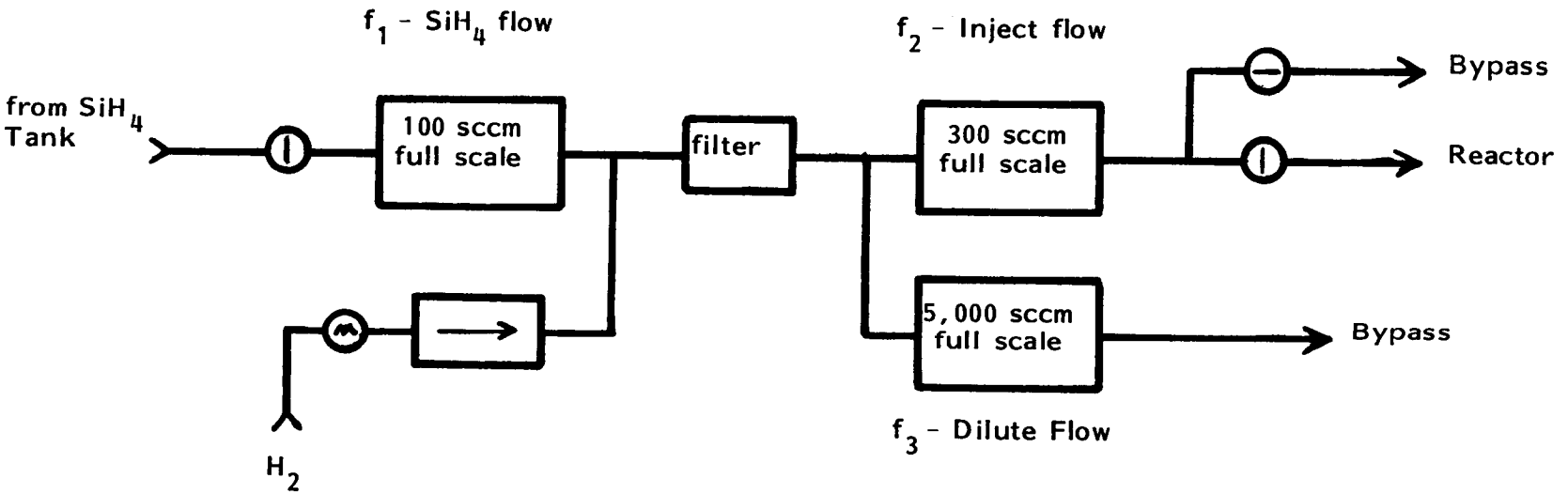


Figure 3.5 - Free Electron Concentration as a function of the Silane concentration injected during layer growth



$$P_{SiH_4} = C_{SiH_4} \cdot f_1 \cdot \frac{f_2}{F_{total}} \cdot \frac{}{f_2+f_3}$$

fi = flow in i-th Mass Flow Controller (percent set x full scale rate)

F_{total} = Total flowrate in Reactor

C_{SiH_4} = Concentration in Silane Tank

Figure 3.6 - Schematic of Double Dilution Dopant Channel

indicate that the doped films are relatively uncompensated lending further credence to the conclusion that the silicon is almost exclusively in the form of donors on gallium lattice sites.

At this point in the program all the information required to grow an epitaxial structure for a single-drift IMPATT diode was available. Although a single-drift structure would not meet the goals of the program, growing such a structure allowed experience to be gained in several areas, such as characterization, fabrication and testing, before the more ambitious double-drift profiles were attempted. A schematic of the doping profile, generated by the device design effort for a 60 GHz single drift IMPATT, is shown in Figure 3.7a. In order to keep the epitaxial growth of this device simple, a Schottky barrier contact of platinum was used in place of the P^+ contact. Due to the reaction which occurs between the platinum and the GaAs during contact formation, an additional 0.05 microns of epitaxial material was grown to compensate and keep the avalanche region at 0.21 microns thick. The doping profile required for this device is shown in Figure 3.7b.

Several growth experiments were conducted to grow the single-drift structure and to investigate the effects of the growth procedure on the abruptness of the HI-LO doping transition. Since the silane and TMG injection valves were independently controlled, several different sequences were tried in making the transition between the drift region (LO) growth and the avalanche (HI) region growth. A few of the possible strategies for making the transition and the results obtained from using these sequences are shown qualitatively in Figure 3.8. Due to the strong absorption of silicon from the gas stream, as demonstrated by the high doping efficiency mentioned above, it is postulated that whenever silane is injected into the reactant flow there is an accumulation of silicon on the surface of the sample. If no TMG is injected concurrent with the silane this accumulation builds to form a spike, as shown in Figure 3.8c. The best results for transition abruptness were obtained when the silane and TMG injection valves were operated together in a

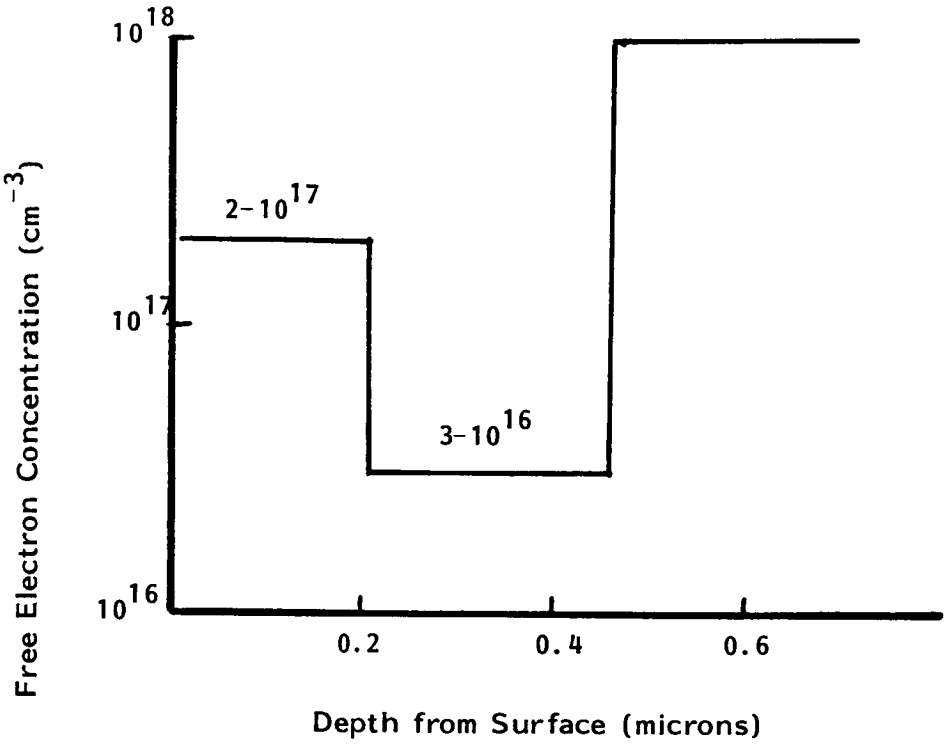


Figure 3.7a - Profile of 60GHZ Single drift IMPATT

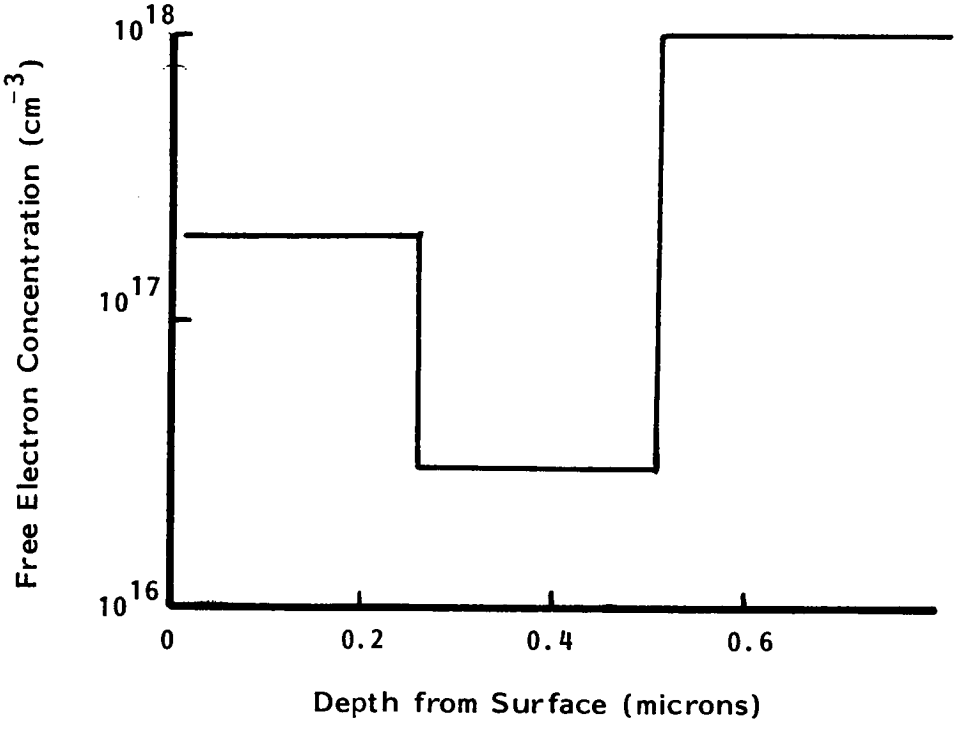


Figure 3.7b - Profile desired for Schottky - contact
Single drift 60GHZ IMPATT

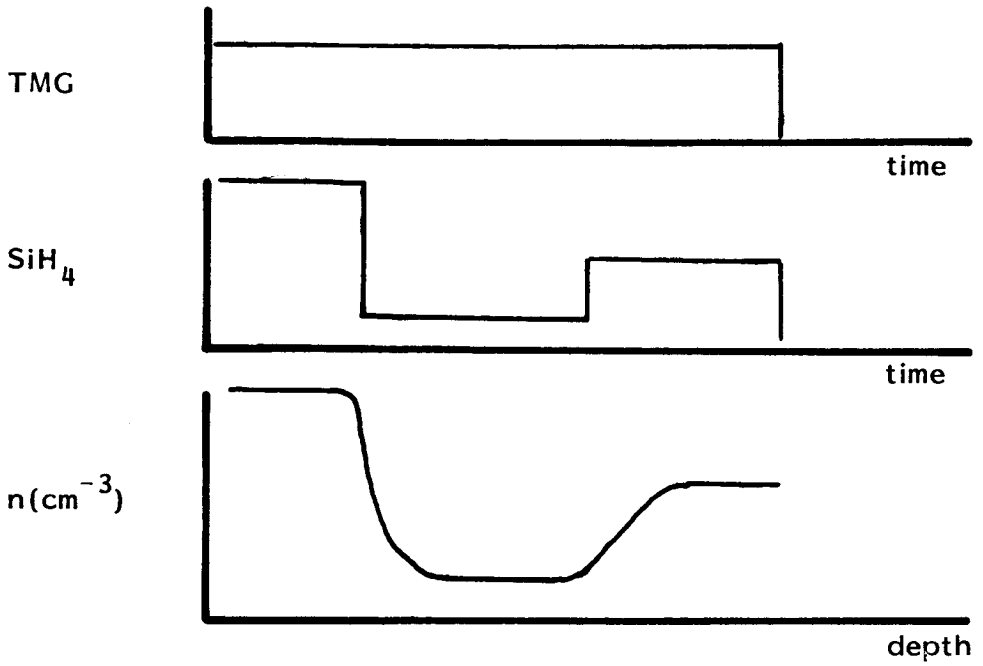


Figure 3.8a

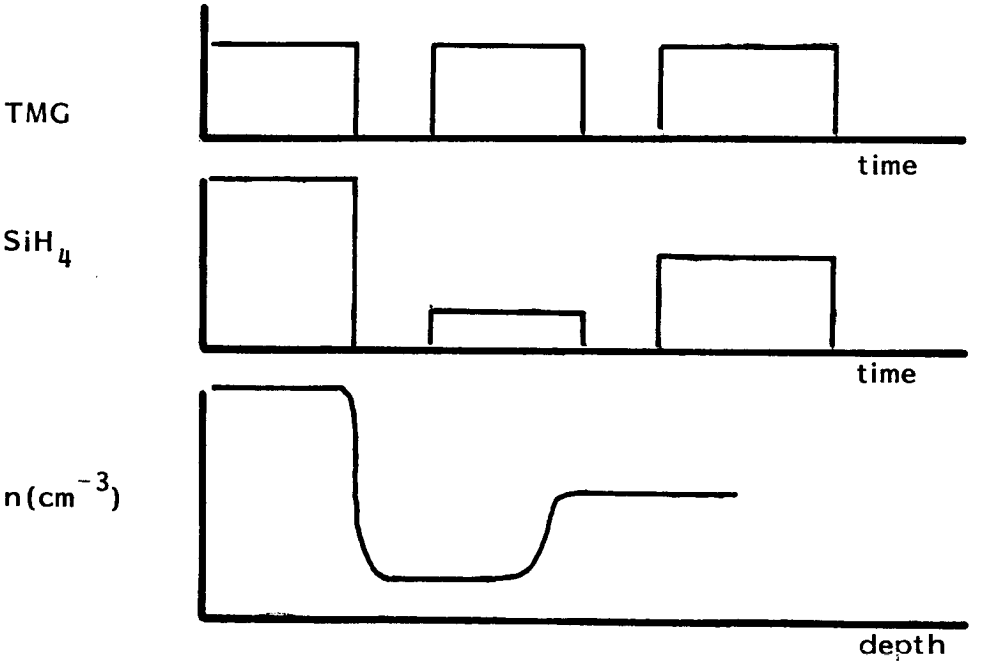


Figure 3.8b

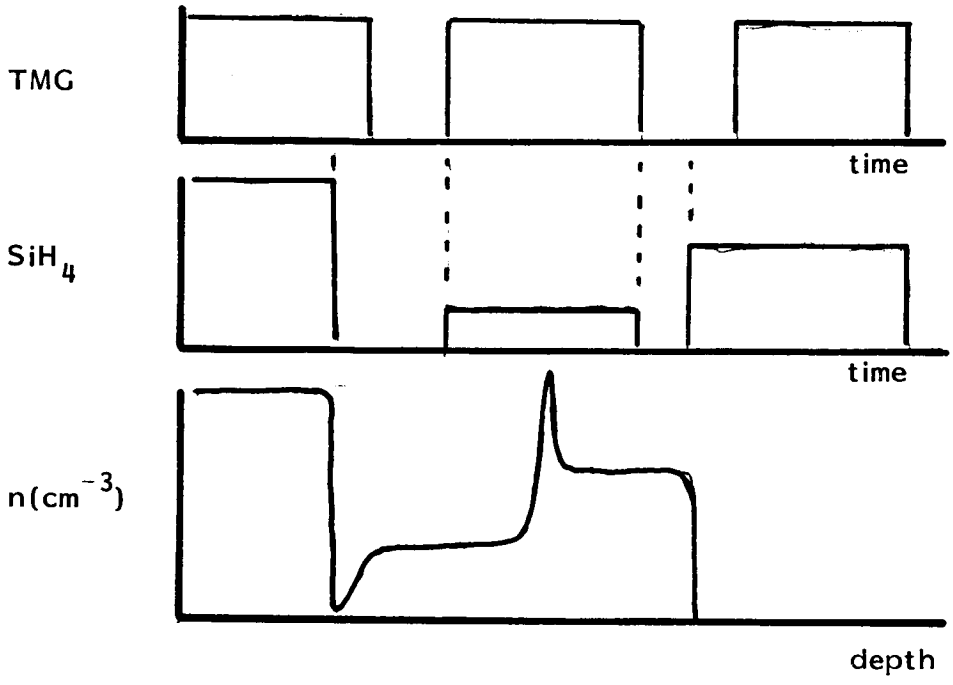


Figure 3.8c

Figure 3.8 - Effects of various sequences between TMG and SiH_4 injection

ganged manner. These experiments also serve to demonstrate one of the major advantages of the MOCVD technique, namely, the ability to start and stop the epitaxial growth in an almost stepwise fashion.

The doping profiles measured on two of the structures grown during the single drift experiments are shown in Figures 3.9 and 3.10. The transitions obtained in these samples are very steep, with a total HI to LO transition length of about 0.06 microns. In evaluating doping profiles taken using capacitance/voltage techniques, as these were, the effects of Debye smearing on the profile must be taken into account. Theoretical calculations have been made for the case of a perfect step-profile in doping and indicate that even in the ideal case the transition becomes broadened by about six times the Debye length in the more heavily doped side of the junction. (Johnson and Panousis, IEE Tran. on Electron Devices, Vol. ED-18 pp. 965, 1971). For the present case the HI level doping is $2 \times 10^{17} cm^{-3}$ which yields a Debye length of approximately 0.01 microns indicating that the transitions measured for these structures are extremely sharp and are in fact beyond the limits of C/V profiling.

Having characterized the growth parameters of the MOCVD system in terms of layer growth rate and N-type doping calibration, and having demonstrated the fabrication of millimeter-wave single drift structures, effort began on developing the P-type doping techniques required for realizing double-drift devices. Controlled P-type doping of MOCVD layers would be expected to present several problems not encountered in N-type doping. The most important point to be made in terms of P-type doping lies in accurately characterizing the doping in P-type GaAs. Due to the low barrier height of Schottky barriers in P-type material, standard capacitance/voltage profiling techniques yield highly questionable results. On the other hand, Hall effect measurements spatially average the electrical properties of an epitaxial structure over all the conductive material present making profile measurements extremely difficult and limiting their accuracy. Even on uniform layers grown on semi-insulating substrates the accuracy of the Hall effect measurement of

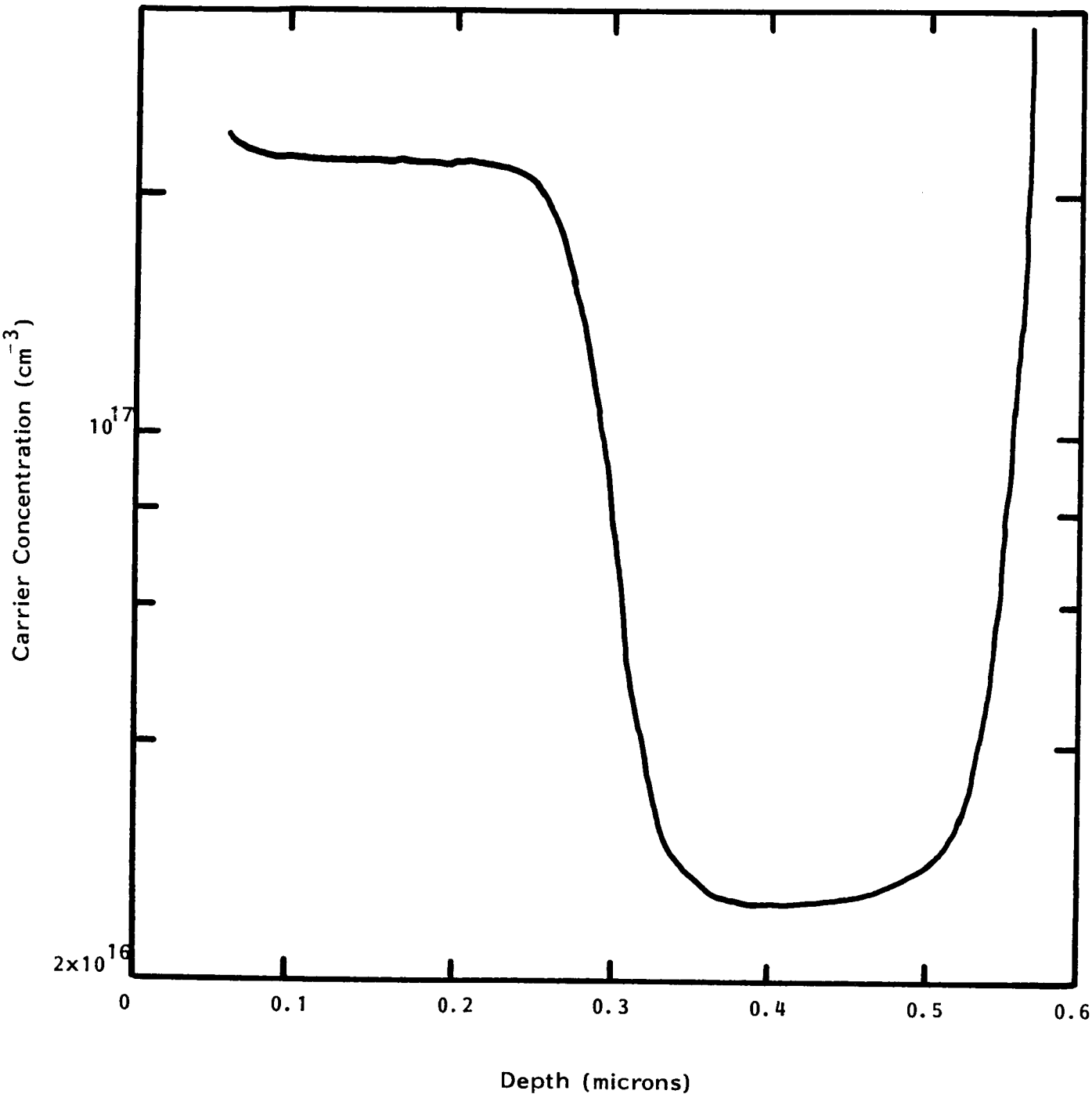


Figure 3.9 - Sample grown for 60 GHz single-drift IMPATT

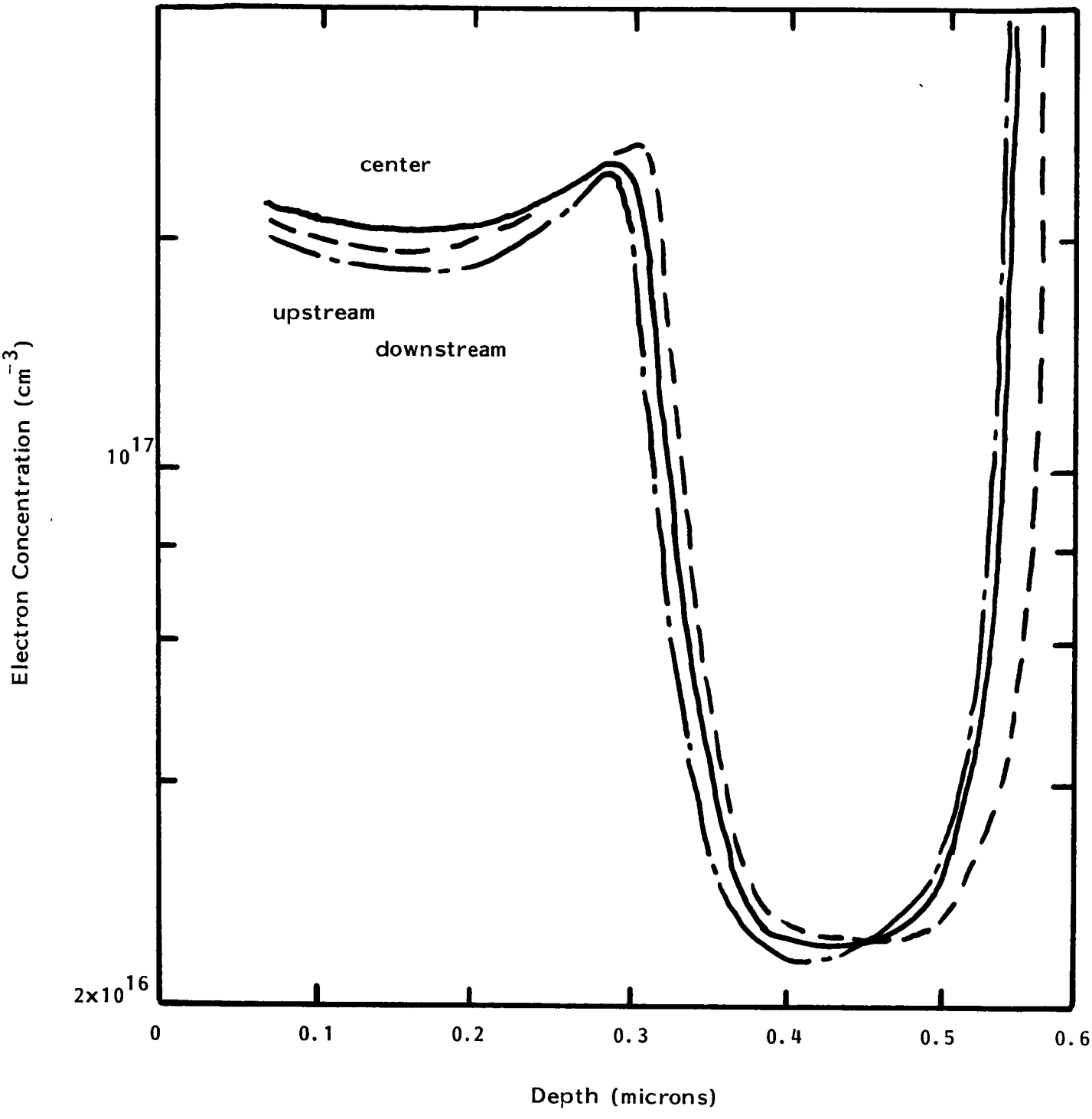


Figure 3.10 - An example of the uniformity over a 2cm square sample grown for single-drift diodes

carrier concentration can be degraded by geometric factors, such as precise thickness determination. In addition to these measurement difficulties, controllable P-type doping in the 10^{16}-10^{17} range would be expected to present difficulties since the residual impurity background in high purity OMCVD epilayers is N-type. P-type doping is, therefore, a counter doping process with a possible interference from the residual dopants.

In order to obtain an estimate of the calibration factors involved for P-type growth, a series of relatively thick (1um) uniformly doped layers were grown on semi-insulating substrates. Dimethylzinc, (DMZ) supplied as a mixture of 2700 ppm DMZ in hydrogen, was used as the dopant source. Hall effect measurements were used to characterize the free hole concentrations using thickness measurements derived from the cleave and stain optical microscopy technique. The results of these experiments are given in Figure 3.11. It is noteworthy that as was found in the case for silicon doping, zinc doping yields free hole concentrations which are linearly proportional to the partial pressure of DMZ in the reactant system. The efficiency with which zinc was incorporated was found to be roughly comparable in MOCVD to that found for the halide VPE process.

Zinc doping was found to be relatively straightforward for concentrations in the 10^{17} to $10^{19}cm^{-3}$ range. Attempts to obtain P-type layers in the low $10^{16}cm^{-3}$ range yielded data with a large degree of scatter possibly due to the effects of interface and surface depletion layers on the Hall effect measurement technique. All of the P-type films exhibited excellent electrical characteristics; layers doped to $10^{18}cm^{-3}$ had hole mobilities of around 70 cm^2/V-sec.

Having at least partially determined the P-type doping behavior and having a relatively good estimate of the N-type doping character, a set of experiments was next devised with a view towards growing P-N junction devices. Rather than attempt the growth of the full double-drift structure, it was decided that a simpler structure would

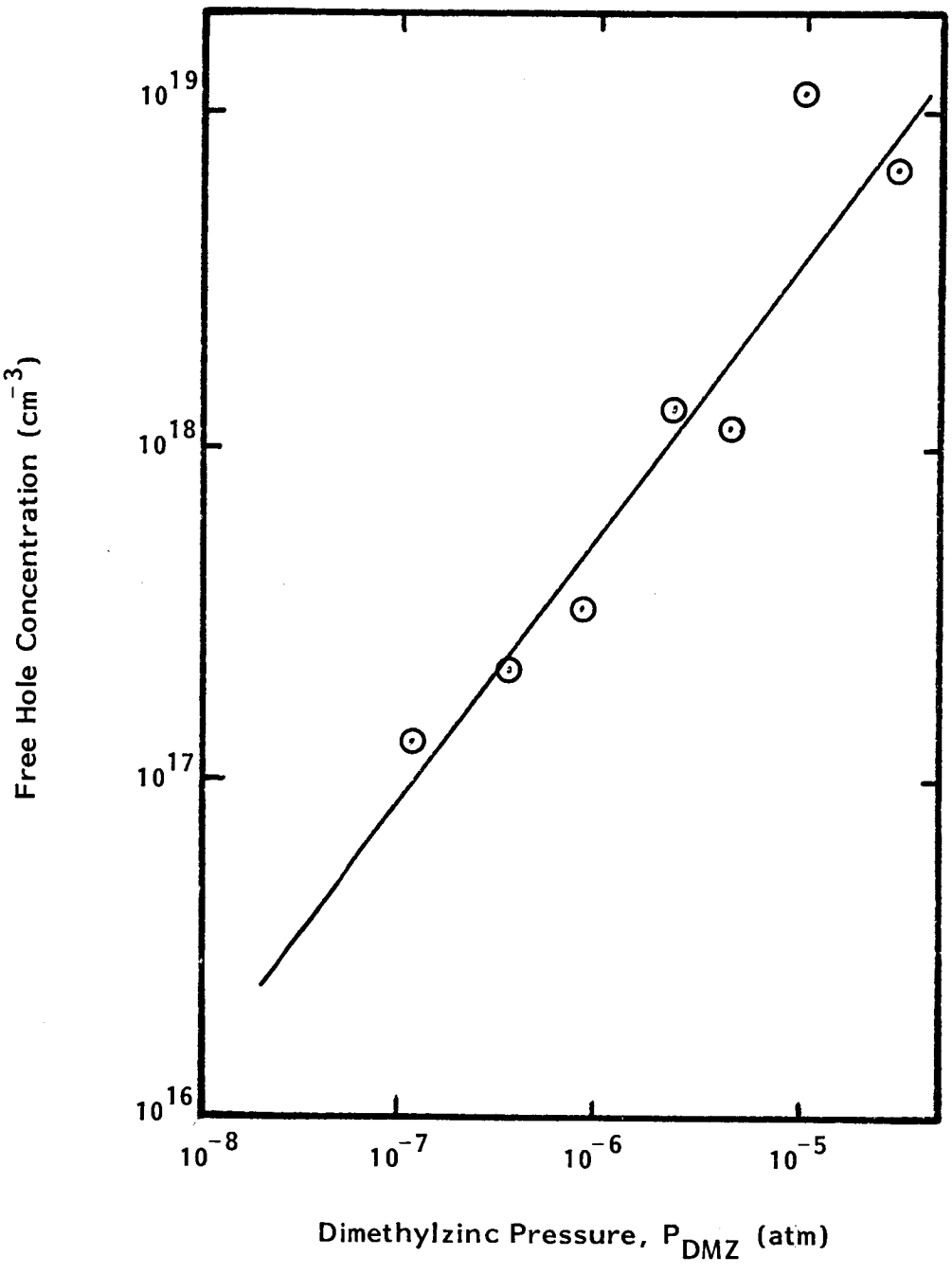


Figure 3.11 - Results of p-type doping experiments

allow experience to be gained in terms of junction formation without the complications involved in double-drift diodes analysis. The initial P-N structure involved a simple 30 volt abrupt varactor. This device consisted of an N^+ buffer, and an N-active region of 1.5 microns thick doped to 2 X $10^{16}cm^{-3}$, followed by a P^+-contact doped to 1 x $10^{19}cm^{-3}$.

Attempts to grow this structure, as well as attempts to grow the 60 GHz single drift IMPATT with a P^+ contact, were not successful. Diodes fabricated from these epilayers were leaky and had poor reverse breakdown characteristics. Since the growth temperature used in these experiments, 700°C, is rather high for MOCVD epitaxy and since zinc is known to be a rapid diffusing specie in GaAs, the cause of these degraded diode characteristics could be junction grading and/or the formation of defects associated with the high temperature growth. The original choice of using 700°C for the growth temperature was based on past experience involving simple, uniform layers for which very good electrical properties were obtained at this temperature. At this point, it was decided that lower temperature growth should be investigated, keeping in mind that the 700°C experiments had been useful in getting the program started and in allowing estimation of the MOCVD system parameters.

Using the same reactant parameters given above for 700°C, growth at lower temperatures (between 600°C and 650°C) produced undoped epitaxial films that exhibited P-type residual conduction with hole concentrations in the high $10^{16}cm^{-3}$ range. Such films were clearly unsuitable as a starting point for the double-drift devices. Consequently, a series of experiments was commenced to determine more optimum growth conditions at these lower temperatures. The conditions which were found to yield high quality epilayers over the 600°C to 650°C range were: total hydrogen flow = 9500 sccm., TMG partial pressure = 1.16 X 10^{-4} atm., arsine pressure = 4.06 C 10^{-3} atm. Undoped layers grown at 650°C with these conditions showed N-type conductivity with free electron concentrations of above 5 X $10^{14}cm^{-3}$. The best surface morphologies resulted from growth at 650°C while at lower temperatures the surfaces had an increasing density of point defects, mostly small hillocks.

A set of experiments were conducted in order to determine the N-type doping behavior at 650°C, which was chosen as the new standard growth temperature. The results from these experiments are shown in Figure 3.12 along with the calibration line determined from the 700°C experiments. As was expected, lowering the growth temperature decreased the efficiency with which silicon was incorporated into the epilayer from the reactant stream. The observed decrease in the residual doping can also be explained by this decrease in the incorporation efficiency since the major residual impurity in the reactant sources was silicon from the TMG. The observed fall in the incorporation of silicon was probably due to the kinetics associated with the decomposition of silane (SiH_4) to form silicon and its subsequent absorption onto the growing surface.

At this point in the program, several mechanical failures occurred in equipment which was either part of, or associated with, the MOCVD system. The gas bottle regulator for the HCl channel developed a leak in the regulating diaphragm; the induction heating generator developed an intermittent arcing problem, and; the purifier which supplied high purity hydrogen exhibited a decreased output. Because of the shutdown associated with correcting these difficulties, especially the H_2 supply, it was decided to move the MOCVD reactor system to the newly completed Commercial Epitaxy Laboratory. The move allowed more floor space to be devoted to the MOCVD system, making operation more convenient, and gave the system its own independent hydrogen purifier.

During the period over which the system was inactive for moving and for re-connection, several projects aimed at improving its operational characteristics were initiated. The first of these modifications was the design and construction of a new electronics control sub-system.

Housed in a separate cabinet from the gas handling and the reactor, this new sub-system incorporated a microprocessor based automatic sequencer which would allow for a fully automated control of the epitaxial growth process. Another effort was to design a larger reaction chamber

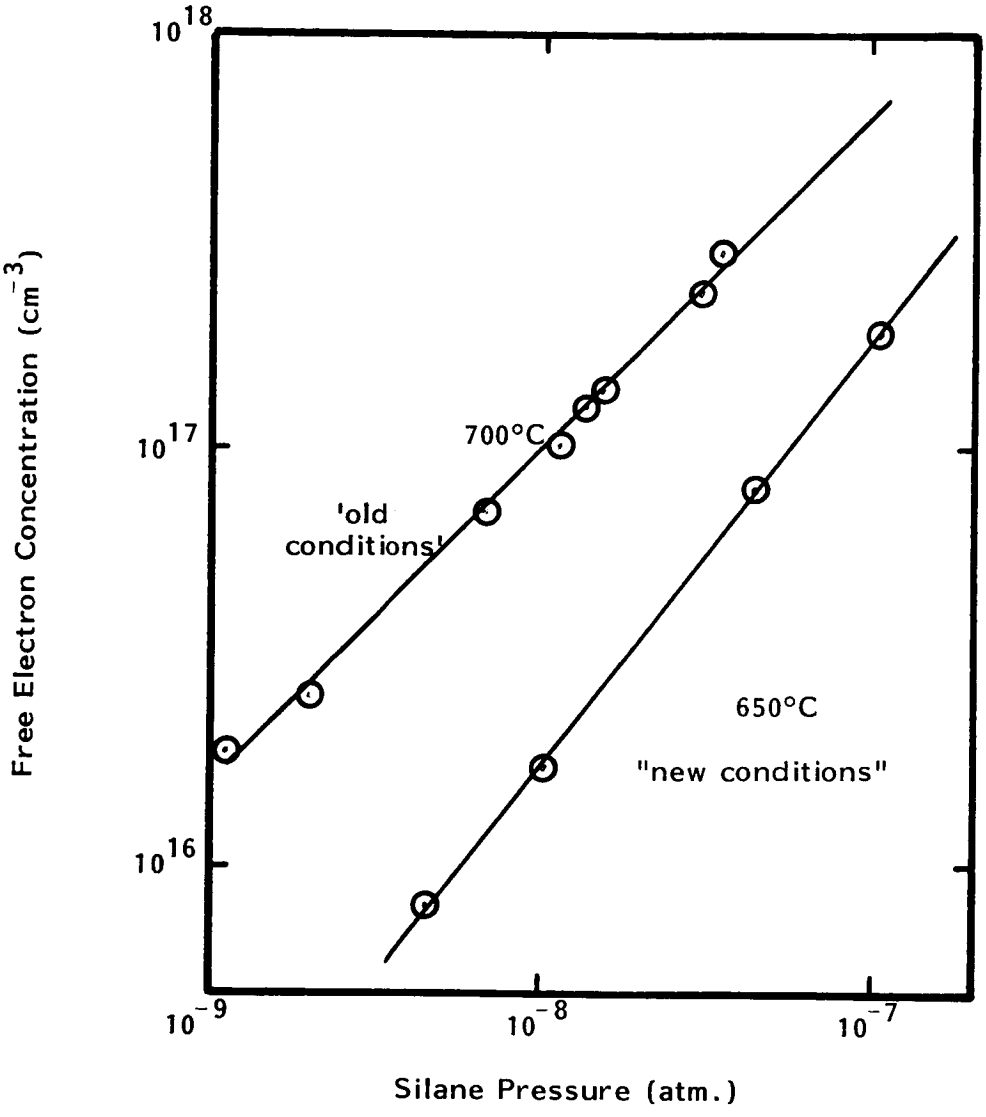


Figure 3.12 - Doping calibration curve for 650°C "new conditions" as compared to "old conditions" curve

capable of yielding improved uniformity over two substrates of 2 inch diameter grown simultaneously. The major benefit of such a modification would be derived from having a larger quantity of material for electrical characterization and actual device fabrication. A third modification consisted of the purchase and installation of a new gas cylinder cabinet to contain the AsH_3 and HCl bottles and their associated purging and regulator networks.

The MOCVD system relocation was completed in mid-December of 1982. A set of control experiments was then performed in order to verify that the operational characteristics were unchanged and that high quality growth can still be obtained. At this time, the design of the new, larger reaction chamber was completed and its fabrication begun. Work also continued on the new electronics sub-system.

The first series of experiments, after revalidating system performance, consisted of a calibration of the P-type doping behavior at the lower growth temperature (650°C). These results are presented in Figure 3.13 along with the results at 700°C as a reference. As is seen from these results, zinc incorporation is dramatically increased by lowering the growth temperature. Such phenomenon have been previously reported by other workers. It is postulated that the volatility of zinc at these elevated temperatures may decrease the absorbed fraction of the element on the surface with increasing temperature. This would then lead to a decreased overall incorporation with increasing temperature. Since the diffusion constant varies exponentially with temperature, decreasing the growth temperature should rapidly decrease the effects of impurity redistribution due to diffusion.

However, in layers as thin as those required in the 60 GHz double-drift IMPATT even a small amount of redistribution by diffusion is of concern. During the fall of 1982, a Polaron-Post Office Plotter was purchased in order to allow further characterization of P-type material and complex doping profiles. A plot of a P-type HI-LO junction taken using this electrochemical instrument is shown in Figure 3.14. The

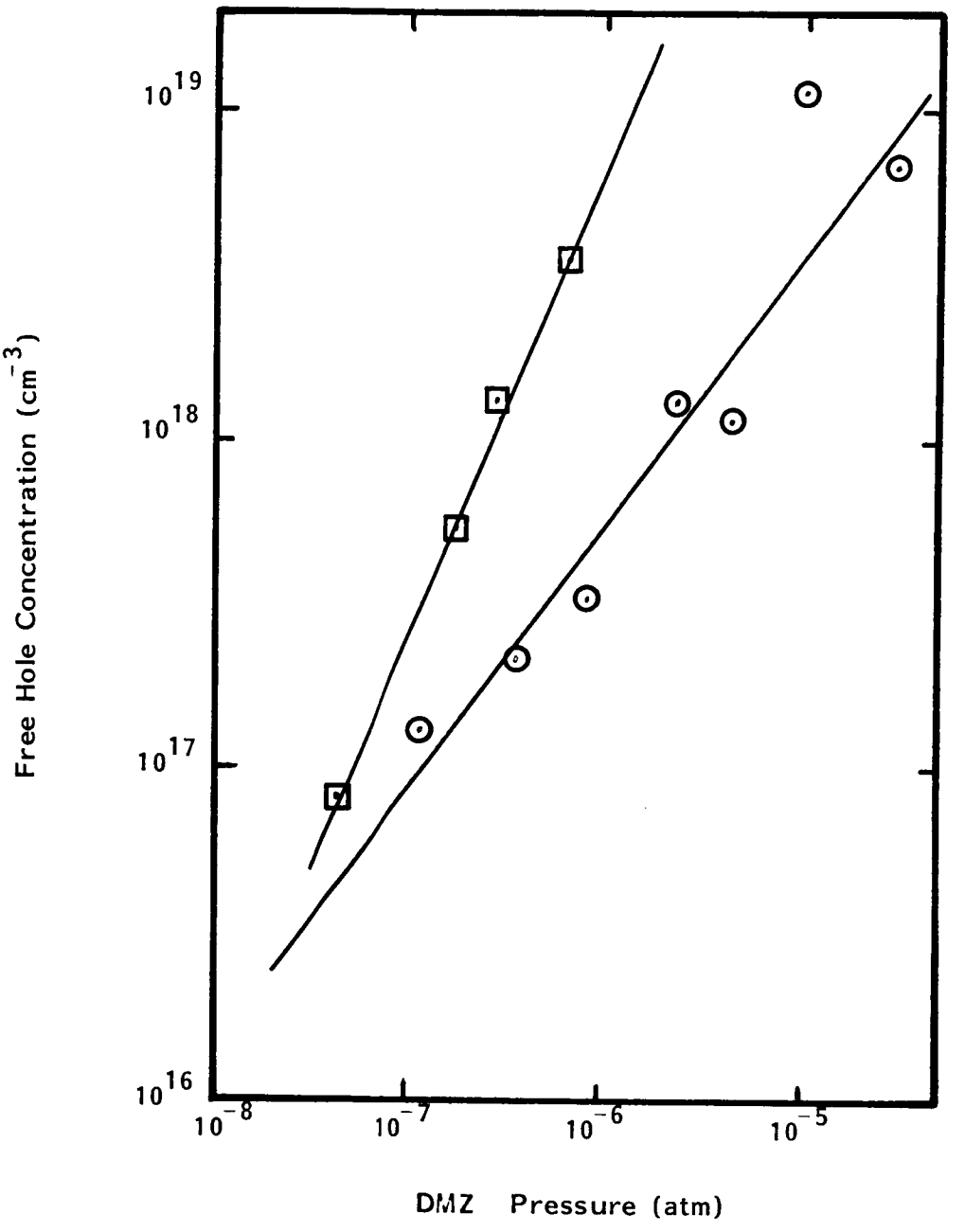


Figure 3.13 - Doping calibration for Zinc doping at 650°C for the "new conditions"

transition from the HI region in this plot would seem to indicate that a large amount of dopant smearing occurred in the vicinity of the junction. Further experience with this instrument indicated that similar results were obtained even in structures known to be very abrupt, such as the HI-LO N-type layers grown for the single-drift devices. It is therefore difficult to draw any conclusions concerning the amount of zinc diffusion which occurred at 650°C growth temperature based on this evidence.

In order to further investigate this phenomenon, abrupt varactor structures, as described above, were grown and fabricated into mesa diodes. For a growth temperature of 650°C excellent diode characteristics were obtained for these P^+-N devices. As is shown in Figure 3.15, these diodes exhibited classic capacitance/voltage curves which, when analyzed mathematically, yielded the doping profile of the N-active layer. The ability to form high quality P-N junctions at 650°C growth temperatures was highly encouraging and provided new possibilities in terms of analyzing the P-type dopant behavior.

One of these possibilities was to grow a P^+-P(active)-N^+ structure where the bulk of the depletion region would spread through the P(active) layer. This structure was of interest since it allowed C/V characterization techniques to be used for the P-type doping analysis. The P-type layers in this structure were also of the same type as those for the double-drift IMPATT. Hence, these devices allowed separate characterization of the P-side of a hybrid double-drift IMPATT.

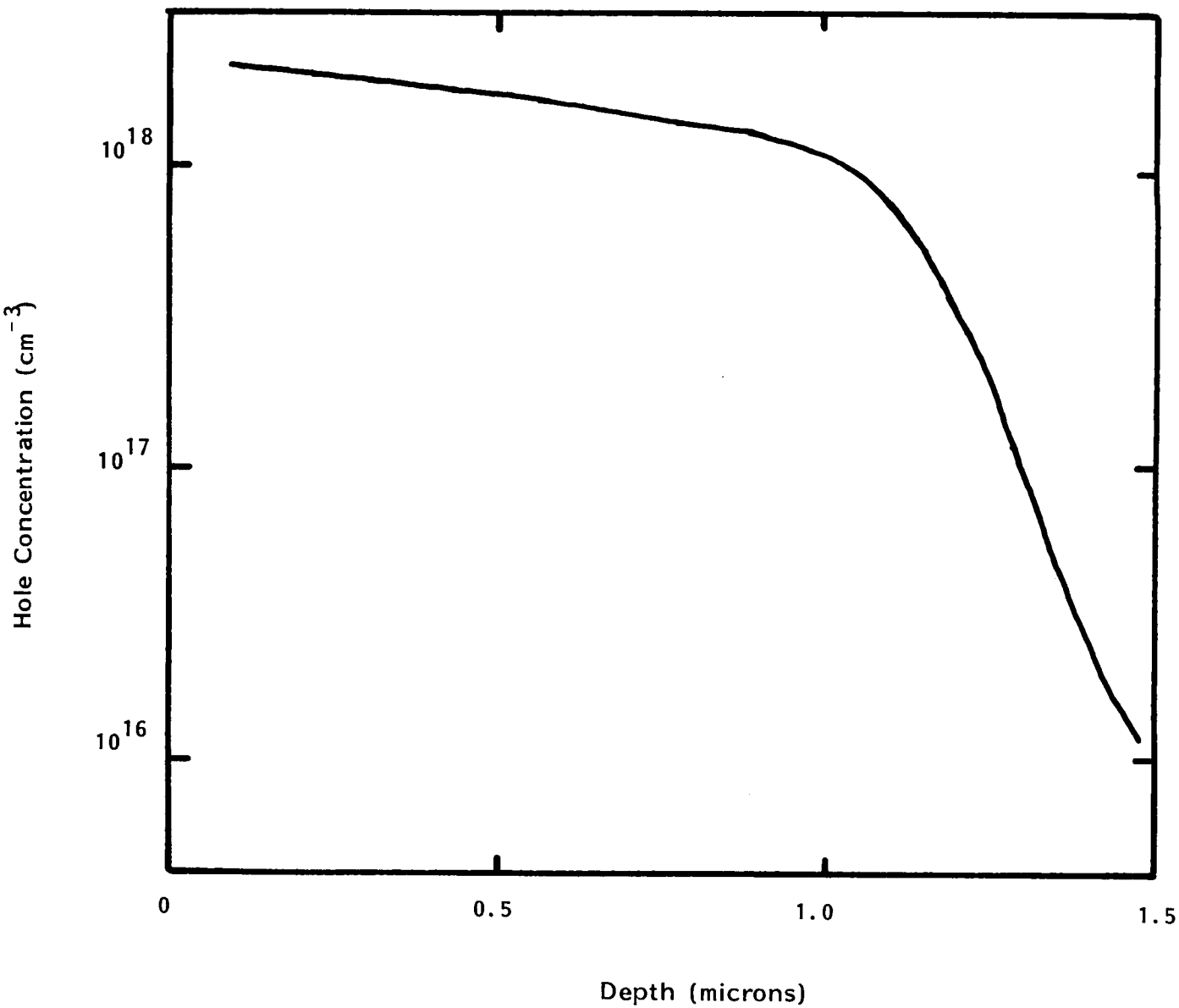


Figure 3.14 - Polaron Profiler plot of p-type doping profile for layer grown at 650°C

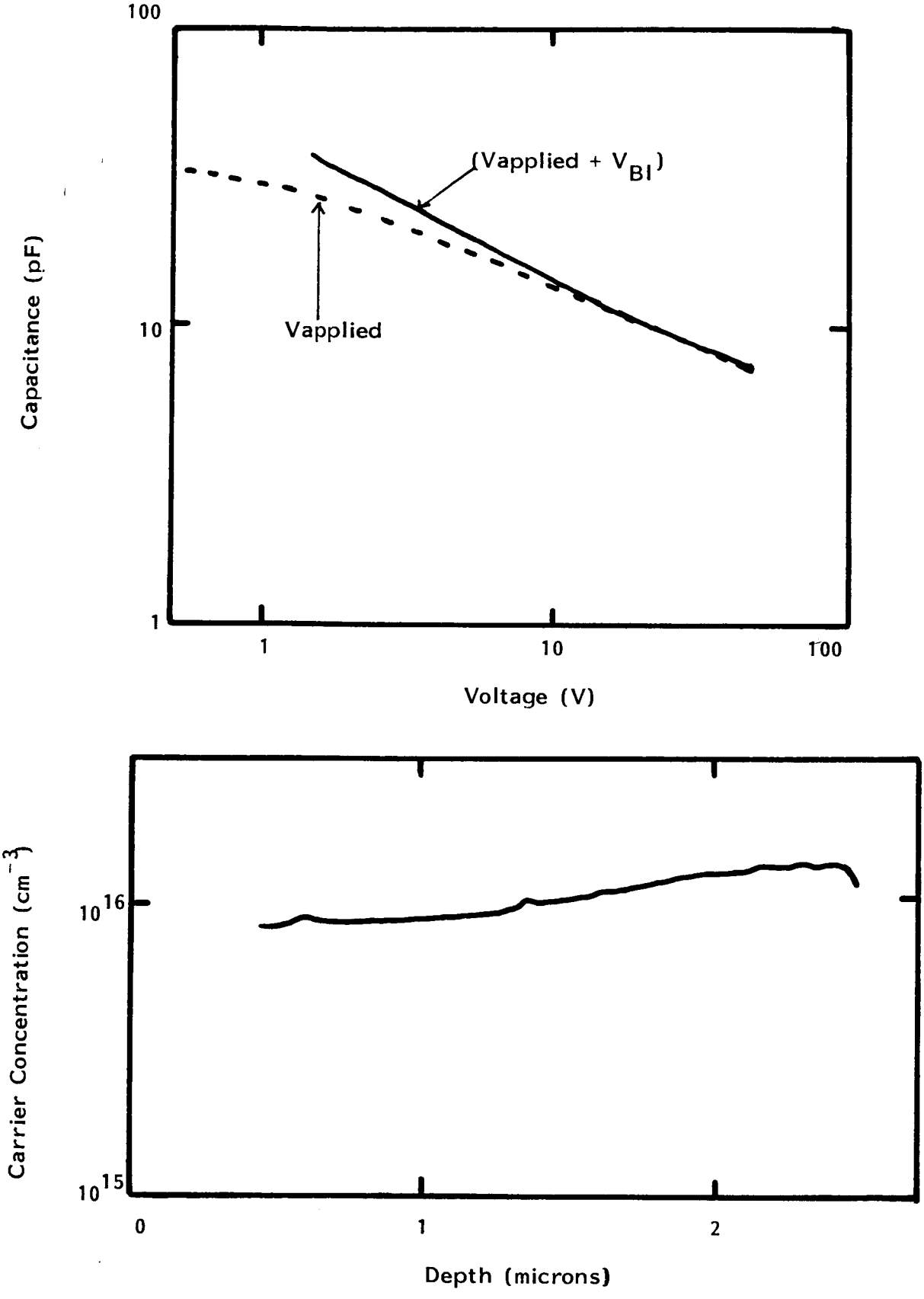


Figure 3.15 - C/V and calculated Doping Profiles of P^+-n diodes grown by MOCVD.

Data taken from a typical P^+-P(active)-N^+ structure is presented in Figure 3.16. It is important to note that the doping profile calculated for the P(active) layer is relatively flat and that a sharp transition to the P^+ layer is observed. This is evidence that little zinc redistribution occurs via diffusion during epitaxial growth. Furthermore, it indicates that abrupt doping transitions in P-type material can be obtained in MOCVD using dimethylzinc.

Epitaxial growth experiments were also carried out for the growth of 60 Hybrid Double-Drift IMPATTs. The characteristics of one of these structures are illustrated in Figure 3.17 for test diodes made by a simple metallization and mesa etching procedure. The effective doping plotted in this figure may be interpreted as:

$$1/N(w) = 1/N_A(x_p) + 1/N_D(x_n)$$

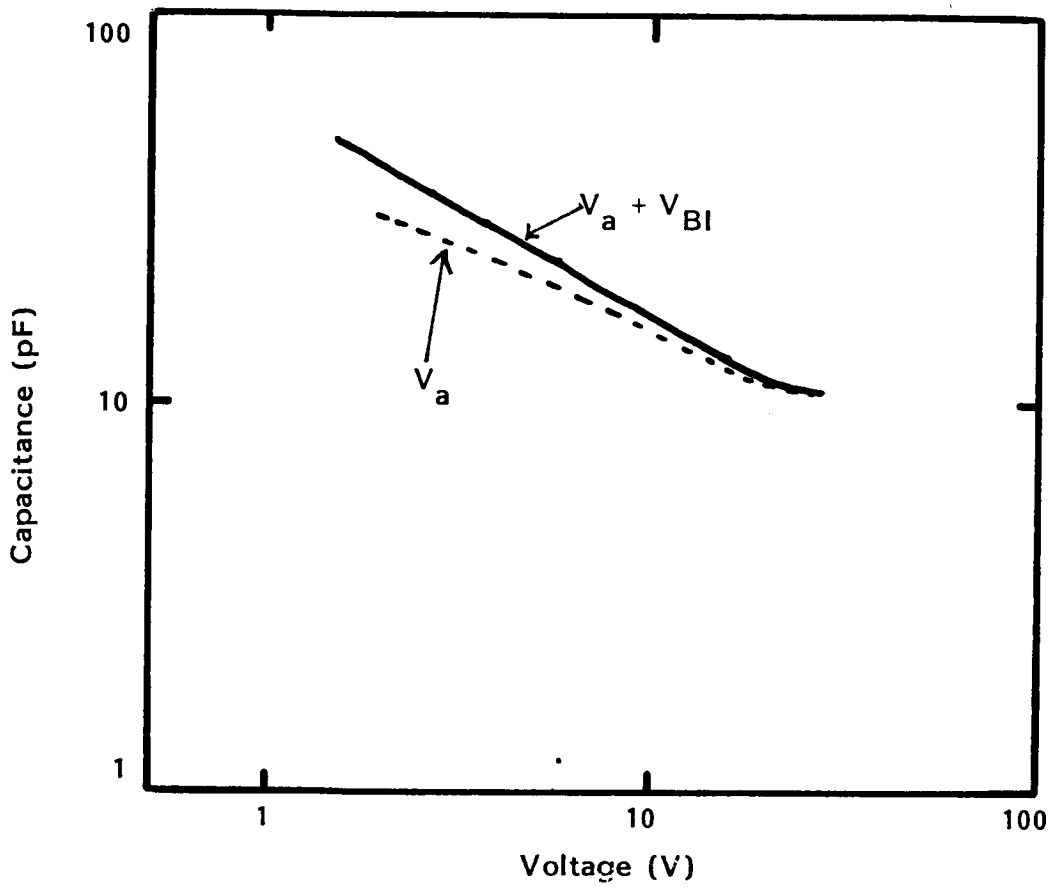
where:

w = total depletion layer thickness ($x_n + x_p$)
x_n = N-side depletion thickness
X_P = P-side depletion thickness
N_A = Hole concentration on the P-side as a function of X_P
N_D = Electron concentration on the N-side as a function of X_n
$N(w)$ = Measure of "effective" doping density

$$N = \frac{C^3}{q \epsilon A^2 \frac{dc}{dv}}$$

The profile obtained by step-etching for the N-side of this structure can be seen in Figure 3.18, along with the overall profile implied from a combination of the two profiles using the equations given above.

During March of 1983, a mechanical failure in one of the valves associated with the TMG bubbler resulted in liquid being expelled



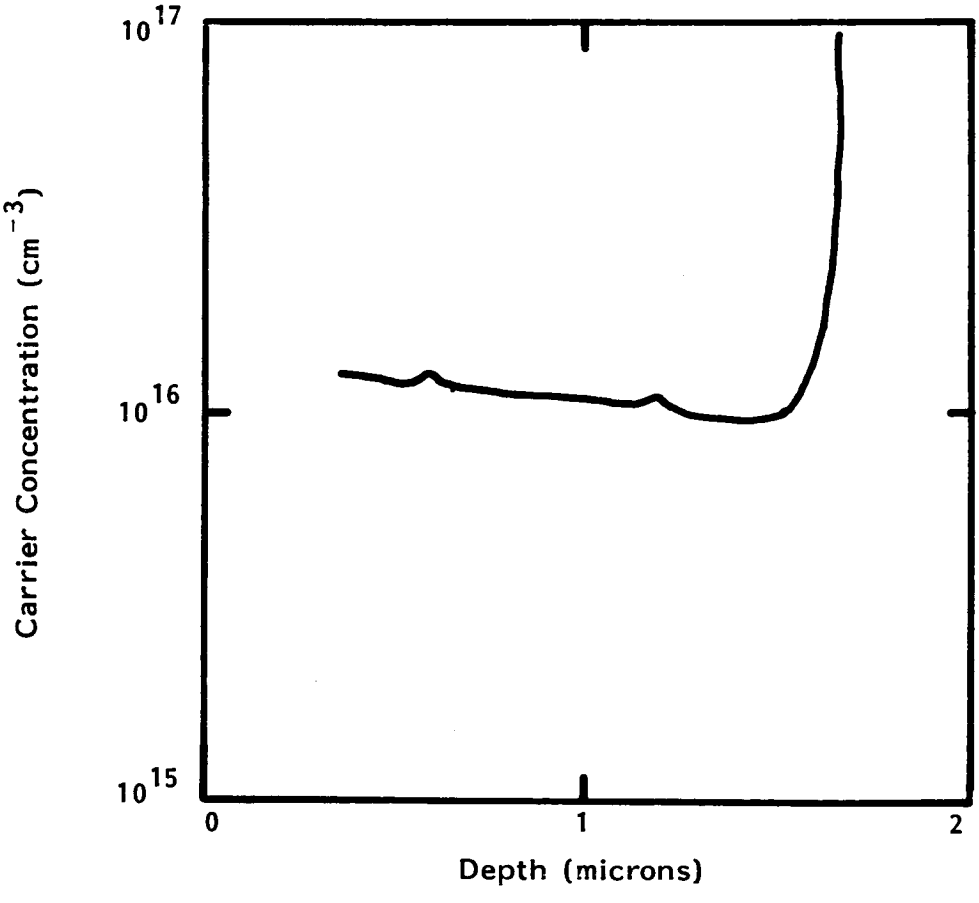
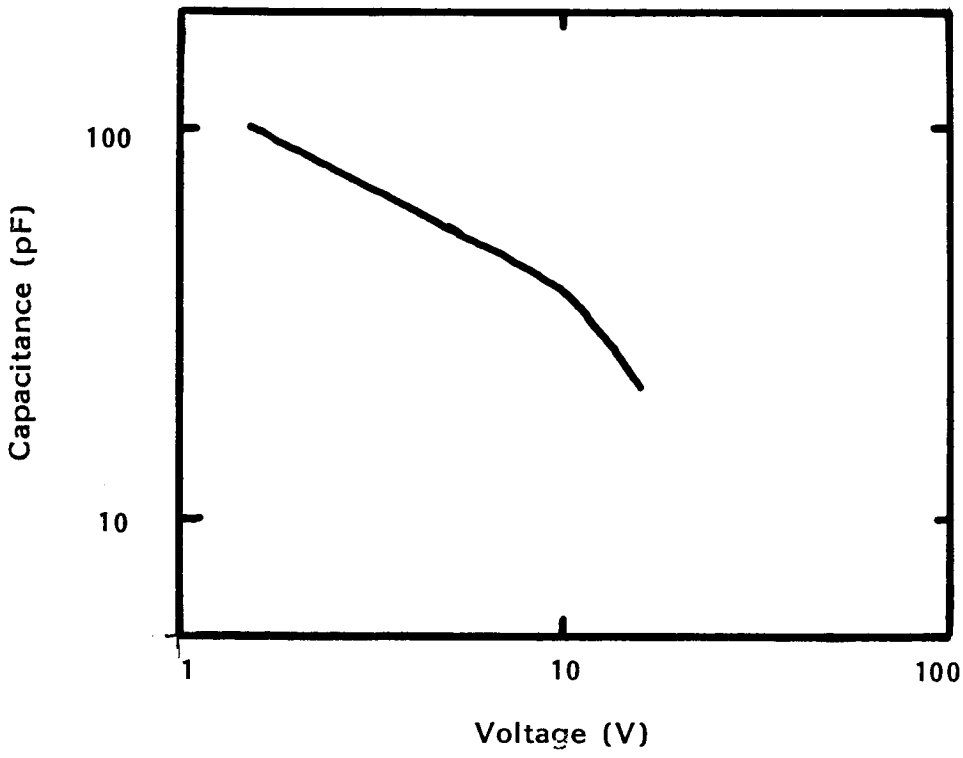


Figure 3.16 - C/V and Carrier Concentration profiles of a $p^+ - p - n^+$ structure.



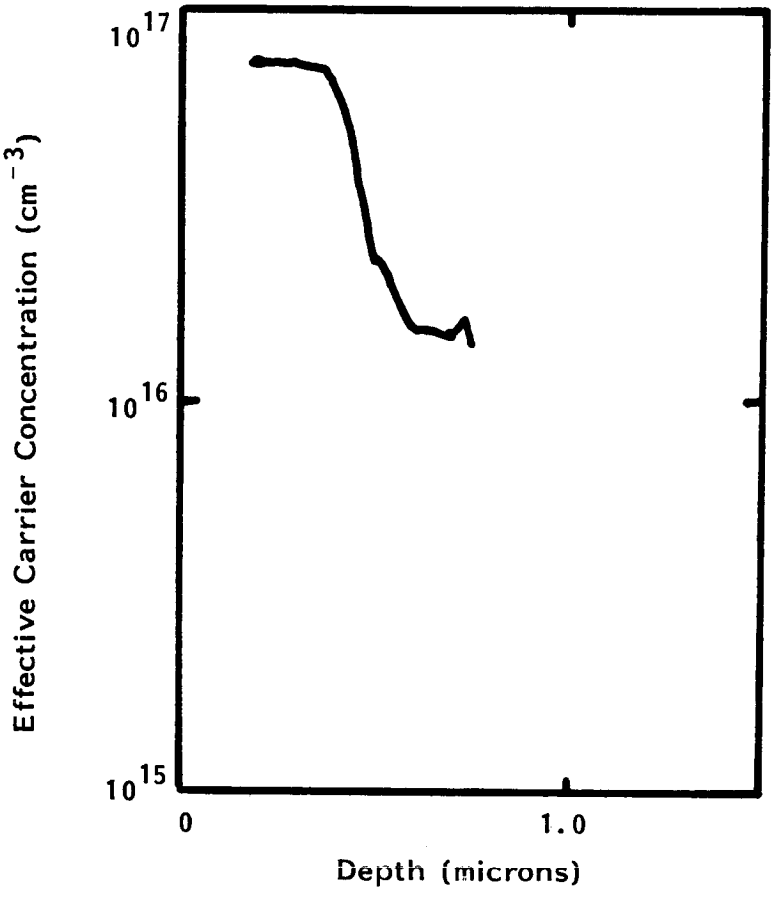


Figure 3.17 - C/V and effective doping profiles for hybrid double-drift structures.

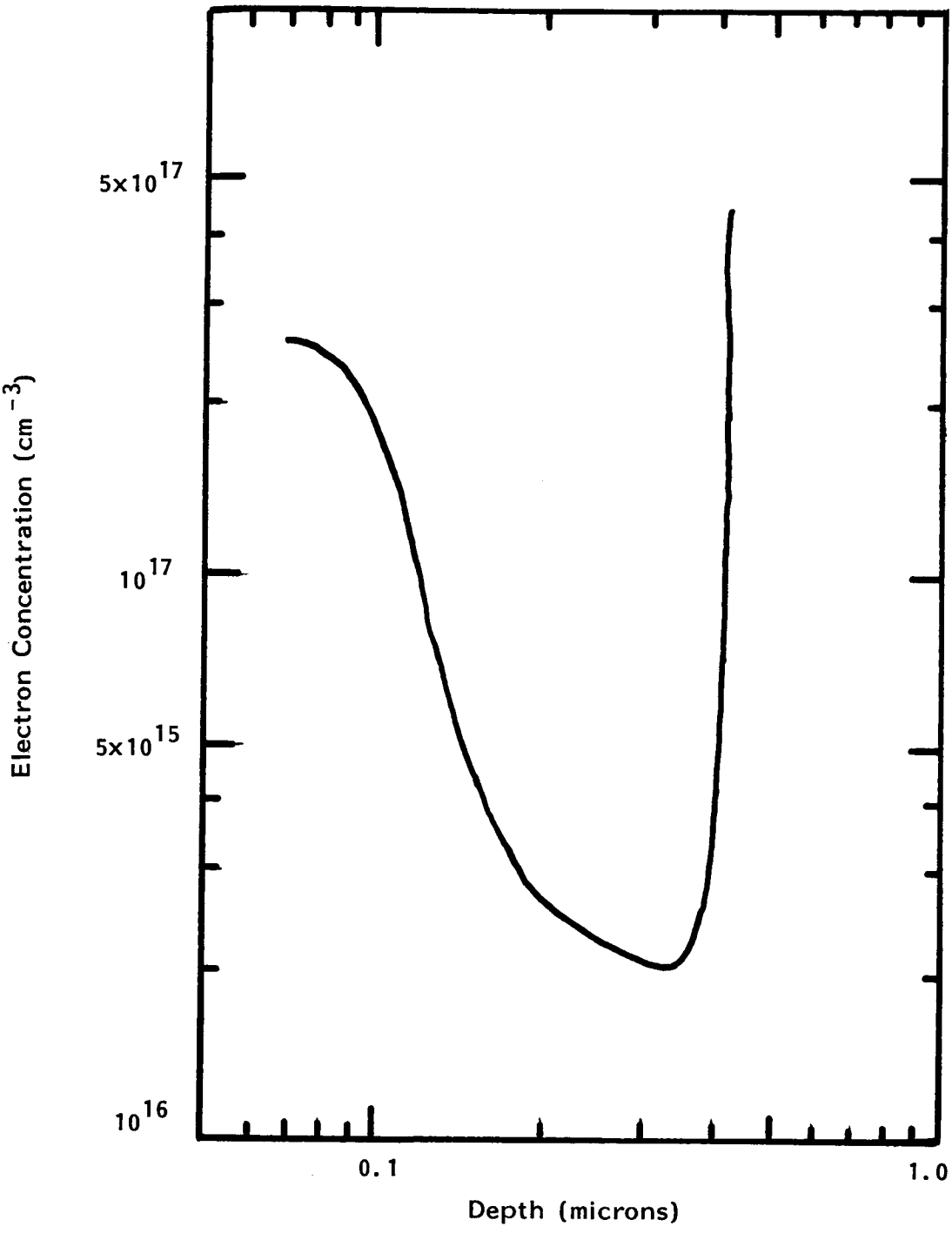


Figure 3.18 - N-side profile of H.D.D diode shown in Figure 3.17 obtained by step-etching.

from the bubbler into the rest of the gas handling system. Extensive cleaning and re-plumbing was required. As a part of this task, new valves and an automatic bubbler control system were added to the TMG channel. In addition, the newly constructed large bore reaction chamber was installed during this shutdown. A drawing of the new chamber is shown in Figure 3.19.

Once the repairs were completed, the system was re-characterized and results comparable to those obtained prior to this work were found. In an attempt to extend the usefulness of the step-etching technique for doping profile measurement, a series of P-type calibration runs were performed on semi-insulating substrates. A comparison of the results obtained from these samples using Hall effect and mercury probe C/V measurements is given in Figure 3.20. As can be seen, the capacitance/voltage technique yields results which vary widely from the more reliable Hall effect data. This confirms our earlier conclusion that the most effective method of analyzing the P-side of the Double-Drift structure is through measurements taken on the composite structure after accounting for the effects on the N-side.

In early April of 1983 the TMG source, which had been in use since March 1982, was exhausted. A bubbler which had been in-house since early 1981 was installed and found to yield heavily doped P-type epilayers, even at extremely high (100:1) arsine to TMG ratios. A new bubbler was obtained and installed. This new bubbler also exhibited residual P-type doping but to a much smaller concentration (mid-10^{16}). By increasing the As/Ga ratio to approximately 100:1, the residual doping was further reduced to the mid-$10^{15}cm^{-3}$ range. Although these results indicated that the new TMG source was not as pure as that used previously, the residual impurity levels were still at least an order of magnitude lower than the required doping concentrations for the 60 GHz IMPATT.

Further experiments were then performed in the direction of better understanding the P-type doping behavior of the system. During this work, the Polaron-Post Office Profiler was found to give reliable

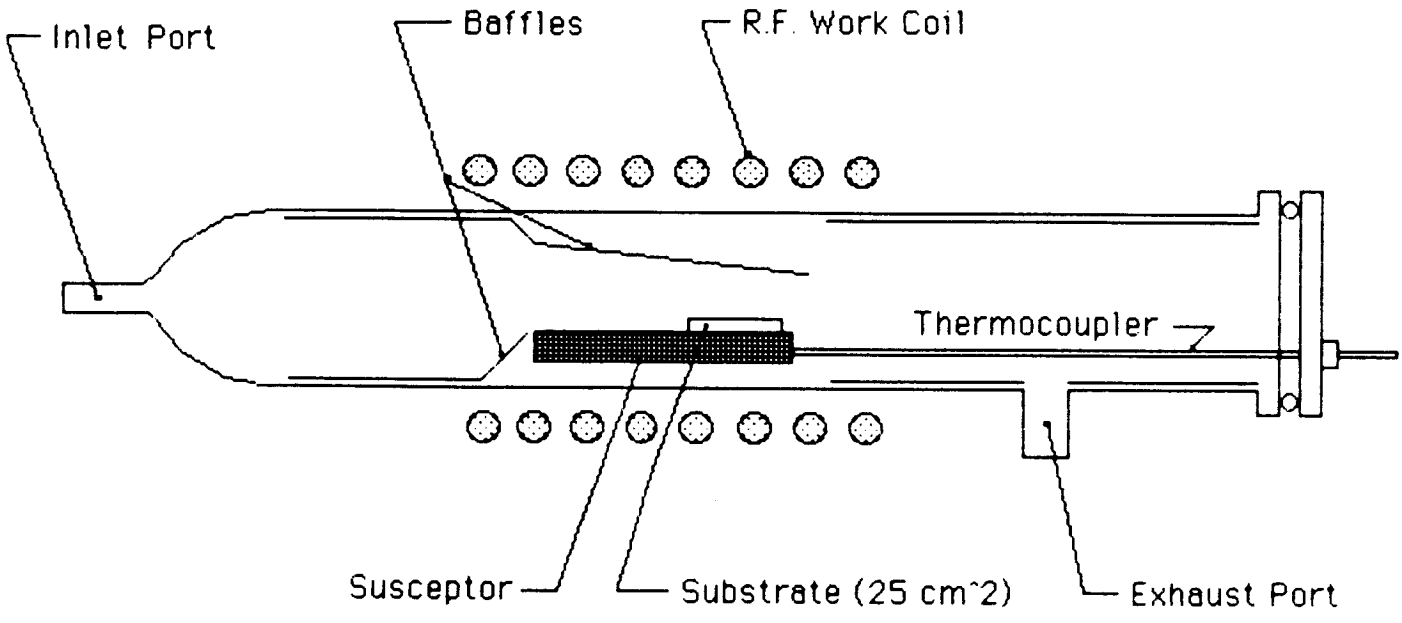


Figure 3.19 - Schematic of the New Large Bore Reaction Chamber

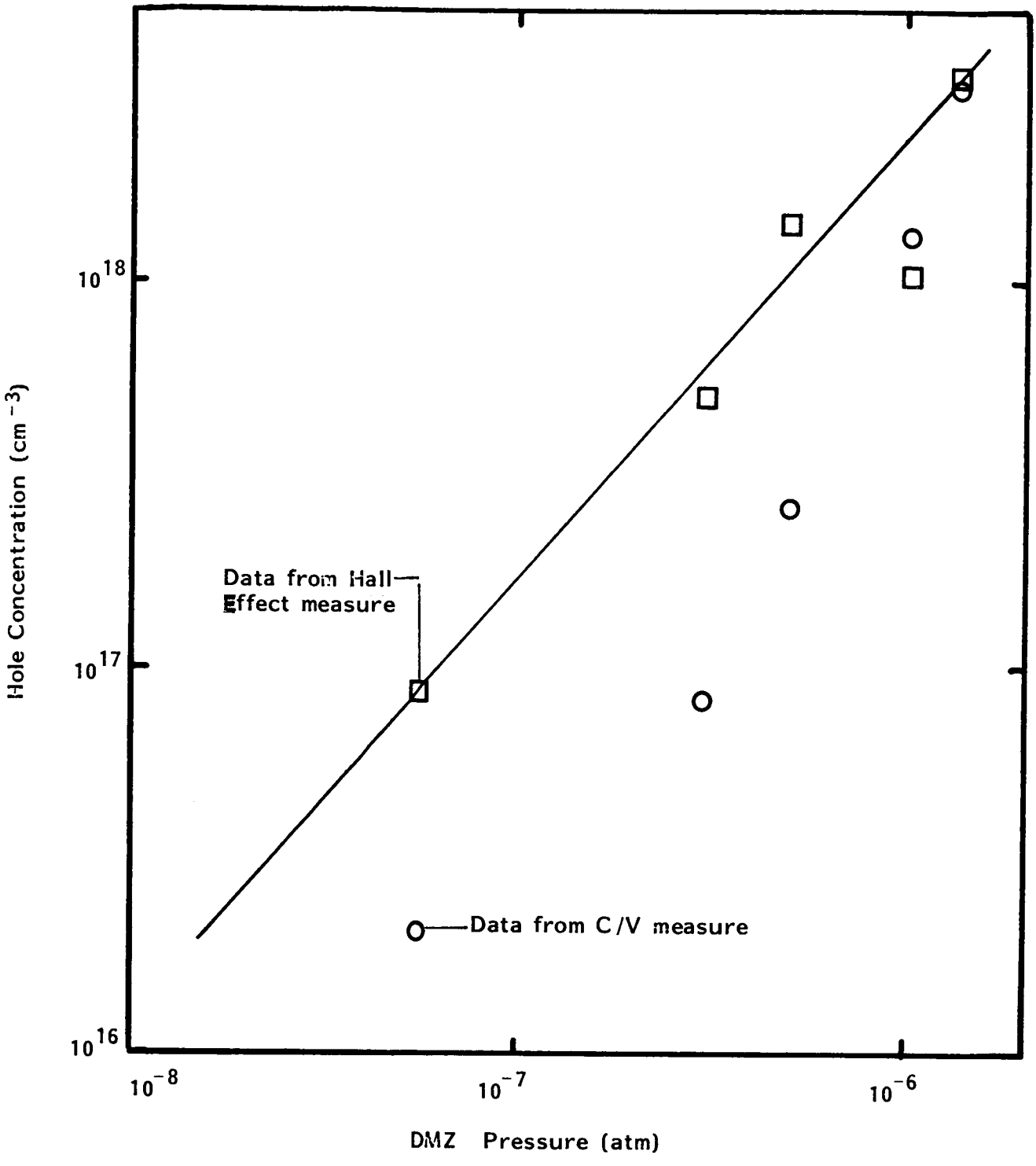


Figure 3.20 - Comparison of Hole concentration measurements by C/V and Hall Effect techniques.

P-type doping measurements providing the surface of the test sample was not heavily doped ($P<10^{17}$) and the layer thickness was greater than about 0.5 microns. A plot of the profile obtained from one experiment is given in Figure 3.21. The Polaron instrument yields good results when the doping level increases with profiled depth but yields profile smearing when profiling from a highly doped layer into a more lightly doped layer. This behavior is probably due to the effects of the sidewalls as the profiled area is etched through the layers.

During the early part of May 1983, further experiments were designed to study the epitaxial uniformity in the new large bore MOCVD reaction chamber. The average variation observed along the center-line of 2" diameter substrates (shown in Figure 3.22) was slightly less than +/- 15% when the total hydrogen flow was 5000sccm. By increasing the gas velocity within the reactor and employing a slight angle between the susceptor and the plate baffle, it was possible to improve the growth uniformity. Operationally, this angle increased the mass transfer rate along the length of the susceptor by decreasing the stagnant boundary layer and, hence, compensated for the effects of reactant depletion along the flow path.

Optimization of the gas velocity within the reaction chamber was achieved by increasing the total hydrogen flow to 9500 sccm. to obtain uniformities of slightly over +/- 5%. Although excellent results were obtained along the center-line, somewhat poorer uniformities (of up to +/- 20%) were observed for the perpendicular directions (see Figure 3.23). Since the reactor geometry was axially symmetric, it was not clear why the side-to-side variation was highly non-symmetric about the axis. Initially, it was believed that the side-to-side variation was due to a temperature difference across the quartz reactor tube. The possible thermal gradient was speculated to be due to an air flow within the reactor cabinet, preferentially cooling one side of the reactor tube. Also, it was possible that the infrared radiation emitted by the hot graphite susceptor was being reflected back onto the opposite side of the reactor tube by a nearby metal panel consequently heating that side more

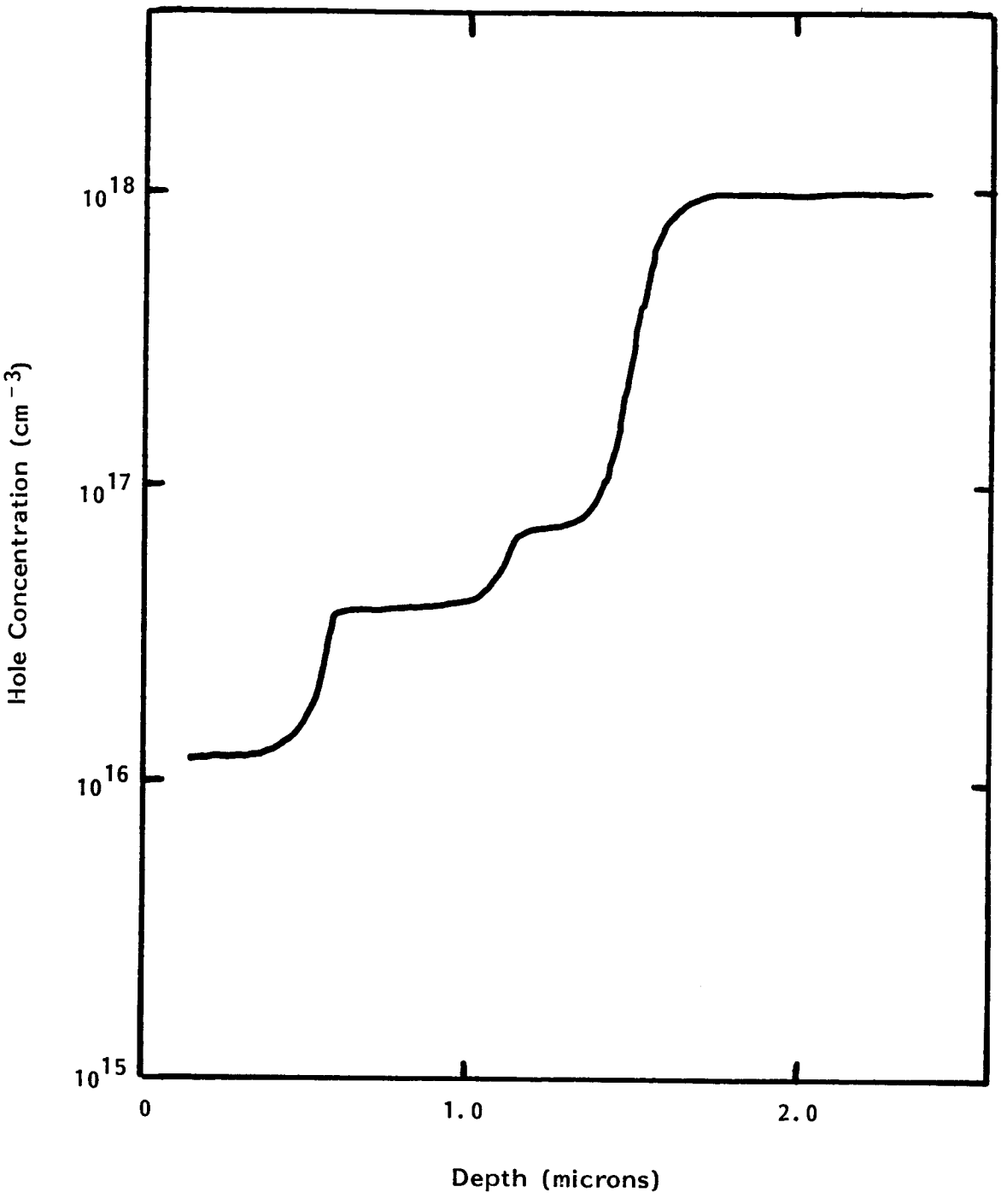


Figure 3.21 - Polaron Profiler plot of stepped p-type structure.

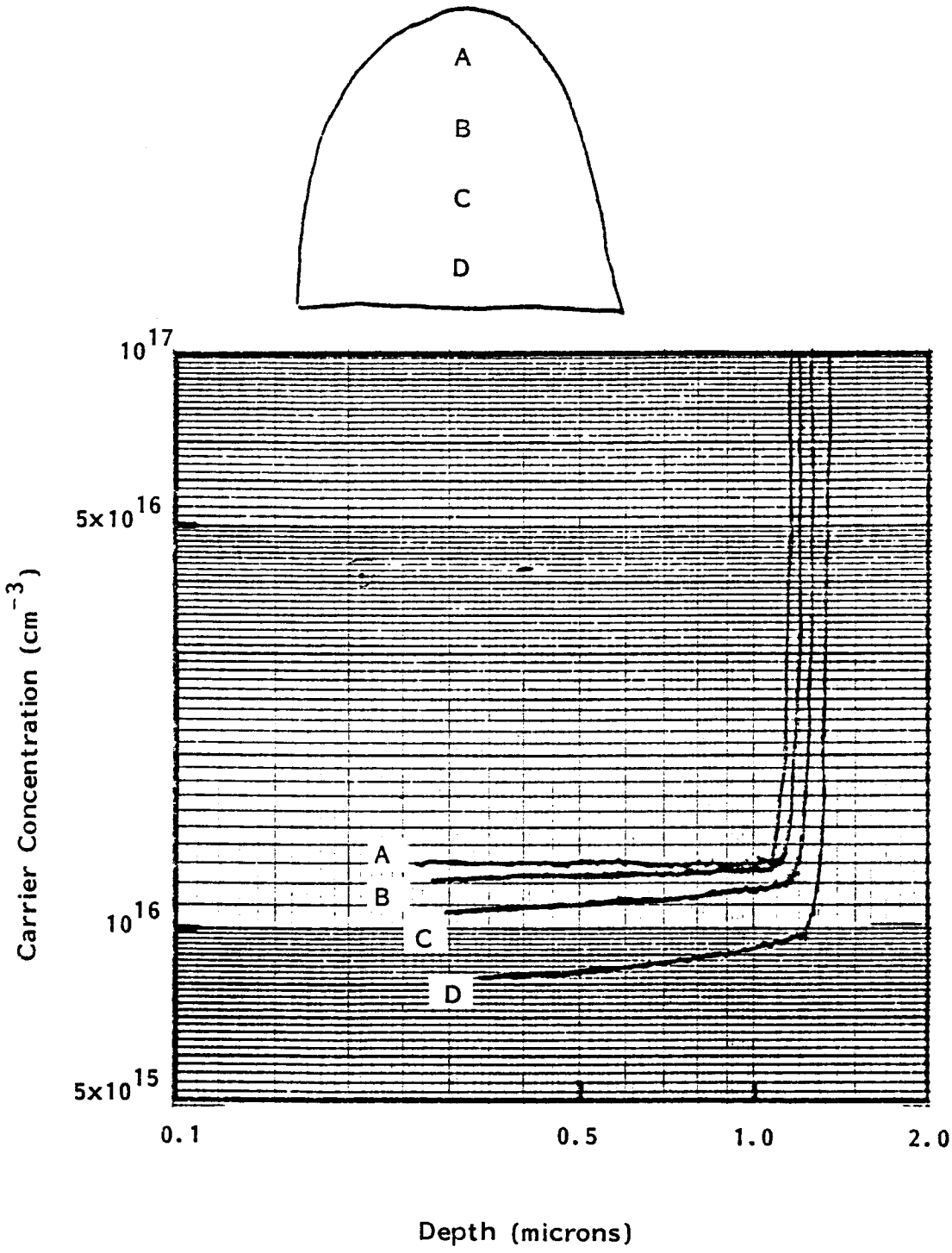


Figure 3.22 Center Line Uniformity Using a Hydrogen Flow of 5000 SCCM

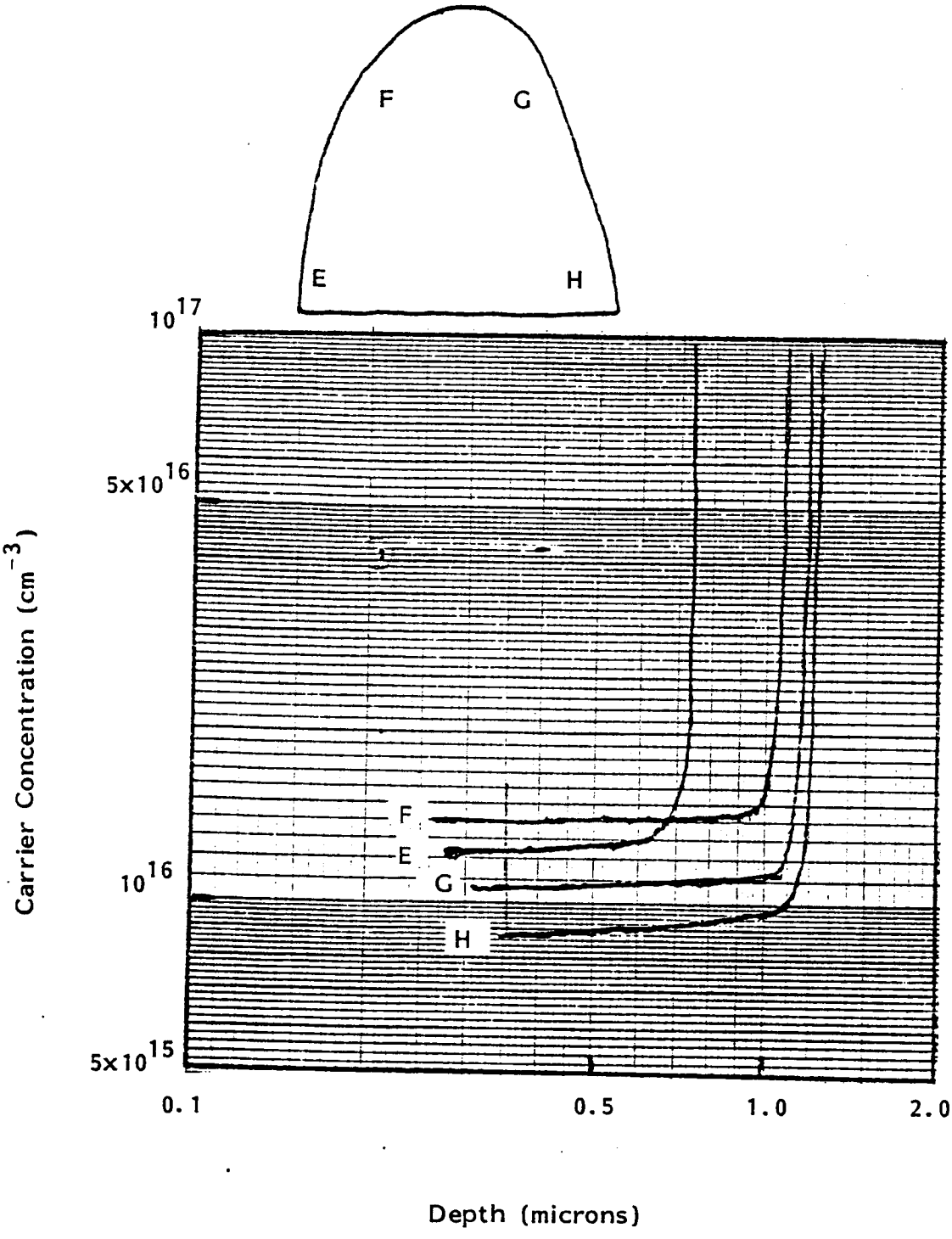


Figure 3.23 Side to Side Uniformity Using a Hydrogen Flow of 9500 SCCM

effectively than the other. To investigate this, a non-reflective air shroud was placed around the reaction tube in order to eliminate the effects of the two possibilities. The results of these experiments were virtually identical to those obtained without the air shroud. This eliminated the possibility of a thermal gradient across the reaction tube and indicated that the problem was within the reaction chamber itself.

Careful examination of the deposition patterns, on the reactor walls and internal quartzware, led to the conclusion that a swirling flow pattern was being induced into the gas stream by some elements of the quartz baffles incorporated around the susceptor. The initial attempt to eliminate the turbulent flow conditions was to incorporate an additional grid baffle at the inlet of the reactor. Any jets of gas caused by the abrupt change of dimension at the reaction chamber inlet and the narrow opening of the inlet tube should be minimized by the inclusion of a fine grid baffle. The results indicated that the grid baffle did provide some improvement for the the side-to-side uniformity. It is speculated that the grid baffle helped to maintain an even distribution of the gas stream over the susceptor by introducing a laminar flow condition through the reaction tube.

The next set of experiments was performed without the front plate baffle which formed a ramp leading to the susceptor. The exclusion of this ramp increased the side-to-side uniformity. Although excellent thickness uniformities of approximately +/- 5% (shown in Figure 3.24) were realized over the entire substrate, poor results were obtained in the doping variation. The observed variation in dopant incorporation was partially due to a thermal gradient within the susceptor. Experiments were performed to reduce these variations by adjusting the RF induction coil so as to even out the susceptor heating. As a result of expanding and contracting various portions of the induction heating work coil, the temperature distribution across the susceptor was minimized. By placing a single 2" diameter substrate on various sections of the susceptor, a "sweet zone" was located where good thickness and doping uniformities were obtained over most of the substrate.

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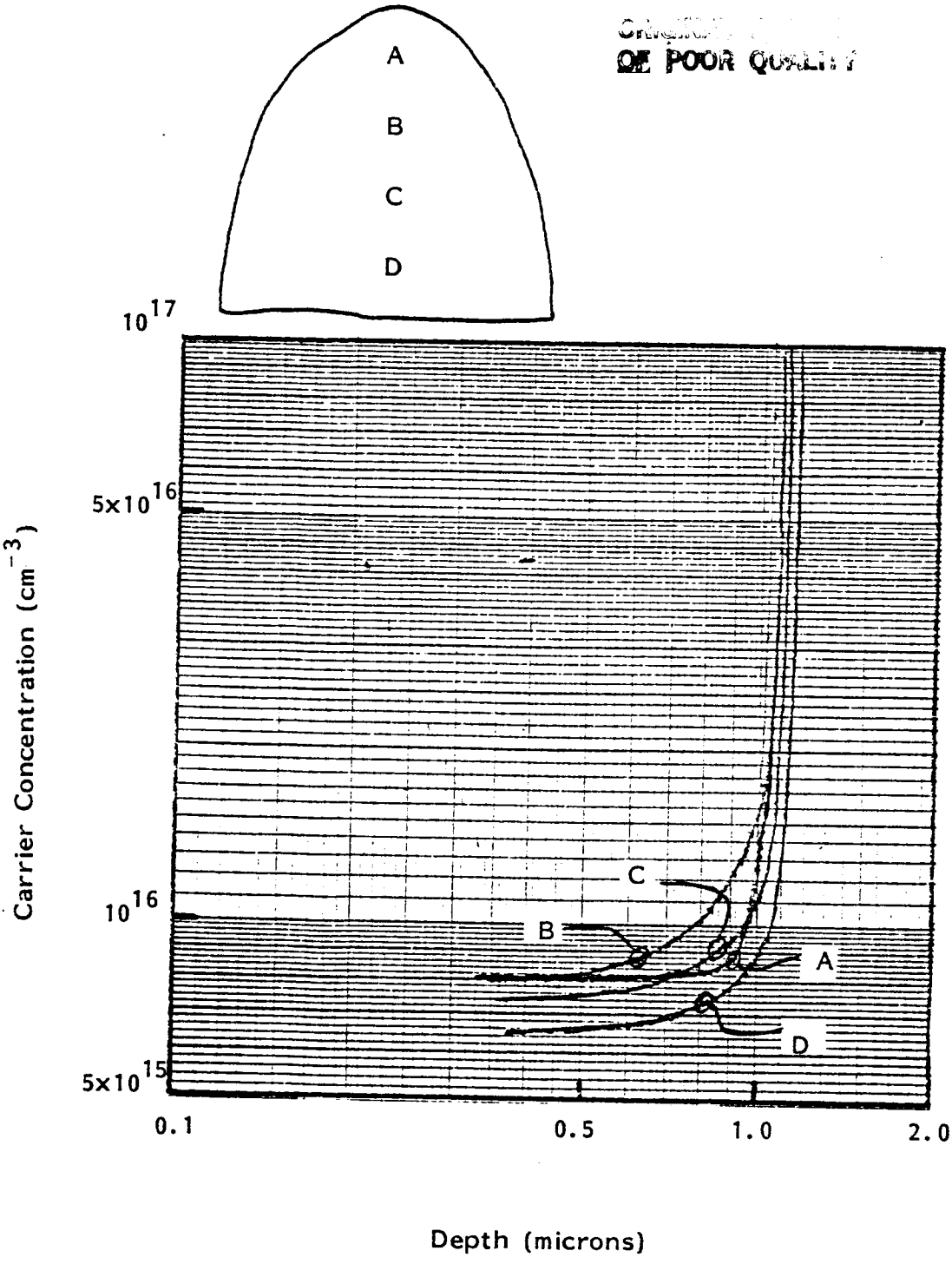

Figure 3.24 Improved Thickness Uniformities as a Result of Reconfiguring the Internal Quartzware

As a result of the uniformity studies mentioned above, several changes were made to the original configuration of the MOCVD system. With the present configuration (shown in Figure 3.25), the system can generate material with uniformities for both doping and layer thickness of less than +/- 5% variation. The large area of uniform material (shown in Figure 3.26), now available from the use of the large bore reactor, significantly increases the availability of usable material. Hence, a thorough characterization of the epilayers can be performed and, still, have sufficient area available for the fabrication of devices.

After the uniformity studies, work was directed towards establishing a new set of operating conditions that would satisfy the design specifications of an IMPATT structure. The new set of operating conditions entailed a reduction in the growth rate from 0.1um/min. to 0.05um/min., as well as decreasing the growth temperature from 650°C to 600°C. The objective in reducing the growth rate was to enhance the controllability of the system to produce sub-micron epitaxial layers. By reducing the growth temperature,the diffusion rate of intersticial dopant atoms through the material would be minimized.

In the process of calibrating the MOCVD system for a lower growth rate and a reduced deposition temperature, other growth parameters were affected. With a lower temperature, the incorporation rate of silicon dopant atoms was greatly reduced causing the background doping to be predominantly P-type. To offset this effect, the arsenic over-pressure in the reaction chamber was increased until the background doping level was 1×10^{15} electrons/cm^3. As a result of this ratio, the growth uniformity over a 2" diameter wafer degraded. To re-establish the uniformity, an increased gas velocity of 12000 sccm was employed. This solution afforded us an additional advantage since it was compatible with the condition necessary to realize sharp doping transitions.

Once the new set of operating conditions was established, several growth experiments were conducted to determine the feasibility of

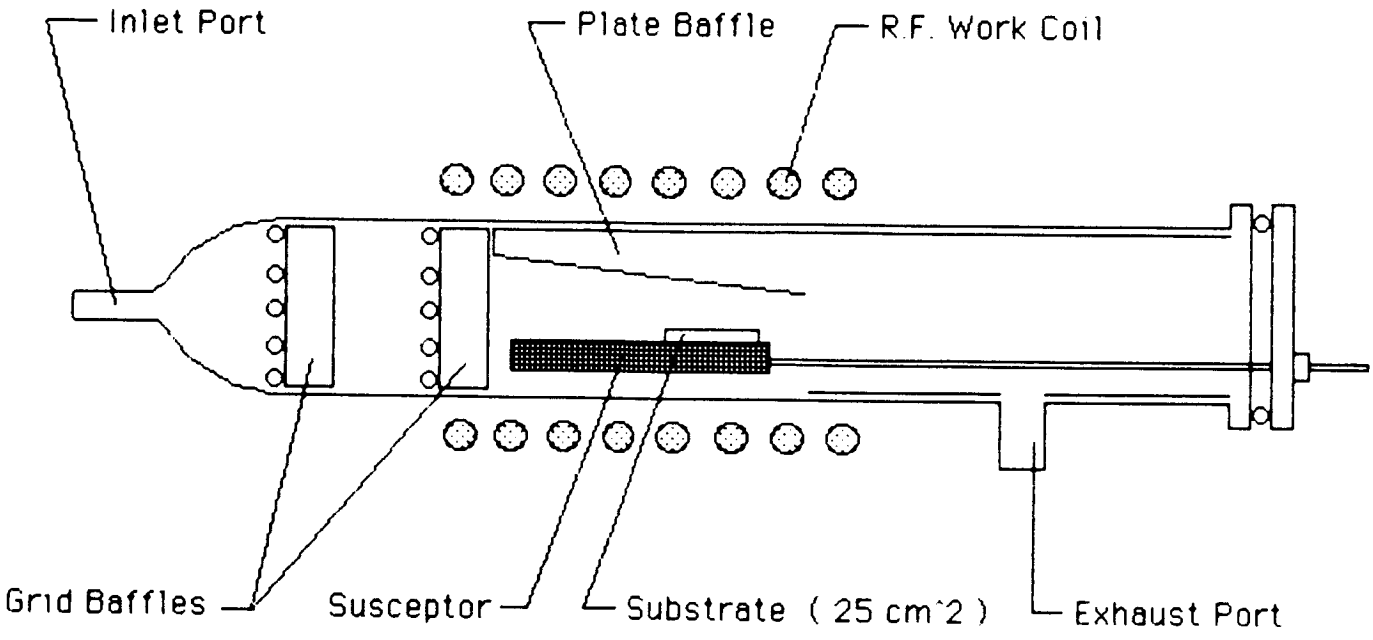

Figure 3.25 - Current Configuration of Large Bore Reaction Chamber

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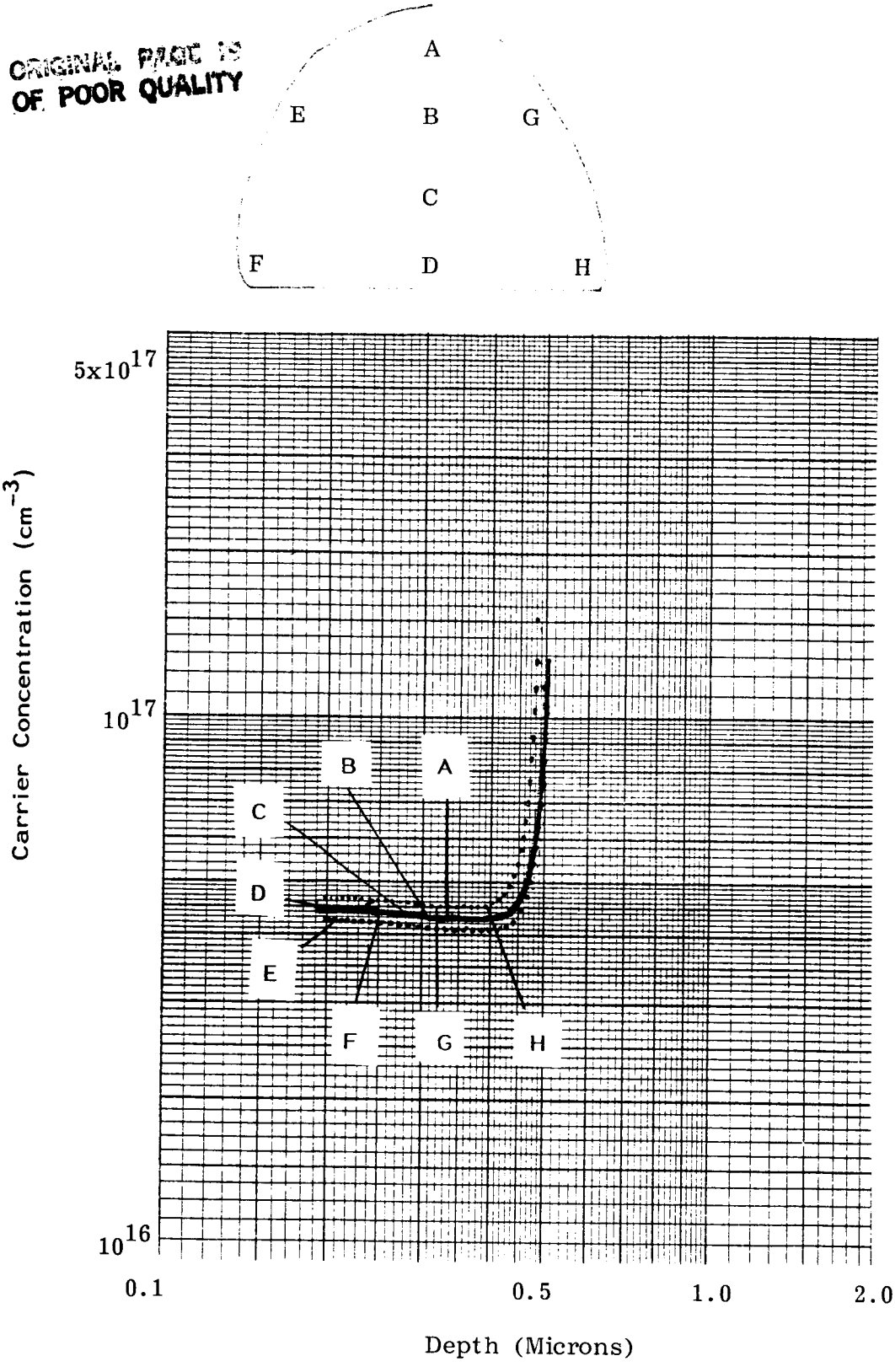


Figure 3.26 Uniformity Plot of a Large Bore Reaction Chamber

developing a two-step (non-sequential) growth procedure. The development of such a technique would facilitate a reliable and accurate method for determining the doping profile of 60 GHz HDD structures. In addition to the two-step approach, some attempts were also made at growing the IMPATT structure using a sequential (one-step) approach.

Using the design parameters given in Table 3.1, calibration growth runs were made to simulate the growth parameter necessary to produce the N and P sections of the profile. Once the proper growth conditions were optimized, the entire structure was grown by sequentially depositing the N and P portions of the structure in a single growth run.

The conventional method for characterizing material grown from a sequential run is to employ the CV/step etching technique. The objective, when employing this characterization technique, is to chemically etch away the P+ contact and p-active layers in order to expose the HI-LO side of the structure as shown in Figure 3.27. One of the inherent limitations of this technique is that it is very difficult to stop precisely at the P-active HI-N interface. As a result, the HI-N layer thickness is at best a minimum value. To further complicate this technique, the zero bias depletion width of the mercury Schottky contact consumes approximately half of the HI-N layer leaving only 600Å of material to be characterized.

Thus, to alleviate the problem associated with material characterization, a non-sequential growth procedure was investigated. The steps for this new procedure were similar to the sequential growth approach in that calibration runs were also performed to determine the appropriate growth parameters needed to achieve a specific design profile. The key difference to this new growth technique was that once a desired HI-LO doping profile was obtained, the test wafer from that run was later reused to complete the structure. After characterization, the second step of the non-sequential process (shown in Figure 3.28) was to reclean and re-load the wafer into the reactor. Using a calibrated etch, approximately 250 to 300Å of epitaxial material was removed from the HI-N

Table 3.1 Parameters of OMCVD 60 GHz HDD Structures

RUN NO.	GROWTH TECHNIQUE	N_{Hi} (Cm^{-3})	X_{Hi} (μm)	N_{Lo} (Cm^{-3})	X_{Lo} (μm)	N_{p} (Cm^{-3})	X_{P} (μm)
012884-1A	Non-Sequential	2.3×10^{17}	0.12	5.5×10^{16}	0.23	1.6×10^{17}	0.25*
020184-1A	Non-Sequential	3.3×10^{17}	0.11	6.8×10^{16}	0.22	1.84×10^{17}	0.25*
020384-1	Continuous	3.0×10^{17}	0.12*	6.0×10^{16}	0.23	3.4×10^{17}	0.25*
Design	---------	2.8×10^{17}	0.12	5.6×10^{16}	0.23	1.87×10^{17}	0.25

* Based on System's Growth Rate

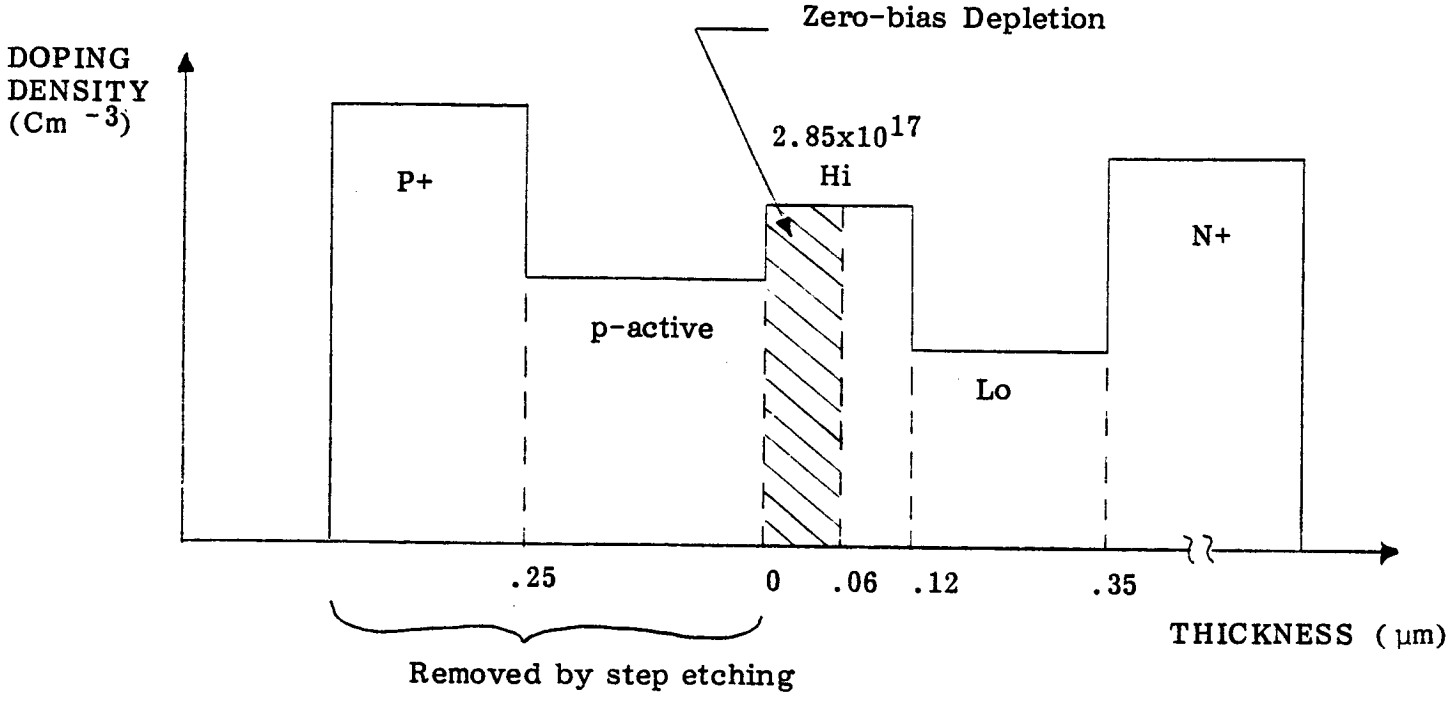


Figure 3.27 C/V - Step Etching Technique

layer. The advantages realized by this etch are as follows: (i) it allowed for the HI-N layer to be tailor-etched to its appropriate value, and (ii) it removed the native oxide and other minor damages caused during handling. Once the wafer was loaded into the reaction chamber, the P-active and P^+ contact layers were sequentially grown.

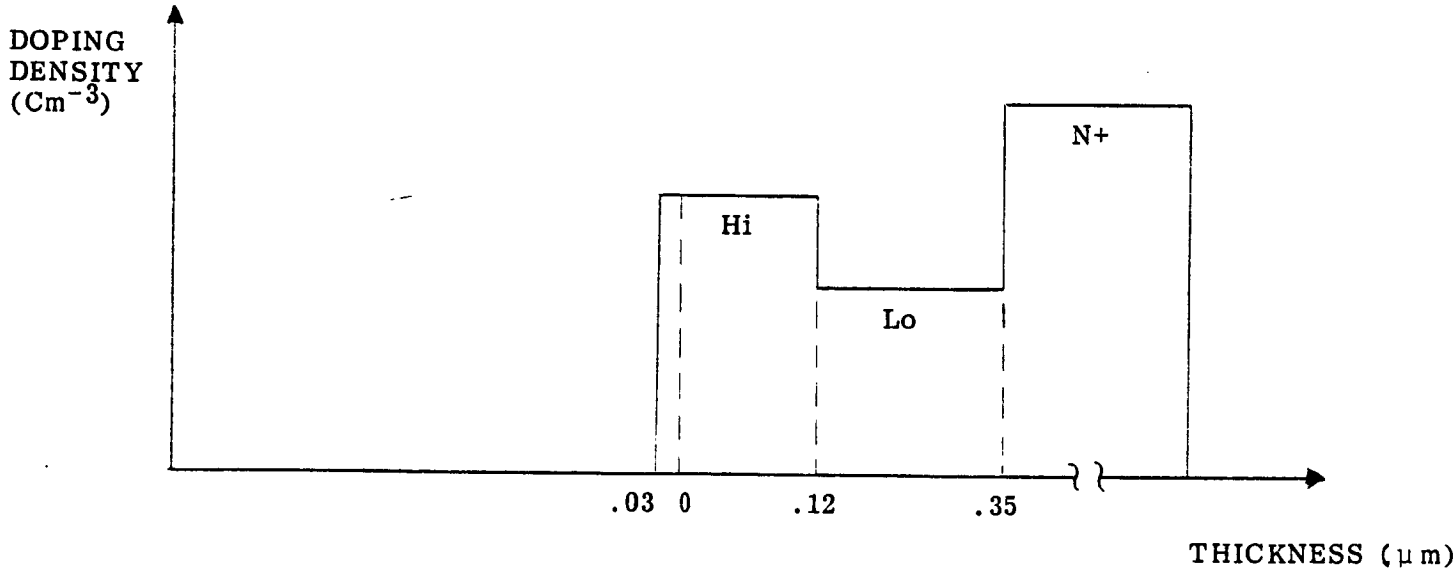
The key advantage of the non-sequential growth technique is that it allowed for the HI-LO portion of the HDD structure to be determined with more certainty and accuracy. Since the technique permits an accurate determination of the HI-LO doping profile over the entire wafer, it has the added advantage of screening the material before continuing the HDD non-sequential growth process. Furthermore, an accurate knowledge of the HI-LO doping profile will increase the accuracy in calculating the carrier concentration of the P-active layer in the HDD structure.

The success of a non-sequential growth technique can have a great impact on future characterization of submicron structures. However, the influence of this technique on the device performance/reliability may have to be determined. Since the two step growth technique is only "experimental", most of the 60 GHz IMPATT structures were grown using the sequential approach.

Because of its encouraging RF performance, doping profile parameters from H-VPE wafer #I10292 were used as guidelines for OMCVD growth attempts. Presented in Table 3.2 are the results of 3 OMCVD growth runs which were intended to duplicate the VPE I10292 structure. Of the three attempts, 030984-1B was grown using the non-sequential growth procedure as described earlier. The results from this run were very encouraging. Excellent surface morphology was achieved after depositing the P-active and P^+ contact layers. Also, sharp I-V characteristics were achieved from test mesa diodes that were fabricated from this material.

In Tables 3.2 and 3.3, a notable deviation in the actual doping values from that of expected values can be seen. This is

Hi-Lo n-active Layers



Complete Structure

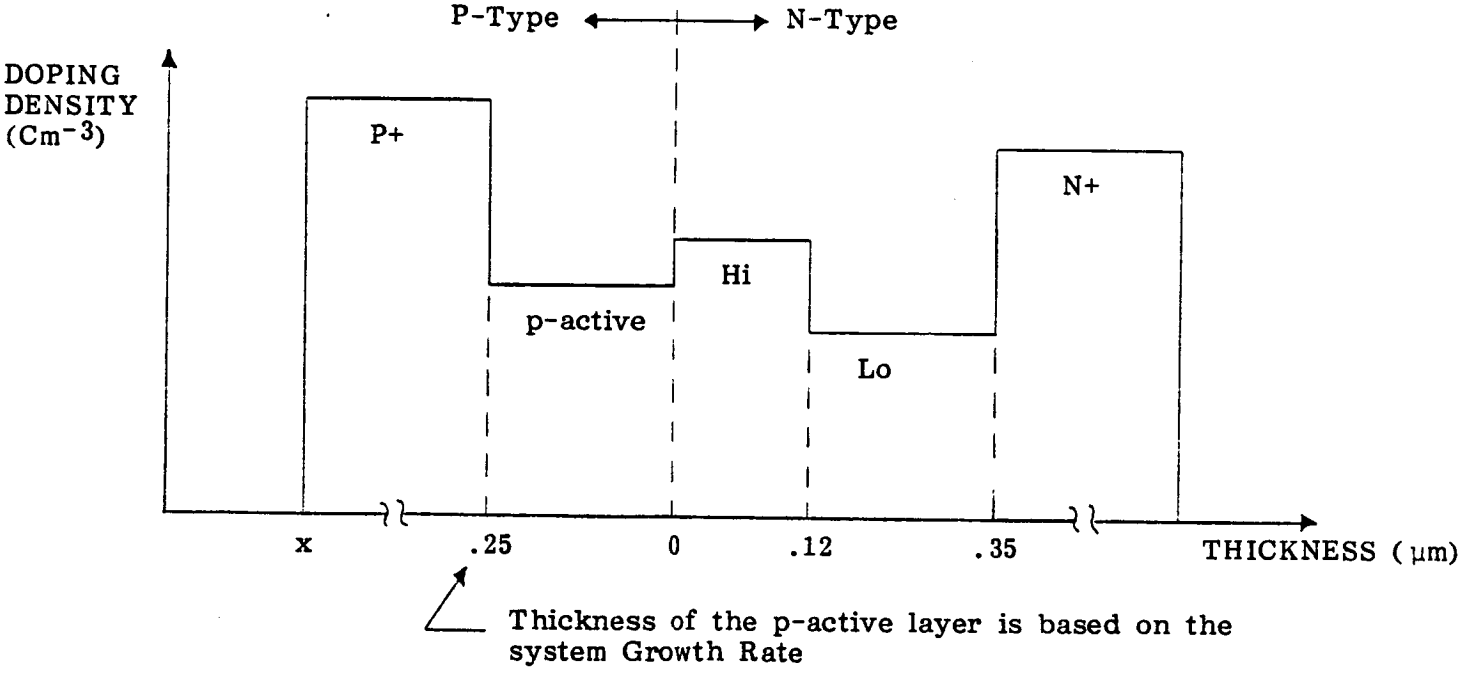


Figure 3.28 Two Step (Non-Sequential) Growth Technique

especially true for the P-active layers which were doped with various concentrations of dimethylzinc. During actual device growth runs, the lines were saturated thereby allowing a greater amount of dimethylzinc to be injected into the reaction chamber. This resulted in a higher P-type doping level than anticipated. Realizing this, the injected concentration of dimethylzinc for each subsequent growth run was intentially decreased while maintaining the same saturation conditions that were used for earlier runs. As a result, the P-dopant levels decreased accordingly.

In early April of 1984, the AsH_3 source, which was in use since September 1983, was exhausted. A new AsH_3 cylinder was installed and found to yield heavily doped n-type background layers, even at extremely low AsH_3/TMGa ratios. Another new cylinder of AsH_3 was obtained and installed. This new cylinder of AsH_3 also exhibited n-type background concentrations in excess of 1E18 electrons/cm^3. The cylinders were returned to the distributor for analysis of the AsH_3. A gas chromatograph analysis of the material uncovered a high concentration, 1200ppm, of hydrogen sulfide, (H_2S), impurities in the AsH_3. An immediate replacement cylinder of AsH_3 was installed and determined to be high purity material. Unintentionally doped layers were measured to have background carrier concentrations of approximately 1E14 electrons/cm^3 with mobilities in excess of 7500 cm^2/V-sec.

Subsequent to establishing the low background doping level, several growth experiments were conducted to revalidate the system's growth uniformity. Using the original growth conditions and the predetermined "sweet zone" of the reaction chamber, preliminary uniformity results were discouraging. As in earlier studies, the axial doping and thickness variations were measured to be +/- 10% from the mean. The side-side variations were in excess of +/- 15% from the mean.

An examination of the recorded data and observations during previous and current uniformity studies led to the conclusion of a possible turbulent flow pattern within the reaction chamber. This was evidenced by deposition patterns on the reactor wall and internal quartzware. The irregular deposition patterns and poor uniformities were

Table 3.2 Results of Three OMCVD Growth Attempts Intended to Duplicate the VPE I 10292 Structure

RUN #	GROWTH TECHNIQUE	N_{HI} (CM^{-3})	X_{HI} (μM)	N_{LO} (CM^{-3})	X_{LO} (μM)	N_P (CM^{-3})	X_P (μM)
I10292 DESIGN	----	3.2×10^{17}	0.14	8.6×10^{17}	0.21	1.15×10^{17}	0.18*
022884-2	SEQUENTIAL	2.15×10^{17}	0.15	6.5×10^{16}	0.19	4.2×10^{17}	0.18*
030984-1B	NON-SEQUENTIAL	3.2×10^{17}	0.13	7.5×10^{16}	0.20	2.2×10^{17}	0.18*
030984-2	SEQUENTIAL	2.9×10^{17}	0.14	6.4×10^{16}	0.20	3.5×10^{17}	0.18*

* BASED ON SYSTEM GROWTH RATE

Table 3.3 Additional Growth Experiments Attempting to Obtain the Specified Parameters of both the Haddad and NCSU Design Models

RUN #	GROWTH TECHNIQUE	N_{HI} (cm^{-3})	X_{HI} (μm)	N_{LO} (cm^{-3})	X_{LO} (μm)	N_P (cm^{-3})	X_P (μm)
HADDAD DESIGN	----	2.85×10^{17}	0.12	5.6×10^{16}	0.23	1.87×10^{17}	0.25
030784-2	SEQUENTIAL	2.9×10^{17}	0.12	7.4×10^{16}	0.2	4.6×10^{17}	0.25*

* BASED ON SYSTEM GROWTH RATE

RUN #	GROWTH TECHNIQUE	N_{HI} (cm^{-3})	X_{HI} (μm)	N_{LO} (cm^{-3})	X_{LO} (μm)	N_P (cm^{-3})	X_P (μm)
NCSU DESIGN	----	3.2×10^{17}	0.06	4.5×10^{16}	0.32	8.3×10^{16}	0.42
031684-2	SEQUENTIAL	3.3×10^{17}	0.08	5.4×10^{16}	0.28	1.84×10^{17}	0.42*
031984-1	SEQUENTIAL	3.4×10^{17}	0.08	4.0×10^{16}	0.29	1.3×10^{17}	0.42*

speculated to be symptoms of an increased backpressure through the reaction chamber caused by a clogging dust separator. To investigate, an attempt was made to remove the dust separator from the systems's exhaust manifold. In the process of removing the dust separator, pyrophoric TMG vapors, that were trapped inside the pores of the activated charcoal, were exposed to the surrounding air causing the unit to spontaneously ignite. Fortunately, the aftermath of the fire left minimal damage to the OMCVD reactor. As a result of this incident, the reactor was shut down for some time to repair the damage. During the shutdown, the remains of the exhaust manifold were dismantled and replaced with a disposable charcoal filter unit.

As a result of reducing the backpressure through the reaction chamber, additional uniformity tests revealed a significant improvement in the growth uniformity within the "sweet zone" of the reaction chamber. The overall measured growth uniformity for both doping and thickness that were obtained from these test runs had, on the average, variations of less than 6%.

Because of another incident, unrelated to the operation of the system, concern was raised regarding the safety of the OMCVD reactor. As a result, a considerable amount of time was spent in reviewing every aspect of its operation. After scrutinizing each step of the operation, a set of recommended procedures for running the OMCVD system was generated. Subsequent to this effort, the decision was made from a safety standpoint, to temporarily shut down the OMCVD system until a new location could be found to accomodate the entire system. The objective in relocating the system was to provide a secure area that was self-contained and isolated from the production epitaxial area.

While plans were being worked out to accomodate the OMCVD reactor, the decision was made to reconstruct the plumbing network of the OMCVD system. During the interim period, several projects were aimed at implementing safety measures and improve the operational characteristics of the system.

The original gas handling panels of the OMCVD system was comprised of compression fittings. In the interest of obtaining the highest level of safety and growing high purity OMCVD epitaxial layers, the gas handling panels were re-assembled. This involved the use of high integrity face-to-face seal fittings in conjunction with "butt-welded" interconnecting joints.

Anticipating extended lead times, major components such as mass flow controllers were returned to the manufacturer with instructions to repair and re-calibrate. Meanwhile, appropriate lengths of 316 stainless steel tubings were prepared for the gas panels. The inner walls of the tubing were solvent cleaned and then passivated using a dilute concentration of hydrofloric acid.

In the process of reconstructing the gas panels, modifications were also made in the original layout of the TMG bubbler network. Instead of having the mass flow controller downstream of the TMG bubbler, it was relocated upstream of the bubbler to prevent it from being constantly exposed to and, hence, clogged by, TMG vapors. To enhance the versatility of the OMCVD system, its gas handling panel was configured for the possible addition of a second bubbler such as one consisting of trimethylaluminum (TMAl) for growing ternary compounds.

The original design of the bubbler network made it tedious and unsafe to replace the bubbler containing the pyrophoric TMG. In the new design, a manual bypass valve was installed close to the bubbler cylinder to minimize the length of "dead volume" that would contain TMG vapors. In addition to the bypass valve, a vacuum transducer was installed so as to enhance the purging of residual TMG vapors from the bubbler network.

Apart from the gas panels, attention was focussed on the modification of the original loading port of the OMCVD system. To establish a particulate free environment, in which precleaned substrates are loaded into the reaction chamber, a laminar flow module was mounted

above the loading port. Using the "push-pull" concept, clean air would be exhausted by the in-house ventilation system as it overwhelms the loading compartment.

The dopant gases, originally housed under the reactor, were placed in vented gas cabinets situated in an adjacent gas chase. The AsH_3 and HCl gas cylinders, which were also located in the gas chase, were connected to the reactor through single jacketed stainless steel lines. In case of an emergency, each source gas could be shut-off by means of a remote controlled high pressure valve in conjunction with a cylinder valve turn-off apparatus.

Shown in Figure 3.29 is a layout of the entire OMCVD reactor room showing the various components and location of the above mentioned OMCVD reactor and gas/mechanical chase. The objective for designing a separate OMCVD facility was to provide an environment that would contain an accidental fire or gas release. The periphery of the lab is constructed of U/L approved fire rated doors and 2-hour minimum fire rated walls. In the event of a gas release, booster fans will assist the dedicated ventilation system in the lab to maintain a negative room pressure. Located in and around the OMCVD reactor as well as in the gas/mechanical chase are toxic gas and hydrogen gas monitors. These are tied in with visual and audible alarms. In addition to the monitors, there are mushroom switches located in each room for emergency shut-down of the entire lab.

After the reconstruction, work on characterizing the various OMCVD system parameters was performed. A series of growth experiments, designed to investigate the quality of the two source materials, were conducted using a wide variety of conditions, namely: different seed temperatures, growth rates and AsH_3/TMG ratios. Relatively thick (10 to 20um) layers were grown using a range of AsH_3/TMG ratios. Hall measurements of the resulting material indicated that the purity of the two source materials was sufficient to yield low background (1E14 electrons/cm^3), high room temperature mobility (>7500 cm^2/V-sec) material.

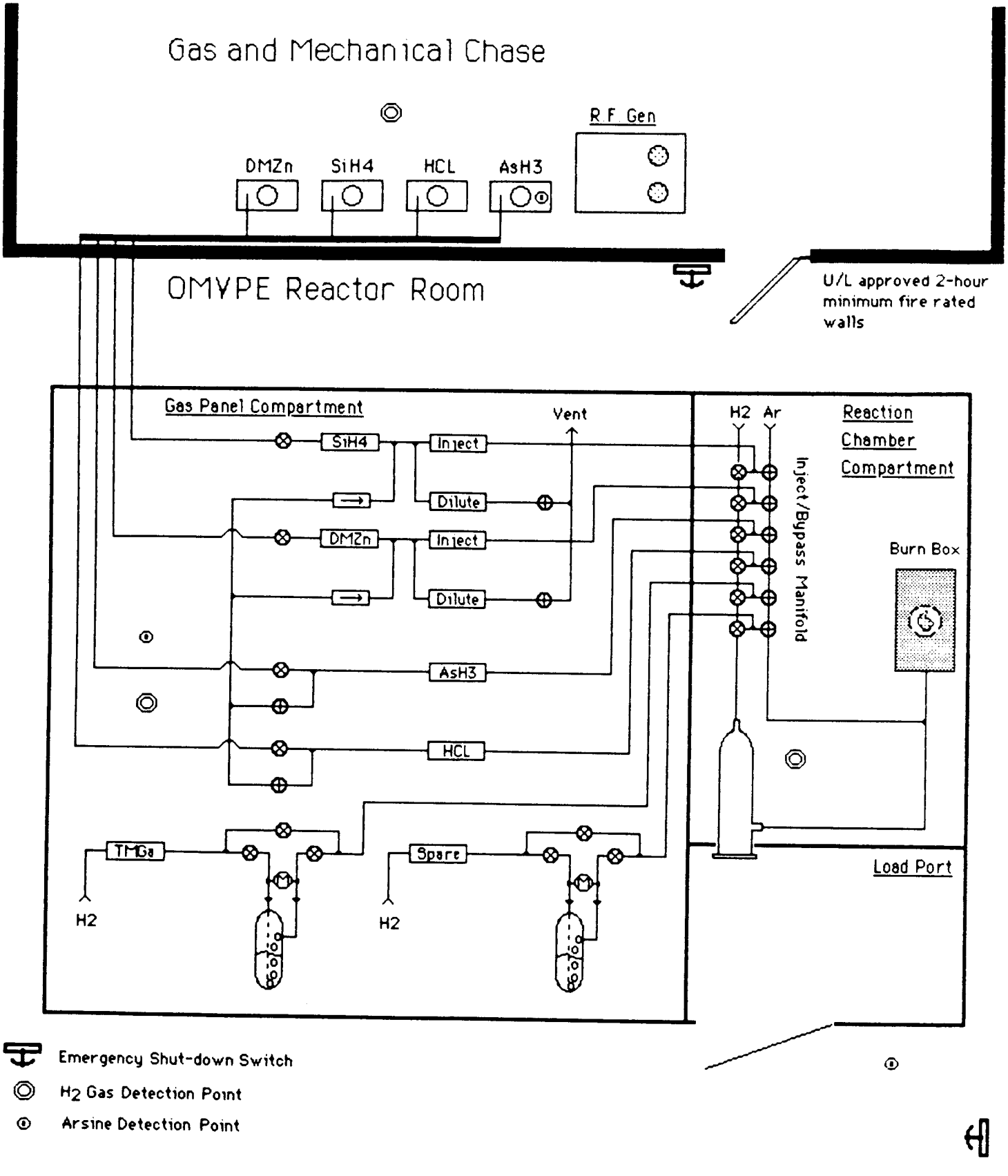


Figure 3.29 - Schematic layout of the OMCVD facility

Using the previous system geometries, several growth runs were performed to revalidate the growth uniformity over the "sweet zone" in the reaction chamber. During these runs, it was noted that the backpressure in the reaction chamber was greatly reduced as a result of the ventillation pull on the burn-off stack. It is believed that the slight vacuum, resulting at the reaction chamber exit port, enhances the laminar flow conditions through the reaction chamber. With the slight vacuum at the exit port, improved growth uniformities were achieved (see Figure 3.30). On the average, the growth variations have been less than 5% for both doping and thickness.

In conjunction with revalidating the growth uniformity, experiments were also conducted so as to generate a curve of electron density versus mole fraction of silane. The resulting log-log curve in Figure 3.31 shows the linear relationship that exists between these two parameters for the N- dilution network.

Soon after calibrating the n-dilution network, a similar set of experiments were conducted so as to generate a hole density versus mole fraction of Dimethylzinc curve. The resulting material from these growth runs were processed into test mesas. The tungsten probe/C-V measurements of these test mesas were conducted on a new computer controlled test equipment. The doping versus depth (N vs X) profiles provided the data points that were used to generate the hole density verses mole fraction of DMZ curve for the p-doping network. The resulting log-log curve in Figure 3.32 shows the linear relationship that also exists between these two parameters for the p-dilution network.

Presented in Table 3.4 are the results of all growth attempts, since the reconstruction, which were intended to duplicate the 60 GHz design structures.

Realizing the importance of accurately determining the doping concentration and thickness of the epitaxial material, steps were taken to have SIMS analysis made on a structure grown in the OMCVD system.

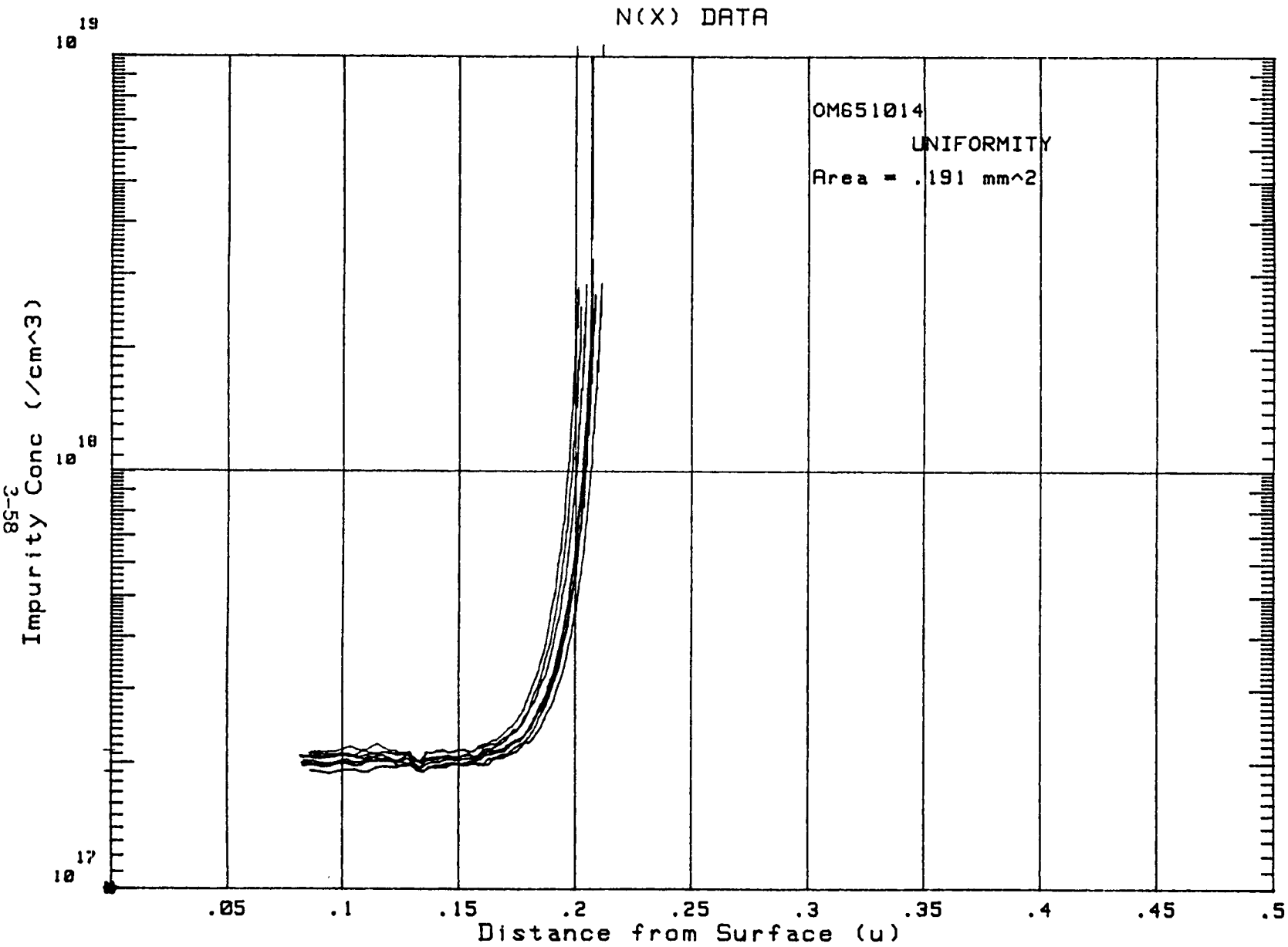


Figure 3.30: Growth uniformity over a 25cm^2 area. Doping and thick variation typically less than +/- 5% from the mean.

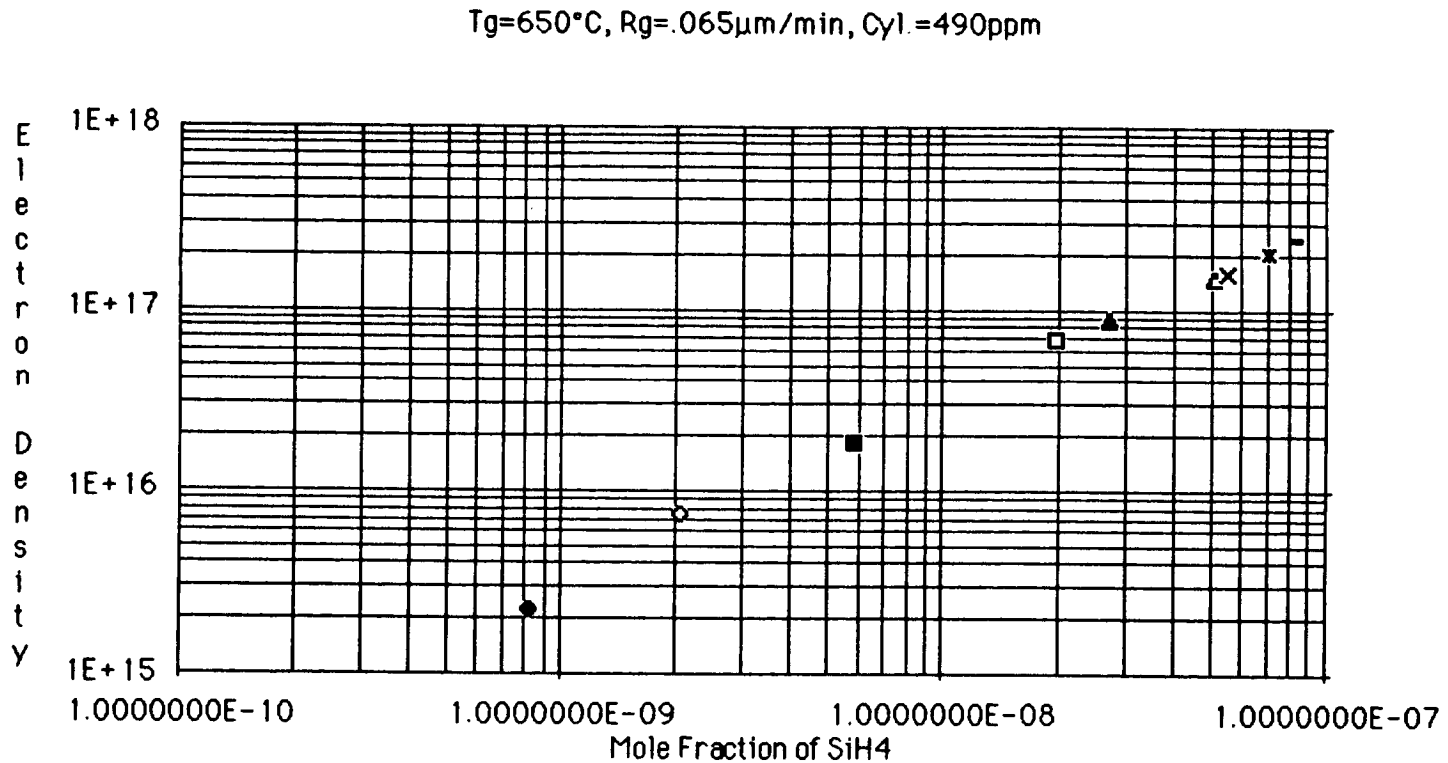


Figure 3.31 - Electron Density versus Mole Fraction of SiH4 for the N-dilution Network

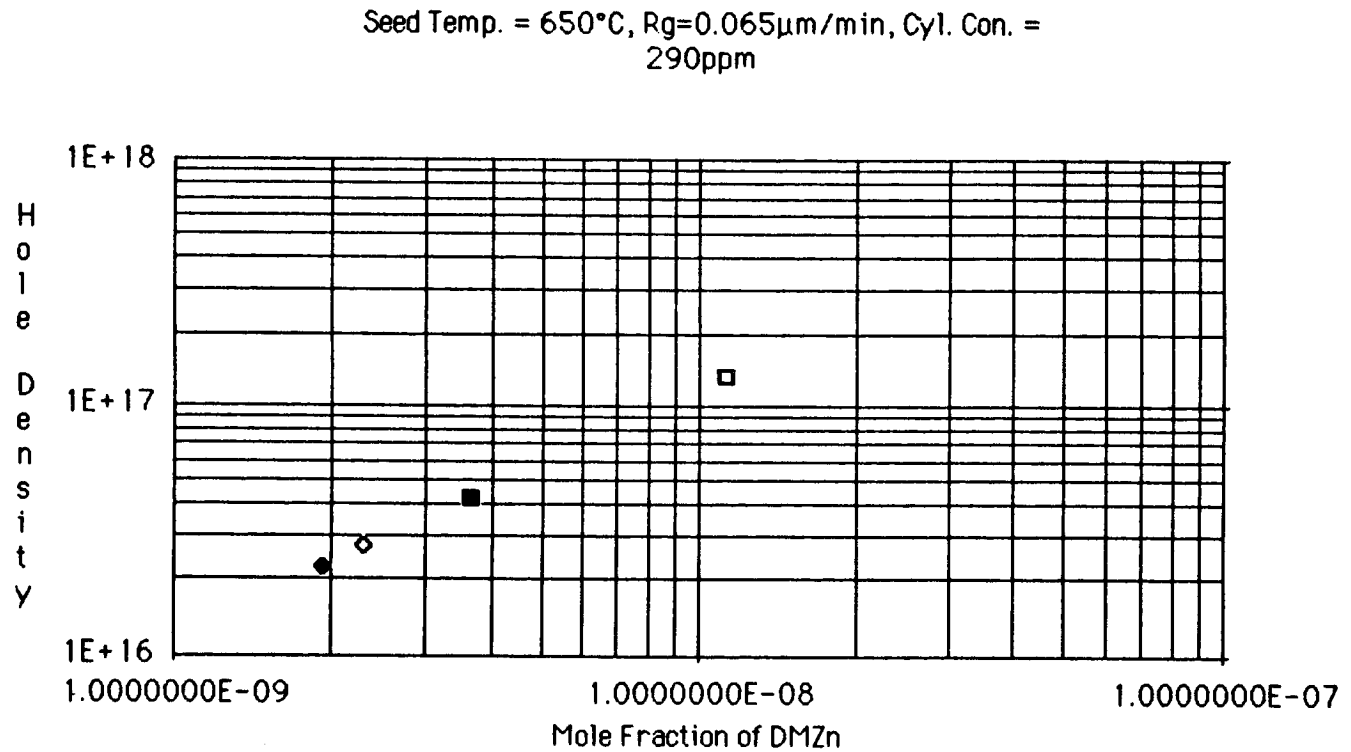


Figure 3.32 - Hole Density versus Mole Fraction of DMZn for the P-dilution Network

Table 3.4 - Epitaxial Characteristics of 60GHz Hybrid Double Drift Impatts

Run#	NLo (cm^-3)	XLo (μm)	NHi (cm^-3)	XHi (μm)	Np (cm^-3)	Xp (μm)	Vb (Volt)
0M851042	'7.1-9.4E16	0.21	2.8E17	≥0.14	'1.2-0.87E17	0.30*	14.8
0M851043	'7.0-9.0E16	0.22	2.8E17	≥0.14	'2.9-2.0E17	0.30*	12.4
0M851044	'8.2-10E16	0.21	2.8E17	≥0.14	'2.9-2.0E17	0.30*	12.8
0M851045	'7.8-9.0E16	0.20	2.6E17	≥0.12	'3.0-1.9E17	0.30*	14.0
0M851046	'7.0-8.5E16	0.22	2.6E17	≥0.12	'2.5-1.4E17	0.30*	14.1
0M851048	8.2E16	0.23	2.8E17	≥0.10	'2.6-1.6E17	0.27*	13.3
0M851049	'9.0-10E16	0.27	3.0E17	≥0.15	'2.6-1.5E17	0.27*	13.2
0M951052	'8.8-10E16	0.31	3.3E17	≥0.14	'2.0-1.2E17	0.30*	13.3
0M951054	'7.3-8.3E16	0.30	3.0E17	≥0.15	'9.3-9.0E16	0.30*	15.0
0M951055	7.9E16	0.30	2.9E17	≥0.11	'8.5-7.6E16	0.30*	15.3
0M951056	7.2E16	0.30	2.7E17	≥0.12	1.1E17	0.30*	16.8
0M951058	6.8E16	0.30	2.7E17	≥0.09	1.2E17	0.30*	14.4
0M951059	6.2E16	0.30	2.9E17	≥0.11	1.3E17	0.28*	14.6
0M951060	6.2E16	0.30	3.0E17	≥0.12	1.3E17	0.28*	14.0
I10293 Design	7.8E16	0.25	2.8E17	≥0.14	'1.7-1.0E17	0.28	12.5

Run#	NLo (cm^-3)	XLo (μm)	NHi (cm^-3)	XHi (μm)	Np (cm^-3)	Xp (μm)	Vb (Volt)
0M851050	'4.5-6.0E16	0.34	3.0E17	≥0.094	'1.5-1.0E17	0.43*	20.5
0M951051	'4.5-6.0E16	0.34	3.0E17	≥0.094	'1.2-0.9E17	0.43*	22.0
NCSU Design	4.5E16	0.32	3.2E17	0.06	8.3E16	0.42	

Run#	NLo (cm^-3)	XLo (μm)	NHi (cm^-3)	XHi (μm)	Np (cm^-3)	Xp (μm)	Vb (Volt)
0M951062	4.8E16	0.2	2.5E17	≥0.11	1.2E17	0.25*	15.4
0M951063	4.6E16	0.24	2.7E17	≥0.12	1.4E17	0.25*	15.3
0M1051064	5.6E16	0.25	2.8E17	≥0.13	1.7E17	0.25*	14.4
0M1051065	5.9E16	0.23	3.0E17	≥0.13	1.4E17	0.25*	13.4
Haddad Design	5.6E16	0.23	2.9E17	0.12	1.8E17	0.25	

* Based on the system's growth rate, $Rg_{(p)}$ = 0.064μm/min, which was determined by SIMS analysis on Run# 0M851049.

' Non-homogeneous doping distribution

Shown in Figure 3.33 is the resulting profile of Run# OM-85-1049 generated by SIMS analysis. The information obtained from the SIMS profile provided calibration data to fine-tune the OMCVD system's growth parameters. Additionally, the SIMS profile allowed for a closer inspection of the doping transition between layers and the uniformity of the doping concentration within a layer. The transitions observed in the profile were very encouraging. The abruptness of the transitions from one doping level to another was well within 250Å. At the interface between the p-active and P+ layers, the redistribution of zinc atoms via diffusion is not evident. The relative doping levels and thicknesses obtained from the SIMS analysis were surprisingly close to the results obtained from C/V measurements. A comparison between the two results is shown in Figure 3.33. From SIMS analysis and C/V measurements, nonhomogeneous doping distributions within the LO-N and p-active layers were observed.

To achieve optimum performance from a 60 GHZ double-drift IMPATT device, homogeneous distribution of the doping concentration within a layer is essential. Several growth experiments were performed to investigate the effect of ramping the injected concentration of SiH_4 during the LO-N growth phase. The results indicated that the increasingly ramped concentration of SiH_4 compensated for the autodoping caused by the desorbtion of residual silicon from the internal quartzware surface. The residual Si, lingering in the reaction chamber from the pervious N+ buffer layer, becomes entrained in the gas stream and arrives at the growth surface. The reduction of the doping gradient within the LO-N layer, seen in Run #OM-85-1048, resulted from the ramping procedure. In addition to ramping, another approach was investigated in which extended purge phases were introduced subsequent to growing the N+ buffer layer. The result, observed in Run #OM-95-1055, was comparable to ramping in that the extended purge phase had flushed the reaction chamber of residual silicon.

Initial experiments to reduce the slope of the p-active doping profile involved the use of a counter slope technique during the p-layer growth. The attempted counterslope appeared to be, in the case of

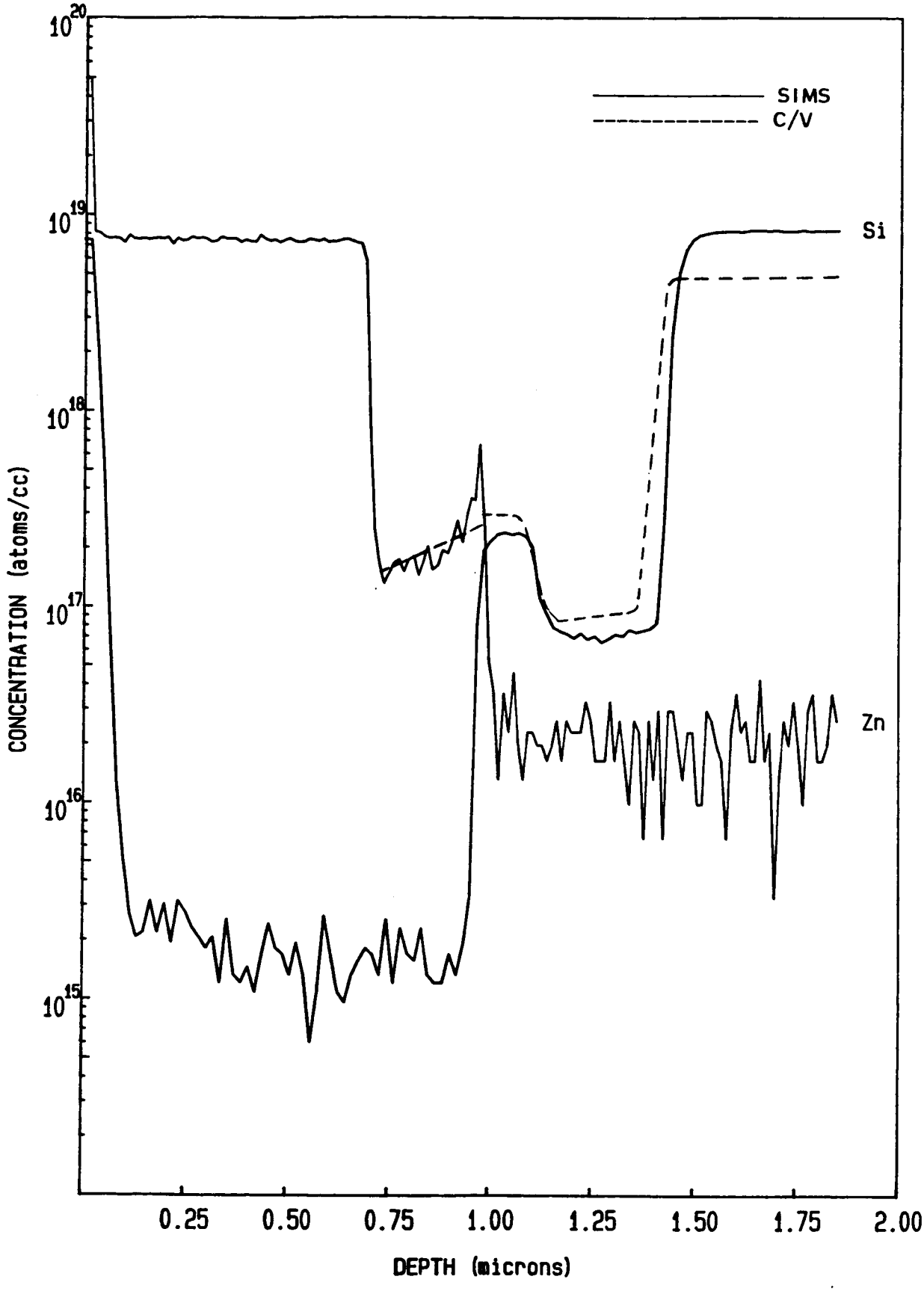


Figure 3.33: SIMS and C/V analysis of OMCVD wafer #1049.

Run #OM-85-1046, ineffective in reducing the doping gradient. However, subsequent growth experiments with an extended purge phase prior to growing the p-active layer had evidenced a significant reduction of the p-active doping gradient (see Run #OM-95-1054 and OM-95-1055). Nevertheless, further reductions were necessary. A series of experiments to reduce the slope of the p-active doping gradient involved incremental increases in the purge phase prior to growing the p-active layers. The results from these experiments showed a significant decrease in the p-doping gradient.

The mechanism that controls the doping distribution within the p-active layer could be explained as follow: During the extended purge phase, the growth environment in the reaction chamber becomes arsenic rich. The arsenic rich deposits, in the vicinity of the hot susceptor, will impede the premature decomposition of TMG. Consequently, a uniform flux of Ga specie arrives at the growth surface simultaneously with the Zn specie. Therefore, the p-active layer doping distribution, grown in such an environment, would be homogeneous.

The slope of the p-doping gradient for the initial growth experiments, utilizing a 2 minute purge phase, was in excess of 2.25E17/ cm^3. When the purge phase was increased to 10 minutes, a notable improvement (0.22E17/cm^3) was observed. The final results of these growth experiments demonstrated that purging phases in excess of 20 minutes were sufficient to eliminate the nonhomogeneous doping distribution within the p-active layer. Shown in Figures 3.24-3.26 are the resulting C/V tungsten probe measurements ulitizing various p-active pregrowth purge phases.

In conclusion, extensive efforts during the term of this program were directed toward the developement of an OMCVD growth technology capable of producing 60 GHz double drift IMPATT devices. Several device quality structures, which qualified for further processing into double drift devices, were grown during this period. Among the major accomplishments achieved during this period were:

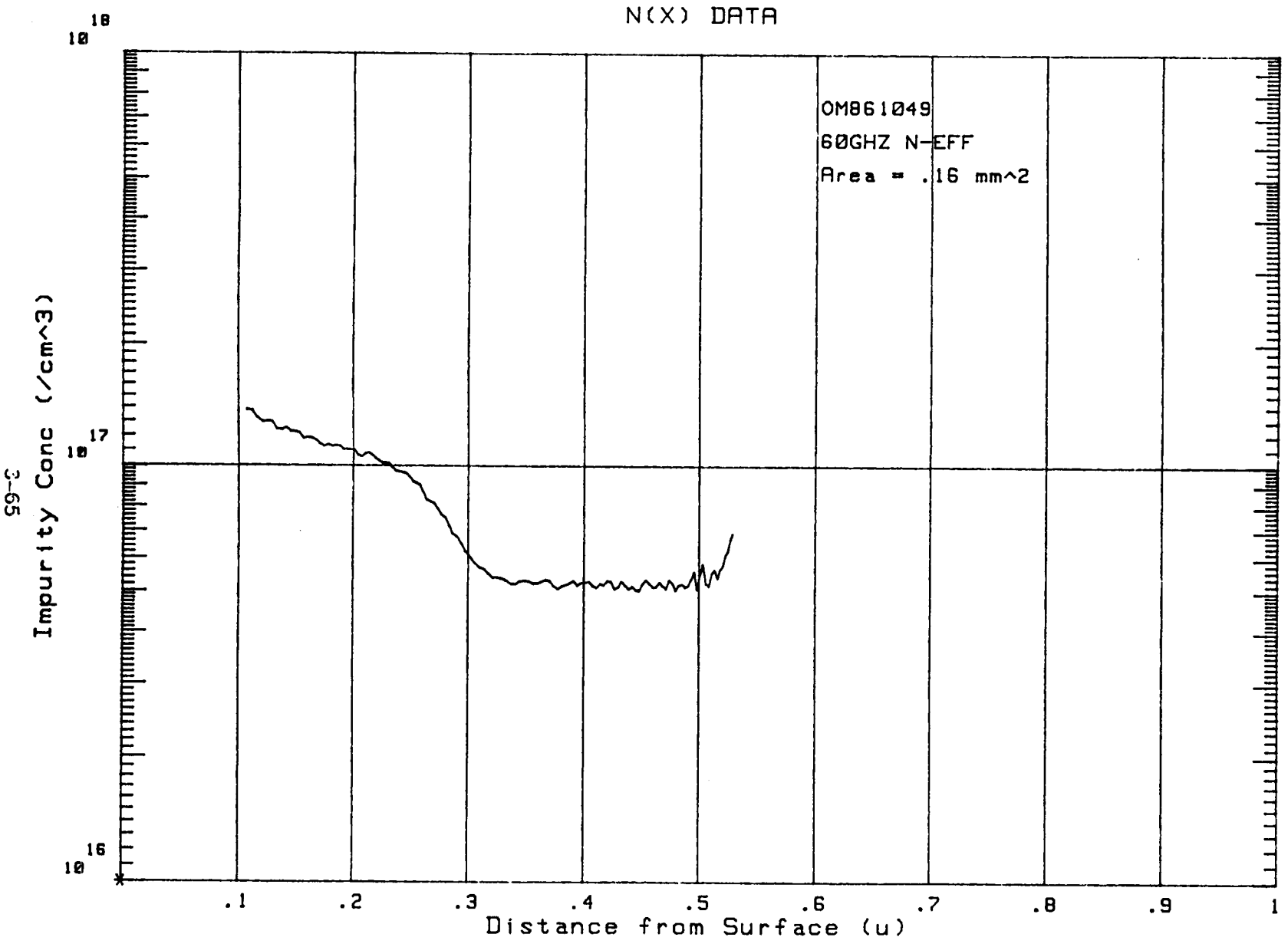


Figure 3.34: Composit profile of run #OM851049 using a 2 min. p-active pregrowth purge phase.

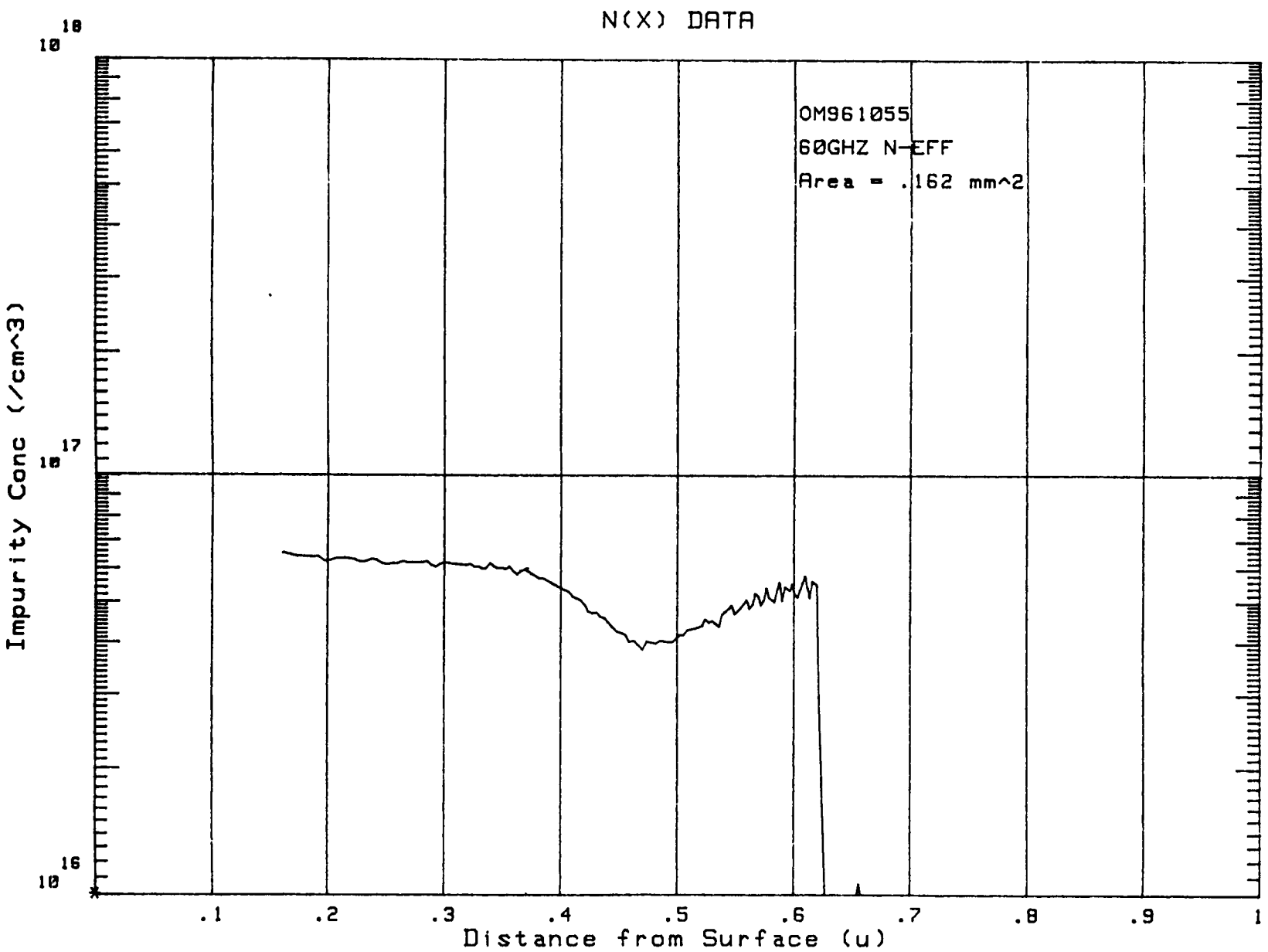


Figure 3.35: Composit profile of run #OM951055 using a 10 min. p-active pregrowth purge phase.

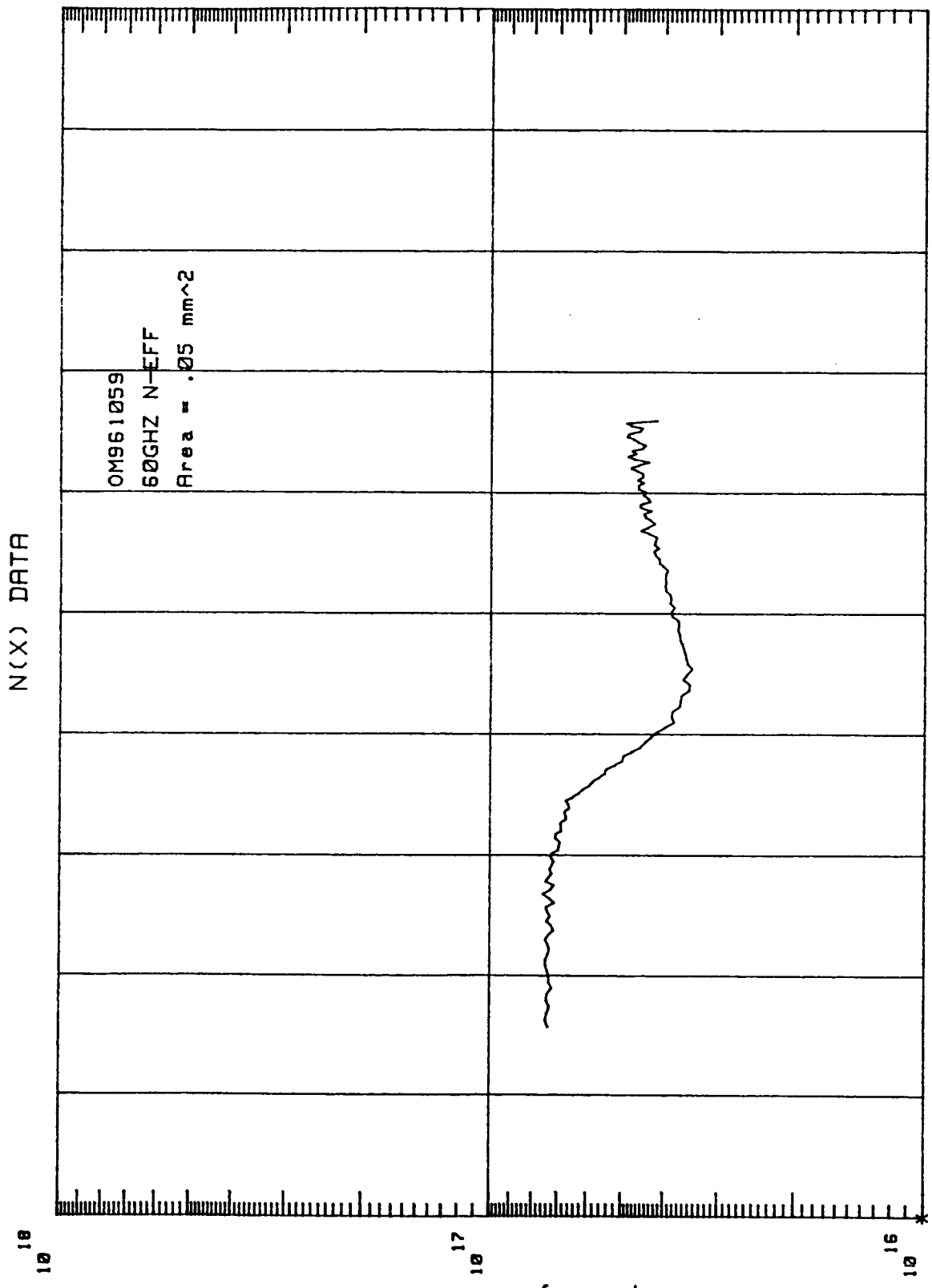


Figure 3.36: Composit profile of run #OM951059 using a 20 min. p-active pregrowth purge phase.

a. The thorough characterization of the growth parameters for submicron epitaxial layers of high electrical quality.
b. The development of a highly reproducible n-type doping technology using silicon from a silane precursor.
c. Demonstration of extremely sharp doping transition for both n and p-type layers.
d. The development of a highly predictable p-type doping technology using dimethylzinc as a zinc precursor.
e. The demonstrated capability to produce 60 GHz double drift IMPATT structures.
f. Extensive modification, improvement and relocation of the OMCVD system in order to optimize it's ability as well as provide an environment conducive to growing milimeter wave epitaxial material.

SECTION 4
WAFER PROCESSING

4.0 INTRODUCTION

Initially, wafers were processed utilizing existing X-Band plated heat sink (PHS) processing techniques developed at M/A-COM. Utilizing this baseline technology, the gold heat sink was 2 to 2.5 mils thick and the GaAs mesas were 25 to 30μm thick (see Figure 4.1). As the program progressed, it became apparent that the both the thermal resistance and the series resistance of the device needed to be reduced. To reduce thermal resistance and improve device performance, the gold plated heat sink thickness was reduced from 50 - 65μm to 2 - 5μm. The GaAs mesa height was reduced from 25 - 30μm to 10 - 15μm.

Processing steps were developed during the program to achieve these device parameters. The process steps for both the baseline PHS process and the modified process are described in detail below.

4.1 Device Fabrication - Plated Heat Sink

To fabricate plated heat sink (PHS) IMPATT diodes for this program, standard wafer processing techniques were employed. These steps include ohmic metallization to the epitaxial surface, gold plating to that metallized surface, wafer thinning, a second ohmic metallization to the N^+ substrate, and mesa definition by etching from the substrate side of the wafer. Processing steps are listed in Table 4.1 and shown in Figures 4.3a through 4.3g.

Once the epitaxial layers of the wafer were determined to be within specification, the surface was inspected for pits, stains and scratches prior to metallization. Surface defects were noted on the traveller which accompanied the wafer through processing (see Figure 4.2). All processing parameters (epitaxial metallization, gold thickness, GaAs thickness, photolithography sizes, mesa diameter and final device capacitance were specified on the traveller.

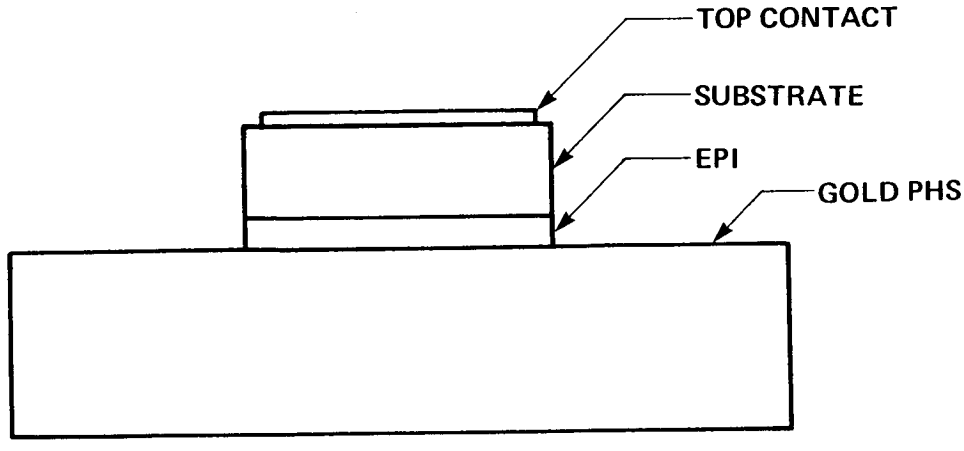


FIGURE 4.1: CROSS SECTION OF 60 GHz GaAs PHS IMPATT DIODE.

Table 4.1

PHS IMPATT PROCESSING STEPS

1. Wafer Inspection and Documentation
2. Epi Metallization (Au/Zn)
3. Protective Gold Plating
4. 435°C Metal Alloying
5. GaAs Flat Lap
6. Gold Heatsink Plating
7. Edge Trimming
8. Gold Lap
9. GaAs Substrate Lap
10. Substrate Polish Etch
11. Grid Photo
12. Grid Etch
13. Back Contact Metallization (Au/Ge/Ni/Au)
14. Sputtering
15. Back Contact Plating
16. 400°C Back Contact Alloying
17. Back Contact Plating
18. Contact Photo
19. Contact Etch
20. Mesa Etch
21. Evaluation
22. Cutback Photo
23. Etch Contact Overhang
24. Documention and Delivery to Assembly

PLATED HEATSINK TRAVELLER

DATE: __/__/__

CUSTOMER: _____

P+ _____

Wafer Thickness _____

RUN No. _____

PORTION _____

PART No. _____

N Active _____

Wafer Size _____

PROCESS No.	PROCESS STEP	DESIRED	MEASURED	DATE	OPERATOR	COMMENTS
	Top Metal					
	Plate Epi	10 min				
	Sinter	400° 8min				
	Flat Lap	9.0mils				
	Plate Heatsink	14 hrs				
	Trim Euges	YES				
	Gold Lap	___mils				
	Thin Lap	___mils				
	Polish Etch	Epi Thick				
	Grid Photo					
	Grid Etch	YES				
	Pad Height/Vb					
	Back Metal	Au Ge Au				
	Sputter	3000A Au				
	Plate Back	15min				
	Sinter	400° 8min				
	Plate Back	30min				
	Contact Photo					
	Contact Etch	YES				
	Mesa Photo					
	Mesa Etch	YES				
	Mesa Size	_____				
	Cap/Vb					
	Delivered	YES				
	Cut Back	YES				
	Inspect	YES				
	Delivered	YES				

FIGURE 4.2 PLATED HEAT SINK TRAVELLER.

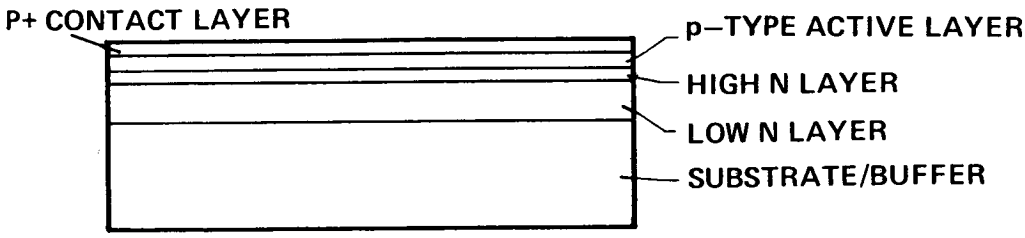
The wafer was thoroughly cleaned prior to loading into an electron-beam evaporator for metallization on the epitaxial side. 750Å of gold and 50Å of zinc were co-evaporated to form a P-type ohmic contact. This metallization was protected by 2μm of gold which was electrolytically plated to the wafer. The ohmic metallization was alloyed at 435°C in a reducing atmosphere of pure hydrogen (see Figure 4.3a).

The wafer was then thinned on the substrate side to a total thickness of 10.0 +/- 0.1 mils (see Figure 4.3b). This thickness was recorded and served as a reference for future wafer thinning operations. 5.5μm aluminum oxide grit suspended in oil was used to lap the GaAs. The actual wafer thickness at this point was not critical, however, the flatness was required to be +/- 0.1 mils across the wafer. This assured uniform thicknesses across the wafer for both the gold plated heat sink and the GaAs mesas.

Once the wafer thickness was recorded, the gold heat sink was plated to the epitaxial side. The current density in the electrolytic plating bath was kept low (~ $1mA/cm^2$) initially to assure a dense gold near the epitaxial layers. This maximized the thermal conductivity of the gold heat sink. The current density was slowly increased to a maximum of $2.5mA/cm^2$. The gold build-up along the edges of the wafer were trimmed to facilitate subsequent lapping steps.

The gold heat sink was then lapped to a uniform thickness using 9.5μm aluminum oxide grit suspended in oil. Using the previous flat lap thickness as a reference, the gold thickness was determined and recorded on the process sheet. The wafer was flipped over and the GaAs was lapped with 5.5μm aluminum oxide grit to a thickness of 1.7 to 1.9 mils. The wafer was then cleaned and chemically etched in 3:1:1 (Sulfuric Acid, Hydrogen Peroxide, DI water) to a GaAs thickness of 25 to 30μm. This process removes the GaAs substrate damaged during lapping and produces a clean, polished GaAs substrate for the subsequent N^+ ohmic metallization (see Figure 4.3c).

STEP 1. EPITAXIAL WAFER.



STEP 2. OHMIC P–TYPE METALLIZATION AND PLATING.

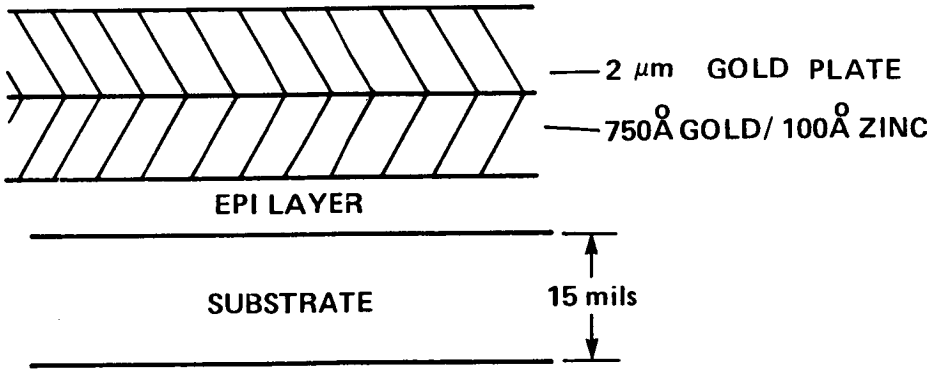


FIGURE 4.3(a): STEPS IN THE PLATED HEAT SINK PROCESS

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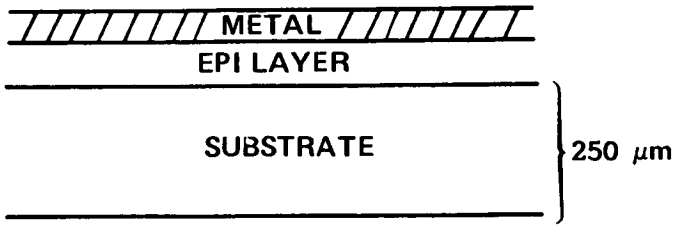
STEP 3. SUBSTRATE FLAT LAP.



STEP 4. GOLD HEAT SINK PLATING.

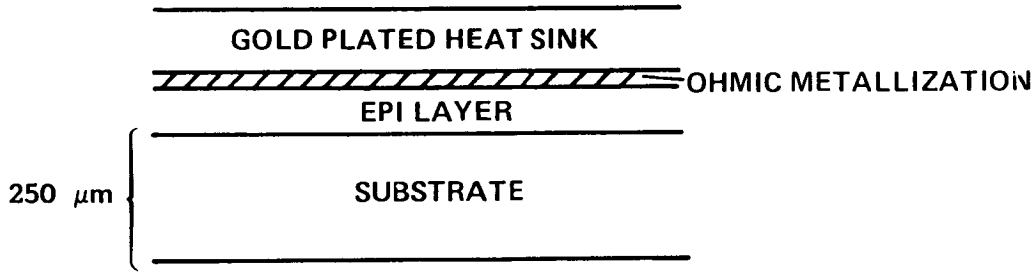


FIGURE 4.3(b): STEPS IN THE PLATED HEAT SINK PROCESS.

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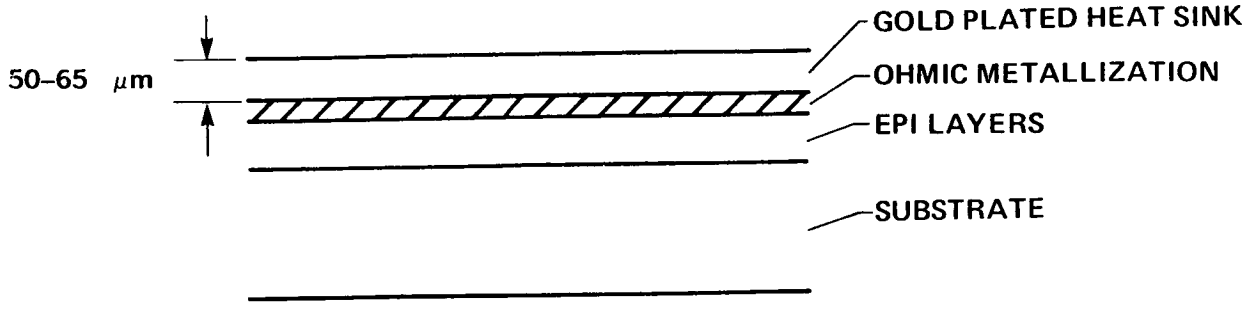
STEP 5. GOLD LAP



STEP 6. GaAs SUBSTRATE LAP & POLISH ETCH

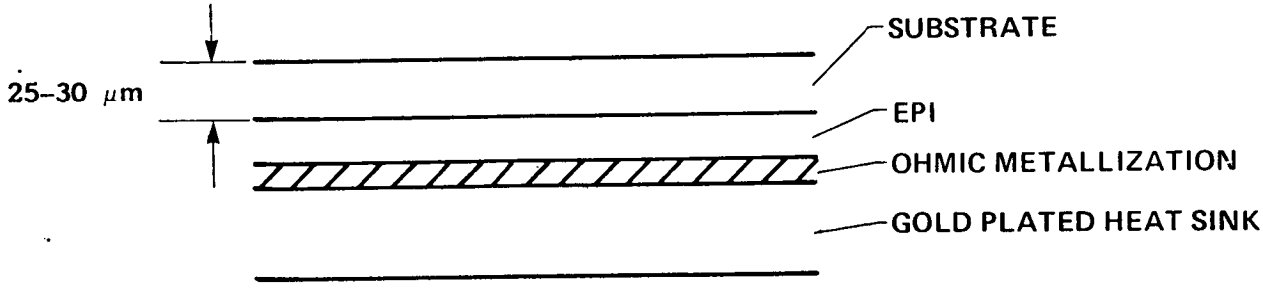


FIGURE 4.3(c): STEPS IN THE PLATED HEAT SINK PROCESS.

The substrate side of the wafer was then patterned with 11 mil squares on 12 mil centers. This pattern was used to etch a grid through the GaAs to the gold heat sink, allowing the N-type ohmic to be sintered without stressing the GaAs. The GaAs mesa height can also be measured at this point and chemically etched if necessary. The reverse voltage breakdown of the device can also be measured at this point. The GaAs mesa height and voltage breakdown were recorded on the process sheet at this step (see Figure 4.3d).

To deposit an ohmic contact to the N-type GaAs substrate, the wafer was given a thorough solvent cleaning and loaded into an electron-beam metal evaporator. To achieve an 88% gold/12% germanium eutectic by weight, 1000Å of gold and 300Å of germanium were deposited simultaneously on the wafer. 150Å of nickel and 2000Å of gold were deposited individually after the initial Au/Ge deposition.

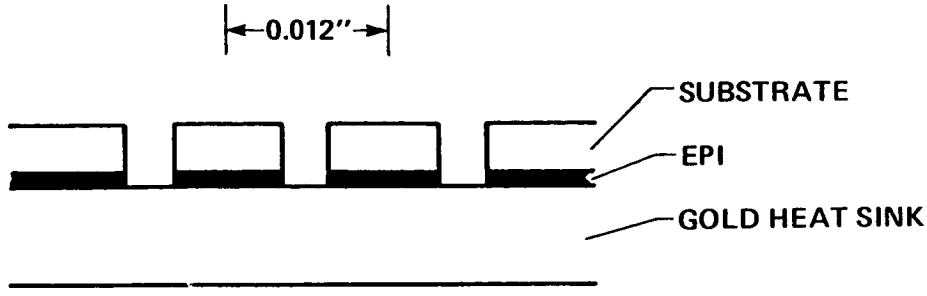
E-beam metallizations typically do not provide the sidewall coverage necessary for plating gold to the substrate side of the wafer. To assure electrical continuity across the slice, the wafer was sputtered with 3000Å of gold (see Figure 4.3e). 2μm of gold was then electrolytically plated to the wafer. The wafer was placed in a 400°C furnace under pure hydrogen for 8 minutes to alloy the N-type ohmic contact.

The wafer was then plated with another 2μm of gold to provide a soft gold for ribbon bonding to the device at assembly.

To define a circular mesa, a circle of photo resist was patterned on the top of the square GaAs mesa. The photo was 6 mils in diameter. This was used as a mask to etch the gold. The GaAs was then etched in 3:1:1 using both the gold and the photo resist as a mask. The final mesa diameter was 2 to 3 mils (see Figure 4.3f).

To remove the overhanging gold from the top contact, a circle of photo resist was patterned over the gold contact. The diameter of this circle was equal to the diameter of the GaAs mesa. This mask was used to etch the gold contact to a diameter slightly smaller than

STEP 7. STRESS-RELIEF GRID ETCH



STEP 8. Au/Ge/Ni/Au METALLIZATION

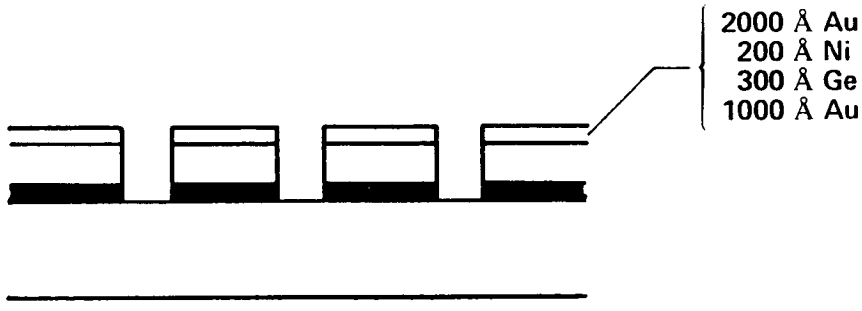
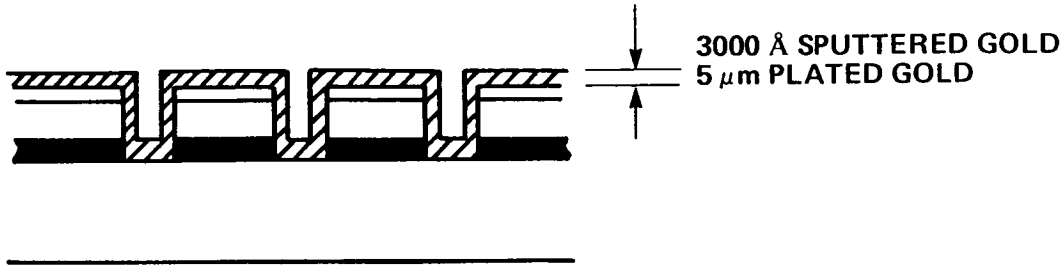


FIGURE 4.3(d): STEPS IN THE PLATED HEAT SINK PROCESS.

STEP 9. SPUTTER/PLATE GOLD



STEP 10. CONTACT PHOTO

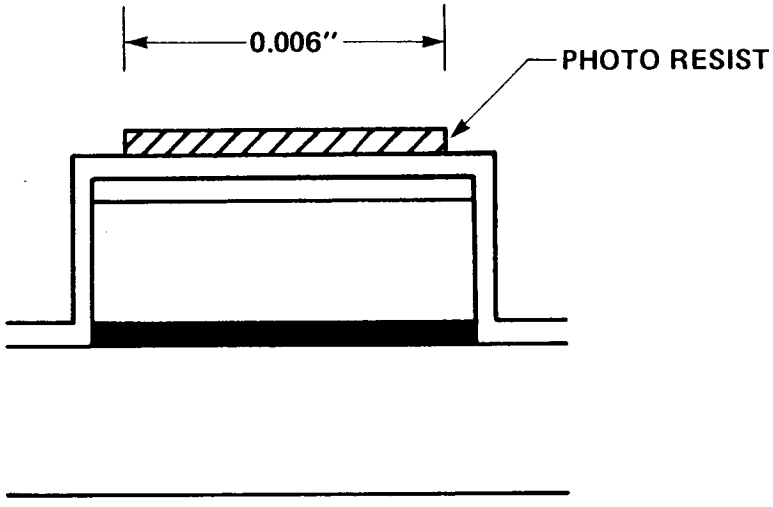


FIGURE 4.3(e): STEPS IN THE PLATED HEAT SINK PROCESS.

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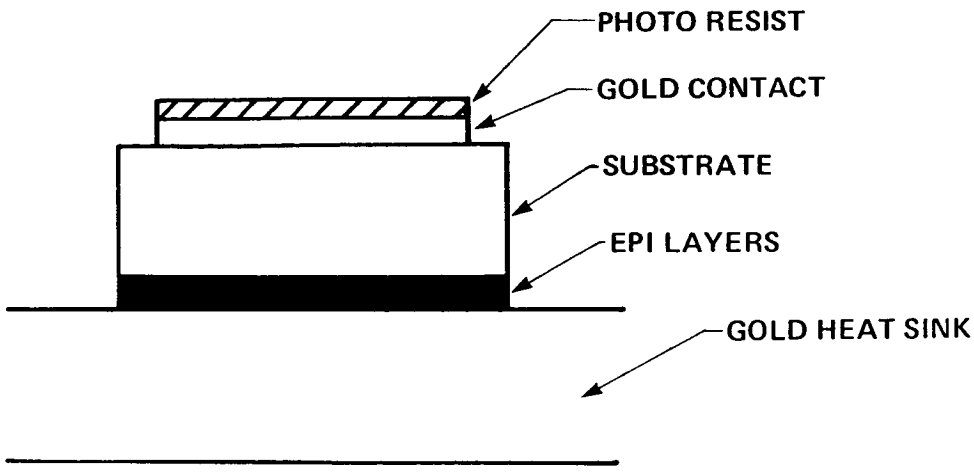
STEP 11. GOLD ETCH



STEP 12. MESA ETCH

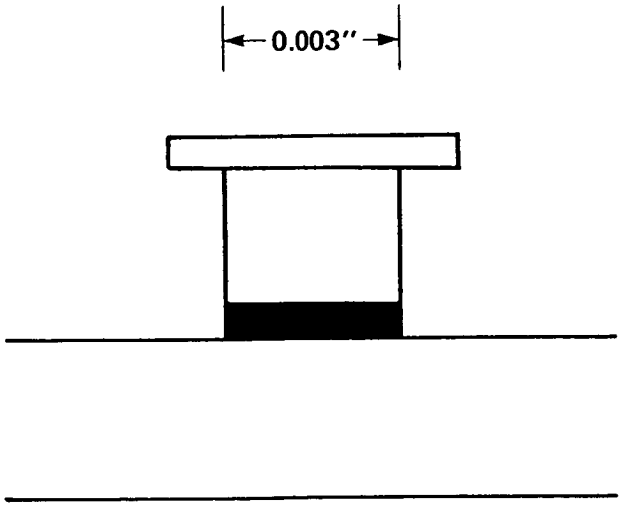


FIGURE 4.3(f): STEPS IN THE PLATED HEAT SINK PROCESS.

the GaAs mesa diameter. The photo resist was then removed (see Figure 4.3g), the wafer was cleaned and prepared for delivery to the assembly lab.

The voltage breakdown and zero bias capacitance were recorded on the process sheet and then wafer was delivered to the assembly area.

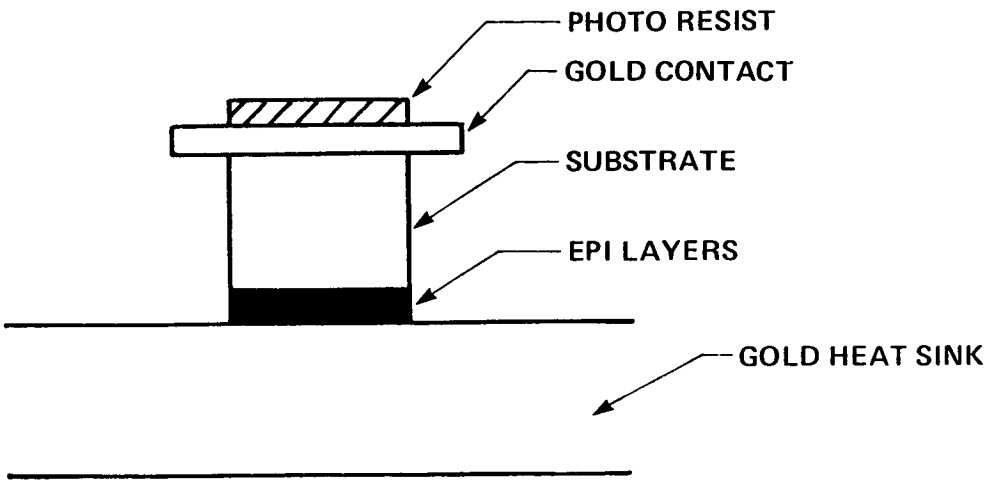
4.2 Process Modifications

The process described above yielded plated heat sink (PHS) devices with 2 mil gold heat sinks. To evaluate the advantages of diamond heat sinks, the device fabrication process was modified. Diodes were fabricated with only 2 to 5μm of gold on the epitaxial side and 10 to 15μm of GaAs. The reduced gold thickness allowed the diode to be thermocompression bonded directly to the metallized diamond heat sink. The reduced mesa height decreased the series resistance by thinning the amount of N^+ GaAs substrate. Processing steps are described below.

The wafer was cleaned and metallized with Au/Zn as described earlier. Once the P-type ohmic contact was sintered at 435°C, a gold heat sink of 2 to 5μm was plated to the epitaxial side of the wafer. The first and only lapping step was then done. The wafer was lapped to a total thickness of 1.4 to 1.6 mils. A small hole was then etched into the GaAs substrate using wax as a mask. This hole was deeper than the final GaAs thickness (10-15μm). The wax was removed and the GaAs was etched in 3:1:1. As the GaAs was etched, the hole etched down to the gold and the depth of the hole was used as an indicator of the GaAs thickness.

Once the GaAs was thinned to 10 to 15μm, the N+ sustrate was metallized with Au/Ge/Ni/Au and plated with 2μm of gold. The wafer was then patterned with photo resist. The gold was etched, exposing the GaAs substrate. The GaAs was then etched to 3 mils mesa diameter. The gold overhang was etched and at the same time the gold heat sink was etched, thus separating the devices into discrete chips. The chips were then cleaned, sintered and sent to assembly. An example of the 60 GHz IMPATT chip fabricated with the above steps is shown in Figure 4.4.

STEP 13. CUTBACK PHOTO



STEP 14. ETCH GOLD OVERHANG

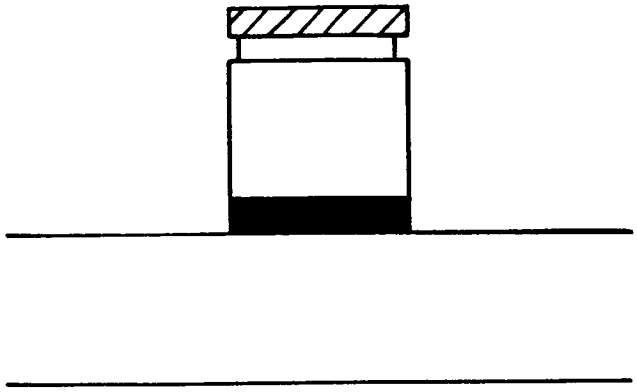


FIGURE 4.3(g): STEPS IN THE PLATED HEAT SINK PROCESS.

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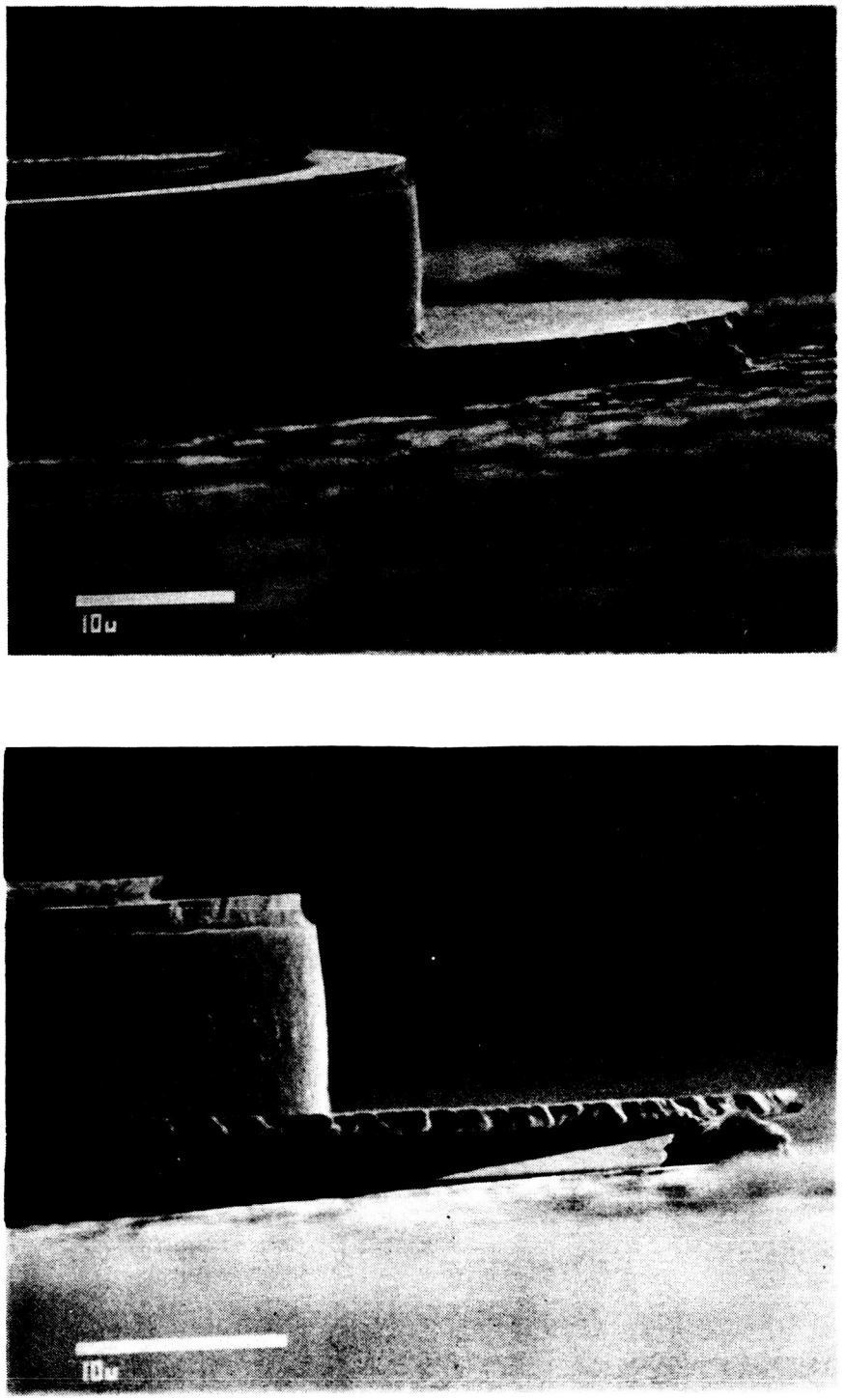

FIGURE 4.4: 60 GHz IMPATT CHIP WITH THIN PHS AND REDUCED GaAs MESA HEIGHT.

SECTION 5
DIODE ASSEMBLY

5.0 INTRODUCTION

As indicated in Section 4, epitaxial wafers were initially processed into single mesa devices having 50-65 microns thick gold plated heat sinks (PHS). Before they could be assembled for RF testing, the processed wafers were diced by cutting through the PHS. Each device was then bonded onto an ODS-138 package using a gold-tin solder preform. With this approach in wafer processing and device assembly, it was quickly determined that the diodes' thermal resistance was unacceptably high (70-80°C/W). Consequently, the RF output power from these devices was low (<200mW).

To reduce the thermal resistance of our 60 GHz IMPATTs, steps were taken to minimize the thickness of the intermediate metal between the junction (hottest region) of the device and its copper heat sink (package). Some of these steps included, (i) the processing of single mesa devices having 2-5 microns instead of 50-65 microns of gold PHS, and (ii) the elimination of gold-tin solder preforms. Without the preforms, devices were thermo-compression bonded (TCB) onto threaded ODS-138 copper packages. As a result of these steps, the thermal resistance was reduced to 50-60°C/W. Unfortunately, this resistance was still high and imposed a thermal limitation on devices operating beyond a current level of 190mA and an output power of 385mW.

5.1 Diamond Heat Sink Package

The constraint imposed by the thermal limitation problem was alleviated by using diamond heat sink packages. These packages were fabricated from our standard ODS-138 design, as shown in Figure 5.1. Basically, the design consists of a gold coated, threaded copper base and a ceramic spacer. The threaded base was 116 mils in diameter and 20 mils

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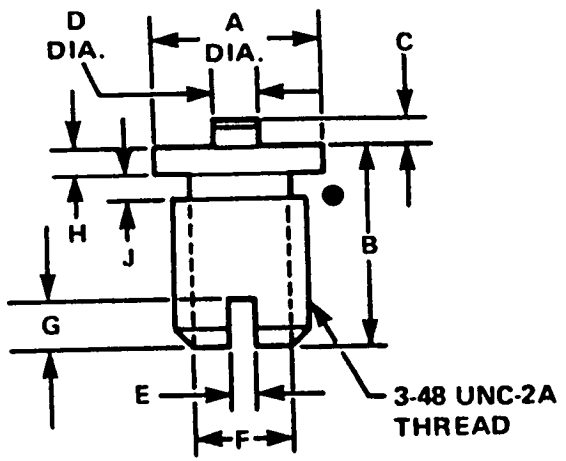

DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.113	0.118	2,87	3,00
B	0.140	0.145	3,56	3,68
C	0.016	0.019	0,41	0,48
D	0.027	0.034	0,69	0,86
E	0.015	0.025	0,38	0,64
F	0.068	0.070	1,73	1,78
G	0.025	0.045	0,64	1,14
H	0.018	0.022	0,46	0,56
J	0.015	0.025	0,38	0,64

C_P = 0.18 pF Typical
L_S = 0.10 nH Typical

Figure 5.1: Schematic of the ODS-138 Package.

thick. The spacer, metallized on its top and bottom surfaces, was bonded to the copper base. The dimensions of the spacer are: OD = 32 mils; ID = 16 mils; height = 8 mils.

The first set of diamond packages used in this program were manufactured with the co-operation of Drukker Ind. of Holland. Copper bases provided to them were embedded with metallized Type IIa diamonds that were cylindrical in shape (10 mils diameter and 4 mils high). As shown in the cross-sections of Figure 5.2, no voids are observed, indicating very good metallization/embedding techniques.

Devices assembled on "Drukker's diamond packages" were able to accommodate 300mA of operating current (versus 190mA for copper packages). However, no RF output power was observed. Examination of these packages after RF testing revealed that the base thickness ranged from 9-11 mils instead of the original 20 mils. It is speculated that this discrepancy was caused by the diamond embedding process. Apparently each diamond was embedded to a depth of 9-11 mils into the base provided to Drukker. To minimize topographical voids between the diamond and copper base interface, the base was lapped to a thickness of 9-11 mils and then metallized. Having a 9-11 mil thick base, rather than the accustomed 20 mils, the diodes did not oscillate as a result of diode-circuit impedance mismatch.

Because of the discrepancy cited above, work began at M/A-COM to develop diamond packages. Without attempting the embedding process, metallized Type IIa diamonds were TCB onto ODS-138 packages (see Figure 5.3). Devices assembled on these packages yielded better RF test results than those on "Drukker packages" and their counterparts on copper heat sinks. While the results were encouraging, they were below our expectation. The reason for this was speculated to be caused by a poor bonding interface between the diamond and copper base, and/or an impedance mismatch as a result of the diodes' position in the cavity (the diodes were assembled on a 4 mil high diamond).

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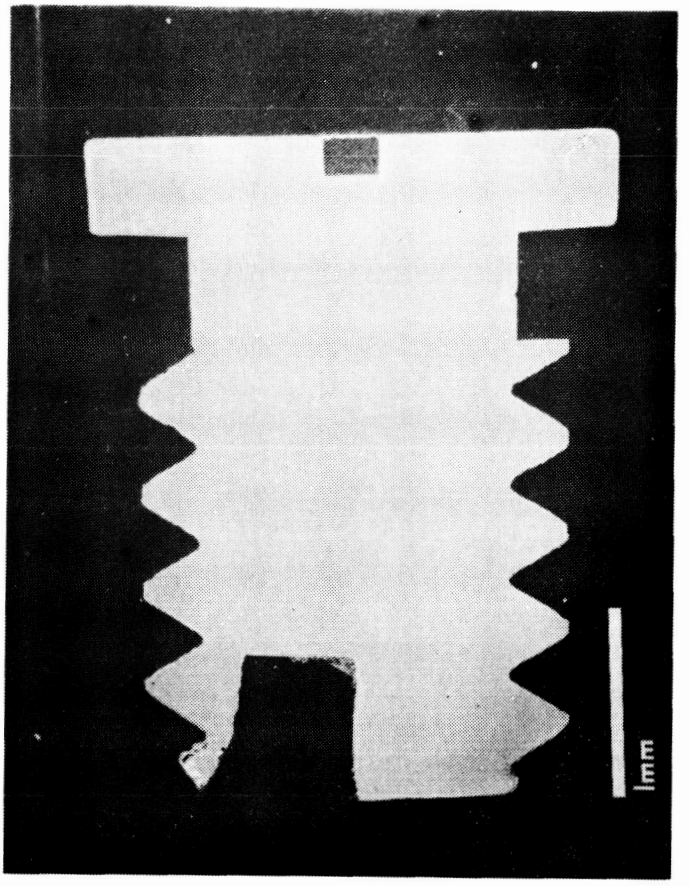
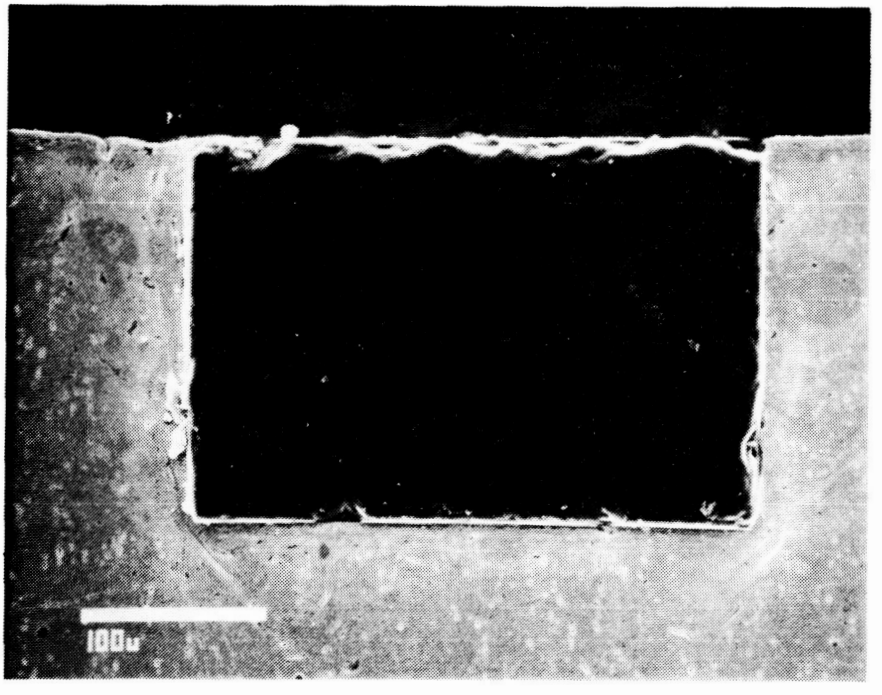


(a) 26X MAG.



(b) 250X MAG.

FIGURE 5.2(a) CROSS-SECTIONAL VIEW OF IIa DIAMOND EMBEDDED (AT DRUKKER) INTO ODS-138 PACKAGE.

(b) CLOSE-UP CROSS-SECTIONAL VIEW OF METALLIZED DIAMOND.

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FIGURE 5.3 A METALLIZED TYPE IIa DIAMOND (WITH IMPATT CHIP) THERMOCOMPRESSION BONDED ONTO AN ODS–138 PACKAGE.

Following the efforts described above, work began on the embedding process. Cylindrical Type IIa diamonds were hand-pressed into ODS-138 bases. While the diamonds were pressed flush to the top of the bases and no lapping was involved, the end product (see Figure 5.4(a)) compares well with that produced by Drukker (see Figure 5.4(b)). Devices assembled onto our embedded diamonds were able to operate at a much higher current level and, hence, produced higher output power than those assembled on TCB diamond packages (see Section 6 for RF results). An example of the cross-sectional view of a 60 GHz, diamond heat sink IMPATT is given in Figure 5.5. Again, the diamond/copper interface shown in Figure 5.5 is free of voids and is similar to that of Figure 5.2.

5.2 Ceramic Spacers

After addressing the thermal problems associated with 60 GHz HDD IMPATTs, work began on other aspects of the package design that would influence the impedance matching between the device and its circuit. Specifically, efforts were focused on minimizing the parasitic contributions from the ceramic spacer that surrounds the device. As mentioned earlier, the spacer of the ODS-138 package has an OD of 32 mils, ID of 16 mils, and height of 8 mils. To reduce the parasitic capacitance and inductance associated with ODS-138, its spacer was replaced with a smaller one having an OD = 16 mils, ID = 8 mils, and height = 4 mils.

As purchased, the smaller ceramic spacers were metallized with tungsten on the top and bottom surfaces. To facilitate bonding to the threaded copper bases, the spacers were further metallized with gold via electroplating. Like the larger spacers, the smaller ones were TCB onto the copper bases containing embedded diamonds (see Figure 5.6). Subsequently, an IMPATT chips was TCB and cross-strapped within each spacer as shown in Figure 5.7.

Before the devices could be evaluated for their DC and RF characteristics, lids were solder bonded onto the spacers to seal the

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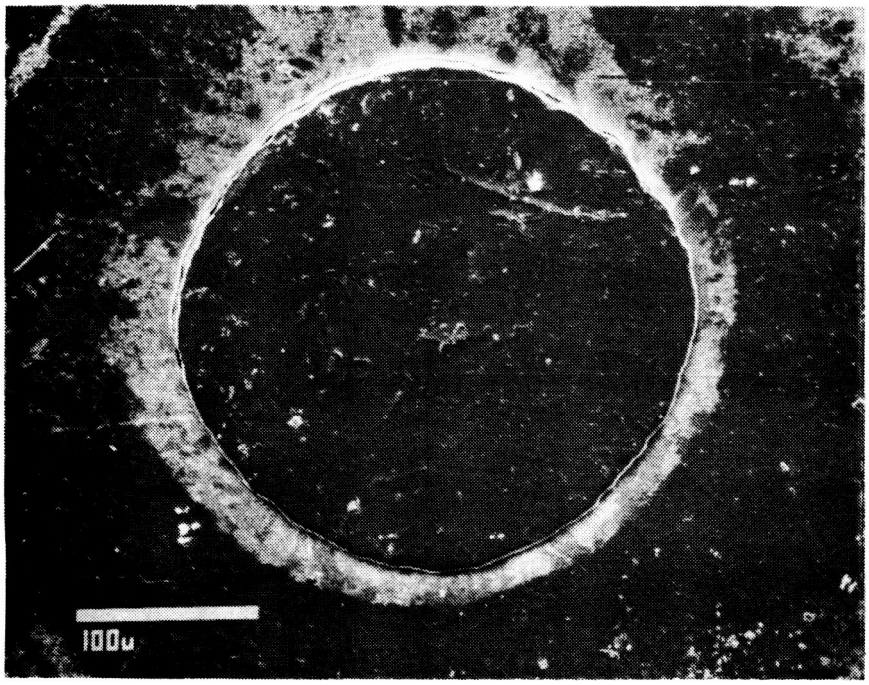

FIGURE 5.4(a)

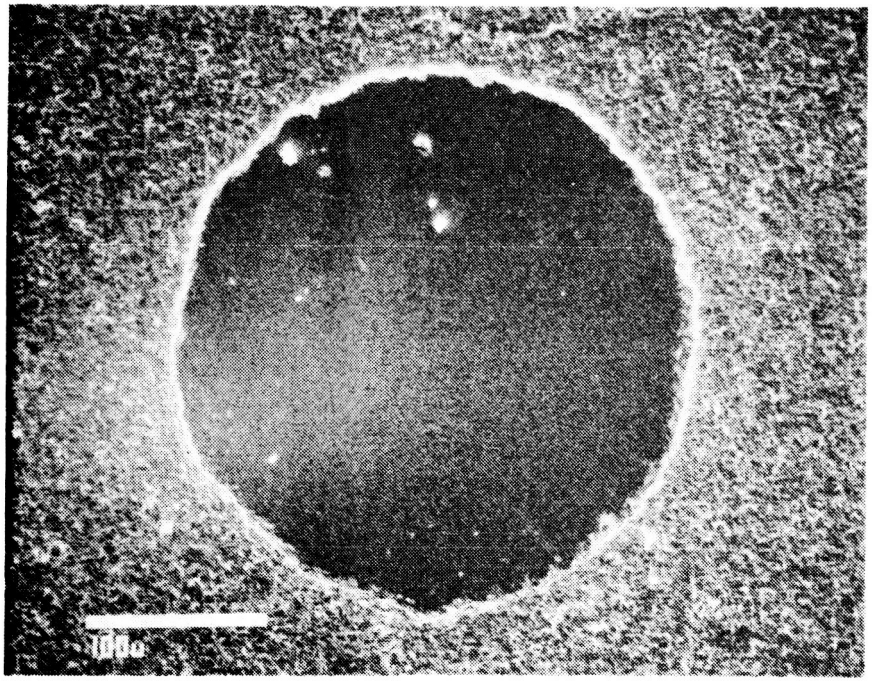

FIGURE 5.4(b)

FIGURE 5.4 TOP VIEW OF METALLIZED DIAMOND EMBEDDED (INTO COPPER BASE OF ODS–138 PACKAGE) AT a) M/A-COM AND b) DRUKKER.

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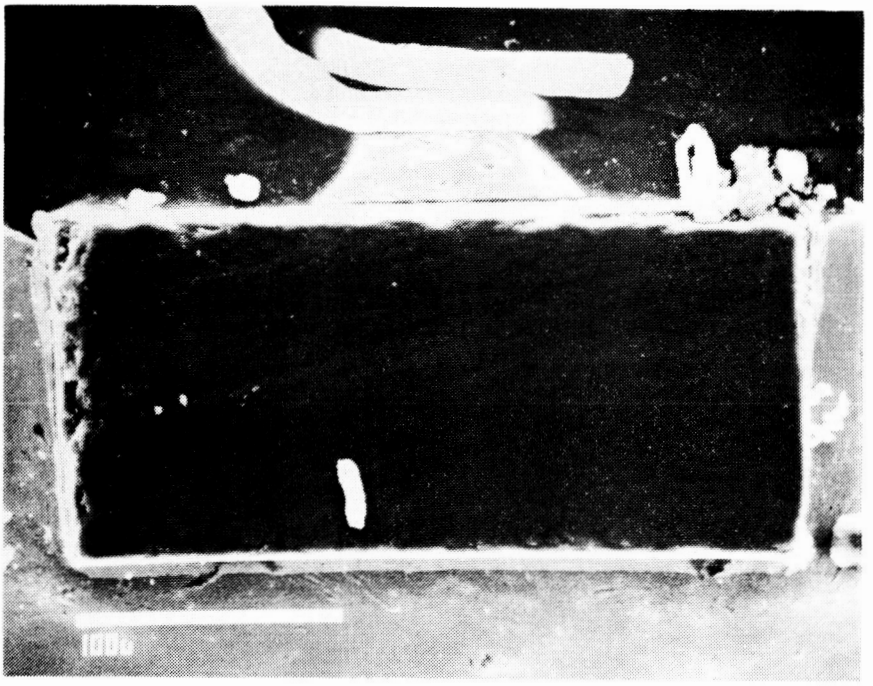

FIGURE 5.5 CROSS-SECTIONAL VIEW OF IMPATT DIODE BONDED ONTO AN EMBEDDED DIAMOND.

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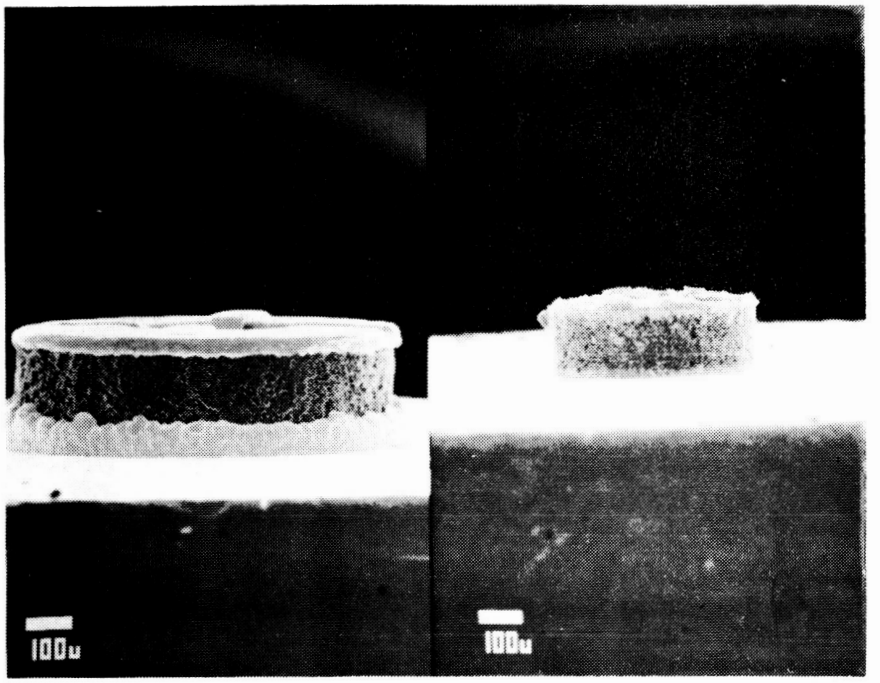

FIGURE 5.6 SIDE VIEW OF SMALL CERAMIC SPACER (RIGHT) COMPARED WITH THAT USED ON ODS–138 PACKAGE (LEFT).

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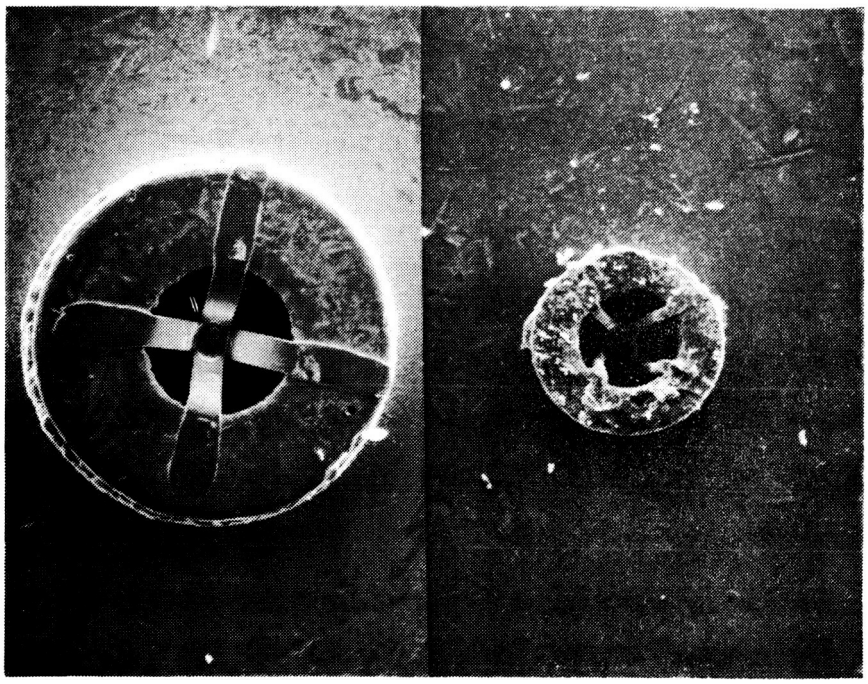

FIGURE 5.7 TOP VIEW OF CERAMIC SPACERS WITH CROSS-STRAPPED 60 GHz IMPATTS. SAME MAGNIFICATION FOR BOTH SPACERS.

devices. While the lids for the large spacers were readily available, those for the small spacers were fabricated by electroplating gold through an array of circular openings (defined by photolithography) onto a layer of titanium. An example of the lid used on the small ceramic spacer is shown on the right of Figure 5.8. For comparative purposes, the conventional ODS-138 package is given on the left of the same figure.

5.3 Ribbon Bonding

Following die bonding, the diodes were prepared for visual inspection. Because of their very small dimensions, the 60 GHz HDD IMPATTs were carefully inspected for several quality criteria which included micro-cracks, metallization voids, and mesa geometry. Electrical connections to each die was provided by thermo-compression bonding gold ribbons to its ohmic contact pad. Devices in the large ceramic spacers were bonded with 1/2 X 3 mil gold ribbons. Because of space limitations the devices in the small ceramics utilized 1 mil diameter gold wires.

To effect the parasitic inductance associated with the larger spacer package, various gold ribbon configurations were used, namely: single, double (crossed), and triple. Based on these experiments, optimum RF performance (see Section 6) was obtained from devices that utilized a cross-ribbon configuration. Consequently, 60 GHz IMPATTs were bonded with two 0.0005" X 0.003" gold ribbons, as shown previously in Figure 5.7 (left).

5.4 Device-In-Package Etch

The final junction area of the device is an important parameter in determining its efficiency and frequency of operation. The optimum junction area for a given wafer lot was determined experimentally by fabricating and testing devices with a range of zero bias capacitance values. After ribbon bonding, the devices were evaluated for their combined junction and package capacitance values as well as breakdown voltages. Depending on the range of interest, the junction areas of the

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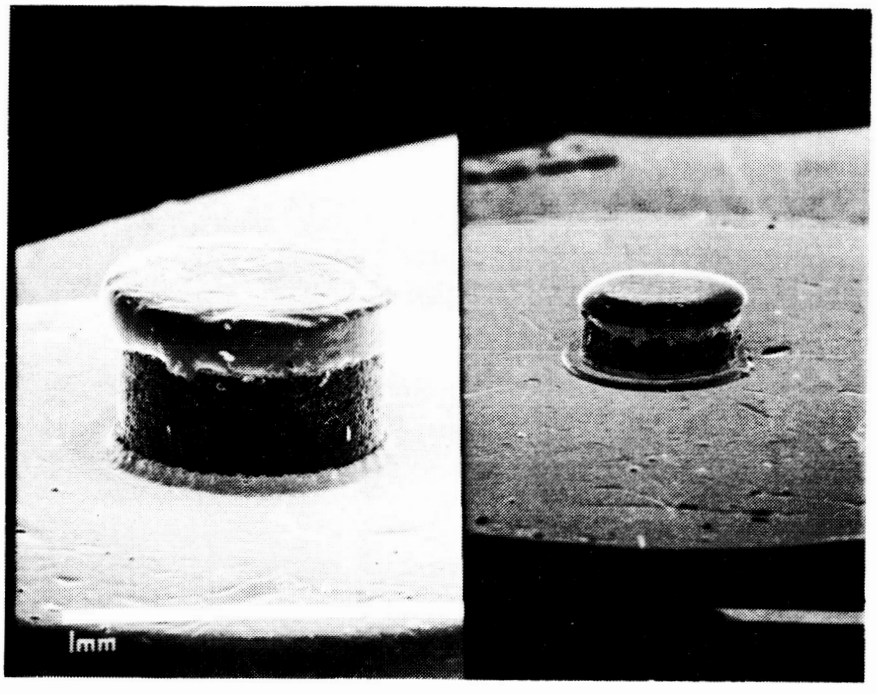

FIGURE 5.8 CONVENTIONAL ODS–138 (LEFT) COMPARED WITH SMALL CERAMIC PACKAGE (RIGHT) AT SAME MAGNIFICATION.

devices were electrolytically etched using a solution of potassium hydroxide. Subsequently, they were washed in DI Water, rinsed in isopropyl alcohol, baked in an atmosphere of forming gas for 30 minutes at 150°C, and then capped.

Based on the RF test results from various wafer lots, optimum performance was achieved when the devices exhibited a zero bias capacitance of 1.8-2.2pF. This range includes approximately 0.15pF of shunt capacitance due to the ceramic spacer used on the package.

5.5 Capping

Once the devices were etched to their desired capacitance values, they were capped using a gold-tin solder preform and a gold plated copper lid. Fixtures were available for a batch of 20 diodes and these were passed through a belt furnace with an inert gas atmosphere for 22 minutes with a peak center zone temperature of 300°C.

SECTION 6
RF CIRCUIT AND TEST RESULTS

6.0 INTRODUCTION

The RF performance of an IMPATT oscillator depends both on attaining the proper diode design and on achieving a good match between the package diode and the RF circuit (cavity). The diode and packaging efforts have already been covered and in this section the program efforts aimed at optimizing circuit design are discussed. There are two important aspects to this subject. First, the RF cavity must be capable to matching the diode impedance at the correct operating frequency; secondly, the bias circuit should be designed to suppress low frequency oscillations. Such oscillations can lead to premature RF power saturation and excessive noise. This section describes the work done in these two key areas.

6.1 60 GHz IMPATT Cavity Development

The general features that are necessary in a properly designed Test Mount for high peak power IMPATT diodes are:

(1) The circuit should provide a proper impedance match between the IMPATT diode chip and the output waveguide, so that the maximum available RF power is delivered to the load when the diode is biased to its maximum safe operating current. Therefore, the impedance transformer should be located as close to the diode as possible and the test mount should be a low-loss circuit.

(2) The circuit should have an external Q which is high enough to provide low noise.

(3) The circuit admittance locus should be a smooth, well behaved curve for frequencies close to the desired operating frequency so as to provide a stable, single frequency operating point which can be tuned smoothly and continuously.

(4) Care must always be taken to prevent subharmonic oscillations.

Two different types of RF circuits were considered: (a) Coaxial - Waveguide and (b) Top Hat. Each has its own relative merits and demerits. The coaxial-waveguide approach has been used successfully up to 94 GHz by Hughes and Raytheon. A reduced height waveguide section is used for broadband matching of the IMPATT diode. The diode is mounted in a recessed coaxial section of the waveguide (see Figure 6.1). Transformation from the 50 ohm transmission line to the diode impedance is accomplished by a fixed low impedance section of transmission line immediately adjacent to the diode.

The resonant frequency of a particular diode in the cavity is determined by the length of the transformer section L_4, and depth to the package L_3, the diameter of the spacer ring D_2 and the reactance of the diode itself. The principal effect of increasing the length of L_3 or decreasing the spacer diameter D_2 is a reduction in the inductance of the package. RF absorbent material at the top of the coaxial line is used as a termination for absorbing undesirable subharmonic oscillations. This type of mount is very expensive and also interchanging of diodes is more difficult. The range of tuning obtainable using a particular transformer is limited in a coaxial type cavity. However, a very broad range of tuning and impedance changes are attained with change of transformers.

The top hat approach was first introduced by Bell Laboratories for use in the 40-90 GHz frequency range where it appears to work successfully, although the operation of the circuit is not completely understood. It is inherently a low-loss circuit which can be easily modified and optimized. A schematic of this circuit is shown in Figure 6.2. The top hat circuit is a method of tuning and coupling an IMPATT diode in a waveguide using a circular disc mounted on top of the pill package. The zone between the disc and ground plane acts as a radial transmission line. The diode circuit performance depends on the following parameters:

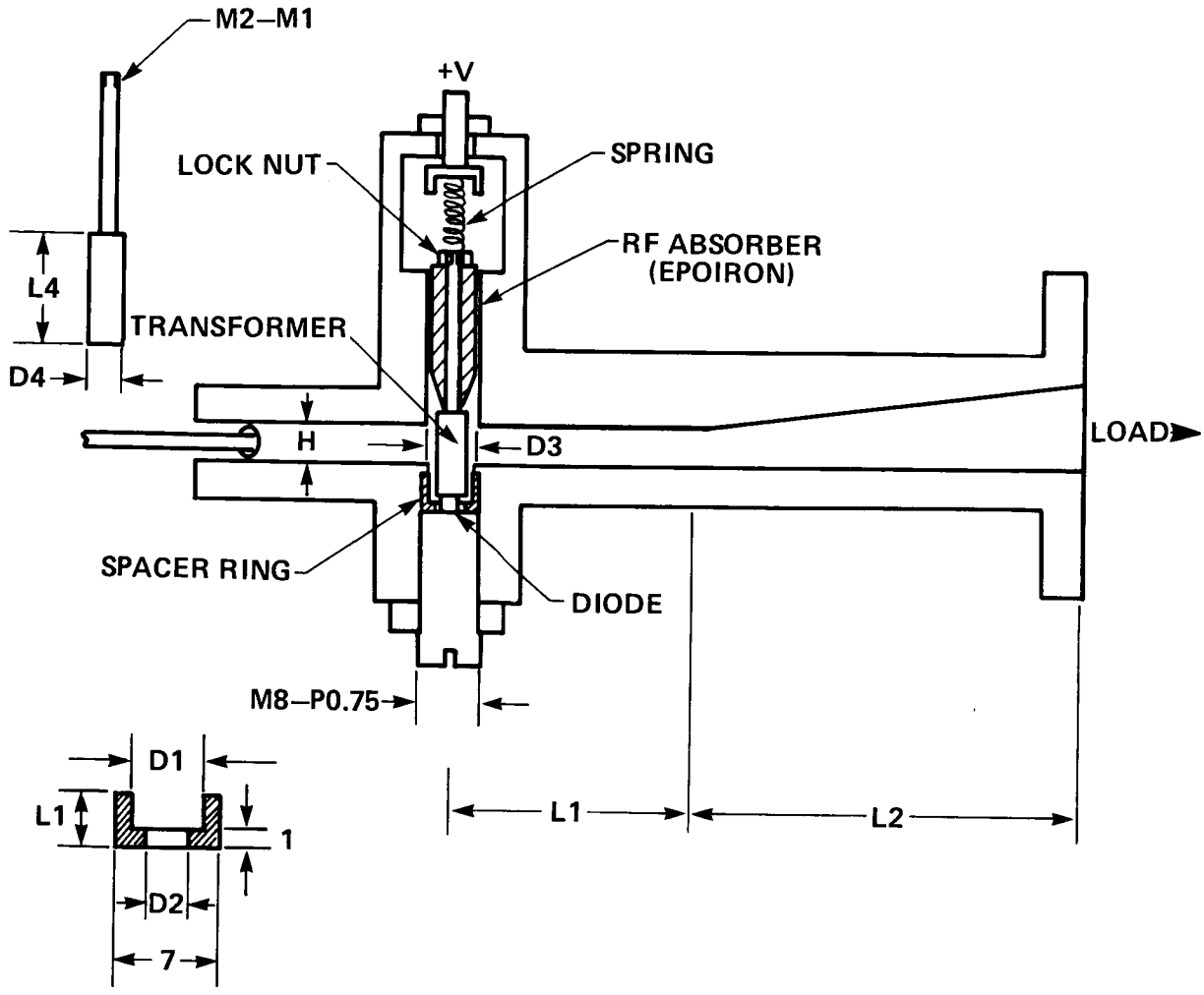

FIGURE 6.1 SCHEMATIC OF COAXIAL TEST CIRCUIT.

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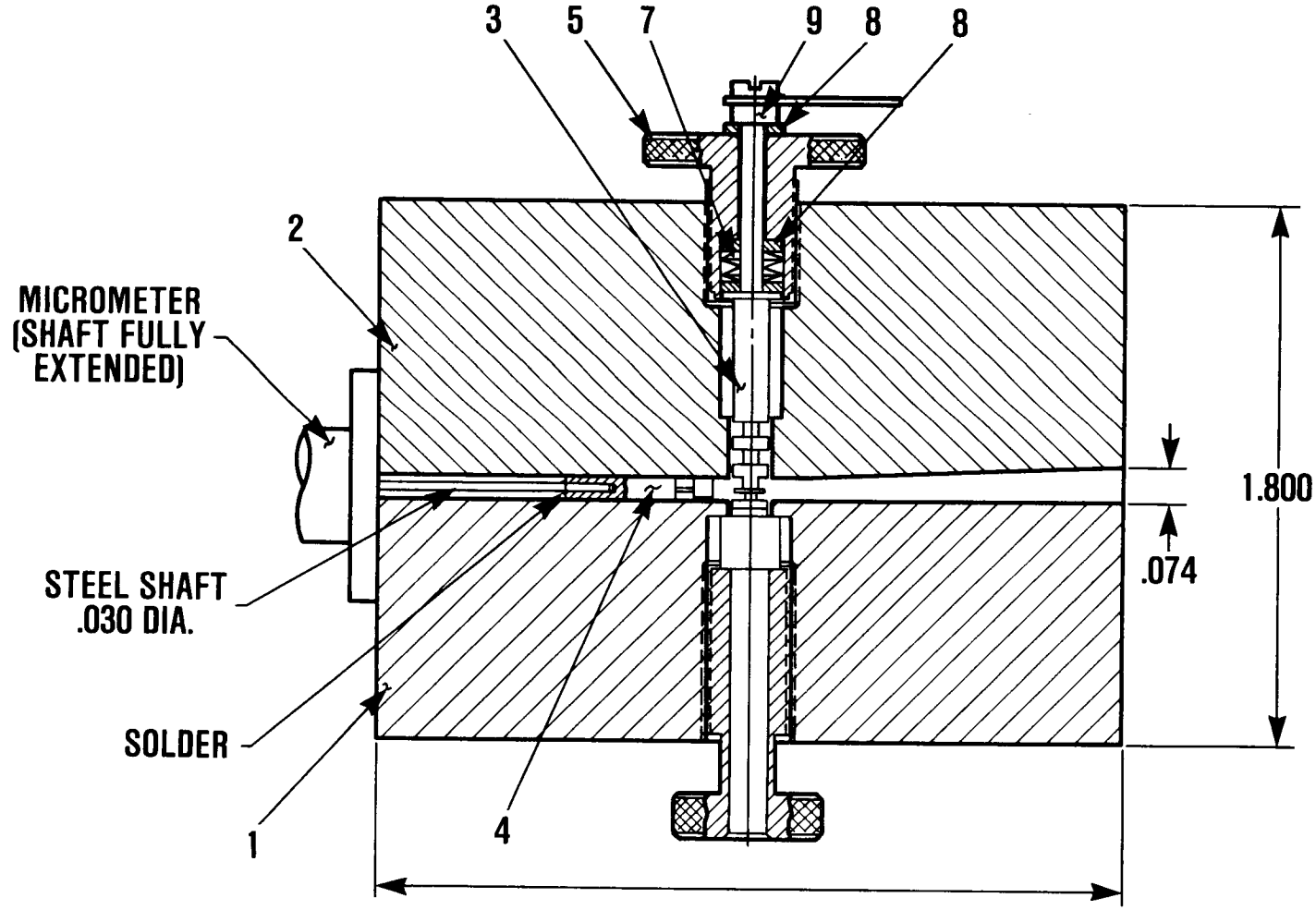

FIGURE 6.2 SCHEMATIC OF TOP HAT CAVITY.

(a) Cap diameter
(b) Cap height above the waveguide wall
(c) Cap thickness

A V-Band (50-75 GHz) test mount using the top hat approach was designed for testing IMPATT diodes at 60 GHz and is shown in Figure 6.3. A long section is included for broadband applications. First order calculations shows that a disc diameter of 0.110" to 0.115" should work for 60 GHz operation. The device impedance and the reduced height waveguide will alter these values to some extent.

This circuit was chosen over the coaxial-waveguide circuit because the top hat is a very broadband circuit. For test purposes, where the actual impedance of the device is unknown, it is faster to match the device in a top hat type circuit and obtain optimum RF power in the oscillator. For this reason, we have designed four (4) top blocks with tapered sections of 0.074", 0.065", 0.055" and 0.045" and thirty (30) top hat structures which incorporated bias filters to match IMPATT diodes with different impedance values. These choke structures are made out of 6061-T6 aluminum and have 0.0005" thick block anodize coating. RF absorbent material, such as "ecoabsorb beads", at the top of the choke structure is used as a termination for absorbing undesirable subharmonic oscillations. A tunable back short is used to improve the match between the diode and the cavity.

6.2 RF Test Results

During this reporting period, several diode lots were evaluated for their RF characteristics using the top hat cavity described above. The diode lots were initially fabricated from H-VPE and OMCVD HDD epitaxial wafers. At the mid-term period of this contract, H-VPE efforts were discontinued in order to give full attention to the OMCVD approach. Before making this transition, experimental results from available 60 GHz H-VPE wafers indicated that our conventional X-Band processing technology was not appropriate at V-Band.

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FIG. 6.3 (a) TOP HAT TEST CAVITY FOR 60GHz IMPATT DIODES

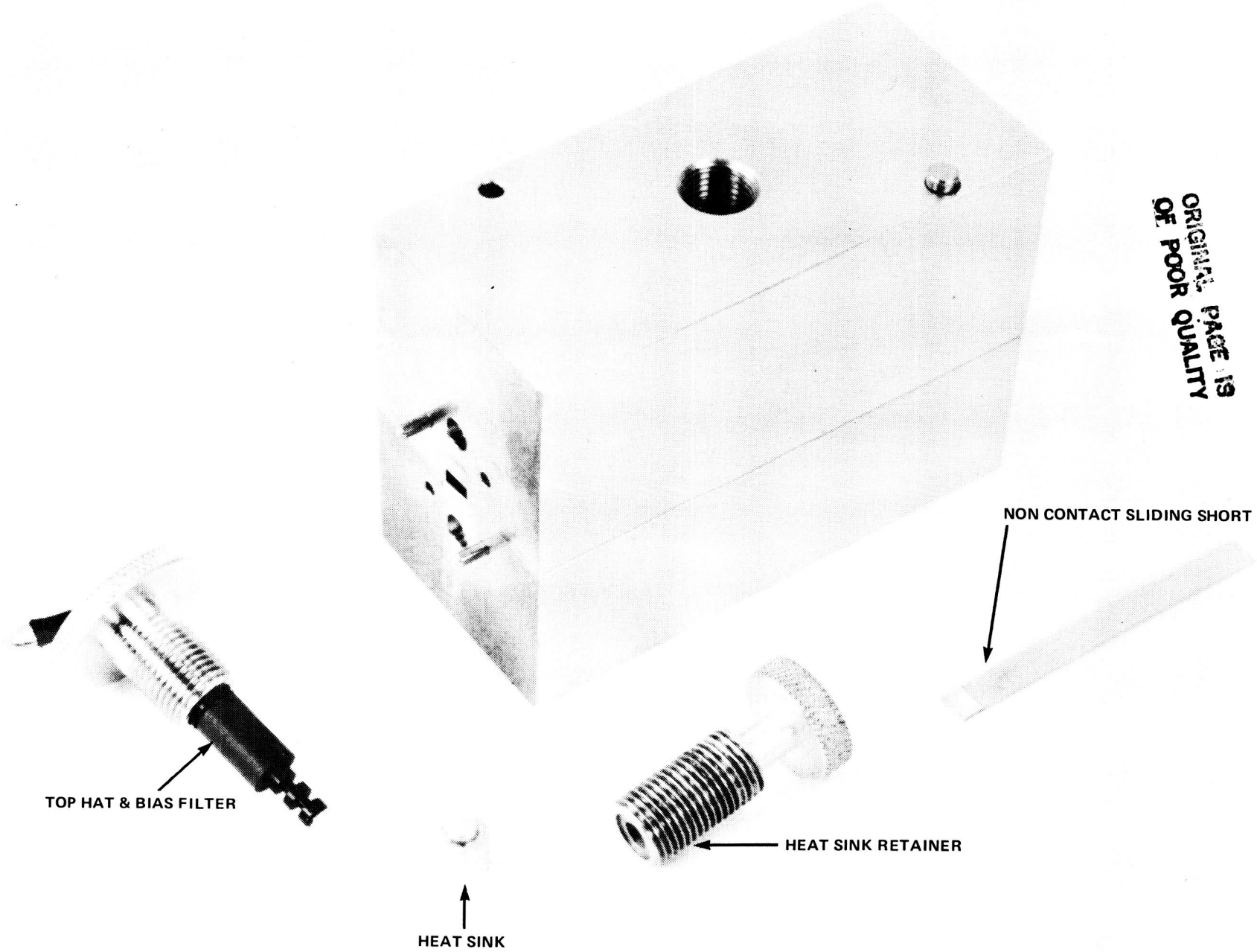

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FIGURE 6.3(b) DETAILS OF THE 60 GHz IMPATT TEST CAVITY

The processing approach that proved satisfactory at 60 GHz involved the thinning of the GaAs mesa to 10-15 microns (compared to 25-30 microns used at X-Band). With this modification, we were able to increase the efficiency of our 60 GHz IMPATTs by a factor of 2. As an example, the following results were obtained from H-VPE wafer #I10292 that was processed the conventional way:

Operating voltage, V_{op}	= 22.7 volts
Operating current, I_{op}	= 179mA
Oscillation frequency	= 56.4 GHz
Output power	= 200mW
Conversion efficiency	= 4.9%

When another portion of the same wafer was re-processed with a GaAs mesa height of 10-15 microns, the following results were obtained:

Operating voltage	= 20.9 volts
Operating current	= 150mA
Oscillation frequency	= 53.8 GHz
Output power	= 300mW
Conversion efficiency	= 9.6%

For the two cases given above, the devices were in-package etched to a typical zero bias capacitance of 1.5pF. At a reverse current of 1mA, the devices exhibited a typical breakdown voltage of 13.4 volts. Since the DC parameters were very close and the diodes were tested in the same top hat cavity, the increase in efficiency from 4.9 to 9.6 percent can only be attributed to the lower series resistance associated with the reduced GaAs mesa height.

The thick versus thin mesa height experiment performed on wafer #I10292 was also carried out on wafer #I10293. Again, the thin mesa devices exhibited a factor of 2 improvement in efficiency over their thick mesa counterparts. As part of the deliverable requirements, five thick and five thin mesa diodes were supplied to NASA-Lewis on two occasions. In addition to the first shipment of diodes, a duplicate of our top hat cavity was also provided.

Because of the experimental results from wafers I10292 and I10293, subsequent 60 GHz epitaxial material were processed into thin (10-15 microns) single mesa devices. Additionally, the conventional 2-2.5 mil thick gold plated heat sink was reduced to 2-5 microns in the thin single mesa devices. To select possible candidates for later use on diamond heat sinks, several diode lots were thermocompression bonded onto ODS-138 copper packages. Using copper as a heat sink, Table 6.1 shows that diodes from five different OMCVD wafers were able to produce output powers ranging from 280mW to 385mW. While there were other OMCVD wafers, their diodes' performance was poor as a result of high reverse breakdown voltages (>16 volts) and, consequently, high operating voltages.

As shown in Table 6.1, the best RF performance (on copper heat sink) was achieved from wafer #85-1049. However, experimental data of output power as a function of operating current (see Figure 6.4) indicates that the copper heat sink devices were thermally limited. As shown in Figure 6.4, the output power increased as the operating current was increased to 195mA. Beyond this current level, the devices failed as a result of not being able to dissipate the heat efficiently. To alleviate this situation, die from wafer #85-1049 were TCB onto metallized Type IIa diamonds (see Figure 5.3 in Section 5.1). When evaluated in the top hat cavity, the following characteristics were obtained:

		TCB Diamond Heat Sink	(Copper heat sink)
Operating voltage	=	21.9 Volts	22.6 Volts
Operating current	=	213mA	194mA
Output power	=	420mW	385mW
Oscillation frequency	=	59 GHz	58.5 GHz
Conversion efficiency	=	9.0%	8.8%

As expected, the above results show that with a diamond heat sink, it is possible to increase the bias current level. Consequently, the output power increases. Nevertheless, the increase in output power

TABLE 6.1: RF TEST DATA FROM OMCVD WAFERS USING COPPER AS THE HEAT SINK.

Wafer No.	V_b [Volts]	C_o [pF]	I_{op} [mA]	V_{op} [Volts]	P_o [mW]	F_{op} [GHz]	η [%]
85-1044	13.1	1.98	300	20.9	340	55	5.4
85-1045	14	1.45	170	22.7	340	59	8.8
85-1048	14	1.85	201	22.4	330	54.5	7.3
85-1049	14	1.75	194	22.6	385	58.5	8.8
95-1052	15	1.85	235	22.9	280	54.5	5.2

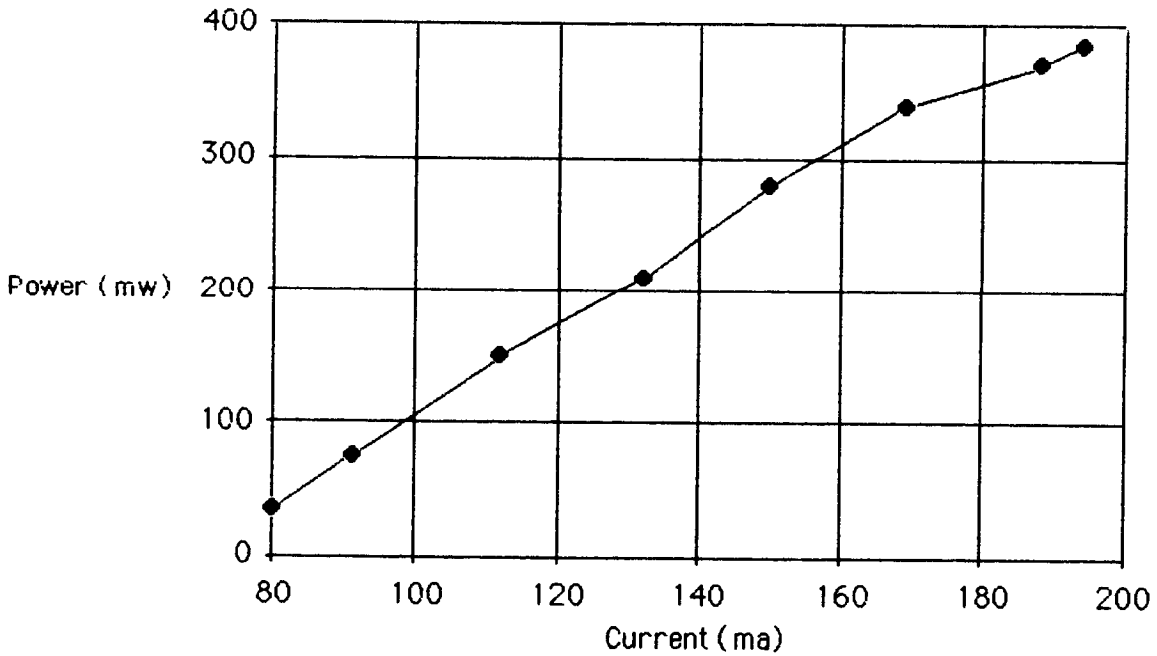

Figure 6.4: Output power versus operating current for a 60GHz HDD IMPATT (OM-85-1049) thermocompression bonded onto a copper heat sink.

from the diamond heat sink devices was well below the anticipated value. The reason for this was thought to be due to a poor bonding interface between the diamond and copper package, and/or an impedance mismatch as a result of the diode's position in the cavity (the diode was assembled on a 4 mil high diamond).

To remedy the situation presented by TCB diamonds, die from wafer #85-1049 were bonded onto diamond embedded packages manufactured at M/A-COM (see Figure 5.5 in Section 5.1). As with other RF evaluations mentioned above, the diodes mounted onto diamond embedded packages were tested in the top hat cavity. Using an optimized choke structure (L = 30 mils and D = 70 mils) and diode holder (H = 35 mils), the following results were achieved:

Operating voltage	=	23.5 volts
Operating current	=	286mA
Output power	=	520mW
Frequency	=	55 GHz
Efficiency	=	7.7%

The above results indicate that devices on embedded diamonds were able to operate at a current density that was approximately 35 percent higher than that for devices on TCB diamonds. To determine if the devices on embedded diamonds were thermally limited, experimental data of output power was plotted against operating current. As shown in Figure 6.5, the output power increased as the bias current was increased. Beyond 286mA of operating current, the devices did not fail as a short or open circuit; however, a power roll-off was observed as the current was increased.

Unlike the graph of Figure 6.4, which indicates that the devices were thermally limited, the plot given in Figure 6.5 is typical of a device that is electronically limited. The reason for the electronic limitation, as manifested by a power roll-off with an increase in bias current is not fully understood. However, efforts were made to improve

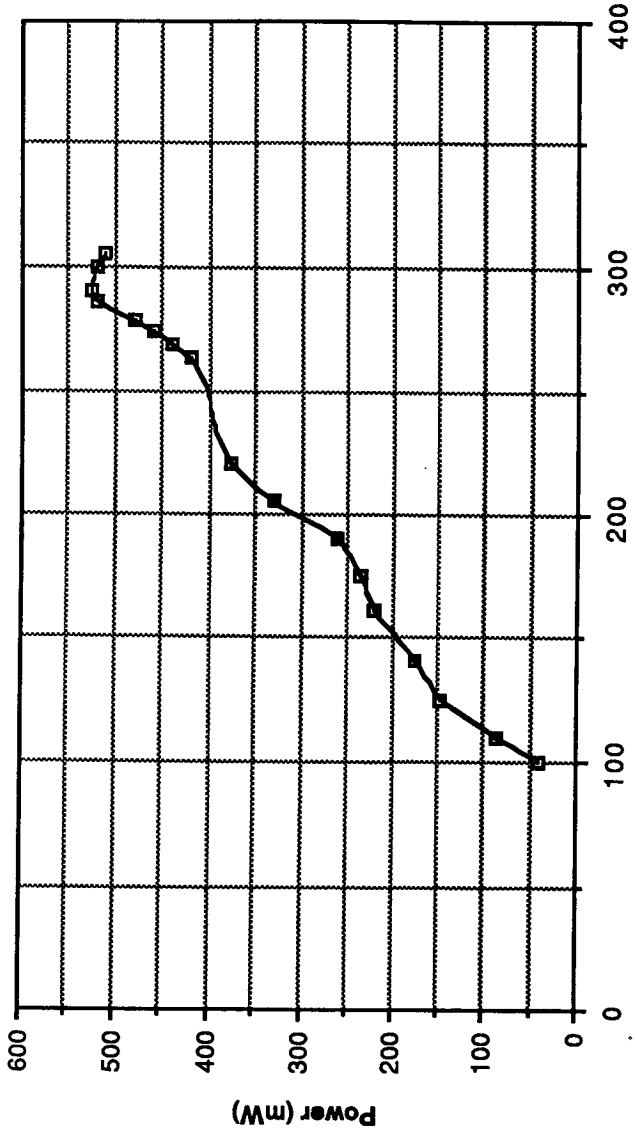

Figure 6.4 Output power versus operating current for a 60GHz HDD IMPATT (OM 85 1049) thermocompression bonded onto an embedded diamond.

the device performance by varying the parasitic capacitance and inductance of its package. The parasitic capacitance was reduced by using a smaller ceramic spacer (OD = 16 mils; ID = 8 mils, H = 4 mils), while the inductance was varied by employing different strap configurations. Based on the RF test results, optimum performance was achieved when the diode was assembled on an embedded diamond in the large ceramic spacer (OD = 32 mils; ID = 16 mils; H = 8 mils) and cross-strapped with 1/2 X 3 mil gold ribbons. The RF test data for this situation is the same as that given above.

Since the device performance (wafer #1049) did not improve with adjustments in the package parasitics, investigations were made to determine if there were deficiencies associated with its doping profile. As discussed in Sections 2 and 3, the wafer's doping distribution was determined using C-V/step etching techniques and mesa diode evaluations. While these measurement techniques were able to determine the drift and avalanche doping levels, they were unable to yield the carrier concentration at the junction because of the limitation imposed by zero bias depletion.

To circumvent the zero bias limitation, the epitaxial doping profile was determined by Secondary Ion Mass Spectroscopic (SIMS) analysis. As shown in Figure 3.33, SIMS analysis was able to produce a continuous plot of doping versus thickness for wafer #1049. The doping and thickness values were close to the I10293 design parameters given in Table 3.4. However, an examination of the P-side of the junction in Figure 3.33 reveals that the acceptor concentration in the P-active layer is not uniform. Instead of being flat at 1.8 X 10^{17} acceptor atoms/cm^3, the profile gives the appearance of a high-low doping distribution with 6.5 X $10^{17}cm^{-3}$ at the junction and 1.3 X $10^{17}cm^{-3}$ at the P^{++} interface.

For high efficiency operation, it would be desirable to have a double-drift IMPATT device with a high-low (or low-high-low) doping distribution on each side of the junction. With such a doping

distribution the electric field increases towards the junction and, hence, causes an increase in the probability for ionization. In a properly designed high-low (or low-high-low) profile, the ionization process is confined to the narrow, "high" doping (avalanche) region and does not spill over into the "low" (drift) region. Because of the increased probability for ionization and the confinement of the avalanche process, a high-low IMPATT produces higher efficiency than one with a uniform profile.

The unintended high-low profile on the P-side of the junction of Figure 3.33 may be why diodes from wafer #1049 only produced 580mW of output power instead of 1 watt at 60 GHz. Another reason could be due to losses associated with the top hat circuitry. With the unintended high-low profile, devices from wafer #1049 may have suffered from one or more of the following deleterious IMPATT effects: (a) tunneling, as a result of the "high P-type" doping at the junction; (b) ionization in the "low P-drift" region because the inappropriate high-low (P-type) doping parameters could not confine the avalanche process to the narrow "high" doping region; (c) series resistance from the undepleted "low-P-layer" caused by the charge clump under the "high-P" region.

Once the graded profile was recognized, via SIMS analysis, corrective actions were taken to produce uniformly doped P-drift regions (see Section 3). Some of the OMCVD hybrid double-drift wafers that were subsequent to run #1049, were grown with uniformly doped P-drift regions. However, the RF characteristics of diode lots fabricated from these wafers were poor as a result of their doping profile deviations from the design specifications.

Inspite of the deficiency cited in the doping profile of wafer #1049, diodes fabricated from this wafer produced the best RF test data when compared with other diode lots that were investigated during this program. As part of the final deliverable items, Table 6.2 gives the DC and RF test data of 25 diodes that were supplied to NASA-Lewis.

TABLE 6.2 DC and RF Characteristics of GaAs HDD IMPATTs Delivered to NASA-Lewis

Diode No.	C_o [pF]	V_b [Volts]	V_{op} [Volts]	I_{op} [mA]	P_o [mW]	F_{op} [GHz]	η [%]
1	2.3	14.0	21.6	273	500	55.5	8.5
2	2.3	14.0	21.8	270	520	54.0	8.8
3	2.09	14.0	21.9	270	530	55.0	8.9
4	1.73	13.8	21.0	212	500	55.7	11.2
5	1.80	13.3	20.7	205	500	54.2	11.7
6	1.96	13.6	20.9	234	500	54.0	10.2
7	1.78	13.7	21.1	230	510	54.5	10.5
8	1.59	14.0	20.5	190	500	56.5	12.8
9	2.06	13.6	21.2	261	520	54.1	9.4
10	2.06	14.3	21.5	223	500	55.7	10.4
11	2.06	14.0	21.2	242	500	55.7	9.7
12	1.95	14.5	21.6	244	510	56.7	9.7
13	2.07	14.2	21.1	237	520	57.4	10.4
14	2.06	14.2	22.5	265	500	55.2	8.4
15	2.20	14.5	22.7	260	530	56.1	9.0
16	1.60	13.8	21.4	210	505	57.6	11.2
17	1.71	14.0	21.3	198	500	58.7	11.8
18	1.84	14.0	22.5	256	500	54.0	8.7
19	1.76	13.8	21.2	239	500	55.0	9.8
20	1.78	13.8	21.7	239	500	55.0	9.6
21	1.76	13.7	21.3	242	500	55.3	9.7
22	1.71	13.8	21.1	212	500	55.9	11.2
23	1.73	13.8	21.2	212	505	55.5	11.2
24	1.74	13.8	21.6	230	500	55.0	10.1
25	1.72	13.8	20.9	216	500	55.8	11.1

SECTION 7
CONCLUSIONS

7.0 INTRODUCTION

As a result of this program, we have designed, fabricated and tested GaAs hybrid double-drift IMPATTs that oscillated at 57 GHz. At this frequency of operation, the diodes were able to produce 580mW of CW output power with a DC to RF conversion efficiency of approximately 8%. The above test results were achieved in a top hat cavity.

Two sets of design parameters for 60 GHz HDD IMPATTs were generated by computer simulations performed at the University of Michigan. The first set of parameters were based on a drift-diffusion model that utilized the static velocity-field characteristics for GaAs. Devices fabricated with those parameters produced oscillations that were much lower than the desired frequency. This type of behavior was attributed to deficiencies in the drift-diffusion model. For example, the model did not consider the effects of velocity undershoot and delay of the avalanche process due to energy relaxation in GaAs.

Using an energy-momentum model, which included the deficiencies of the drift-diffusion model, a second set of doping profile parameters were generated for 60 GHz HDD IMPATTs. Devices fabricated with the revised doping profile parameters produced oscillations around 58 GHz. However, the output power from these devices was very low. The poor RF output power is speculated to be due to a heavily punched-through device as a result of its low doping on the N-drift region. During operation, the electric field in the N-drift region could have been high to initiate impact ionization there and , consequently, ruin the RF characteristics of the device.

To achieve epitaxial wafers according to the design specifications, two growth techniques were employed, namely: H-VPE and OMCVD. While OMCVD techniques were being developed, H-VPE growth attempts were made to produce 60 GHz HDD structures. Of the various attempts

during the early part of this program, two H-VPE wafers (I10292 and I10293) produced results which suggested that the N-type drift doping of the revised design profile was low.

During the course of various calibration growth runs and modifications in system design, several accomplishments were made in the area of epitaxy. Some of these include the following:

(a) A thorough characterization of the growth parameters for submicron epitaxial layers of high electrical quality.
(b) The development of a highly reproducible N-type doping technology using silane.
(c) Demonstration of extremely sharp doping transitions.
(d) Reproducible growth of P-type layers using dimethylzinc.
(e) The demonstrated capability to produce 60 GHz double-drift IMPATT structures.

With the advancement of submicron N and P-type growth technologies, we have developed/explored techniques to successfully characterize these epitaxial wafers using:

(a) Conventional C-V/step etching techniques;
(b) Automatic electro-chemical profiling for continuous plotting of N and P-type doping profiles;
(c) Raster and line scanning (using a SEM) of cleaved cross-sections for thickness evaluations;
(d) Secondary Ion Mass Spectroscopy (SIMS) for complete profiling of 60 GHz HDD structures. This technique overcomes the zero bias limitation of C-V measurements and thus, provides doping profile information at the junction.

The initial approach in fabricating 60 GHz double-drift IMPATTs utilized existing X-Band process technologies. While the preliminary results were encouraging, significant improvements were realized after modifying certain process parameters. Based on the RF test results, it

was evident that by reducing the GaAs mesa height from 30μm to 15μm we were able to increase the device efficiency by a factor of 2. Additionally, the conventional 50-65 microns thick gold PHS was reduced to 2-5 microns so as to prepare the chips for assembly onto diamond heat sinks. Without the thick PHS, the junction of the device could be positioned closer to the diamond for efficient heat transfer.

Of the various wafers that were fabricated, the best RF performance was achieved from OMCVD wafer #1049 that was grown to the specifications of H-VPE #I10293. Devices from this wafer were first TCB onto ODS-138 copper packages. Experimental data of output power versus bias current indicated that the devices were thermally limited. To alleviate this situation, the devices were then TCB onto Type IIa diamond packages. These packages, manufactured in-house, utilized ODS-138 threaded bases into which the metallized diamonds were hand pressed. In comparison with devices on copper heat sink, which produced 385mW with 194mA of operating current, those on embedded diamonds were able to produce 580mW with 313mA of current. Instead of being thermally limited, the devices on embedded diamonds were electronically limited.

Efforts to improve the device performance (beyond 580mW of output power) by varying the parasitic inductance and capacitance of its package were unsuccessful. The parasitic capacitance was reduced by using a smaller ceramic spacer (OD = 16 mils; ID = 8 mils; H = 4 mils versus 32; 16; 8), while the inductance was varied by using different strap configurations. These efforts revealed that optimum performance (580mW at 57 GHz) was achieved with the larger ceramic spacer and cross-strapped, 1/2 X 3 mil gold ribbons.

One of the reason why diodes from wafer #1049 only produced 580mW of output power instead of 1 watt at 60 GHz may be due to the diodes' doping profile. Another reason could be due to losses associated with the top hat circuitry. An examination of the SIMS profile for wafer #1049 reveals that the acceptor concentration in the P-active layer is not

uniform. Instead of being flat at 1.8 X $10^{17}cm^{-3}$, the profile gives the appearance of a high-low doping distribution with 6.5 X $10^{17}cm^{-3}$ at the junction and 1.3 X $10^{17}cm^{-3}$ at the P^{++} interface.

The unintended high-low profile may have caused devices from wafer #1049 to suffer from one or more of the following deleterious IMPATT effects: (a) tunneling, as a result of the "high P-type" doping at the junction; (b) ionization in the "low P-drift" region because the non-optimum high-low (P-type) doping parameters could not confine the avalanche process; (c) series resistance from the undepleted "low-P-layer" caused by the charge clump under the "high-P" region.

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