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20 GHz Spacecraft IMPATT Solid State Transmitter

T. Best
Y.C. Ngan

TRW Electronic Systems Group
One Space Park
Redondo Beach, CA 90278

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Lewis Research Center
21000 Brookpark Road
Cleveland, OH 44135

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. INTRODUCTION

This report details the engineering development of a solid-state transmitter amplifier operating in the 20-GHz frequency range. The development effort involved a multitude of disciplines including IMPATT device development, circulator design, multiple-diode circuit design, and amplifier integration and test. The program objective was to develop a transmitter amplifier which would demonstrate the feasibility of providing an efficient, reliable, lightweight solid-state transmitter to be flown on a 30 to 20 GHz communication demonstration satellite. The work was performed under contract from NASA/Lewis Research Center for a period of three years.

The result of this effort was the development of a GaAs IMPATT diode amplifier capable of an 11-W CW output power and a 2-dB bandwidth of 300 MHz. GaAs IMPATT diodes incorporating diamond heat-sink and double-Read doping profile capable of 5.3 W oscillator output and 15.5 percent efficiency were also developed. Up to 19 percent efficiency was also observed for an output power level of 4.4 W. High performance circulators with a 0.2 dB insertion loss and bandwidth of 5 GHz have also been developed. These represent a significant advance in the state-of-the-art in both device and power combiner circuit technologies in K-band frequencies.

One area needing further improvement is the diode yield. Although we have demonstrated up to 5.3 W CW output power per device, there were not enough of these devices for the 6-diode power combiner development, thus we were forced to revert to the devices having the more typical output power level of 2 W. Nevertheless, the 11-W power combiner output power does indicate a highly efficient and nearly optimum combiner circuit design. We believe that the circuit design is sufficiently versatile to accommodate higher power devices.

The contents of this report are summarized as follows: Section 2 describes the program objectives, specifications, and requirements; Section 3 presents design methodology, fabrication and performance of IMPATT diodes developed in the program; Section 4 contains discussions on circuit development on the program as well as key component development, such as circulators and current regulators, and the relevant electrical and mechanical drawings. Measurement data obtained from functional tests are presented in Section 5. Section 6 discusses the overall achievement of the program, implications of

the results, and assessment of future development needs. All discussions which are mostly mathematical in nature are presented as appendices so that the presentation in the other sections is not obscured. Finally, all references used for the report are listed at the end of the report.

2. PROGRAM OBJECTIVE

The objective of this program was to develop 20 GHz GaAs IMPATT diodes supplying 4.5 W output power with 20 percent conversion efficiency and a junction temperature of less than 250°C. This effort involved the design and fabrication of IMPATT diodes with double drift read (DDR) doping profiles.

With the successful development of these diodes, a six-diode combiner module capable of 20 W output power, with an overall dc-to-RF conversion efficiency of 17 percent, and 8 dB gain over the 19.7 to 20.2 GHz frequency range was to be developed.

3. IMPATT DIODE DEVELOPMENT

3.1 MATERIAL GROWTH AND CHARACTERIZATION

The double drift Read device structures developed at TRW for this program were grown by molecular beam epitaxy (MBE) using a Varian MBE 360 exclusively in the GaAs IMPATT diode layer growth. The MBE system (Figure 3-1(a)) employs ion and titanium sublimation pumps as well as liquid nitrogen cooling shrouds to obtain vacuum in the low 10^{-11} torr range prior to epitaxy growth. The system has eight source furnaces, allowing flexibility in the choice and number of doping sources. Four doping sources were employed for the IMPATT diode epilayers; two silicon sources were used for the n-type GaAs material. This technique allows the furnaces to be set at independent temperatures, one high for n^+ buffer layers and n^+ spikes, the other low for the n-drift and avalanche regions.

Similarly, two beryllium sources are used for p-type GaAs layers. The source furnace flange on the Varian system is depicted in Figure 3-1(b). The complete IMPATT profile consisting of eight separate layers can be grown in one continuous sequence with this source configuration. The step from high to low doping requires only the simultaneous opening and closing of the source doping shutters. The shutters and growth time are controlled by a microprocessor. It is unnecessary to stop the growth to change source temperatures when using all four doping sources. The aluminum source is employed for the growth of AlGaAs, which is used as a stop etch layer prior to IMPATT layer growth.

3.1.1 Material Preparation and Growth

The substrates used for the MBE growth were n^+ GaAs silicon doped with $n = 2 \times 10^{18}$ cm^{-3}. They were carefully cleaned and the growth surface etched before being mounted on molybdenum blocks with indium and loaded into the system. The substrates were heat-cleaned in an arsenic flux to remove residual oxides from the surface. Typically, a growth temperature of 575°C was used. An n^+ buffer layer was first grown on the substrate for most of the IMPATT material described here. The IMPATT profile layers were then grown sequentially.

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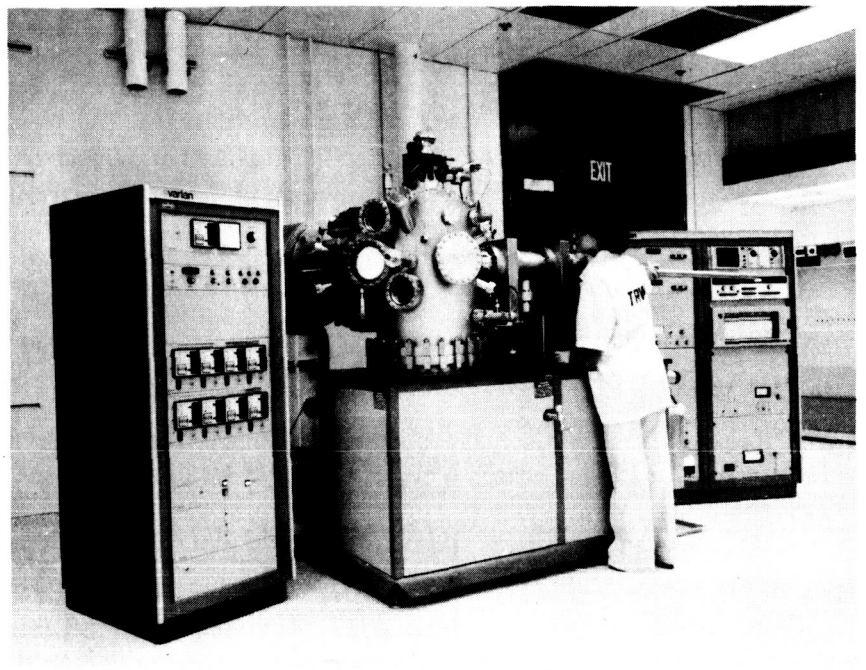
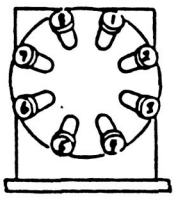


A. MBE-360 SYSTEM

MBE-360 SOURCE FLANGE



1) SILICON
2) ARSENIC
3) GALLIUM
4) ALUMINUM
5) BERYLLIUM
6) SILICON
7) SnTe
8) BERYLLIUM

B) MBE FURNACE ASSIGNMENTS

Figure 3-1. TRW's MBE system

The Ga flux was adjusted to obtain a 110 A/minute growth rate. Very abrupt changes in doping profiles can be obtained with this slow growth rate and the fast source shutter times. Transition regions between high and low doping levels can be on the order of tens of angstroms, a distinct advantage of MBE at the high IMPATT operating frequencies.

3.1.2 Material Characterization

Numerous techniques employed to determine the doping profile of the IMPATT material grown by MBE are briefly detailed below.

N-W Profiling.

Measurement of the net effective doping profile by C-V profiling techniques is an invaluable tool to monitor material growth from run-to-run. Gold dots are deposited on the wafer and mesa etch to isolate the structure. The C-V profile is then measured and net effective doping versus depth N-W is obtained. These plots will be shown in the following section.

SIMS Profile

Secondary ion mass spectroscopy (SIMS) has been used to measure the dopant density as a function of depth, providing an independent check of the doping profile and abruptness of the transitions. The concentration levels are, unfortunately, only accurate within a factor of 2.

The IMPATT breakdown voltage characteristics can also be measured on the test mesas. This allows mapping of the electrical characteristics of the entire wafer to determine uniformity.

The double drift Read profile (Figure 3-2) was chosen for the IMPATT material growth for 20 GHz. Forty layers have been grown in the TRW MBE system. This material is summarized in Table 3-1, where the MBE run number refers to growth in the Varian 360 system and the DKR number refers to the particular lot processed for IMPATT diodes. Not all wafers are processed, and some may be processed on two or more lots and receive separate DKR numbers.

Five design profiles, described below, were grown at K-band: TRW-A, TRW-B, TRW-C, Raytheon, and TRW-HE. Data reflecting the best performance of each particular lot is shown in Table 3-1. The best power (P_o = 5.37 W) was obtained from lot DKR21 of the TRW-B design. It must be noted that this power was not corrected for losses in the circuit. The best efficiency (η = 19 percent) was obtained from lot DKR26 of the TRW-6 design; this value is also uncorrected for circuit efficiency.

The doping profile of the TRW design is shown in Figure 3-3. The sharpness of the doping region transition is seen in the SIMS profile of wafer MBE 302 (Figure 3-3). The net effective doping profile for MBE 227, the highest power lot, is shown in Figure 3-4. The peak at 0.2 μm is the net effective doping level of both spikes (p and n); however, the p^+ spike depletes completely before the n^+ spike and the p^+ drift region are depleted. The p-drift doping level is $p = 1 \times 10^{16}$ cm^{-3} as desired. A value of

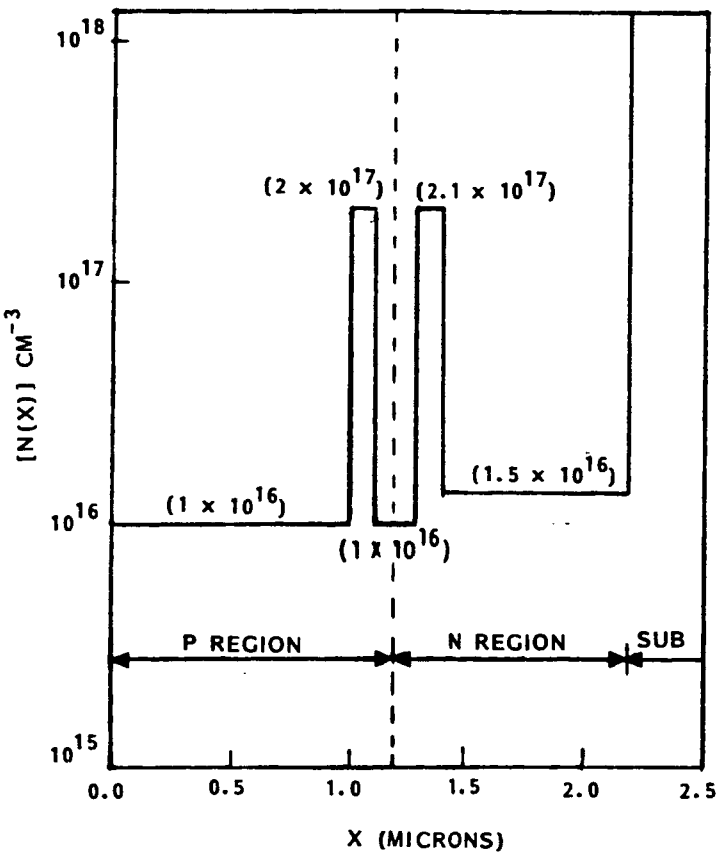


Figure 3-2. GaAs double-drift read profile for 20 GHz

Table 3-1. Performance summary

MBE NO.	DATE	DESIGN	DKR NO.	DATE	P_o (mW)	FREQUENCY (GHz)	EFFICIENCY (%)	V_{br} (V)	CAPACITY (pF)	COMMENTS
166	6/16/83	TRW-A	1a	7/07/83				45.00	19.00	
168	6/23/84	TRW-A	2f	2/01/84	3,890	20.34	12.80	29.50	11.10	n = 13.7
174	7/19/83	TRW-A	3a	8/22/83	910	20.74	5.00	31.50	13.40	
181	8/18/84	RAYTHEON	7c	12/06/83	144	17.00	0.70	25.00	14.23	
183	8/25/83	RAYTHEON	8c	12/06/83				34.00	16.00	NO OSC
185	9/01/83	RAYTHEON	6b	9/30/83	560	18.67	4.00	31.50	9.17	
190	9/29/83	RAYTHEON	10a	11/04/83				43.00	15.00	NO OSC
192	10/10/83	RAYTHEON	11c	1/09/84	1,230	18.22	4.80	34.50	13.13	
199	10/28/83	RAYTHEON	13c	1/09/84	1,000	18.74	6.50	39.50	9.53	
200	11/04/83	RAYTHEON	14c	1/19/84	1,620	18.70	5.80	39.00	10.20	
204	11/22/83	TRW-B	15b	2/09/84	1,620	18.37	5.90	30.50	10.13	
210	12/19/83	MOD.RAYTH.	16a	2/08/84				46.00	11.00	NO OSC
212	12/23/83	MOD.RAYTH.	17a	2/08/84	1,860	19.48	8.20	33.50	12.52	
218	1/30/84	TRW-B	18a	2/16/84	2,230	20.30	10.20	30.50		
220	2/03/84	TRW-B	19a	2/24/84	3,230	19.77	12.40	30.50	10.94	
220	2/03/84	TRW-B	22	3/23/84	3,230	19.84	12.50	28.50	12.24	MOD PROC
225	2/17/84	TRW-B	20a	3/07/84	3,020	19.32	11.50	26.50	10.06	
227	2/24/84	TRW-B	21a	3/07/84	5,370	18.28	15.50	26.00	12.07	n = 16.0
227	2/24/84	TRW-B	25	5/03/84	3,090	17.80	9.10	30.00	11.15	MOD PROC
231	3/07/84	TRW-B	23	3/23/84	2,450	19.31	11.70	28.00	10.00	
235	3/20/84	TRW-C	24	3/30/84	3,010	18.00	9.70	36.00	11.70	
238	3/29/84	TRW-C	26	5/03/84	4,360	19.93	19.00	29.50	12.45	P = 4.78
257	6/11/84	TRW-C	27	6/25/84				38.70		$>V_b$
259	6/15/84	TRW-C	28	7/31/84	575	20.40	5.90	22.10		$<V_b$
261	6/20/84	TRW-C	34	9/07/84				27.60		E238
264	7/18/84	TRW-C	31	8/22/84	2,810	18.60	11.40	25.10		E238, <p
266	7/23/84	TRW-C	32	8/22/84	1,690	19.00	9.10	23.60		$>W_{av}$
268	7/27/84	TRW-C	33	8/22/84	3,230	18.30	12.40	24.20		$<W_{av}$, N = 14
271	8/13/84	TRW-C	35	9/24/84				21.60		$<V_b$
272	8/15/84	TRW-C	36	9/24/84	478	20.70	7.40	29.70		<W, <P
279	8/29/84	TRW-C	37	9/24/84	1,730	19.50	9.20	30.20		<W, <P
285	9/21/84	TRW-C	38	10/10/84				31.00		E238
287	9/26/84	TRW-HE	39	10/10/84				29.00		LOW P
289	10/01/84	TRW-HE	40	11/05/84				31.00		LOW P
294	10/22/84	TRW-C	41	11/05/84	670	18.40	7.40	31.00		
299	12/18/84	TRW-C	42	1/18/85	2,240	18.70	13.90	29.00		
300	12/20/84	TRW-HE	43	1/18/85	1,900	21.30	9.40	30.00		HIGH EFF
302	1/08/85	TRW-C	44	2/11/85	3,470	19.27	12.90	24.00		
304	1/16/85	TRW-B	45	2/11/85	3,800	18.10	15.90	20.00		E227, $<V_b$
305	1/22/85	TRW-B	46	2/11/85	3,980	19.83	15.70	22.00		$<V_b$
308	1/31/85	TRW-B	51	4/11/85	2,950	18.76	11.10	29.00		REPROCESS
310	2/07/85	TRW-B	52	4/11/85	3,390	18.58	12.70	27.00		E227

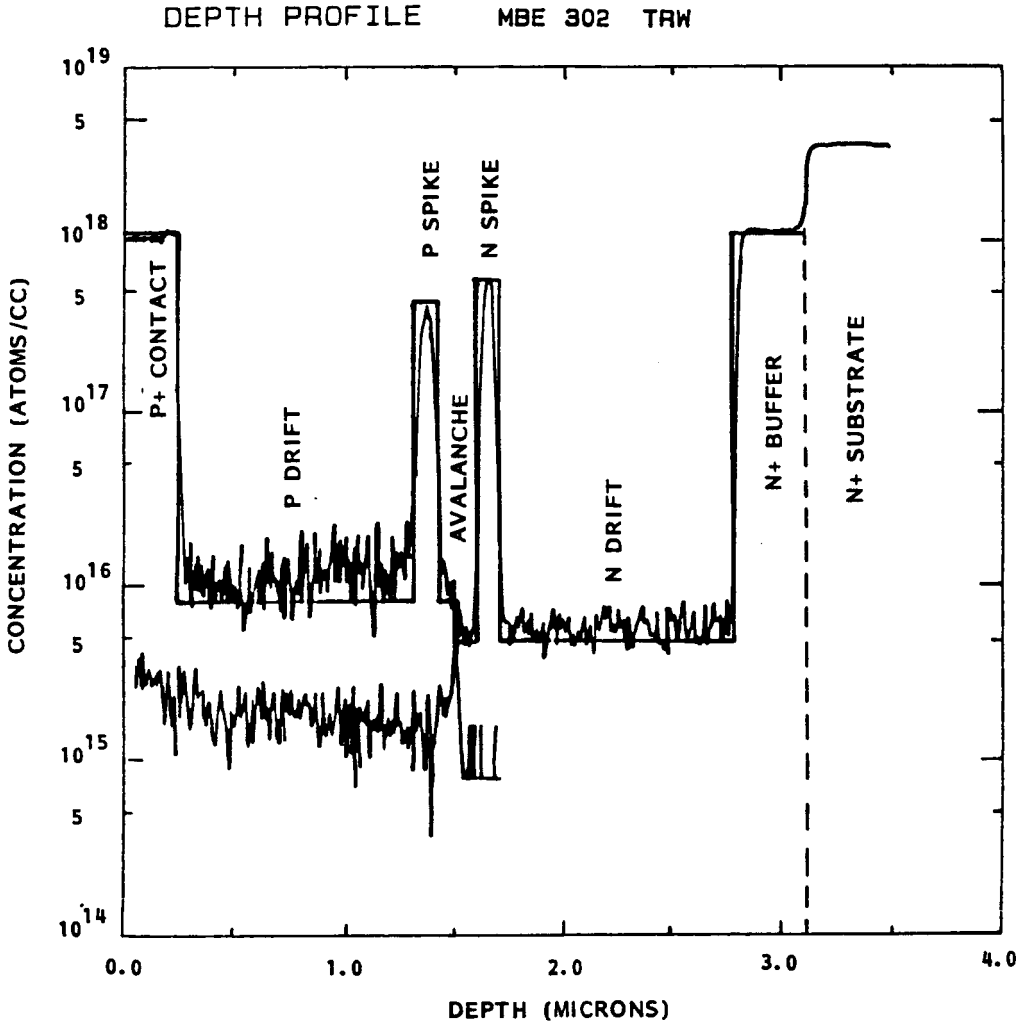


Figure 3-3. Doping profile of 20 GHz IMPATT diode

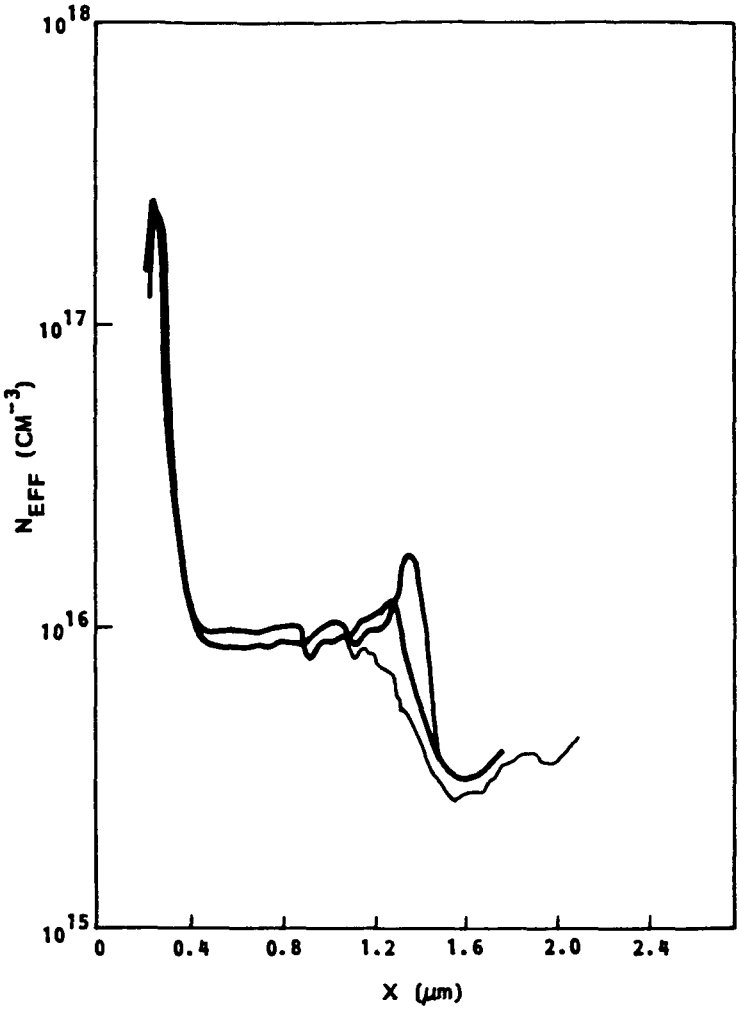


Figure 3-4. Net effective doping profile for MBE 227

n = 3 x 10^{15} cm^{-3} is found for the n-drift layer as desired. The structure has a device thickness of w = 1.2 μm when totally depleted, which is very close to the design thickness. The rounding of the transactions is due to the limited resolution of the C-V profiles. The breakdown voltage map for half of this wafer (1-inch diameter) is shown in Figure 3.5. The spread across this wafer has a sigma of σ = 3.4 V. This non-uniformity in electrical characteristics was one difficulty in the combiner development.

3.2 DEVICE PROCESSING AND PACKAGING

TRW has an established GaAs mesa IMPATT diode process which is used with diamond heatsinking. Figure 3-6 is a flow diagram of the fabrication process which is discussed below.

		28.5	26.8	25.6	25.2		
	30.7	28.5	27.2	25.5	25.0	26.8	
32.0	29.6	27.9	26.5	25.0	25.0	26.4	29.5
31.9	29.0	27.9	26.1	24.8	25.9	26.6	28.8
31.2	28.9	L	25.4	25.0	26.5	26.8	29.5
30.2	27.9	26.2	25.1	25.8	26.8	27.3	
	27.1	25.5	25.7	25.6	27.1	28.8	
		25.6	26.2	25.6	28.0		

$\overline{V}_B$ = 26.8

σ = 3.4

#Pts. = 50.0

Figure 3-5. Breakdown voltage map for MBED 227

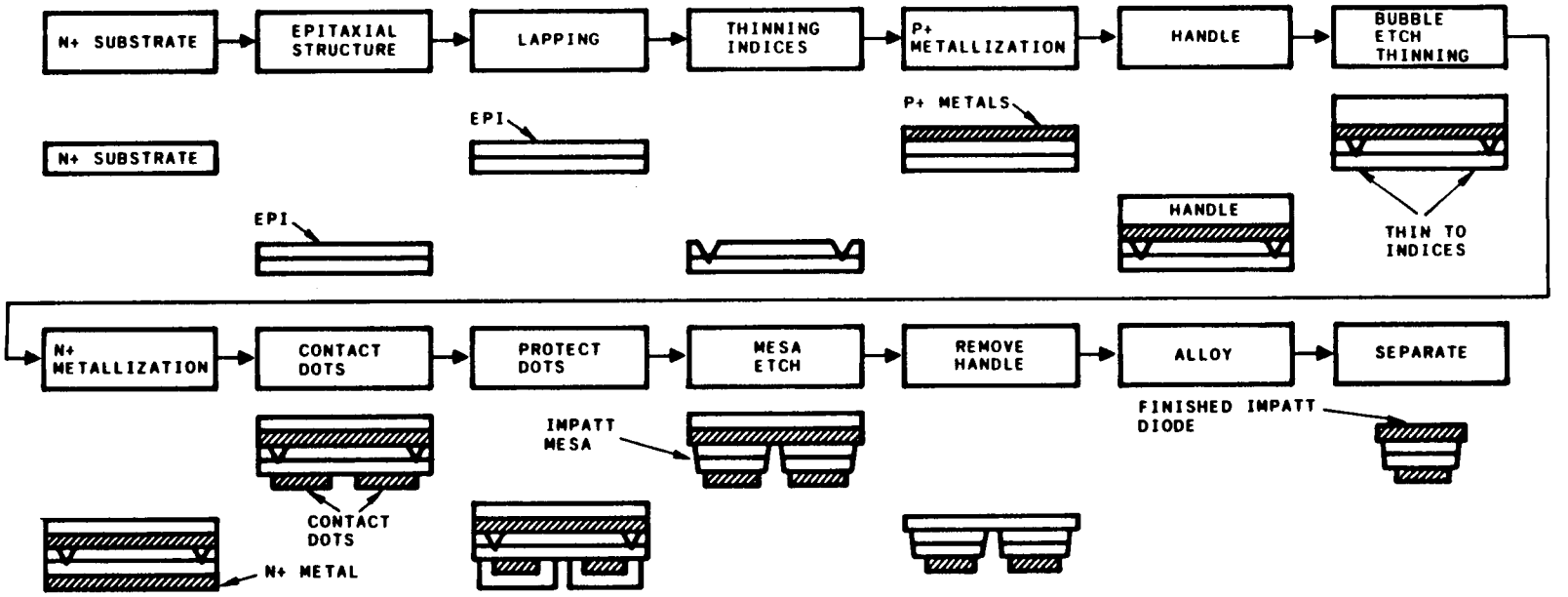


Figure 3-6. Flow diagram for GaAs DHS mesa diode process

Each epitaxial wafer introduced into the IMPATT fabrication process is identified with a process traveler sheet, which allows the wafer to be monitored at any point in the sequence. All fabrication information is permanently recorded on the traveler sheet for later reference. Pertinent information, such as n^+ and p^+ metallizations and diode thicknesses, is also entered into an HP9845 computer for later device optimization.

Lapping

The wafer is mounted on the center of the quartz plug using red wax. The original thickness of the mounted wafer is measured using a surface caliper. The wafer is polished down to a thickness of 4 mils with Br_2-MeOH (4:250 by volume) solution using a lapping machine under a hood. The wafer is then demounted and cleaned, and the final wafer thickness measured with a caliper and recorded. Lapping is done before any processing is performed on the wafer to ensure wafer thickness uniformity.

Thinning Indexes

The thinning indexes, unique to TRW, are used in conjunction with bubble etching to accurately thin the diode to less than a skin depth.

Waycoat negative photoresist is spun on the epi side of the wafer, air dried, and baked at 95°C for half an hour. The indexing mask, consisting of 15 mil dots, is exposed and developed. After 1 hour of hard bake at 110°C, the index patterns are etched using H_3PO_4/H_2O_2/MeOH (1:1:1) to a depth of 10 to 15 μm, depending on the diode frequency desired. (The skin depth is 15 μm at 44 GHz.) The depth of the indexes is measured with a Dektak (also see bubble-etch thinning).

P+ Metal

P+ metallization is done on the Perkin-Elmer 2400 sputtering system using Pt/TiW/Pt/Au (250/800/1000/5000 Å).

Handle

A handle is added to support the wafer after thinning. This is done by spinning thick negative Waycoat photoresist on a quartz or sapphire disk. The wafer is then mounted on the disk in the center with the epi side down and baked dry at 95°C for an hour. The photoresist provides good wafer adhesion to the disk and provides support through the remainder of the processing.

Bubble Etch Thinning

The wafer is clamped and dipped into the solution facing the bubbler using a bubble-etch apparatus using a solution of H_3PO_4:H_2O_2PMeOH (1:1:1). A regulated flow of nitrogen is introduced into the bubbler.

After etching for 10 seconds, the wafer is removed and inspected. Etching continues until the thinning indexes start to appear. Remember that these indexes determine the required final diode thickness. This technique ensures uniform thinning to the desired diode height.

N+ Metal

N+ metals consisting of 800 Å AuGe and 5000 Å Au are sputtered using a Perkin-Elmer 2400 sputtering system.

Contact Dots

Photolithography is used to define contact dots. With the wafer still mounted to the quartz disk, it is spun with Waycoat negative photoresist, air-dried, and baked at 95°C for 30 minutes. A 2-mil dot mask is then exposed and developed. After a hard bond at 110°C for one hour the gold pads are etched in KI-I_2 solution.

Protection Dots

Another layer of Waycoat negative photoresist is spun on the wafer to protect the contact dots during etching. A 5-mil dot mask is aligned to the 3-mil contact dots, exposed, developed, and baked at 110°C for two hours.

Mesa Etch

Mesas are etched using $H_2SO_4/H_2O_2/H_2O$ (7:2:1) solution, which is stirred throughout this step. The wafer is held at different angles to get uniform etching. To prevent overetching, etched mesas are covered with black wax.

Remove Handle

The wafer is removed from the quartz disk by immersing in 712-D stripper heated at 95°C.

Alloy

The wafer is alloyed for 15 seconds at 450°C in H_2 atmosphere in a hydrogen annealing furnace.

Separate

The diodes are placed in acetone and separated by using ultrasonic vibration.

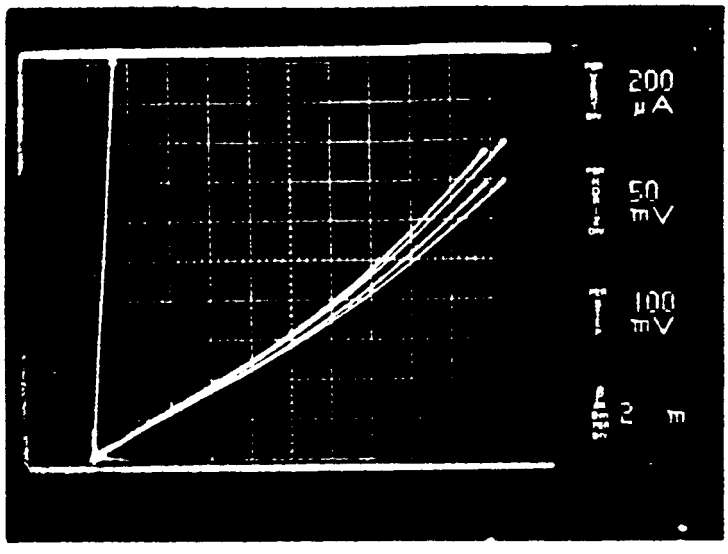
The metallization process for the fabrication of IMPATT diodes was described previously. It is important that a good ohmic contact be formed to the GaAs for good device performance. A series resistance of a few tenths of an ohm can have a significant detrimental effect on diode efficiency. The AuGe-Ni-Au contact to the n^+ substrate side of the diode provides an excellent contact. This is a commonly used contact to n-type GaAs and is considered very reliable.

Ohmic contacts to p-type GaAs have been an ongoing problem. The most common contact metallization has been a Au:Zn alloy. This is not an acceptable technique for IMPATT diodes because the Zn diffuses readily into the active areas of the device. The reliability of such devices is very low.

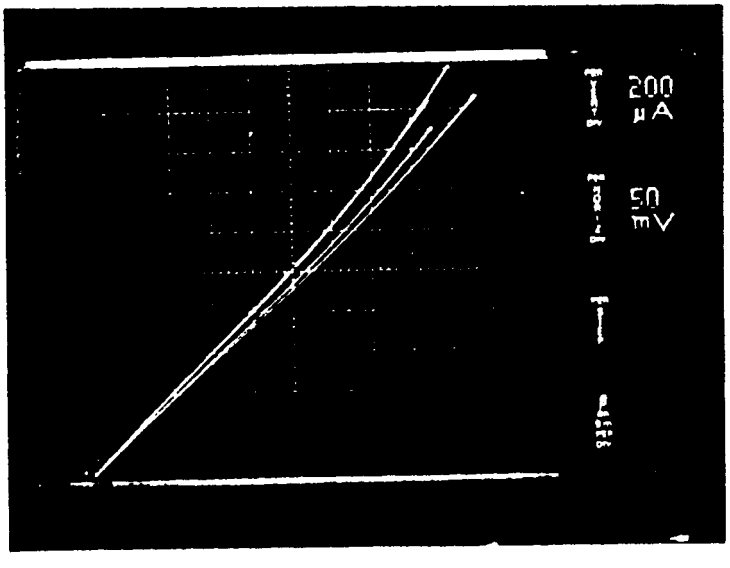
The p-contact metallization presently used in the TRW process is Pt-TiW-Pt-Au metallization. This has proved to be a very good, reliable contact. The contact resistance of several pure metals and alloys was examined for this phase of the program. The contact resistance was calculated using the transmission line model (TLM) measurement approach of Berger [1]. Contacts are evaporated and the patterns defined lithographically. To determine specific contact resistance, the resistance between contact pads of various separations was measured.

Pt:Au was evaporated on p+ GaAs ($p = 1 \times 10^{18}$ cm^{-3}) to measure the contact resistance of the standard process metallization. The I-V characteristic of the as-deposited Pt contact is shown in Figure 3-7(b). The contact is ohmic and a contact resistance of $R_C = 4.37 \times 10^{-3}$ ohm-cm^2 was obtained. In searching for an improvement in the ohmic contact, an Au:Mn alloy was examined, was evaporated, and the pattern defined. This was then alloyed and the contact resistance measured. The I-V characteristics of the alloyed Au:Mn contact are shown in Figure 3-7(a). The contact resistance was $R_C = 4.5 \times 10^{-3}$ ohm-cm^2, which is comparable to that of Pt.

Significant progress was then made in realizing a low resistance ohmic p+ contact metallization. An alloy of 4 percent by weight Mg in Au was prepared in an electron beam evaporation system [2]. A test pattern consisting



A) ALLOYED AuMn



B) As-DEPOSITED Pt

Figure 3-7. Comparison of p+ contact metallization I-V characteristics

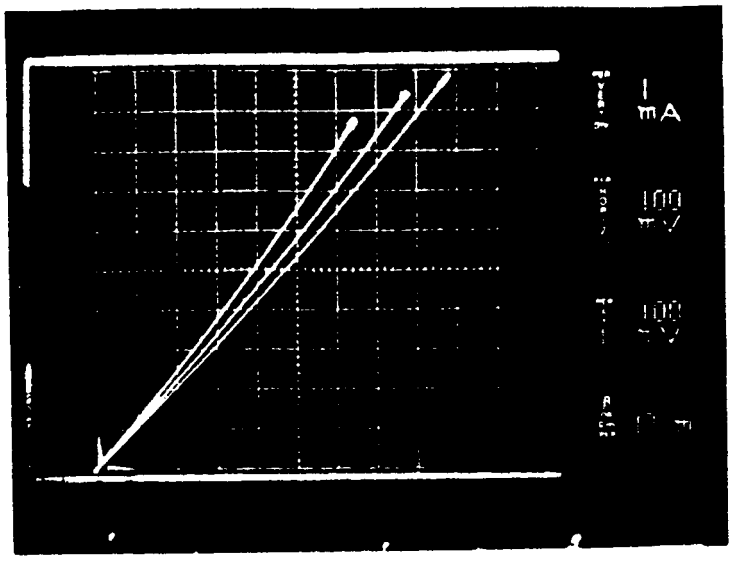
of pairs of rectangular contact pads having different separations was defined by photolithography on p+ epilayer ($p = 1 \times 10^{18}$ cm^{-3} and 0.25 μm thick) which was grown on a semi-insulating substrate (MBE 241) specifically for this investigation. The metallization system consisted of an Au-Mg:Au-Au "sandwich" structure (50 Å : 500 Å : 800 Å). The test pattern was defined by conventional photoresist "liftoff" techniques. The sample was alloyed at 360°C for 30 seconds in a hydrogen atmosphere to form the ohmic contact. The I-V trace is shown in Figure 3-8(a). The plot of gap resistance versus gap separation is shown in Figure 3-8(b). The contact resistance was calculated from these measurements to be $R_C = 3.99 \times 10^{-4}$ ohm-cm^2.

The primary advantage of the Au:Mg alloyed contact is that it has a contact resistance as low as gold-zinc, but the diffusivity of magnesium in GaAs is two orders of magnitude lower than zinc in GaAs. As a result, the reliability of the Au:Mg contact is expected to be superior to the Au:Zn contact. The diffusion coefficients of several elements are given in Table 3-2. The lower contact resistance is expected to significantly lower series resistance and improve the conversion efficiency of the devices. We have reprocessed MBE 195 to demonstrate this advantage. This lot has not been packaged at this time.

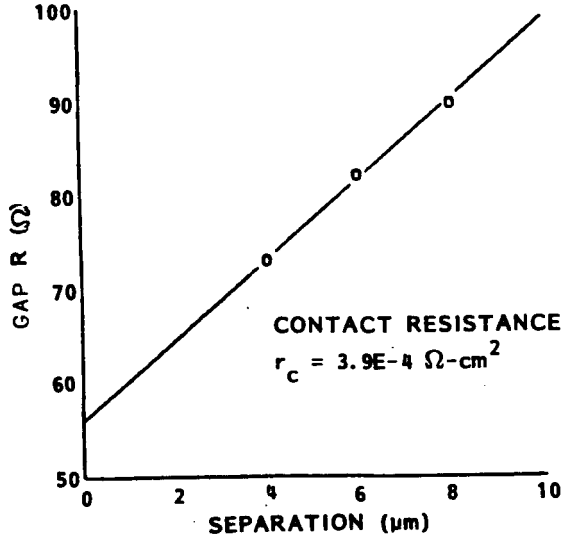
TRW has developed a diamond heatsink GaAs IMPATT diode packaging process. A flowchart of this packaging process is shown in Figure 3-9, and photographs of the package parts are shown in Figure 3-10. Each step is described in detail below. Excellent thermal resistance measurements have been obtained for GaAs IMPATTs using this process. Since the diode package is a circuit element which is extremely critical for device-to-circuit-impedance matching, the package parasitics must be carefully tailored and controlled for operation at millimeter wave frequencies. Optimum package parasitics, minimum thermal resistance, and minimum RF loss are essential, and dictate the choice of package configurations for this program. The diodes fabricated for this program used a ring package which yields consistently good results at this frequency. It is also mechanically stable, hermetically sealable, and easily reproducible.

Package Components

The process of optimizing package parasitics was accomplished by using a variation of package components at each frequency.



A) I-V CHARACTERISTICS



B) GAP RESISTANCE MEASUREMENT

Figure 3-8. AuMg contact metallization on p+ GaAs

3-8. AuMg contact metalization on p+ GaAs

Table 3-2. Diffusion properties of various elements in GaAs

ELEMENT	D_o	ΔE
Mg	2.6×10^{-2}	+2.7
Zn	0.15	+2.49
Mn	0.65	+2.49
Au	1×10^{-3}	+1.0

$D = D_o \epsilon^{\Delta E/kT}$

D_o = DIFFUSION CONSTANT

ΔE = ACTIVATION ENERGY

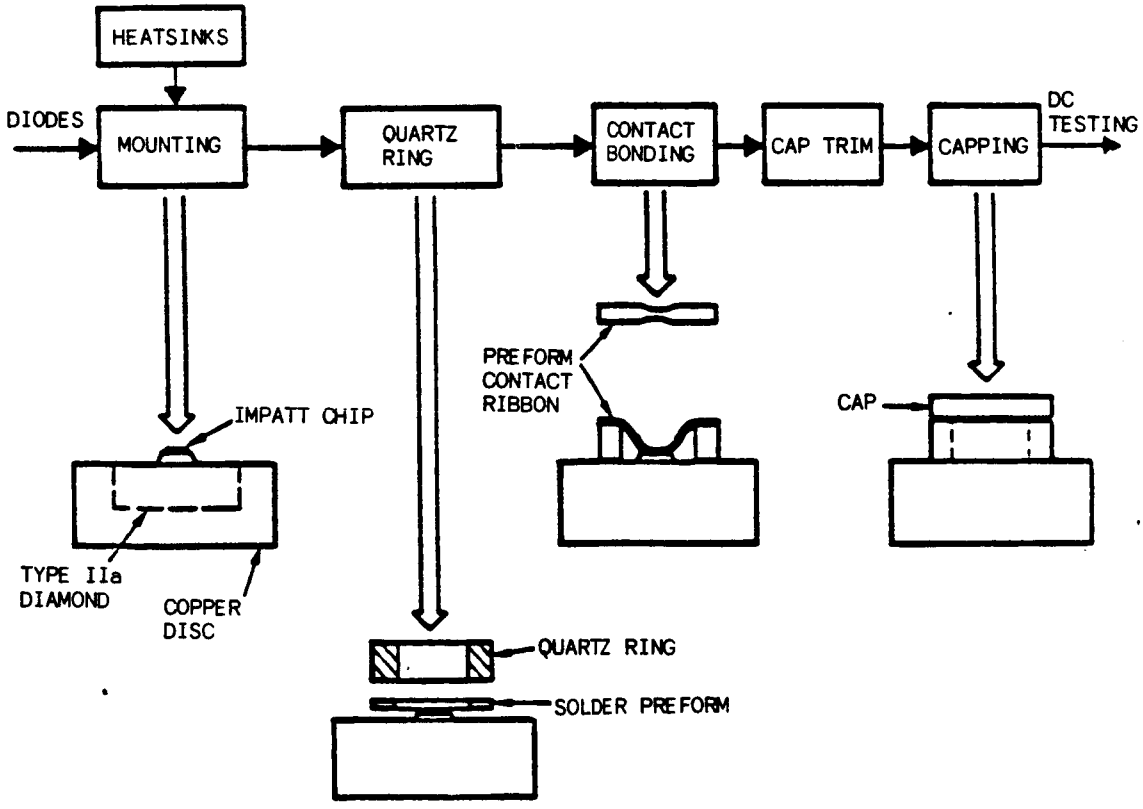
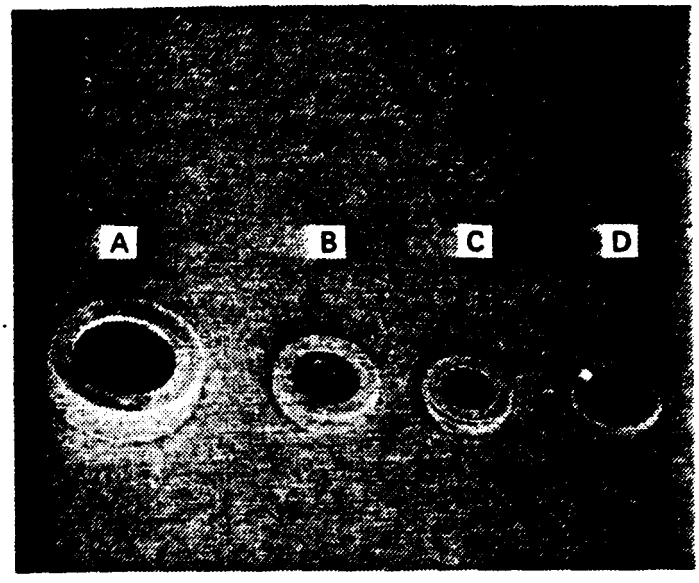


Figure 3-9. Schematic of IMPATT diode packaging process



(A) LARGE CERAMIC

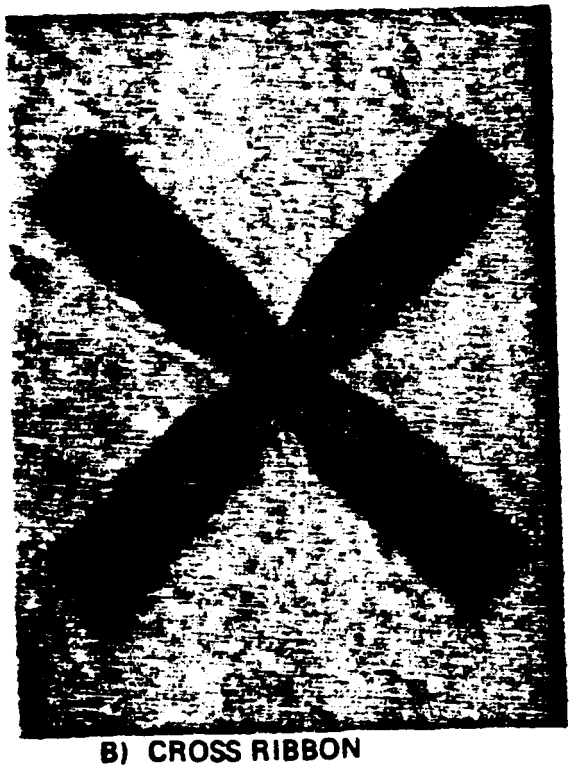
(B) SMALL CERAMIC

(C) THICK QUARTZ

(D) THIN QUARTZ

SEM PHOTO OF CERAMIC AND QUARTZ RINGS

A) FULL RIBBON



B) CROSS RIBBON

Figure 3-10. Photographs of ring and ribbon package parts

Two materials were used for the rings: quartz and ceramic. The dimensions and parasitic capacitance of the various rings are listed in Table 3-3. Each ring structure offers a different parasitic capacitance for impedance matching the diode to the circuit. The top and bottom are metallized with 300 Å Cr/10,000 Å Au using sputter deposition. An ultrasonic grinder and special tooling are used to cut the rings from the stock material.

Table 3-3. Ring and ribbon package parameters

QUARTZ RING	C_p(pf)	DIMENSION (OD X ID X H MILS)
QUARTZ RING - THICK WALL	0.123 ±0.002	31 X 17 X 5
QUARTZ RING - THIN WALL	0.085 ±0.002	28 X 21 X 5
CERAMIC RING	C_p(pf)	DIMENSION (OD X ID X H MILS)
LARGE CERAMIC	0.220 ±0.003	51 X 34 X 15
SMALL CERAMIC	0.255 ±0.003	35 X 24 X 7
RIBBON	L_p(nH)	DIMENSION (L X W X H MILS)
HALF RIBBON	0.18	15 X 4 X 0.5
FULL RIBBON	0.12	30 X 4 X 0.5
CROSS RIBBON	0.09	2 (30 X 4 X 0.5)
TRIPLE RIBBON	0.07	3 (32 X 4 X 0.5)

All ribbons are fabricated at TRW using photolithographic and electroforming techniques, ensuring uniform length and thickness for reproducible package inductance. The single ribbons are 100 μm wide, 7.5 μm thick, and 0.76 μm long. They are necked to 50 μm wide in the middle where they bond to the diode. This taper also helps achieve consistent bond loops to the top of the quartz rings. The ribbon preform is bonded to the top of the diode and the top of the quartz ring.

Package Assembly

Heatsinking

Type IIA diamond heatsinking is used for the 20 GHz IMPATTs. The diamonds are 0.76 x 0.76 square and 0.025 cm high. They are metallized with 300 Å Cr/5000 Å Au and hot-pressed into a gold plated copper stud (0.15 cm diameter and 0.064 cm high)

Thermocompression Bonding

The GaAs IMPATT diodes are thermocompression bonded to the heatsink. Since the diode and diamond surfaces are both metallized with gold, a gold-to-gold bond is formed.

The weight required for bonding was determined experimentally. For bonding weights less than 160 grams, the diodes came off the heatsinks during ultrasonic vibration. For weights greater than 160 grams, the GaAs IMPATT diodes were cracked. Therefore, an optimum TC bonding weight of 160 grams was determined. The temperature was 280°C and a bonding time of 2 minutes was used.

Ring Soldering

An Au/Sn solder preform is used to bond the ring to the heatsink. All soldering operations are done in the package soldering station. This bell jar system allows melting of the preform in a forming gas (10 percent H_2 in N_2) environment. Otherwise, the Au/Sn preform will oxidize and incomplete wetting would occur.

The diodes to be packaged are placed in a soldering fixture in which up to 42 diodes can be soldered at one time. The system is first evacuated and then backfilled with nitrogen to purge it. The nitrogen is then evacuated and the bell jar filled with forming gas, allowing complete wetting of the solder preform on melting and providing an excellent package seal.

Heating the diode under a partial vacuum (during the package soldering process) is also an important step to achieve high diode reliability and reproducibility. The high temperature activates any contaminants and etching residue in the package. The partial vacuum enhances the evacuation of these contaminants. Essentially, this method provides final cleaning of the package before sealing, and conditions the mesa surface for reduced surface leakage current, which is known to reduce diode reliability.

Ribbon Bonding

Bias contact to the diode is made with the previously described preform gold ribbons which have been used at TRW for the past six years. The ribbons are bonded to the diode and the top of the quartz ring. Specially adapted KS wedge bonders are used for ribbon bonding. The contact weight on the GaAs

diode is adjustable and set to 100 grams to prevent cracking of the diode during this operation.

Capacitance Trim Etching

The final diode capacitance required for impedance matching to the circuit is achieved by chemically trim etching the diode to the desired area. using a 1:1:1 solution of $H_3PO_4/MeOH/H_2O_2$. Both capacitance and electrical parameters are measured on the probe station. The final capacitance is recorded for later data analysis.

Capping

A hermetic seal is obtained by soldering a gold-plated Kovar (Ni/Fe alloy) cap to the top of the quartz ring. The cap is marked to indicate the orientation of the ribbon with respect to the heatsink to facilitate uniform mounting of the diode into the RF cavity. An Au/Sn solder preform is again used in the package soldering station.

DC Evaluation

The dc evaluation step is used to prescreen the packaged IMPATT diodes before RF evaluation. A flowchart of this evaluation is shown in Figure 3-11. This step, which is essential for screening out diodes which exhibit undesirable characteristics, saves time and labor by eliminating RF testing of bad diodes, and is also important for accumulating data for later device optimization. All measured data is put into an HP9845 computer for analysis.

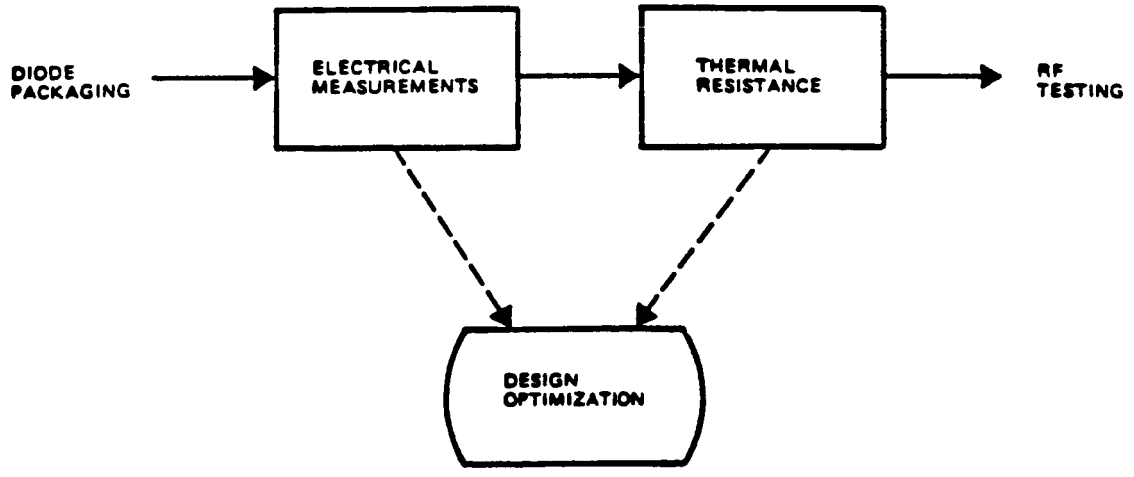


Figure 3-11. DC evaluation flowchart

Electrical Measurements

After the IMPATT chips are mounted in packages, the device I-V characteristics are examined on a curve tracer. Reverse leakage current, breakdown voltage, forward conduction current, and voltage are determined. From these, any undesirable breakdown characteristics, such as microplasmas, will be identified. The measured breakdown voltage is compared with theoretical calculations to determine premature breakdown. The leakage current is measured to determine if the junction surface has been contaminated during the in-package etching process. The slope of the I-V characteristic in the forward direction is measured to determine the series resistance of the structure.

Junction capacitance is measured using standard bridge techniques at 1 MHz on completed devices. This information is used to obtain accurate area control during in-package etching. Both zero bias (C_0) and breakdown capacitance (C_B) will be measured.

Thermal Resistance

The reverse pulse technique was used to measure the CW thermal resistance of the GaAs IMPATT diodes. This thermal evaluation method necessitates performing baseline oven measurements to monitor a temperature sensitive parameter, the 1 mA breakdown voltage is usually selected. This information takes the form shown in Figure 3-12. On completion of the oven measurement a pulse measurement is made. This involves switching the diode into reverse breakdown for a significant period of time to allow operation at a specific current level and then rapidly switching the device back to its now increased 1 mA breakdown voltage level and noting the change that has occurred as a result of internal heating of the diode. A typical pulse is shown in Figure 3-13.

It should be noted from Figure 3-13 that V_b (1 mA), i.e., the breakdown voltage at a current level of 1 mA, decays rapidly due to cooling, therefore imposing rather fast switching in order to observe V_b (1 mA) before any cooling can take place. The shift in breakdown voltage as a result of internal heating is then correlated with the baseline oven measurement and heat flow resistance is determined.

Recent thermal resistance results are shown in Table 3-4.

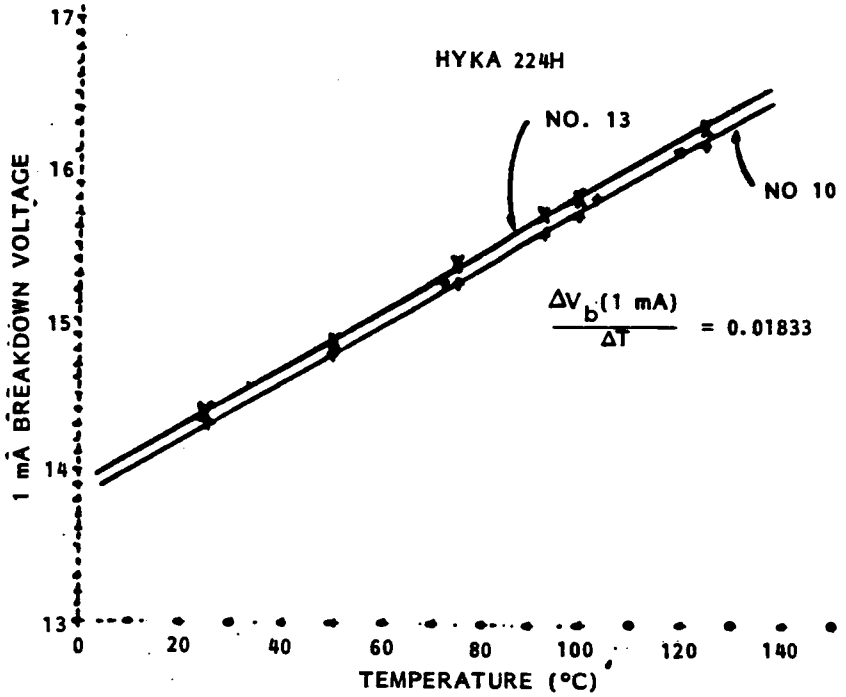


Figure 3-12. Baseline oven measurement data of V_b(1 mA) vs. temperature

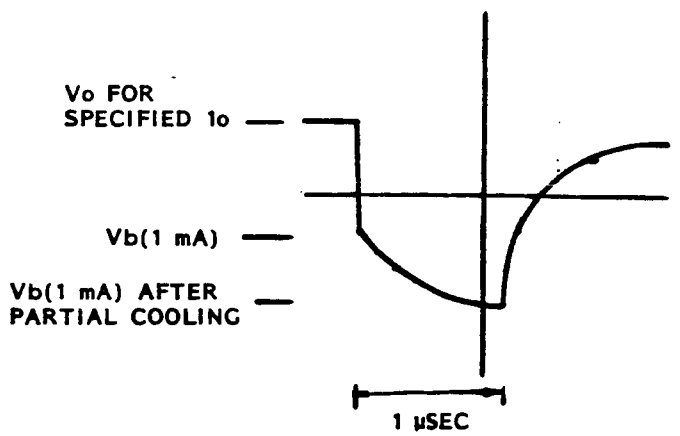


Figure 3-13. Typical reverse pulse used in thermal measurements

Table 3-4. Recent thermal resistance data

DIODE	C_o (pF)	V_b (V)	R_o (°C/W)
KR46D#1	11.21	22.0	32.4
#2	11.22	22.5	22.4
#3	11.21	22.1	17.1
#4	11.22	23.5	24.8
#5	11.05	24.0	--
#6	11.20	21.9	--
#7	11.21	21.9	23.9
#8	11.26	23.4	20.5
#9	11.20	21.2	12.7
#10	11.15	21.8	12.3
#11	11.16	22.8	13.7
#12	11.10	22.0	16.9
#13	11.07	21.8	25.9
DKR46E#1	11.54	21.6	17.7
#2	11.50	21.5	SHORT
#3	11.56	23.5	42.8
#4	11.53	22.2	21.5
#5	11.42	22.5	28.4
#6	11.53	20.9	SHORT
#7	11.50	22.9	OPEN
#8	11.49	21.5	17.3
#9	11.54	21.5	16.9
#10	11.46	23.2	15.3
#11	11.53	23.2	33.5
#12	11.53	22.0	14.3

3.3 CIRCUIT DESIGN AND RF EVALUATION

An appropriately designed cavity is essential to obtain maximum diode power output. Three circuits were investigated for the evaluation of the GaAs IMPATT devices:

1) A beveled top-hat full-height waveguide circuit developed at Cornell University

2) A reduced height, reduced width waveguide circuit originally developed by Varian, Inc.

3) A reduced-height waveguide circuit designed by TRW.

Top Hat Circuit

A top hat circuit as shown in Figure 3-14 was investigated. This circuit is distinguished by several features which differ from those of the reduced height cavities. First, the waveguide remains at full height throughout the length of the circuit, including the point at which the diode sits. There is no stepped output transformer to decrease the characteristic impedance in the waveguide section. Second, there is no coaxial well. Instead, the diode is mounted in the center of the floor of the waveguide (broadwall) with the diode sitting flush with the waveguide surface. In this type of circuit, the impedance transformation takes place solely through the bias pin, which, unlike that in the reduced height circuit, is quite broad in the middle of the waveguide and beveled down to a point at which it makes contact with the diode. The impedance transformation takes place through this bevel, increasing as the diameter gets larger. The angle of the bias pin top-hat bevel next to the diode is thus critical in determining the performance of the diode in the cavity. Because series resonance is achieved in the top hat itself, the diameter of the hat is critical in determining the frequency of oscillation.

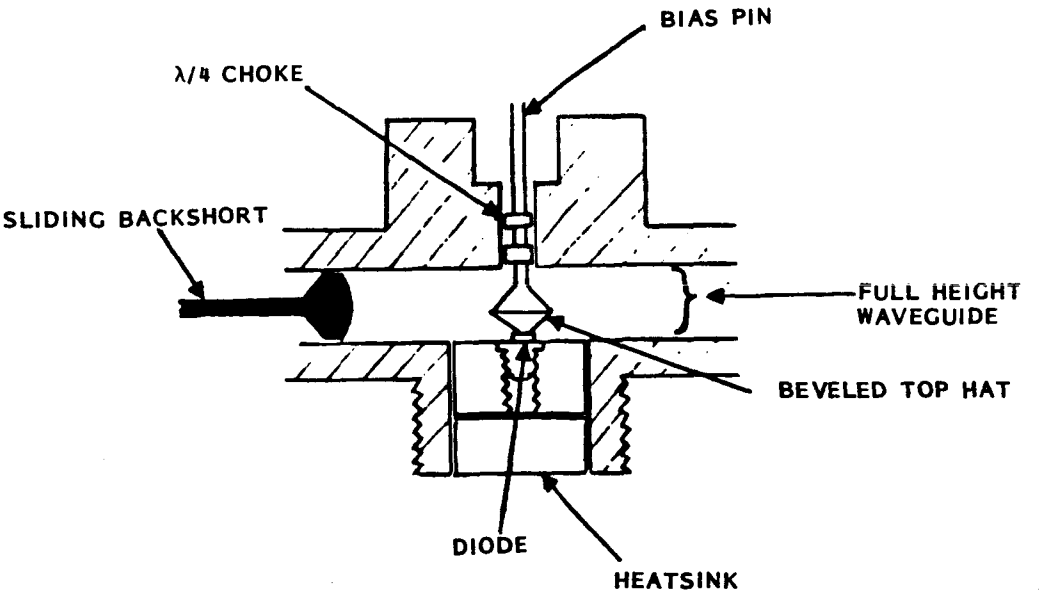


Figure 3-14. Top hat waveguide circuit

A unique mechanical feature of this circuit is the tunability of the λ/4 choke in the bias pin. The bias pin above the top hat is threaded so that the barrels which make up the low impedance sections of the choke on the pin are tunable along the axis of the pin. The tunability of this choke aids in peaking the available power output.

Unfortunately, the results achieved using the top-hat circuit were discouraging. The diodes placed in this circuit for oscillation suffered an extremely high failure rate at low bias levels. When the diodes placed in this circuit did oscillate and were tuned to peak performance, the results were consistently less than those achieved with the same diode in a reduced height circuit. Table 3-5 shows a comparison of performance with the same diode in both the reduced-height and top-hat circuits. Because many diodes were being lost in this circuit, it was decided to conduct some comparison testing using the Varian single-drift GaAs IMPATT diodes from the original amplifier program. By using these diodes to compare the circuits, the better TRW diodes manufactured for this program would not risk failure and could be saved for tuning to maximum power output. Some of the Varian diode results are also listed in Table 3-5.

Table 3-5. Top hat circuit performance comparison

	REDUCED HEIGHT CIRCUIT		TOP HAT CIRCUIT	
DIODE	POWER (W)	EFFICIENCY (%)	POWER (W)	EFFICIENCY (%)
DKR14C-6	0.298	2.0	0.0	0.0
DKR17A-6	1.86	8.2	1.12	6.6
DKR19B-8	3.23	11.3	2.51	11.4
E1112-20	1.26	14.9	0.355	8.0
E1112-21	1.35	14.4	0.389	7.2
E1172-1	1.70	12.2	1.23	9.0
VSK9250AB-2	0.537	9.4	0.537	8.8
VSK9250AB-11	0.676	9.8	0.794	11.1

The suspected causes for the lower power achieved and the greatest problems encountered with this circuit were mechanical. One problem concerned the concentricity of alignment of the bias pin. Because the waveguide section of the cavity where the bias pin passes through is full WR-42 height, there is a larger degree of freedom for lateral movement at the point at which the

bias pin makes contact with the diode. Unfortunately, even precision machining these intricate parts could not ensure that the pin always made contact at its centered position. Another problem, and probably the greatest cause for the lower power, was the extremely critical sensitivity of the diode to the angle of bevel and dimensions of the top hat. A 7-degree versus 9-degree bevel angle had a demonstrable effect on power output. Once machined, this angle is fixed and not tunable while the diode is oscillating in the cavity. This sensitivity is to be expected because it is this angle that determines the impedance match between the diode and the circuit. The same degree of sensitivity was found for the frequency with relation to the top-hat diameter.

Other problems with the top-hat circuit included the tunable choke in the bias line and the heatsink structure. The choke in the bias line was designed to be tunable along the axis of the bias pin; this tuning was critical to achieving maximum power output. However, this choke was tuned externally by tuning the bias pin, and there was no way of measuring its exact position while tuning it. Repeating power output performance was thus difficult to achieve unless the choke was left in the same fixed position. The final difficulty was the heatsink structure in which the diode was mounted; the structure was thermally excellent but very difficult to work with mechanically. Each time a new diode was to be put into the cavity, the tedious process of disassembling and carefully reassembling the circuit was involved.

Reduced Height/Reduced Width Circuit

Another circuit used in the preliminary stages of diode evaluation in this program was the reduced height/reduced width waveguide cavity shown in Figure 3-15. This circuit is fundamentally the same as the reduced height circuit that was eventually used to achieve maximum power output. The three significant differences are: 1) the output transformer, which is one step instead of two; 2) reduced width in addition to reduced height; and 3) the coaxial well, which is implemented with enclosed cylindrical spaces instead of transformer shims. A comparison of the results achieved using this circuit versus the current circuit is shown in Table 3-6. It was found that the transformer shims in the newer cavity provided a much better impedance match and thus the performance was consistently better, as shown in Table 3-6. Note

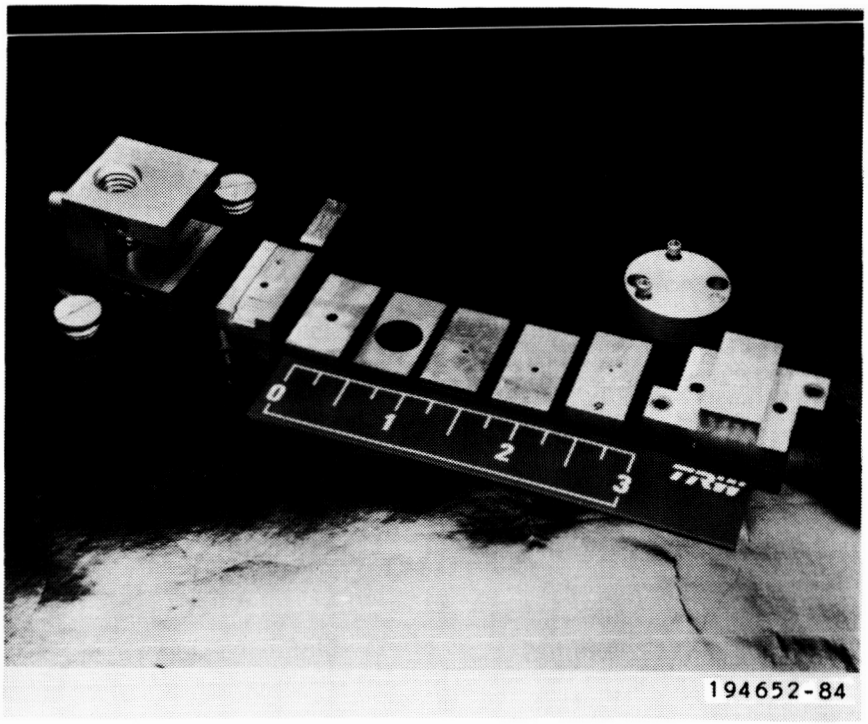


Figure 3-15. Reduced height waveguide cavity

Table 3-6. Reduced height circuits

DIODE	REDUCED HEIGHT CIRCUIT		REDUCED HEIGHT/ REDUCED WIDTH	
	POWER (W)	EFFICIENCY (%)	POWER (W)	EFFICIENCY (%)
DKR3A-2	0.851	4.4	0.758	4.3
DKR3A-4	0.870	4.8	0.912	5.0
DKR3B-1	0.758	0.7	0.346	4.5
DKR3B-4	0.095	0.7	0.309	2.2

that the power levels reported in Table 3-6 are quite low because this cavity was only used in the initial stages of the program before the better diodes were produced.

The principal limitation of this reduced height/reduced width cavity was the concentricity of alignment of the bias pin within the transformer spacers. Unless the spacers were perfectly concentric around the bias pin, the very tight fit of the pin inside the spacers that was needed could not be achieved. To present to the diode a coaxial impedance on the order of 1 ohm, the spacers that were needed could not be achieved mechanically; therefore, this cavity was abandoned for the TRW reduced height cavity.

Reduced Height Circuit

The circuit which gave the greatest performance in the RF evaluation of the 20-GHz GaAs diodes is the reduced height waveguide circuit shown in Figure 3-16. The most important factor affecting the diode output power is the impedance match between the diode and the circuit. Because the IMPATT diodes developed on this program are very low impedance devices (on the order of 1 ohm), the circuit must present a compatibly low impedance to achieve the best match possible. The circuit must therefore be designed so that it can transform this low impedance to the very high impedance (350 to 450 ohms) of the full-height waveguide output. The diode in the circuit is located in the center of the floor of the waveguide at the bottom of a coaxial well. The impedance transform is performed over two sections. First, a low coaxial impedance (~0.8 ohms) is presented to the diode in the coaxial section. To achieve this low impedance the center conductor was enlarged to a diameter just slightly smaller than that which would produce higher order modes of oscillation in the coaxial well. An extremely tight fit of the inner-to-outer conductor, aided by a very thin dielectric insulator (<1 mil), allows this low impedance. The first impedance transform occurs in the coaxial well with the use of the transformer shims. With enlarged holes in the transformer shims, the impedance gradually rises away from the diode. The second impedance transform occurs in the waveguide output section after the coaxial-to-waveguide transition. This impedance transformation is made up of $1/4\,\lambda$ waveguide sections stepped up in height to the WR-42 full-height waveguide. Since the value of the characteristic impedance Z_0 is proportional to the waveguide height b, this $1/4\,\lambda$ transformer gradually increases the impedance according to the height of the waveguide section. The bandwidth for this transformer was found to be sufficiently greater than 4 GHz using only two steps as shown in Figure 3-16.

A lowpass filter, located in the bias line above the top wall of the waveguide, was added to the circuit to increase the performance. This filter serves the functions of providing dc isolation for the bias line, providing the proper harmonic terminating impedance, and, most important, establishing an additional tuning element required to stabilize the diode at its operating frequency.

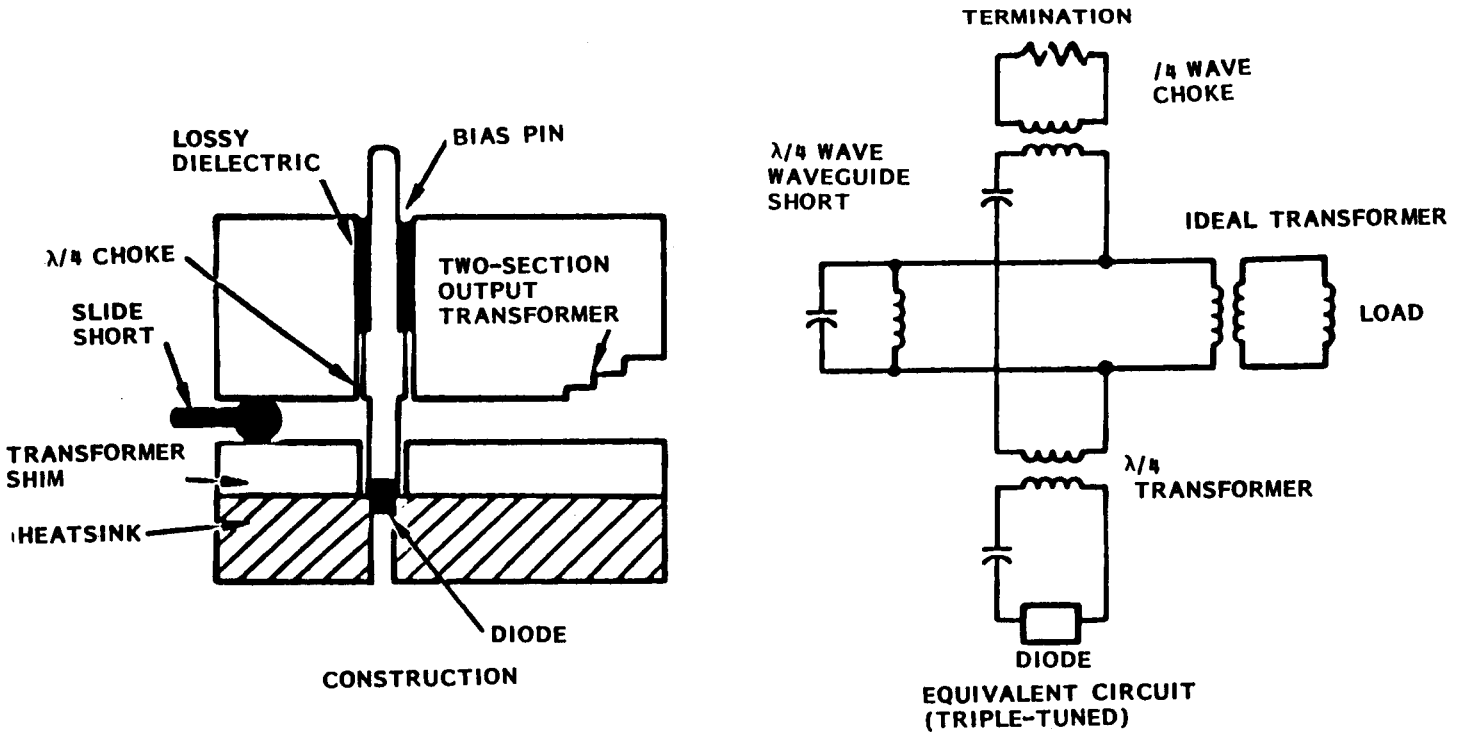


Figure 3-16. Reduced height waveguide circuit

As the development of high power 20 GHz GaAs IMPATT diodes on this program progressed, the limiting factor to better performance was identified as premature output power saturation. This phenomenon manifests itself as a decrease in power output with an increase in bias drive after a sufficiently high bias has been achieved. This result is caused by oscillations on the bias line or subharmonic oscillations in the circuit producing power at undesirable frequencies, thus sacrificing power output at the fundamental. In an effort to reduce the effects of this phenomenon, we first attempted to diminish bias oscillation by using Brackett's method [3]. A dc pass, rf choke was put into the bias line, but no change was observed in the power saturation. We then focused on addressing the problem of subharmonic oscillations in the circuit. In an effort to prevent oscillations at the first subharmonic frequency, a radial filter was implemented in the coaxial well of the bias line beneath the floor of the waveguide. Unlike our attempt at using Brackett's method, this filter was placed as close as possible to the diode to stem the build-up of subharmonic oscillations close to the diode plane. With the filter implemented, the diode bias could be driven higher and power output increased as much as 2 dB before power saturation occurred.

Silver Plating

An investigation was conducted early in the program on the dependence of circuit performance on the conductivity of the material used in the circuit. The material used for the bias pin, transformer shims, and cavity housing for the reduced height circuit was gold-plated half hard brass. Because it is suspected that most of the loss incurred in the circuit occurs very close to the diode, an attempt was made at minimizing this loss by using materials with very low electrical resistance. Specifically, silver plating was applied to the transformer shims and bias pins in the reduced height cavity and the oscillator performance was compared against that with pure brass and gold plated parts. The resistance of silver compared with that of gold is:

	Electrical Resistance ($\mu\Omega$cm)
Gold	2.19
Silver	1.59

The results of the comparison, listed in Table 3-7, overwhelmingly indicate that using either gold or silver has very little effect on the performance of the circuit. The conclusion drawn was that the material used had far less of an effect on the circuit performance than did the dimensions determining the impedance of the circuit. Note on Table 3-7 that most values listed for the silver parts are either identical to or lower than the performance of the circuit using the gold parts because the diode was tuned to peak power using the gold shims with an optimum circuit configuration. The silver plated parts were made on identical size parts; however, the size changed slightly because it is very difficult to control the thickness of silver plating. Thus the difference in the values measured is probably a result of the slight difference in the shim and pin dimensions.

Table 3-7. Silver parts comparison

DIODE	GOLD PIN AND SHIM		SILVER PIN AND SHIM	
	POWER (W)	EFFICIENCY (%)	POWER (W)	EFFICIENCY (%)
DKR19B-6	3.38	10.7	3.38	10.6
DKR19B-6	3.09	9.8	3.31	10.1
E1112-20	1.26	14.9	1.05	13.6
E1112-21	1.35	14.4	1.10	11.4
E1112-31	1.32	14.5	1.15	15.1

RF Evaluation Results

The RF test setup used for evaluating the 20 Ghz IMPATT diodes is shown in Figure 3-17. The IMPATT diode is mounted inside the oscillator cavity which is then rigidly fixed to the 90-degree waveguide twist at the front end of the waveguide test setup. The setup contains a frequency meter and spectrum analyzer for monitoring the frequency response of the oscillator output, and a variable attenuator and power meter for making precision oscillator power output measurements. The high power load absorbs most of the power output to prevent damaging the more sensitive measurement equipment with lower power ratings. The insertion loss of the waveguide setup, from the input at the 90-degree twist through and including the thermistor mount, ranges from 11.64 to 12.52 dB across the frequency range of 18 to 22 GHz.

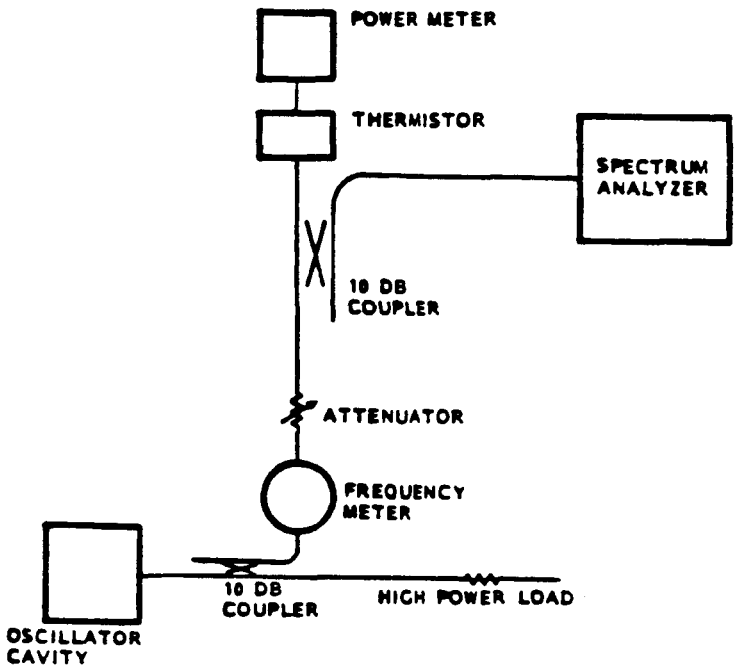


Figure 3-17. Test setup for 20 GHz GaAs double drift diodes

The reported power outputs are those recorded at the waveguide flange. The best results for power and efficiency are summarized in Table 3-8. The program goals and results achieved are summarized below.

	Goal	Performance Achieved
Output power (W CW)	4.5	5.37
Center frequency (GHz)	19.7 to 20.2	18.2
Conversion efficiency (%)	20	15.5
Junction temperature (°C)	250	~300

It should be noted that the diode output power figures quoted in the test data in Table 3-8 were obtained with the test circuit optimally matched to the diode at one single frequency. For a wideband operation, such as the case of the amplifier, the diode output capability must be degraded. This results from the fact that the power-bandwidth product of a single diode stage is invariant. That is, for a maximum output the bandwidth of the stage must be comparatively narrow. Conversely, for a large operating bandwidth, the output power must be lowered.

Table 3-8. Sample of diodes with above average output power and dc-to-RF efficiency

EPI RUN	DIODE LOT	POWER OUTPUT (W)	EFFICIENCY (%)	FREQUENCY (GHz)
238	DKR26M	4.36	19.0	18.08
238	DKR26C	3.80	18.3	18.09
238	DKR26N	3.24	16.3	20.80
238	DKR26G	3.09	16.0	22.24
304	DKR45B	3.80	15.9	18.10
227	DKR21E	4.89	15.8	18.35
168	DKR2K	3.55	15.8	18.15
305	DKR46B	3.39	15.8	19.56
168	DKR2N	2.95	15.7	18.66
238	DKR26D	2.95	15.4	19.95
227	DKR21F	5.37	15.5	18.28
238	DKR26C	4.78	16.1	19.93
238	DKR26B	4.67	14.3	19.10
238	DKR26M	4.67	18.3	18.38
235	DKR24B	4.36	13.2	19.91
227	DKR21B	4.07	12.0	18.28
305	DKR46B	3.98	15.7	19.83
238	DKR26N	3.98	14.8	19.77
304	DKR45B	3.80	15.9	18.10
168	DKR2K	3.63	15.7	18.15

4. AMPLIFIER DEVELOPMENT

The amplifier development in this program is conveniently classified into four areas: circuit development, circulators, constant voltage biasing, and bias regulators. A description of the development of these elements is presented in the following sections.

4.1 IMPATT CIRCUIT DEVELOPMENT

Due to the high output power requirement, the output stage is, of necessity, a multidiode circuit. Nonlinear interactions among the diodes impose restrictions on circuit performance. Consequently, the output stage is always the limiting member in an amplifier chain in terms of output power and operating bandwidth. There are two possible approaches to meet the power and operating bandwidth. One is to develop an IMPATT amplifier operating in the stable amplifier mode; the other is to develop an IMPATT amplifier operating in the injection-locked oscillator mode.

Although the stable amplifier mode has the potential of wide operating bandwidth, the circuit requires the use of 3-dB hybrid couplers to achieve power combining. This scheme has the following disadvantages:

- Because of hybrid losses, the coupler is only capable of combining up to four diodes. This mandates the use of 6-W IMPATT diodes, which are nonexistent at the present time
- Stable amplifiers generally have lower gain than injection-locked amplifiers, consequently the required 8 dB gain could not be achieved with one stage
- Hybrid-coupled amplifiers are, in general, more bulky than injection-locked oscillators. The larger number of stages also increases the overall size.

In contrast with the stable amplifier mode, the injection-locked oscillator mode offers the following advantages:

- Many diodes can be combined in a very small volume
- The high gain required in this program should be achievable in a single stage
- A resonant cavity is used as the medium for power combining.

There are basically two configurations of resonant cavities suitable for 20 GHz circuits: the cylindrical cavity and the rectangular waveguide cavity.

The cylindrical configuration has enjoyed great success at lower frequencies due to its compact size. At 20 GHz, however, the diameter of the cavity is about 1.5 cm (0.45 inch), making it too small to accommodate the required number of IMPATT diodes. A larger diameter cylindrical cavity is not recommended because of the problem of overmoding; the number of resonant modes within a specific frequency range varies with the square of the cylinder radius. On the other hand, the waveguide cavity can accommodate a large number of diodes by increasing only the longitudinal dimension of the cavity. This results in a linear increase in the number of resonant modes rather than a quadrate increase, as in the case of the cylindrical cavity. Consequently, mode spacing is large and single mode operation is possible. An added advantage of the waveguide cavity is the direct interface with the output waveguide, because the cross-sectional dimensions of the cavity are identical to those of the waveguide. Based on these considerations, the waveguide cavity configuration was adopted for this amplifier development.

The basic construction of a rectangular waveguide combiner is shown in Figure 4-1. It essentially consists of a number of individual diode modules coupled to a rectangular waveguide through the sidewalls of the guide. The resonant cavity is formed by a short circuit on one end and an iris opening on the other. The diode module is very similar to those of the input and driver stages.

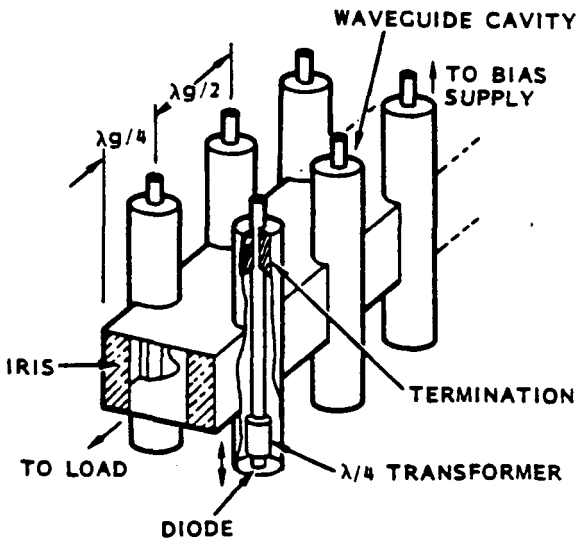


Figure 4-1. Basic configuration of waveguide cavity combiner

Figure 4-2(a) shows the construction of the diode module, which differs from the single-diode circuit in two respects. First, there is no quarter-wave choke in the bias port. Instead, a half-wave section (with air as the dielectric) is used before the bias port is terminated by lossy dielectric (Eccosorb MF124). This arrangement has the advantage that the half-wave section behaves as a series resonator at the resonant frequency, and is essentially a short circuit. The diode sees the load and the bias termination in series. Because the bias termination is designed to have a relatively low impedance, most of the RF power is delivered to the load.

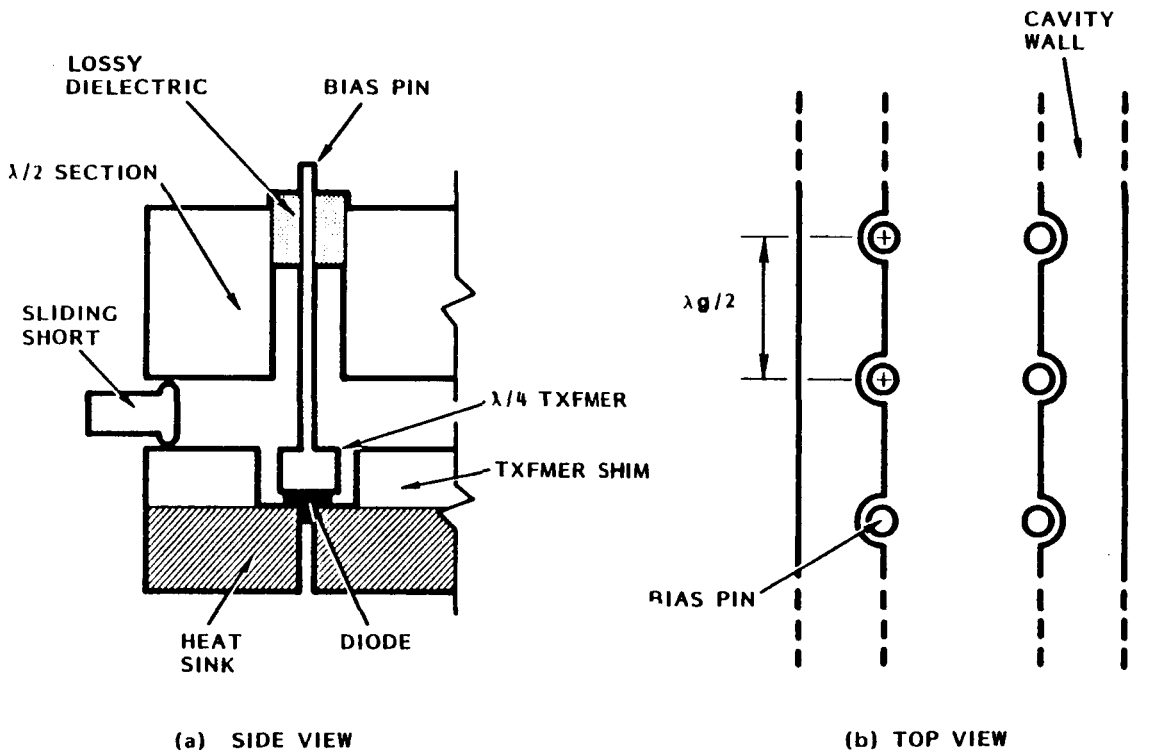


Figure 4-2. Construction of waveguide cavity combiner

Second, the diode modules are coupled to the waveguide from the sidewalls instead of from the center of the guide. This configuration has the advantage that two diode modules can be placed at the same cross section, thereby cutting the length of the cavity in half.

The actual construction of the combiner is shown in Figure 4-3. The individual components are readily identifiable and need no further elaboration. An assembled view of the combiner is shown in Figure 4-4. The measurement data of the unit are presented in Section 5.

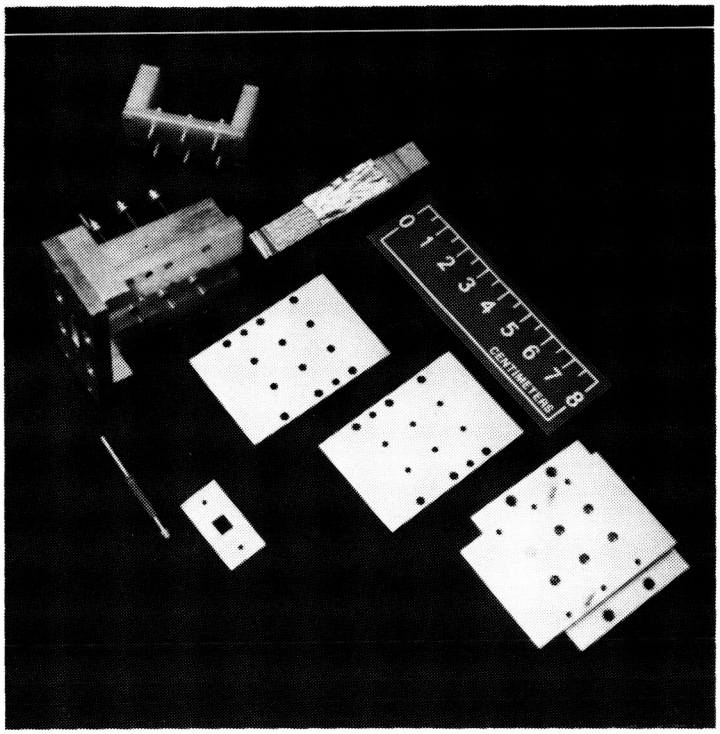


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Figure 4-3. Construction of combiner

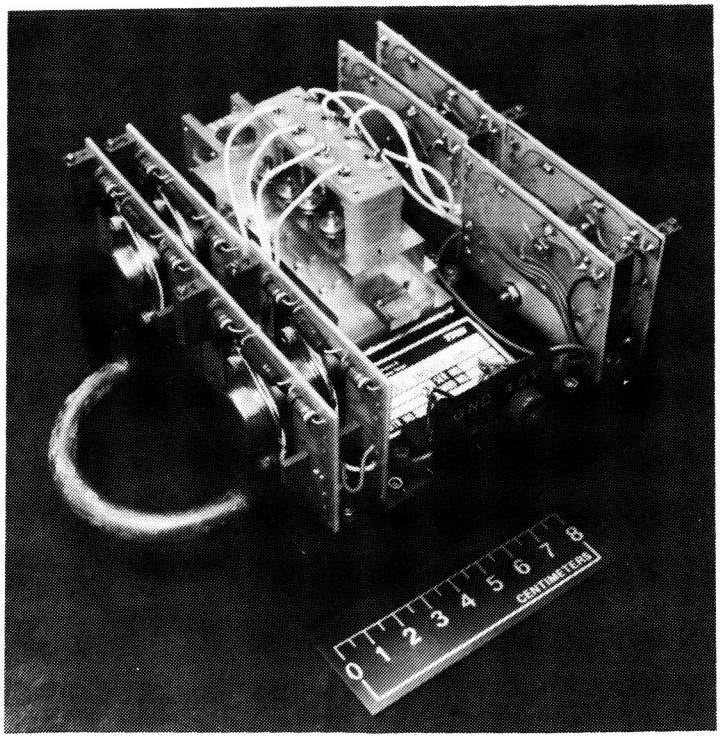

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Figure 4-4. Assembled view of 8-diode combiner

One design feature of the combiner, which is visible from Figure 4-4, is the bias pin assemblies. The contacts between the IMPATT diodes and the bias pins are very important. Large current, dc and RF, flows through each contact because it is within the low impedance region. Contacts with low ohmic loss are essential for the power performance of the combiner. To maintain a low loss contact, the bias pin must be pressed against the diode package by a large force. A nonconducting bridge (made of epoxy glass) holds the bellows used to provide this contact force. The round knobs are used as a micro-adjuster for the chokes, allowing for a much finer adjustment of the choke position.

The equivalent circuit of the output stage is shown in Figure 4-5. With the numerous resonators identified in the figure, the output stage can be classified as a multituned circuit. In actual operation, however, the combiner behaves as a single-tuned circuit because, in comparison, the Q of the resonant cavity is so much higher than those of the other resonators that the effects of the latter are almost diminished. This statement was confirmed by experiment that the free-running frequency of the combiner was varied by the adjustment of the waveguide short and the iris (two elements of the waveguide cavity) and, to a large extent, not varied by the alternation of the transformer shim or the half-wave sections. Consequently, the output stage suffers from relatively narrow operating bandwidth as with other single-tuned circuits. It was initially believed that by lowering the cavity Q to 25 and the stage gain to 8, the program objectives of a 20-W CW output and a 2-dB bandwidth of 500 MHz could be achieved. During the course of the development it was found that the wide dispersion of characteristics, in terms of output power and free-running oscillation frequency of the IMPATT diodes used, severely limits the power-bandwidth performance of the output stage. The mechanism behind this limitation process is shown in Appendix C. A high Q resonant circuit was required to compensate for the variations in diode impedances (due to package and diode chip variations) to achieve power combining. Since the Q of the circuit could not be increased without affecting the bandwidth, a compromise was made and both output power and bandwidth suffered.

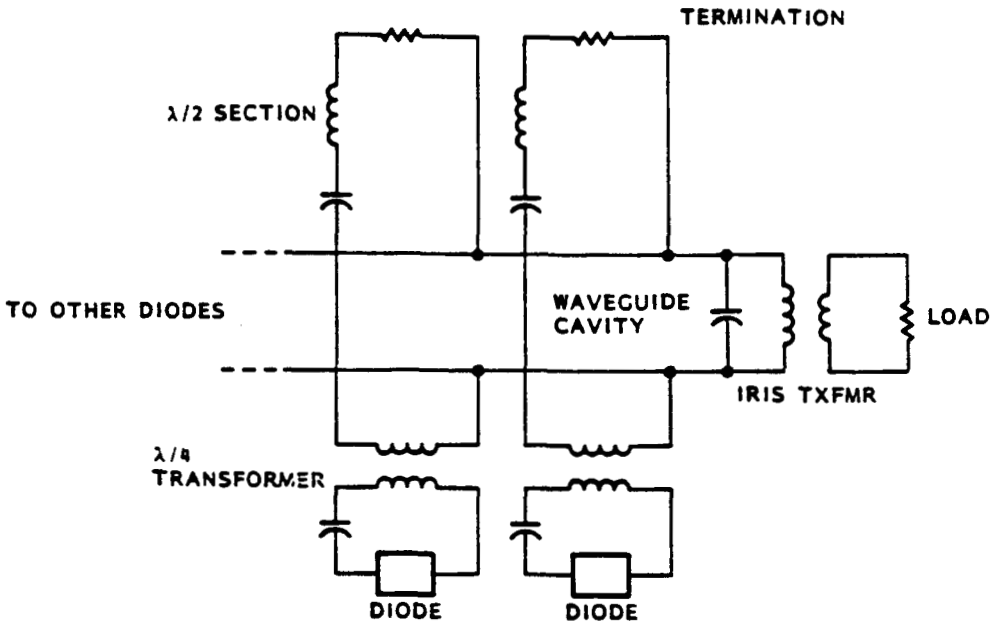


Figure 4-5. Equivalent circuit of waveguide cavity combiner

4.2 CIRCULATORS

One essential component found in most injection-locking oscillators or reflection amplifiers employing IMPATT diodes is the three-port circulator. The circulator decouples the input circuit from the output circuit and, in effect, transforms a one-port network into one with two ports. Since both the input and output signals are transmitted through the circulator, the electrical characteristics of the circulator have a profound influence on the overall circuit performance. The requirements imposed on the circulators are stringent. The circulators must be capable of handling the signal power and have a wide bandwidth (with low SWR) for proper circuit operation and an adequate isolation for input/output decoupling. Moreover, the circulators must have an extremely low insertion loss - in the vicinity of 0.1 dB - to prevent further degradation of the relatively poor efficiency of IMPATT devices. TRW has developed and patented such high performance circulators [11].

The development of high performance circulators was initiated at TRW in 1974. A market search had disclosed that even on special order, state-of-the-art circulators were totally inadequate for our purposes and an R&D effort was initiated to develop a low loss circulator at Ka-band. What appeared at that time as a technically ambitious task resulted not only in a device with performance characteristics far exceeding the original goals, but

also led to several significant advances in ferrite component technology. Among these were improvements in analytical design methods and a better understanding of ferrite material applications, resulting in a high degree of control over performance parameter, such as insertion loss, power capacity, and thermal stability. The improvements in structural design resulted in much higher reliability components which totally outperformed, under shock and vibration, the epoxy-bonded, triangular junction designs common to the industry.

Figure 4-6 depicts the simplified construction of a three-port junction circulator. The circulator consists of three TE_{10} rectangular waveguides which are 120 degrees apart and intercept to form a symmetric junction. A ferrite post is placed at the center of the junction. An external status magnetic field H_a is required to bias the ferrite post. Commercially available circulators employ ferrite posts with a triangular cross-section as shown in Figure 4-7(a). The triangular geometry was considered to have the potential of offering a wide circulator bandwidth; however, due to fabrication and mechanical alignment difficulties, the wideband potential was never practically realized. In fact, each triangular geometry circulator has to be individually tuned to meet the electrical requirements. TRW, on the other hand, adopted the cylindrical ferrite post as shown in Figure 4-7(b). It was found that the cylindrical geometry offers not only superior mechanical properties, but also electrical performance that equals or surpasses that of the triangular geometry. Individual tuning of the TRW circulator is not needed once the proper junction design is completed.

A detailed graphic representation of the TRW circulator junction is depicted in Figure 4-8. The junction consists of two ferrite discs, two dielectric spacers, a septum in the center of the cylinder dividing the junction into two turnstiles, and a dielectric tube enclosing the above parts.

The junction assembly is nested in metallic transformer discs, which are indexed precisely in the circulator housing formed by three intersecting waveguides. The operation of a junction circulator is best explained with the aid of Figures 4-9(a) and (b). Note that the symmetric junction formed by the waveguides behaves as a TM_{110} mode cylindrical cavity. When the external magnetic bias H_a is removed and the cavity is excited by the TE_{10} wave from one waveguide, the resulting TM_{110} field pattern is oriented in the

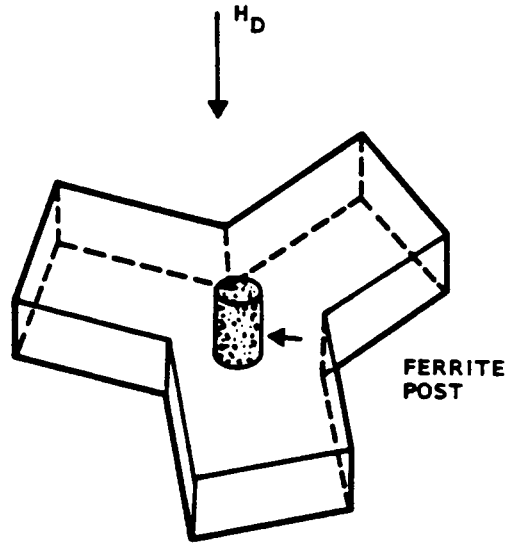
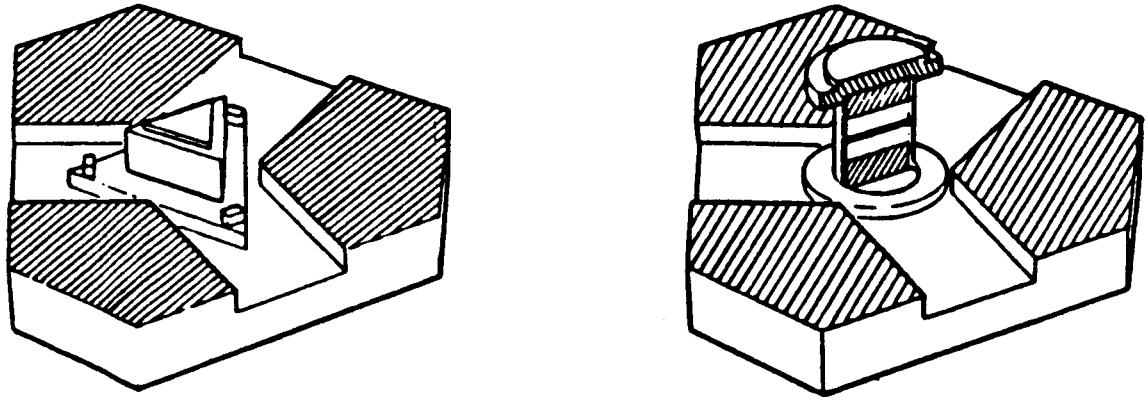


Figure 4-6. Simplified construction of 3-port circulator



a) TRIANGULAR GEOMETRY

- PARTS DIFFICULT TO FABRICATE AND INSPECT
- ASSEMBLY REQUIRES LOCATING FIXTURES, QUALITY CONTROL OF SIX EPOXIED INTERFACES, CURING OVEN
- ASSEMBLED CIRCULATOR REQUIRES POST-ASSEMBLY TUNING - NO TWO CIRULATORS ALIKE
- DIFFICULT TO QUALIFY UNDER SHOCK AND VIBRATION
- EXPENSIVE LOW RELIABILITY CIRCULATOR

b) CYCLINDRICAL GEOMETRY

- PARTS EASY TO FABRICATE AND INSPECT
- SIMPLE ASSEMBLY
- NO POST-ASSEMBLY TUNING, REPRODUCIBLE AND REPEATABLE
- CIRCULATOR SHOCK AND VIBRATION PROOF
- SIGNIFICANTLY LESS EXPENSIVE, HIGH RELIABILITY CIRCULATOR

Figure 4-7. Comparison of conventional triangular and TRW's cylindrical circulator junctions

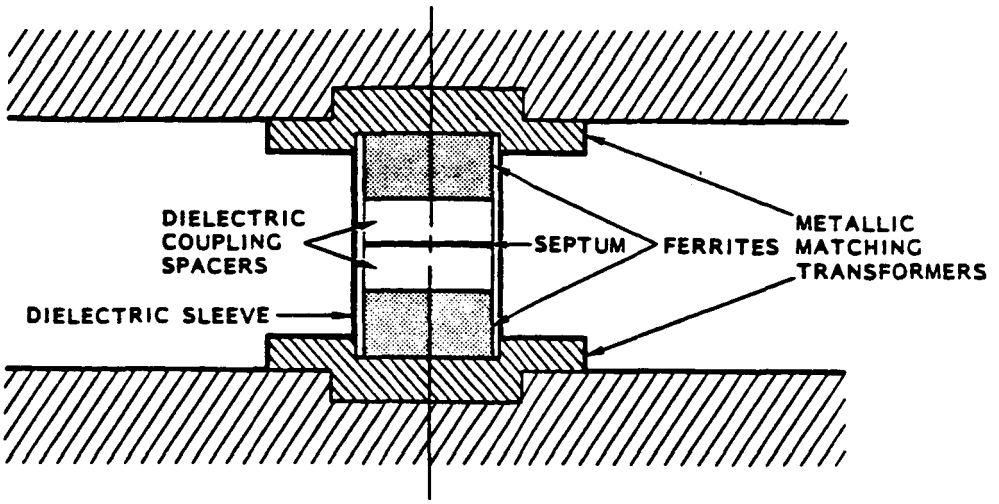
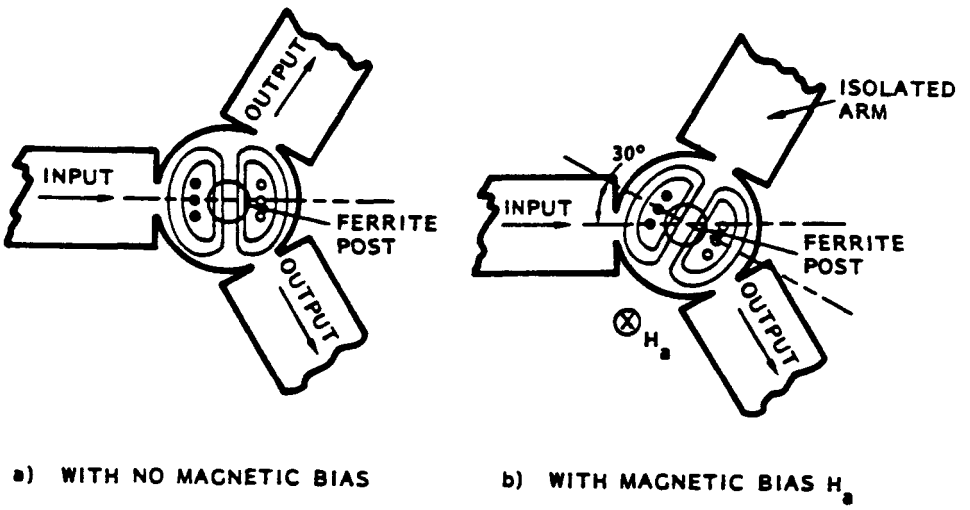


Figure 4-8. Graphic representation of TRW's circulator junction



a) WITH NO MAGNETIC BIAS b) WITH MAGNETIC BIAS H_a

Figure 4-9. Field pattern for H-plane waveguide circulator using TM_{110} mode

direction shown in Figure 4-9(a). The pattern orientation is identical to the one when no ferrite post is present. The ferrite post does not change the pattern orientation because in the absence of an external magnetic bias, the electromagnetic left and right polarized waves existing inside the ferrite have the same propagation constant. The two waves emerge from the ferrite in-phase and no rotation of the cavity field pattern takes place. As shown in Figure 4-9(a), the presence of electric and tangential magnetic fields at the waveguide-cavity interface allows excitation of TE_{10} waves in the two output waveguides.

When the external magnetic bias, H_a, is applied the situation is changed. The two polarized waves in the ferrite no longer have the same propagation constant, resulting in rotation of the mode pattern of the cavity by 30 degrees, as shown in Figure 4-9(a). The final outcome is that while one of the output waveguides stays unchanged, the remaining waveguide is isolated (i.e., no output). The cavity field pattern no longer has electrical and tangential magnetic fields at the waveguide-cavity interface to excite the TE_{10} wave in the isolated waveguide.

The bandwidth of a cylindrical circulator is related to its geometry by [12]

$$BW \quad 3.08 \left(\frac{R}{a}\right)^2 \frac{M_s}{1 - \frac{\gamma^2}{\omega_0^2} \left(H_o + \frac{M_s}{2}\right)^2} \qquad (4\text{-}1)$$

where R = radius of ferrite post

a = radius of cavity

γ = gyromagnetic ratio of the electron

ω_o = center frequency of the passband

H_o = external magnetic bias field,

M_s = ferrite saturation magnetization.

The upper limit on the circulator bandwidth is, of course, the single-mode bandwidth of the waveguides used.

Figure 4-10 indicates the electrical performance of a TRW K-band circulator. The upper curve represents the VSWR data and the lower curve, insertion loss data. It can be seen that for a VSWR of 1.2, the circulator has a passband from 18 to 23 GHz - a bandwidth of 5 GHz. The insertion loss in the passband is less than 0.2 dB. Tests have shown that the circulator also has an excellent thermal stability; a temperature variation from -21° to 51°C has little effect on the electrical performance.

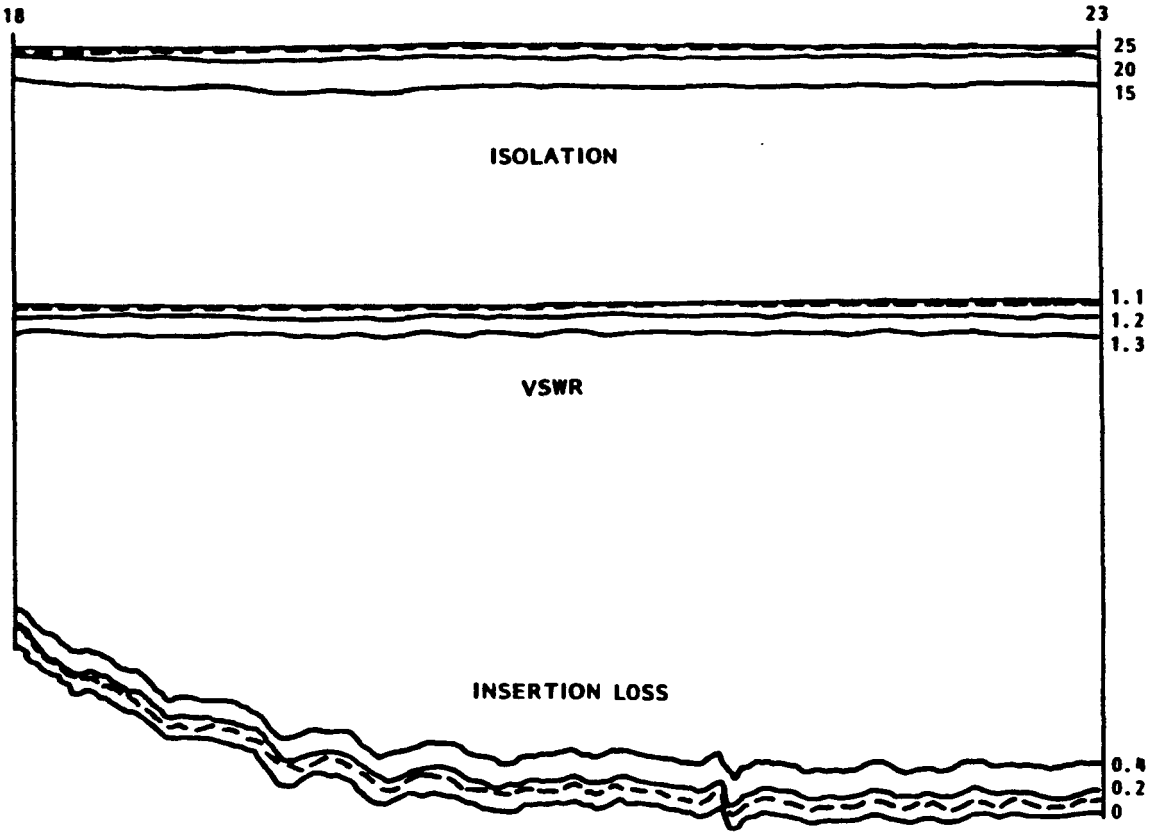


Figure 4-10. Electrical performance of 20-GHz circulator

4.3 CONSTANT VOLTAGE BIASING

It is well known that in the avalanche breakdown mode, the IMPATT diode behaves very much like a zener diode; that is, as far as the bias supply is concerned, the IMPATT diode acts as a constant voltage device; therefore, a constant current source has always been used without exception to bias an IMPATT diode. It has been reported [4] that an IMPATT diode operating in the amplifier mode has been successfully biased by a constant voltage source with encouraging results. The report claimed that by using constant voltage biasing, improved amplifier linearity and stability could be obtained while increasing the overall dc-to-RF conversion efficiency. Inspired by the finding, it was decided that constant voltage bias would be tried on the IMPATT amplifier operating in the injection-locked oscillator mode.

It appears that for a well-designed circuit, the IMPATT diode is stable with either constant current bias or constant voltage bias. Similarly, improvement of amplifier linearity was not observed since, in an objection locking mode, only the output frequency follows that of the input; the output

power remains more or less constant. One distinct advantage of this operational mode is that the amplifier offers a thermal property superior to when it was under constant current bias. For any reverse-biased semiconductor junctions, Si and GaAs included, the decreased ionization rate at high temperature gives rise to a positive temperature coefficient of breakdown voltage. A good approximation of the breakdown voltage-temperature relationship was found to be:

$$V_b(T_j) = V_b(T_o)\,[1 + \beta(T_j - T_o)] \tag{4-2}$$

where T_j is the junction temperature, T_o the reference temperature, $V_b(T_o)$ the breakdown voltage at T_o, and the normalized temperature coefficient defined by:

$$\beta = \frac{1}{V_b(T_o)} \quad \frac{dV_b(T_j)}{dT_j} \tag{4-3}$$

Rise of the junction temperature, T_j, is caused by external heating (due to rise of the ambient temperature) and internal heating (due to power dissipation in the diode).

When the device is operating under constant current bias, any increase in ambient temperature results in an increase of the junction temperature, as well as the increase in breakdown voltage. Consequently, power dissipation in the diode is increased, in turn causing the junction temperature to further elevate. This is the well-known thermal runaway phenomenon which can eventually lead to the destruction of the device.

If the device is operating under constant voltage bias, it can be shown (see Appendix B) that the junction temperature actually rises at a slower rate than the rise of the ambient temperature. This action results from the increase in diode breakdown voltage, according to equation (4-2), as external heating takes place. Since the diode voltage is kept constant, the diode current decreases. This is followed by a decrease in power dissipated in the diode and a decrease in junction temperature; hence, the device is prevented from thermal runaway. It was shown [5,6] that output RF power of an IMPATT diode is proportional to the square of diode current. The price for the thermal protection is a graceful degradation of output power with ambient

temperature elevation. Appendix B shows that the output power as a function of junction temperature can be expressed approximately as:

$$P_o = k(c_1^2 + d_1^2 \Delta T^2 - 2c_1 d_1 \Delta T) \tag{4-4}$$

where k, a, b are constants defined in Appendix A and $\Delta T = T - T_o$ is the relative ambient temperature. The output power decreases with temperature elevation at a rate equal to:

$$\frac{\Delta P_o}{\Delta T} = 2d_1^2 \Delta T - 2c_1 d_1 \tag{4-5}$$

The output power approaches zero as the temperature differential approaches a cutoff value defined as:

$$\Delta T_c = c_1/d_1 = \frac{V_d - V_b(T_o)}{\beta V_b(T_o)} \tag{4-6}$$

where V_d is the constant bias voltage. At relative temperature, which is equal to or above ΔT_c, the diode current is totally cut off.

In many applications in an extreme thermal environment, a graceful degradation in power with respect to temperature elevation is usually preferred over a catastrophic failure, such as a thermal runaway. It is well known that the failure rate of IMPATT diodes is directly related to the junction temperature and is described by the Arrhenius equation:

$$\lambda = \lambda_o \text{ EXP } (-E/kT) \tag{4-7}$$

where λ = failure rate, λ_o = a constant, E = activation energy, T = temperature, and K = Boltzmann's constant. For example, an increase of 28°C in junction temperature leads to a tenfold increase in failure rate. Similarly, if the junction temperature is cooler by 28°C, the failure rate drops tenfold. The advantage of constant voltage is obvious.

4.4 CONSTANT VOLTAGE BIASING REGULATORS

The bias circuit to be used in this program is essentially that of a voltage regulator (constant voltage source). One voltage regulator is needed

for each IMPATT diode. Due to their numerous applications, voltage regulators of various capacity and capability have been produced by the industry in integrated circuit (IC) form and are available in large quantities at low cost.

One regulator suitable for our application in the program is the LM150K, manufactured by the National Semiconductor Corporation. This regulator offers internal current limit, thermal overload protection, and safe-area protection to ensure high reliability. The internal circuitry of the regulator is provided in Figure 4-11. The circuit is quite complete. Only three external components, namely, potentiometer, resistor, and capacitor, are needed to connect the regulator as an adjustable constant voltage source (see Figure 5-25). The IC can operate in a temperature range of -55° to +150° C. Line regulation is typically 0.005 percent; load regulation typically 0.1 percent. The photograph of a complete regulator assembly is shown in Figure 4-12.

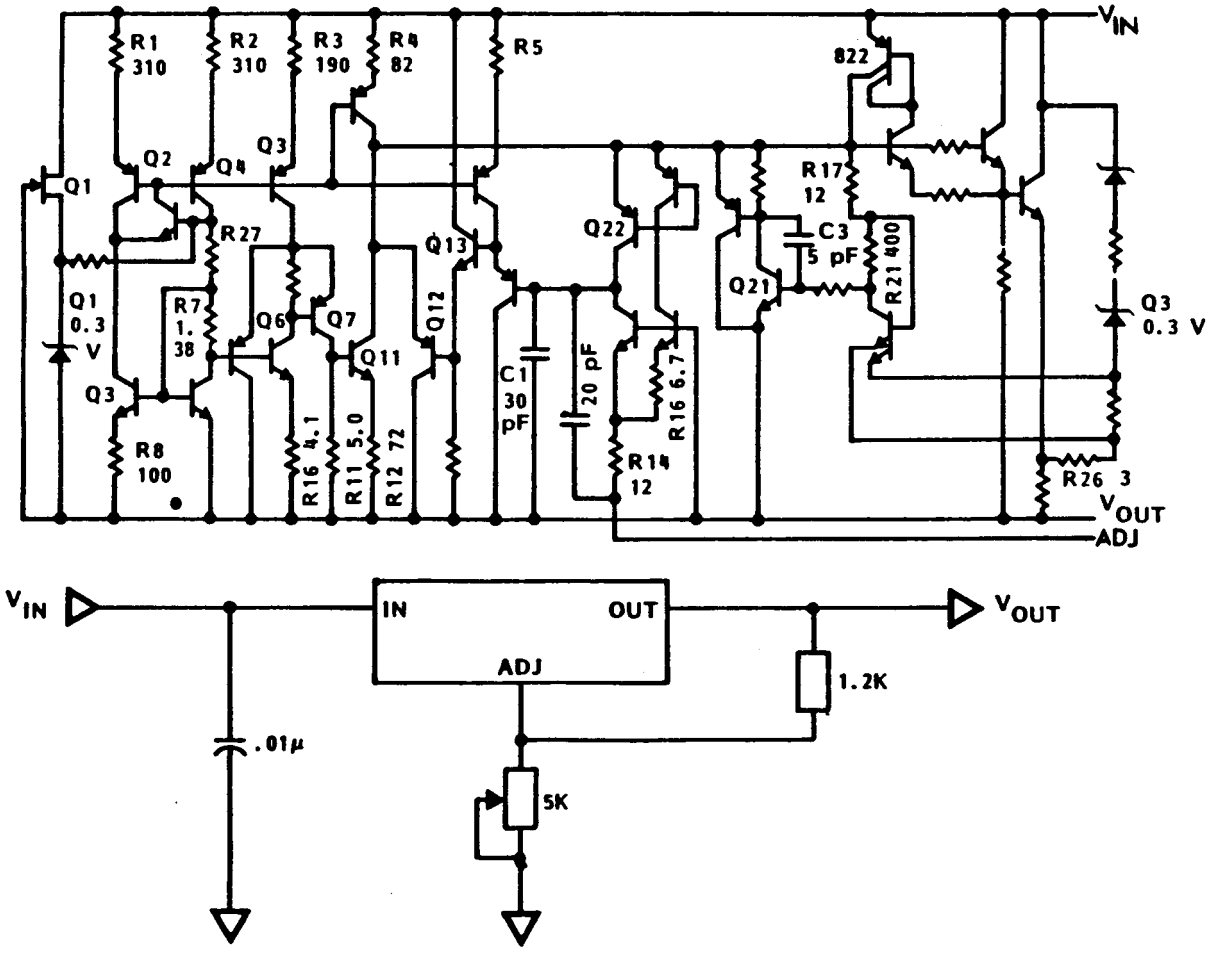


Figure 4-11. Bias regulator schematics

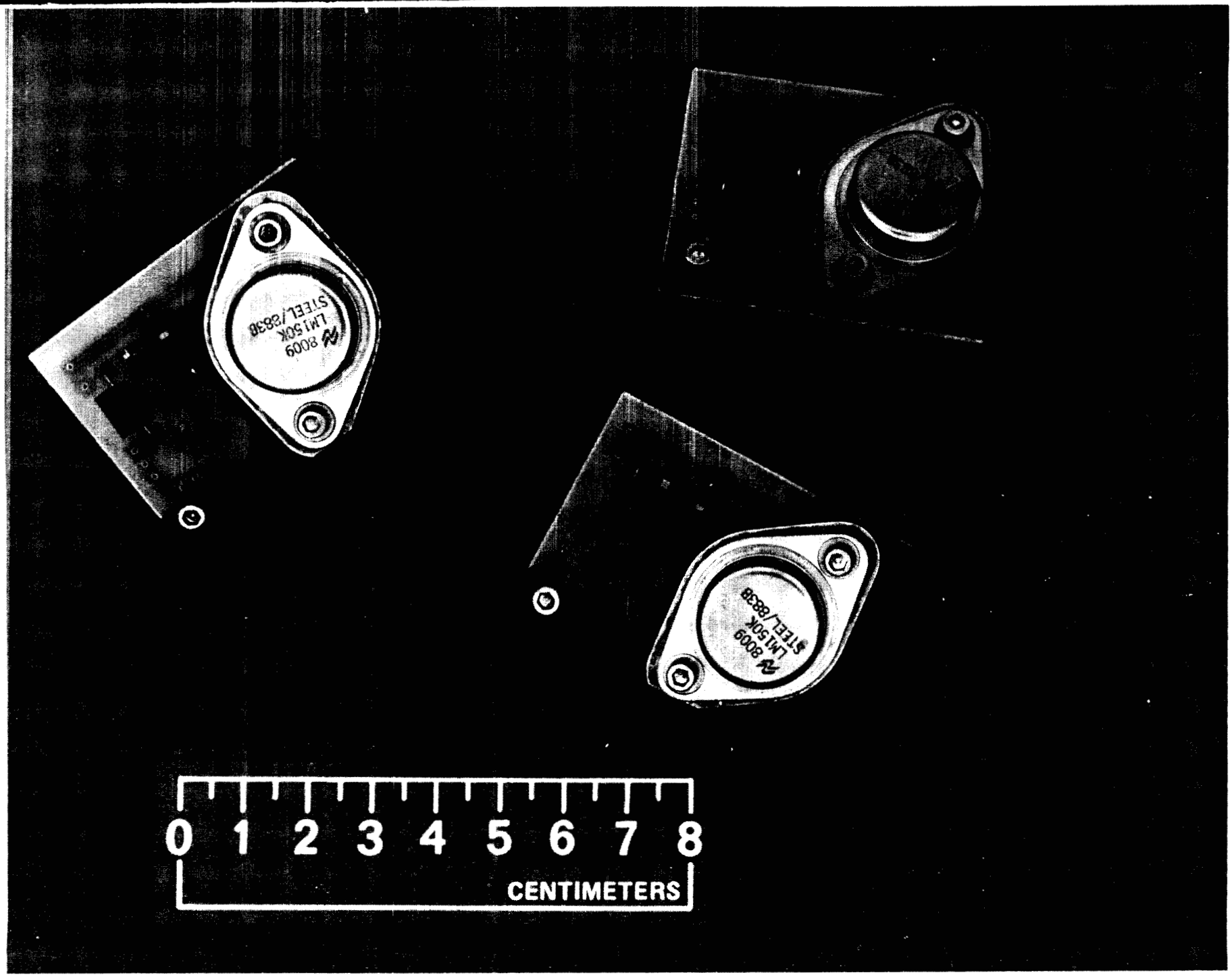


Figure 4-12. Regulator assemblies

5. AMPLIFIER PERFORMANCE EVALUATION

5.1 TEST OBJECTIVES

The test objectives were to determine the amplifier performance with respect to the parameters outlined in the contract. Amplifier testing consisted of the performance characteristic tests identified in Table 5-1.

Table 5-1. Performance tests

JUNCTION TEMPERATURE
EFFICIENCY
GAIN
BANDWIDTH
POWER OUTPUT

5.2 MEASUREMENT IDENTIFICATION

To adequately characterize the amplifier electrical performance, the four measurements required are listed in Table 5-2, in addition to the parameters which can be evaluated using data from the various measurements. As can be seen, the parameters in the table completely identify with the requirements listed in the table can be grouped into scalar or dc measurements.

Table 5-2. Amplifier/tests/measurements

TESTS/MEASUREMENTS	RESULTING DATA FOR EVALUATION
1. OUTPUT POWER VS INPUT POWER	OUTPUT POWER, GAIN
2. OUTPUT POWER VS FREQUENCY	BANDWIDTH, OUTPUT POWER, GAIN VARIATION
3. EFFICIENCY MEASUREMENT	AMPLIFIER DC-TO-RF CONVERSION EFFICIENCY
4. DIODE THERMAL RESISTANCE MEASUREMENT	THERMAL RESISTANCE, JUNCTION TEMPERATURE

5.3 TEST METHODOLOGY

Scalar RF Measurements

The measurements listed as 1 to 3 in Table 5-2 are termed scalar because only the power level and frequency information of the test signal can be obtained. The test setup (Figure 5-1) consists primarily of a variable frequency signal source, power monitor at the input port of the circuit under test, power monitor at the output port, and spectrum analyzer at the output port.

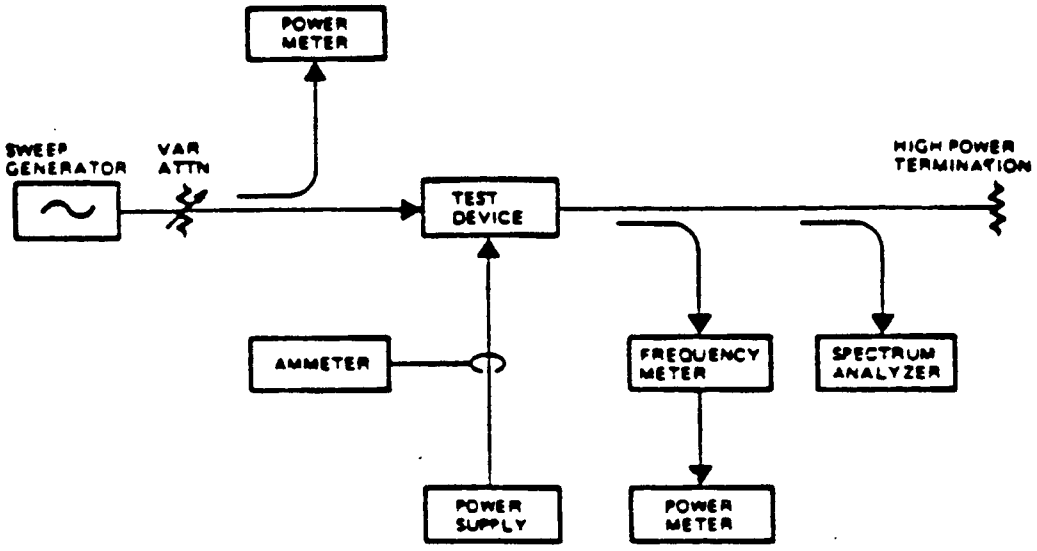


Figure 5-1. Scalar measurement setup

5.4 MEASUREMENT DATA EVALUATION

Output Power versus Frequency

The output power of the amplifier was measured against the RF frequency for four configurations during its development: a two-diode module, a four-diode module, a six-diode module, and an eight-diode module. The results of these measurements are shown in Figures 5-2 through 5-5, respectively. The power output of the eight-diode combiner within a bandwidth of 300 MHz (19 to 19.3 GHz) can be summarized as follows:

Power output = min. 6.2 W, max. 10.5 W

Power Gain versus Frequency

The amplifier gain versus frequency for the eight-diode combiner can be calculated from this data and is shown in Figure 5-6. From this data it can be seen that the gain varies as follows:

Power Gain = 2.9 dB min; 5.2 dB max

DC-to-RF Conversion Efficiency

The dc-to-RF conversion efficiency of the amplifier, excluding the bias regulators, can be found from the equation:

$$\eta_o = \frac{100\ (P_o - P_i)}{I_{d1}V_{d1} + I_{d2}V_{d2} + \ldots + I_{d8}V_{d8}} \qquad (5\text{-}1)$$

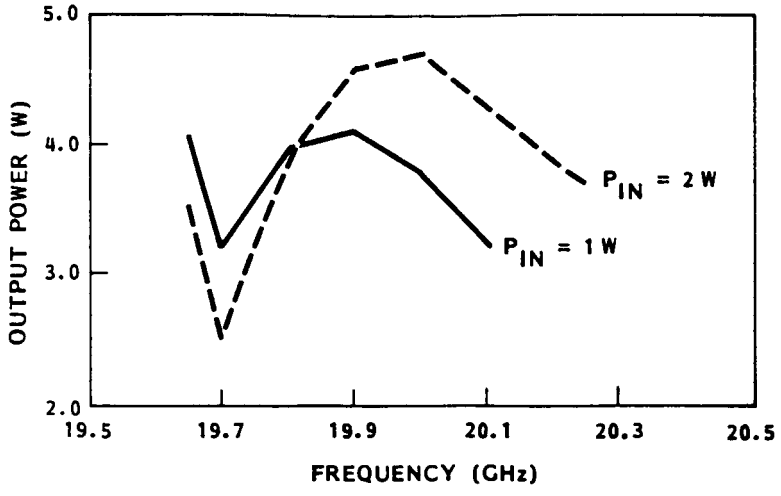


Figure 5-2. Two-diode module performance

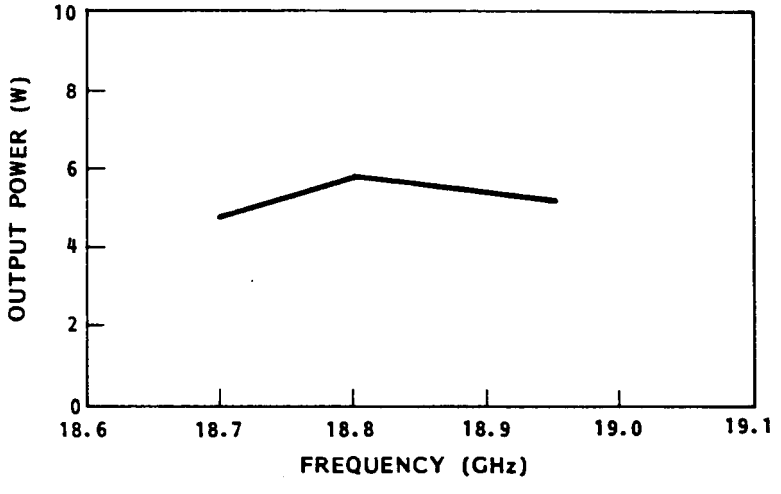


Figure 5-3. Four-diode module performance

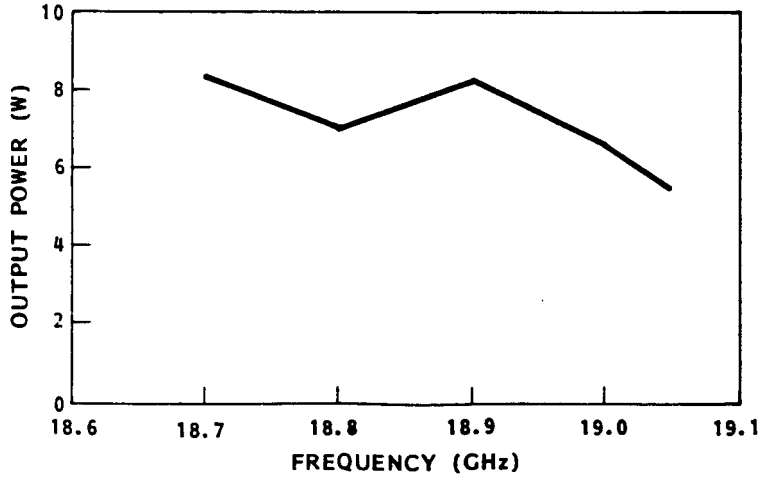


Figure 5-4. Six-diode module performance

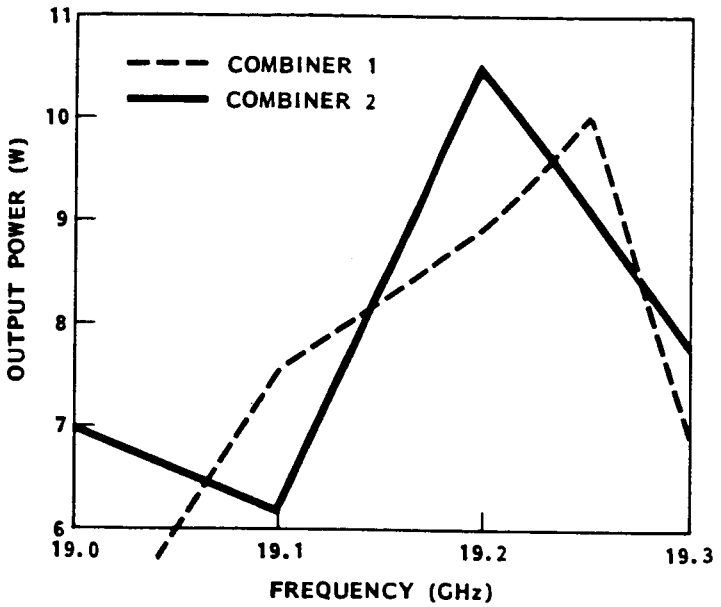


Figure 5-5. Eight-diode combiner performance

where P_o = RF output power
P_i = RF input power
I_d = IMPATT diode current
V_d = IMPATT diode voltage.

The overall dc-to-RF conversion efficiency of the amplifier, including the bias regulators, can be found from the equation:

$$\eta_T = \frac{100\ (P_o - P_i)}{I_T V_T} \qquad (5\text{-}2)$$

where I_T = EC supply current
V_T = DC supply voltage.

The following data were used for the efficiency calculations:

f	= 19.35 GHz	V_{D4}	= 36.4 V
P_i	= 3.16 W	I_{D4}	= 0.470 A
P_o	= 11.48 W	V_{D5}	= 35.6 V
V_T	= 42 V	I_{D5}	= 0.400 A
I_T	= 3.97 A	V_{D6}	= 38.5 V

V_{D1} = 36.4 V

I_{D1} = 0.500 A

V_{D2} = 36.2 V

I_{D2} = 0.540 A

V_{D3} = 32.7V

I_{D6} = 0.520 A

V_{D7} = 34.8 V

I_{D7} = 0.560 A

V_{D8} = 34.6 V

I_{D8} = 0.500 A

Upon calculations, the EC-to-RF conversion efficiencies are:

η_o = 5.9 percent (excluding bias regulators)

η_T = 5.0 percent (including bias regulators)

Diode Thermal Resistance Measurement

The thermal resistance of each diode was measured using the method outlined in Section 3.2. The diode junction temperature was calculated using the equation:

$$T_j = T_A + R_\theta \ (V_D I_D - Prf) \qquad (5\text{-}3)$$

where T_j = diode junction temperature

T_A = ambient temperature

R_θ = diode thermal resistance

V_D = diode voltage

I_D = diode current

Prf = RF power generated per diode.

From this equation the junction temperature of each diode was calculated for an ambient temperature of 20°C and is given in Table 5-3.

Table 5-3. Diode junction temperature

DIODE NO.	DIODE	V_B (V)	I_B (mA)	R_θ (°C/W)	T_j (°C)
1	DKR46Pt3	36.4	500	13.9	259
2	DKR46Pt4	36.2	540	13.2	264
3	DKR46Pt1	32.7	480	16.9	268
4	DKR46Pt2	36.4	470	15.6	271
5	DKR46E8	35.6	400	17.3	249
6	DKR46C5	38.5	520	11.7	242
7	DKR46Ex3	34.8	560	12.4	249
8	DKR46Ex6	34.6	500	13.6	241

6. CONCLUSIONS AND RECOMMENDATIONS

As a result of this program, TRW has successfully developed a 20-GHz double-drift GaAs IMPATT diode with a maximum observed CW oscillator output power of 5.3 W and dc-to-rf efficiency of 19 percent measured at the cavity output port. We have also developed the necessary millimeter-wave circuitry to combine eight 2-W GaAs IMPATT diodes in a Kurokawa power combiner producing close to 12 W of output power. These results represent a significant advance in the state-of-the-art in both device and power combiner circuit technologies in K-band frequencies.

Several areas warrant further development or improvement.

1. Although a maximum power output of 5.3 W has been measured, most of the diodes fall in the 2-W category. Additional work is necessary to improve the diode yield in the 4 to 5 W range. The wide variations in the breakdown voltage across the wafer (Figure 3-5) may be a fundamental problem associated with the extremely complex low-high-low doping profile of the double-drift Read diode. It may therefore be necessary to examine the factors governing MBE uniformity across the 3-inch wafer.

2) There is considerable variation in the device thermal resistance (Table 3-4). It is well known that the thermal resistance for silicon IMPATT diodes is highly dependent on the thermal compression bonding procedure as well as the precise thickness of the gold on the diamond heatsink. Because of the more brittle nature of GaAs material, these factors will undoubtedly magnify any imperfections in our bonding techniques and result in highly nonuniform thermal resistance from diode to diode. This will in turn contribute to large variations in output power and efficiency.

3) Because of the extremely low yield of 4 to 5-W diodes, it was not possible to achieve the desired 20-W output power. However, we believe that the basic circuit design is sound and only a minimum effort will be required to accomplish the desired output power once the diode yield is improved.

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APPENDIX A. THEORY OF WIDEBAND MULTITUNED CIRCUITS

The bandwidth of a tuned circuit is characterized by the rate of change of the circuit susceptance, B (or reactance, X), with the operating frequency, ω. In other words, the bandwidth is a function of the parameter $\partial B/\partial\omega$. A smaller value of $\partial B/\partial\omega$ implies a larger bandwidth. Since $\partial B/\partial\omega$ is related to the Q of the circuit, it can be said that a smaller circuit Q implies a larger operational bandwidth. For a single-tuned circuit, however, the circuit Q can not be lower without limit since some selectivity (frequency determination) must be maintained. The optimum solution in a single-tuned circuit is always a compromise between bandwidth and output power. Consequently, output power always drops at band edge in a single-tuned circuit. In the following paragraphs, it is shown that a multituned circuit, such as the double-tuned circuit used in the analysis, possesses a smaller $\partial B/\partial\omega$ compared with the single-tuned circuit, even if the individuals Q's in the former circuit are high.

A single RLC parallel circuit, as indicated in Figure A-1, derives the following:

$$Y_1(\omega) = \frac{1}{j\omega L_1} + j\omega C_1 + \frac{1}{R_1} = j\left(\omega C_1 - \frac{1}{\omega L_1}\right) + \frac{1}{R_1} = jB + G \qquad \text{(A-1)}$$

The rate of change of susceptance with frequency is found to be

$$\frac{B}{\partial\omega} = C_1 + \frac{1}{\omega^2 L_1} = \frac{Q_1}{\omega R_1} + \frac{Q_1}{\omega R_1} = \frac{2Q_1}{\omega R_1} \qquad \text{(A-2)}$$

where

$$Q_1 = \omega C_1 R_1 = \frac{1}{\omega L_1} \qquad \text{(A-3)}$$

Now, suppose a second resonator is added across the circuit as shown in Figure A-2, with the stipulation that its resonant frequency is the same as that of the first resonator. $Y_{IN}(\omega)$ then becomes

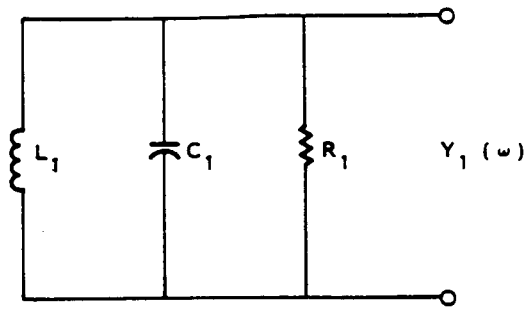

Figure A-1. Equivalent circuit for single resonator circuit

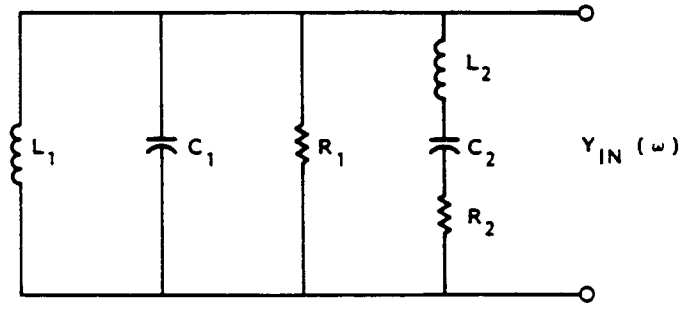

Figure A-2. Equivalent circuit of dual resonator circuit

$$Y_{IN}(\omega) = j\ \omega C_1 - \frac{1}{\omega L_1} + \frac{1}{R_1} + \frac{1}{R_2 + j\omega L_2 + \frac{1}{j\omega C_2}}$$

$$= j\left(\omega C_1 - \frac{1}{\omega L_1}\right) + \frac{1}{R_1} + \frac{R_2 - j\left(\omega L_2 - \frac{1}{C_2}\right)}{R_2^2 + \left(\omega L_2 - \frac{1}{C_2}\right)^2} \qquad \text{(A-4)}$$

Since

$$Y_{IN}(\omega) = G_{IN} + jB_{IN} \qquad \text{(A-5)}$$

we have

$$jB_{IN} = j\left(\omega C_1 - \frac{1}{\omega L_1}\right) - j\ \frac{\omega L_2 - \frac{1}{\omega C_2}}{R_2^2 + \left(\omega L_2 \frac{1}{C_2}\right)^2} \qquad \text{(A-6)}$$

Differentiating with respect to

$$\frac{\delta B_{IN}}{\delta \omega} = \frac{2Q_1}{\omega R_1} - \frac{\left[R_2^2 + \left(\omega L_2 - \frac{1}{\omega C_2}\right)^2\right]\left(L_2 + \frac{1}{\omega^2 C_2}\right) - \left(\omega L_2 - \frac{1}{\omega C_2}\right)\left(2\omega L_2^2 - \frac{2}{\omega^3 C_2^2}\right)}{\left[R_2^2 + \left(\omega L_2 - \frac{1}{\omega C_2}\right)^2\right]^2} \quad \text{(A-7)}$$

The first term was determined earlier for the case of the single-tuned circuit. In the second term, we substitute for L_2 and C_2 from the relation

$$Q_2 = \frac{\omega}{R_2} = \frac{1}{\omega C_2 R_2} \quad \text{(A-8)}$$

Then,

$$\frac{B_{IN}}{\delta \omega} = \frac{\delta Q_1}{\omega_{R_1}} - \frac{R_2^2\left(\frac{Q_2 R_2}{\omega} + \frac{Q_2 R_2}{\omega}\right) - 2\left(Q_2 R_2 - Q_2 R_2\right)\left(\omega L_2^2 - \frac{1}{\omega^3 C_2^2}\right)}{\left[R_2^2 + \left(Q_2 R_2 - Q_2 R_2\right)^2\right]^2} \quad \text{(A-9)}$$

The second term simplifies by inspection so that

$$\frac{\delta B_{IN}}{\delta \omega} = \frac{2Q_1}{\omega R_1} - \frac{2Q_2}{\omega R_2} \quad \text{(A-10)}$$

or

$$\frac{\delta B_{IN}}{\delta \omega} = \frac{2}{\omega}\left[\frac{Q_i}{R_1} - \frac{Q_2}{R_2}\right] = \frac{2Q_{equiv}}{R_{equiv}} \quad \text{(A-11)}$$

The significant conclusion, which is evident from this last equation, is that the rate of change of susceptance B with frequency, at least in the vicinity of the resonant frequency, is less for the combination of two circuits than for either circuit separately. This indicates a mutual susceptance compensation and broadbanding action. Allowing qualitatively the possibility of $R_1 = R_2$, we obtain a net Q_{equiv} of the combination circuit, which is the difference between the two individual Q's, and difference which could be small.

APPENDIX B. THEORY OF CONSTANT-VOLTAGE BIASING

Breakdown Voltage as a Function of Temperature

For any reverse-biased semiconductor junctions, Si and GaAs included, the decreased ionization rate at high temperature gives rise to a positive temperature coefficient of breakdown voltage. A good approximation of the breakdown voltage-temperature relationship was given as [14,15]:

$$V_b = V_{bo} (1 + \beta (T_j - T_o)) \tag{B-1}$$

where V_b is the device breakdown voltage at a junction temperature of T_j, V_{bo} is the same at a reference junction temperature of T_o, and β is the normalized temperature coefficient defined by

$$\beta = \frac{1}{V_{bo}} \frac{dV_b}{dT_j} \tag{B-2}$$

Notice that the rise of the junction temperature, T_j, is caused by external heating (due to rise of the ambient temperature) and internal heating (due to power dissipation in the diode). Consider first the effect of external heating. Equation (B-1) can be rewritten as:

$$V_b = V_{bo} + \Delta V_b \quad ; \quad \Delta V_b = \beta V_{bo} \Delta T \tag{B-3}$$

where $\Delta T = T - T_o$ is the relative ambient temperature in reference to T_o and T is the ambient temperature. Equation (B-3) states that a change in the ambient temperature in reference to T_o introduces a change in diode breakdown voltage, V_b, in reference to V_{bo}. We shall say that ΔV_b is caused by external heating.

When avalanche breakdown occurs, bias current flows through the device junction. In the case of an IMPATT diode, only a small fraction of the bias power is converted to the RF. The remaining bias power is dissipated at the junction as heat, and as a result, T_j rises. This process causes the voltage across the diode to increase above V_b in a fashion identical to external heating. We shall express the increase in diode voltage in analog to equation (B-3) and with the aid of a well-known heat equation:

$$\Delta V_{d1} = \beta V_{bo} \theta_t (V_d I_d + P_i - P_o) \tag{B-4}$$

where ΔV_{d1} is the increase in diode voltage above V due to the internal heating, θ_t is the thermal resistance from the diode junction to the ambience, V_d and I_d are the bias voltage and current, respectively, of the diode, P_1 is the RF injection power, and P_0 is the RF output power. Also, during avalanche breakdowns, the space charge of the carriers distorts the electric field profile in the space charge layer, giving rise to a positive electric resistance [16]. This, so-called, space-charge resistance produces a voltage drop across the diode in addition to ΔV_b and ΔV_{d1}. The voltage drop can be expressed as:

$$\Delta V_{d2} = R_{sc} I_d \tag{B-5}$$

where R_{sc} is the space-charge resistance of the diode and can be determined experimentally [14].

For the sake of closed-form solutions, we shall restrict ourselves to a first-order analysis in the next section by ignoring the terms involving P_i and P_0. (Notice that P_0 is a function of I_d^2.) The error so introduced is acceptable since only a small fraction of the bias power is converted to P_0. ΔV_{d1} is now expressed as:

$$\Delta V_{d1} \approx \beta V_{bo} \theta_t V_d I_d \tag{B-6}$$

The total voltage across an IMPATT diode under avalanche conditions can be written as:

$$V_d = V_{bo} + \Delta V_b + \Delta V_{d1} + \Delta V_{d2}$$

$$= V_{bo} + R_{sc} I_d + \beta V_{bo} \theta_t V_d I_d + \beta V_{bo} \Delta T \tag{B-7}$$

A plot of equation (B-7) is shown in Figure B-1.

Thermal Properties of C-I and C-V Biasings

With C-I biasing, $I_d = I_o$ = constant, and the diode voltage as a function of termperature, by rearranging equation (B-7), can be written as:

$$V = \frac{1}{1 - \beta \theta_t V_{bo} I_o} (R_{sc} I_o + V_{bo} + \beta V_{bo} \Delta T) = a_1 + b_1 \Delta T_1 \tag{B-8}$$

The junction temperature of the diode is found to be:

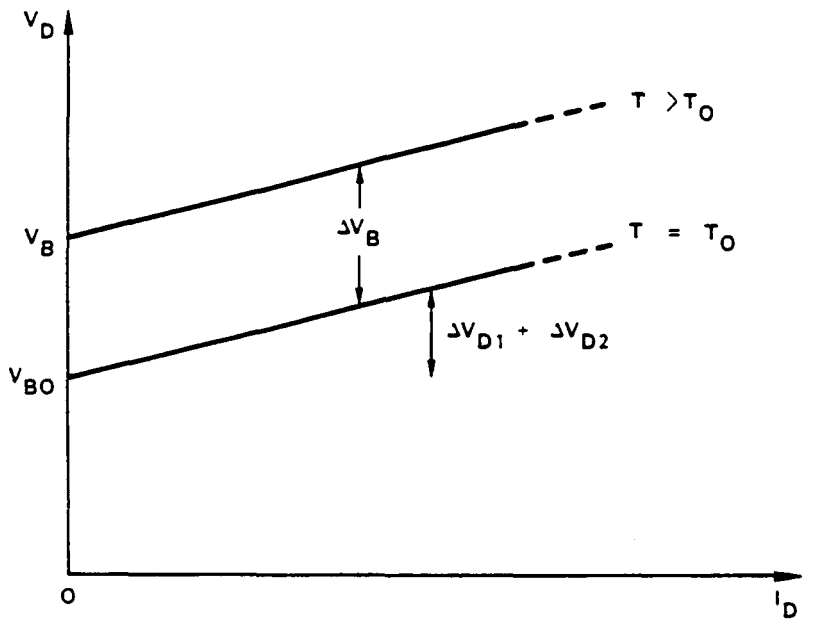

Figure B-1. Diode breakdown voltage characteristic

$$T_j = \theta_t I_o V_d + T$$

$$= \theta_t I_o (a_1 + b_1 \Delta T) + \Delta T + T_o \qquad \text{(B-9)}$$

$$= a_2 + b_2 \Delta T$$

For practical cases, the parameters a_1, a_2, b_1, b_2 are found to be positive. It is readily seen that with C-I biasing, both diode voltage and junction temperature rise with any temperatures above T_o (i.e., for $\Delta T > 0$) and there is a possibility of a thermal runaway due to internal heating if the condition $\beta\theta_t V_{bo} I_o = 1$ is met.

On the other hand, with C-V biasing, $V_d - V_o$ = constant, and the diode current and junction temperature can be shown to be

$$I_d = \frac{1}{R_{sc} + \beta\theta_t V_{bo} V_o} (V_o - V_{bo} - \beta V_{bo} \Delta T) \qquad \text{(B-10a)}$$

$$= c_1 - d_1 \Delta T \qquad \text{for } \Delta T \leq \Delta T_c \qquad \text{(B-10b)}$$

$$= 0 \qquad \text{for } \Delta T > \Delta T_c$$

$$T_j = \theta_t I_d V_o + T$$

$$= \theta_t V_o (c_1 - d_1 \Delta T) + \Delta T + T_o$$

$$= c_2 + d_2 T \qquad \text{for } \Delta T \leq \Delta T_c \qquad \text{(B-11a)}$$

$$= \Delta T \qquad \text{for } \Delta T > \Delta T_c \qquad \text{(B-11b)}$$

Again, the parameters c_1, c_2, d_1, d_2 are found to be positive for practical cases. A new parameter, T_c, which we shall call the cutoff temperature, is introduced here and is defined as

$$T_c - T_o = \Delta T_c = c_1/d_1 = \frac{V_o - V_{bo}}{\beta V_{bo}} \qquad \text{(B-12)}$$

Equation (B-10) indicates that diode current decreases with elevating temperature. As the ambient temperature reaches T_c, the diode current goes to zero and remains zero for any temperatures above T_c. On the other hand, the junction temperature increases with ambient temperature at a rate d_2. As the ambient temperature goes above T_c, the rate changes to unity. I_d and T_j under C-V bias are plotted against temperatures and are shown in Figures B-2 and B-3.

Comparison of C-I and C-V Biasing

Although T_j increases with temperature when the diode has either C-I bias or C-V bias, T_j increases with temperature at a slower rate in the C-V case than the C-I case, as can be seen from the following inequality.

$$b_2 = 1 + \frac{\beta\theta_t I_o V_{bo}}{1 - \beta\theta_t I_o V_{bo}} > d_2 = 1 - \frac{\beta\theta_t V_o V_{bo}}{R_{sc} + \beta\theta_t V_o V_{bo}}$$

The slower rate is due to the fact that with C-V biasing internal heating decreases with elevating temperature. Take a commercial IMPATT diode, HP 5082-0400, for example. The diode parameters were given as follows [17]:

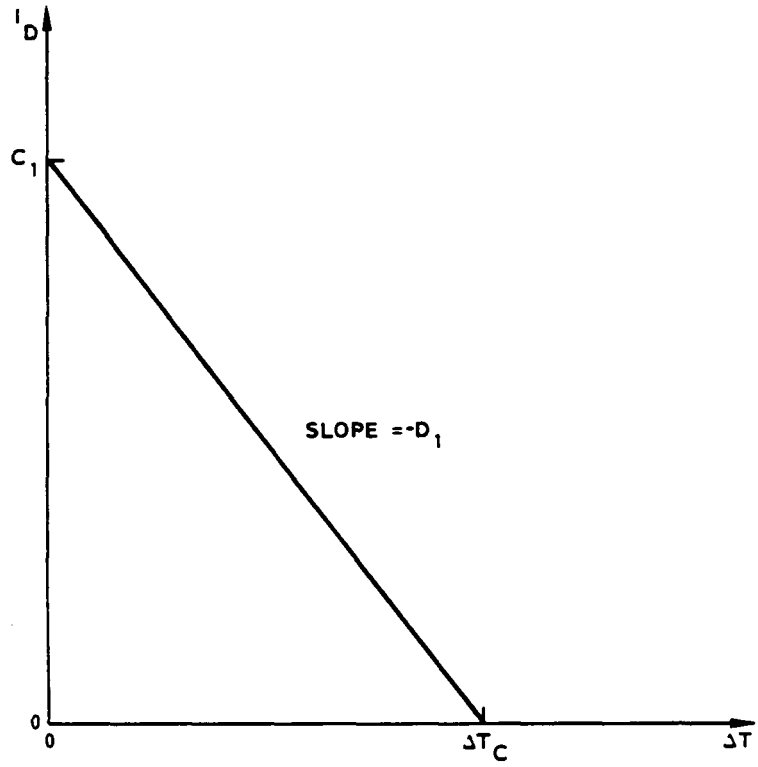

Figure B-2. Diode current vs temperature, C-V bias

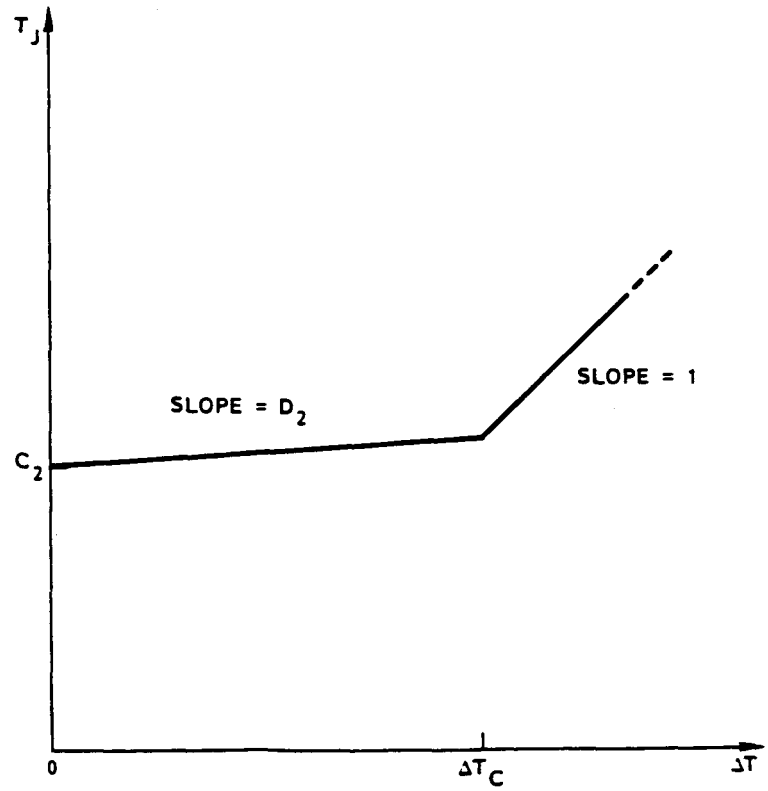

Figure B-3. Diode junction temperature vs temperature, C-V bias

$\beta = 1.17 \times 10^{-3}/°C$ $\quad V_{bo} = 76.1\ V$

$R_{sc} = 31$ ohms $\quad V_d = 83.6\ V$

$\theta_t = 16°\ C/W$ $\quad I_d = 0.05\ A$

If this diode were employed, we would have $b_2 = 1.08$ and $d_2 = 0.21$. The diode junction temperature would increase with temperature at a rate five times faster with a C-I bias than with a C-V bias. The price to pay for this thermal advantage is RF output. With C-V biasing, diode current decreases with temperature at the rate of d_1. Output power is proportional to the square of diode current or

$$P_o = k(C_1^2 + d_1^2 \Delta T^2 - 2C_1 d_1 \Delta T) \qquad \text{(B-14)}$$

where k is the constant of proportionality. Output power decreases, therefore, at the rate of

$$\frac{\Delta P_o}{\Delta T} = 2d_1^2 \Delta T - 2C_1 d_1 \qquad \text{(B-15)}$$

APPENDIX C. EFFECTS OF DIODE NONUNIFORMITY

It is important to examine the effects of IMPATT diode parameter dispersion on the performance of the IMPATT amplifier, since it is the amplifier which largely determines the overall performance of the communications system. A review of these effects is presented in which it is assumed that the most significant IMPATT diode parameter variation is the maximum power available from the diode. Initially, it has been assumed that this variation in power results principally from variations in the diode area. It is shown that the locking bandwidth and center frequency, as well as the output power, are sensitive to these variations.

In the following paragraphs, a simple equivalent circuit model of a single-diode injection-locking oscillator is discussed. (This will suffice for the purpose of illustrating the effect of diode nonuniformity.) Power output variations due to diode chip area variations are calculated. For simplicity, it is assumed that the oscillator has been adjusted initially for optimum performance using an average diode and that no changes in the oscillator coupling system are made to accommodate diodes of different chip areas. The effects of diode area changes on power, frequency, and bandwidths are then calculated. The results of the analysis have shown that the most significant influence of diode chip area variations is on the center frequency of the amplifier. To compensate for this, it will be necessary to individually tune each amplifier to the desired center frequency. The equivalent circuit of the injection-locked oscillator is shown in Figure C-1. Y_e is the electronic part of the diode chip admittance, C_d is the chip capacitance, C_c and L_c are the equivalent capacitance and inductance of the circuit referred to the chip plane, and R_s and G_L are the values of the bias stabilizing resistance and external load conductance referred to the chip plane. Typically, R_s, which is used to suppress subharmonic oscillations, and $1/G_c$, the equivalent circuit loss resistance are small compared to $1/G_L$. The effect of both terms, R_s and G_L, will be neglected to simplify the analysis.

Power Output Variations

The power output of an injection-locked amplifier operating in the free-running oscillator mode is given by

$$P_o = 1/2 \; | -G_e | V_1^2 = 1/2 \; G_L \; V_1^2 \qquad \text{(C-1)}$$

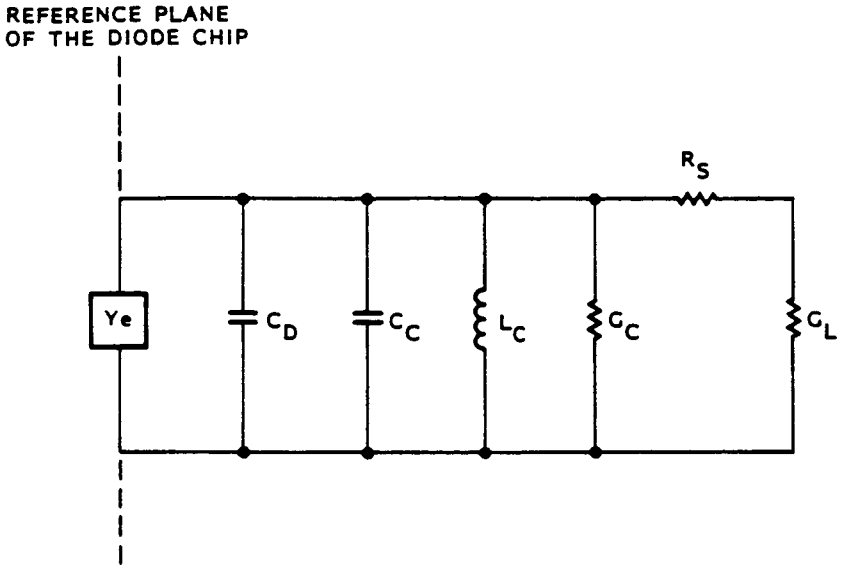

Figure C-1. Equivalent circuit of injection locked amplifier

where $-G_e$ is the negative electronic conductance of the diode chip and V_1 is the peak value of the ac chip voltage. For purposes of discussion, a diode with an optimum power of 2.5 W is assumed. It is further assumed that $(-)G_e = (-)20 \times 10^{-3}$ mhos and $V_1 = 15.8$ V under the conditions of optimum power output. It should be noted that the discussion which follows can be modified readily when the actual diode characteristics become available. Near the optimum power operating condition, G_e is assumed to vary as

$$G_e = G_s \left(1 - \frac{V_i^2}{V_m^2}\right) \tag{C-2}$$

where G_s is an equivalent small signal electronic conductance and V_m is defined so that when $V_1 = V_m$, $G_e = 0$ (i.e., $P_o = 0$). Solving for V_1^2 and substituting into the P_o equation, we have

$$P_o = \frac{G_L}{2} \left(1 - \frac{G_L}{G_s}\right) V_m^2 \tag{C-3}$$

In terms of the two diode parameters, G_s and V_m, the optimum power occurs when $G_L = G_{Lo} = G_s/2$. For this condition

$$V_1(\text{opt}) = \frac{V_m}{\sqrt{2}} \text{ (optimum chip voltage)} \tag{C-4}$$

and

$$P_{(opt)} = \frac{G_s V_m^2}{8} \quad \text{(optimum power output)} \tag{C-5}$$

For the diode assumed, $V_m = 22.34$ and $G_s = 40 \times 10^{-3}$ mhos. Thus

$$P_o = 249.5\ G_L - 6238.5\ G_L^2 \tag{C-6}$$

A plot of this equation near $G_{L(opt)}$ is given as the middle curve of Figure C-2.

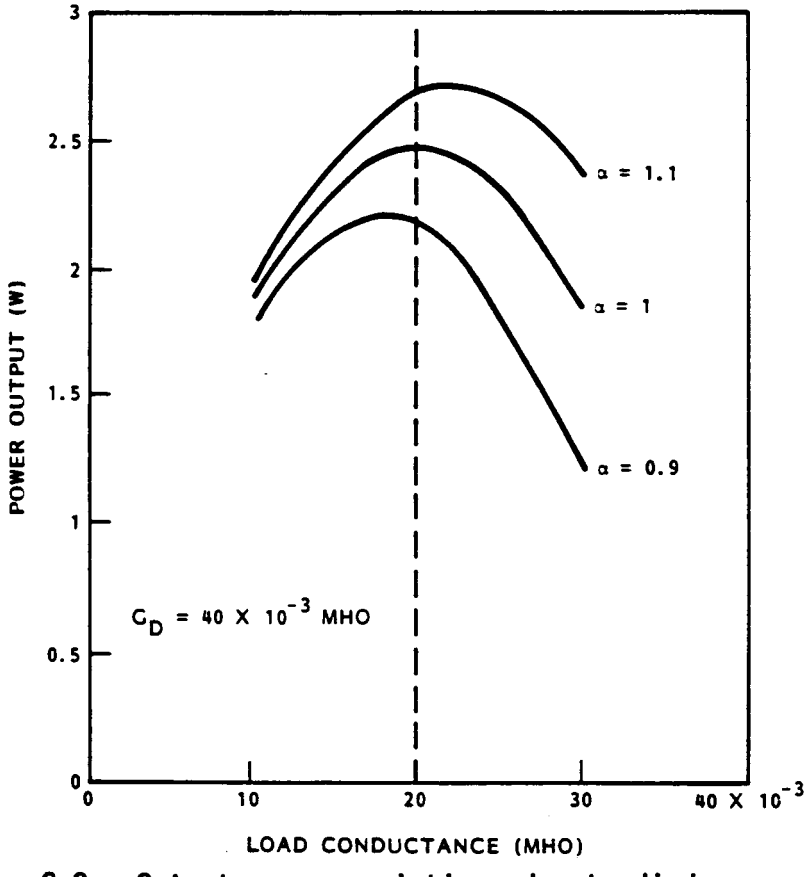

Figure C-2. Output power variations due to diode area variations

If the diode area varies by a factor α, then

$$P_o = 249.5\ G_L - \frac{6238.5}{\alpha}\ G_L^2 \tag{C-7}$$

It has been assumed that V_m remains unchanged, because only area variations are considered and that the new value of G_s is G_s.

Figure C-2 shows the effect of changes of from 1.1 to 0.9 (±10 percent change in area). It is seen that since the load conductance is assumed constant, the power varies about the nominal 2.5-W value from 2.2 to 2.7 W.

Oscillator Frequency Variations

The sensitivity of the oscillator frequency to changes in the diode area can be estimated from

$$\Delta f_o = -\frac{f_o}{2}\frac{\Delta_c}{c} \qquad \text{(C-9)}$$

where f_o is the change in f_o, the free-running oscillator frequency, Δc, is the change in capacitance of the diode, and c is the equivalent capacitance of the oscillator. It is estimated that the capacitance of the diode chip will be 1.3 pF and the effective capacitance of the oscillator will be 2 pF. Therefore, a 10 percent change in diode chip area will result in $\Delta c = \pm 0.13$ pF so that $\Delta f_o = 650$ MHz.

This calculation shows that the oscillator is very sensitive to changes in the diode capacitance. It is interesting to note that the amplifier design factors which produce large locking bandwidths will also increase the sensitivity to diode capacitance variations. It should also be noted that because of this sensitivity, it will be necessary to provide a frequency adjustment element in each oscillator to maintain a center frequency of about 20 GHz.

Locking Bandwidth Sensitivity

The external Q of the amplifier is given by

$$Q_x = \frac{\omega_o C}{G_L} \qquad \text{(C-10)}$$

where C is the effective capacitance of the oscillator, G_L is the load conductance as measured at the diode chip plane, and ω_o is 2 times the free-running frequency of the oscillator. Assuming, for the average diode, that $G_L = 20\times10^{-3}$ mho, $\omega_o = 2\pi \times 20 \times 10^9$ rads/sec, and $C = 2\times10^{-12}$F, Q_x is approximately 12.5. For a diode with 10 percent larger diode chip area, Q_x is 13.4, assuming all other design parameters are unchanged. For a 10 percent reduction in diode chip area, Q_x becomes 11.75.

The small-signal locking bandwidth of an oscillator is given by

$$f = \frac{f_0}{Q_x}\left(\frac{P_i}{P_0}\right)^{1/2} \qquad \text{(C-11)}$$

where f_0 is the center frequency

Q_x is the external Q

P_i is the locking power

P_0 is the output power.

Assuming that the nominal values of the amplifier P_i and P_0 are 0.25 and 2.5 W, respectively, the nominal locking bandwidth is, assuming Q_x 12.5, 505 MHz. For a 10 percent increase in diode chip area, accounting for the power variations and Q_x variations, the locking bandwidth is estimated to be 472 MHz, and for a 10 percent decrease, the estimated bandwidth is 538 MHz. These results are shown graphically in Figure C-3.

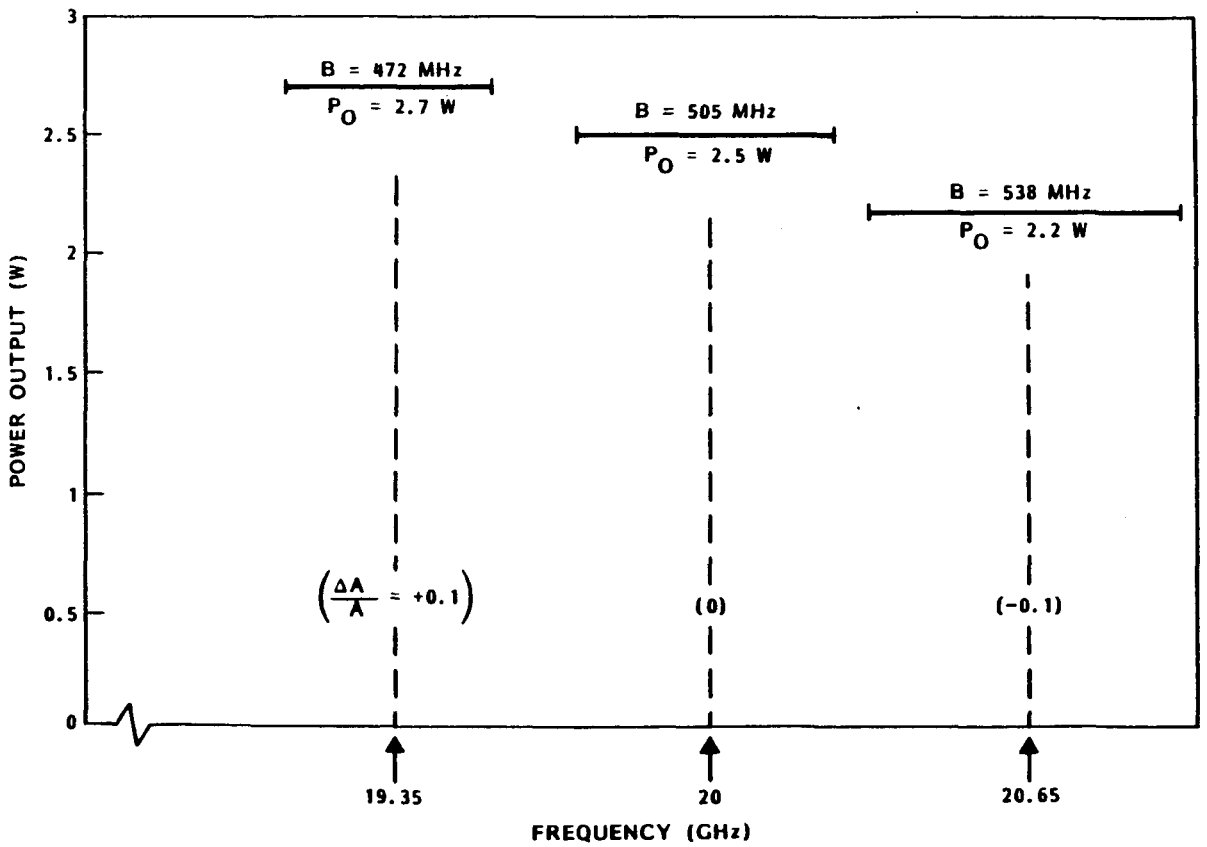

Figure C-3. Center-frequency and locking-bandwidth changes due to diode-area variation

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15. Supplementary Notes

NASA Project Manager: G. Chomos

16. Abstract

This report details the engineering development of a solid-state transmitter amplifier operating in the 20-GHz frequency range. The development effort involved a multitude of disciplines including IMPATT device development, circulator design, multiple-diode circuit design, and amplifier integration and test. The program objective was to develop a transmitter amplifier which would demonstrate the feasibility of providing an efficient, reliable, lightweight solid-state transmitter to be flown on a 30 to 20 GHz communication demonstration satellite. The work was performed under contract from NASA/Lewis Research Center for a period of three years.

The result of this effort was the development of a GaAs IMPATT diode amplifier capable of an 11-W CW output power and a 2-dB bandwidth of 300 MHz. GaAs IMPATT diodes incorporating diamond heatsink and double-Read doping profile capable of 5.3-W CW oscillator output power and 15.5% efficiency were developed. Up to 19% efficiency was also observed for an output power level of 4.4 W. High performance circulators with a 0.2 dB insertion loss and bandwidth of 5 GHz have also been developed. These represent a significant advance in the state-of-the-art in both device and power combiner circuit technologies in K-band frequencies.

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GaAs Double Drift IMPATT Diode, Kurokawa Multidiode Combiner, Injection Locking	Unclassified

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