PROCESSOR-CONTROLLED TIMING MODULE FOR LORAN-C RECEIVER*

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Hardware documentation is provided for the modified Loran-C timing module which uses direct software control in determining loop sample times. Computer loading is reduced by eliminating polled operation of the timing loop.

I. SUMMARY

The original design for the Ohio University Loran-C receiver featured a software/hardware locked-loop signal processor, based upon the Mostek 50395 timing integrated circuit (IC) [1,2]. This IC provides a six-digit binary-coded decimal (BCD) counter and a BCD register compared to generate an output pulse when the register and counter contents are equal. Operated at 1 MHz, this timing circuit permits microcomputer-selected sample times to be set precisely within a one-second counter interval, with a resolution of one microsecond.

In order to accomplish the data load for the IC register, the computer must detect that the IC digit scan oscillator has selected the appropriate 4-bit BCD digit, and then strobe the new digit data into the register. The IC design requires a scan oscillator frequency of no higher than 20 kHz, which places a lower limit on the time required to load all six digits. In practice, the complete register load required 500-800 microseconds (μs).

The original receiver design makes all six IC digit strobe signals available to the microcomputer, which then strobes the new digit data into the register after detecting the presence of the appropriate strobe signal. This operation must take place in order to preset the next loop sample time, triggered by the EQUAL pulse from the Mostek IC. Therefore, the register load must be performed between each Loran-C pulse. The technique of polling the digit strobe lines to detect the next digit to be loaded requires full attention from the microcomputer, delaying background processing.

The modified circuit described in this technical memorandum ignores digit strobes, by bringing the SCAN input under control of the processor. Register loading becomes a synchronous process, with no polling loop. When a digit datum is ready for loading, the scan counter is updated immediately by the processor, with no lost time. See figure 1 for a block diagram.

This modification is required to permit the single processor (a MOS Technology 6502) to perform all required computations for the entire Loran-C process. Expansion of the receiver from a three-station tracker to full five-station operation would cause over 20 percent of processor power to be lost to the strobe polling operation, causing a reduction in navigation data output rates, and a reduction in the number of pilot-oriented features which could be added using the single processor. This modified circuit saves some 350 to 650 μs per Loran pulse.

Full hardware documentation is provided in this paper for the circuit card implementing the Loran-C timing loop, and the receiver event-mark and re-track functions. This documentation is to be combined with overall receiver drawings to form the as-built record for this device. Computer software to support this module is integrated with the remainder of the receiver software, in the LORPROM program.

II. CIRCUIT DESCRIPTION

Figure 2 shows the complete logic diagram for the Loran-C timing module. To the far left are signal descriptors for the system computer, an MAI SuperJolt based upon the MOS Technology 6502 with 6520 peripheral interface adapter (PIA). All connections, except for CLOCK and IRQ, are made through the 6520 PIA. Figure 3 gives a summary of PIA pin assignments, useful in software design and coding. The Mostek 50395 chip description is given as figure 4, and pinouts are shown in figure 5.

Referring to figure 2, note that seven lines provide data and control signals to the Mostek IC (U3). All these signals are output by the computer as TTL-compatible signals, and must be changed to the 12-volt MOS specification required by U3. This conversion is performed in open-collector drivers U1 and U2, pulled up to 12v through 1.1 K-ohm resist~ These lines carry the four data bits for register digits Ra, Rb, R the LR (Load Register) strobe and $\overline{SET}$ (Set digit counter to most-significant digit) signals.

The timing chip U3 is wired for free-running counter, counting up is driven by the CLOCK, which is a buffered version of the main microcomputer clock (a temperature-compensated crystal oscillator). The SCAN inp which increments the digit counter to indicate the load window for each register digit is driven by the computer via the SCAN line.

The computer is programmed to select ($\overline{SET}$) the high order digit first, and to set LR to enable the register load digit at a time. Each digit is then placed on RA through RD, and loaded by toggling SCAN.

Once the register is fully loaded, the U5 Loran-C interrupt and data latches are enabled by bringing $\overline{CLRP}$ high. When the free running counter in U3 reaches the register value just loaded, U3 issues an EQUAL pulse for one clock period (one μs) which clocks the U5 latches. The IRQ low since the $\overline{Q}$ output of the U5 interrupt latch always goes low upon clocking. An interrupt is signaled at $\overline{IRQ}$ to the computer. LDAT, latched by the U5 Loran-C latch, assumes the instantaneous value of the Loran-C digital waveform received at $\overline{LRIN}$ from the receiver front-end module. Note that $\overline{LRIN}$ is processed by U4 to set a pulse width of approximately 70 μs before it is sampled. This pulse width is necessary to provide a guard time after the leading pulse edge to permit successful pulse tracking, and to minimize initial search time. Since the various front-end processors designed to date have presented various pulse widths, this U4 mono-stable multivibrator has been provided to equalize the waveform before sampling.

The remainder of the circuit, U12, deals with receiver features included for evaluation. The event latch is driven by a front-panel pushbutton to place on the receiver output tape a unique mark so output data may be correlated with flight events. The retrack latch, also operated by pushbutton, signals the computer that the operator wishes to restart the Loran-C search process. To minimize contact bounce, these latches are configured to operate on the pushbutton release cycle.

Once the computer program has serviced the Loran-C sample interrupt thus generated, the U5 latches are disabled by a low at $\overline{CLRP}$. Another register load sequence begins.

In this manner, successive samples may be taken of the Loran-C input waveform at times which are precisely controlled by the microcomputer. The programmer may now select algorithms for detecting received Loran-C chains and stations by varying the sample time and observing the result at LDAT.

The module pictorial appears in figure 6, giving placement of ICs and other major components.

III. REFERENCES

[1] Lilley, R. W. and D. L. McCall, "A Loran-C Prototype Navigation Receiver for General Aviation," paper (No. 81-2329), presented at the AIAA/IEE Fourth Digital Avionics Systems Conference, November 1981.

[2] Lilley, R. W. and D. L. McCall, "A Loran-C Prototype Navigation Receiver for General Aviation," Technical Memorandum 80, Avionics Engineering Center, Department of Electrical and Computer Engineering, Ohio University, August 1981.

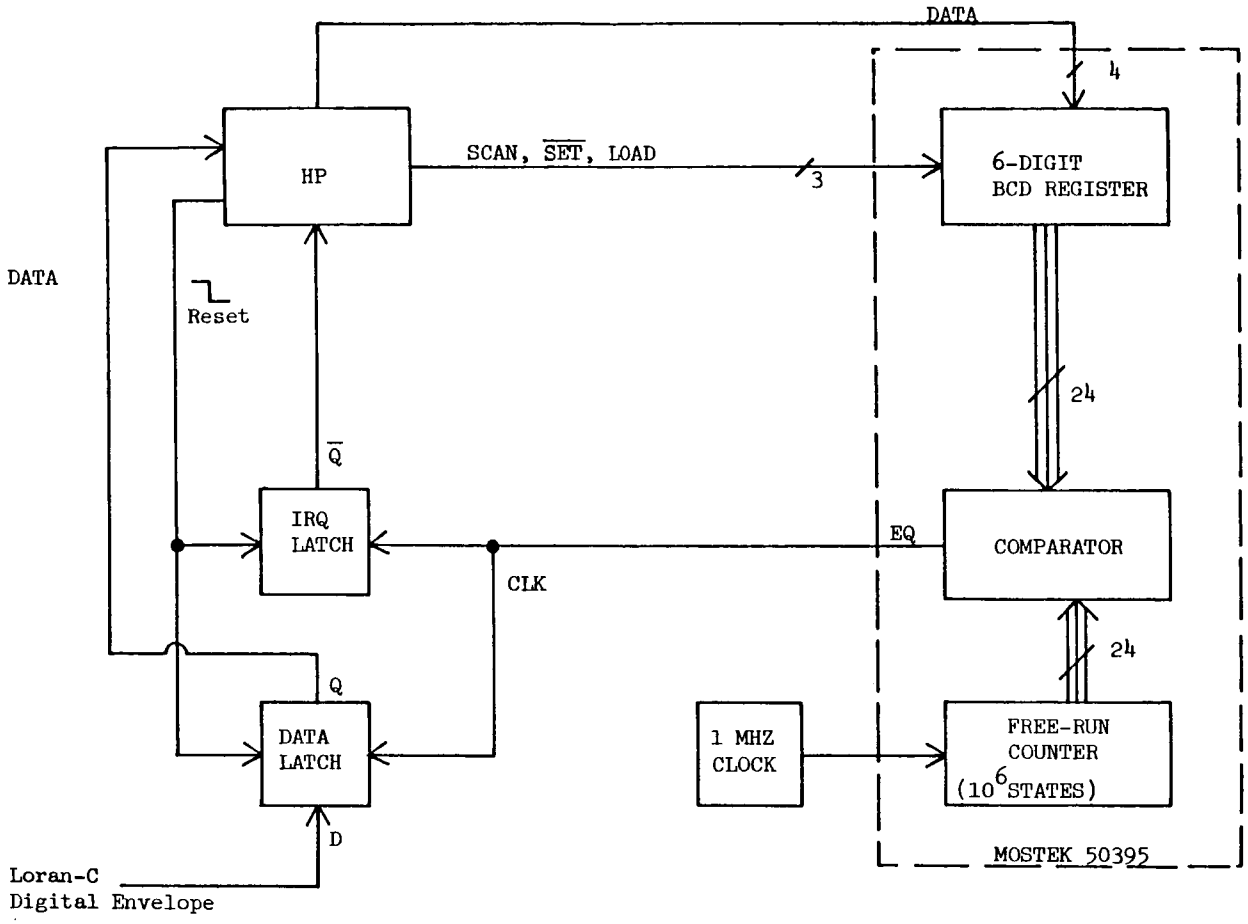


Figure 1. Block diagram, Loran-C timing module.

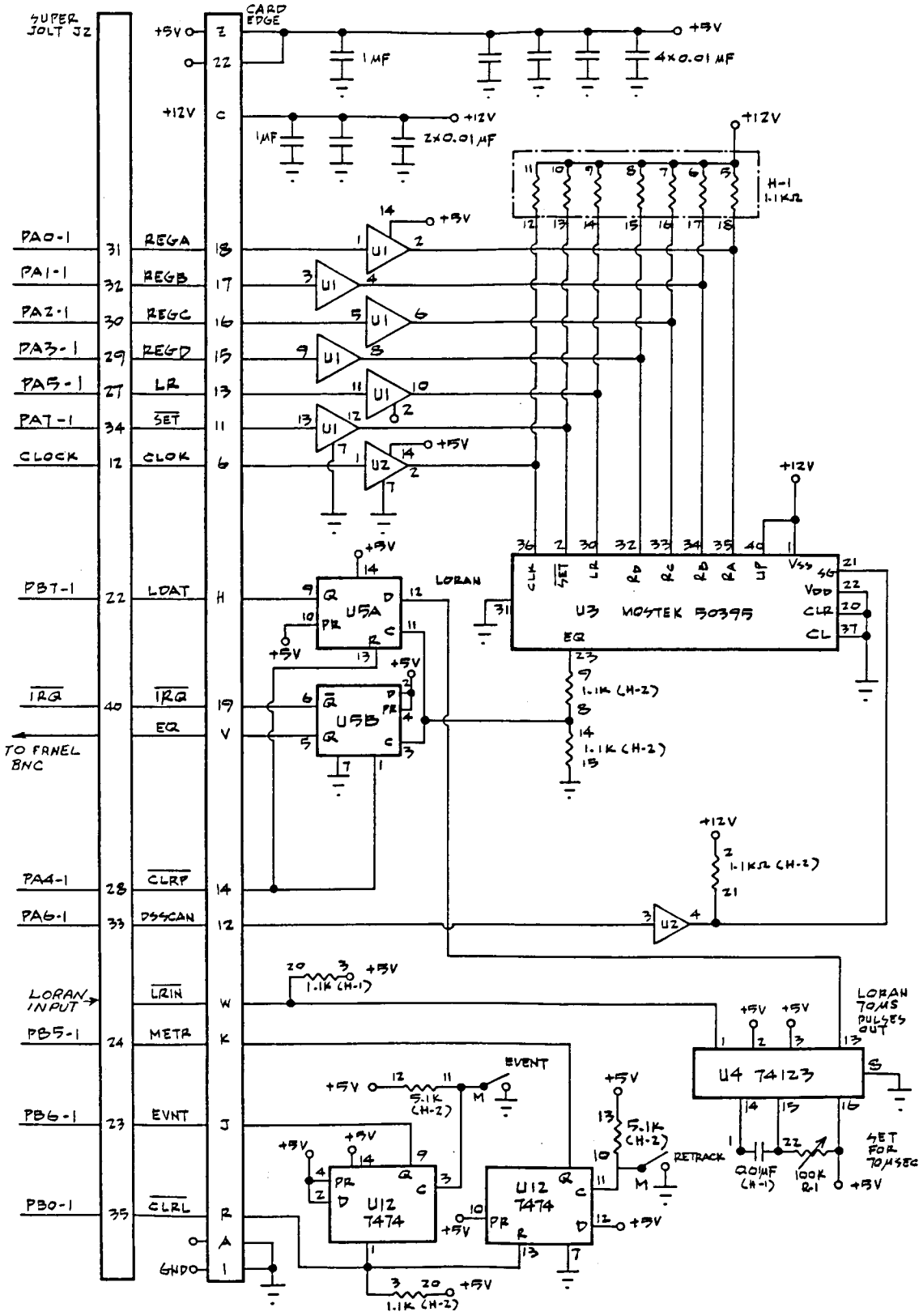


Figure 2. Revised timing board schematic.

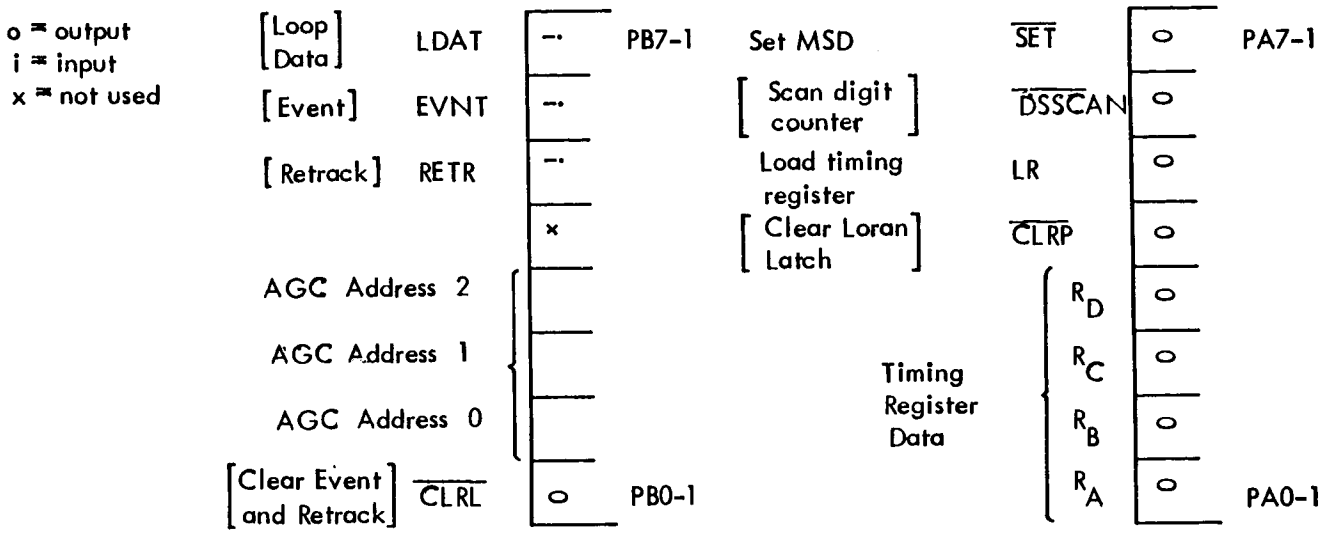


Figure 3. Super Jolt to timing board summary of PIA assignments.

FUNCTIONAL DIAGRAM

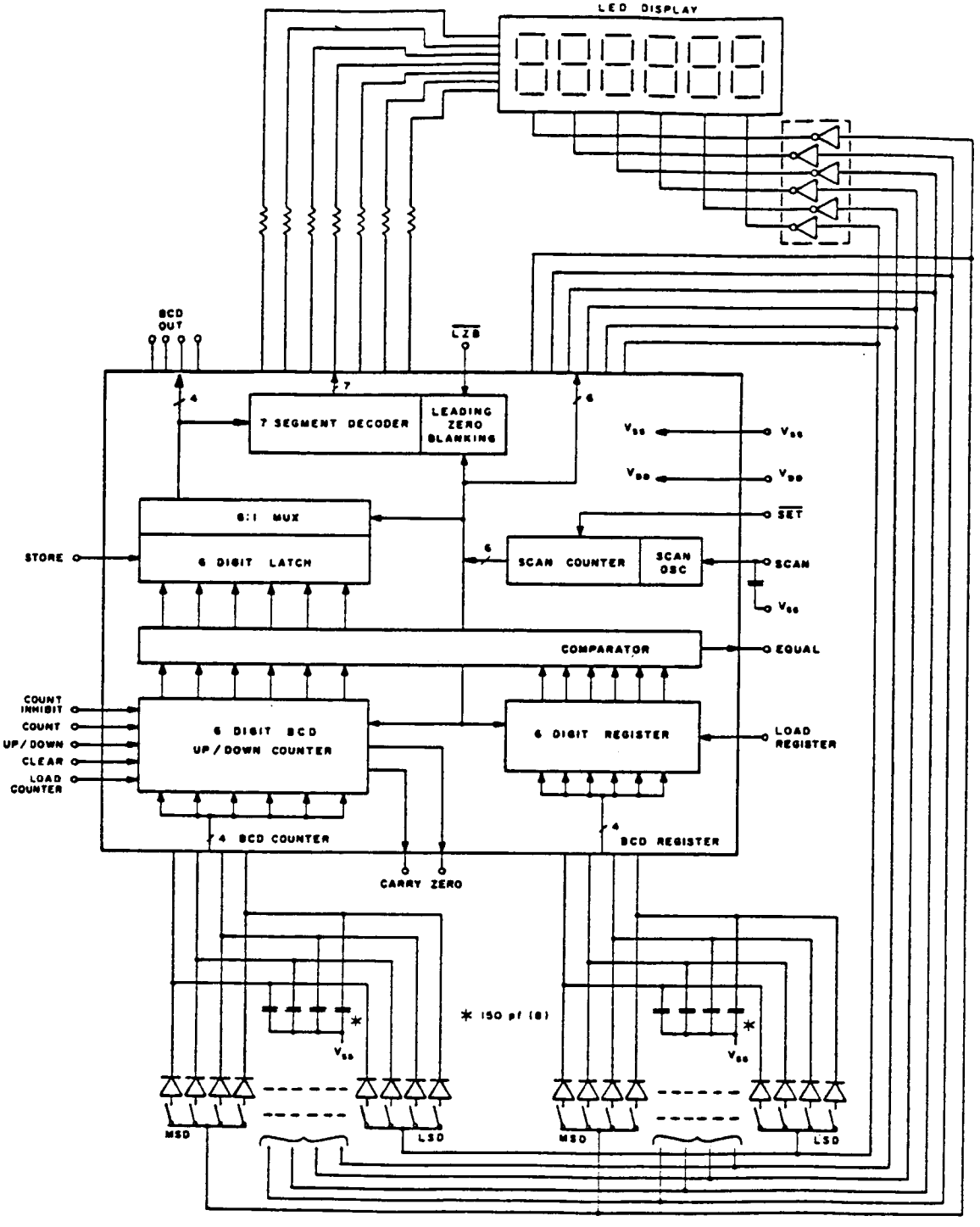


Figure 4. MOSTEK 50395 integrated circuit.

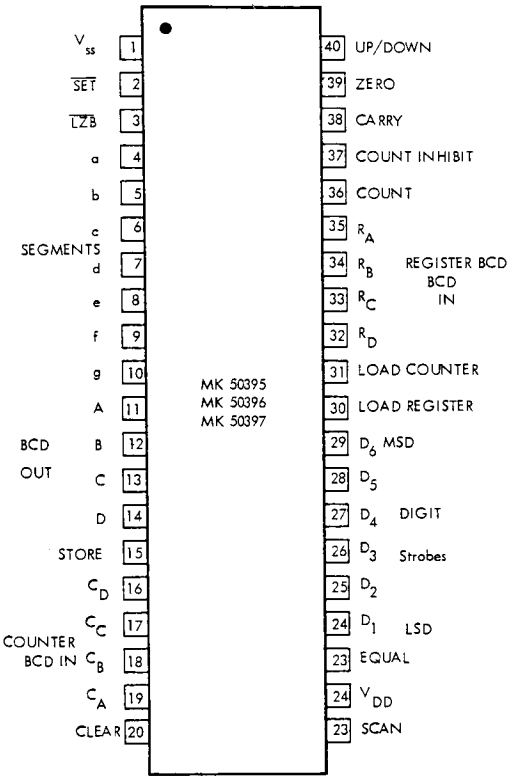
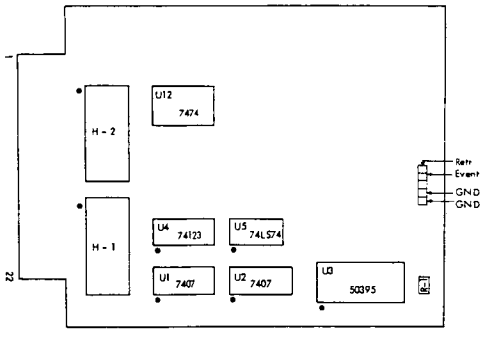


Figure 5. MOSTEK 50395 pinouts.



Pin	Signal	Description
R	$\overline{CLRL}$	Low clears retrack & event latches.
J	EVNT	High indicates user event mark, cleared by $\overline{CLRL}$.
K	RETR	High indicates user retrack, cleared by $\overline{CLRL}$.
W	$\overline{LRIN}$	Input Loran-C pulses from front-end. TTL, open-collector, pulled up to 5V on this board
18	REGA	4-bit BCD digit load for U3 register.
17	REGB	
16	REGC	
15	REGD	
13	LR	Load 50395 (U3) Register strobe.
11	$\overline{SET}$	Set U3 to MSD for data load.
6	CLOK	1 MHz clock, from microcomputer.
12	DSSCAN	Scan Input for Digit Counter
14	$\overline{CLRP}$	Low clears Loran data latch.
H	LDAT	Loran data - loop sample output.
19	$\overline{IRQC}$	Combined IRQ from loop and digit strobes.
V	EQ	Equal pulse, for monitoring.

Figure 6. Pictorial and signal glossary.