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Synchronization Trigger Control System for Flow Visualization

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ABSTRACT

The use of cinematography or holographic interferometry for dynamic flow visualization in an internal combustion engine requires a control device that globally synchronizes camera and light source timing at a predefined shaft encoder angle. The device is capable of 0.35° resolution for rotational speeds of up to 73 240 rpm. This was achieved by implementing the shaft encoder signal addressed look-up table (LUT) and appropriate latches. The developed digital signal processing technique achieves 25 nsec of high speed triggering angle detection by using direct parallel bit comparison of the shaft encoder digital code with a simulated angle reference code, instead of using angle value comparison which involves more complicated computation steps. In order to establish synchronization to an AC reference signal whose magnitude is variant with the rotating speed, a dynamic peak follow-up synchronization technique has been devised. This method scrutinizes the reference signal and provides the right timing within 40 nsec. Two application examples are described.

NOMENCLATURE

ADC	analog to digital converter
ACTION	logic signal, output of the action trigger logic circuit
$\overline{A11}$	most significant bit of address data
ANG TRIG	logic output of the 11-bit comparator circuit
BCD	binary decimal code
CYCLE	logic output of the counter control circuit
DET	output pulse of the high speed analog comparator (U54)
EOC	end-of-conversion, a logic status signal of analog to digital convertor
EPROM	electrically programmable read-only-memory
f	laser operating frequency, Hz
f_{max}	high limit operational pulse frequency of a laser system, Hz
f_{min}	low limit operational pulse frequency of a laser system, Hz
HIGH	logic state of 1, 5v in TTL level
LED	light emitting diode
LEND	latch enable signal to the angle data latches
LE1	latch enable signal to two low significant digit LED display modules
LE2	latch enable signal to two higher digit LED display modules
LOW	logic state of 0, 0v in TTL level
LUT	look-up table
M	number of live pulses
MPX	multiplexer
N	number of hidden pulses
ns	nanosecond
pps	pulse per second, 1/sec
RDY	logic status signal of the device

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RNG logic output of the peak track range limitter circuit

SEL logic status signal for a trigger mode of operation

SYNC logic pulse output of the dynamic peak follow-up synchronization circuit

Tc reciprocal of f, sec

tp operating pulse clock period of the control device, sec

TRIGA trigger pulse input to the action trigger logic circuit

TRIGD trigger pulse input to the display control logic circuit

TTL transistor-transistor logic

TW1~TW13 thumbwheel switches

U6 voltage controlled oscillator

U7 digital divider of 100

U15~U21 gray to binary converter

U34 digital divider of 10

U49 peak track range limitter

U52 peak detector

U53 inverting amplifier

U54 differential input analog comparator

U59 multiplexer

U60-U62 angle data latches

U63-U65 11 bit comparator

U71-U72 angle data display control logic circuit

U73 LUT

VCO voltage controlled oscillator

V_c AC sync reference signal from the camera, V

V_{pk} peak trace, output of the peak trace, V

V'_{pk} phase-compensated peak trace, V

VR1 trigger angle set potentiometer

VR2 peak track range set potentiometer

VR3 operating frequency set potentiometer

V_{RNG} DC trigger level to the peak track range limitter circuit, V

EXTENSIVE EFFORTS ARE - being made to develop fuel-efficient and more powerful intermittent combustion (I.C.) engines (1)*, which leads to fundamental studies of the physics and thermodynamics involved in a high speed combustion process. Theoretical computer modeling and simulations have been developed to predict two-dimensional air flow patterns in an I.C. engine (2,3). These codes require experimental verification. Cinematography or holographic interferometry has been determined to visualize and to quantitatively analyze dynamic air flow in a combustion chamber (4,5).

To achieve a successful flow visualization, a synchronization must be established. The synchronization here means proper timing of a film exposure relative to the light to record an event of interest. Pulsed laser systems, because of their high power and coherence, are widely used as lighting sources with cinematography or holographic interferometry for dynamic flow visualization.

Photographic flow visualization may be classified into two groups, continuous and discrete. Continuous photography corresponds to photographing flow motions in continuous time such as movies; while discrete applies to taking a single photograph of an event of interest at a discrete time such as a snapshot or holographic interferogram. Discrete photography requires a preset of a specific engine crank angle at which time a laser should be single-pulsed or multiplepulsed at specified time intervals. A control device is used to monitor the angular position of the engine crankshaft, and it generates a single pulse or a sequence of pulses to trigger a laser when it detects the engine at the preset angular position.

A programmed pulse burst sequence may be required to automate a visualization process or to run a slow speed movie camera that does not have a camera sync reference available. As shown in Fig. 1, a pulse burst cycle may consist of "M" number of live pulses and "N" number of hidden pulses. The live pulses actually trigger the laser, but the hidden pulses are not available externally. Instead, the hidden pulses will be counted internally to accumulate an amount of off-time, compensating for the frame period of the camera. This off-time is equal to N•Tp where Tp is the period of an operating pulse that actually drives a laser system. The pulse period is desired to be adjustable within the range of operational repetition pulse frequency of a laser system. The operational repetition frequency of a laser system is

*Numbers in parenthesis indicate references listed at the end of this paper.

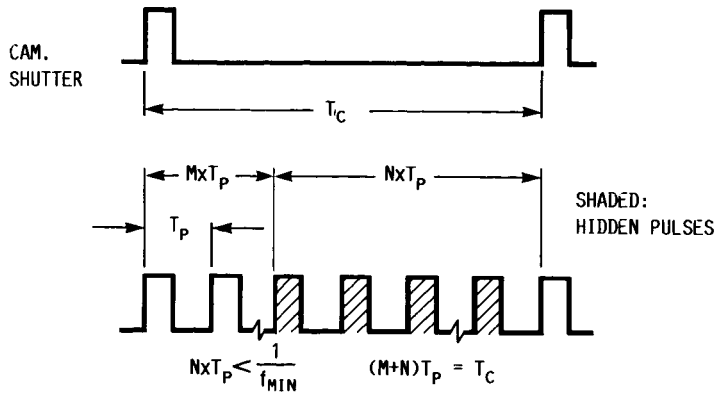


FIGURE 1. - PROGRAMMED PULSE BURST SYNCHRONIZATION WITH A SLOW SPEED MOVIE CAMERA.

bounded by the physical operating characteristics of that laser. For a typical example of a copper vapor laser, the minimum operational frequency (f_{min}) is 3000 pps and the maximum (f_{max}) is 8000 pps. Therefore, referring to Fig. 1, the off-time of N•Tp should be set less than $1/f_{min}$ for a laser system, while maintaining the summed period of live and hidden pulses (M+N)Tp equal to the frame period T_c of a camera that does not give a sync reference.

The operating pulse period may be used as a time measure for the derivation of a flow velocity by observing a seed particle displacement in a double exposure picture. The period, therefore, is required to be accurate and stable.

The use of a high speed movie camera that has a sync reference for each film frame may not need a programmed sequence of pulses because one laser trigger pulse may be appropriate for each frame. However, the control device should dynamically scrutinize the frame reference signal and extract the right time when a film frame is fully aligned with the camera aperture, independent of frame speed. At that time, the device must issue a trigger pulse that will immediately trigger a laser system to give light power to film a flow image.

In this development two types of synchronization are realized: one is internal trigger mode operation and the other is external trigger mode operation. In the internal trigger mode operation, the device generates sync pulses at the instant when it detects the engine at the preset trigger angle position. In the external trigger mode operation, the device generates sync pulses referenced to an externally provided camera frame signal.

In both trigger mode operations, the processing time required to generate sync pulses should be minimized, otherwise a significant timing error will occur. The process is desired to be done within a time required for 0.01° angle change of an engine running at 6000 rpm.

A 360° cycle can be resolved to 0.3516° using a 10-bit angle encoder, which at 6000 rpm corresponds to 9.8 μsec. A movement of 0.01° occurs in 271 nsec, therefore, the synchronization process should be done in less than 271 nsec. The design criteria for the device are:

1. Preset of a trigger angle in between 0° and 720° with 0.3516° angle resolution.
2. Triggering delay less than 271 nsec.
3. Programmability of up to six digit number of live and hidden pulses for a burst cycle.
4. Repeatibility of burst cycles.
5. Adjustibility of the operating pulse frequency in a range of 1 to 10 kHz with 0.1 Hz accuracy and stability.
6. Derivation of an optimal synchronization from the provided AC reference signal in less than 271 nsec.

This report is organized in four main sections. The section for Angle Display and Triggering Circuit describes a design technique to realize the criteria 1 and 2. The Camera Sync Acquisition section handles a technique to accomplish the design criteria 6. A method to realize the design criteria 3, 4, and 5 is presented in the section of Pulse Burst Sequence Generation. Finally, the performance section provides application examples of the developed device.

ANGLE DISPLAY AND TRIGGERING CIRCUIT

The control system employs an absolute optical shaft encoder to monitor an angular position of the engine rotation. An absolute shaft encoder generates a digital code output unique to each angular position. The shaft angle encoder produces a Gray code output. This code has only one bit change for each incremental angle change so it makes the fastest logic transitions with less jittering noise compared to other digital codes. The Gray code from the encoder is converted to a complimentary binary code by a Gray to Binary converter consisting of the components U15 through U21 as shown in a block diagram of Fig. 2. Complete electronic schematics are given in Appendix A.

Even though each complimentary binary code represents a unique angle, it still has to be

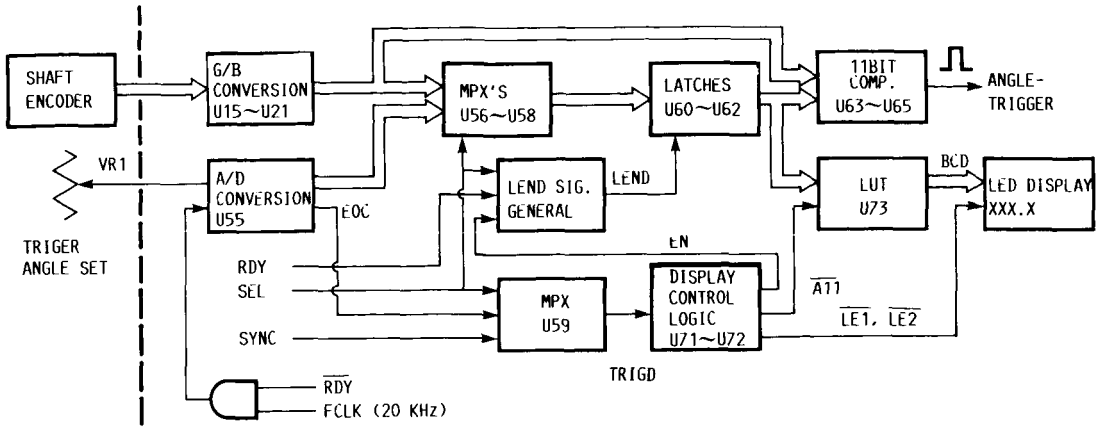


FIGURE 2. - ANGLE DISPLAY AND TRIGGERING CIRCUIT.

translated to a value in the unit of degrees. The translated angle value corresponding to each binary code is programmed into an EPROM. The program of EPROM implements a look-up table (LUT), which is accessed by a binary code. Thus, a binary number derived from a Gray code of the shaft encoder addresses an entry of LUT that contains its corresponding angle value. The angle is displayed in four significant decimal digits including one fraction on four HP5082-7302 LED display modules. Since the LED display modules take positive BCD (binary coded decimal) formatted input, the angle value programmed into EPROM (LUT) should be a BCD number which is then directed to the input of the LED displays. One decimal digit takes four bits to be converted to a BCD number. Therefore, BCD conversion of a four significant decimal digit number requires 2 bytes (16 bits). The two bytes wide BCD representation of an angle value needs to be split into two one-byte wide memory spaces of EPROM. This requires one additional most significant address bit, $\overline{A11}$. A 2732 EPROM is used, which has 4096 bytes of memory. Since an angle value takes two bytes, 2048 angle values can be stored. The two least significant BCD numbers of angle data reside in the upper half of the EPROM. The two most significant BCD numbers reside in the lower half of the EPROM. Therefore, the LUT in the EPROM contains 4096 bytes of BCD formatted angle data representing 2048 angles in increments of 0.3516°. For 360° revolution with 0.3516 angle resolution a 10 bit absolute shaft encoder is required. To interface with a 1080° combustion process, such as for the rotary engine, the shaft encoder should be coupled with the output shaft in a 3 to 2 ratio.

Logic "HIGH" on $\overline{A11}$ points to two lower significant digits of angle data, and logic "LOW" on $\overline{A11}$ points to two other higher significant digits of the angle data. The method of loading the two parts of an angle data onto four LED display modules is illustrated in a logic timing diagram of Fig. 3. A display control logic circuit consisting of U71 and U72 as shown in Fig. 2, first generates an 800 nsec wide positive pulse, LEND, on the rising edge of TRIGD. The logic state HIGH of LEND releases

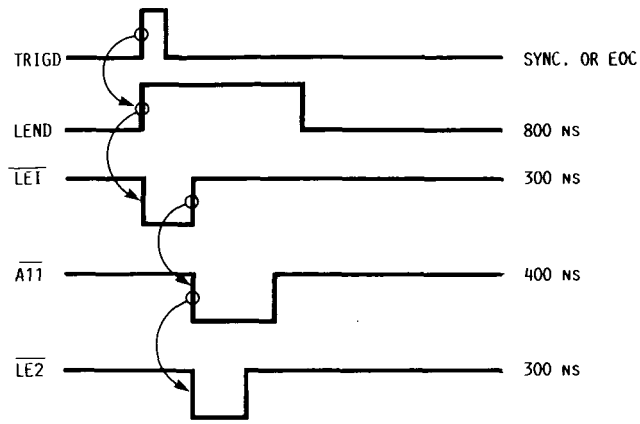


FIGURE 3. - LOGIC TIMING DIAGRAM FOR ANGLE DATA DISPLAY.

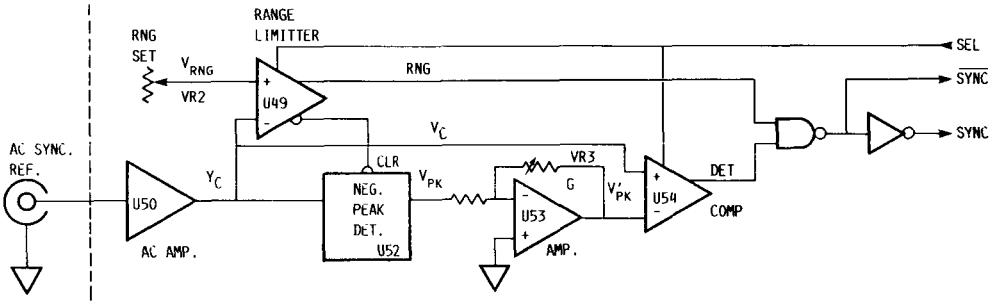
the latches (U60 through U62) and allows them to take new address data that will access new event angle data on the LUT. Once the latches are released, a 300 nsec negative pulse $\overline{LE1}$ is generated on the rising edge of LEND. When $\overline{LE1}$ is low, two low significant digit LED display modules are unlatched and loaded with two lower BCD numbers which represent new angle data from the LUT.

Memory access to the LUT and loading takes less than 300 nsec. After 300 nsec, $\overline{LE1}$ returns back to logic HIGH state to hold the display of the updated two low significant numbers of the angle data. This logic transition triggers a state change of $\overline{A11}$ from HIGH to LOW to point to the other two high BCD numbers of the new angle data. Once the address lines point to the other two high BCD numbers of the updated angle data, $\overline{LE2}$, which is another enable input to two other higher significant digit display modules, changes from HIGH to LOW. When $\overline{LE2}$ is LOW, the two higher digit display modules are unlatched and loaded with two new high BCD numbers of the new angle data.

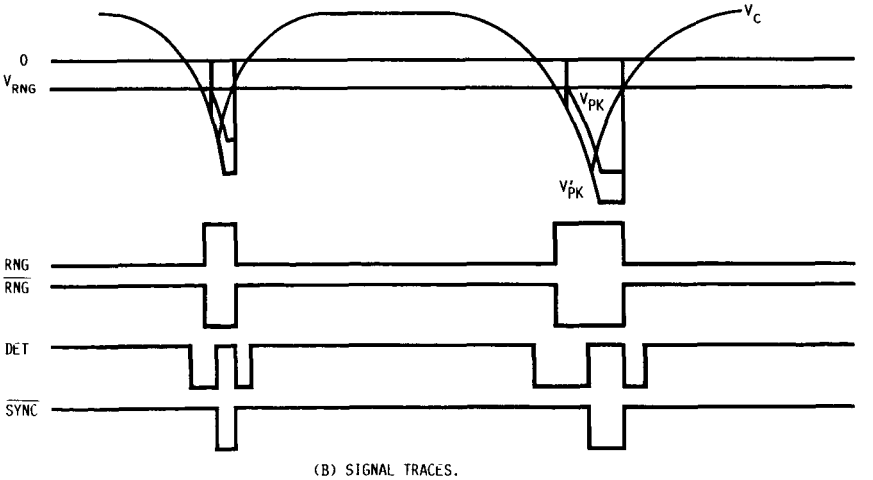
The signal TRIGD that initiates all the aforementioned angle display processes is an output from a two input multiplexer (U59). For the internal trigger mode of operation, the SEL input to the multiplexer (MPX) is low and the MPX selects an EOC input to TRIGD output. For the external trigger mode operation, SEL is HIGH

and the MPX connects the SYNC input to TRIGD output. The latter is derived from a sync acquisition circuit that is discussed in a later section and the former is obtained from an output of an analog to digital converter (ADC). The updating processes of the angle display take place within 800ns of logic HIGH of LEND. This results in enabling the device to capture an event timing of an engine running up to 73240 rpm speed with the use of a 10 bit gray code shaft encoder (0.3516° resolution).

In order to take discrete photographs, one should preset a specific triggering angle at which a lasing sequence starts and exposes film over a flow sequence of interest. A trigger angle is set by adjusting a potentiometer VR1 on the front panel. VR1 has a built-in push-pull switch. The switch has to be pushed in for the internal angle trigger mode operation, which puts SEL in logic LOW. A DC voltage drop on VR1 goes to the analog input of a 12 bit ADC. This produces an 11 bit digital output corresponding to the input voltage magnitude. The digital output from ADC is configured in complimentary binary format and simulates an actual address data that is obtained as described above. The digital word simulated by the ADC addresses an entry on the LUT through multiplexers and latches. The multiplexers U56 to U58 select address data either from the ADC if SEL = 0 (LOW), or from the Gray to Binary converter if SEL = 1 (HIGH), and allow them to access the LUT. Since SEL = 0, the output of the multiplexers is the digital word generated from the ADC. The latches U60 through U62 holds the current address data while the latch enable input LEND is LOW until the address data is updated for new event angle display with HIGH on LEND. The latch enable input to the latches, LEND is developed from the LEND logic signal generator circuit. The logic function of the generator is, LEND = $\overline{SEL}\cdot\overline{RDY}$ + SEL•EN. Since SEL = 0, the second term is removed, and the equation becomes LEND = $\overline{SEL}\cdot\overline{RDY} = \overline{RDY}$. During the preset operation, RDY stays LOW (0). Therefore, LEND = $\overline{RDY} = \overline{0} = 1$. HIGH of LEND frees the latches and allows them to follow up any change of the input address data. A free running clock of 20 kHz is gated with RDY signal and goes to the start input of the ADC. Therefore, the digital output of the ADC is updated every 50 µsec as the triggering angle setting pot is turned. When a desired trigger angle is set on the angle display, SET switch is depressed to put RDY in HIGH (logic 1). RDY = 1 and $\overline{RDY}$ = 0 stops the start pulse input to the ADC and locks the latches since LEND = $\overline{RDY} = \overline{1} = 0$. The latches are now holding the address data that represents the desired triggering angle. The simulated address data that represents the prespecified trigger angle is loaded into the 11 bit comparator circuit which is built by cascading three four-bit comparators, (74LS85's), and compared with the running address data derived from the shaft encoder. When all bits of both the reference and running address data are equal, the comparator circuits generate the



(A) BLOCK DIAGRAM.



(B) SIGNAL TRACES.

FIGURE 4. - DYNAMIC PEAK FOLLOW-UP SYNCHRONIZATION.

ANG TRIG pulse which initiates a programmed pulse burst sequence to trigger a laser system.

It should be noted that the developed angle triggering technique employs direct parallel bit comparison of the shaft encoder digital code with a simulated angle code that actually represents a specified triggering angle, rather than angle value comparison. The angle value comparison method usually takes more complicated steps beyond the method presented, to compute a running angle value from the shaft encoder signal and to perform four significant digit number comparison between the running angle and the reference angle. These cause longer processing times and require complicated calibration procedures. No calibration is required with the method presented: The set-up is as simple as to get 0° shown on the angle display at the physical TDC of an engine, by turning the shaft encoder. The developed technique achieves 25 nsec of high speed triggering angle detection that corresponds to 0.0009° of the output shaft rotation of an engine running at 6000 rpm, with an assumption of no 1/2 LSB error in 10-bit Gray code form the shaft encoder.

CAMERA SYNC ACQUISITION

Establishment of an interface and synchronization with a camera is a typical application. The technique described in this section is to establish synchronization with a high speed movie camera which uses a magnetic pick-up as a position sensor. The sensor monitors the alignment of a film frame with the camera aperture. The negative peak point on the magnetic pick-up frame signal references the time when a film frame is fully aligned with the camera aperture. The negative peak time for each film frame cycle is the sync time at which the laser is preferred to be triggered. The magnitude of the induced voltage from a magnetic pick-up signal varies with a time rate of change of magnetic flux linkage. The time rate of change of the magnetic flux linkage is proportional to the speed of a rotating device. Therefore, negative peaks on the frame signal are not the same, but vary with the camera running speed. For a Fastax 16 mm high speed rotating prism camera, the negative peaks ranged between -1.5 and -2.1 V. Therefore, the synchronization cannot be adequately established by simply setting a fixed trigger level to a negative peak. Excellent synchronization has been achieved by using a dynamic peak follow-up trigger level scheme instead of a fixed trigger level scheme which does not have the ability to dynamically update the change of the negative peaks of the reference signal. The developed dynamic peak follow-up synchronization method is block-diagramed in Fig. 4. Also, signal traces from components are shown in Fig. 4.

The negative peak detector tracks the camera frame signal V_c until a negative peak is reached while the clear input to the detector, RNG is LOW. The negative peak is then retained for a time long enough to acquire the peak event time as described later. The detector then resets by setting RNG = HIGH, to update another peak for the next cycle. The pulse RNG and its compliment $\overline{RNG}$ are outputs of a high speed range limiter circuit (U49), and define the peak track range. The range is set by a DC trigger level V_{RNG}, which is obtained from the range set potentiometer VR_2. Whenever the camera frame signal V_c crosses the trigger level V_{RNG}, the limiter trips and produces TTL complimentary outputs RNG and $\overline{RNG}$ as shown in Fig. 4.

Since the peak detector (U52) produces the negative peak in absolute value, the peak detector output is inverted by an inverting amplifier (U53) to get the true negative peak trace. The negative peak trace V_{pk} is phase shifted relative to the camera frame signal V_c due to the acquisition time delay of the detector. The phase shift is compensated by adjusting the gain of the inverting amplifier such that the peak trace is superimposed on V_c. The magnitude of

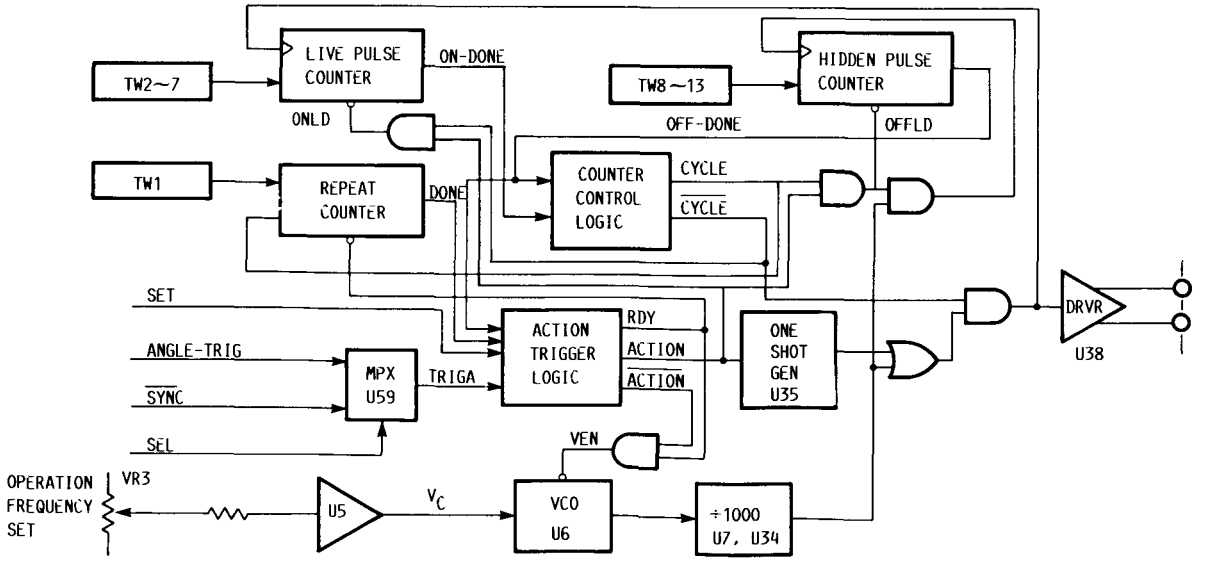


FIGURE 5. - BLOCK-DIAGRAM OF PROGRAMMABLE PULSE BURST GENERATOR AND CONTROL CIRCUIT.

the peak trace is not a matter of a concern in this application.

The phase compensated peak signal V'_{pk} and the frame signal V_c go to the differential inputs of a high speed analog comparator (U54), which develops TTL output pulse DET in 20 nsec time when the strobe input to the comparator SEL is HIGH. For the external trigger mode of operation, the mode select switch on the trigger angle set potentiometer VR1 is pulled out to put SEL in logic HIGH. In the internal angle trigger mode of operation, the switch is pushed in and SEL becomes LOW. The LOW state of SEL disables the output strobe of two comparators U49 and U53. The two signals V'_{pk} and Vc start to break the superposition at a negative peak. The comparator (U53) therefore guarantees a pulse transition at the negative peak. The output DET retains the peak event logic transition with other transitions. To extract the peak event pulse labelled as $\overline{\text{SYNC}}$, DET is NAND-gated with the pulse RNG to extract the pulse which occurred during the peak track range. The described dynamic peak follow-up synchronization technique achieves 40ns of high speed processing time.

PULSE BURST SEQUENCE GENERATION

A programmed pulse burst sequence should start in synchronization with ANG-TRIG or SYNC. Care must be taken to minimize synchronization delay and timing error. A block diagram of the pulse burst sequence generation is presented in Fig. 5 for the description of this section. A desired operating pulse frequency is preset by the frequency set potentiometer VR3 on the front panel. The DC voltage provided by the potentiometer goes to the frequency control input of a voltage controlled oscillator (U7) through a buffer (U5) and sets an output frequency up to 10 MHz. Then, the VCO output frequency is divided by 1000 by digital dividers U7 and U34. Hence, a desired TTL level operating pulse is obtainable up to 10 kHz of frequency with 0.1 Hz accuracy and stability.

Two sets of six BCD output thumbwheel switches TW2 through TW7 and TW8 through TW13 specify any burst of length less than 10^6 of live pulses and hidden pulses. Repetition of burst cycles is set by a thumbwheel switch TW1 up to 9, or infinite by setting 0. The specified numbers are loaded into each counter. Six 74190 decimal up/down counters are used to form a 10^6 decimal down counter to count live pulses and hidden pulses.

When all the desired operation parameters are set, a set switch on the front panel is depressed which puts a status signal RDY to HIGH. This positive logic transition enables the action trigger logic circuit to respond to three other inputs; TRIGA from a multiplexer U59, $\overline{\text{OFF-DONE}}$ from the hidden pulse counter, and $\overline{\text{DONE}}$ from the repetition counter. The multiplexer connects either ANG-TRIG or SYNC input to TRIGA output according to the logic state of the control input signal SEL as described in the previous section. When RDY = HIGH, the action trigger logic circuit asserts a positive transition of TRIGA and puts the output ACTION in HIGH, at which a one-shot generator is triggered to produce the first pulse of burst pulses. The application of the one-shot generator is used to eliminate the plus/minus one-half operating pulse clock timing error which is inherent with a free running clock sync method. The consecutive pulses following the first pulse are generated from the VCO that is activated by LOW of the enable input derived from an AND gate having two inputs $\overline{\text{ACTION}}$ and RDY. The period of the consecutive pulses is equal to the period of the prespecified operating pulse frequency because the succeeding pulses are every thousandth pulse from the VCO. This output is initiated by the signal ACTION. These pulses are AND gated with a status logic signal $\overline{\text{CYCLE}}$ outputted from the counter control logic circuit. At the time of the positive transition of ACTION, CYCLE is LOW and its complement $\overline{\text{CYCLE}}$ is HIGH. The pulse bursts then pass through the AND gate and are available externally through a RS-422 line driver to begin laser pulsing. The live pulses from the output of the pass AND gate are counted (a preset number M) by the live pulse counter. This counter is activated by ONLD = HIGH, which is obtained from an AND gate consisting of two inputs, ACTION = HIGH and $\overline{\text{CYCLE}}$ = HIGH. It should be noticed that CYCLE = LOW or $\overline{\text{CYCLE}}$ = HIGH activates the live pulse counter and deactivates the hidden pulse counter. When CYCLE = HIGH or $\overline{\text{CYCLE}}$ = LOW the reverse action of the two counters occurs.

Once N number of live pulses is asserted, the live pulse counter generates a negative pulse $\overline{\text{ON-DONE}}$, which triggers a logic state change of CYCLE from LOW to HIGH. CYCLE = HIGH or $\overline{\text{CYCLE}}$ = LOW inhibits the pass of pulses through the aforementioned AND gate and activates the hidden pulse counter. The hidden pulses obtained from the VCO through the digital dividers, are not available externally because they are nulled by the LOW input of the pass AND gate. The hidden pulse counter also generates a negative pulse $\overline{\text{OFF-DONE}}$ when it finishes counting N hidden pulses. The negative pulse $\overline{\text{OFF-DONE}}$ switches the logic state of CYCLE and terminates one cycle of the pulse burst sequence. On the rising edge of another pulse, TRIGA, the control system repeats the action of generating pulse burst sequence for another cycle. The burst cycles are repeated until the specified number of repetition is done or the system is reset. The logic timing diagram of the described pulse burst sequence generation is shown in Fig. 6.

AUXILIARIES

The system is incorporated with two monitoring circuits and displays for the engine operating speed and pulse frequency. The engine speed monitoring circuit measures the engine RPM and updates the display 256 times per minute. The frequency monitoring circuit checks the preset

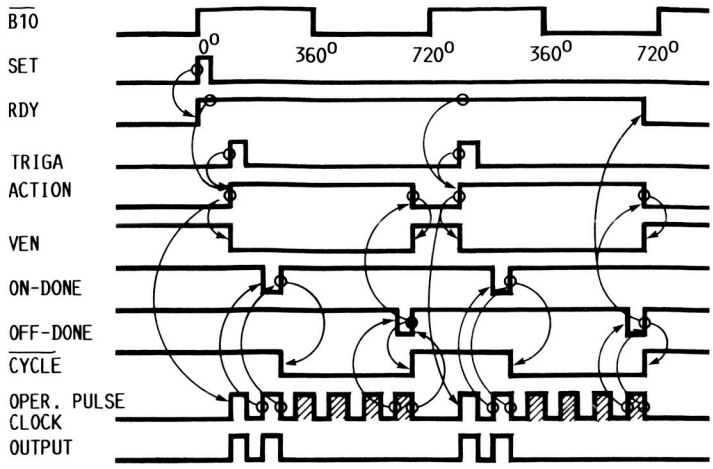


FIGURE 6. - LOGIC TIMING DIAGRAM FOR PULSE BURST GENERATION.

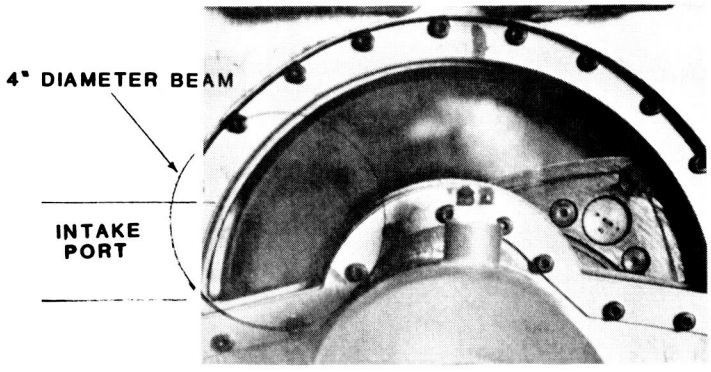
operating pulse frequency and updates the display in every 0.1 sec. Seven LED lamps are installed on the front panel to indicate the system functioning status. They are marked as Power, Ready, Triggered, Ext.- Trig., Live Pulse, Hidden Pulse and Over Range.
The Over Range lamp indicates that the preset burst cycle period determined by the sum of M live pulses and N hidden pulses over-ranges the period of a combustion cycle.

The whole circuits are assembled in Tektronix TM 500 series blank modules and they are plugged into a TM 503 power module mainframe. The cards are bused through 56 pin edge connectors and four 16 pin dip connectors.

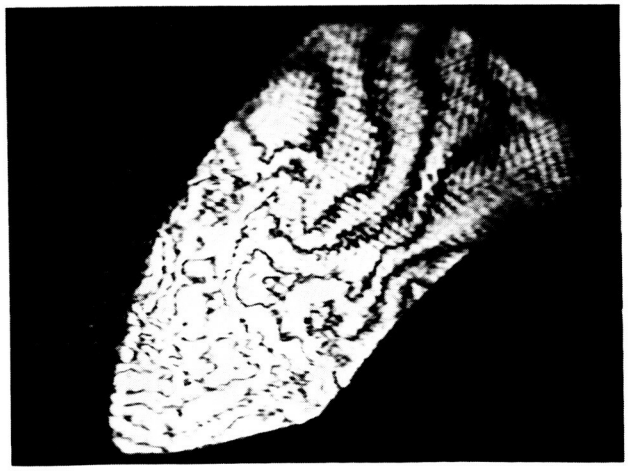
PERFORMANCE

The control system developed has been successfully used to make holographic interferograms and high speed movies for dynamic flow visualizations in internal combustion engines. Holographic interferometry has been successfully used for the first time to visualize flowfield structures in the combustion chamber of a motored rotary engine (4). One of the interferograms from the referenced paper is presented in Fig. 7. Figure 7(a) shows the rotor position and field of view at which the interferogram of Fig. 7(b) was taken. In this experiment, a pulsed, q-switched ruby laser was used in a double pass reference beam path matched system. In order that the flow patterns of interest could be observed, small quantities of helium were injected with the intake air. The laser was triggered at a prespecified shaft crank angle using the developed control system. The interferogram was made by first taking one exposure without helium and a second exposure with helium on. The photograph shows that intense mixing takes place in front of the intake port just below the injection point and the helium soon becomes well dispersed. In this experiment, the control system is well conducted as designed.

Another flow visualization example shows the use of the dynamic peak follow-up synchronization technique implemented in the control system. High speed movies were taken to view the air flow activities in a motored, single-cylinder piston engine, which is believed to be the first published study showing a high speed

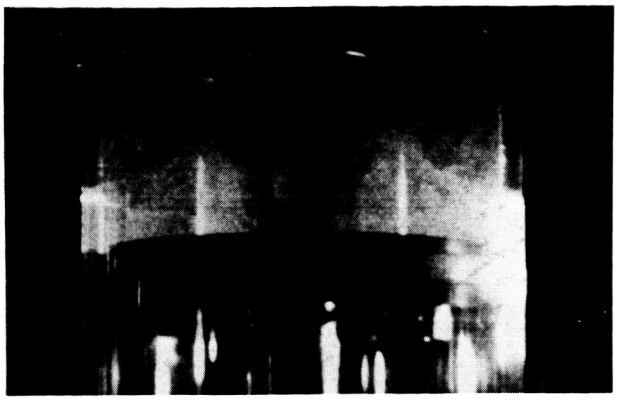


(A) Rotor Position and Field of View

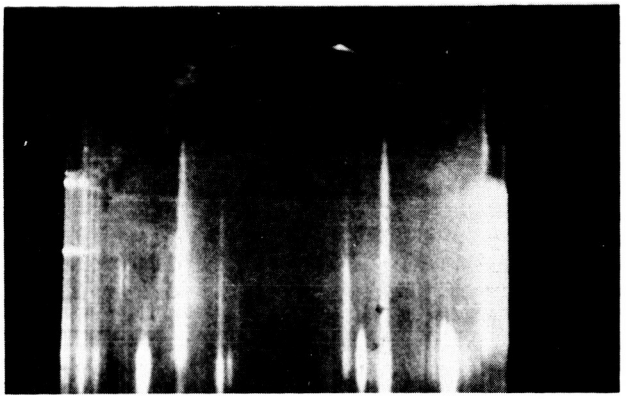


(B) Double Exposure Interferogram

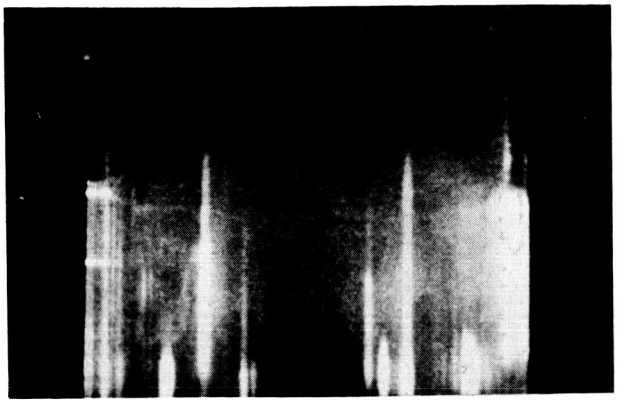
Figure 7. Holographic Interferogram of Flow in a Motored Rotary Engine



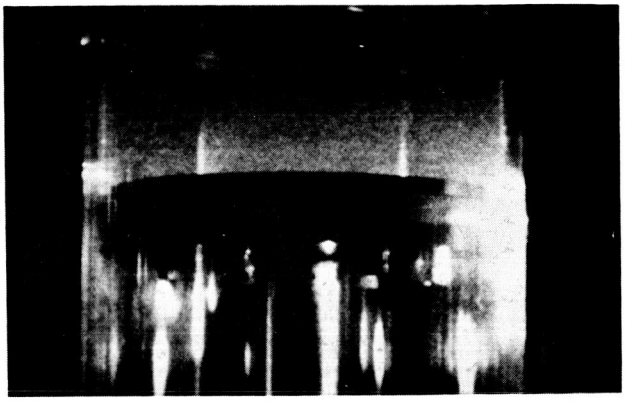
(A) intake 45 deg



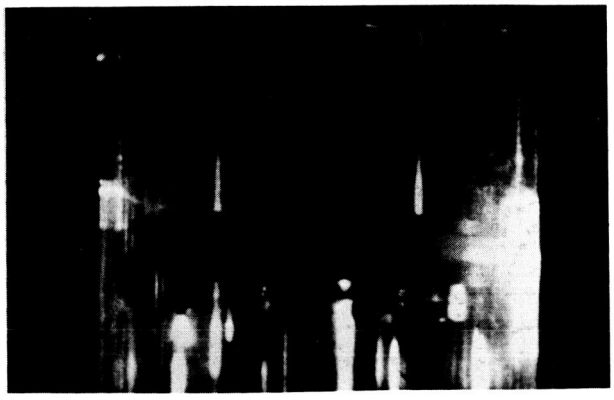
(B) intake 135 deg



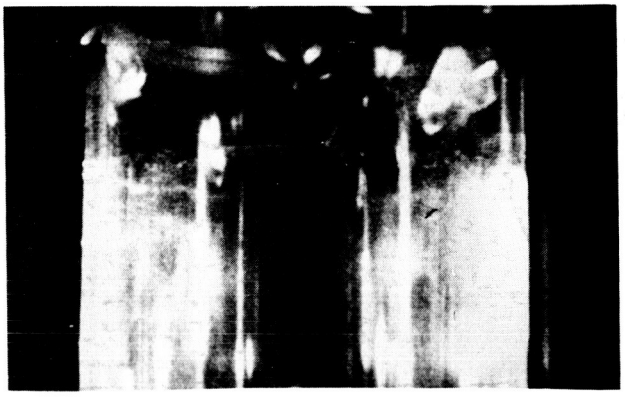
(C) compression 225 deg



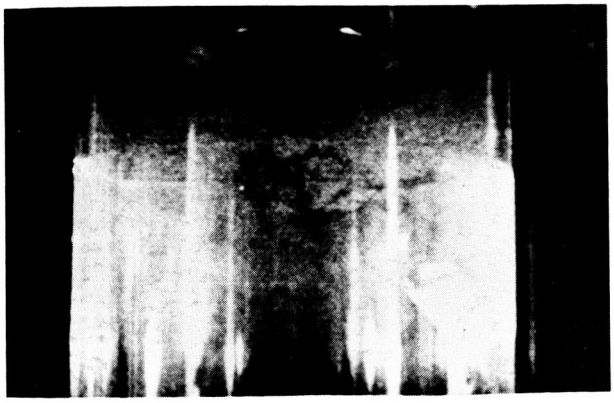
(D) compression 315 deg



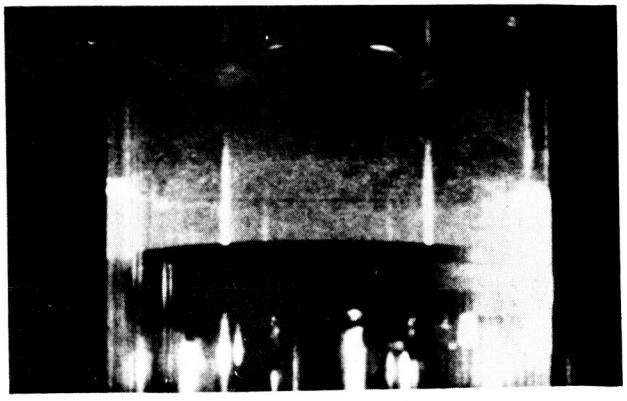
(E) expansion 405 deg



(F) expansion 495 deg



(G) exhaust 585 deg



(H) exhaust 675 deg

Figure 8. Frames taken from a movie showing the air flow through one engine cycle at 300 RPM.

planar observation of air flow in a four-stroke pistoncylinder assembly (5). In this work, a 40 W copper vapor laser was used as the light source. It was chosen because it has a fairly high lasing repetition rate, up to 8000 Hz, and can provide 8 mJ in a 30 nsec pulse. Since a flow visualization movie is made possible with light scattered off particles which are following the air flow, particles are seeded into the combustion chamber. The particles used in this experiment are dioctylpthalate (DOP), of which 85 percent have diameters less than or equal to 1.53 ?m. A Fastax 16 mm high speed movie camera what provides an AC frame sync reference signal was used to film the flow. Synchronization was established using the dynamic peak follow-up synchronization technique in one laser pulse per frame because the camera frame speed of 5000 frames/sec is equal to the optimal operation pulse repetition rate of the laser. Selective photographs taken from a movie showing the air flow through one engine cycle at 300 rpm are presented in Fig. 8.

It should be recognized that the depiction of the flow is difficult without actual viewing of the movie, because it is by observing the movement of the flow structures from frame to frame that the flow direction is inferred. As seen in Fig. 8, glare of transparent quartz cylinder is a significant problem which impeded the observation of the flow structure. An attempt was made to eliminate it and to extract the flow information using a digital image processing system. It was not possible to remove glare without the loss of the flow information because the flow information is hidden under the saturated grey level of the glare. The use of antireflective coatings would substantially alleviate glare problems. High turbulence and reversals of air flow were observed in movies.

CONCLUSIONS

A programmable synchronization trigger control system for dyanmic flow visualization has been successfully designed and demonstrated. The design is unique in direct parallel bit comparison of the shaft encoder digital code with a simulated angle reference code instead of angle value derivation and comparison. High speed angle detection of 25 nsec has been achieved. Displaying an event timing of an engine running up to 73 240 rpm has been also realized in the design. A fixed trigger level scheme failed to establish the necessary synchronization, because of an AC reference signal whose magnitude is variant with the rotating speed. The problem has been solved by the dynamic peak follow-up synchronization technique.

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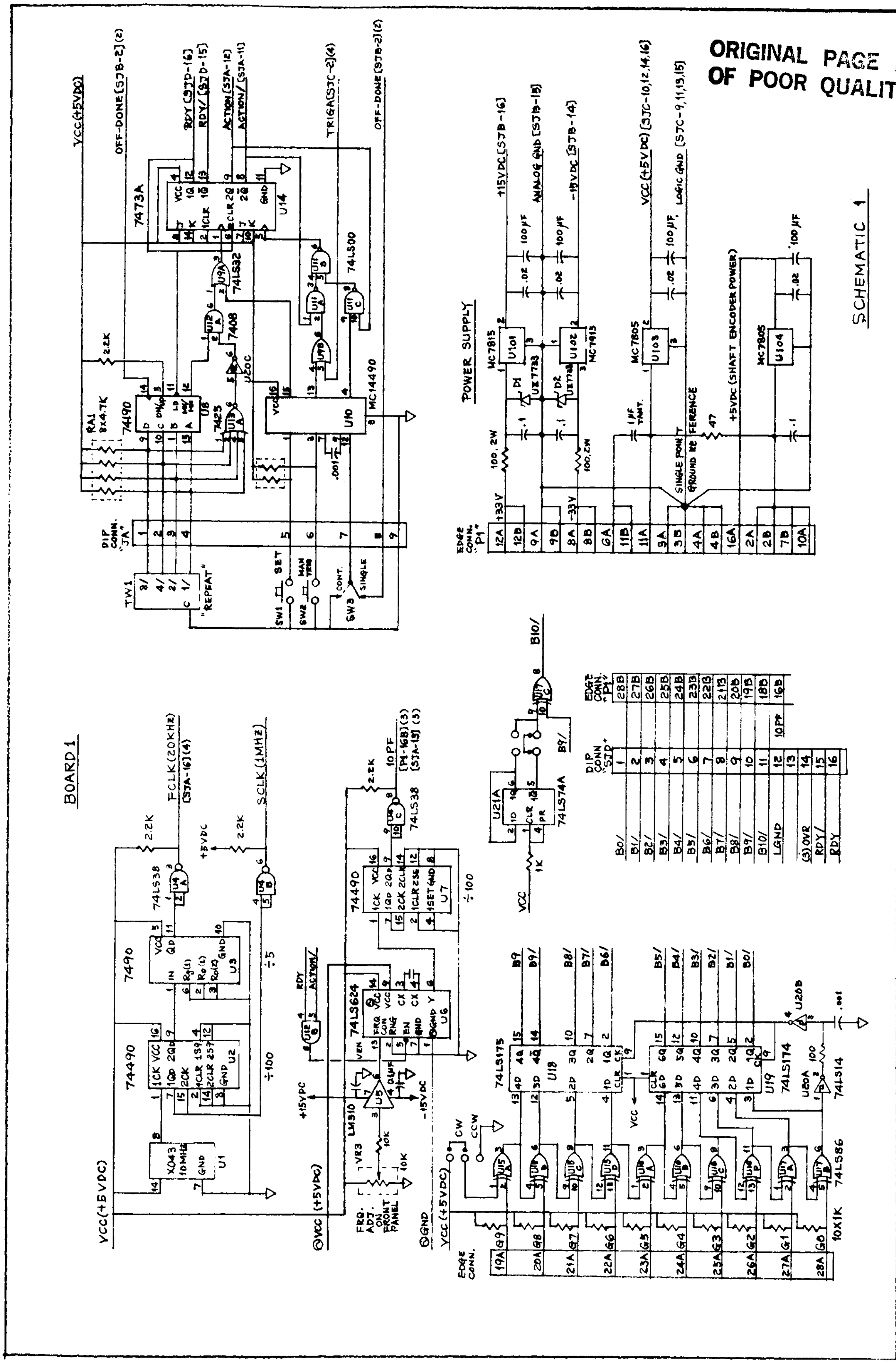

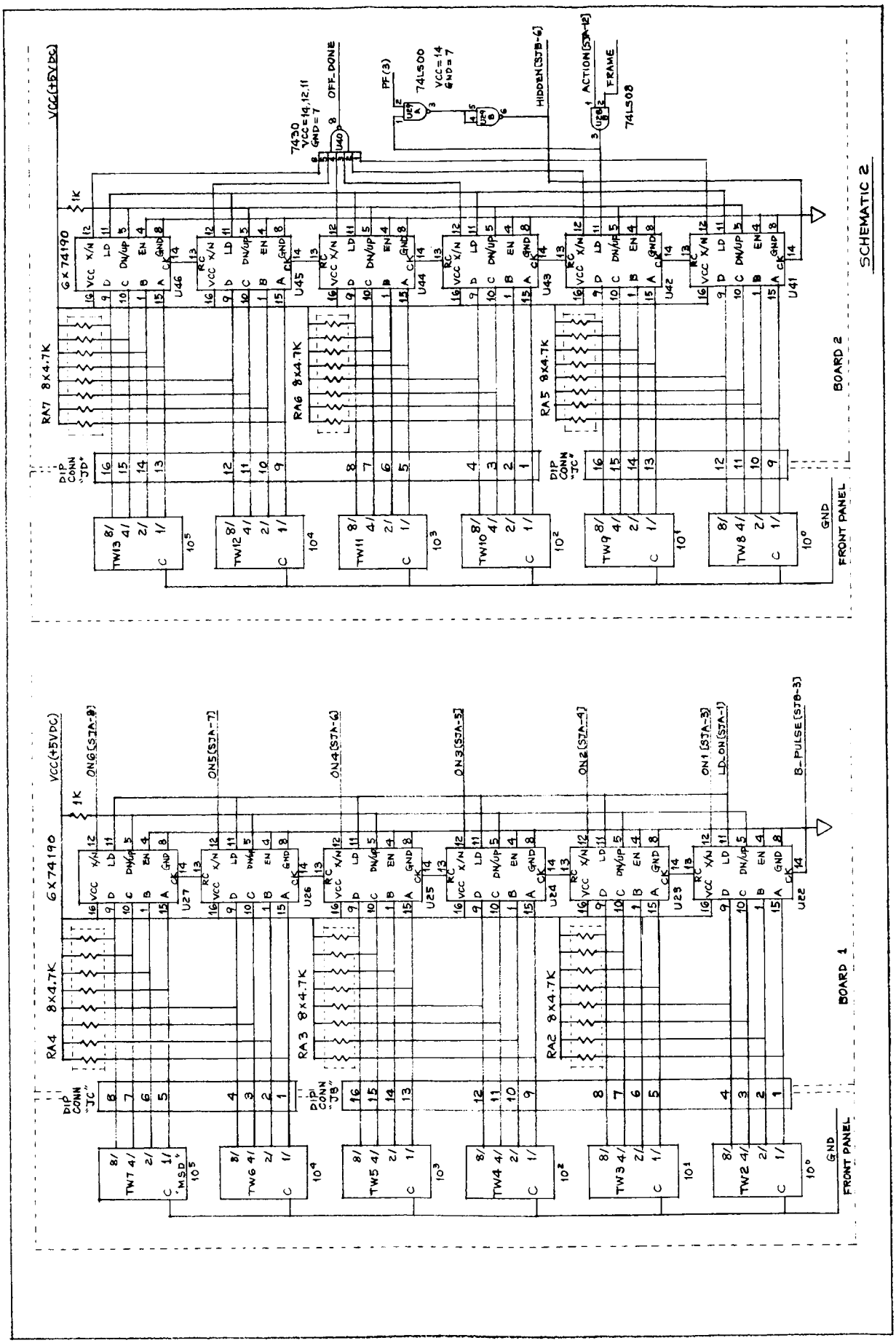

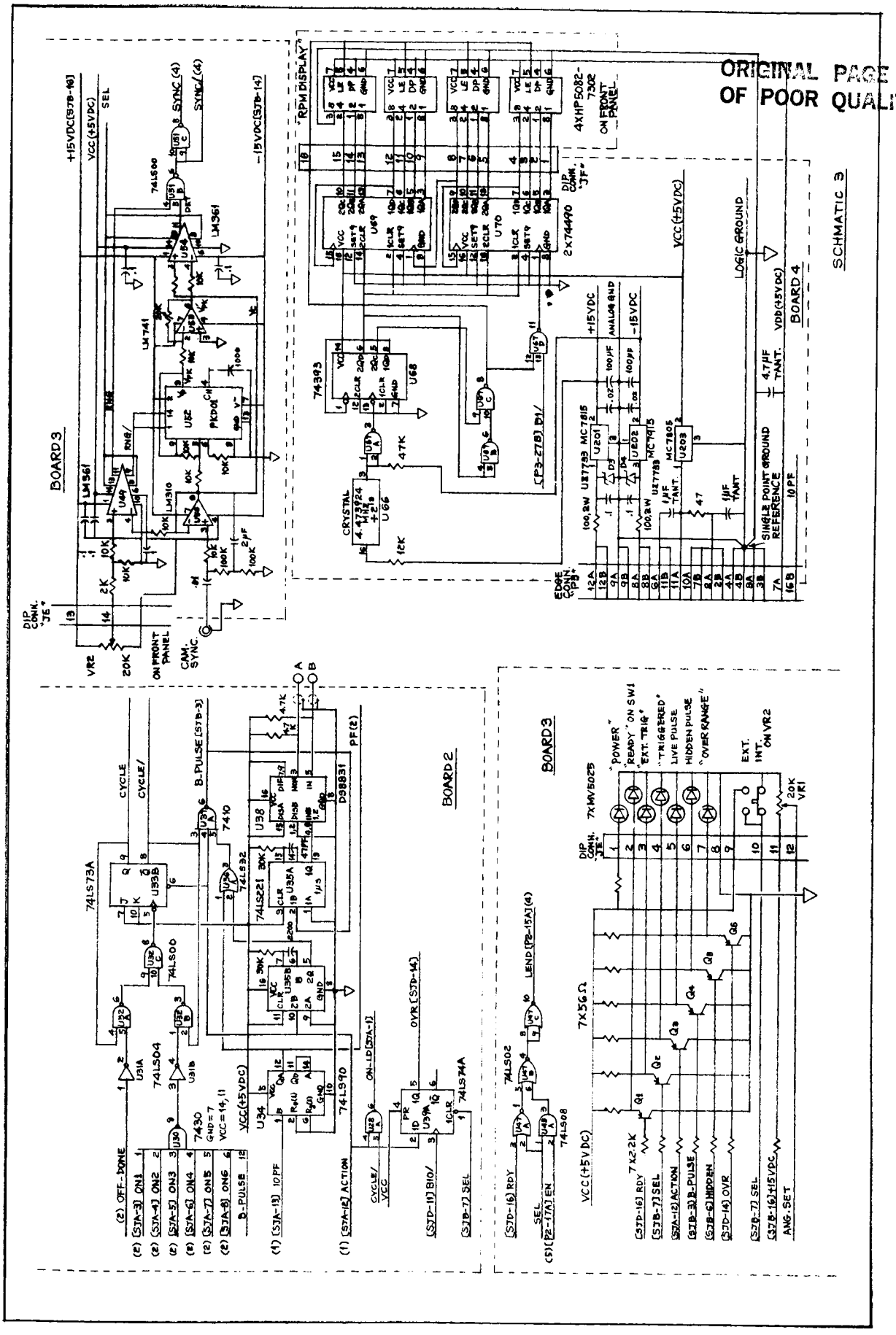

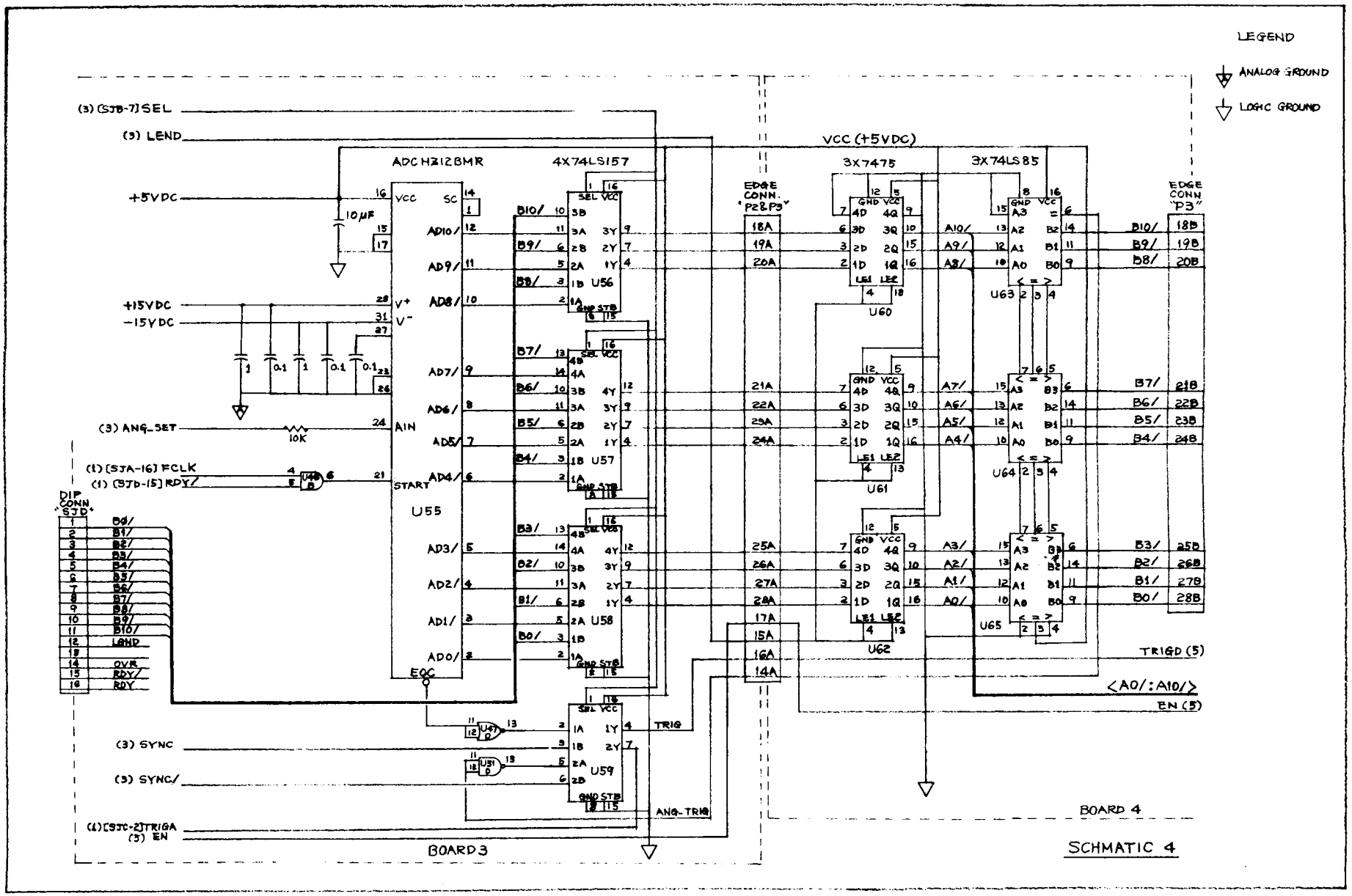
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ANALOG GROUND
LOGIC GROUND
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(3) LEND
VCC (+5VDC)
ADC HI2BMR
4X74LS157
3X7475
3X74LS85
EDGE CONN. "P2&P3"
EDGE CONN "P3"
+5VDC
10 µF
+15VDC
-15VDC
(3) ANG_SET
10K
(1) (SJA-16) FCLK
(1) (SJD-15) RDY/
DIP CONN "SJD"
U55
U56
U57
U58
U59
U60
U61
U62
U63
U64
U65
TRIG
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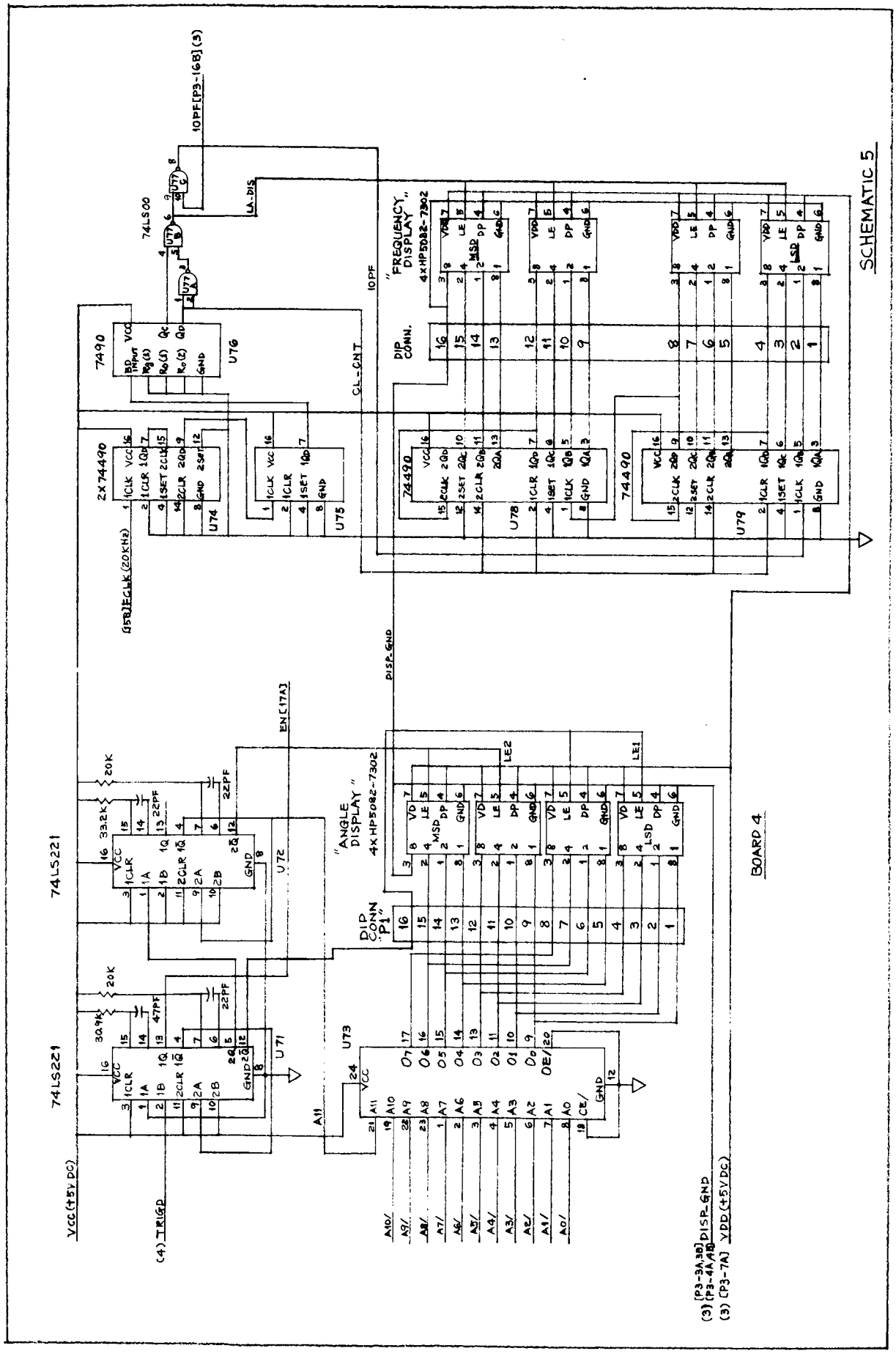
SCHMATIC 4



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15. Supplementary Notes

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16. Abstract

The use of cinematography or holographic interferometry for dynamic flow visualization in an internal combustion engine requires a control device that globally synchronizes camera and light source timing at a predefined shaft encoder angle. The device is capable of 0.35° resolution for rotational speeds of up to 7 3240 rpm. This was achieved by implementing the shaft encoder signal addressed look-up table (LUT) and appropriate latches. The developed digital signal processing technique achieves 25 nsec of high speed triggering angle detection by using direct parallel bit comparison of the shaft encoder digital code with a simulated angle reference code, instead of using angle value comparison which involves more complicated computation steps. In order to establish synchronization to an AC reference signal whose magnitude is variant with the rotating speed, a dynamic peak followup synchronization technique has been devised. This method scrutinizes the reference signal and provides the right timing within 40 nsec. Two application examples are described.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
Laser control system; Flow visualization; Programmable synchronized burst pulse; Control system	Unclassified - unlimited STAR Category 33

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