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A SYNCHRONOUS DATA ANALYZER FOR THE MINIMUM DELAY DATA FORMAT (MDDF) AND LAUNCH TRAJECTORY ACQUISITION SYSTEM (LTAS)

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INTRODUCTION

As a result of the Space Shuttle Program, Wallops Flight Facility (WFF) has become increasingly more involved in transmission and reception of MDDF and LTAS data. Since WFF's initial efforts relating to Shuttle support, these data formats have been adopted as the primary radar data formats employed at WFF. With the development of more sophisticated data systems utilizing these formats, the need for more sophisticated test equipment has become apparent.

Early test and monitoring apparatus employed at WFF provided for elementary display of mostly undecoded or uninterpreted raw data. This, in conjunction with the instantaneous nature of these displays, created a void in precisely determining whether a problem might exist with the raw data. It was, therefore, desirable to devise a test apparatus which would not only provide a more intelligible presentation of the data but also allow one to selectively capture several frames for scrutiny of data content. The Synchronous Data Analyzer (see Figure 1) provides for these capabilities and more.

FUNCTIONAL DESCRIPTION

The Synchronous Data Analyzer is a device that can be utilized in monitoring and troubleshooting activities associated with certain data formats employed at WFF. It is capable of receiving, decoding, and displaying any one selected channel out of eight synchronous 2400 baud serial data inputs. The decodeable data formats include MDDF and LTAS as well as a locally devised time format. For the purpose of this paper, discussion is limited to that involving MDDF and LTAS. Once decoded, the data is then reformatted to provide useful information related to both the data content and format configuration. This formatted data is then displayed in real-time and updated at the 10 frames per second rate consistent with the data input rate. In addition, a history of 100 frames of data is maintained for post reception evaluation.

Other useful functions available to the operator include data sync and quality error (MDDF Cyclic Redundancy Code (CRC) or LTAS checksum) checking, counting and trapping. It is also possible to simultaneously transmit a static frame of modulated data in any of the formats while still receiving real-time data in another format.

Sample displays for MDDF and LTAS are depicted in Figures 2 and 3, respectfully. The top display line indicates the operator selected data format and channel to be decoded. The following six lines contain information decoded from the data itself and is displayed in units and/or terminology consistent with the selected data format. The bottom display line provides for data sync and quality error count as well as the operator selected mode of operation. The selected channel can also be displayed in a

binary format (see Figure 4) for easy observation of the logic levels of the entire 240 bit frame.

DESIGN CONCEPT

The fundamental concept applied to the design of the Synchronous Data Analyzer was to accomplish as many functions as possible in software. This approach was taken in order to minimize unique hardware design, therefore minimizing production time, cost, and efforts. This approach resulted in utilization of commercially available hardware in all cases except one simple interface card for the alphanumeric plasma display. Actual cost of materials approaches $5,000 with about one man week of labor required to completely assemble and test one unit.

HARDWARE CONFIGURATION

The Synchronous Data Analyzer is comprised of a modem, a microcomputer system, a keypad and an alphanumeric plasma display as configured in Figure 5.

The modem used is a synchronous, 2400 baud, Bell 201C compatible unit. It is configured to operate as a four wire receiver/transmitter and supplies the microcomputer with RS-232 receive data and clock. The transmitter timing is internally derived and is also provided to the microcomputer for transmit synchronization.

The microcomputer is an 8085 microprocessor base system built upon the STD BUS. It is comprised of an 8085 microprocessor with firmware and buffer memory, relay cards used for multiplexing the eight data inputs to the modem, a synchronous communication card to provide RS-232 interface to the modem, and interface cards to drive the plasma display and keypad. The

keypad is a 3x4 matrix with labeled dedicated functions for keeping command sequences to a minimum with operator ease in mind.

The alphanumeric plasma display is an 8x32 character matrix capable of displaying data of the ASCII format. A display memory buffer (in the microcomputer memory) is employed such that the static legend data can be overlaid with the dynamic data.

SOFTWARE

The software is written in Intel 8085 assembly language with the present 8K byte version residing in firmware. It was developed using a modular approach in order to facilitate possible format additions in the future. However, it is important to note that format additions would be limited to those which are physically similar to MDDF and LTAS (i.e., 240 bit frames, 2400 baud synchronous).

The software controlling operator keypad interaction was developed with the concept of "user friendliness" in mind. Any valid keypad depressions generate visible indications on the display for operator feedback.

SUMMARY

The Synchronous Data Analyzer gives its user an independent source for checking the validity of raw MDDF and LTAS data. It's ability to produce real-time displays comprised of decoded parameters as well as it's ability to capture several frames for non-real-time display makes it a valuable tool for monitoring and troubleshooting applications involving these data formats. It's composition of portable firmware and mostly commercial hardware makes it a low cost, easily fabricated, product.

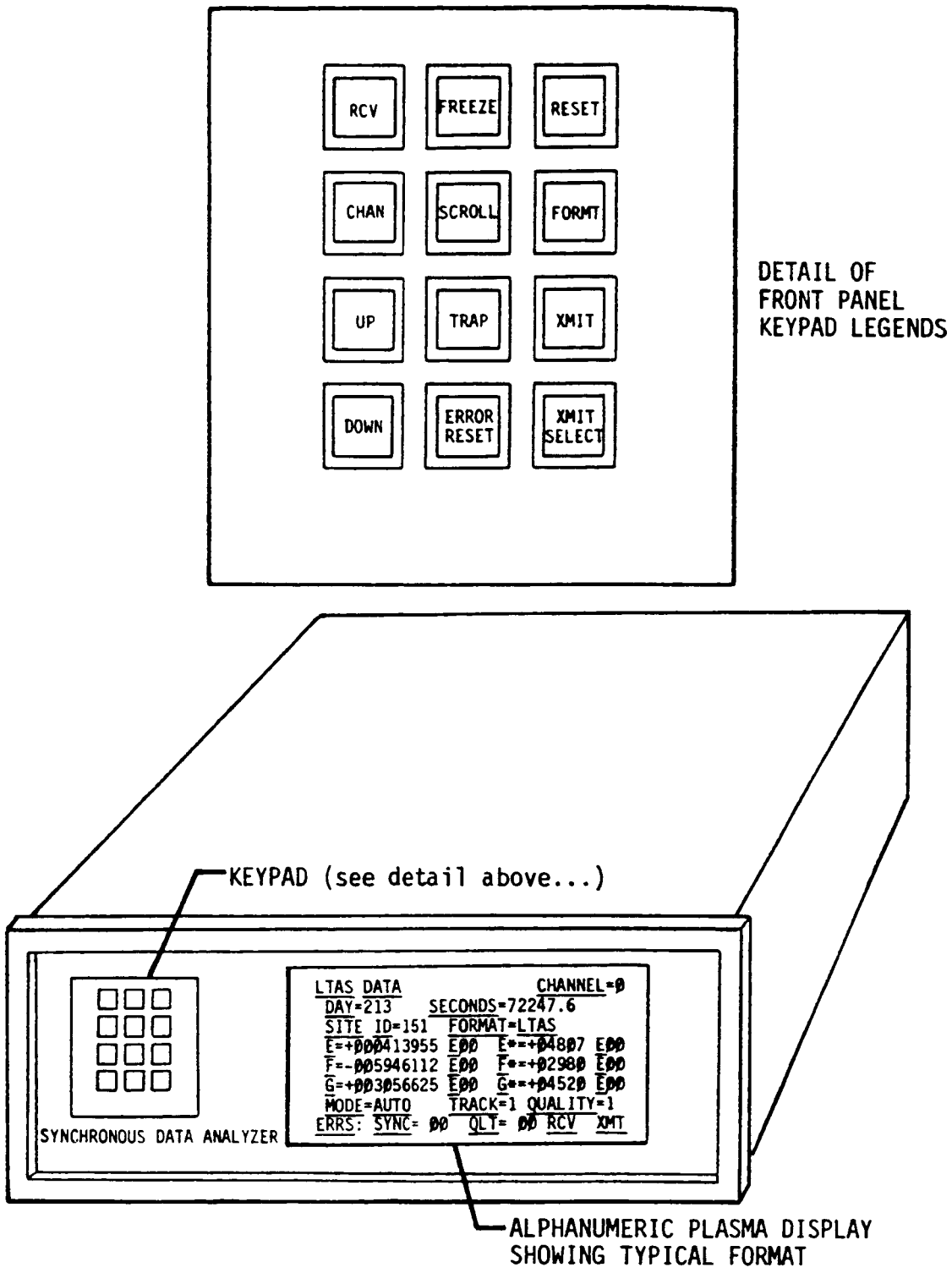

Figure 1.-Synchronous data analyzer unit.

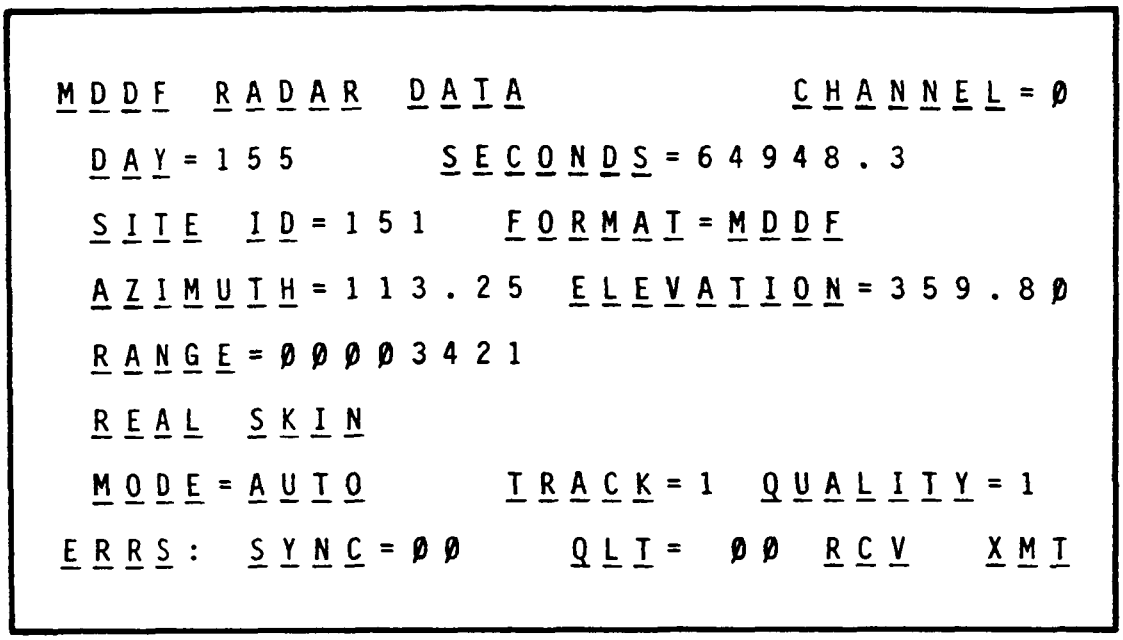

Figure 2.-MDDF display format.

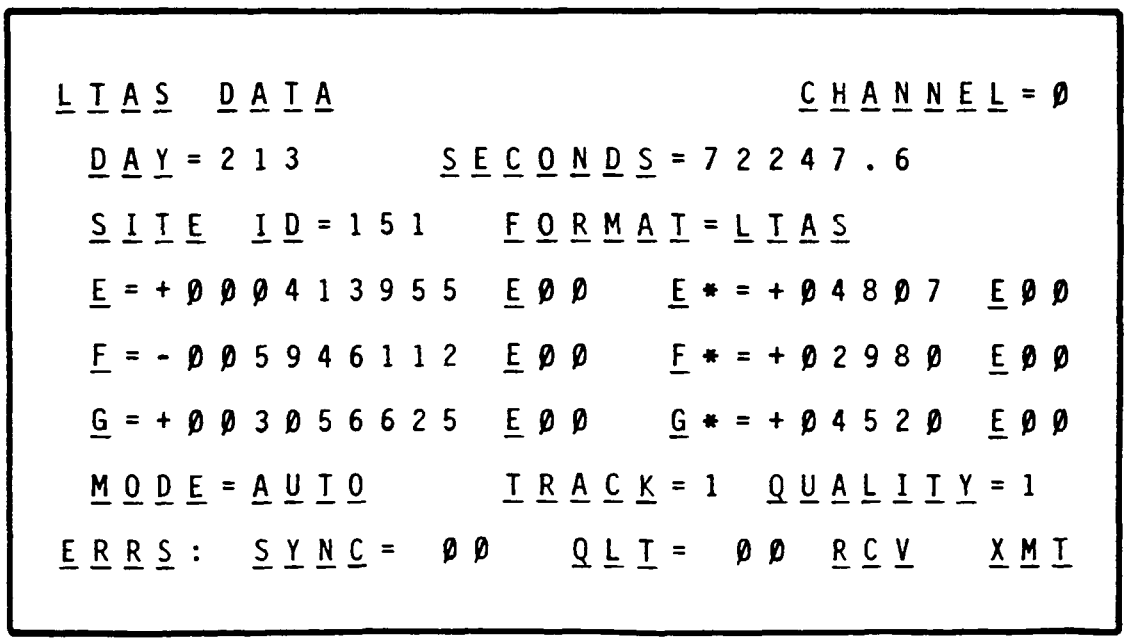

Figure 3.-LTAS display format.

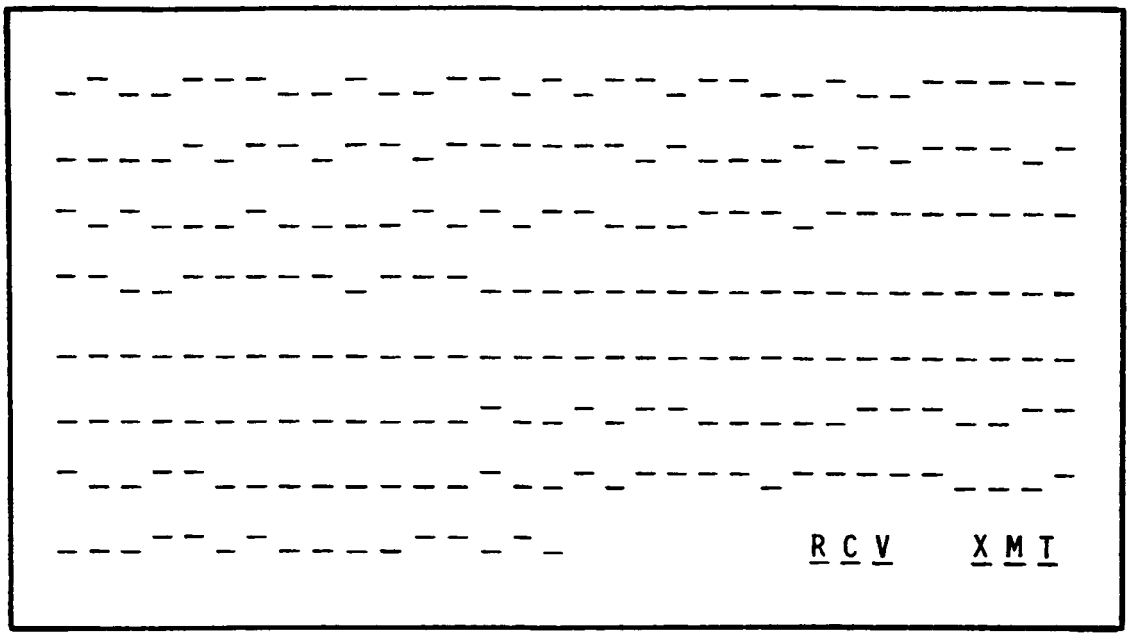

Figure 4.-Binary display format.

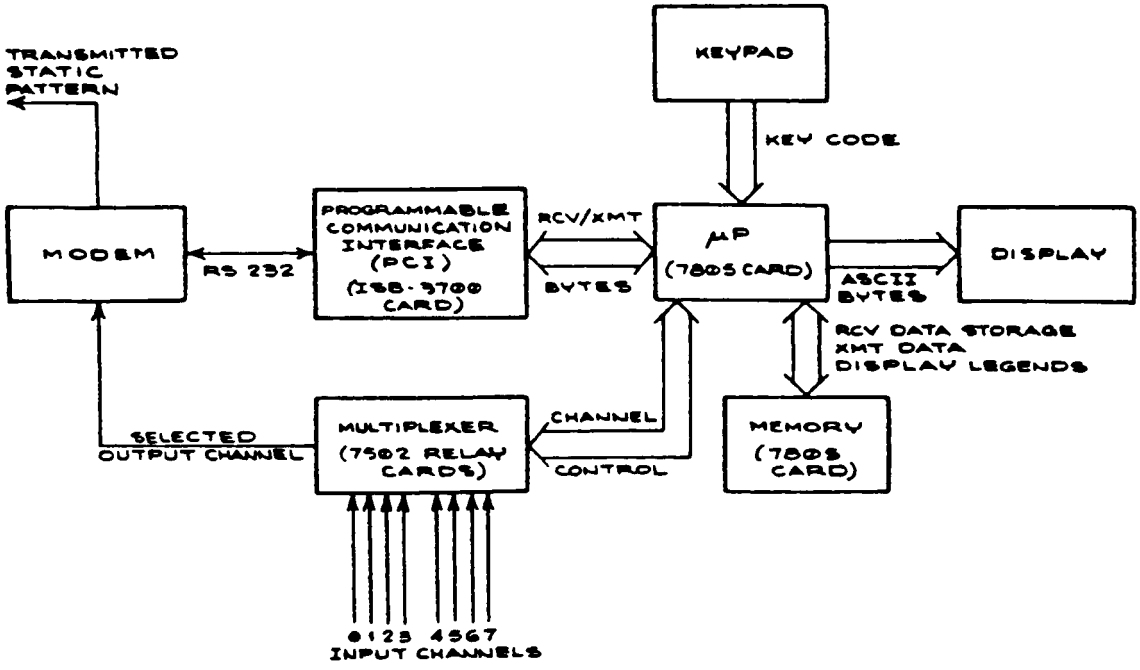

Figure 5.-Synchronous data analyzer unit functional-flow block diagram.

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16. Abstract

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