Surface Inspection - Research and Development

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Abstract

Introduction.

Surface inspection techniques are used for process learning, quality verification, and postmortem analysis in manufacturing for a spectrum of disciplines. We will first summarize trends in surface analysis for integrated circuits, high density interconnection boards, and magnetic disks, emphasizing on-line applications as opposed to off-line or development techniques. We will then look more closely at microcontamination detection from both a patterned defect and a particulate inspection point of view.

Trends in surface analysis

While the critical problem of the week on a given manufacturing line will fluctuate dramatically, taken over time there are at least five types of measurements that are key to yield and productivity today, and which will tend to gate future manufacturing capability. One is pattern inspection of integrated circuits and dense interconnection packages. This is done to verify the pattern back to a software data base, and to un-cover process variations and contaminants that manifest themselves as pattern defects. The second is detection of contamination (particulates and asperities) on monitors and product parts. Particles are the single biggest yield killer in the silicon industry, and they will probably retain that distinction for the near future. The third is metrology in two and three dimensions. This would include linewidths, via sizes, trench aspect ratios, and head dimensions and flying heights. This tests processes like deposition, etching, and lithography overlay, exposure, and development. The fourth is film characteristics such as haze, film thickness, roughness, step coverage, and the presence of contaminating films. The fifth is electrical characteristics, which would include dopant concentration, surface passivation, resistivity (including shorts and opens), and oxide integrity.

Looking at surface inspection in the electronics industry in very general terms, we can assert that inspection will become an area of heightened activity for two reasons. To a large degree due to the influence of Japan (and soon Korea), the learning curves of linewidths, yield, defect density, and other critical parameters against time will probably have to be steeper in the future than their historical trends. Inspection is crucial to allow development and manufacturing the ability to learn how to improve, and to learn quickly. A second reason is that both silicon devices and magnetic disk flying heights are moving into the 0.1 to 1 micron size range; a regime where particles are more abundant and they are much harder to remove from surfaces. If particles are a key yield killer today, they will probably be worse tomorrow.

There are several new specific surface inspection problems that deserve attention.

- Integrated circuits are moving towards designs using high aspect ratio trenches. These might be a micron across and more than five microns deep. How should the profile of these trenches be measured without destroying the parts? How can the presence of contamination in the trenches be detected?

- At the termination of Triology's chip manufacturing stage, Amdahl described one of their key problems as eliminating inter-level shorts in the on-chip multi-level wiring. Insulator opens should be expected to be a problem that will require an appropriate measurement for process feedback and control. Contamination is likely to be a major contributor to insulator failure.

- There is a need for an accurate disposable absolute calibration standard for particle size. The features used to simulate particles should be sufficiently similar to actual contamination that a variety of different detection techniques can use the same standard.

New front end detection techniques

Most of the surface inspection work today is done using variations on optical microscopy, ellipsometry, total integrated scattering, and stylus techniques. There are enhancements and alternatives which could be fruitful.

- Parallel optical processes looks very attractive because of its high information processing rate. InSystems has explored holography for mask inspection. Similar techniques might be applied to opaque surfaces.

- Confocal laser microscopy looks promising for accurate non-contact height and lateral metrology. Heterodyned versions give height sensitivity that is better than typical sensitivities for total integrated scatter techniques.

- The use of evanescent wave illumination for particle detection on monitor surfaces could offer considerable improvements in sensitivity, due to the lack of the reflection interference node at the surface.

- Electron beam techniques will become more common. For example, a thermal technique has been demonstrated in which the surface is heated with a rastered electron beam, and particles on the surface are detected by their subsequent infra-red emission.

Tool development

The decreasing defect densities required for the next VLSI generation imply a parallel increase in processing speed for defect and particulate inspection systems. For example, the number of particles per unit area of size greater than some threshold value goes roughly as the inverse area subtended by that particle. If the sensitivity of a particulate inspection technique goes at some constant ratio of the inspection pixel size to the particle size, and the number of allowable particles or defects per chip stays constant to obtain a given yield, then the bandwidth of the inspection technique should increase as the inverse square of the allowable particle size.

The use of monitor surfaces, such as bare silicon, to measure process induced contamination is not the method of choice. Running monitor wafers uses process tool time. Many deposition and etching steps produce surfaces that are so rough that monitor inspection tooling is relatively insensitive. Particle collection rates depend on the features, composition, and chemical treatment of the surface, and are therefore different between monitors and product.

There are allowable local and global variations in the patterns on the surface due to process variables that should not be flagged as defects. These variations can be, for example, larger than the one tenth ground rules limit. Pattern defect inspection systems need to be locally adaptive to ignore anomalies typical of process variation.

The rule will soon be that inspection systems contain the equivalent of a small main frame computer. In order to retain maintainability of the code, reasonable adaptability of the tools, and acceptable software development costs, the same disciplines that have been developed for large military and commercial software systems should be applied to inspection equipment. Optimally, this would allow more rapid up-grades and diversification of the tool's application.

Research topics

Total integrated scatter is not sufficient to detect particles on rough or highly patterned surfaces. We need to understand better the effect of simple geometries present at a surface on the scattered light field. In particular, this would include a step, an ellipsoid, and a line, all with geometries on the order of the wavelength of light, as a function of the incident angles of the illuminating field, and as a function of the roughness and composition of the features and the surrounding surface.

Along the same lines, the inverse scattering problem needs attention; namely, under what conditions can the observed light scatter field be used to infer the structure or composition of the scattering object? What are the critical components of the scattered light field that can be used to determine characteristics of the scattering feature?

There are a host of electronic and optical parallel processing schemes that might be applied to defect detection. Are any of these particularly applicable? Are there alternative algorithms to those in use today that would particularly suite one of these architectures?

SENSORS DEVELOPED FOR IN-PROCESS THERMAL SENSING AND IMAGING*

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As large-scale integration requires smaller geometry and larger chip size, fabrication process control becomes more stringent and thus reliable and efficient process evaluation during wafer processing becomes more important. Among various evaluation methods, non-contact non-destructive techniques including thermal and optical methods have been of our particular interest. Temperature profiles can be used to provide a diagnostic tool for in situ process control and to find optimal process conditions. Optical methods can provide material and process characterizing information such as thin-film thickness and quality, carrier concentration, or content of contaminants [1-4].

Although a variety of sensors are available in association with these non-contact methods, infrared detectors are attractive since they can be used for both methods. Most of infrared detectors can be classified into two major categories: photon-type and thermal-type detectors. A thermopile, a type of thermal-type detector, was chosen for our research due to the following reasons. A thermopile can respond from ultraviolet to far-infrared and its sensitivity is almost flat over this region. It can be also operated over a relatively wide range of ambient temperatures as well as at room temperature. Unlike a pyroelectric detector, this detector exhibits a stable response to DC radiant signal and, if appropriately designed, it can show a wide dynamic operating range. These factors are particularly significant for an in situ process or material evaluation system; process-related signals are typically slow-varying and have a broad range of signal levels, and the corresponding sensors may have to be reliably operated at various ambient temperatures.

Compared with conventional thin-film thermopiles, the thermopile we have proposed [5] uses silicon as a substrate material which should have a high thermal conductivity to sink heat effectively. PolySi is used as a major thermoelectric material and gold is used essentially as an interconnecting material to form a thermopile structure. Another important aspect is use of dielectric diaphragm to support the thermopile. Since SiO_2 and Si_3N_4 are relatively high in thermal resistance, a diaphragm formed by a combination of these films can provide an effective thermal isolation between the hot junction and cold junction regions in the thermopile.

Figure 1 shows a photograph of the silicon-based thermopile chip and a schematic cross-sectional structure of the detector. To realize this thermopile, silicon micromachining was cooperated with conventional IC process technology. Since this fabrication process is particularly compatible with standard MOS process, this approach has the potential to contain on-chip signal conditioning and processing circuitry. This aspect becomes particularly significant for detector arrays. It is desirable for an array to have on-chip

readout capability, which will much simplify the whole system and help the system less plagued by noise pickup.

A detector array is useful and demanding to obtain such information as distributions or profiles of certain physical properties. Some examples include temperature profile or uniformity in carrier concentration or film thickness. For such applications, a 32-element linear thermopile array has been designed and successfully fabricated.

Figure 2 shows the linear thermopile array fabricated on a silicon substrate. This array consists of two 16-element linear subarrays and the two subarrays are staggered to each other to improve array spatial resolution. A second subarray collects the radiative signal incident onto the inactive rims between the detector elements in a primary subarray when the whole array is scanned in a direction perpendicular to the linear arrays. A proper time-delay compensation should be determined by the scanning speed and the distance between the two subarrays.

Each thermopile element consists of 40-junction polySi-Au thermocouples and is supported on a rectangular dielectric diaphragm window. The diaphragm window has a dimension of 0.4 mm x 0.8 mm and the diaphragm is 1.3 μm thick. Each thermopile element is separated by a 20μm-thick, heavily-boron-doped silicon rim, which also supports the cold junctions in each thermopile.

Another important aspect of this array is use of on-chip analog multiplexers. There are two 16-channel analog multiplexers and each multiplexer converts 16 parallel outputs from each detector subarray into a serial output. Thus there are only two output nodes required, compared with 32 output nodes without multiplexing. This advantage becomes more significant if the number of detector elements is larger. Each analog multiplexer consists of a NOR-type decoder having 4 control inputs and 16 MOS-type switches.

This array was mounted on a dual-in-line package and was coated with carbon blacks to characterize its optical and electrical performance. Typical detector responsivity in an array ranges from 65 V/W to 80 V/W and their detectivity ranges from 3.6 cm$\sqrt{\text{Hz}}$/W to 4.6 cm$\sqrt{\text{Hz}}$/W. Nonuniformity in detector responsivity in an array was less than 10 % and interelement cross-talk was less than 3 %. Their response time is distributed between 7 msec to 12 msec when blacks were coated.

A theoretical performance was evaluated for a thermal imaging system using this array while a practical system is under construction. Assuming a typical scanning-mode system which has a Gaussian modulation transfer function (MTF), the assumed system exhibits a noise equivalent temperature difference (NETD) of 0.6 ° C and a minimum resolvable temperature difference (MRTD) of 0.9 ° C at a spatial frequency of 0.2 cycles/mrad. Although this result is reasonably moderate, the imaging performance of such a system could be improved significantly since thermopile detectivity can be further improved and signal pass-band can be further limited in most practical cases associated with process monitoring and evaluation.

On the other hand, this type of array is being considered to be used for laser-based infrared analysis. For example, using a CO_2 laser as a radiation source and measuring infrared absorption or reflection, film thickness or carrier concentration profiles throughout a wafer could be evaluated [6].

As a conclusion, a monolithic thermopile infrared detector array has been developed using conventional MOS technology and micromachining, and this type of array has a potential to be used for an inexpensive non-contact in situ process evaluation system.

ACKNOWLEDGEMENT

REFERENCES

[1] L. A. Murray and N. Goldsmith, "Nondestructive Determination of Thickness and Perfection of Silica Films," *J. Electrochem. Soc.*, vol. 113, no. 12, pp. 1297-1300, December 1966.

[2] L. Jastrzeske, J. Lagowski, and H. C. Gatos, "Quantitative Determination of the Carrier Concentration Distribution in Semiconductors by Scanning IR Absorption: Si," *J. Electrochem. Soc.*, vol. 126, no. 2, pp. 260-263, February 1979.

[3] T. Motooka, T. Warabisako, T. Tokuyama, and T. Watanabe, "Optical Measurement of Carrier Profiles in Silicon," *J. Electrochem. Soc.*, vol. 131, no. 2, pp. 174-179, January 1984.

[4] P. Stallhofer and D. Huber, "Oxygen and Carbon Measurements on Silicon Slices by the IR Method," *Solid State Technology*, vol. 26, no. 11, pp. 233-237, November 1983.

[5] I. H. Choi and K. D. Wise, "A Silicon-Thermopile-Based Infrared Sensing Array for use in Automated Manufacturing," *IEEE Tran. Electron Devices*, vol. ED-33, no. 1, pp. 72-79, January 1986.

[6] G. E. Crook and B. G. Streetman, "Laser-Based Structure Studies of Silicon and Gallium Arsenide," *IEEE Circuits and Devices Magazine*, vol. 2, no. 1, pp. 25-31, January 1986.
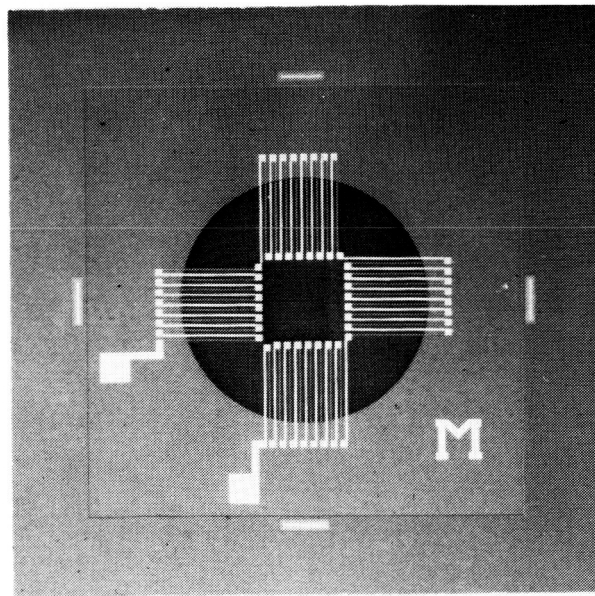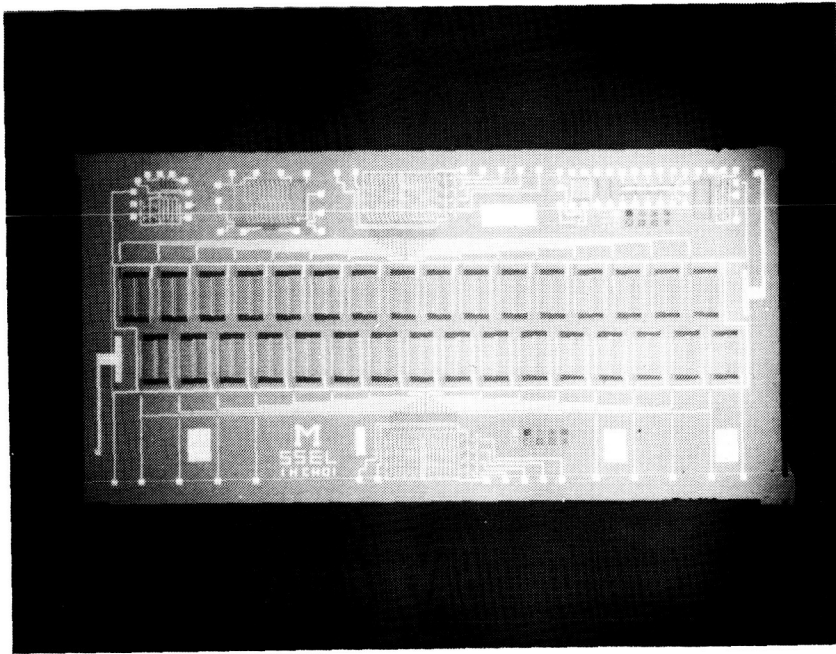
(a) A 32-junction polySi-Au thermopile detector based on a Si substrate. The chip size is 3.6 mm x 3.6 mm.
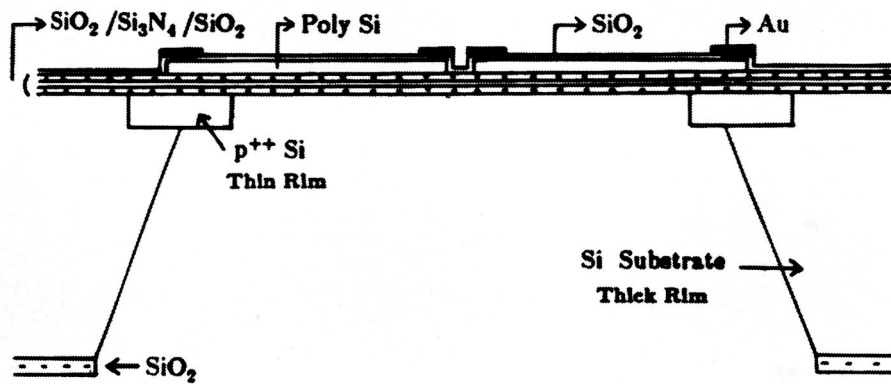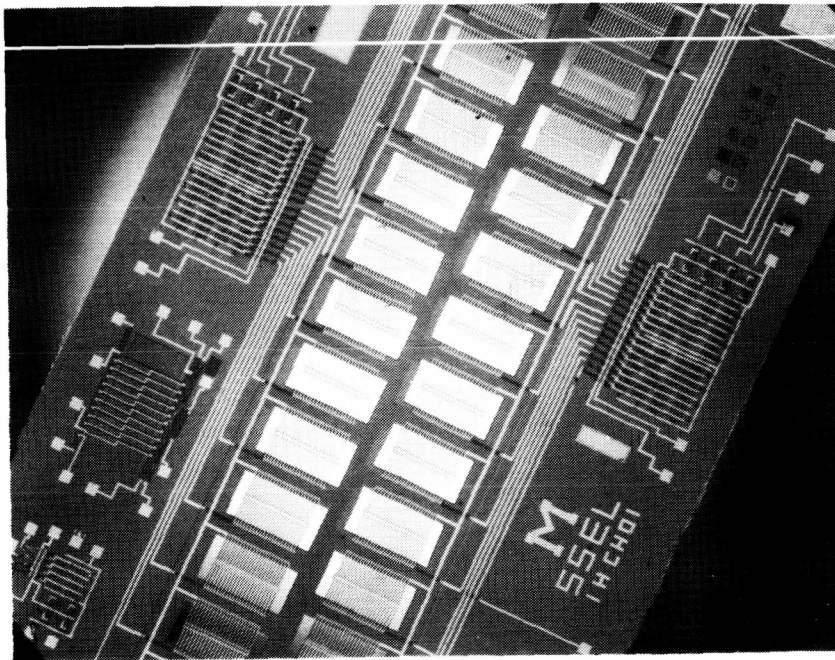

(b) A schematic diagram of the thermopile cross-sectional structure.

Figure 1

(a) A 32-element thermopile linear array containing two on-chip analog multiplexers. The chip size is 11 mm x 5.5 mm.

(b) A close-up view of the monolithic array. Each thermopile element is supported on a 0.4 mm x 0.8 mm diaphragm window.

Figure 2