A VHSIC GENERAL PURPOSE PROCESSOR

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INTERNATIONAL TRAFFIC IN ARMS REGULATIONS
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BENEFITS TO NASA DATA SYSTEMS PROGRAM

THE VHSIC PROGRAM OFFERS NASA AND ITS CONTRACTORS ASSURED AVAILABILITY OF MIL-SPEC EMBEDDED COMPUTER COMPONENTS AND INTEGRATING CAD/CAE AND SOFTWARE DEVELOPMENT SUPPORT TO GIVE LOW SYSTEM LIFE COSTS FOR DATA MANAGEMENT SYSTEM ON SPACE STATION AND EOS.

SUMMARY

THIS TALK WILL BRIEFLY REVIEW PROGRESS, TO DATE, BOTH IN THE DoD VHSIC PROGRAM AND IN THE NASA VHSIC RELATED INSERTION DEVELOPMENT OF A GENERAL PURPOSE PROCESSOR.

TOPICS:

LONG TERM OBJECTIVE OF LARC PROGRAM

RELATED PROGRAMS

APPROACH

RESULTS AND ACCOMPLISHMENTS

RELATIONSHIP TO NASA PROGRAMS

LONG TERM PLANS

SHORT TERM PLANS

SUMMARY

LONG TERM OBJECTIVES:

OAST PROGRAM:

TO CO-DEVELOP WITH THE DoD VHSIC PROGRAM A GENERAL PURPOSE HIGH DATA RATE SIGNAL PROCESSOR AND THE ACCOMPANYING HANDS ON TECHNOLOGY BASE INCLUDING CAD/CAM SYSTEM AND SOFTWARE DEVELOPMENT TOOLS SUITABLE FOR CORE SUBSYSTEM PROCESSING REQUIREMENTS.

SPACE STATION:

TO DELIVER VHSIC TECHNOLOGY TO THE SPACE STATION PROJECT AS A TECHNOLOGY FOR INSERTION INTO IOC; TO DEMONSTRATE READINESS BY A SET OF INTERLOCKING STUDIES WITH BRASSBOARD DEMONSTRATION; TO INSERT THIS TECHNOLOGY INTO SPACE STATION DATA MANAGEMENT SYSTEM TEST BED; TO USE THIS INSERTION TO LEARN HOW TO UPGRADE DMS TO FOC.

EOS:

TO DELIVER VHSIC TECHNOLOGY TO THE EOS COMMUNITY OF USERS AS A TECHNOLOGY FOR IMPLEMENTATION OF ONBOARD PROCESSING ELEMENTS FOR HIGH DATA RATE SENSORS.

IMPORTANCE OF PROBLEM

- NASA MUST ASSURE A HIGH RELIABILITY LONG LIFETIME COMPONENT TECHNOLOGY FOR ITS MISSIONS AND MUST HAVE A TECHNICALLY AGGRESSIVE POSTURE IN DEALING WITH ITS SYSTEMS CONTRACTORS.

- THE DoD RECOGNIZED THIS NEED IN 1979 AND IS CAPITALIZING THEIR WEAPONS SYSTEMS CONTRACTORS WITH THE TECHNOLOGIES OF SYSTEM INTEGRATION, IC DESIGN, FABRICATION, AND TEST TO MEET THEIR EMBEDDED SYSTEM NEEDS, AND ARE ALLOWING THEIR CONTRACTORS TO VERTICALLY INTEGRATE THEIR WEAPONS SYSTEMS DEVELOPMENTS.

- NASA SHOULD PARTICIPATE AND LEVERAGE AGAINST THE DoD TO ASSURE THAT ITS LONG TERM NEEDS ARE MET, SINCE NASA AND THE DoD SHARE CONTRACTORS ON MAJOR SYSTEMS BUILDS.

RELATED R&D

DoD VHSIC PROGRAM

- PHASE 1, HALF OF CONTRACTORS COMPLETE
  ALL CONTRACTORS IN FIELD ENHANCEMENT
- PHASE 2, THREE CONTRACTS AWARDED
  ALL ORGANIZING
  FIRST CHIP FROM EACH CONTRACTOR, COMMON BIU
- AF VHSIC 1750A GPC AT TRW/WESTINGHOUSE

NASA INSERTION ACTIVITIES

- WORK REPORTED HERE
- JPL MAX ARCHITECTURE
- AMES AI PROCESSOR

ENHANCED CAPABILITY OF EMBEDDED PROCESSING

- VHSIC SPEED AND POWER ENHANCEMENTS NECESSARY TO ACCOMMODATE INITIAL ADA INEFFICIENCIES
- LONG TERM DoD INVESTMENT/COMMITMENT
  - LONG TERM CONTINUING AVAILABILITY OF MIL-SPEC QUALIFIED COMPONENTS
- LOW SYSTEM LIFE/PROGRAMMING COSTS
  - BUILT IN TEST TO CHIP LEVEL TO FACILITATE MAINTAINABILITY
  - HARDWARE DESCRIPTIVE LANGUAGE TO FACILITATE HARDWARE FUNCTIONAL UPGRADABILITY
  - ADA LANGUAGE ACCOMMODATION
- POTENTIAL FOR SPACE QUALIFICATION

TECHNICAL APPROACH

- TO GENERATE VHSIC PROCESSOR SYSTEMS CONCEPTS EMBODYING DIRECTED GRAPHS AND PETRI NETS TO ALLOW QUASI STATIC REPARTITIONING OF HIERARCHICAL PROCESSOR TOPOLOGIES TO ACCOMMODATE HIGH PERFORMANCE DATA DRIVEN REQUIREMENTS IN THE SAME CONFIGURATION AS REDUNDANT, SELF-CHECKING, SELF-TESTABLE SYSTEM REQUIREMENTS.

- TO PROVE CONCEPTS IN LABORATORY ENVIRONMENT FOR USER FRIENDLY HARDWARE INSERTION/PLANNED SCARRING IN IOC AND FOC SPACE STATION SUBSYSTEMS.

- TO DETERMINE FEASIBILITY OF FLYING SUCH A SYSTEM TO EVALUATE SEU PERFORMANCE IN OPERATING ENVIRONMENT.

- TO INTEGRATE INTO TEST BEDS TO FACILITATE DMS SYSTEM INTEGRATION AND DEVELOPMENT OF SCARRING CONCEPTS.

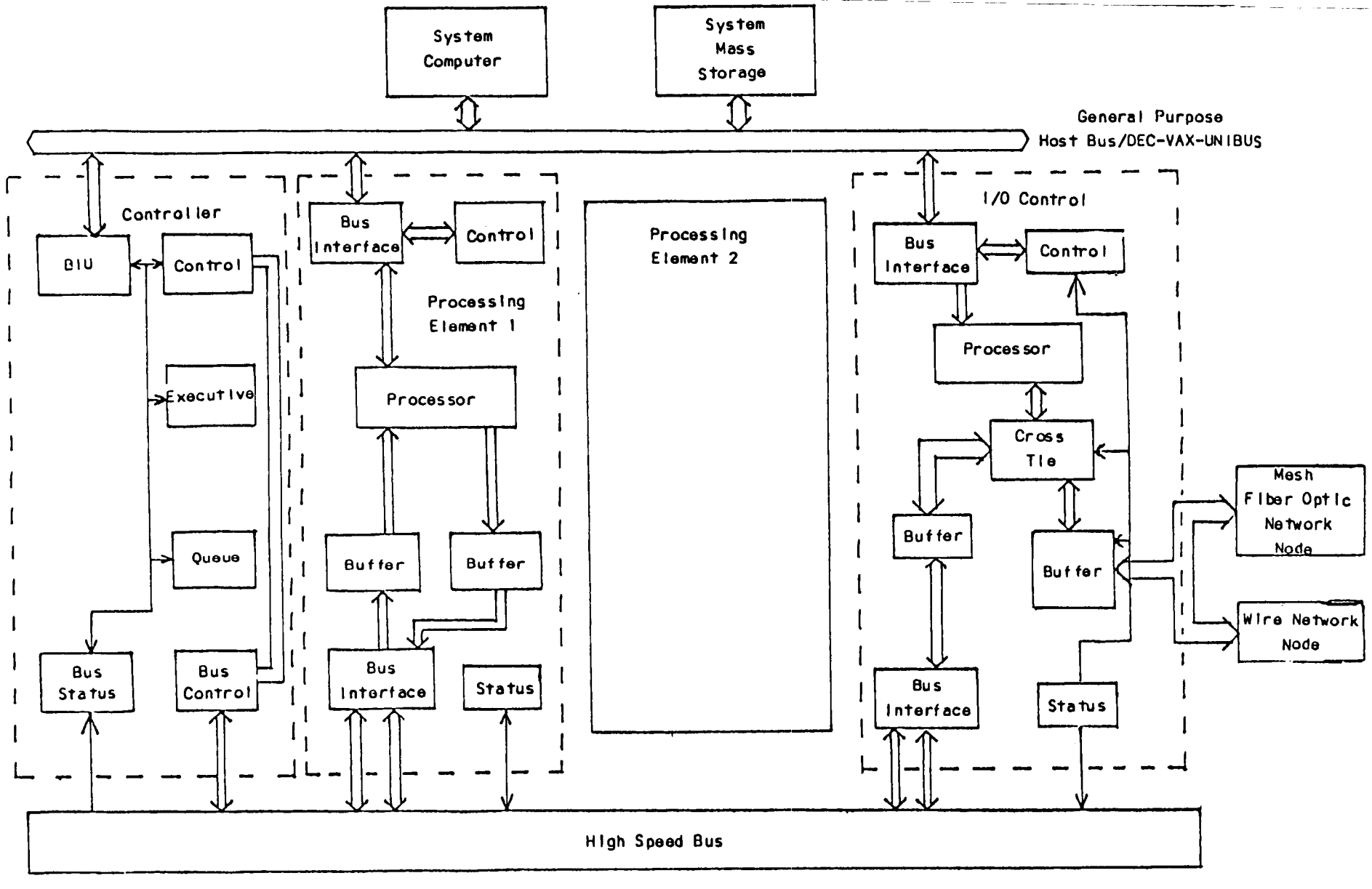


Fig. 1. High-Speed Processor

SUBSYSTEM TARGETS

HARDWARE

VHSIC SPACE STATION GP BRASSBOARD

- PARTITIONED SUBSYSTEM OF LARGER ARRAY
- 10 VHSIC CHIPS EXCLUSIVE OF MEMORY
- 3-5 MIPS DAIS
- 15-50 WATTS
- HIGH-SPEED INPUT/OUTPUT NODE
- INTEGRABLE INTO SPACE STATION DATA MANAGEMENT SYSTEM TEST BED

EXERCISER

- CONVENTIONAL MINICOMPUTER HOSTING COMPILERS, HARDWARE AND SOFTWARE DIAGNOSTICS, AND PROGRAM DEVELOPMENT TOOLS

SOFTWARE

- ADA (OR PASCAL) COMPILER RESIDENT ON MINICOMPUTER HOST
- EXECUTION OF SINGLE STRING PROGRAMS ON SUBSYSTEMS, INCLUDING CLASS II PROCESSING
- 1750A OR 1862 INSTRUCTION SET ARCHITECTURE WITH CONTROLLED USE OF XOP'S
- STAND ALONE OPERATION
- PROVISIONS FOR EXTENDED ARRAY SOFTWARE

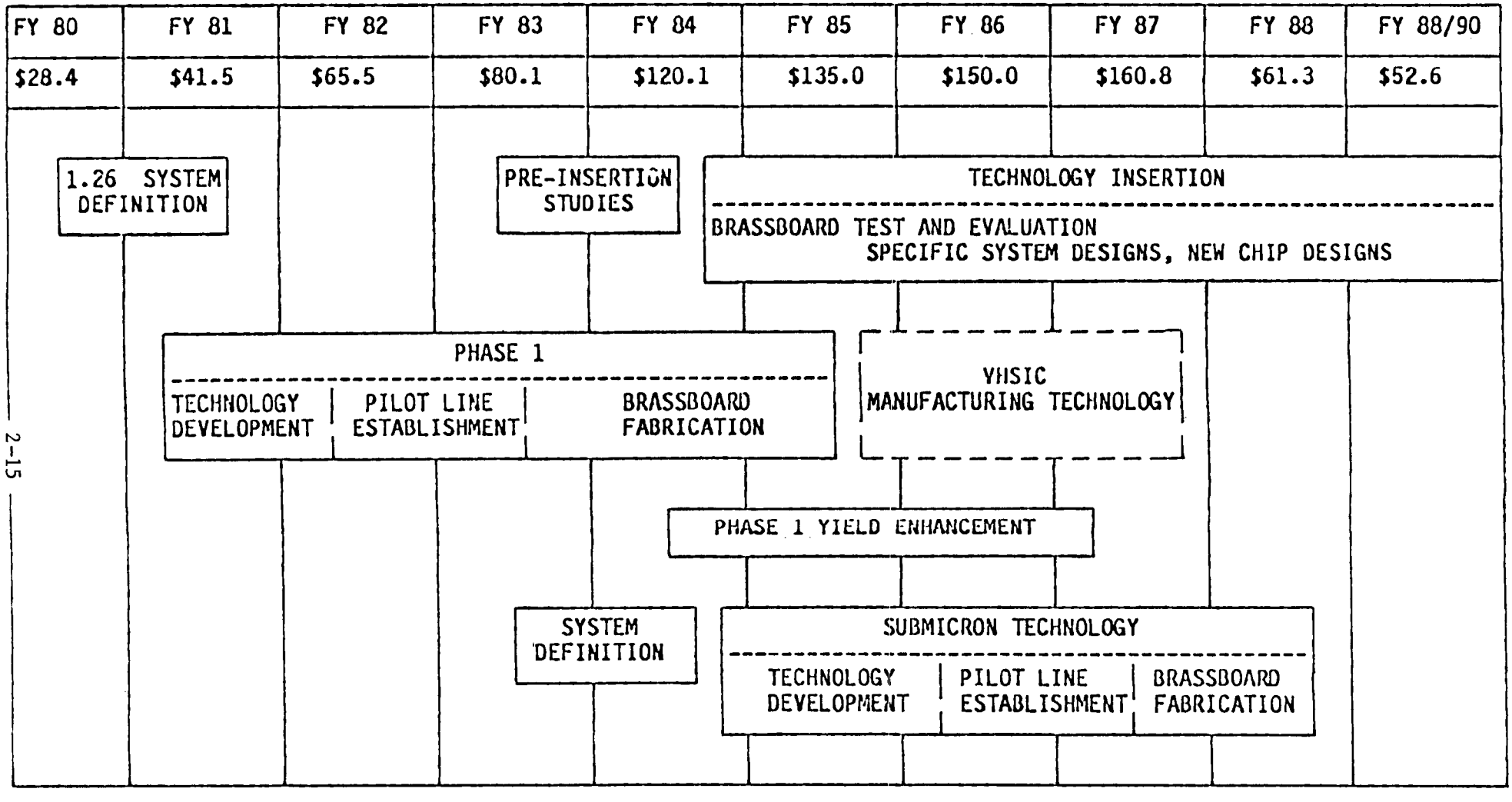
'85 ACCOMPLISHMENTS TO DATE

- FIRST LEVEL DGM TOOLS UP AND RUNNING ON IAS-VAX
  - NOT USER FRIENDLY
  - 2 GRAPH USERS TO WORKSHOP, 1 PROGRAMMER TO ADA SCHOOL
- PROCESSOR STUDY AT WESTINGHOUSE
  - INITIAL CONFIGURATION
  - CONCEPT FOR ASYNCHRONOUS TRIPLEX TASK DISPATCHMENT
  - OPERATING SYSTEM MODELING
  - CONCEPTS EMBODIED IN AF 1750A AWARD TO TRW/WESTINGHOUSE
- EOS INSERTION STUDY
  - 100^{+} INSTRUMENTS SURVEYED
  - 24 INSERTION CANDIDATES IDENTIFIED AND MAPPED TO BRASSBOARDS
  - DRAFT REPORT IN APPROVAL CYCLE
  - 3 INTERCENTER BRIEFINGS GIVEN
- BACK UP PROCESSOR FROM TI CONTRACTED WITH ARMY
- BACK UP CONFIGURATION MODELING CONTRACTED WITH RTI, ADAS-TI
- VHSIC WORKSHOP AT JSC IN NOVEMBER
- LARC DECISION TO IMS INVESTMENT IN CAD/CAM
- VHSIC COMPATIBLE HW TO FACILITATE "HANDS ON" IN PROCUREMENT
- FLIGHT EXPERIMENT IDENTIFIED FOR DATA SYSTEM TO SS-TDAG
- SELF-TESTABLE 1750A DESIGN SBIR PROGRAM COMPLETED PHASE I, PHASE II AWARDED

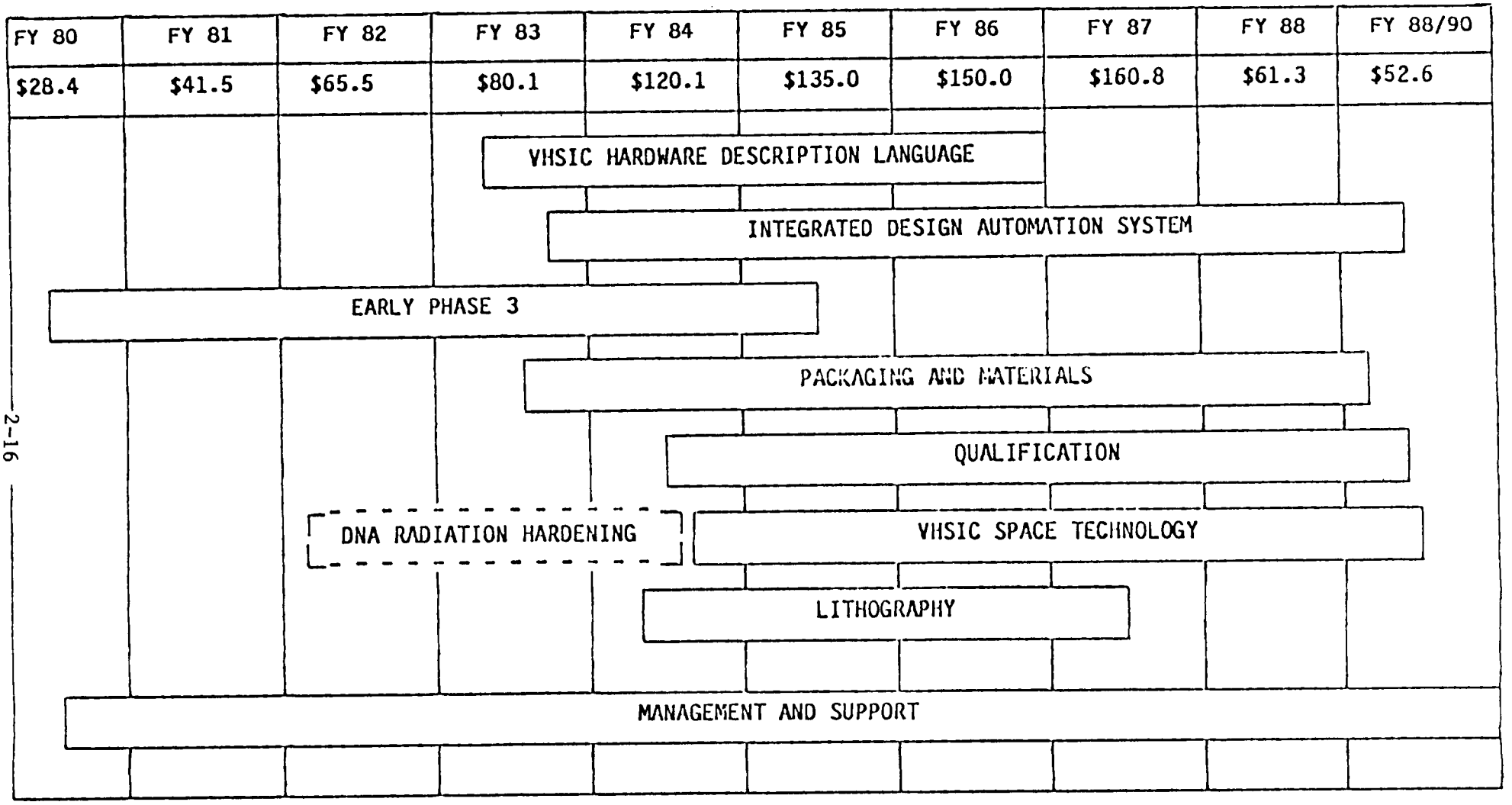
EXPECTED DURING BALANCE OF '85

- COMPLETION OF WESTINGHOUSE AND NICHOLS STUDIES
  - SIMULATION OF 4 PROCESSOR CONTROLLER CONFIGURATION
  - PROJECTION OF IMPLEMENTATION COSTS FOR FULL UP SYSTEM
  - INITIATION OF OPERATING SYSTEM FOR M OF N FAULT DETECTION
- FIRST VHSIC COMPATIBLE HARDWARE IN-HOUSE AND OPERATING (FAIRCHILD 9450 CHIPSET IN AVIONICS BRASSBOARD)
- ADVOCACY AND PLAN FOR RAD TOLERANT EOS PROCESSOR DEVELOPMENT
- DEFINED ROLE IN VHSIC 1750A SPACE TECHNOLOGY PROGRAM

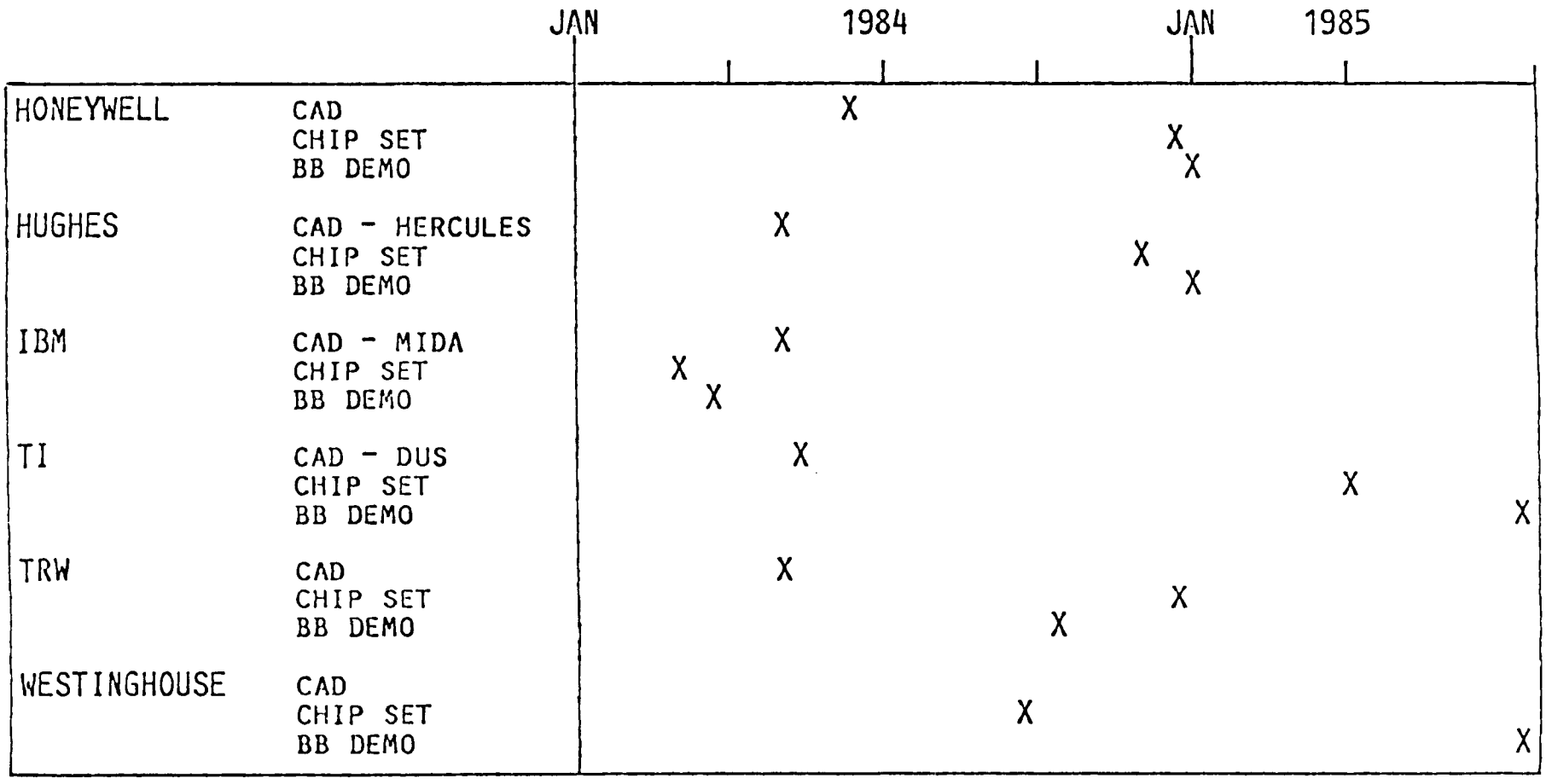
VHSIC PROGRAM ROAD MAP



VHSIC PROGRAM ROAD MAP
(CONTINUED)



MAJOR MILESTONES FOR PHASE I



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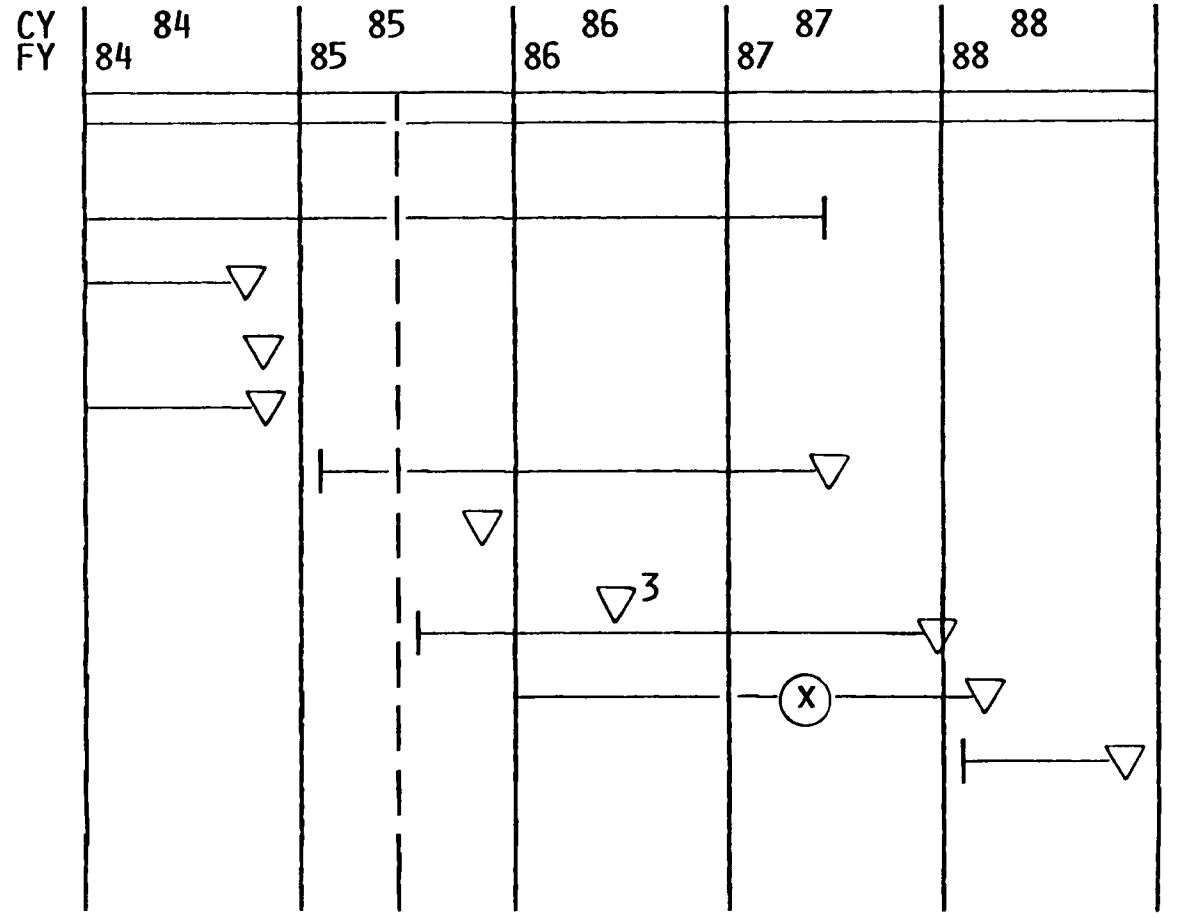

[1]ASSUMING NASA/DOD MOU ACTIVITY

[2]AS PART OF ONGOING DOD PROGRAM

[3]TECHNOLOGY IS FROZEN HERE

(X) INTERIM TEST DATA AVAILABLE

[4]STUDY RESULTS AVAILABLE JULY 84, IN DRAFT FORM

RESOURCES: FY	83	84	85	86	87	88
R&D	200	400 (180)	560 (100)	2000	2000	2000
MP	2	3	5	10	10	10

LONG TERM PLANS

COMPLETE AND INSERT PROCESSOR SUBSYSTEM INTO SS DMS TEST BED
BY C/D PDR

DEVELOP POTENTIAL SCARRING METHODS FOR BOTH HARDWARE AND SOFTWARE
BY C/D PDR

EXAMINE FEASIBILITY OF SCARRING HARDWARE THROUGH POTENTIAL FOC TEST BED
BY C/D CDR

EXAMINE POTENTIAL OF DEVELOPMENT OF VHSIC SPACE PROCESSOR WITH DoD AND EOS FOR IMPLEMENTATION IN 1990'S

PLAN FOR VHSIC II UPGRADES INTO NASA SYSTEMS BY MID 90'S

SUMMARY

- REVIEW PROGRESS
- PROGRESS INDICATES SUCCESS