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MAX

A SPACE STATION COMPUTER OPTION

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General Purpose Space Computing

- Typified by most
  - engineering subsystems
  - payloads
  - other "intelligent" devices
- Specifically excludes
  - top end, special-purpose signal processors
  - low end, in-circuit μ-processor applications

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CHARACTERIZED BY

- Embedded, real-time applications
- Both synchronous, cyclic operation and asynchronous, event driven operation
- Both computationally intensive (e.g. signal processing, guidance) and data intensive (e.g. command and telemetry) processing
- Wide range of throughput and memory requirements
- Range of fault tolerance requirements from none to full, uninterruptable operation through faults or damage
- Maintainability, including capability for on-line substitution in critical systems

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MAX HARDWARE FEATURES

- General purpose computer module
  - Small, light weight, & low power
  - Radiation hard & single event upset immune
  - ≈ 1 Million Whetstone equivalent instructions per second (floating point)
  - 256 Kbytes (expandable) memory
  - High speed communication ports & memory mapped I/O
  - Global semaphore capability without shared memory

- Special features support
  - Multi-computer concurrency
  - Software implemented fault tolerance
  - Spatial distribution for damage tolerance

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MAX SOFTWARE FEATURES

- Conventional programming and test environments
- Layered software design supporting
  - high level languages
  - real time, multi-tasking & task migration
  - packet communication
  - data management
  - concurrency
  - fault tolerance
- Optional low resolution data-flow concurrency support

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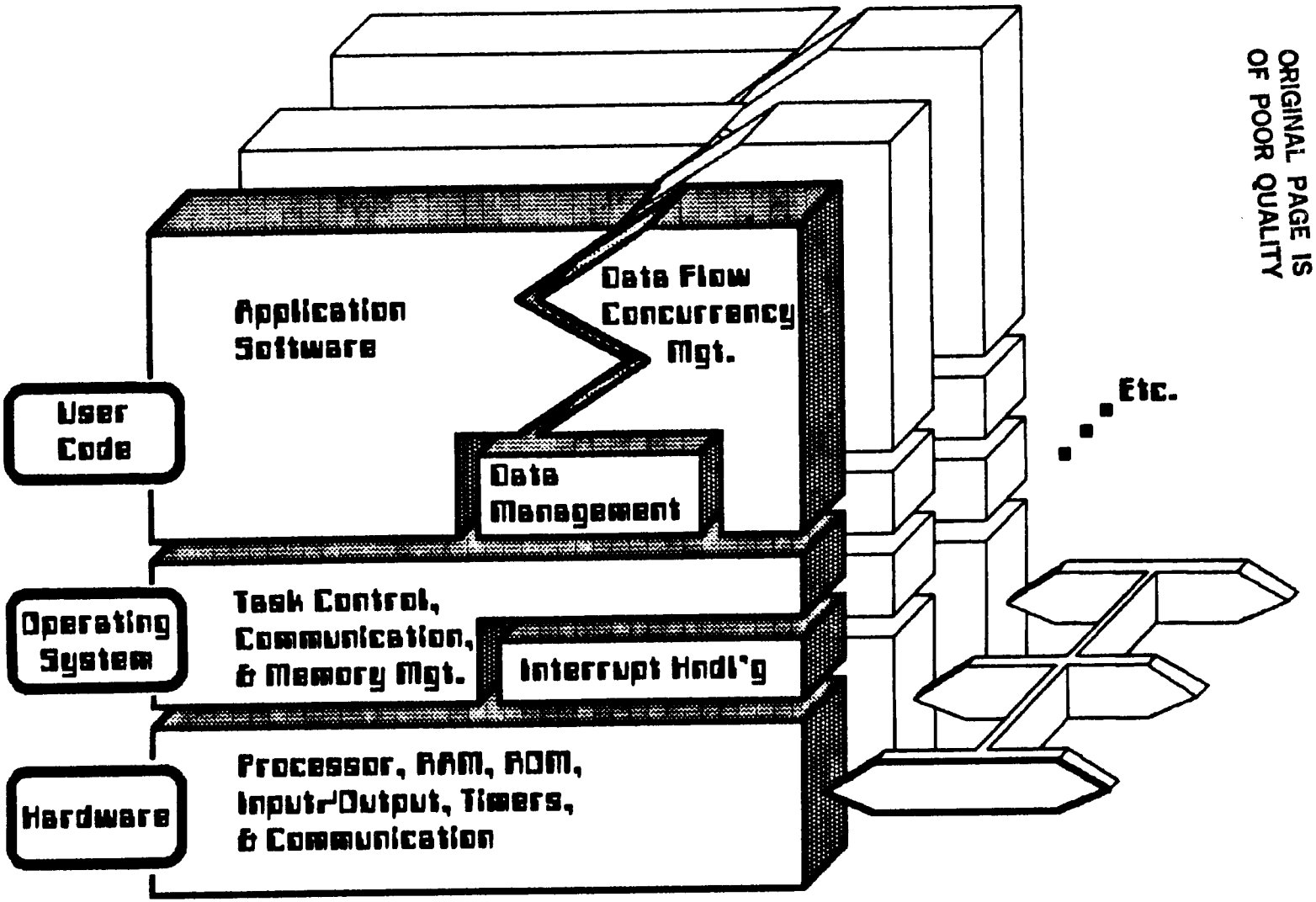
MAX LAYERED ARCHITECTURE



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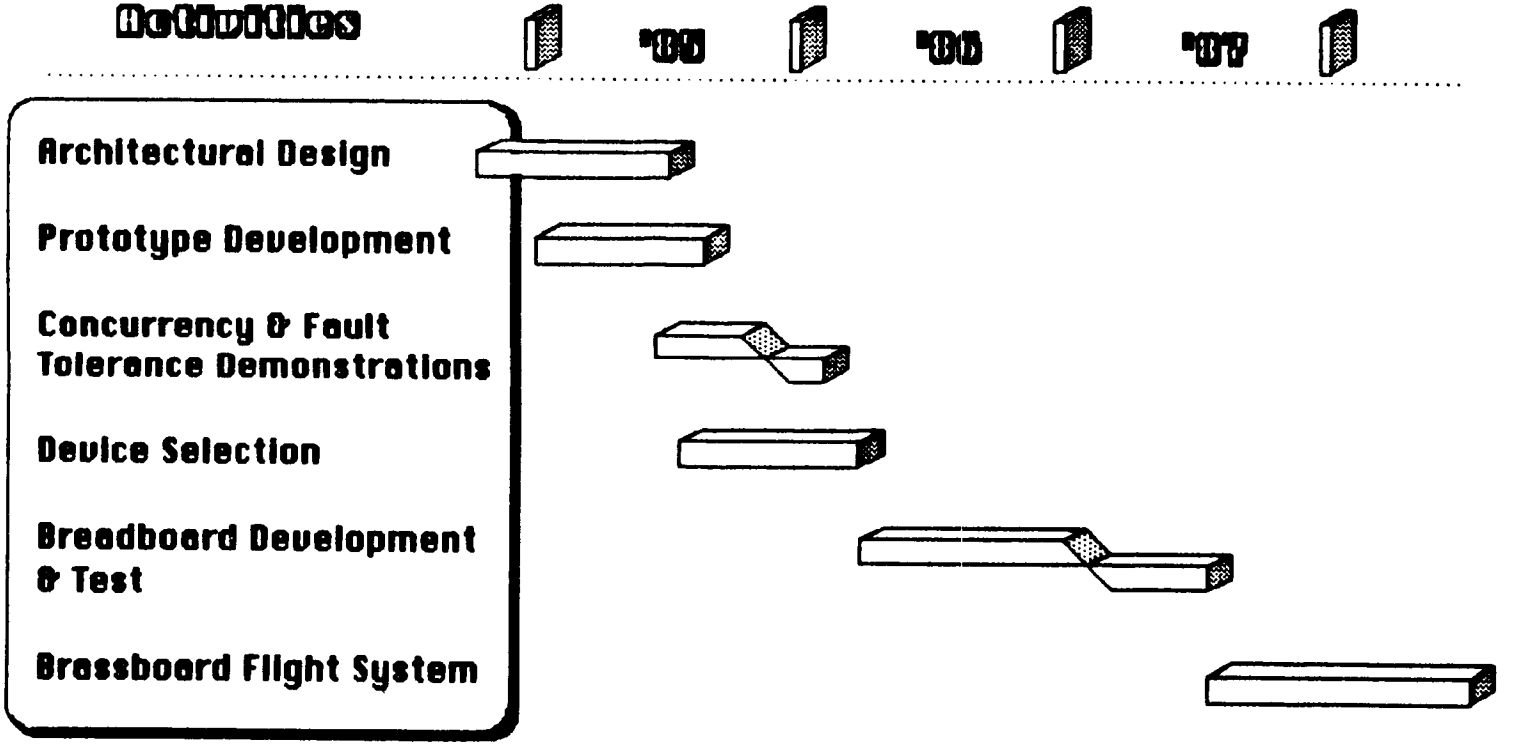
MAX DEVELOPMENT PLAN



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IMPLEMENTATION OPTIONS

- Low power bipolar devices are susceptible to single event upset
- Preferred device technology is CMOS
  - High density CMOS is fast, but low power
  - Can be made single event upset immune
- Existing CMOS part sets include
  - EPIC bit-slice family & related parts
  - 2900 family bit-slice component emulations
  - Custom standard cell and gate array components
  - 8085, 80C86 and 1802 μ-processors (& selected peripheral parts)
  - Memory components
- Comparable VHSIC components in development

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PROMISING NEW ARRIVAL

- 2 micron (10-15 MHz) CMOS emulation of National Series 32000™ and supporting devices by Sandia National Laboratories
  - 32032 and 32016 µ-processors
  - 32081 Floating Foint Unit
  - 32201 Timing Control Unit
  - 32202 Interrupt Control Unit (plus timers & I/O)
  - 8K×8 static RAM, 32K×8 ROM, 32K×8 EEPROM, & non-volitile RAM
  - 1K (and 2.5K -10K ?) gate array
  - Standard cells (up to 30,000 transisters per chip)
  - Miscellaneous glue chips (buffer, latch, decoder, byte I/O,...)
  - Bus arbiter & DMA controller under consideration
- Replacement compatible with commercial versions

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ADVANTAGES

- Prototyping can begin now with commercial parts
- Throughput comparable to VAX-11/750 (≈ 1 MIPS)
- Modern architecture explicitly and efficiently supporting
  - modular programming
  - complex data structures
  - structured language control flow, etc...

  Result» lower cost, more compact, more reliable code
- Small chip count and small physical size
- Clean support for custom slave processors
- Wide range of commercially available support tools
- Potential direct path to subsequent VHSIC level integration (NSC is a VHSIC phase I subcontractor to WEC)

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RADIATION HARDNESS

- Total dose hardness of 1×10^6 Rads (Si)
- No upset to 1×10^9 Rads (Si) /sec
- No upset from 140 MeV Krypton, any angle

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SANDIA DEVELOPMENT PLAN

- NSC enthusiastic and involved in program (contract not yet signed as of March 85)
- Engineering samples of 32016 and all other components (except 32032) available by fourth quarter of 1988
- 32032 available by second quarter 1989
- Six months from engineering samples to production quantities
- JPL considering test & qualification of commercial parts (both NSC & second source TI) for acceptibility in low dose environments