# COMPUTER SCIENCE/DATA SYSTEMS TECHNICAL SYMPOSIUM

April 17, 1985

# ADVANCED DIGITAL SAR PROCESSOR (ADSP)

JPL

Tom Bicknell

792-2523

JPL

# ADSP

OBJECTIVES

- DEVELOP THE TECHNOLOGY REQUIRED TO MEET THE SAR PROCESSING NEEDS FOR MISSIONS IN THE LATE 1980's
- BUILD AND DEMONSTRATE A HIGH PERFORMANCE ENGINEERING MODEL FLEXIBLE ENOUGH TO BE EASILY ADAPTED TO A WIDE VARIETY OF SAR PROCESSING TASKS AND CAPABLE OF REAL-TIME OR NEAR REAL-TIME THROUGHPUT RATES

APPROACH

- IMPLEMENT SAR PROCESSING ALGORITHM ELEMENTS (FFT'S, MULTIPLIERS, MEMORY SYSTEMS, INTERPOLATORS, FUNCTION GENERATORS, ETC.) INTO A PROGRAMMABLE PIPELINE ARCHITECTURE
- USE ONLY COMMERCIALLY AVAILABLE INTEGRATED CIRCUITS TO MINIMIZE COST AND RISK
- OPTIMIZE ARCHITECTURE AND CIRCUIT DESIGN FOR THE BEST BALANCE OF TESTABILITY, FLEXIBILITY, AND EFFICIENCY

JPL

# WHAT IS THE ADSP?

THE ADSP IS A VERY EFFICIENT DIGITAL SAR PROCESSOR IN TERMS OF PERFORMANCE PER UNIT DEVELOPMENT COST OR PER UNIT OPERATIONS COST

THE MOST COST EFFECTIVE SAR PROCESSING TECHNOLOGY CURRENTLY IN USE IS A MINI-COMPUTER WITH ARRAY PROCESSORS

| COST ITEM | | MINI-COMPUTER SYSTEM (WITH 4 AP) | ADSP |
|---|---|---|---|
| DEVELOPMENT/ACQUISITION COST ($K) | | 1000 | 5000 |
| DEVELOPMENT COST ($K) PER MEGAFLOP | | 20 | 1 |
| DATA PROCESSING OPERATIONS COST ($K) (PER 100 SECONDS OF DATA TAKEN) | SEASAT | 8 | 0.2 |
| | SIR-B | 2 | 0.1 |
| DATA PROCESSING COST ($K) FOR A 100 HR SIR MISSION: | | 7000 | 500 |

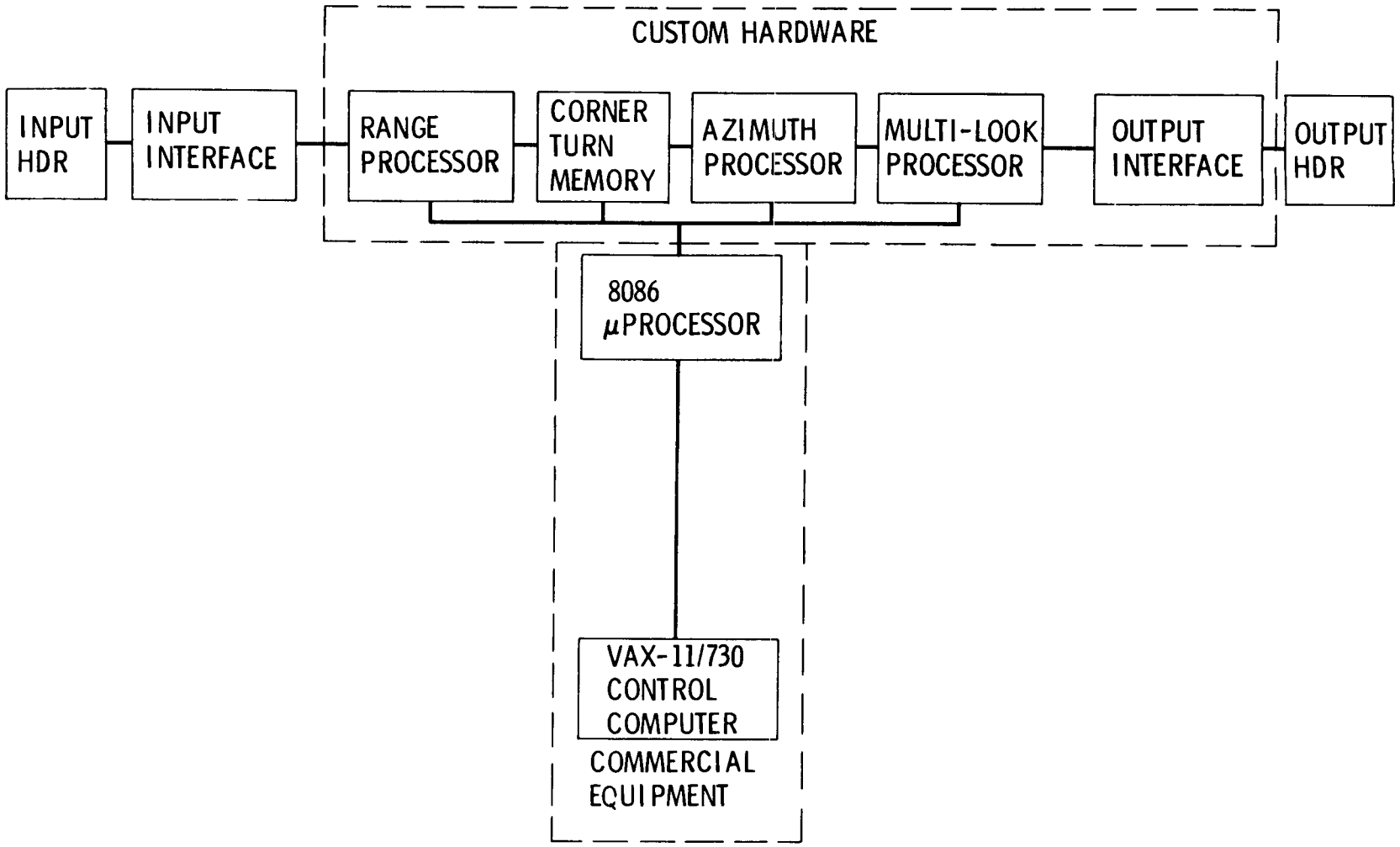
JPL

# CURRENT AND FUTURE DATA PROCESSING TASKS

| MISSION* | HOURS OF DATA TAKEN (EXPECTED) | MISSION PROCESSING COST $K | |
|---|---|---|---|
| | | MINICOMPUTER-AP SYSTEM | ADSP |
| SEASAT (1978) | 50 | 14,000 | 300 |
| SIR-B OCT (84) | 9 | 500 | 25 |
| SIR-B' FEB '87 | (50) | 2,500 | 125 |
| VRM 1988-89 | (1200) | 5,000 | 1,000 |
| SIR-C 1989 | (100) | 10,000 | 400 |

*POTENTIAL SIR REFLIGHTS AND EXTENDED VRM MISSION NOT INCLUDED

# ADSP ENGINEERING MODEL SYSTEM DIAGRAM

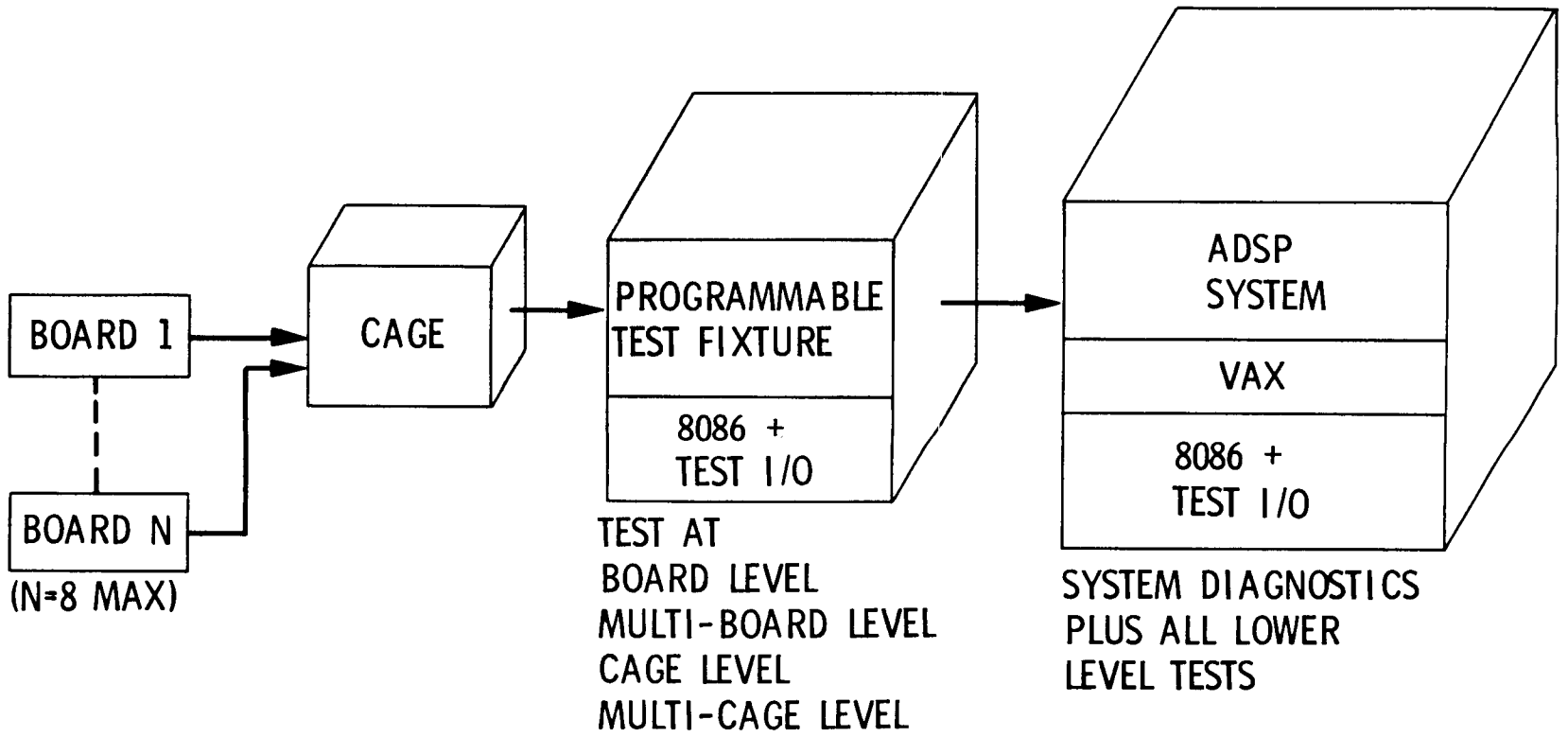


JPL

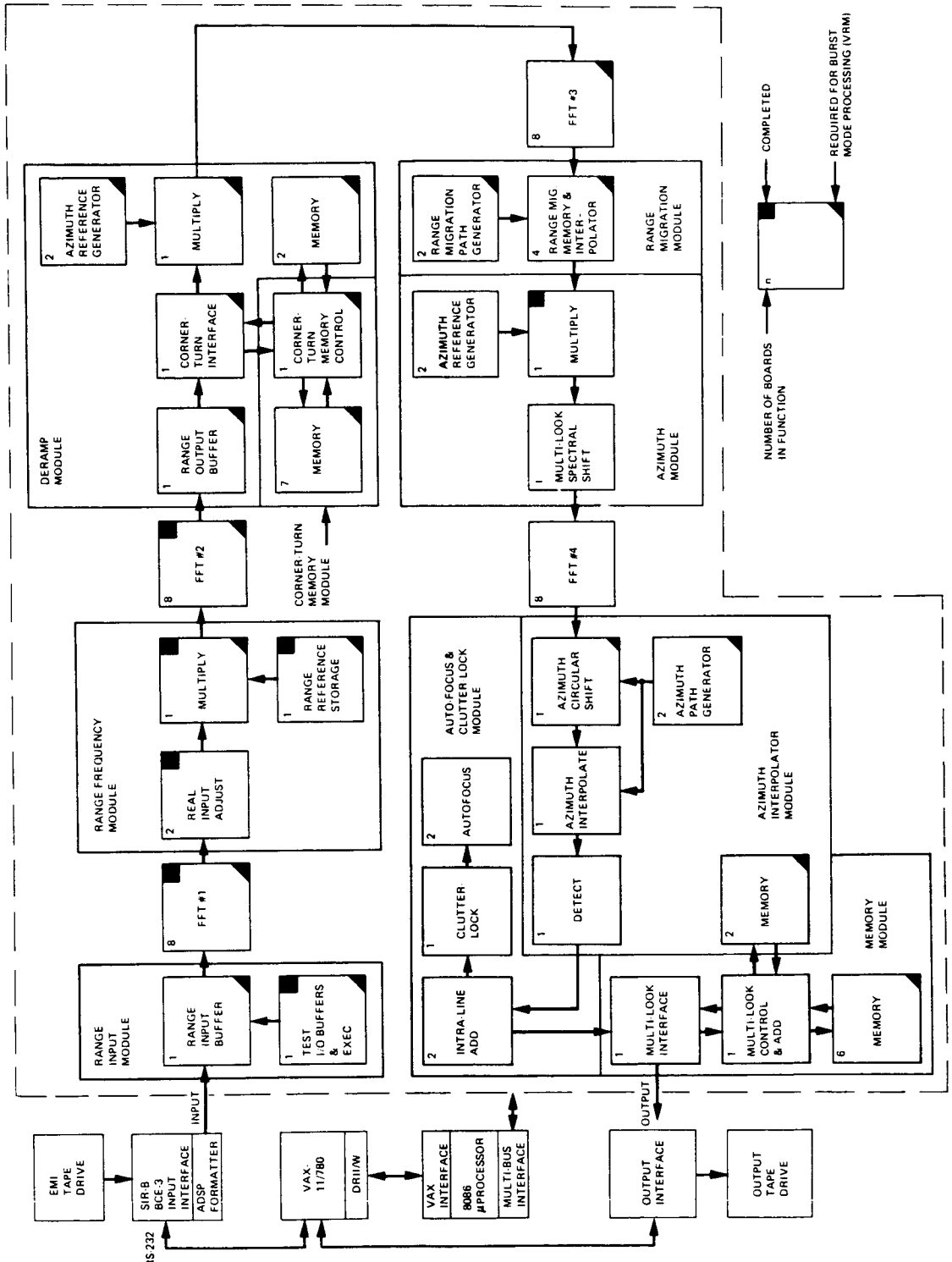
# ADSP SYSTEM ATTRIBUTES

- 6 GIGAFLOP RATE AND 160 MEGABYTES OF MEMORY (~35,000 ICs)
- BUILT-IN DIAGNOSTICS
- PROVIDES FLEXIBLE SAR PROCESSING WITH VARIABLE: LOOKS, WEIGHTING FUNCTIONS, INTERPOLATION FUNCTIONS, AND PIXEL SPACINGS
- MULTI-LEVEL CONTROL CAPABILITY FROM AUTOMATED PRODUCTION DOWN TO MANUAL BIT MANIPULATION

# ADSP DEVELOPMENT TEST METHOD

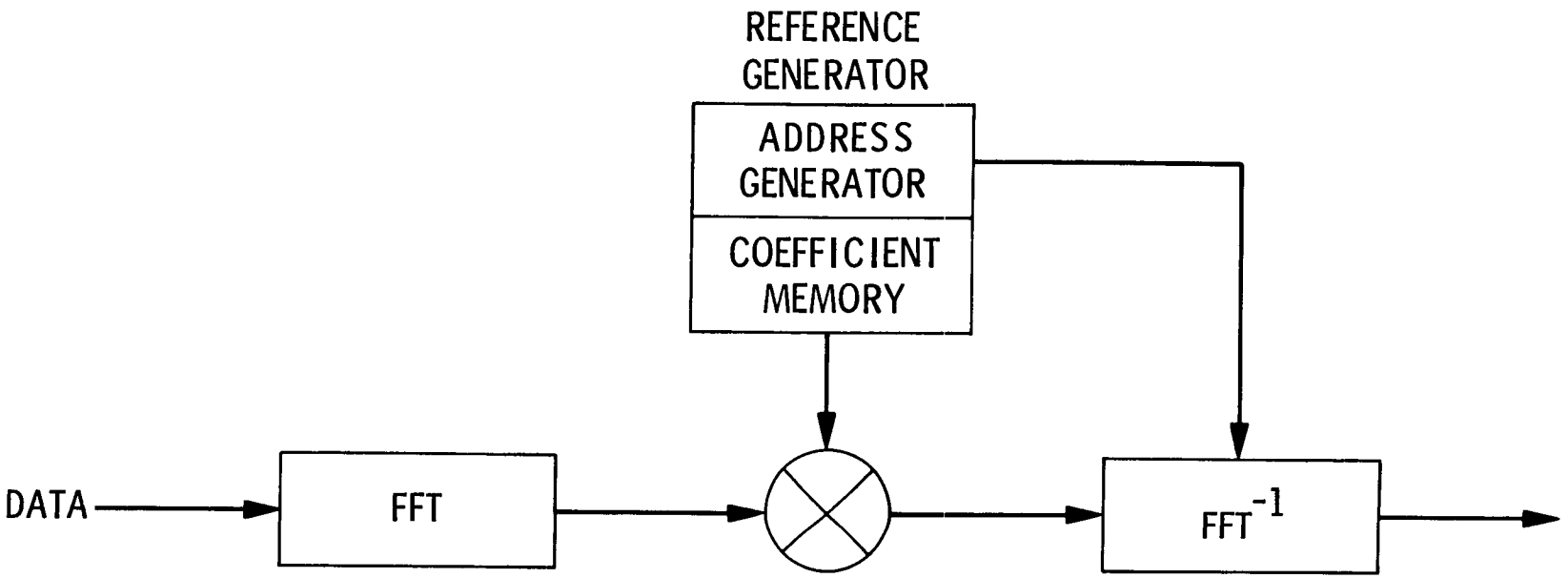


# JPL ADSP HARDWARE BLOCK DIAGRAM



JPL

# RANGE PROCESSOR




FFT MODULE

20 MHz PIPELINED FFT
PROGRAMMABLE UP TO 16K COMPLEX SAMPLES/LINE
22 BIT REAL, 22 BIT IMAGINARY (TRW FLOATING POINT)

REFERENCE GENERATOR

128K WORDS (12R, 12I)
LINEAR INTERPOLATE FUNCTION

JPL

# OTHER USES OF ADSP

- SOME NON-SAR SIGNAL PROCESSING
- POWERFUL RESEARCH SAR PROCESSING
- TECHNOLOGY BASE FOR POTENTIAL ERS-1 PROCESSOR
- OPTIMIZED USE OF MATH AND MEMORY FUNCTIONS WILL AID GREATLY IN DESIGN OF FUTURE ON-BOARD SAR PROCESSORS