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RESONANT AC POWER SYSTEM PROOF OF CONCEPT TEST PROGRAM FINAL REPORT

VOLUME 1

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16. Abstract

Proof-of-concept testing was performed on a 20-kHz, resonant power system breadboard from 1981 through 1985. The testing began with the evaluation of a single, 1.0-kW resonant inverter and progressed to the testing of breadboard systems with higher power levels and more capability. The final breadboard configuration tested was a 25.0-kW breadboard with six inverters providing power to three user-interface modules over a 50-meter, 20-kHz bus. The breadboard demonstrated the ability to synchronize multiple resonant inverters to power a common bus. Single-phase and three-phase 20-kHz power distribution was demonstrated. Simple conversion of 20-kHz to dc and variable-frequency ac was demonstrated as was bidirectional power flow between 20kHz and dc. Steady-state measurements of efficiency, power-factor tolerance, and conducted emissions and conducted susceptibilty were made. In addition, transient responses were recorded for such conditions as start up, shut down, load changes. The results showed the 20-kHz resonant system to be a desirable technology for a spacecraft power management and distribution system with multiple users and a utility-type bus.

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FOREWARD

This report contains two volumes. The main text (Volume 1) summarizes the test results and gives a detailed discussion of the response of three early , first generation configurations of ac power system IRAD breadboards to the contracted tests imposed on them. It explains photographs, measurements, and data calculations, as well as any observed anomalies or lessons learned. Volume 2 (Appendix 1), Tests Results and Data, published under separate cover, includes all of the data taken on the 1.0 kW single-phase; 5.0 kW three-phase; and 25.0-kW three-phase system breadboards. The format of this data is raw, ie. it is a direct copy of the data sheets for the test data notebook.

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SECTION 1

INTRODUCTION

The spacecraft being designed for new NASA and DOD missions are projected to have demands for power at levels of one to two orders of magnitude greater than current spacecraft. The evolving spacecraft power systems for these missions will require increased efficiency and versatility to meet load requirements of greater power, multiple users, and increased life. The initial Space Station will have a power system on the order of 100 kW. It should also have the capability of being expanded to cover expected power needs of hundreds of kilowatts, while remaining versatile enough to meet the needs of a varied and constantly changing set of users. In addition to the Space Station, communications and military spacecraft power systems are evolving toward larger power systems capable of meeting diversified user load requirements.

A high-frequency, high-voltage ac power system would fulfill the needs of the Space Station or any other multiple-user spacecraft as a versatile, utility-type power system. The ac system concept is described in the study of power management technology for orbital multi-100kWe applications (Contract NAS3-21757), which suggested many advantages of an ac power system. For example, an ac system allows the selection of the optimum voltage at any portion of the power system. The power distribution, therefore, can be done at high voltages to ensure a high distribution efficiency. Also, switching and fault isolation can be performed with conventional inverter silicon controlled rectifiers (SCRs), as described herein.

Resonant inversion is a straight-forward and efficient way to produce high-frequency ac power. Since all switching is done when the current is zero, switching losses are close to negligible in a resonant inverter. Also, the power generated is a pure single-frequency sine wave (See Figure 1-1), which minimizes the filtering required. Since the resonant inversion frequency is in the high audio range (20 kHz), the size of the reactive components is reduced by half compared to conventional 400 HZ

technology.

This report chronicles a five year long test and evaluation of 20 kHz power conversion and distribution hardware. There were three different development phases, a 1 kW demonstration phase, a 5 kW phase, and a 25 kW phase, as shown in figure 1.1.1. Under the terms of the contract, General Dynamics supplied the government with test and evaluation data obtained using their own IRAD hardware. The characteristics of the hardware are those of early, first generation breadboard systems. In the beginning two to three years, no attempt was made to optimize efficiency, the primary goal was to establish whether the resonant approach could be made to work at all. A more recent contract report (CR175068) contains information concerning second generation testbed hardware, which contains many of the improvements suggested by the test and development activity described herein.

The major objective of the contract was to verify the theoretical advantages of 20 kHz power conversion and distribution,i.e. will it work,will it be stable, will it be as simple as anticipated, and will it meet its efficiency expectations? The contracted testing demonstrated that a resonant power system could be built and operated at a significant power level, and evaluated the system response to a variety of transient conditions; including load changes, startup, shut down, and input voltage changes. The steady-state operation of the system was also analyzed and the efficiency of an optimized power system calculated.

The contract was conducted in three phases (tasks). They were:

1. Task 1, which was the testing and evaluation of a system with two, single phase, 1.7 kW inverters,
2. Task 2, which evaluated three inverters in a three phase, 5 kW configuration, and,
3. Task 3, which evaluated six inverters in a three phase, 25 kW configuration.

These successive generations of IRAD hardware represent modifications and improvements in the hardware suggested by the earlier test results, with the final 25 kW hardware demonstrating a power level technology required for the space station.
This report has two volumes. They are:

Volume I, Resonant AC Power System Proof-of-Concept Test Program-Final Report This report contains a summary of the test results and a detailed discussion of the response of the various configurations of the ac power system breadboards to the tests imposed on them. Photographs, measurements, and calculations on the data, as well as any observed anomalies or lessons learned are explained.

Volume II (Appendix), Resonant AC Power System Proof-of-Concept Test Program - Test Results and Data This report includes all of the data taken on the single-phase, 5.0-kW three-phase, and 25.0-kW, three-phase system breadboards.

Together, these two volumes provide the wealth of material required to justify the development fo the technology further for use on Space Station and on othe larger satellites.

SECTION 2

TEST RESULTS SUMMARY

2.1 TASK 1.SINGLE-PHASE SYSTEM TESTING See Table 3-1 (Test Matrix)

In this summary, the results of the multi-year contracted test program are summarized. Readers who are not familiar with resonant inverter circuit topology may well want to read section 3, as it provides a summary of the approach.

The first step of the testing was an evaluation of a single phase resonant inverter which showed that the unregulated inverter has a load regulation of 6.0% over its entire load range of 0 to 1.1 kW. This demonstrated that the parallel-output type resonant inverter is an ideal source for a utility type of power system, because it is a relatively stiff voltage source, i.e. it has good inherent voltage regulation as the load changes. The next step in the testing was to combine the outputs of two inverters in parallel and synchronize their clocks to provide power to the transmission line. This testing demonstrated that:

1. Inverters can readily and simply be paralleled with no changes to the inverter circuit, and
2. That the load will be shared among the inverters to within 5.0%, as determined by the test.

A 50-meter transmission line was used to illustrate that transmitting power over long distances can be accomplished with the line impedances having minimum effect on the inverter modules. For all these tests, the frequency of the power on the transmission bus was determined by the clock that triggers the inverter SCR's and is, therefore, not affected by load, line voltage, or other principal power system parameter.

To demonstrate the various forms of power that are easily available from this type of an ac power system, three power receiver modules 50 meters from the inverter drivers were connected to the transmission line as load modules (shown in Figure 2-1). They were:

a. a DC Receiver Module: a 1.0-kW output module capable of supplying

voltages from 0 to 40 Vdc, and

b. a ac receiver module: a 1.0-kW output module capable of supplying a 115 Vrms output over the frequency range of 400 Hz to 1.0 kHz, and

c. a Bidirectional module: a 1.0-kW module capable of supplying 90 Vdc output or acting as an inverter and supplying power to the distribution bus from a dc source.

The bidirectional module was tested for its ability to deliver power in both directions, from dc to 20 kHz and from 20 kHz to dc. Such a module would be useful as an interface to batteries or other energy storage medium in an actual system configuration. It was also determined from the evaluation of the ac and dc receivers that using a phase-controlled bridge was an acceptable means to provide either dc or low-frequency ac power to a load. (See figure 3.7) When loads on these modules were switched abruptly, the system responded very quickly and quietly as the loads were changed from zero to full load on each of the receiver modules. Power losses were measured component by component throughout the system.

These first single phase tests immediately started to validate the promise of the 20kHz technology, namely that transformers could be used to provide the isolation and easily adjusted voltage levels, that typical dc and ac loads could be supplied with 20 kHz power over the transmission line, and that resonant inverters worked, producing the expected, low distortion sine wave.

2.2 Task 2. THREE-PHASE, 5.0 KW SYSTEM TESTING

In this phase of the testing, three 1.7 kW inverters were synchronized 120 degrees apart and connected via a three-phase transformer to a transmission line. The bus was a three-phase power transmission line that is also fifty meters in length. This system configuration had four receiver modules:

a. a DC receiver: a 1.0-kW output module capable of supplying voltages of 10 to 40 Vdc (Same as task 1), and

b. a Bidirectional module: a 1.0-kW module capable of supplying 90 Vdc output or acting as an inverter and supplying power to the distribution bus (Same as task 1), and

c. a Variable-frequency ac receiver: a 1.0-kW output module capable of supplying 20 to 130 Vrms over a frequency range of dc to 1200 Hz, and

d. a Three-phase ac receiver: a 1.0-kW output module capable of supplying three-phase, 60-Hz power at voltages of 50 to 230 Vrms.

In addition to the active load modules, resistive loads were transformer-coupled to the transmission line to bring the system up to the 5.0-kW power level. The variable-frequency ac receiver was successfully tested for its ability to start and operate a 230 Vrms, three-phase, 1.0-Hp induction motor. During the startup of the motor, the converter output frequency was "ramped" to match the starting speed rate of change.

Because the power of each of three phases is provided by a separate inverter, the breadboard was able to operate with unbalanced loads. For example, the breadboard was operated and worked well when fully loaded with a 0.58 lagging power factor load. It was also operated with a leading power factor less than 0.60. Even with the active load modules fully loaded, the total harmonic distortion in the system was low, it varied between 3.1% and 3.7% over the three phases at the inverter outputs, and 3.9% And 6.8% on the bus. The distortion on the transmission line is caused by the switching in the receiver modules and the bus impedance and can be greatly reduced by improved receiver modules which appear as a more continuous load on the bus.

It was already known from the single-phase system testing that inverters could be operated in parallel provided their outputs are in phase. It was established in this phase of the testing that inverter modules will operate in series whether the outputs are in phase or not. Using this information, an inverter output voltage regulation approach was tested in which the outputs of two inverters were connected in series and the phases between the two varied. Using this approach, the transmission bus voltage remains

constant for input voltage swings in excess of 100%. This allows the inverter to handle the voltage swings that a solar array produces as it emerges from the eclipse with a significantly lower temperature than it has for most of its insolated period.

2.3 TASK 3, 25.0-KW, THREE-PHASE SYSTEM TESTING

In this final phase of the testing, six 4.6-kW inverters were configured to drive a three-phase bus. For comparability of results, the inverters were connected to the same 50-meter transmission line, dc receiver module, bidirectional receiver module, and the variable-frequency, variable-voltage ac receiver module as used in the 5.0-kW, three-phase system testing (see Section 2.2). An additional 22.0 kW of resistive loads were connected to the bus.

The most significant upgrade of this breadboard is its incorporation of closed-loop, "phasor" regulation to maintain its bus voltage. The outputs of two inverters are connected in series to drive each phase of the bus as shown in Figure 2-3. The bus voltage of each phase is determined by the phasor or vector sum of the two voltages. Thus, by varying the phase shift of the output voltages of the two inverters, the bus voltage of each phase can be regulated independently. The voltage regulation of this technique was measured over the full load range, over 0.7 lagging to 0.7 leading power factor loading, and over a 120 Volt dc to 200 Volt dc input voltage variation. Through all of these variations, the bus voltage was maintained to better than 2.0%. The test results indicate that it should be possible to maintain the bus voltage to well within 0.50% over this entire range of conditions.

Phasor regulation is implemented with equal load sharing among all inverters under full load conditions (27.5 kW). Using this approach, the total harmonic distortion can be kept below 5.0% on the bus under test conditions where the system was loaded with an 80 percent resistive load. Employing no special filters or shielding of any kind, the breadboard meets or exceeds the majority of requirements of MIL-STD-461B for conducted emissivity and susceptibility. Simply improving existing filters would enable the breadboard to meet all but a few of the remaining specifications. To pass all of the specifications, some new filters would have to be added.

The 25 kW system test configuration also included a fault-isolation switch installed on the bus between the inverters and the loads. This switch consisted of a pair of antiparallel SCR's and their associated control circuitry. It cleared short circuits from the bus in less than two periods of the 20 kHz waveform, under both light and heavy load conditions (21.6 kW). This rapid fault isolation approach, described further in section 4.9, is one of the unique safety features of the 20 kHz approach for the Space Station.

Another interesting demonstration in this phase of the testing is the addition and removal of one inverter module from an operating, loaded system. The removal of the module went undetected by the user, i.e. a single phase of the three phase system can fail and the remaining two phases continue to supply power. This demonstrates the modularity of the resonant approach.

It should be noted that although six inverters were required to achieve a 25 kW output, the technology itself is expected to be capable of using only one inverter module to generate the full 25 kW. This ultimate limit on inverter power comes from the size of the resonant components; as the module power is increased their size decreases until they are no longer a practical size.

2.4 LESSONS LEARNED

One of the important discoveries was the simplicity with which multiple inverter modules can be synchronized to drive a common load. When the inverter outputs are of a single frequency and in phase, which is easily accomplished by running them from a common clock, the inverters will share the load to within 5.0% With no modifications of the inverter circuits. Another result was the dependence of efficiency on the resonant frequency of an inverter. In a resonant inverter, the resonant frequency of the reactive components is higher than the switching or line frequency. It was shown that as the two frequencies are brought closer together, the stored energy in the reactive components increases. This increased energy increases the current in the inverter causing the resistive power losses in the inverter to rise as the square of the current while the output power rises linearly with current. Thus, a tradeoff must be performed between

power per module, efficiency, and waveform purity. For the space station this trade is being performed during the phase B study activity.

By tracing system losses, it was learned that significant power was being dissipated in the resonant capacitor. A closer look revealed that much of the losses were caused by eddy currents being induced in the cases of these capacitors. When designing and testing sample transmission lines, it was learned that adding a shield to a transmission line increases the apparent line resistance and thus the power dissipation of the line. It turns out that this additional power loss is attributable to eddy currents being induced in the shield from the current in the line. The power in these eddy currents is dissipated in the resistance of the shield. A final system design would include careful design and analysis of any cases and shielding used on system components to minimize power dissipation.

Besides the detailed lessons learned which will improve system performance in the future, there were, of course, the macro lessons of significance: the technology does work, the inverters run stably, in parallel, and with less difficulty than we might have expected.

2.5 RECOMMENDED SYSTEM IMPROVEMENTS

The two early breadboard testing tasks; the single-phase, 2.0 kW system tests and the three-phase, 5.0 kW system tests, led to the identification of several areas where the breadboard systems could be improved in a progression toward an optimized system. These improvements were:

- Selection of an optimum inverter power switch to improve of switching times, efficiency, and turn-off ability.

- Use of litz wire where possible to eliminate losses caused by skin effect.

- Use of non-ferrous capacitor cases to reduce eddy current losses.

- Implementation of center-tapped, half-bridge, full-wave configurations for dc receivers.

- Regulation of low-voltage dc receivers on the high-voltage side of the

user transformers, rather than on the low side, to improve converter efficiency.

- Development of a receiver module that draws continuous currents from the transmission line, to minimize the power handling capability required of the inverters.

All the test data gathered to date on this contract has been on breadboards which use SCRs as the power switches. Although we have verified the operation for a resonant inverter with both D60T transistor and power MOSFETs, we have not measured the efficiency of these types of inverters. A trade study to determine the best switch for each portion of the system is recommended. Such a study will evaluate the performance of SCRs, bipolar transistors, MOSFETs, insulated gate FETs, and other semiconductor switches in resonant inverters and other system modules.

The testing has also shown that Litz wire can be used to significantly reduce losses over stranded wire of the same size at 20-kHz. Litz wire will be used to its maximum advantage in all transformers and inductors present in the system. Capacitors housed in steel cases exhibit significant power dissipation due to eddy currents induced in these cases. Using nonferrous, aluminum cases on the resonant capacitors greatly reduces eddy current dissipation in these devices, which improves the inverter efficiency.

The efficiency of any transformer-rectified receiver module will be increased by using, where possible, a center-tapped bridge configuration with only two switching elements. This reduces the number of switches from four to two, when compared to the full-bridge approach used in the breadboard power systems. Additionally, the efficiency of a dc receiver module can be further increased by moving the regulation function of the bridge to the high-voltage side of the load transformer and using rectifiers on the low-voltage side of the transformer. This allows the SCR voltage drop to be incurred on the high-voltage side of the transformer where the current and, therefore, the power loss is smaller. The development of a receiver module that would draw current continuously over the entire 25 micro-second half period will improve system efficiency and reduce bus distortion by more effectively loading

the inverter modules.

2.6 PROJECTED SYSTEM EFFICIENCY

Although initially the efficiency of the single-phase breadboard hardware measured only 70.3 percent end-to-end, the components contributing most significantly to the total power dissipation were identified. Several improvements were found to raise the receiver module efficiencies (Section 2.4). The transformers and the transmission line used in this breadboard were found to be highly dissapative and substantially less efficient than can be designed using commonly available parts. For example, the efficiency of the transmission line was only 90%.

In the three-phase system breadboard, an improved transmission line was used that was designed to be 99.5% efficient. Based on the testing conducted later at the 25 kW level, this line met its designed efficiency. Thus, the efficiency measured on these two resonant ac power system breadboards increased from 70.3% to 77% in upgrading from the initial single-phase, 2.0 kW power system breadboard to the three-phase, 5.0 kW breadboard.

The major improvements were made in upgrading the power system breadboard from the 5.0-kW power level to the 25.0-kW, three-phase power system breadboard were:

1. The replacement of the inverter transformers with litz-wire-wound transformers.
2. The inverter modules were completely redesigned and rebuilt. They used new SCRs, inductors, and capacitors because of the increased power level.

In addition to these improvements, "Phasor" regulation (described in Section 3.8) was incorporated into the system controller to maintain the bus voltage. With these module and component improvements and with a new bus regulation technique, the end-to-end efficiency was measured to be 87.3% at an output power of 27.5 kW. To reflect actual Space Station user loads, the 50-meter bus was loaded with the dc, ac, and bidirectional load-interface receivers tested in the previous two phases of testing and an additional three resistive loads. See figure 2.3.

Much of the inefficiency of the present 25 kW breadboard can be attributed to the 50-meter bus that was sized to carry 5.0 kW with less than a 0.5% loss. By running this same bus at five times the power, the power loss (I^2R) is multiplied by the square of the current increase which is 25. This means that at 20 kHz, the bus is only designed to be 87.5 percent efficient. The bus is actually 93% efficient, but it is still the largest contributing factor to the breadboard power dissipation. Replacing the bus with a 25-kW bus would drive the end-to-end system efficiency of this breadboard well above 90%. By upgrading the components and modules of the 20-kHz power system breadboard and scaling up the power level from the 2.0-kW proof-of-concept breadboard to a power system breadboard that is the actual power level of a Space Station power channel, the system efficiency has been improved rather quickly from the initial 70.3% toward the goal of 92%. Figures 2.6.1 and 2.6.2 show the expected efficiency chain for the inverters and a typical receiver for the system.

SECTION 3

SYSTEM TEST CONFIGURATIONS

3.1 AC SYSTEM OPERATION

The main component of the resonant ac power system is the inverter or system driver, which is simply a series resonant circuit as shown in Figure 3-1a. The inverter operates as follows. When switch S1 is closed, the resonant circuit is excited and "rings" at the natural resonant frequency of the circuit determined by the values of L, R and C. The voltage across the load will appear as in Figure 3-1b. The load resistance dissipates energy from the resonant circuit and causes the voltage and current waveforms of the circuit to be damped. If the resonant circuit is now excited from a pair of opposite polarity sources through a pair of toggled switches operating at the natural frequency (Figure 3-2a), a sustained ac wave can be developed as shown in Figure 3-2b.

This circuit can be implemented in the usual bridge arrangement depicted in Figure 3-3. F.C. Schwarz has designed a series of bidirectional power converters using this configuration. Alternatively, the load can be placed in parallel with the resonant capacitor as proposed by Neville Mapham (Figure 3-4). Each type of resonant inverter has its advantages and disadvantages.

The current in the resonant circuits of either of these inverters is primarily determined by the L and C of tank circuits. Therefore, the Schwarz-type inverter is basically a current-source device because the load is in series with the L-C tank circuit. The Mapham configuration acts as a voltage source since its load is in parallel with the resonant capacitor. The Schwarz inverter is tolerant of short circuits but becomes overdamped and begins to operate irregularly for light loads. The Mapham inverter is a voltage source but becomes overdamped and begins to operate irregularly for heavy loads. Because the ac breadboard is a utility-type

power system, the Mapham configuration was chosen as the driver module.

If the resonant frequency of the inverter is increased above the switching frequency, devices with significant turn off times (such as SCRs) can be used as switches. Replacing the load resistor of Figure 3-4 with a transformer allows the inverter to be used as the driver to a high-voltage bus capable of providing power to a variety of loads. Larger power systems are possible by combining multiple inverter modules.

The initial Task 1 testing demonstrated that such a power system could be built and successfully operated. This testing also demonstrated that power could be delivered over long distances on a power bus driven by multiple resonant inverters to several types of loads. The power bus was operated at a high voltage and high frequency to maximize efficiency and minimize weight. A matrix listing the system test configurations and the tests performed on each configuration is shown in Table 3-1. The tests began on a single inverter module and progressed to the testing of an entire power system breadboard composed of two inverters and three active load modules and, finally, to the testing of a three-phase power system breadboard. The system test configurations (Table 3-1) are described one by one in the following sections.

3.2 SINGLE DRIVER (CONFIGURATION 1)

The initial test configuration was a 1.0-kW inverter module with a resistive load (Figure 3-5). The inverter schematic is shown in Figure 3-6. This module was operated with a 90-Volt input and run through a series of tests to determine its start-up performance, response to load changes, load regulation, and efficiency.

3.3 SINGLE DRIVER-TRANSMISSION LINE-DC RECEIVER (CONFIGURATION 2)

The inverter module of Configuration 1 was transformer-coupled to a 50-meter transmission line. The dc receiver module, which converts the 20-kHz power to dc (Figure 3-7), was connected to the bus with a simulated transformer disconnect as illustrated in Figure 3-8. This configuration was subjected to the same tests as the single inverter as well as an additional test to measure the gain and the step response of the closed-loop control circuitry of the dc receiver.

3.4 BIDIRECTIONAL MODULE (CONFIGURATION 3)

In this test, the operation of the bidirectional module (Figure 3-9) in the dc-to-ac mode was also verified as depicted in Figure 3-10. Its operation in the ac-to-dc mode was verified and tested in the system testing of Configuration 4.

3.5 DUAL DRIVER SYSTEM (CONFIGURATION 4)

Two 1.0-kW inverters were synchronized to drive the 50-meter transmission line and three 1.0-kW receiver modules: the dc receiver module (Figure 3-7), the bidirectional module (Figure 3-9), and a 20 kHz-to-400 Hz receiver module (Figure 3-11), as shown in Figure 3-12. This configuration was also run through the same set of tests as the single inverter module to determine its start up and shut down performance, response to load changes, control signal response, and system efficiency.

3.6 3.0-KW, THREE-PHASE BREADBOARD (CONFIGURATION 5)

As shown in Figure 3-13, three upgraded inverters capable of operating at 1.7 kW each (Figure 3-14) were synchronized to provide power over a three-phase transmission line to three 1.0-kW load-interface modules: a dc receiver module (Figure 3-7), a bidirectional module (Figure 3-11), and a variable-frequency, variable-voltage ac receiver module (Figure 3-15). The steady-state system performance was measured. This included measurements of efficiency, harmonic components, total harmonic distortion of the bus, and waveform photographs of the system parameters. Transient system response data was not recorded as this configuration is actually the 60%-load case of the 5.0-kW system, which was subjected to the entire set of transient tests (Section 3.7).

3.7 5.0-KW, THREE-PHASE BREADBOARD (CONFIGURATION 6)

In this configuration the breadboard used the same circuitry as that described in section 3.6,except that to bring the load power level up to the

level of the drivers, 2.0-kW of resistors were connected to the bus of the 3.0-kW, three-phase system breadboard (Section 3.6) with step-down transformers as shown in Figure 3-16. In order to make a comparison between the single-phase power system breadboard test data and the three-phase system test results, the same set of tests and measurements (start up, shut down, load change response, control signal response, etc.) were performed on this 5.0-kW system. Additional tests were also performed: bus line regulation measurements, power factor measurements, and motor testing.

3.8 25-KW, THREE-PHASE BREADBOARD (CONFIGURATION 7)

This test configuration is a 25.0-kW power system breadboard consisting of six newly-designed 4.2-kW resonant inverters (Figure 3-17); six new inverter transformers; the 1.0-kW dc receiver module; the 1.0-kW bidirectional module; the 1.0-kW variable-frequency, variable-voltage ac receiver module; a 50-meter, three-phase bus; and 22.0 kW of resistive loads arranged as in Figure 3-18. The 25.0-kW power level was chosen because it was estimated to be the size of one power channel on the Space Station (a solar dynamic generator or 4 solar array wings).

A new feature of this breadboard is that it uses the "Phasor" regulation technique in which the outputs of two or more inverters are summed by connecting them in series. The voltage of the sinusoidal output waveform is regulated by shifting the phase relationships between the inverters. In this way, the voltage can be varied between the maximum voltage when the inverters are in phase and 0.0 Volts when the inverter phase relationships are:

$360°/$the number of inverters (180° out of phase for two inverters, 120° for three,etc.).

This phase shifting of the inverters causes the inverters to be unbalanced, each supplying a different amount of the total delivered power to the load. In the breadboard, two of the six inverters supply power to each phase of the three-phase bus. When there is a phase difference between the inverter output voltages, one lags the resulting bus voltage and hence, the bus current. The other leads. So, one inverter sees an apparent inductive load and supplies less power, while the other sees an apparent capacitive load and delivers the majority of the load power. However, the inverter

unbalance can be corrected. A capacitor placed across the output of the inverter driving the apparent inductive load cancels the inductive phase shift and allows it to supply more power. This compensation technique was the standard for the testing on this breadboard. An alternative technique for balancing the two inverters is evaluated in Section 4.2.6. It should be noted that the topology of phasor regulation employed in the 25 kW breadboard circuitry allowed each phase to be independently regulated.

The 25.0-kW breadboard was subjected to the same set of tests as were run on the other two breadboards. In addition, the line and load bus voltage regulation and the conducted susceptibility and emissivity of the 25.0-kW system were measured. Photographs were also taken of the response of the system and its fault-isolation switches to a bus short. The measurement points used throughout the testing on this system are shown on the system diagram of Figure 3-18.

SECTION 4

TEST RESULTS

This section contains a detailed discussion of the data gathered under this test program. The discussion is presented in the order of the tests listed in Table 3-1. All of the photographs and measurements taken during this program are contained in Volume II of this report.

4.1 START UP TESTING

The purpose of this testing was to observe the response of the device under test to a step application of voltage. For each test configuration, a relay was used to apply the power. Two different start up procedures were tried. In one case, the firing signals were present when the relay was closed. In the second, the relay was closed prior to the SCR firing signals being enabled.

4.1.1 Start Up of a Single Inverter

The test circuit for the single inverter configuration is shown in Figure 4.1-1 and the inverter schematic in Figure 3-6. For this test configuration, the SCR firing signals are enabled prior to the closing of the relay. The oscilloscope is triggered as the relay coil is energized. The inverter was able to start up in this manner under all load situations except full load (1.1 kW). The rise time of the input voltage is about 10 micro-seconds as observed in the photograph of Figure 4.1-2. For loads of 0.0w, 130w, and 570w, the transient response of the inverter ended in 150 micro-seconds (3 cycles), independent of load. This is illustrated in the photograph of the inverter output voltage for the 570w case shown in Figure 4.1-3. When this 1.0-kW inverter is step-started under full load conditions (1140w), the resonant circuit responds as if it is overdamped. This causes one pair of SCRs to be triggered while the current in the other pair of SCRs has not yet returned to zero (see Figure 3.6). The result is a short circuiting of the input. In a power system implementation, this would not be encountered since the inverters can be started under light load. Once the inverter is operating (after 150 micro-seconds), it can easily tolerate having the load increased to full load (Section 4.3).

The current from the power supply to the dc input capacitor was the only parameter that had a transient response that lasted longer than 150 micro-seconds (Figure 4.1-4). The time constant of this current is determined by the time constant of the load and the dc input capacitor. When the relay is closed, there is 2.8 Joules of energy in the dc capacitor. After the relay is closed, the capacitor supplies the inverter and its load with power. By doing so, the voltage of the capacitor starts to decay exponentially with a time constant determined by the load and the capacitance. The power supply delivers current to counter this effect and maintain a constant voltage on the capacitor. It should be expected then that when the load is decreased, the stored charge is drained more slowly and the power supply current increases with a longer time constant as shown in the photograph in Figure 4.1-5. The rise time of the current, while the inverter is only delivering 130w, is now 600 micro-seconds instead of the 300 micro-seconds at 570w (Figure 4.1-4).

4.1.2 Start Up of the Driver-Transmission Line-DC Receiver

This configuration was unable to be step-started under any load conditions while the dc receiver was on the bus with its logic turned on. The uncharged dc capacitor of the dc receiver appeared as too much of a load on the inverter at startup and the system was unable to be started with a step application of power. The use of an L-C filter instead of just a capacitor would rectify this problem by limiting the initial current surge. It was not tried for this receiver because of limited funds. However, the ac receiver which employs an L-C filter had no problems with startup (Section 4.1.4).

4.1.3 Start Up of the Dual Driver System

Because of the uncharged capacitors on the outputs of the dc receiver and the bidirectional module, the system was unable to be step-started while these receiver modules were on the bus and running. As with any power system, a start-up procedure is needed. It was observed that this system configuration can be started if the voltage is ramped up over a 200 micro-second period. Alternatively, the system can be step-started with the receiver modules turned off. The inverters will tolerate the start up of the receivers once the inverters have reached steady-state operating

conditions (3 cycles). However, as explained in the following section, the system can be step-started with a heavy load if the large capacitive filters on the receivers are replaced by L-C filters. A final system design would incorporate all of this: an autonomous start-up procedure directed by the system controller to load the system gradually over the first few milliseconds and properly designed receiver output filters so the inverters could tolerate a step start up if necessary.

4.1.4 Start Up of the 5.0-kW, Three-Phase System

The three-phase system was tested with both kinds of start up. In the first case, the relay was closed after the inverter control circuitry was on and the SCRs were receiving gate signals as shown in Figure 4.1-6. Closing the relay and then enabling the inverter control circuitry was also tried as shown in Figure 4.1-7.

The test with the logic turn on before the energizing of the relay was only run for the 0.0w load power case. As expected, there is a huge inrush of current into the dc input capacitor as the relay is closed (Figure 4.1-8). Because of the limited response time of the three HP 6269A power supplies, the input voltage only rises to 40v initially instead of the nominal 120v that they eventually supply. Figure 4.1-9 shows the large current that flows through the Inverter number 3 inductors as the system is started and required to charge the large (9,000 micro-farads) capacitor of the dc receiver. However the inverter does not short the input for longer than 1.0 millisecond because the huge current forces the voltage across the input capacitor to zero momentarily allowing the SCRs to shut off. As the input voltage rises again, the inverter starts and operates normally.

This illustrates two points. First, it demonstrates that a short in an SCR bridge can be eliminated by bringing the input voltage to zero for a short time (greater than 10 microseconds). In an application where the current is limited such as with a photovoltaic array, this could be accomplished by placing a transistor across the input rails. The transistor would be normally off. It would only be turned on momentarily to clear the SCRs in a fault condition. Secondly, once there is some charge on the dc filter capacitor of a receiver from the huge initial current surge, the inverter no longer responds as if its resonant circuit is overdamped. It can then be

started with the receiver on the line and operating. This demonstrates that it is the uncharged capacitor that causes the system to balk at start up. This is easily eliminated by substituting an L-C filter for the capacitive filter.

Discussion of the response of the three-phase system to start up when the control circuitry is enabled after the relay is closed follows with the 0.0w load case being presented first. Figure 4.1-10 shows the large inrush current as the relay is closed and the dc input capacitor to the inverter is charged. Approximately 40 milliseconds later, the input current rises as the inverter logic is enabled. Figure 4.1-10 was taken with the bidirectional module filter capacitor charged. If this capacitor is not charged, Inverter 2, which is the inverter driving the phase to which the bidirectional module is connected, draws a large inductor current and the input power supplies are shorted as shown in Figure 4.1-11. The inductor current of Inverter 2 during start up, both when the dc output capacitor of the bidirectional module is charged and discharged is shown in Figure 4.1-12. This again demonstrates that the uncharged filter capacitor hampers start up. It can be replaced by a more desirable L-C filter. The dc receiver has a larger capacitor, 9,000 as opposed to 700 microfarads, and draws such a large surge current that the input voltage momentarily goes to zero, the SCRs in inverter number 3 turn off, and the inverter restarts. However, like the bidirectional module, if the dc receiver is started with its filter capacitor charged it also starts without the large surge current. None of this shows up in the dc receiver output voltage (Figure 4.1-13). It ramps up smoothly to its steady-state value and the effect of the input current spike is not apparent.

For the reasons stated in the preceding paragraph, the bidirectional module would also prevent the system from starting up when the bidirectional module is loaded to 100w. Therefore, when the logic for the bidirectional module was turned off, the system was able to be started with the dc receiver at 140w and the ac receiver at 60 Hz and 75w (10% load). As expected, since the load on the dc receiver assured that its filter capacitor is uncharged, the large current spike is again present. Even with this load, the system starts correctly.

However, in looking at Figure 4.1-14 it can be seen that the inductor current of Inverter 1 starts up with no current spikes and reaches

steady-state by the third cycle. Inverter 1 is the driver for phase a and the ac receiver (Figure 3-15). The variable-frequency, variable-voltage ac receiver module is the only receiver that uses an L-C filter. This lends credence to the idea that the system will start up if the filters on the receivers are not strictly capacitive. The inductance serves to limit the current drawn by the large capacitor during start up. The inverter resonant circuit, therefore, does not see as large a load and the circuit does not become overdamped. This is not a shortcoming of the resonant system approach as L-C filters are preferable because of their double-pole response and smaller component values.

4.1.5 Startup of the 25-kW, Three-Phase System. As can be seen from the circuit of Figure 4.1-15, the 150.0-Vdc input voltage was applied to the inverters with an SCR, which is the most abrupt application of input power employed in any of the three phases of this test program. As expected from the startup tests on the other breadboards, the startup at no load is smooth. Figure 4.1-16 shows the transient free startup of the inverter as the SCR is switched on and the large inverter input capacitor (4200μF) begins to charge. Both the inverter branch current and the output voltage start smoothly and ramp up with the input voltage over 600μs.

Figure 4.1-17 shows one phase of the bus voltage as the input voltage is switched on. There is a 50% overshoot that lasts for about 500μs until the regulator begins to responds. The regulator has appreciable 3-kHz oscillations that last for a couple of milliseconds. This phenomenon only occurs when the bus is unloaded. It can be corrected by compensating the regulation loop.

As explained in Section 4.1.4, start up of a load-interface receiver with a capacitive filter is hampered by the tendency of the uncharged capacitive filters to appear as a short to the bus at start up. This was again the case, as the system was unable to be started with a step application of power while the dc receiver was on the line and loaded. As explained in that previous section, by simply replacing the capacitive filter with an L-C filter, the system can be started with the receivers on and loaded. In the absence of L-C filters, except on the ac receiver, the start up test was continued with only resistive loads.

With a load of 3.42 kW, the system started cleanly as shown in the bus

voltage photographs of Figure 4.1-18. Again, there is a large 500μs overshoot due to the response time of the regulator circuitry. However, there are no regulator oscillations this time. When the load level was increased to 11.1 kW, some difficulty was encountered with the internal inverter fault protection. The fault-prevention circuitry in the inverters experiencing the apparent inductive load, and hence,having less power available, sensed a larger than usual load and shut these inverters down to protect the system.

This can be seen in Figure 4.1-19, which shows the phase A bus voltage. Every 800μs the protected inverter tries to restart and again shuts down. The regular voltage spikes are caused by the inverter turning on for one-half cycle, sensing an over load, and shutting down to protect itself. When the power level was increased to the full load value of 25.21 kW, the same results were observed. Three of the inverters started smoothly. The other three inverters sensed an over load condition and shut down to protect themselves and the system. The remainder of the inverters and the system continued to operate. Although the circuitry is too sensitive, this anomaly demonstrates the successful operation of the internal inverter fault protection. New fault-protection circuitry has been designed and implemented in the NASA testbed hardware. It has adjustable sensitivity and can be set so that startup is not viewed as an overload condition.

4.1.6 Conclusions and Recommendations for Start Up

The resonant power system configurations that were tested exhibited no problems starting up with a step application of voltage while under no load to 50% resistive-load conditions. Difficulty with start up in this manner was only observed when load-interface modules with strictly capacitive filters were connected to the bus and operating. No difficulty was seen when the variable-frequency, variable-voltage ac receiver with its L-C output filter was on the power line. The system started just as smoothly with this module at 10% load as with any resistive load. An uncharged capacitor appears as a low impedance to the resonant circuit and forces it to be overdamped. However, an inductor serves to limit the current that the capacitor can draw and is a buffer between the inverter and the filter capacitor. The test data indicates that a system composed of resistive loads and receivers with L-C filters will have no problem starting with a step application of power while heavily loaded.

Nevertheless, the start up of a resonant power system, like any other power system, should have a turn-on procedure. There are a couple of ways that these types of systems can be step-started no matter what kind of loads are present. First, the voltage can be ramped up over several hundred microseconds or more. Second, the system drivers can be step-started while all the active load modules are turned off. A couple of hundred microseconds after the inverters are operating, the load modules can be turned on. This is not a problem as observed in the load switching section (Section 4.3). These two methods will guarantee start up independent of the loads. However, the system should be capable of system step start up if the receiver modules employ L-C filters rather than capacitive filters. A final system design would take advantage of these test results. The system controller computer would initiate and carry out a start-up sequence which would start the inverters and gradually add the system loads over a few milliseconds. However, each receiver module will have the appropriate output filters to allow the system to be step-started if necessary.

4.2 STEADY-STATE SYSTEM OPERATION

The goal of this test was to evaluate and understand the performance of resonant power systems. This was done by performing an in-depth study of the system parameters. Photographs of the system waveforms such as inverter output voltages, inverter tank currents, inverter leg or inductor currents, load voltages and currents, etc. were taken. Measurements of the total system efficiency and the load regulation for each configuration were recorded. On the three-phase system, the harmonic frequency components and the total harmonic distortion of the waveforms throughout the system were measured.

4.2.1 Steady-State Operation of a Single Inverter Module

A schematic of the 1.0 kW-inverter module is shown in Figure 3-6. The currents and voltages referred to in this section are labeled in the Figure. An interesting aspect of the inverter operation is the way the resonant circuit reacts to various loads. Figure 4.2-1 shows the leg current of the inverter and its output voltage for the 0.0-kW case and the 1.1-kW case. The positive portion of the leg current is the current in the SCR and the

negative portion is the diode current.

The load dissipates the power in the resonant circuit reducing the stored power and thus the reverse current available to flow back through the diode. The peak diode current is 19A at no load and 4A at full load. It should also be noted that the high frequency oscillations present on the leg currents in these photographs are due to the measurement equipment and not the inverter circuit. The leg currents photographed on the other test configurations do not have the oscillations.

As shown in Figure 4.2-1, it is also apparent that the inverter output voltage amplitude does not change much with load. In fact, the graph of output voltage versus load power (Figure 4.2-2) Indicates that the inverter is a stiff voltage source. Over the range of 0.0 to 1.14 kW, the output voltage of the inverter decreased from 124 Vrms to 117 Vrms. This yields a load regulation of 6.0% for the unregulated inverter. At 1220w, the voltage was still at 114 Vrms.

As expected, since the triggering of the SCRs is controlled by a clock, the frequency of the inverter output changed very little with load. It was measured as 20.01 kHz while unloaded and 20.00 kHz with a load of 1220w. This is not the case for efficiency (Figure 4.2-3). With a 90 Vdc input, the inverter is most efficient (96.8%) under full-load conditions. This is the point at which efficiency is most importanrt because at the points where less power is flowing, there is always always plenty of solar power available. Not only does the efficiency of the inverter increase with load, but the power dissipated in the inverter actually decreases. This is because the SCR current, and thus its power loss, remains fairly constant with load while the current in the inductor and diode is actually reduced.

4.2.2 Steady-State Operation of a Single Driver and Receiver

A schematic of the driver-transmission line-dc receiver configuration showing the location of the parameters measured is shown in Figure 4.2-4. Photographs of the system parameters while the dc receiver is supplying 410w can be seen in Figure 4.2-5. From the Figure, the RMS input current ripple for a single-phase power system is calculated to be 28%. This is much larger than the ripple measured on the input of the three-phase system as discussed in Section 4.2.5. The tank current of the inverter is

merely the summation of the leg currents as shown in Figure 4.2-5.

The dc receiver output voltage decreased from 28.0 Vdc at no load to 26.8 Vdc at 410w. This gives it a load regulation of 4.3%. However, the dc receiver is not limited by its control logic but rather the resistance of the transmission. The transmission line is far from optimal, having an efficiency of 90%. As more and more current is drawn by the dc receiver, the line voltage at the receiver droops. After a certain point, the SCRs in the dc receiver are operating at a conduction angle of zero. The output voltage of the dc receiver is then determined by the voltage available at its inputs. A more efficient bus and transformers will greatly improve the load regulation of the dc receiver.

The maximum efficiency of this configuration was 70.3%. There are several reasons for this and many ways in which it could be improved. As explained above, the transmission line was measured to be only 90% efficient. Also, the dc receiver phase-control regulation is not as efficient as it might be. The dc receiver switches are prone to large power losses because of the high current that they encounter. This could be changed by putting the regulation switches on the high-voltage side of the dc receiver transformer where the currents are much smaller. Schottky rectifiers could then be used in the high-current bridge. Additionally, half of the dc receiver power dissipation can be eliminated by using a center-tapped rectifier instead of a full-bridge rectifier because it would use only two rather than four SCRs.

Another problem with a phase-controlled dc receiver is that it draws current over only a portion of the 25 microsecond half period because of its capacitive filter. The receiver rectifier switches can only be turned on after the input voltage rises higher than the filter capacitor voltage. Replacing the capacitive filter with an L-C filter would lengthen the period that the dc receiver draws current from the inverter. This would allow the inverter to be loaded more heavily with more continuous load current, the inverter can handle more load and its efficiency will be higher. The ideal case would be a continuous current dc receiver.

4.2.3 Steady-State Operation of a Bidirectional Module

A schematic of the bidirectional module is given in Figure 4.2-6 with the

parameters labeled. The purpose of this test was to verify that the bidirectional module would operate in the dc-to-ac mode. It is operated in the ac-to-dc mode in Configuration 4. The bidirectional module operated similarly to the inverters as expected. The efficiency of the bidirectional module in this mode of operation is about the same as an inverter module. At full load of 1.13-kW, an efficiency of 96.9% was measured.

4.2.4 Steady-State Operation of Dual Driver Power System

The schematic for this configuration is in Figure 4.2-7 and shows the parameters measured in this test. Since three receiver modules were connected to the system bus, eight different load combinations were tested. Table 4-1 lists the system load combinations tested and the corresponding total system efficiency. Figure 4.2-8 shows the four leg currents of the two system drivers under the heaviest load conditions. The photographs show that the inverters share the load very well. The only discrepancy is that the diode current of IB is smaller than the other three diode currents, even IA. This is due to a mismatch between the inductors of Inverter 1 and not the load sharing capability of the inverters. The 400-Hz modulations in the currents are caused by the ac receiver, which draws more power at the peak of its 400-Hz output than at the zero crossing.

Figure 4.2-9 Is a block diagram of the system breadboard detailing the power losses point by point. Much of the power loss is in the transmission line and the transformers. Improved designs can practically eliminate losses in both of these types of devices. Improvements can be made in the receiver modules to enhance their performance. Center-tapped transformers can be used wherever possible. This would reduce the number of switches in these receivers by half. In the dc receiver module, high-voltage side regulation can be tried. This approach would place the regulation SCRs on the high-voltage side of the load transformer and Schottky diodes on the low-voltage side. As discussed in section 4.2.2, continuous current receivers would be the ideal load-interface power modules. They load the inverters more effectively, making them more efficient. Some of the system power loss can be attributed to the components such as the diodes. Figure 4.2-10 shows the current overshoot in the diodes. These components (A139MS) were replaced by 40HFL fast-recovery rectifiers in the three-phase system configuration to

eliminate this overshoot.

4.2.5 Steady-State Operation of the Three-Phase System

Figure 4.2-11 is the schematic showing the test parameters for this configuration. As expected, the input current ripple is small because of the three-phase drivers. The ripple due to the 60-Hz receiver module load is larger than the 120-kHz ripple (Figure 4.2-12). The measurable RMS ripple is about 3%.

The three-phase system was loaded with the same 1.0 kW-dc receiver and bidirectional modules as was the single-phase system. In addition, a 1.0-kW variable-frequency, variable-voltage ac receiver module was applied as a load to the system. Figure 4.2-13 contains photographs of the output voltages and currents of the three receiver modules. The output of the ac receiver module was variable from 0 to 130 Vrms and dc to 1200 Hz. Because this module delivers more power at its peak amplitude than at zero, it had the effect of modulating the diode current of Inverter 1 (Figure 4.2-14).

Although the receiver modules used for this configuration were basically the same as those used for the single-phase system testing, the total system operating efficiency with a 5.0-kW load was improved from 70.3% to 77.1%. The efficiency gain is mostly due to both an improved transmission line and upgrades made to the inverter modules. Improving the receiver modules (Section 4.2.4), redesigning the system transformers and continuing to develop the inverters indicates that a total system efficiency of 92% is certainly attainable.

Total harmonic distortion (THD) measurements of the system voltage waveforms were taken on a meter with a bandwidth of 200 kHz. Table 4-2 lists the power and THD measurements of the three-phase system with a load of 2.0 kW. The bus distortion is between -21.8 and -28.3 Db and is primarily due to the switching in the receiver modules. Next, as an experiment, the resonant capacitors of all the inverters were decreased from 1.5 to 1.0 microfarads. This increases the resonant frequency from 26.5 kHz to 32.5 kHz and subsequently reduces the power capability of each inverter. It also adds distortion to the inverter output voltage as evidenced by the data in Table 4-3. The THD on the bus was degraded to

between -16.4 and -18.2 Db.

When the 1.5 microfarad capacitor was replaced in the inverters, the power jumped to 5.0 kW and the THD measurements were improved (see Table 4-4). Thd measurements were made at points throughout the system including the output of the variable-frequency, variable-voltage ac receiver. Unfortunately, these measurements were made on this receiver before it was upgraded. The total harmonic distortion measured on the output of the module after it was upgraded (Figure 4.2-13) would have been much lower than the -13.6 Db THD measured on the output of the unimproved module (Figure 4.2-15).

It is apparent that the distortion is caused by the receiver modules. The THD measured on the inputs to the receivers ranges from -16.8 to -24.2 dB while at the inverter output the range is -28.6 to -30.2 dB for the three phases. There is some distortion on each line caused by the other lines. With the other two lines turned off, the THD measured at the output of the inverter was improved for all three inverters over the THD measured on the inverter outputs with the system operating normally. Replacing the capacitive filters of the receiver modules with L-C filters or implementing some other scheme to limit the large, non-continuous currents drawn by the dc and bidirectional modules would greatly improve the THD of the system.

A spectrum analyzer was used to provide photographs of the measurements of the harmonic frequency components of the three-phase system breadboard. Figure 4.2-16 shows the harmonic frequency components of each line of the bus. As would be expected, phase b and phase c have large third harmonic components (60 kHz) because they are loaded by the bidirectional module and dc receiver module respectively. Both of these devices employ capacitive output filters which tend to enhance the odd harmonics. The components of phase a are all below -30 dB and most are below -40dB.

Figure 4.2-17 displays the harmonic frequency components centered at 250-kHz of the line-to-neutral voltage for each phase. There are some rather significant oscillations at around 250 kHz especially on phase b. These oscillations are created by the receivers, but it appears that the line may have its resonant frequency around 250 kHz. Future designs

would assure that the resonant frequency of the parasitic inductance and capacitance of the line are taken into account. Figure 4.2-18 provides evidence that the receivers are the cause of the high frequency components by comparing of the harmonic frequency components of phase c with and without the dc receiver. Most of the high-frequency components are larger when the dc receiver is on the line.

Finally, a man-in-the-loop test was devised to evaluate the "phasor" regulation approach that will be part of the 25.0-kW breadboard system. The circuit of Figure 4.2-19 was used to vary the phase between the two inverters under test. This circuit will only vary the phase between the inverters from 0 to 90 degrees whereas the closed-loop implementation for the 25.0-kW system will be able to vary the angle from 0 to 180 degrees. The tests were performed with a 60-volt nominal input rather than the usual 120 volts because the input voltage was to be doubled during the test, and the power supplies were limited to 130 Vdc.

The results of the measurements are contained in Table 4-5. Figure 4.2-20 shows the leg currents of the two inverters at the 230w power level. The efficiency is low as is expected in the lightly loaded case. The regulation technique was effective. As the input voltage was doubled to 120 Vdc, the bus voltage level was maintained.

However, in the case of a larger load, the leg currents in the inverter become unbalanced as shown in Figure 4.2-21. This affects the shape of the load voltage waveform especially in the 120-volt input case. In the development of the 25-kW power system breadboard, it has been discovered that this unbalance is due to the inverters and their transformers not having matched output impedances. By slightly modifying the resonant components of one of the inverters, this unbalance disappears. The regulation is effective because the input current to the inverter actually decreases as the voltage is increased and the load impedance remains constant. It actually alters the input impedance of the inverters and because there are no additional power dissipating components added, this regulation approach is ideal for a resonant power system.

4.2.6 Steady-State Operation of the 25.0-kW, Three-Phase System.

The single most important improvement in the 25.0-kW power system breadboard upgrade is the incorporation of a closed-loop "phasor" regulation controller to regulate the voltage of the three-phase, 440-Volt bus. With no modification to the inverter resonant components, this technique causes the inverters to become unbalanced as described in Section 4.2.5. In this section, two methods of compensation to eliminate unbalance in the phasor-regulated power system breadboard of Figure 3-18 are examined and compared to uncompensated regulation. The three types of inverter compensation studied were:

A. Uncompensated phasor regulation
B. Capacitive-compensation phasor regulation
C. Inductive and capacitive-compensation phasor regulation

These regulation schemes are explained in detail in the following sections. The phasor regulation technique was implemented in the breadboard with each of these compensation techniques. In all of the implementations of phasor regulation on this breadboard, two inverters are used to provide power to each phase of the bus. The output voltages of the two inverters are summed by connecting them in series to drive the bus. Regulation is performed by shifting the phase between the two inverters. The output voltage of the odd-numbered inverters is delayed with respect to the output voltage of the even-numbered inverters, which are operated from a fixed three-phase clock.

4.2.6.1 Uncompensated Phasor Regulation. The configuration of the two inverters for this implementation of phasor regulation is shown in Figure 4.2-22. Basically, the outputs of the two inverters are coupled in series to sum the voltages at the bus. The outputs of the odd numbered inverters are shifted with respect to the even numbered inverters as shown in Figure 4.2-23. Therefore, the output voltage leads the output current in the even numbered inverters and the voltage lags the current in the odd numbered inverters. So, Inverters 2,4, and 6 see an apparent inductive load, which reduces the effective capacitance of the resonant circuit and hence the power capability.

The photographs of Figure 4.2-24 show the inverter resonant inductor currents at no load and full load for Inverters 3 and 4, which combine to produce the power for phase B. The currents in the two inverters are equal at 60 amperes peak when there is no load. At full load, the peak forward inductor current in the inverters is 70 amperes in inverter number 3 and 50 amperes for inverter number 4. At this point, inverter number 3 is capable of supplying more power than inverter number 4. Indeed, it is seen that the flyback diode current in inverter number 4 is small with respect to the forward current, indicating heavy loading. The ratio of the reverse diode current to the forward current in inverter number 3 is not nearly as small, indicating much lighter loading. Therefore, Inverter4 limits the amount of power that the inverter pair can supply.

This unbalance condition reduces efficiency and total system power level. In fact, the total end-to-end measured system efficiency is 83.9% with a maximum available load power of only 16.2 kW (25kW was required). This unbalance condition can be corrected by the two compensation schemes described in Sections 4.2.6.2 and 4.2.6.3. The situation can also be greatly improved by reducing the nominal phase angle between the inverter voltages. The phase angle between the inverters can be seen for both no load and full load conditions in Figure 4.2-25. It only varies between about 94° and 85° from no load to full load, indicating the inverters are extremely stiff voltage sources.

A 90° regulation phase angle causes the inverters to see a resistive load as a load with a power factor of 0.7 (45° phase shift between voltage and current). Although the inverters can tolerate this large phase angle, it affects the resonant circuit causing some distortion (see Section 4.7.2). It will also increase the distortion when the inverters are loaded with actual power factor loads. By changing the transformer turns ratio, the regulation phase angle could be reduced to 20° or so. In doing so, the inverters will see only a 0.985 apparent power factor (10°) at no load and an even larger (closer to 1.0) apparent power factor with greater loads. A 0.985 power factor has virtually no effect on the inverters whereas a 0.7 power factor has a significant effect.

These angles are large because of some improvements made on the inverters. The simple L-C resonant circuit of the 1.7-kW inverters of the 5.0-kW system (Figure 3-14) has been augmented by adding a capacitor in

series with the resonant capacitor and the inverter output transformer (Figure 3-17). This capacitor blocks dc currents from the transformer primary and also improves inverter distortion and load regulation properties. Another effect is to increase the dc to ac gain of the inverter. So, the inverter output voltage was increased when these capacitors were added to the system. The added voltage pushes the phase angle up to maintain the 440 Volts on the bus.

Table 4-5.1 shows the exceptional bus-voltage load regulation performed by the phasor regulation. In changing the load from 0.0 kW to 16.2 kW, the bus voltage changed 1.6% for Phase A, 0.79% for Phase B, and 0.60% for Phase C. This demonstrates that the bus voltage can be maintained within 1.0% over the full range of loads even if the inverters are not equally sharing the load. Also, the voltage drop along the 50-meter bus was 3.1% on Phase A, 2.9% on Phase B, and 3.4% on Phase C. This is not bad considering that the bus was designed and built to be a 5.0-kW transmission line. However, bus voltage drop is linear with bus current. Therefore, most of the bus drop encountered in the system can be corrected by adding circuitry to monitor bus current and proportionally increase the bus voltage above nominal. The capability to do just this is being incorporated into the 20-kHz NASA Testbeds.

In the uncompensated phasor regulation implementation, the distortion on the power bus was low as shown in the photographs of the three-phase, line-to neutral bus voltage waveforms of Figure 4.2-26. Indeed, the measurements of the total harmonic distortion in Table 4-5.1 show the bus to be relatively free of distortion. The total harmonic distortion was measured on a distortion analyzer with a bandwidth of 200 kHz as in Section 4.2.5 above. The distortion present on the bus did increase somewhat as the load on the system was increased. This is because as the system is loaded, the apparent reactances encountered by the inverters increase with load and have a greater impact on the effective resonant capacitance of the inverters. Varying the value of the resonant capacitor alters the resonant frequency of the inverters, which causes some distortion to appear.

The worst case total harmonic distortion on any of the three-phases of the bus was 2.09% at no load. This rose to 3.80% at a 7.54-kW load and eventually to 4.36% when the system was fully loaded to 16.2 kW.

However, in all cases the worst case distortion on any of the three phases is well below the specification level of 5.0%. In addition, the output waveform of the variable-frequency, variable-voltage ac receiver was clean as shown in Figure 4.2-27. Its total harmonic distortion was 3.02%, well below the 5.0% distortion level.

The next portion of the test program was to determine what frequency components are the major contributors to the bus distortion. Looking at the photographs of the spectrum analyzer screen of Figure 4.2-28 when there is no system load, it is seen that the larger frequency components are the odd harmonics. Of these, the largest is 2.23% of the magnitude of the fundamental 20 kHz and occurs at 60 kHz. The next largest component (the seventh harmonic) occurs at 140 kHz and the magnitude is between 0.79% and 1.4% of the 20 kHz component for the three phases. The magnitude of the remainder of the frequency components are significantly below 1.0% of the magnitude of the fundamental.

Corresponding with the total harmonic distortion measurements made earlier on the system, the magnitude of the harmonic components increases with increasing load. With the system fully loaded (16.2 kW), again, the odd harmonics of the fundamental are significantly larger than the even harmonics (see Figure 4.2-29). The third harmonic (60 kHz) is the largest frequency component with a magnitude as high as 4.47% of the fundamental on Phase A. The fifth harmonic (100 kHz) reaches 2.5 % of the fundamental on all three phases. After these two harmonic components, the only frequency component that has a magnitude greater than 1.0% is the seventh (140 kHz); and this is only on Phase A.

At higher frequencies (100 kHz to 300 kHz), the magnitude of the harmonic components of the three phases are virtually identical and vary only with load. Figure 4.2-30 shows the high frequency harmonic components for one phase of the system for the no load and the full load cases. Above 100 kHz, all of the magnitudes of the frequency components are well below 1.0% of the fundamental and are beginning to approach the lower limits of the spectrum analyzer.

To sum up, the uncompensated phasor regulation implementation has the advantage of extremely low total harmonic distortion, measuring less than 5.0% for any phase of the bus over the entire load range. The bus voltage

load regulation was exceptional measuring less than 2.0% on all of the phases over the complete load range and much better than 1.0% on two of the phases over the same range. The disadvantage of using the phasor regulation without any compensation is that the regulating inverters share the load unequally. This causes lower efficiency and lower power capability (16.2 kW) for the system. One inverter of each pair is not very heavily loaded, causing low efficiency. The power capability is limited by the other, which is heavily loaded.

4.2.6.2 Capacitive Compensation Phasor Regulation. In order to obtain more power from the even-numbered inverters, a capacitor is placed across the resonant capacitors of the these inverters to cancel the apparent inductive power factor that these inverters would otherwise encounter. This is shown in the schematic of Figure 4.2-31. As in Section 4.2.6.1, the phase of the output voltage of the odd-numbered inverters is shifted with respect to the output voltage of the even-numbered inverters, which are operated from a fixed three-phase clock.

For the unloaded case, the inverter inductor currents of inverter number 4 are 90 amperes peak compared with the 65 Amp peak currents of inverter number 3 as shown in the photographs of Figure 4.2-32. Figure 4.2-33 shows the effects of loading on these currents. At 50% load (14.9 kW), the currents become almost equal at 85 amperes peak. When the power is boosted up to the full 25.6 kW, the current of inverter number 3 grows to 110 amperes peak as a reaction to the apparent capacitive load. Because it is compensated, inverter number 4 does not see the reactive load that inverter number 3 does. Its inductor leg current remains constant at 85 amperes peak. The compensation has allowed inverter number 4 to produce more power, which increases both the efficiency and the power capability of the inverters. The maximum efficiency of 85.3% was measured at the full load power of 25.6 kW.

However, although the power level and efficiency were both increased, the odd-numbered inverters are still not being fully loaded as shown in Figure 4.2-33. The next step in compensation is to compensate all inverters so that at full load, the output voltage and current of each inverter is in phase. This approach has been implemented and examined in Section 4.2.6.3.

Now that the even-numbered inverters do not have the apparent inductive power factor to deal with, these inverters operate at increased voltages. As a result, the phase shift between inverters necessary to keep the bus voltage down to 440 Volts RMS is greater (see Figure 4.2-34). The phase between inverters varies from 106° to 94° over the entire 25.6-kW load range. As stated in the previous section (Section 4.2.6.1), when the phase shift is this large, the inverters are presented with a 53° (0.60 power factor) to 47° (0.68 power factor) voltage to current phase angle, which is large for a resonant inverter to handle without waveform degradation. Reducing the phase shift between inverters to a reasonable range such as between 20° and 10° would present the inverters with a 10° (0.985 power factor) to 5.0° (0.996 power factor) voltage to current phase shift, which would have no noticeable effect on inverter operation.

Once again, the phasor regulation of the bus voltage was excellent as shown in Table 4-5.2. Data were not taken for Phase A; but over the load range of 0.0 to 14.9 kW (50% load), there was no change in the line-to-neutral voltage of Phase B. It remained constant at 442 Volts RMS. Over the same load range, the Phase C bus voltage changed from 442 Volts RMS to 444 Volts RMS, a change of 0.45%. The bus voltage load regulation results were just as remarkable for the full 0.0 to 25.6-kW load range. The voltage on each phase varied only 0.23%.

The voltage drop on the 50-meter bus under full load conditions (25.6 kW) was 2.9%. This is roughly the same as measured in Section 4.2.6.1 and is understandable considering the bus was intended for 5.0-kW power transmission. As stated in Section 4.2.6.1, bus voltage drop is linear with current. As such, it can be compensated for by monitoring the bus current and proportionally increasing the bus voltage above 440 Volts RMS.

The waveform distortion is appreciably higher for the capacitive compensation case than the uncompensated. This can be seen in the bus voltage waveforms of Figure 4.2-35. The total harmonic distortion measurements of Table 4-5.2 show the distortion to be somewhat higher, but fairly uniform with load. The worst case distortion is above the goal of 5.0%. It is 6.1% for no load, 6.4% for 50% load (14.9 kW), and 6.6% when the full 25.6 kW is on the bus. However, the purity of the output waveform of the variable-frequency, variable-voltage ac receiver was unaffected by a change in the compensation approach. It again had low

harmonic distortion (4.2%). See Figure 4.2-36.

The major contributors to the distortion in the unloaded case were the third (60 kHz), seventh (140 kHz), and eighth (160 kHz) harmonics of the fundamental 20 kHz component as seen in the photographs of Figure 4.2-37. The third was the largest contributor, being 2.8% of the fundamental. The seventh and eighth harmonics were about 1.0% and all other components were below 1.0% of the fundamental. For Phase A, there was also a frequency component of 3.0% of the fundamental at 60 Hz due to the modulation of the bus by the ac receiver, which had been commanded to a 60 Hz output frequency. Since the frequency converter load was only connected to phase A, this distortion did not appear on either phase B or phase C. The reaction time of the phasor regulator was not set fast enough to correct for the 60 Hz modulation of power caused by this receiver.

Under full load conditions (25.6 kW), the odd harmonics are the main contributors to the waveform distortion on the bus as seen in Figure 4.2-38 and 4.2-39. The largest of these is the third harmonic (60 kHz), which has a magnitude of almost 4.0% of the 20 kHz. The fifth harmonic (100 kHz) is around 2.2% and the seventh (140 kHz) about 1.6%. The remainder of the frequency components are not significant, having a magnitude less than 1.0% of the magnitude of the 20 kHz component.

In summary, by compensating the output of the even-numbered inverters, the power output of those inverters has been increased relative to the other inverters. This has improved both the efficiency and the power output capability of the system. However, the two inverters of each regulating pair still cannot be equally loaded, limiting efficiency. In addition, the total harmonic distortion on the bus is higher with capacitive compensation than with the uncompensated system described in Section 4.2.6.1 above. The worst case distortion increased from 4.36% for the uncompensated case to 6.6% for the capacitive compensation approach, slightly more than a 50% increase. The distortion measurements for this compensation approach exceeded the goal of 5.0% in most load cases.

4.2.6.3 Inductive and Capacitive Compensation for Phasor Regulation. In this approach to implementing phasor regulation, the output of each inverter is compensated with reactances to cancel the apparent power factors encountered by the inverters in phasor regulation as shown in

Figure 4.2-40. A capacitor is placed in parallel with the output of the even-numbered inverters to align the output voltage and current of each of these modules at full load as was done in the previous section (Section 4.2.6.2). In addition, a parallel inductor is added to the output of the odd-numbered inverters. The phasor regulation creates a capacitive phase shift between the output voltage and current of the odd-numbered inverters. The parallel inductor is sized to cancel this capacitive phase shift at full load power, the point at which balancing inverters is most critical. So, at full system load the inverter output voltage and current are in phase for all six inverters. In this way, all inverters are able to be fully loaded, which increases the system efficiency.

This compensation has some interesting effects on the resonant inverters. When the inverters are unloaded, the inductor leg currents of the inverters are very different as shown in the photographs of Figure 4.2-41. Because there is no large reactive phase shift to cancel, the compensating components have a significant effect on the resonant circuits of the inverters. The parallel compensating inductor of the odd-numbered inverters diminishes the effective resonant capacitance increasing the resonant frequency and decreasing the resonating current in these inverters. Likewise, the parallel compensating capacitor of the even-numbered inverters adds to the effective resonant capacitance of these modules decreasing the resonant frequency, which in turn increases the resonating current in these modules. The peak inductor branch currents in the photographs are 34 Amps for inverter number 3 and 88 Amps in inverter number 4.

When the system is loaded to the 50% level (14.6 kW), the peak currents of the two regulating inverters are virtually equal at 66 amperes (see Figure 4.2-42). However, inverter number 3 has less flyback diode current and is thus more heavily loaded. Its parallel compensating inductor impedance is still larger than the capacitive effect of 50% resistive load. Similarly, inverter number 4 has more power capability because its compensating capacitor is larger than the inductive effect of 50% resistive load.

When the load reaches the full load level of 27.5 kW, the percentage-wise loading on the inverters is equal as shown in Figure 4.2-43. There is some mismatch of the peak inductor leg currents indicating that the inverters

are not sourcing the same amount of power. However, the inverters are loaded to an equal degree, meaning that each is operating at the same efficiency. Neither is limiting the system efficiency, which is the goal of compensation. By adjusting the compensating components more precisely, the power contributions of the inverters can be made identical, but this is not necessary as long the efficiencies are identical. Indeed, using this compensation method, an end-to-end efficiency of 87.3% was achieved at 27.5 kW, which is the highest efficiency achieved on any of the breadboard tested in this entire test program.

The phase shift between the inverter voltages is again large as shown in Figure 4.2-44. The phase shift is around 100° as in the previous two implementations of phasor regulation. If this phase shift was reduced to around 20°, the apparent voltage to current phase angle encountered by each inverter would be a mere 10° (0.985 power factor), which would only have a negligable effect on the resonant circuit of the inverters. The need for compensation would most likely be eliminated. If an inductive and capacitive compensation scheme were needed at all,it would be much simpler to implement. The parallel impedances would be greatly increased over the values in this breadboard. This would drastically reduce any remaining unbalance between inverters and would also greatly diminish the bus waveform distortion as explained in the paragraphs that follow.

The results of the regulation and total harmonic distortion measurements are shown in Table 4-5.3. As the load was increased from 0.0 kW to 14.6 kW, the voltage on Phase A deviated only 0.02%. The regulation on Phases B and C is also quite good, 0.11% and 0.25% respectively. Over the full range of 0.0 kW to 27.5 kW, the gain of Phase B was not high enough and the bus voltage strayed 2.4%. However, Phases A and C demonstrated that better than 1.0% regulation was certainly possible over the entire load range. Each of these recorded a 0.52% voltage variation.

Table 4-5.3 also shows a voltage drop along the 50-meter bus of between 4.04% on Phase A to 4.6% on the other two phases. There are two reasons that this is larger than the 3.0% that was recorded for the other two implementations of phasor regulation. First, the system power level and thus, the bus currents are higher in this compensation method. Secondly, because of the large amount of power (27.5 kW) required to fully load the system for the inductive and capacitive compensation method and the fact

that the EMHP300-200 dc power supply can only source 200 amperes, the measurements on each phase had to be run with the other two phases turned off. Doing this causes current to flow in the neutral of the wye-connected bus, which sees no current in balanced three-phase operation. The additional voltage drop in the neutral adds to the normal bus voltage drop measured in a three-phase system.

It should be noted that for this same reason, the measured efficiency of 87.3% would be higher with all three phases running simultaneously because the power dissipation in the neutral would be eliminated. However, any bus voltage that is present in the system can be corrected as described in Section 4.2.6.1 because bus voltage drop is proportional to current. As such, it can be corrected for by monitoring the bus current and increasing the bus voltage above 440 Volts RMS linearly.

As can be seen from the photographs of the bus voltage waveforms in Figures 4.2-45 and 4.2-46, the waveform distortion is fairly high, but it decreases rather substantially with load. Table 4-5.3 shows the worst case bus waveform distortion to vary from 7.3% at no load, to 6.8% at 50% load, and all the way down to 4.7% at full load, where the compensation was designed to work. By operating with a much smaller nominal phase shift between inverters, such as 20° instead of 100°, the bus total harmonic distortion would not ever get much above the 4.1% to 4.7% measured at the full-rated power. Then, the system with inductive and capacitive compensation would then meet the 5.0% distortion goal at all load power levels.

Figures 4.2-47 and 4.2-48 show the frequency components for the low and high frequencies on the three phases of the bus while it is unloaded. The significant frequency components of the observed distortion are the third (60 kHz), fifth (100 kHz), and eighth (160 kHz) harmonics of 20 kHz. The third harmonic reaches 5.6% of the magnitude of the 20 kHz. Surprisingly, the eighth harmonic of 20 kHz is the next largest, but only is 1.8% of the 20 kHz component. The fifth harmonic is 1.4% of the fundamental component. The remainder of the frequency components are below 1.0% and thus, inconsequential.

As expected, the frequency components contributing to the bus distortion are much reduced when the system is fully loaded. The photographs in

Figure 4.2-49 show the results of the spectrum analyzer measurements for Phase B and C (Data were not taken for Phase A). The third (60 kHz) and fifth (100 kHz) harmonics of 20 kHz are now the only significant frequency components. The magnitude of the third is 3.2% of the fundamental and the fifth is 1.4%. These reductions with load reflect the reduction in total harmonic distortion with increasing load.

In summary, the inductor and capacitor compensated implementation of phasor regulation proved to be the most efficient. This was achieved by balancing the loading of all inverters at full load. Although it had high waveform distortion under no load, it had less than 5.0% total harmonic distortion at full load. However, since this method of compensation was relatively new at the time of testing, capacitive compensation was chosen as the method of phasor regulation to be used in all the tests in the 25.0-kW phase of the test program because it does improve the efficiency over uncompensated phasor regulation.

4.2.7 Conclusions and Recommendations

The initial portion of the testing (2.0-kW, single-phase power system breadboard) has demonstrated that resonant inverters are efficient and versatile as system building blocks. The 1.0-kW inverter breadboards are 96.9% efficient. The inverters can supply power over long distances (50 meters) to active load modules. When the bidirectional module was operated in its dc-to-ac mode, it performed just as efficiently as the inverters. The testing also illustrated how the resonant system is inherently modular. Two inverter modules were synchronized to power the same bus and share the load equally. Three different modular load-interface units were powered by this bus. Although the total system efficiency was not very high, its 70.3% efficiency is not unreasonable considering that the bus was only 90% efficient, the transformers were between 90% and 95% efficient, and many improvements remain to be made on the other system components. It must also be remembered that at this point in the program efficiency was not the principal goal, and therefore no attempt was made to optimize it.

Proof-of-concept of a three-phase, 5.0-kW power system breadboard was also demonstrated. Predictably, its RMS input ripple was less than 3%. With only a new transmission line and improved inverters, the efficiency

of this breadboard was increased to 77.1%.

In the case of a larger load, the leg currents in the inverter become unbalanced as shown in Figure 4.2-21. However, the line voltage was maintained at 250 Volts, even though the shape of the bus voltage waveform does exhibit some distortion, especially in the 120-Volt input case. In the development of the 25.0-kW power system breadboard, it has been discovered that this unbalance is because each of the regulating inverters experiences an apparent power factor. In a two-inverter regulation scheme, one inverter sees an apparent lagging power factor, and the other an apparent leading power factor. By slightly modifying the resonant components of one or both of the inverters, as explained in Section 4.2.6, this unbalance can be corrected.

This "phasor" regulation technique is effective because the line voltage regulation is good over input swings of greater than ±50% and the input current to the inverter actually decreases as the voltage is increased with a constant load impedance (See Table 4-5.). It successfully alters the input impedance of the inverters. Because there are no additional power dissipating components added, this regulation approach is ideal for a resonant power system.

Many improvements have been made in the 25.0-kW power system breadboard. The most significant of these is the closed-loop, phasor regulation used to regulate the three-phase bus voltages. The controller regulates by varying the phases between two inverters and summing the sine wave outputs. It adds no power losses and is able to regulate to better than 1.0% over the entire load range. In one instance, the regulation of the bus voltage was measured to be 0.23% over the load range of 0.0 kW to 25.6 kW.

Three different methods of phasor regulation were evaluated for efficiency, bus waveform purity, load regulation, and inverter load sharing ability. In terms of these characteristics, the best implementation of phasor regulation turned out to be adding a parallel inductor or capacitor to the output of each inverter (inductive and capacitive compensation). By canceling the apparent power factor encountered by all six inverters, phasor regulation is implemented in such a way as to maintain balanced power and efficiency in all the inverters. With phasor regulation

implemented in this manner, the total harmonic distortion at full load is under 5.0%.

However, by reducing the nominal phase shift between inverters to 20°, the need for compensation would be eliminated. The inverters would encounter a power factor of 0.985. The effect of this on the inverters would be slight. Uncompensated inverters would be balanced over the entire load range. This reduction in nominal phase shift would produce a combination of the highest possible efficiency, the lowest possible bus distortion, and the elimination of the need for compensation. If compensation were still desired, it would be slight and easily implemented because the impedances required would be large (large inductors and small capacitors).

The six inverters and inverter transformers were newly designed and built for the 25.0-kW system breadboard. These new components combined with the inductive and capacitive compensation phasor regulation produced the most efficient breadboard of all the configurations tested in this test program. The end-to-end system efficiency was 87.3% even though the 50-meter bus was designed to be 99.5% efficient for only 5.0 kW. Because the power dissipation is proportional to the square of the current, increasing the power level on this line from 5.0 to 25.0 kW multiplies the power loss in that line by 25. So, the bus power dissipation is a major portion of the losses in this breadboard and replacing it with a properly rated line would put the system efficiency very close to the goal of 92% total system efficiency.

Further improvements are possible, the development of a unity power factor receiver module would increase system efficiency and reduce the bus waveform distortion. Other improvements can be made in the present receiver module designs. These include center-tapped transformer rectifier designs and output voltage regulation of receiver modules from the high-voltage side of the step-down transformer.

Improvements in the inverters can also be made. Since the majority of the power loss in an inverter is attributable to the SCRs, alternatives should continue to be explored. Although proof-of-concept resonant inverters with MOSFET and D60T transistors have been built, an efficiency study has not yet been completed. Such a study will be performed and will include

SCRs, GTOs, MOSFETs, bipolar transistors, insulated-gate FETs, and other power semiconductors available in this power range.

4.3 TRANSIENT LOAD RESPONSE

The purpose of this section of testing is to observe and measure the response of the power system and its modules to instantaineous changes in the user loads. A spacecraft power system should be oblivious to any changes in the user loads provided they are within the power capability of the system. This section describes how the resonant inverter and the various resonant power system configurations that were tested satisfied this requirement.

4.3.1 Transient Load Response of a Single Inverter

The inverter circuit is shown in Figure 3-6 and the circuit used to abruptly change the inverter load is shown in Figure 4.3-1. Three load change cases were tested:

a. 0.0 W to 580 W and reverse
b. 580 W to 1110 W and reverse
c. 130 W to 1110 W and reverse

The most dramatic power change takes place in the 130 to 1110-w case. Yet, the inverter experienced only a short and smooth transition period as shown in figures 4.3-7 and 4.3-3 which show the inverter output voltage and current for the 130 to 1110-w and 1110 to 130-w case respectively. Discounting the switch bounce in Figure 4.3-2, these figures show that the overshoot of the inverter is small and the entire transient response lasts only about three periods or 150 microseconds. The other inverter parameters such as the leg current (Figure 4.3-4) also show a smooth and brief transition for abrupt load changes. The transient response characteristics in the other two cases (0.0 w to 580 w and reverse, and 580 w to 1110w and reverse) lasted for a shorter amount of time because the load variation was not as great.

4.3.2 Transient Load Response of a Single Driver and Receiver

The schematic of the closed-loop, voltage-regulated dc receiver module is

shown in Figure 3-7 and the transient load response test circuit in Figure 4.3-5. Again, three load cases were measured:

a. 0.0 W to 180 W and reverse
b. 180 W to 410 W and reverse
c. 34 W to 410 W and reverse

In all of these cases, the load switching is accomplished with no major glitches. However, the transient response time of the system is substantially longer than in the case of just a single inverter because of the time it takes for the dc receiver module control circuit to respond to a change in load. This is shown clearly in the photographs of the dc receiver module output voltage and filter current and the inverter leg current in Figure 4.3-6. The settling time of the system response for a load change of 180 w to 410 w is on the order of 2.0 milliseconds. The increase in the settling time over the 150 microseconds measured on just the inverter (Section 4.3.1) can be attributed to the low cutoff frequency of the low-pass filter in the feedback of the dc receiver controller. This frequency was intentionally raised in the dc receiver module when it was tested in the three-phase system configuration (Section 4.3.4) and its settling time was much less.

4.3.3 Transient Load Response of the Single-Phase System

For this test configuration, the loads were switched on each receiver module while the other two receiver modules were operating at normal power levels. The test circuitry is shown in Figure 4.3-7 and the schematics of the dc, ac, bidirectional modules, and the inverters are shown in Figures 3-7, 3-11, 3-9, and 3-6 respectively. The bidirectional module was operated in the 20- kHz-to-dc mode throughout this test. The load resistor on the ac receiver module was never actually changed during this test. Rather, the control electronics for this module was turned on and off with a switch to observe the effect of abruptly adding and removing a module from the transmission line.

The ac receiver module was turned on and off into a 200 w load. The output of the module reached the steady-state operating conditions in less than 0.5 milliseconds as shown in the photographs of Figure 4.3-8 which shows the output voltage for both the turn-on and turn-off cases. The

branch current of Figure 4.3-9 shows that the inverter also responds smoothly and quickly to the load change.

Measurements were taken as the load on the bidirectional module was changed from 210 w to 410 w and back. The control circuitry of the closed-loop controlled bidirectional module responds to the load change in about 200 microseconds as shown in the photograph of the output voltage and filter current (Figure 4.3-10). There is virtually no change in the output voltage of this module as the load is changed demonstrating that this load change is effectively transparent to the system.

The output voltage and filter current of the dc receiver module as the load is increased from 200 w to 420 w are shown in Figure 4.3-11. The low cutoff frequency of the feedback filter is again apparent as the current being drawn by the module does not reach steady-state conditions until 4.0 milliseconds have passed. Modifying the filter will alter the settling time.

4.3.4 Transient Load Response of the 5.0-kW Three-Phase System

In this test of transient load response, the loads on each of the three receiver modules was switched individually and then the loads on all three modules were switched at once. The schematics for the receivers that were used in this test; the dc, bidirectional , and the variable-voltage, variable- frequency ac; are shown in Figures 3-7, 3-9, and 3-15 respectively. The test circuit used is shown in Figure 4.3-12 and the inverter schematic is shown in Figure 3-14.

The circuit used to measure the three-phase system response as the dc receiver load was switched from 0.0 w to 730 w and back is shown in Figure 4.3-13. The photograph of Figure 4.3-14 shows that there is no noticeable change in the output voltage of the dc receiver as the 730 w is applied and removed. The response time of the system is about 500 microseconds as shown in the leg current of Figure 4.3-15. This is considerably shorter than the 2.0 and 4.0 millisecond times observed in sections 4.3.2 and 4.3.3 because the cutoff frequency of the feedback filter has been raised.

A relay was used to switch the 100-volt output of the bidirectional

module (Figure 4.3-16). The leg current of Inverter 2 (Figure 4.3-17) shows the settling time of the system to be about 300 microseconds as the load on the bidirectional module is changed from 0.0 w to 980 w.

Switching the load on the variable-voltage, variable-frequency ac receiver module from 170 w to 400 w was performed with the circuit of Figure 4.3-18. The output voltage of this module is not regulated and the settling time is about 150 microseconds, the same as an inverter with a resistive load (see Section 4.3.1). Figure 4.3-19, the photograph of the output current of the module, shows that the current starts and stops abruptly but without any transients. There is a 100-millisecond transient that is caused by the temperature rise in the incandescent light bulb load which increases the load resistance and subsequently decreases the load current.

Finally, the loads on all three receiver modules were switched simultaneously as shown in Figure 4.3-12. Switching glitches are nonexistent on the system input as the system load is changed abruptly from 170 w to 2190 w as shown in Figure 4.3-20. Although the relays exhibit some bounce as the loads are switched off, the system responds very quickly to a heavy and sudden load change. Because the system bus is unregulated, there is some decrease in the bus voltage as the load is increased. Figure 4.3-21 shows the line-to-neutral voltages on the three-phase bus as the total system load is pushed to 2200 w. The response of each individual inverter module to the simultaneous load change is essentially the same as discussed in the paragraphs dealing with single-load switching because each inverter drives one phase and thus one receiver.

4.3.5 Transient Load Response of the Three-Phase, 25.0-kW System

The voltages and currents of the system were monitored as the full loads of the receiver modules were individually switched on and as the full three-phase resistive load was switched on and off the bus. Unlike in previous tests, the switching was performed with SCRs, which provide much faster switching than the relays used previously.

The SCR circuit used to apply the 705-W load to the dc receiver module is shown in Figure 4.3-22. The photographs of Figure 4.3-23 show that the load voltage and current are supplied instantly and with no overshoot. The

ripple present in the photographs is due to the limitations of the electrolytic capacitor in the 40-kHz environment. Figure 4.3-24 shows the effect of the load switching on the bus voltage and current. The bus current makes a smooth and rapid transition from 10.6 amperes RMS to 12.7 amperes RMS. The effect of the load switching on the bus voltage is undetectable. Like the bus current, the response of the inverters is smooth and rapid, with no overshoot as seen in the photographs of the inverter inductor leg currents of Figure 4.3-25.

The circuit used to switch the load on the bidirectional receiver module from 20 to 816 W is shown in Figure 4.3-26. The bidirectional receiver was operated in the dc output mode for this test. Unlike the test on the dc receiver, the output voltage monitored was the capacitor voltage (module output voltage) as opposed to the load voltage. The power output capability of this module is limited to about 1100 W of instantaneous power. Since the resistance of the load light bulbs is low when they are cool, the output voltage droops because of the large load current and the 1100-W limitation (see Figure 4.3-27). As the resistance increases, the voltage returns to 100 Volts and the current to 8.2 amperes. Again, the load switching of this module has no effect on the stiff bus voltage as shown in Figure 4.3-28.

The circuit of Figure 4.3-29 shows the switching circuit used to switch the load on the ac receiver from 190 to 490 W. The output current displays a large overshoot primarily due to the changing resistance of the light bulb load (see Figure 4.3-30). The bus voltage is not affected by the transition (see Figure 4.3-31). The bus current shows a smooth transition.

Next, 21 kW of resistive load was applied instantaneously to the bus. The circuit used is shown in Figure 4.3-32. When the load was applied, a current surge of 130 amperes was measured with an ac current probe on the dc system input as shown in Figure 4.3-33. Figures 4.3-34 and 4.3-35 show the effects of the load switching on Phases A and C. Although there is no current overshoot, there is a large voltage overshoot of 160 Volts on the bus, which lasts briefly (300 to 400 μs). As expected from the steady state testing of Section 4.2.6.2, the odd-numbered and even-numbered inverters react differently. Because of the apparent power factors encountered by the inverters, the even-numbered inverters absorb

the majority of the load after the same 300 to 400 μs transient period.

The reverse test was then performed with the circuit of Figure 4.3-32. This transition was again handled very smoothly by the system. As shown in Figure 4.3-36, the bus current goes to zero abruptly and the bus voltage changes only slightly. The transient period lasts only 200 μs (4 periods).

4.3.6 Live Inverter Replacement.

This test was devised to demonstrate how easily inverters could be added or removed from a loaded, operating system. One inverter (Inverter 6) was connected to a 100-meter transmission line into a 5.5-kW load. A second inverter (inverter number 4) was then switched on and off the bus with the circuit of Figure 4.3-37. The effect on the load voltage and current as the second inverter is switched into the system is only a momentary rise and fall in voltage as shown in the photographs in Figure 4.4-38. The output currents of the inverters show a smooth transition over 400 to 600 μs. Figure 4.3-39 shows the perfect load sharing of the two inverters. The photograph on the left shows the inverter inductor leg currents before inverter number 4 is added to the bus. Inverter 6 is heavily loaded and inverter number 4 is unloaded. The photograph on the right shows the two inverters to be loaded equally after inverter number 4 has been added to the system. This test shows that addition or removal of inverter modules to or from operating power systems is undetectable by the user.

4.3.7. Transient Load Response Conclusions.

Sudden load variations appear nearly transparent to the resonant power system. The receiver modules were able to maintain their output voltages for instantaineous no-load to full-load fluctuations. The system responded with little overshoot. Within six to ten periods (300 to 500 microseconds), the transients had settled out. Even when the loads on all three phases of the 5.0-kW, three-phase power system breadboard were switched simultaneously, the system responded smoothly and returned to steady-state conditions within 1.0 millisecond.

When 21.0 kW of load was abruptly switched on and off the bus in the 25.0-kW system breadboard, the bus returned to its steady-state condition in only 400 us. In addition to its tolerance of abrupt, large load changes,

the system was demonstrated to be perfectly suited to the replacement of modules (inverter or receivers) without affecting the operating of the system or any of the user loads. This was clearly illustrated in a test in which an inverter was switched into an already operating and loaded system to share the load perfectly. Any change was virtually unobservable by the load.

4.4 OUTPUT RESPONSE TO CONTROL SIGNAL CHANGES

The purpose of this test was to measure the gain of the receiver modules, to record the response of each receiver module to step changes in its reference control signal, and to measure the frequency response of the modules.

4.4.1 Control Signal Response of the DC Receiver with a Single Driver

A schematic of the dc receiver is shown in Figure 3-7 and it is basically a phase-controlled, full-bridge rectifier. The output voltage at the load is fed back and compared to a dc reference signal to produce an error signal. This error signal then modifies the firing angle of the SCRs accordingly. The load voltage is graphed versus the reference signal voltage for two different resistive loads in Figure 4.4-1. The graphs show that the control system is very linear with a gain of 3.75. In the heavier load case, the gain becomes nonlinear at a certain point. At this point, the firing angle of the SCRs is zero and can go no lower. Since the transmission line that was used in this configuration has significant loss, the voltage at the input to the receiver is lower than the voltage at the inverter end of the bus. Therefore, the load voltage is now limited by the step-down ratio of the dc receiver transformer and the transmission line voltage.

The nonlinearity in the dc receiver module can be easily corrected. First, this effect will not be present when a low resistance, low inductance transmission line is implemented. Second, if desired, the receiver transformer can be sized so that the receiver always operates in the linear region even with a high-loss transmission line. Finally, a receiver module that draws a more continuous current would would not draw the large currents that the present dc receiver draws from the inverter. This would reduce the end-to-end voltage drop on the line and the output voltage of the dc receiver under loads would not be as limited. As

explained in the start up section, simply replacing the capacitive filter with an L-C filter would cause the current to be more continuous.

Next, a square wave was connected to the reference signal input to record the response of the dc receiver to step changes in its reference signal. The logic circuitry of the receiver responds quickly to the change in the reference signal as shown from the output current photographs of Figure 4.4-2. The output voltage, on the other hand, takes 15 milliseconds to reach its steady-state value because the dc receiver filter capacitor, which is 4500 microfarads, stores a tremendous amount of energy and has a large time constant.

The final portion of the testing of the dc receiver in this configuration was the frequency-response section. In this test, the reference signal of the dc receiver was modulated with an ac signal. The output voltage and the reference voltage are shown in Figure 4.4-3 for the 100-Hz, 1.0-kHz, and the 2.0-kHz cases. The receiver responds well to the 100-Hz modulation, reproducing the reference signal on the receiver output. At 1.0 kHz, the response of the receiver begins to fall off. By 2.0 kHz, the ac part of the output voltage is barely existent. Again, this due to the R-C time constant of the receiver output and not its control circuitry.

4.4.2 Control Signal Response of the AC, DC and the Bidirectional Modules With Dual Drivers

The initial part of this test was to measure the control signal gain of both the dc receiver and the bidirectional module. One of the resistors on the dc receiver circuit card was changed since the testing discussed in the previous section was performed. The gain of this module is now 4.00 as shown in the graph of Figure 4.4-4. The output voltage of the bidirectional module has been graphed versus its reference signal voltage in Figure 4.4-5. The gain of these modules is constant to a certain point at which the voltage drop on the line becomes so large that the SCRs are down to a zero conduction angle. The receiver output voltage is then determined by the turns ratio of the transformer.

As explained in the previous section, this is not a problem because a low loss, low inductance bus and a receiver module that is more of a continuous current source will reduce the line voltage drop and thus the

nonlinearity of the receiver. If a totally linear gain is desired, the transformer can be sized accordingly.

Since the frequency response of the dc receiver is covered in Sections 4.4.1 and Section 4.4.3, it is not discussed in this section. Likewise, the bidirectional module frequency response is explained in section 4.4.3 and not here. However, the frequency response of the 400 Hz ac receiver is discussed. The ac receiver schematic is shown in Figure 3-11.

Photographs of the output voltage and the input current of the L-C filter are shown in Figure 4.4-6 for 100-Hz and 2.0-kHz reference signals. The receiver module maintains a sinusoidal output voltage over the entire frequency range. In the 2.0-kHz case, the 20-kHz components are clearly visible as there are only ten 20-kHz pulses per 2.0-kHz half cycle.

4.4.3 Control Signal Response of the DC, Bidirectional, and Upgraded AC Receivers in a Three-Phase System

The graphs of the output voltage versus reference signal level for the dc receiver and the bidirectional module are shown in Figures 4.4-7 and 4.4-8 respectively. Although there is some nonlinearity, the graphs show that the controller is linear until the output voltage reaches a certain value. After this point, the output voltage maintains a constant level independent of further increases in the reference signal. This value is 28.5 Vdc for the dc receiver and 123.8 Vdc for the bidirectional module. This shows that the there is not much sag in the bus voltage but rather a sudden limit set by the step-down ratio of the transformer. This is because the transmission line used in this configuration is much more efficient than the one used in Configuration 4. In other words, changing the transformer ratios for these modules will extend their maximum operating voltage.

The ac receiver was upgraded from the one tested in Configuration 4. The new receiver (Figure 4.4-8) has both variable-voltage and variable-frequency capability. Its control signal gain was measured with the module operating at 60 Hz and at 400 Hz. The graphs of these measurements are shown in Figure 4.4-9. These graphs are also linear except when the output voltage becomes limited by the receiver input voltage.

To evaluate the response of the receivers to changes in their control signals, the receiver module reference control inputs for the dc and bidirectional receiver modules were replaced by square waves. Figure 4.4-10 shows a block diagram for the dc receiver module control circuit and the square wave that was input to the circuit. The output voltage and the square wave reference signal are shown in the photograph in Figure 4.4-11. The output responds with a slew rate determined by the time constant of the output capacitor and the load resistor.

A block diagram of the bidirectional module control circuit showing the square wave reference signal is illustrated in Figure 4.4-12. The output waveforms of the bidirectional module and the reference signal are shown in Figure 4.4-13. The voltage is well regulated, but the current changes throughout the entire period of the square wave. This is because the resistance of the incandescent light bulb loads decreases as they get warm (increased current) and increases as they cool (decreased current). The final measurement for each of the receiver modules in this configuration was the frequency. For the dc receiver module, the nominal reference signal was modulated by an ac signal of various frequencies as shown in Figure 4.4-14. From the photographs of the dc receiver output waveforms and the reference signal of Figure 4.4-15, the receiver follows the 10-Hz reference signal.
The response of the module starts falling off at 100-Hz. The output of the module shows no effect of the 1000-Hz modulation. The frequency response of this module starts falling at a lower frequency than it did when it was tested in Configuration 4 because the output capacitor of the receiver was increased from 4,500 to 19,000 microfarads and the R-C time constant has increased proportionally.

The circuit used to measure the frequency response of the bidirectional module is shown in Figure 4.4-16. The time constant of the bidirectional module is also large due to its 700μF capacitor and larger load impedance as shown in the photographs of the output waveforms of Figure 4.4-17. The frequency response falls off at around 100 Hz. By taking a look at the input current to the power system for the 100 Hz and 1.0-kHz cases (see Figure 4.4-18), it is noted that the control circuit of the bidirectional module has a much higher fall-off frequency than the output since the input current and thus the current into the bidirectional module follows the reference signal past 100 Hz and starts falling off out around 1.0 kHz.

The block diagram of the ac receiver module controller is shown in Figure 4.4-19. The reference signal of this module was varied from 10 Hz to 1.0 kHz. The module was able to maintain its sinusoidal waveshape and output voltage over the entire range as shown in Figure 4.4-20.

4.4.4 Conclusions and Recommendations for the Receiver Modules

Although the phase-control receivers may not be the optimal load-interface modules as described in Section 4.2, they had very good responses to the control signal tests. The control signal gain was linear once the original, high-loss transmission line was replaced by the improved 5kW version as discussed previously in paragraph 2.6. The receivers responded to step changes in the control signals quickly and with no switching traansients. In addition, the operation of ac receivers was demonstrated over the output frequency range of 10 Hz to 2.0 kHz.

4.5 POWER SUPPLY SENSITIVITY

The purpose of this test was to measure the sensitivity of the system parameters as the input voltage was increased or decreased 20%. Data was recorded for both the steady-state and transient cases.

4.5.1 Power Supply Sensitivity of a Single Inverter

The test circuit of Figure 4.5-1 was used to gather both the transient and steady-state data on this configuration. The steady-state measurements of the power sensitivity are listed in Table 4-6. Since the inverter is unregulated, its output voltage changes the same percentage as the input voltage, and the sensitivity is 1.0 as expected. In Table 4-6, the efficiency of the driver appears low because the inverter is not fully loaded.

In the transient case, the relays switch fast but when the input voltage is decreased, the settling time is determined by the time constant of the input capacitor (700 microfarads) and the load resistance. This capacitor can store about 1.0 Joule of energy at 90 Vdc, which is enough to supply 1.0 kW for 1.0 millisecond. Indeed there is a period of about 0.3 milliseconds when neither relay of Figure 4.5-1 is closed, and the input

capacitor supplies all the power to the load. Figure 4.5-2 shows the input current to the input capacitor going to zero for 0.3 milliseconds. Otherwise, every parameter in the system shows a smooth transition such as the inverter output voltage (Figure 4.5-3). The shift to a higher input voltage is also a smooth transition, but its time constant is much longer and is determined by the response time of the power supplies.

4.5.2 Power Supply Sensitivity of the DC Receiver with a Single Driver

The circuit shown in Figure 4.5-1 was also used to gather the data on this configuration and the measurements are recorded in Table 4-7. There was a 20% decrease in dc receiver output for a 20% decrease in input voltage. This was somewhat better for the other case in which the output only increased 10% for a 20% increase in input voltage. As described in Section 4.4, this is caused by the line voltage dropping with load. The reference voltage was set to deliver 28.0 Vdc, but the receiver didn't even manage that with a system input voltage of 87 Vdc. As the input voltage and thus the line voltage decreases, the load voltage follows suit. On the other hand, when the input voltage increases, the dc receiver output increases to 28.0 Vdc at some level of input voltage and the module resumes regulating to hold the voltage to 28 Vdc.

The dc receiver module is certainly capable of regulating itself as discussed in Section 4.5.3, where its power supply sensitivity is measured to be only 1.6%. This means that the output of the dc receiver changed 0.3% as the input voltage was increased 20%. With an improved transmission line, good voltage regulation of the receivers is not a problem.

Once again, the transient response of the system to changes in its power supply voltage level is very smooth. This is verified by the photographs of the dc receiver output waveforms (Figure 4.5-4) taken when the input voltage is increased and decreased. The settling time is determined by the power supply for the increasing case and the time constant of the input capacitor and the load for the decreasing case. The small transients in the output voltage of the receiver for increasing voltage are caused by the relay contacts bouncing.

4.5.3 Power Supply Sensitivity of the Single-Phase System

The test circuit of Figure 4.5-5 was used to measure the sensitivity of the entire single-phase power to changes in the input voltage. The sensitivity data for all three receivers are presented in Table 4-8. For these measurements, the loads on the receivers were decreased to reduce the voltage drop on the line. The dc receiver output voltage decreased 8.6% for the corresponding 20% decrease in input voltage and increased only 0.3% for the 20% increase in input voltage. The bidirectional module also performed well. For 20% input voltage swings, its output voltage only decreased 4.0% and increased 1.0%. Because the ac receiver tested here did not have closed-loop regulation, it had no way to perform as well. Table 4-8 demonstrates that it is possible to design and implement receivers in a resonant power system that have voltage regulation capabilities better than 0.5%.

The tight regulation of the bidirectional module and the dc receiver is further shown by the photographs in Figure 4.5-6 and 4.5-7. Figure 4.5-6 shows the input voltage of the system and the output voltage of the bidirectional module as the input voltage is switched from 85 Vdc to 68 Vdc. Figure 4.5-7 shows the system input voltage and the output voltage of the dc receiver as the input voltage increases from 85 to 102 Vdc. The change in either of these output waveforms is difficult to detect.

4.5.4 Power Sensitivity of the Three-Phase System

The testing was done slightly differently for this configuration as shown in Figure 4.5-8. Four power supplies were connected in series, and one of them was turned on and off from a remote switch. A list of the input voltages and output voltages of the three-phase system for three different input voltages is contained in Table 4-9. Unfortunately, as described in section 4.4.4, the receivers are set up to deliver their nominal output voltage with a 120 Vdc input. Since the power supplies were not able to deliver much more than 120 Vdc, the input voltage test levels were selected as 80 and 100 Vdc even though the receivers were not able to deliver their nominal voltage at 80 and 100 Vdc. As a result, the regulation of the receivers does not appear to be good even though a sensitivity of the dc receiver output to input voltage changes of 1.6% was measured in section 4.5.3. Had voltages of 120, 145, and 160 Vdc been selected as the test levels, the regulation of the receivers would again be

tight.

However, regulation of the receivers is apparent in the photographs taken during the transient-response measurements. For example, the transient response of the dc receiver as the input voltage is decreased lasts about 170 milliseconds as measured from the photograph of Figure 4.5-9. The time is established by the time constant of the load and the 19,000 microfarad capacitor. In the reverse case when the input voltage is switched from 100 to 120 Vdc, the transient period is only about 90 milliseconds (see Figure 4.5-10). With this increase in voltage, the output voltage of the receiver begins to rise following its normal exponential curve until the voltage reaches that voltage set by the reference signal and the control circuitry begins regulating to level off the output voltage, cutting short its normal rise time.

4.5.5 Power Supply Sensitivity of the Three-Phase, 25.0-kW Power System

This was a test of the ability of the phasor regulation to maintain the bus voltage as the input voltage is varied. The test was run on phase A of the system with capacitive compensation while it was unloaded. The data of Table 4-9.1 was taken as the input voltage was increased from 120 to 200 Volts dc, which is a 67% increase in voltage. There is some upward drift of the bus voltage as the input voltage is increased, but the bus voltage never deviated more than 0.50% from the nominal voltage of 440.4 Volts RMS (set for an input of 150 Volts dc). The input current rises with input voltage because the resonating current and power capability of the inverters naturally increase with input voltage even though the load does not change.

4.5.6 Conclusions and Recommendations on Power Supply Sensitivity

Although a phase-control receiver may not be the optimum design from an efficiency standpoint, as explained in Section 4.2, the regulation of these modules proved to be quite satisfactory. For example, the dc receiver output voltage was measured to increase only 0.3% with a 20% increase in dc input voltage. For the step changes in the system input voltage, the modules responded smoothly and with no switching transients on their

outputs. The control circuits responded faster than the input voltage was able to change. The phasor regulation was demonstrated to maintain the bus voltage accurately over an input range of 120 Volts dc to 200 Volts dc. Over this range, the bus voltage varied only 0.91% and deviated only 0.50% from the 440.4 Volts RMS level at which the regulator was set (at 150 Volts dc).

4.6 POWER TURN OFF

The purpose of this test was to observe the power system during power shut down. Once again, this test was performed on the four major power system breadboard configurations as described in the sections that follow.

4.6.1 Power Turn Off of a Single 1 kW Inverter

A relay was used to remove the power from the inverter for this test. The test circuit, shown in figure 4.6-1, located the relay between the power supply filter capacitor and the inverter. When the relay was opened, the input voltage became a square wave because the input capacitor is no longer connected to the inverter and therefore it can no longer hold the input voltage constant. This voltage alternates between the resonant capacitor peak voltage (initially twice the input voltage) and zero at 40 kHz as shown in the no-load case of Figure 4.6-2. The voltage decreases exponentially until the energy of the tank circuit is dissipated. The time constant of this decay becomes shorter as the inverter is loaded as shown in Figure 4.6-3, which shows the inverter output voltage for the no-load and the 580-w case. The remainder of the inverter parameters show this same exponential decay.

4.6.2 Power Turn Off of a Single 1 kW Driver and Receiver

In this case, the relay was located before the dc-input capacitor (Figure 4.6-4). Ignoring the relay bounce, the input voltage is now a smooth exponential decay for all load cases as shown Figure 4.6-5. As expected, the decay of the system voltages and currents depends on the load. As shown in Figure 4.6-6, the decay time of the output voltage and current of the dc receiver decreases from over 70 milliseconds at 34 w load to about 25 milliseconds at 410 w (the relay bounce is again present in these photographs).

4.6.3 Power Turn Off of the Single-Phase 2 KW Breadboard

Figure 4.6-7 shows the test circuit used to photograph the transient response of the power system breadboard as the input power is removed. Other than relay bounce, the parameters of the system breadboard again display the expected decay (Figure 4.6-8).

4.6.4 Power Turn Off of the Three-Phase 5 kW breadboard

Since the waveforms produced by removing the input power to the power systems results in a very predictable exponential decay, this final power turn off test was run a little differently. As shown in the test circuit of Figure 4.6-9, the logic circuitry of the three inverters is turned off before the power relay is opened. By doing this, the resonant inductors of the inverters (Figure 3-14) are essentially removed from the circuit while there is still energy in the resonant tank. This causes the transmission line to resonate at a frequency determined by the resonant capacitors of the inverters, the inductance of the transformers, and the parasitic capacitance and inductance of the bus. Figure 4.6-10 shows the resonating voltages on phase c of the bus with and without 20-kHz resistive loads on the system. The resistive loads damp the oscillations. Meanwhile, the output voltage of the receivers decays to zero as expected (Figure 4.6-11).

4.6.5 Power Turn Off for a Three-Phase, 25.0-kW Power System

The system data for the 25 kW case shows that the system behaved in essentially the same fashion as the 5 kW system behaved.

4.6.6 Power Turn Off Conclusions.

Three different methods of system shutdown were simulated: removing input power, removing power and input capacitor, and turning off controller then removing input power. Although the latter method is the way power shut down would occur in a utility-type power system such as Space Station, the system response was about the same either way. The user voltages merely decay to zero with a time constant based on the filter components and the load. It is a smooth process in any case.

4.7 POWER FACTOR TESTING

4.7.1 Power Factor Testing of the Three-Phase, 5.0-kW Power System

By adding series inductors and parallel capacitors to all of the three-phase system loads, the operation of the system was evaluated for lagging, leading, nominal, and unity power factors. The efficiencies recorded during this test are somewhat low because an input voltage of 50 Vdc was used instead of the usual 120 Vdc. The voltage was lowered because if it had remained set at 120 vdc, the capacitive load would have drawn more current from the inverter than it was designed to supply.

4.7.1.1 Lagging Power Factor

An inductor whose value was approximately 24 micro-henerys was added to each load of the three-phase system as illustrated in Figure 4.7-1. This amounts to placing 0.64, 0.57, and 0.61 power-factor loads on phases 1, 2, and 3 respectively. The variation in the three values was caused by inductor tolerance, and by the fact that the transmission line and transformer leakage inductance also affected the power factor slightly. The phase shift present on the transmission line is shown in Figure 4.7-2 which shows the bus voltages and currents of each phase. These inductive loads yield a power factor on the line of between .61 and 0.70 lagging as calculated from these photographs.

The inductors have the effect of reducing the resonant capacitance seen by the inverters (see Figure 3-14). This reduces the current in the inverter tank circuit, which reduces the voltage and power available from the inverter (see Table 4-10). The output power of 583w is the lowest of the power levels from any of the power factor cases. However, due to the reduced inverter currents, the system had the highest efficiency of any of the power factor cases. The total system efficiency is 76.5% which is fair considering the input voltage is only 50 Vdc. The lower circulating inverter currents leads to decreased resistive power loss in the inverters.

Because of their impact on the resonant circuit of the inverter, the load inductors noticeably affected the resonant frequency of the inverters. The photograph of the inductor current of one of the inverter modules is shown in Figure 4.7-3. The measured frequency from this photograph is 29.4 kHz

as opposed to the 24 kHz observed with no added reactive load components. No harm is caused by increasing the resonant frequency of the inverters and it gives the SCRs even more time to turn off.

In summary, the resonant system has no problem with inductive loads and, in fact, runs most efficiently with a lagging power factor. In an actual system implementation, the power factor on the line would probably be limited to a value such as 0.70 lagging. This would serve to limit the range over which the inverters would have to regulate in compensating for the reduction in the bus voltage caused by the inductors. However, the power factor in a 20-kHz system would probably never approach 0.70 lagging because the normally inductive loads such as motors are operated through receiver modules. The inductance of the motors is not apparent to the bus in the same way a charge of capacitive filter does not look capacitive to the bus.

4.7.1.2 Nominal Power Factor

The three-phase power system breadboard was next fully loaded with strictly resistive loads so that comparison data could be gathered (see Figure 4.7-4). The bus voltage and current for each phase is shown in Figure 4.7-5. The inductance of the transmission line caused the power factor on the bus to be about 0.97 lagging.

As listed in Table 4-11, the output power is now 1.06 kW. The efficiency is 74.7%, which is only slightly lower than the inductive case. The inverter current of Figure 4.7-6 shows that the amplitude of the SCR current is 20A compared to 16A in the lagging power factor case. These higher circulating currents in the inverter account for the higher inverter losses. This photograph also shows the resonant frequency of the tank to be about 24 kHz.

4.7.1.3 Unity Power Factor

Small capacitors were added in parallel to the loads to bring the power factor on the bus to 1.0. The schematic of Figure 4.7-7 shows the system configuration used to gather data in the unity power factor case. The bus voltage and current waveforms are shown in Figure 4.7-8. Some distortion in the bus voltage is evident and is due to the resonant frequency beginning

to approach the line frequency. From the inductor current of the inverter in Figure 4.7-9, the resonant frequency is measured to be about 21.5 kHz. The capacitor that has been placed across the system loads adds to the capacitor in the inverter tank circuit decreasing the resonant frequency.

As the two frequencies come together, the circulating currents in the inverters increase. This results in the system power capability rising to 1.34 kW as seen in Table 4-12. The higher circulating currents are also responsible for increased resistive losses in the inverters. The end-to-end system efficiency is now 74.2%, however, which is only slightly less than the nominal case. All of these concerns can be eliminated by sizing the inductor and capacitor of the resonant circuit to produce the desired power or efficiency.

4.7.1.4 Leading Power Factor

In the final portion of the power factor test, capacitors were placed in parallel with the loads as shown in Figure 4.7-10 to produce a leading power factor. The calculated leading power factors of the loads were 0.76, 0.78, and 0.57 For phase 1,2, and 3 respectively. The voltages and currents on each phase of the bus are shown in Figure 4.7-11.

The phase shift on the bus appears as only 2.5 to 4.0 microseconds for the three phases, which corresponds to a power factor of 0.95 to 0.88 leading, while the calculated power factor of the load is much lower. Again, as was the case with the lagging power factor test, leakage and transmission line inductance affected the measured data. Also, the waveforms on the bus are quite distorted. Both of these phenomena are caused by the drastic increase in capacitance presented to the inverter resonant circuit by the load capacitors, which are basically in parallel with the resonant capacitor.

The change in capacitance is so large that the resonant frequency of the inverter is almost identical to the switching or line frequency as shown by the inductor current of inverter number 3 in Figure 4.7-12. This has brought the amplitude of the SCR current up to 40A and the system output power to just over 2.0 kW. As shown in Table 4-13, these circulating currents have, in turn, brought the efficiency down to 66.9%. Indeed, the larger the capacitor the lower the efficiency of that line of the bus

becomes. For example, the efficiency of phase 2 is 72.1 %. It has a 2.0μF capacitor on its load. The efficiency of phase 3 with its 3.0μF capacitor is a mere 63.5%. However, the system efficiency can be increased and the waveform distortion reduced for loads of the same power factor by simply raising the frequency of the inverter tank circuit so that the added capacitance at the load will only reduce the tank frequency to a manageable level.

4.7.2 Power Factor Testing of the 25.0-kW, Three-Phase System. This test monitors the reaction of the 25.0-kW system breadboard to non-unity power factor loads. Inductors and capacitors are used to create power factors of 0.7 lagging and 0.7 leading on the bus. The final test in this section involved running unbalanced power factor loads. A resistive load was placed on one phase of the bus, a 0.7 leading power factor load on another, and a 0.7 lagging power factor load on the third. Since the reactive components are placed in series with the load in these tests, the load banks are not able to achieve low enough resistance to fully load the system. Therefore, the efficiencies recorded in these tests are somewhat low. The test data tables for this test indicate that the is a drop in the voltage supplied to the load. This can be compensated for to some extent by sensing the load voltage at the point where the maximum currents are expected to be drawn, and controlling the inverters based on this value. Another possible solution is to employ a transformer to make voltage adjustments, at the 440 Vac distribution voltage very little loss would result if the feature were employed.

4.7.2.1 Lagging Power Factor. The reactances used to create the 0.7 lagging power factor on all three phases of the bus is shown in Figure 4.7-13. The photographs of Figure 4.7-14 show the bus voltage and current waveforms. As in the 5.0-kW system, the inductive load had little effect on the inverters driving the system. Table 4-14 shows that the capacitive compensation phasor regulation is able to maintain the bus voltage on all phases to within 1.0% of the nominal 440 Volts RMS with this large inductive load. One interesting point is the increased voltage drop on the line due to the inductive loading. This is because of the interaction of the inductive load with the excessive bus resistance and inductance of the 5.0-kW bus. It is interesting to note that in the next section (Section 4.7.2.2) the load-end voltage on the bus is higher than the source-end voltage because of this interaction. A bus designed for the 25.0-kW

system and with low inductance, such as the one developed by NASA/Lewis Research Center, would remedy this.

4.7.2.2 Leading Power Factor. The capacitors added to the load to produce a 45° phase shift on the bus are shown in Figure 4.7-15. Because of the inductance of the bus, obtaining a bus phase shift of 45° involved adding a load with a leading power factor of 0.64. The bus waveforms are shown in the photographs of Figure 4.7-16. The bus voltage waveform appears to be fairly distortion free. However, the current is somewhat distorted because the capacitor near the load adds directly to the value of the resonant capacitor of the inverter. As a result, a portion of the resonant current flows down the bus to resonate with the load capacitor. The bus current begins to take on some characteristics of the resonant tank current of the inverter.

Table 4-15 shows that two of the regulator circuits had trouble maintaining the bus voltage to within 1.0%. The Phase A voltage fell 1.89% while Phase C rose 1.5%. However, Phase B demonstrated that the phasor regulation can work perfectly with capacitive loads as well as resistive loads. Its voltage only strayed 0.14% from the nominal 440 Volts RMS. The interaction of the large bus inductance and resistance with the series reactance at the load produced an interesting effect. The voltage at the load end of the 50-meter bus was higher than the voltage at the inverter end. As explained above, with a more appropriate transmission line, this effect can be remedied.

4.7.2.3 Unbalanced Power Factor. In this test, a different power factor was placed on each phase of the bus as in Figure 4.7-17. Phase A was loaded with a 7.14-kW resistive load (0.9997 power factor), Phase B had a 0.71 lagging power factor, and Phase C had a 0.78 leading power factor load. The bus voltage and current waveforms are shown in Figure 4.7-18. The system had no problems operating with the unbalanced power factors. The phasor regulation was able to cope well with the various loads as shown in Table 4-16, since each phase was independently regulated. The zero to full load regulation on Phase A with its resistive load was 0.08%, on Phase B with its inductive load was 0.05%, and on Phase C with the capacitive load was 1.5%. As expected from the lagging and leading testing on this system, there was interaction between the line with its losses and the reactive loads. This interaction produced varying bus

voltage drops and gains among the phases.

4.7.3 Conclusions and Recommendations on the Bus Power Factor

The resonant power system is tremendously tolerant of non-unity power-factor loads and was successfully operated under full-load conditions with load power factors ranging from 0.57 lagging to 0.57 leading. The system is most efficient driving inductive or resistive loads and is ideal for a utility-type power system since most loads will appear resistive because they will be connected to the line with a receiver module. For example, consider the case of a typical 60 Hz induction motor. With a 60 Hz supply, its current lags the voltage and requires a generator with an increased volt-ampere capability. When 20 kHz is used for the supply, an AC to AC converter is placed between the bus and the motor. The converter synthesizes the 60 Hz waveform the motor requires by switching the 20 kHz pulses in one direction for 1/120th of a second, and then switching them the other direction for the next 1/120th of a second. The 20 kHz current is either in phase or out of phase with the applied voltage; it follows the envelop that the 60 Hz current would follow. Thus the 20 kHz breadboard showed a power factor close to unity (with a slight lag because of the bus inductance), operating at the point close to where the system is most efficient.

Although the various power factor loads caused the bus voltage to vary on this unregulated bus, a regulated bus would maintain constant line voltage and load power. In any event, the inverters can be designed to take any type of reactive load by appropriately setting the resonant frequency to compensate for the effect of the reactive load.

When the power factor testing was performed on the 25.0-kW system breadboard, which uses phasor regulation to control its bus voltages, the system performed just as well. With phase shifts on the bus varying from 45° lagging to 45° leading, the voltage on the bus was maintained to within 2.0% on all phases regardless of the power factor. Phase B demonstrated particularly well that the phasor regulation technique can handle reactive loads. As the load was changed from 0.7 power factor lagging to resistive to 0.7 power factor leading, its bus voltage never deviated more than 0.14% from the nominal 440 Volts RMS.

4.8 THREE-PHASE MOTOR TESTING

The purpose of this test was to evaluate the performance of a 20-kHz-to three-phase, 60-Hz motor-driver receiver. This module was transformer-coupled to inverter number 3 (see Figure 4.8-1). As shown in Figure 4.8-2, the motor-driver receiver module had a delta-type output. Because of the three-phase output of the receiver module, no 60-Hz modulation can be seen on the inverter output. In the case of the ac receivers with single-phase outputs, there was obvious low-frequency modulation of the inverter parameters. The three-phase module loads the inverter much more evenly. Figure 4.8-3 shows the inverter output voltage and one phase of the motor input voltage as the one horsepower motor was operated at 230 Vrms line-to-line. The motor was started with a switch on the 20-kHz input to the receiver.

This early testing of the AC to AC motor driver converter did not include a closed loop regulator circuit, but it nonetheless demonstrated that a typical 60 Hz induction motor could be started by applying the synthesized 60 Hz with a switch and run as expected. It further points the way toward the promise of speed control converters which will operate at close to maximum torque, and which could conceivably be regenerative as well.

4.9 Fault Isolation Testing. This is a new test that was only performed on the 25-kW system breadboard. The fault-isolation switch was designed and fabricated using General Dynamics Independent Research and Development funds. It is composed of two anti-parallel SCRs (see Figure 4.9-1) and control circuitry that monitors the bus voltage and current. The fault-isolation switch opens if the current exceeds a limit and the voltage falls below a preset limit. In this test, the switch was installed on one phase of the 50-meter bus at the load end as shown in Figure 4.9-2. Then, the two leads of the bus were shorted with an SCR and the reaction time of the fault-isolation switch and its effect on the system were monitored.

The phase of the system is operating at a power level of about 7.2 kW, which is close to the full-rated power level. The photographs of Figure 4.9-3 show the response of the bus voltage and current when the fault is applied to the bus. The SCRs in the switch are fairly slow SCRs, having a maximum turn off recovery time of 20μs. Because of this, they are not able to remain turned off until the high frequency transient has settled out

and the voltage is not reapplied with the same polarity for 20μs. The switch reacts quickly to the surging current as shown in the photographs; but under these circumstances, the switch is not able to successfully break the bus current until after the first period. It takes 60 and 90μs for the switch to completely sever the fault current in the two cases in Figure 4.9-3.

The bus voltage, on the other hand, has a 50% overshoot after the fault, and the phasor regulator begins to ring at about 3.0 kHz. This oscillation remains at a significant level for 5 milliseconds after the occurrence of the bus fault. However, the oscillations are easily corrected by compensating the regulator loop.

In summary, the fault-isolation switch is able to completely break the current to a fault in two cycles. This time could be greatly reduced by using SCRs with faster turn off recovery times. SCRs are currently available in this voltage and current range with maximum turn off times of 10μs. If the SCR turn off limitation can be removed, the fault-isolation switches will remove a fault from the bus in 30μs or less.

4.10 EMI Measurements

This is another new test that was run only on the 25.0-kW system breadboard. As in all the other tests on this system breadboard, the EMI testing was performed with the capacitive compensation phasor regulation (see Section 4.2.6.2). Conducted emissivity tests CE01 and CE03 and conducted susceptibility tests CS02 and CS06 were performed on this system in accordance with the methods of Mil-Std-462. The results were compared against the specifications of Mil-Std-461B.

All tests were performed on the 20-kHz power processing system while it was operating at 23.4 kW, which included all the receiver module loads and the resistive loads (see Table 4-17). Conducted susceptibility test CS01 was also scheduled to be performed on the dc input leads of the system. However, a current-injection probe that could handle the 180 amperes dc on these leads was not available, and conducted susceptibility tests CS02 and CS06 were substituted.

Although the system filters consist merely of aluminum electrolytic

capacitors on the dc input and output leads and an L-C filter on the 60-Hz ac receiver output , the system was well within the specifications for CE01 (30 Hz to 15 kHz) at all points of the system breadboard. This included the dc input leads, the output leads of every receiver module (dc, bidirectional, and ac), and each phase of the unfiltered 20 kHz bus phases. Figures 4.10-1, 4.10-2, and 4.10-3 show the conducted emissions for the 30 Hz to 15 kHz frequency for the dc input leads, Phase A, and the dc receiver output respectively.

The results of the CE03 tests (15 kHz to 50 MHz) indicate some filtering is necessary if the system is to meet the specification levels above 20 kHz. The system breadboard fails to meet the specifications in the 15-kHz to 10-MHz range. This is shown in Figure 4.10-4, which shows the narrow-band conducted emissions on Phase A of the bus for the 15-kHz to 50-MHz range. However, in the 10 to 50-MHz range, the unfiltered system again falls below the specification at all points. Filtering the system to meet these conducted emission specifications is straight forward. It already meets or exceeds the requirements in the frequency ranges most difficult to filter, namely the frequencies below 20 kHz because of the large reactances required and above 10 MHz because of the purity of the reactances needed.

Simply substituting capacitors with high-frequency dielectrics such as polypropylene and polycarbonate would do much to bring the system below the specification range. For example, the ac receiver is equipped with an L-C filter that uses a polypropylene capacitor, and it only exceeded the broadband specification significantly (greater than 10 db) between 600 kHz and 4.9 MHz (see Figure 4.10-5). It only significantly exceeded the narrowband spec at 20 kHz, 40 kHz, and sporadically between 890 kHz and 5.15 MHz as shown in Figure 4.10-6.

The power processing system breadboard passed the CS02 specification on all three phases of the power system. In this test ac signals were applied to each phase of the bus from 0.05 to 400-MHz and the response of the system measured. No response could be measured on any phase for any frequency.

In the CS06 test, large voltage pulses were applied to the dc input leads. The system passed the portion of the CS06 test in which a 100V, 10 μs

pulse was applied to the input power leads. It also passed the application of 100, 200, 300, and ±400-Volt, 5μs pulses to the dc input leads. When the pulse width was shortened to 0.15μs, the system could tolerate pulses up to 40 Volts, but no larger. This limitation is caused by the application of dv/dt across the SCRs in excess of the manufacturers specifications. Excessive dv/dt will falsely trigger the SCRs. This indicates that a high-frequency filter will have to be added to the system input if such sharp voltage transients of this magnitude are to be present on the system input.

So, the system breadboard without any shielding or additional filtering, passes the CE01 tests (30 Hz to 15 kHz), the CS02 test (50 kHz to 400 MHz), the CE03 tests (15 kHz to 50 MHz) for frequencies from 10 to 50 MHz, and all but one of the CS06 tests. The remainder of the requirements (excepting 20 kHz limitations on the bus) could be met as they now stand through additional filtering on the system input and on the input and output of each module. However, before this is done, the applicability of this specification to a large spacecraft power system must be determined. Specifications limiting the 20 kHz component on the bus and limitations of microamps or even milliamps of noise on input leads carrying hundreds of amperes are examples of portions of the specification that may have to be reevaluated for this application.

SECTION 5

CONCLUSIONS AND RECOMMENDATIONS

With data taken from actual operating hardware, this test program has answered the questions about the resonant power distribution system proposed in the Study of Power Management for Orbital Multi-100kWe Applications (contract NAS3-21757). The resonant ac power system has been demonstrated to be an available power system technology resulting from this thorough study of the three operating breadboards. In the course of this test program, the system breadboards were evaluated in configurations and conditions resembling a Space Station power environment. Power transmission was demonstrated over fifty meters on three-phase and single-phase distribution busses. These busses were operated at voltage levels between 200 and 1,200 Volts RMS at a constant frequency of 20 kHz independent of load. System input voltages between 40 and 200 Volts dc were used to run the systems breadboards. On the far end of the busses, power was delivered through several types of user-interface receiver modules to dc, low-frequency ac, and 20 kHz ac loads to reflect actual Space Station user requirements.

For example, a 60-Hz, three-phase, motor-driver module was tested driving a 1.0-horsepower motor typical of induction motors expected to be used on Space Station. A bidirectional module capable of delivering power in forward and reverse directions provides an interface between the energy storage medium or motor/generators and the distribution bus.

The final breadboard configuration operates at the same power level as one power channel (one solar dynamic generator or solar array wing set) is estimated to be likely to be for the Space Station. Upgrades from the original breadboards have pushed the end-to-end system efficiency to 87.3%. This, despite no improvements in the 50-meter bus in the 5.0 kW to 25.0 kW upgrade. This indicates that a flight system with optimized system components will reach 92% total system efficiency.

Phasor regulation was demonstrated to maintain the bus voltage to within 2.0% over the entire load range from zero to full-rated power, over a power

factor range of 0.7 lagging to 0.7 leading, and over a 120 to 200 Volt dc input voltage swing. Indications of the test results are that this can be improved to better than 0.50% over these same conditions. Phasor regulation has been implemented in such a way that there is no inverter power unbalance under full load conditions.

Many other system features and components have established the maturity of resonant power conversion and distribution. Bus faults are cleared in less than two periods (100μs) with the fault-isolation switch. Multiple resonant inverter modules can be frequency and phase-synchronized and placed either in series or parallel with no circuit modifications. The load is shared equally among the inverters to within 5.0%. The addition and removal of inverter and receiver modules can be done from the system without interrupting its operation and be totally undetected by the user. With no added shielding or filtering, the breadboard met the majority of the EMI specifications as listed in Mil-Std-461B. Finally, as a result of the testing performed on this contract, the system has been shown to have a satisfactory response to start up, shut down, and load switching over the entire range of system loads.

Based on the test results from these three system breadboards, a resonant ac power system would be ideal for the Space Station or any other multiple-user spacecraft. It is a utility-type power system that has a stiff, well-regulated bus. The bus is high voltage for greater efficiency and transmits power at 20 kHz to keep reactive components small and lightweight. Because it is an ac system, it is versatile and the voltage at any point on the spacecraft can be set with a transformer. This power system can deliver dc, low-frequency ac, or high-frequency ac power to users.

Portions of the technology still require development to reach their ultimate potential. These include:

1. Efficient low voltage user converters with regulation on the primary side of the transformer to maximize efficiency,
2. Software which monitors the system and incorporates the expert knowledge of how the system and its components operate, so that predictable faults and failures can be predicted and avoided, or if they can't, at least their effect on system performance can be minimized.

3. Interfaces to motors and generators; so that the performance of the combined electronics/electromechanical subsystem is optimized.

It is recommended that the development of all of the above technologies begin so that 20 kHz technology quickly expands to reach its ultimate potential with the components and knowledge available today.

TABLES AND FIGURES

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TABLE 3-1. TEST MATRIX

CONFIGURATIONS				TESTS																		
				POWER TURNON LOADS (4)	STEADY-STATE OPERATION	TRANSIENT LOAD RESPONSE				STEADY-STATE CONTROL GAIN			CONTROL SIGNAL STEP RESPONSE		CONTROL SIGNAL FREQ RESPONSE			STEADY STATE POWER SUPPLY SENSITIVITY (±20%)	POWER SUPPLY STEP RESPONSE (±20%)	POWER TURNOFF LOADS (4)	POWER FACTOR (−0.87 TO +0.87)	MOTOR OPERATION
						30 kHz	DC RECEIVER	AC RECEIVER	BIDIRECTIONAL RECEIVER	DC RECEIVER	AC RECEIVER	BIDIRECTIONAL RECEIVER (10%)	DC RECEIVER	BIDIRECTIONAL RECEIVER	DC RECEIVER	AC RECEIVER	BIDIRECTIONAL RECEIVER					
SYSTEM I	DRIVER-AC LOAD	(1)	INPUT OUTPUT OTHER	VT, IT VT, IT IA, IO IC, IO	VS, IS VS, IS, f IA, IO n	VT, IT VT, IT IA, IO	—	—	—	—	—	—	—	—	—	—	—	VS, IS VS, IS f	VT, IT VT, IT -	VT, IT VT, IT IA, IO	—	—
	DRIVER-TRANS LINE- DC RECEIVER	(1) (1)	INPUT OUTPUT OTHER	VT, IT VT, IT IA, IO	VS, IS VS, IS IA, IO VK1, IK1 f, n	—	VT, IT VT, IT IA, IO VK1, IK1	—	—	VS, IS VS, IS VK1, IK1 f, n	—	—	VT, IT VT, IT VK1, IK1	—	VT, IT VT, IT VK1, IK1	—	—	VS, IS VS, IS f, n	VT, IT VT, IT VK1, IK1	VT, IT VT, IT IA, IO	—	—
	BIDIRECTIONAL MODULE- AC LOAD (INVERTOR LOAD)	(1)	INPUT OUTPUT OTHER	—	VS, IS VT, IT IE, IF n	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	DRIVERS TRANS LINE- DC RECEIVER AC RECEIVER BIDIRECTIONAL MODULE (RECEIVER MODE)	(2) (1) (1) (1)	INPUT DC OUT AC OUT BD OUT OTHER	VT, IT VT, IT VT, IT VT, IT IA, IO IC, ID VK1, IK1 VK2, IK2	VS, IS VS, IS VS, IS VS, IS IA, IO IC, IO VK1, IK1 VK2, IK2 f	—	VT, IT VT, IT - - IA, IO IC, IO VK1, IK1 VK2, IK2	VT, IT - VT, IT - IA, IO IC, IO VK1, IK1 VK2, IK2	VT, IT - - VT, IT IA, IO IC, IO VK1, IK1 VK2, VK2	VS, IS VS, IS - - -	—	VS, IS - - VS, IS -	—	—	—	VT, IT - VT, IT - IA, IO IC, IO VK1, IK1 VK2, IK2	—	VS, IS VS, IS VS, IS VS, IS -	VT, IT VT, IT VT, IT VT, IT IA, IO IC, IO VK1, IK1 VK2, IK2	VT, IT VT, IT VT, IT VT, IT IA, IO IC, IO VK1, IK1 VK2, IK2	—	—
SYSTEM II	DRIVERS 3-φ LINE DC RECEIVER AC RECEIVER BIDIRECTIONAL MODULE (RECEIVER MODE)	(3) (1) (1) (1)	INPUT DC OUT AC OUT BD OUT OTHER	—	VS, IS VS, IS VS, IS VS, IS IA, IB, IC ID, IG, IH VK1, IK1 VK2, IK2 VK3, IK3 VX1, VX2 VX3, n f, H	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	DRIVERS 3-φ LINE- DC RECEIVER AC RECEIVER BIDIRECTIONAL MODULE (RECEIVER MODE)	(3) (1) (1) (1)	INPUT DC OUT AC OUT BD OUT OTHER	VT, IT VT, IT VT, IT VT, IT IA, IB, IC ID, IG, IH VK1, IK1 VK2, IK2 VX3, IK3	VS, IS VS, IS VS, IS VS, IS IA, IB, IC ID, IG, IH VK1, IK1 VK2, IK2 VK3, IK3 VX1, VX2 VX3, n, H, f T	—	VT, IT VT, IT - - IA, IB, IC ID, IG, IH VK1, IK1 VK2, IK2 VK3, IK3	VT, IT - VT, IT - IA, IB IC, ID IG, IH VK1, IK1 VK2, IK2 VK3, IK3	VT, IT - - VT, IT IA, IB IC, ID IG, IH VK1, IK1 VK2, IK2 VK3, IK3	VS, IS VS, IS - - -	VS, IS - VS, IS - -	VS, IS - - VS, IS -	VT, IT VT, IT - - -	VT, IT - - VT, IT -	VT, IT VT, IT - - -	VT, IT - VT, IT - -	VT, IT - - VT, IT -	VS, IS VS, IS VS, IS VS, IS VK1, IK1 VK2, IK2 VK3, IK3 VX1, VX3 VX2, n	VT, IT VT, IT VT, IT VT, IT -	VT, IT VT, IT VT, IT VT, IT	VS, IS - - - IA, IB, IC ID, IG, IH VK1, IK1 VK2, IK2 VK3, IK3 n	VS, IS - VT, IT - IA, IB, IC ID, IG, IH VK1, IK1 VK2, IK2 VK3, IK3 VX1, VX2 VX3, n
SYSTEM III 25.0 kW	DRIVERS 3-φ LINE- DC RECEIVER AC RECEIVER BIDIRECTIONAL MODULE (RECEIVER MODE)	(3) (1) (1) (1)	←	SAME AS SYSTEM II					→	—	—	—	—	—	—	—	—	← SAME AS SYSTEM II			→	VT, IT - VT, IT - IG, IH VK3 IK3

770 126 0 1

Load Configuration	Load* (W)					Efficiency (%)
	P_{IN}	P_{DC}	P_{BD}	P_{AC}	P_{OUT}	
a	796	200	210	0	410	51.7
b	1020	423	205	0	628	61.6
c	1024	202	210	190	613	60.0
d	1210	418	205	171	794	65.7
e	1000	200	413	0	613	61.3
f	1210	418	413	0	831	68.6
g	1200	200	405	170	780	64.8
h	1370	403	405	140	950	69.5

*P_{IN} = Total System Input Power
P_{DC} = dc Receiver Output Power
P_{BD} = Bidirectional Module Output Power
P_{AC} = ac Receiver Output Power
P_{OUT} = Total System Output Power

TABLE 4-1. LOAD COMBINATIONS OF THE DUAL DRIVER SYSTEM

60% Load Test
System Frequency, 20.15 kHz
Resonant Capacitance, 1.5 μF

Input Power

Input Voltage, V_{IN}, Vdc	120
Input Current, I_{IN}, Adc	27.23
Total Input Power, P_{IN}, W	3268

Total Harmonic Distortion (THD) Transmission Line, dB

Into the Line

Phase a - 28.3
Phase b - 21.8
Phase c - 23.0

Output Power	Output Voltage, V_{OUT} (Vdc)	Output Current, I_{OUT} (Adc)	Power, P (W)
ac Receiver	120.6	3.38	408
dc Receiver	28.06	30.0	842
Bidirectional Receiver	100.2	7.77	779
Total Output Power			2029

Total System Efficiency = $\frac{\text{Power Output}}{\text{Power Input}} = \frac{2029}{3268} = 62\%$

TABLE 4-2. POWER AND THD MEASUREMENTS ON THE THREE-PHASE SYSTEM WITH NO RESISTIVE LOADS

Full Load Test at Steady-State Operation
System Frequency, 20.06 kHz
Resonant Capacitance, 1.0 μF

Input Power

Input Voltage, V_{IN}, Vdc	120
Input Current, I_{IN}, Adc	30.70
Total Input Power, P_{IN}, W	36.84

THD, dB

Inverter 1 - 20.4
Inverter 2 - 17.4
Inverter 3 - 19.4

THD Transmission Line, dB

	Into the Line	Out of the Line (Load End)
Phase a	17.4	-
Phase b	16.4	17.8
Phase c	18.2	-

Output Power	Output Voltage, V_{OUT} (Vdc)	Output Current, I_{OUT} (Adc)	Power, P (W)
ac Receiver	110	3.0	330
dc Receiver	253	23.0	582
Bidirectional Receiver	99.3	6.35	631
Resistive Loads			
Phase a	74.96	7.96	597
Phase b	68.3	4.38	299
Phase c	67.9	4.40	299
Total Output Power			2738

Total System Efficiency = $\frac{\text{Power Output}}{\text{Power Input}} = \frac{2738}{3684} = 74.3\%$

TABLE 4-3. POWER AND THD MEASUREMENTS FOR THE FULLY LOADED THREE-PHASE SYSTEM WITH A RESONANT FREQUENCY OF 32.5KHZ

Full Load Test at Steady-State Operation
System Frequency, 20.16 kHz
Resonant Capacitance, 1.5 μF

Input Power

Input Voltage, V_{IN}, Vdc	120
Input Current, I_{IN}, Adc	54.1
Total Input Power, P_{IN}, W	6492

THD (at the inverter), dB

	Run Together	Each Phase Run Independent of Others (Others Turned Off)
Inverter 1	-28.8	-33.0
Inverter 2	-28.6	-29.2
Inverter 3	-30.2	-30.8

THD Transmission Line, dB

	Into the Line	Out of the Line (Load End)
Phase a	-28.2	26.8
Phase b	-23.4	24.8
Phase c	-24.2	20.0

Output Power	Output Voltage, V_{OUT} (Vdc)	Output Current, I_{OUT} (Adc)	Power, P (W)
ac Receiver	120	3.4	408
dc Receiver	27.6	30.0	828
Bidirectional Receiver	99.8	7.8	778
Resistive Loads			
Phase a	83.6	14.67	1226
Phase b	77.2	9.77	754
Phase c	76.5	13.2	1010
Total Output Power			5004

Total System Efficiency = $\frac{\text{Power Output}}{\text{Power Input}} = \frac{5004}{6492} = 77\%$

TABLE 4-4. POWER AND THD MEASUREMENTS FOR THE FULLY LOADED THREE-PHASE SYSTEM WITH A RESONANT FREQUENCY OF 26.5KHZ

THD, dB

	Into the Receiver	Out of the Receiver
ac Receiver	-24.3 (4.7%)	-13.6 (at 60 Hz)
dc Receiver	-16.8	
Bidirectional Receiver	-19.4	
Toaster Loads		
Phase a	-28.4	
Phase b	-24.4	
Phase c	-23.7	

TABLE 4-4. POWER AND THD MEASUREMENTS FOR THE FULLY LOADED THREE-PHASE SYSTEM WITH A RESONANT FREQUENCY OF 26.5KHZ

	230W Load		450W Load	
Input				
Voltage, V_{IN}, Vdc	60.05	120.0	60.50	120.03
Current, I_{IN}, Adc	7.41	6.89	11.42	9.28
Output Voltage, Vrms				
Inverter 1	93.9	186.0	94.4	168.6
Inverter 2	80.1	186.0	69.6	160.9
Transmission Line Voltage, V_L, Vrms	250	249	248	249
Load Voltage, V_{LOAD}, Vrms	36.8	35.9	34.2	34.7

TABLE 4-5. REGULATION MEASUREMENTS

MEASUREMENTS	LOAD LEVEL								
	NO LOAD			50% LOAD			FULL LOAD		
I. INPUT									
Input Voltage (Vdc)	150.9			151.1			150.2		
Input Current (Idc)	13.98			69.42			128.9		
Input Power (kW)	2.11			10.49			19.36		
II. BUS (INV. END)	ØA	ØB	ØC	ØA	ØB	ØC	ØA	ØB	ØC
Voltage (Vrms) (Line-neutral)	437.8	441.5	442.3				445	445	445.0
Current (Irms)									
Total Harmonic Distort (%)	2.09	1.82	2.15	3.80	2.26	2.82	4.36	3.65	3.98
Frequency (kHz)	19.912			--			--		
III. OUTPUT									
AC RCVR OUTPUT	OFF								
Voltage (Vrms)	0			106			106		
Current (Irms)	0			4.46			4.52		
Power (kW)	0			0.455			480		
Total Harm. Dis. (%)	--			--			3.02		
DC RCVR OUTPUT									
Voltage (Vdc)	28.73			28.15			28.16		
Current (Idc)	0			36.76			36.44		
Power (kW)	0			1.035			1.026		
BD RCVR OUTPUT									
Voltage (Vdc)	206			94.6			97.7		
Current (Idc)	0			9.37			8.28		
Power (kW)	0			0.886			0.809		
RESISTIVE LOADS	ØA	ØB	ØC	ØA	ØB	ØC	ØA	ØB	ØC
Voltage (Vrms)	437.5	442.2	442.8	433.7	434.9	431.3	431.1	432.1	429.7
Current (Irms)	0	0	0	4.90	3.86	3.15	10.58	11.77	9.94
Power (kW)	0	0	0	2.126	1.676	1.358	4.56	5.09	4.27
POWER IN (kW)	2.11			10.49			19.36		
POWER OUT (kW)	0			7.536			16.235		
EFFICIENCY (%)	0			71.8			83.86		

TABLE 4.5.1 SYSTEM MEASUREMENTS FOR UNCOMPENSATED PHASOR REGULATION

MEASUREMENTS	LOAD LEVEL								
	NO LOAD			50% LOAD			FULL LOAD		
I. INPUT									
Input Voltage (Vdc)	152.6			149.64			149.15		
Input Current (Idc)	21.0			124.14			200.9		
Input Power (kW)	3.20			18.58			29.97		
II. BUS (INV. END)	ØA	ØB	ØC	ØA	ØB	ØC	ØA	ØB	ØC
Voltage (Vrms) (Line-neutral)	441.0	442.0	442.0	--	442	444	--	443	443
Current (Irms)	0	0	0	--	--	--	--	--	--
Total Harmonic Distort (%)	6.10	5.96	4.73	5.6	6.4	5.9	5.8	6.6	6.0
Frequency (kHz)	19.96			19.97			19.96		
III. OUTPUT									
AC RCVR OUTPUT	OFF								
Voltage (Vrms)	0			109			105		
Current (Irms)	0			4.56			4.50		
Power (kW)	0			0.494			0.472		
Total Harm. Dis. (%)	--			--			4.2		
DC RCVR OUTPUT									
Voltage (Vdc)	28.75			28.15			28.18		
Current (Idc)	0			36.44			36.51		
Power (kW)	0			1.030			1.029		
BD RCVR OUTPUT									
Voltage (Vdc)	203			96.6			95.6		
Current (Idc)	0			8.53			8.49		
Power (kW)	0			0.824			0.812		
RESISTIVE LOADS	ØA	ØB	ØC	ØA	ØB	ØC	ØA	ØB	ØC
Voltage (Vrms)	445.3	444.6	445.0	437.6	434.4	434.0	433.3	430.3	430.0
Current (Irms)	0	0	0	9.87	9.41	9.58	18.16	17.77	18.16
Power (kW)	0	0	0	4.320	4.090	4.160	7.870	7.650	7.810
POWER IN (kW)	3.20			18.58			29.97		
POWER OUT (kW)	0			14.92			25.60		
EFFICIENCY (%)	0			80.3			85.3		

TABLE 4.5.2 SYSTEM MEASUREMENTS FOR CAPACTIVELY COMPENSATED PHASOR REGULATION

MEASUREMENTS	LOAD LEVEL								
	NO LOAD			50% LOAD			FULL LOAD		
I. INPUT									
Input Voltage (Vdc)	150.9			150.6			151		
Input Current (Idc)	15.18			115.4			208.3		
Input Power (kW)	2.29			17.39			31.5		
II. BUS (INV. END)	ØA	ØB	ØC	ØA	ØB	ØC	ØA	ØB	ØC
Voltage (Vrms) (Line-neutral)	442.8	437.5	441.8	442.9	438.0	442.9	445.1	427.1	444.1
Current (Irms)	--	--	--	11.35	11.6	10.18	--	--	--
Total Harmonic Distort. (%)	6.9	7.1	7.3	6.8	6.5	5.9	4.7	4.1	4.3
Frequency (kHz)	19.96			19.92			19.92		
III. OUTPUT									
AC RCVR OUTPUT	OFF								
Voltage (Vrms)	0			107			106		
Current (Irms)	0			4.52			4.51		
Power (kW)	0			0.475			0.471		
Total Harm. Dis. (%)	--			--			--		
DC RCVR OUTPUT									
Voltage (Vdc)	28.76			28.29			28.28		
Current (Idc)	0			22.23			22.13		
Power (kW)	0			0.629			0.626		
BD RCVR OUTPUT									
Voltage (Vdc)	112			95.5			90.2		
Current (Idc)	0.19			8.16			8.08		
Power (kW)	0.021			0.779			0.729		
RESISTIVE LOADS	ØA	ØB	ØC	ØA	ØB	ØC	ØA	ØB	ØC
Voltage (Vrms)	442.8	437.5	441.8	431.8	429.0	432.7	427.1	407.4	423.7
Current (Irms)	0	0	0	10.15	10.34	9.011	18.1	22.4	20.7
Power (kW)	0	0	0	4.380	4.440	3.90	7.73	9.13	8.77
POWER IN (kW)	2.29			17.39			31.5		
POWER OUT (kW)	0			14.60			27.5		
EFFICIENCY (%)	0			84.0			87.3		

TABLE 4-5.3. SYSTEM MEASUREMENTS FOR INDUCTIVE AND CAPACITIVE PHASOR REGULATION.

Change in Input Voltage	Input Power		Output Power		
	Input Voltage, V_{IN} (Vdc)	Input Current, I_{In} (Adc)	Output Voltage, V_{OUT} (Vrms)	Output Current, I_{OUT} (Arms)	Frequency, f (kHz)
-20%	69.6	10.20	93.0	6.9	20.0
--	87.0	12.76	117.0	8.6	20.0
+20%	104.4	15.24	140.6	10.2	20.0

TABLE 4-6. POWER SUPPLY SENSITIVITY OF THE INVERTER

Component	Unit*	Change in Input Voltage		
		-20%	--	+20%
Fluke 8000A	V_{IN}, Vdc	72.0	87.0	104.4
Fluke 8000A	I_{IN}, Adc	6.33	7.60	7.84
Fluke 893A	V_{OUT}, Vdc	21.5	26.3	28.9
SRI No. 900083	I_{OUT}, Adc	13.4	16.4	17.8
HP 5315B	f, kHz	20.725	20.726	20.726
Efficiency	η, %	63.2	65.2	62.8

*V_{IN} = Input Voltage
I_{IN} = Input Current
V_{OUT} = Output Voltage
I_{OUT} = Output Current
f = Frequency
η = System Efficiency

TABLE 4-7. POWER SUPPLY SENSITIVITY OF CONFIGURATION 2

Change in Input Voltage	Input Power*			Output Power**								
				dc Receiver			Bidirectional Receiver			ac Receiver		
	V_{IN} (Vdc)	I_{IN} (Adc)	P_{IN} (W)	V_{OUT} (Vdc)	I_{OUT} (Adc)	P_{OUT} (W)	V_{OUT} (Vdc)	I_{OUT} (Adc)	P_{OUT} (W)	V_{OUT} (Vrms)	I_{OUT} (Arms)	P_{OUT} (W)
-20%	68.2	10.28	701	26.39	6.5	172	96	1.93	185	54.4	1.54	83.8
—	85.4	11.02	941	28.86	7.1	205	99	1.99	197	76	2.14	163
+20%	102.3	11.67	1190	28.95	7.1	206	100	2.01	201	96	2.72	261
				R_{LOAD}*** = 4.06 ohms			R_{LOAD}*** = 49.7 ohms			R_{LOAD}*** = 35.3 ohms		

*V_{IN} = Input Voltage
I_{IN} = Input Current
P_{IN} = Total Input Power

**V_{OUT} = Output Voltage
I_{OUT} = Output Current
P_{OUT} = Total Output Power

***R_{LOAD} = Resistivity Load

TABLE 4-8. POWER SUPPLY SENSITIVITY IN THE SINGLE-PHASE SYSTEM

Input Power		Output Power							
					Resistive Loads (Vrms)				
Input Voltage, V_{IN} (Vdc)	Input Current, P_{IN} (kW)	ac Receiver (Vrms)	Bidirectional Receiver (Vdc)	dc Receiver (Vdc)	Phase a	Phase b	Phase c	Total Output Power, P_{OUT} (kW)	Efficiency (%)
80.0	3.26	79.14	71.0	17.3	52.5	50.3	51.3	2.45	75.2
100.0	5.08	105.0	94.0	22.2	66.6	64.7	64.3	3.93	77.4
120.0	6.88	120.5	99.7	26.0	80.2	77.4	77.8	5.37	78.1

TABLE 4-9. POWER SUPPLY SENSITIVITY OF THE THREE-PHASE SYSTEM

INPUT VOLTAGE (Vdc)	INPUT CURRENT (Adc)	BUS VOLTAGE (Vrms)
120.0	5.70	438.6
130.0	5.97	439.0
140.0	6.27	439.5
150.0	6.60	440.4
160.0	6.89	440.7
180.0	7.64	441.7
200.0	8.40	442.6

TABLE 4-9.1. BUS VOLTAGE REGULATION MEASUREMENT FOR LARGE INPUT VOLTAGE SWINGS.

	Phase		
	1	2	3
Input Power			
Input Voltage, V_{IN}, Vdc	50.0	50.0	50.0
Input Current, I_{IN}, Adc	5.09	4.83	5.29
Total Input Power, P_{IN}, W	255	242	265
Output Power (Resistive Loads)			
Output Voltage, V_{OUT}, Vrms	22.14	19.8	21.4
Output Current, I_{OUT}, Arms	8.87	9.42	9.33
Total Output Power, P_{OUT}, W	196	187	200
Efficiency,* η, %	76.9	77.3	75.5

*Total Efficiency, η_{TOTAL} = 76.5%

TABLE 4-10. LEADING POWER FACTOR MEASUREMENTS

	Phase		
	1	2	3
Input Power			
Input Voltage, V_{IN}, Vdc	50.0	50.2	50.4
Input Current, I_{IN}, Adc	9.86	10.11	10.27
Total Input Power, P_{IN}, W	493	508	518
Output Power (Resistive Loads)			
Output Voltage, V_{OUT}, Vrms	31.18	31.43	32.02
Output Current, I_{OUT}, Arms	11.85	12.23	11.88
Total Output Power, P_{OUT}, W	369.5	384.4	380.4
Efficiency,* η, %	74.9	75.7	73.4

*Total Efficiency, η_{TOTAL} = 74.7%

TABLE 4-11. NOMINAL POWER FACTOR POWER MEASUREMENTS

	Phase		
	1	2	3
Input Power *			
Input Voltage, V_{IN}, Vdc	50.0	50.0	50.0
Input Current, I_{IN}, Adc	11.11	11.39	13.60
Total Input Power, P_{IN}, W	556	570	680
Output Power (Resistive Loads)			
Output Voltage, V_{OUT}, Vrms	32.94	33.07	36.51
Output Current, I_{OUT}, Arms	12.57	12.9	13.6
Total Output Power, P_{OUT}, W	414.1	427	497
Efficiency,* η, %	74.5	75.0	73.0

*Total Efficiency, η_{TOTAL} = 74.2%

TABLE 4-12. UNITY POWER FACTOR POWER MEASUREMENTS

	Phase		
	1	2	3
Input Power			
Input Voltage, V_{IN}, Vdc	50.0	50.2	50.4
Input Current, I_{IN}, Adc	18.30	15.90	26.0
Total Input Power, P_{IN}, W	915	798	1310
Output Power (Resistive Loads)			
Output Voltage, V_{OUT}, Vrms	40.9	43.05	56.33
Output Current, I_{OUT}, Arms	15.07	13.37	14.77
Total Output Power, P_{OUT}, W	616	575.6	832.0
Efficiency,** η, %	67.3	72.1	63.5

*f = 20.3 kHz

**Total Efficiency, η_{TOTAL} = 66.9%

TABLE 4-13. LAGGING POWER FACTOR POWER MEASUREMENTS

	TABLE 4-14			TABLE 4-15			TABLE 4-16		
MEASUREMENTS	POWER FACTOR CONDITIONS								
	0.7 LAGGING			0.7 LEADING			UNBALANCED PF		
I. INPUT									
Input Voltage (Vdc)	149.65			153.0			149.93		
Input Current (Idc)	123.6			125.4			141		
Input Power (kW)	18.5			19.2			21.1		
II. BUS (INV. END)	ØA	ØB	ØC	ØA	ØB	ØC	ØA	ØB	ØC
Voltage (Vrms) (Line-neutral)	437.7	440.4	435.7	431.7	440.6	446.8	436.4	439.8	446.8
Current (Irms)	--	--	--	--	--	--	--	--	--
Total Harmonic Distort. (%)	--	--	--	--	--	--	--	--	--
Frequency (kHz)	19.95			--			--		
III. OUTPUT									
AC RCVR OUTPUT									
Voltage (Vrms)	OFF			OFF			OFF		
Current (Irms)									
Power (kW)									
Total Harm. Dis. (%)									
DC RCVR OUTPUT									
Voltage (Vdc)	OFF			OFF			OFF		
Current (Idc)									
Power (kW)									
BD RCVR OUTPUT									
Voltage (Vdc)	OFF			OFF			OFF		
Current (Idc)									
Power (kW)									
RESISTIVE LOADS	ØA	ØB	ØC	ØA	ØB	ØC	ØA	ØB	ØC
Voltage (Vrms)	414.5	414.2	407.0	449.6	458.2	463.6	427.9	412.2	466.0
Current (Irms)	15.5	17.0	19.2	14.6	15.0	15.1	16.7	17.2	15.1
Power (kW)	4.43	4.93	5.47	4.66	5.02	5.11	7.14	5.03	5.49
Power Factor	0.69La	0.70La	0.70La	0.71Le	0.73Le	0.73Le	0.9997	0.71La	0.78Le
POWER IN (kW)	18.5			19.2			21.1		
POWER OUT (kW)	14.8			14.8			17.7		
EFFICIENCY (%)	80.0			77.1			83.9		

TABLES 4-14, 4-15, 4-16. POWER SYSTEM MEASUREMENTS WITH REACTIVE LOADING.

	MEASUREMENTS		
I. INPUT Input Voltage (Vdc) Input Current (Idc) Input Power (kW)	150 180 27		
II. OUTPUT AC RCVR OUTPUT Voltage (Vrms) Current (Irms) Power (kW) Total Harm. Dis. (%)	109 4.40 0.475		
DC RCVR OUTPUT Voltage (Vdc) Current (Idc) Power (kW)	28.1 23.1 0.649		
BD RCVR OUTPUT Voltage (Vdc) Current (Idc) Power (kW)	99 6.9 0.68		
RESISTIVE LOADS	ØA	ØB	ØC
Voltage (Vrms) Current (Irms) Power (kW)	426.1 16.53 7.04	423.4 16.48 6.98	427.5 17.66 7.55
POWER IN (kW)	27		
POWER OUT (kW)	23.4		
EFFICIENCY (%)	≈ 87		

TABLE 4-17. SYSTEM OPERATING CONDITIONS FOR THE EMI TESTING.

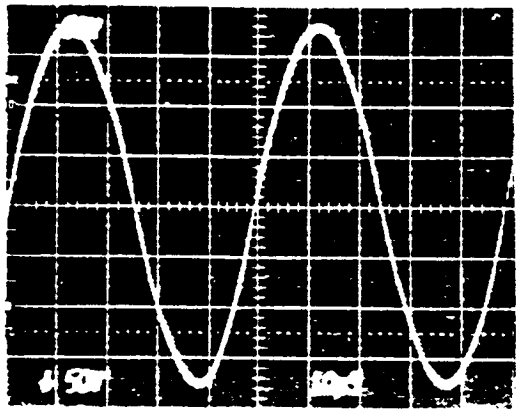


FIGURE 1-1. INVERTER OUTPUT VOLTAGE

ORIGINAL PAGE IS
OF POOR QUALITY

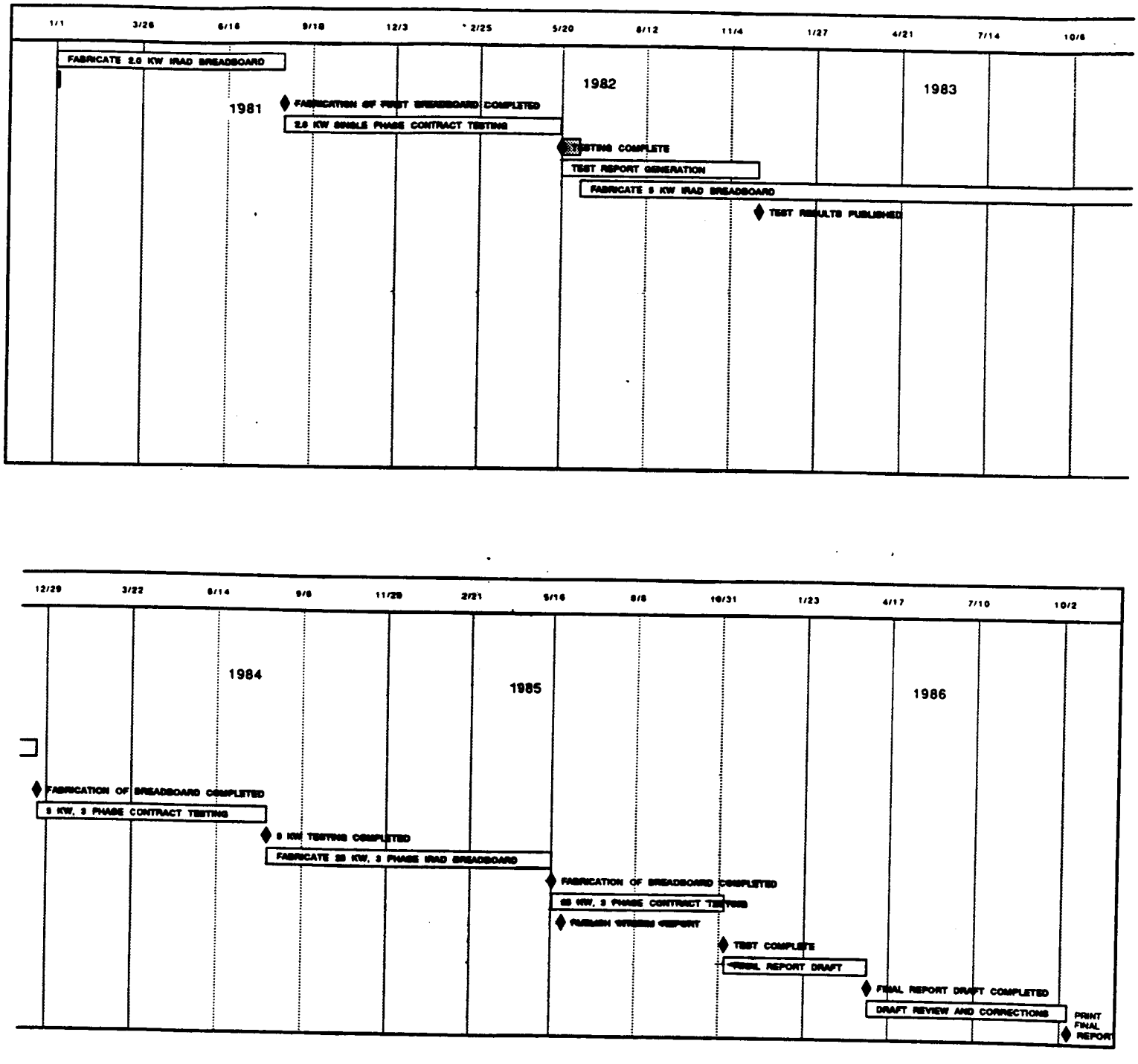


FIGURE 1-1.1 PROGRAM TIMELINE

C-2

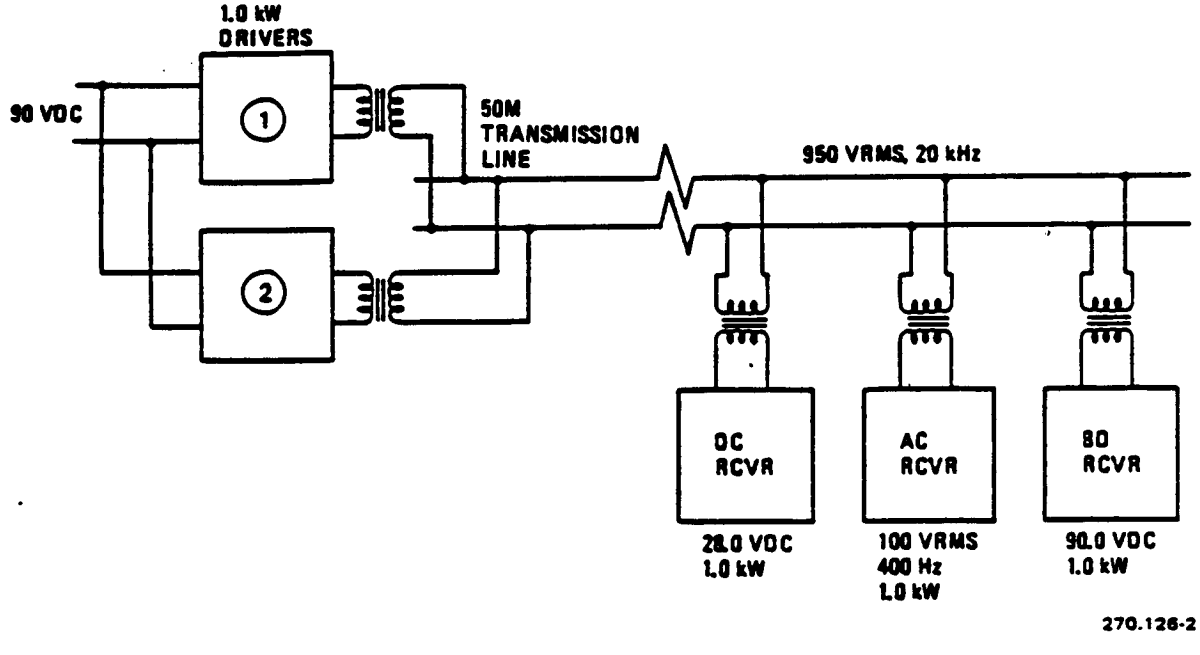


FIGURE 2-1. SINGLE-PHASE SYSTEM TEST CONFIGURATION

FIGURE 2-2. 5.0 KW, THREE-PHASE SYSTEM TEST CONFIGURATION

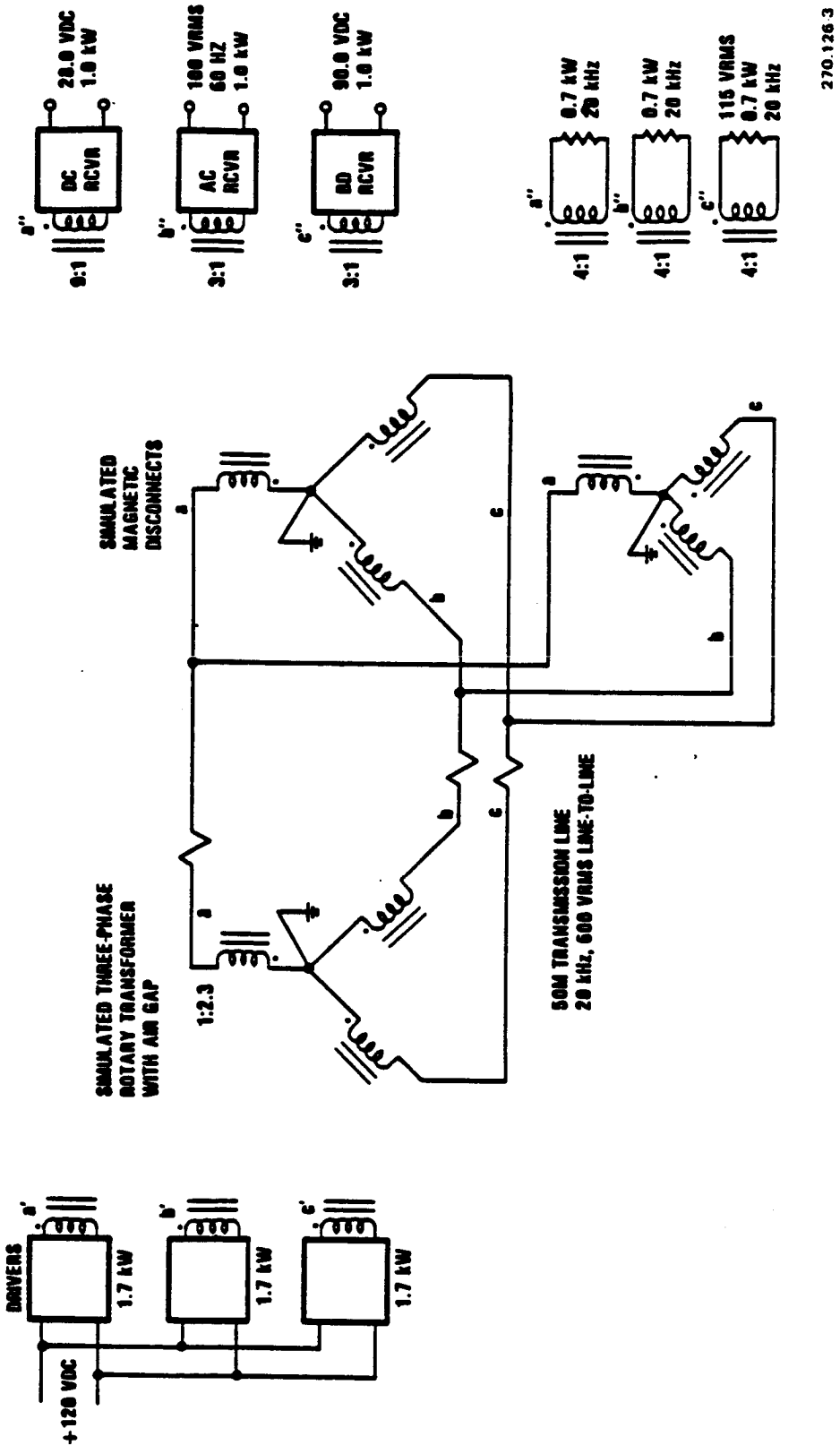
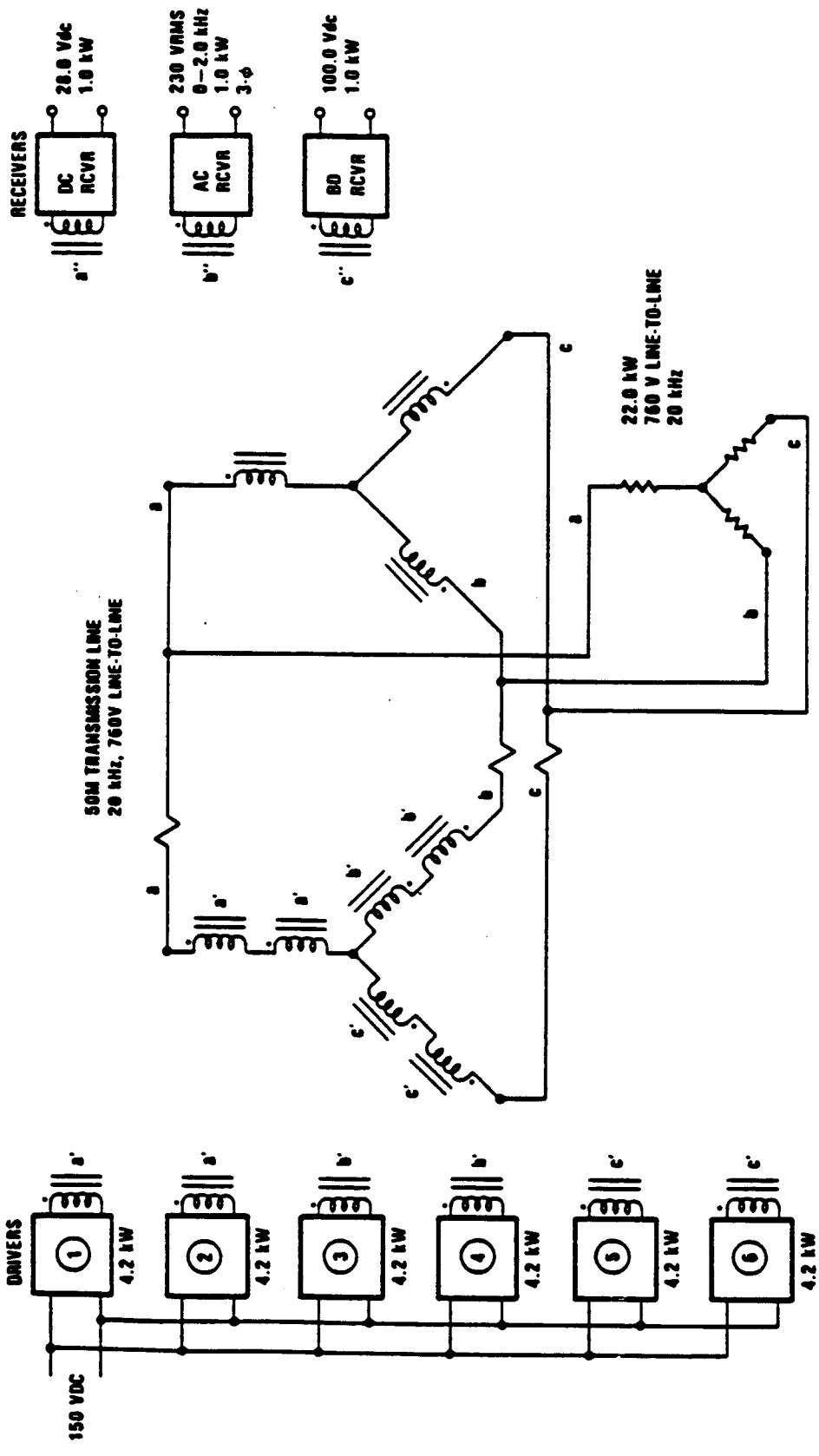
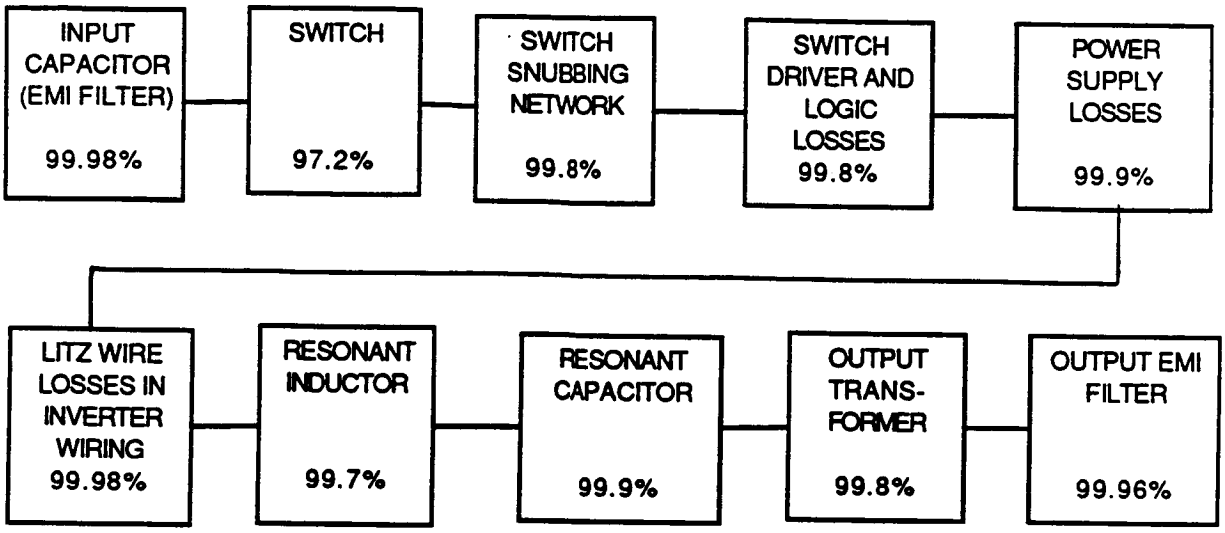


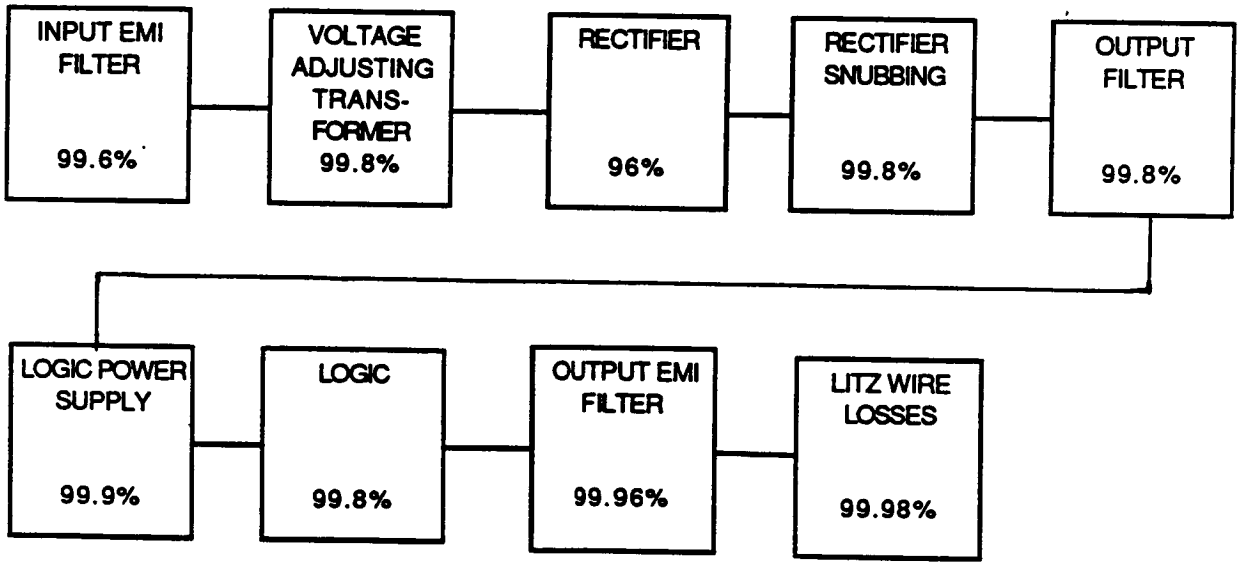
FIGURE 2-3. 25.0-KW SYSTEM CONFIGURATION.





FULL LOAD (6 KW), 150 VDC IN, 440 VAC OUT

FIGURE 2.4 INVERTER EFFICIENCY



FULL LOAD (5 KW), 440 VAC IN, 150 VDC OUT

FIGURE 2.5 CONVERTER EFFICIENCY

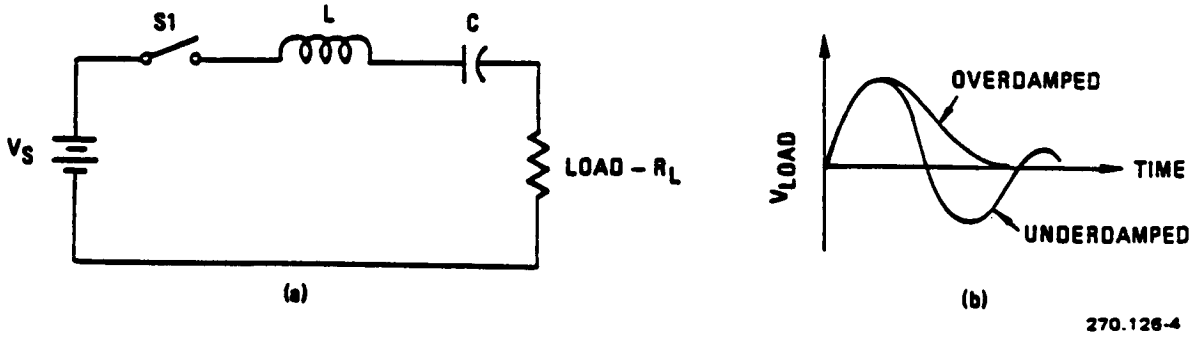


FIGURE 3-1. BASIC SERIES RESONANT CIRCUIT

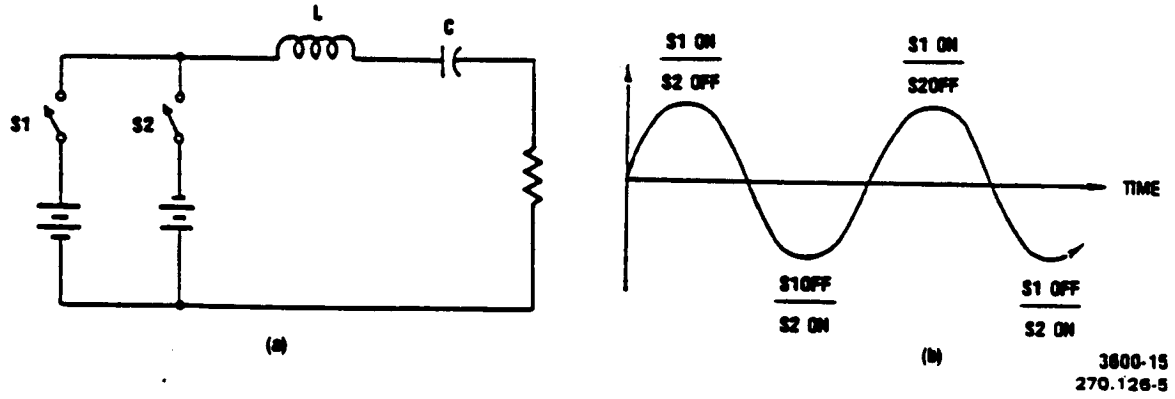


FIGURE 3-2. DUAL-POLARITY SERIES RESONANT CIRCUIT

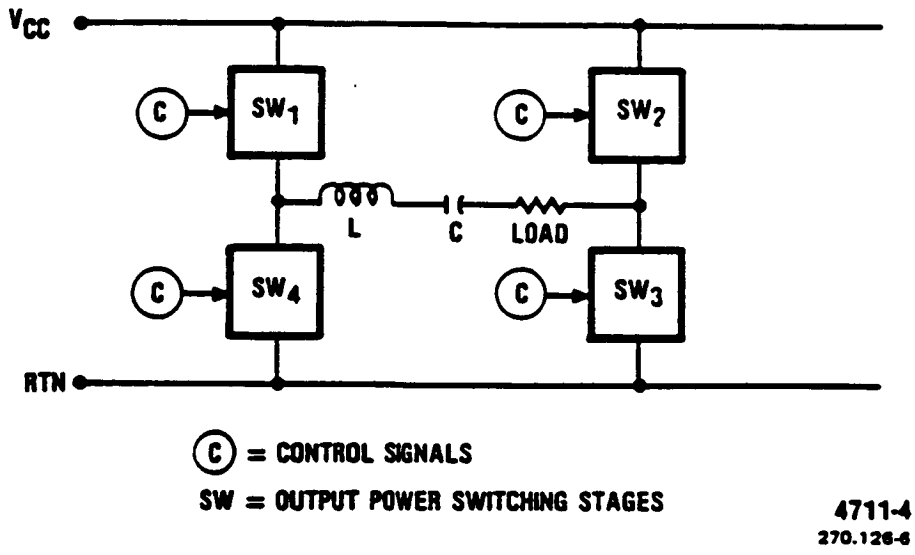


FIGURE 3-3. SERIES-OUTPUT TYPE SERIES RESONANT BRIDGE CIRCUIT

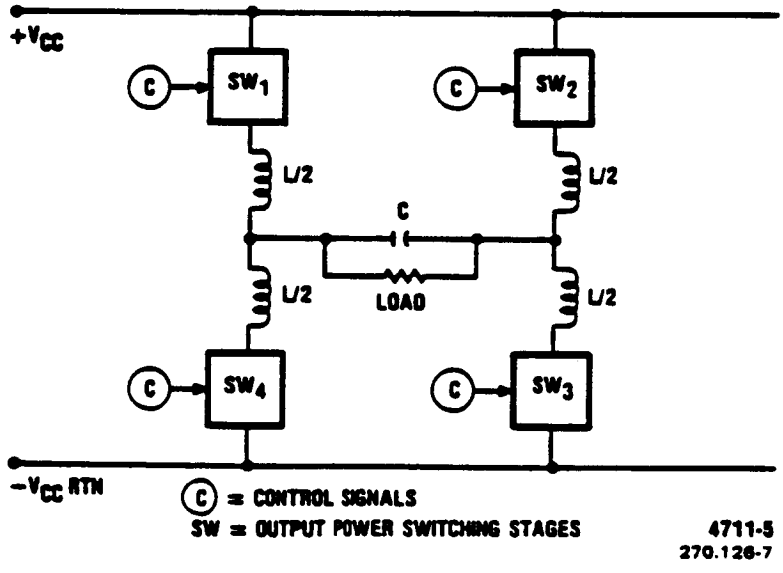


FIGURE 3-4. PARALLEL-OUTPUT TYPE SERIES RESONANT BRIDGE CIRCUIT

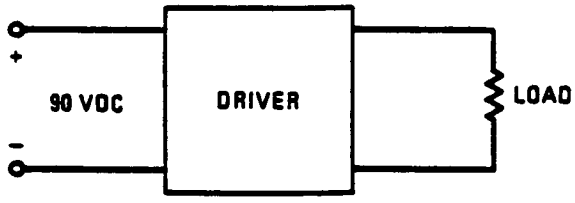


FIGURE 3-5. TEST CONFIGURATION 1: DRIVER WITH RESISTIVE LOAD

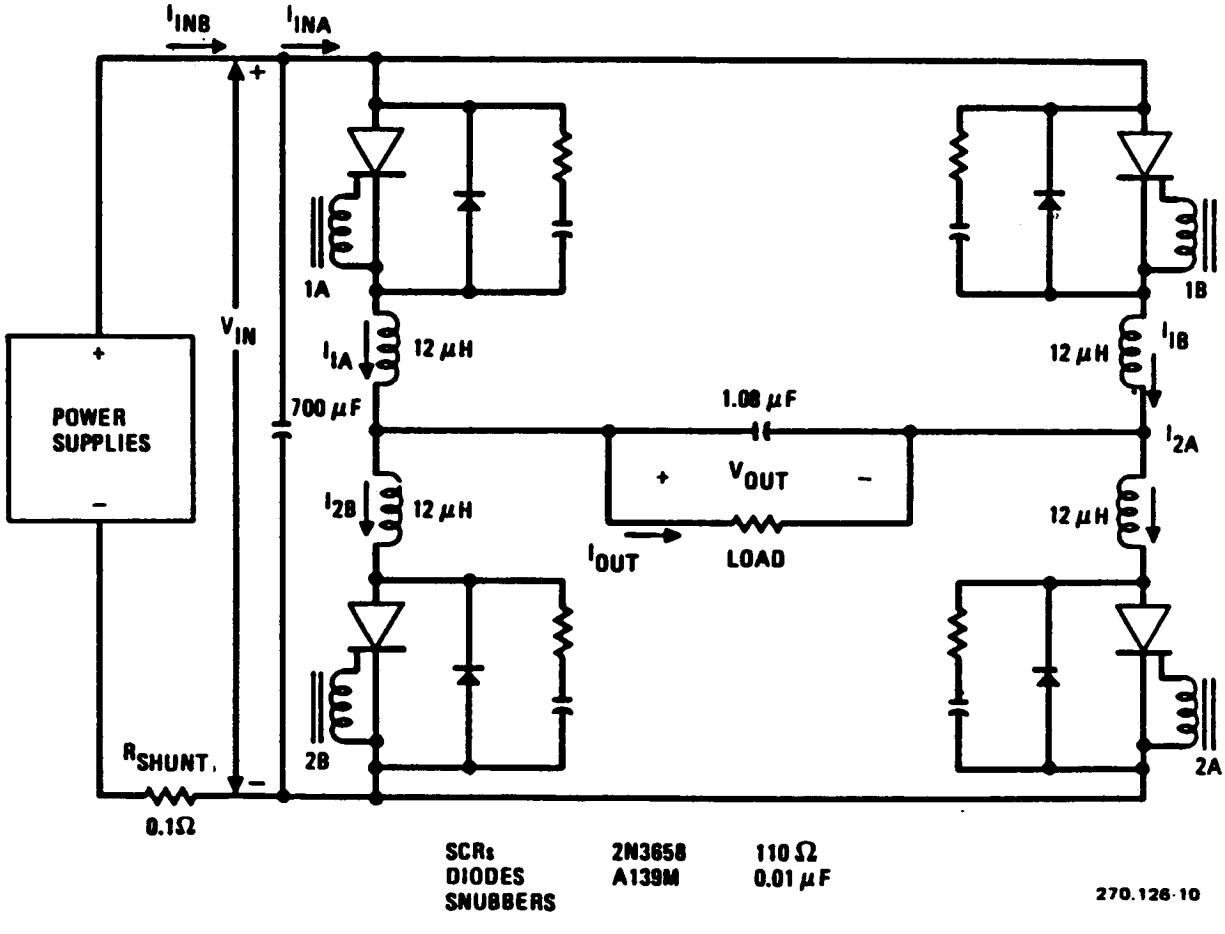
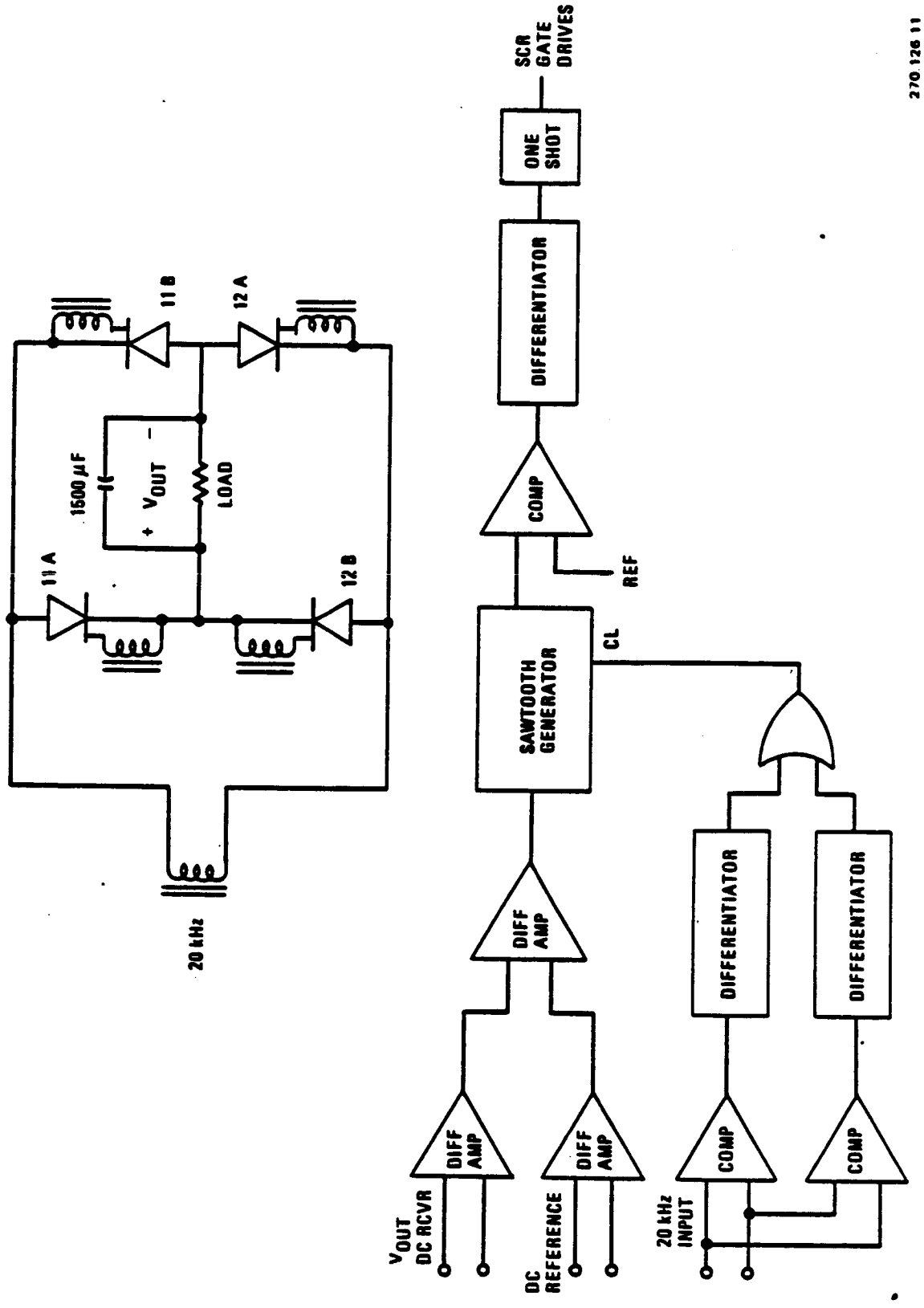


FIGURE 3-6. 1.0 KW INVERTER SCHEMATIC

FIGURE 3-7. BLOCK DIAGRAM OF THE DC RECEIVER MODULE AND ITS CLOSED-LOOP CONTROLLER



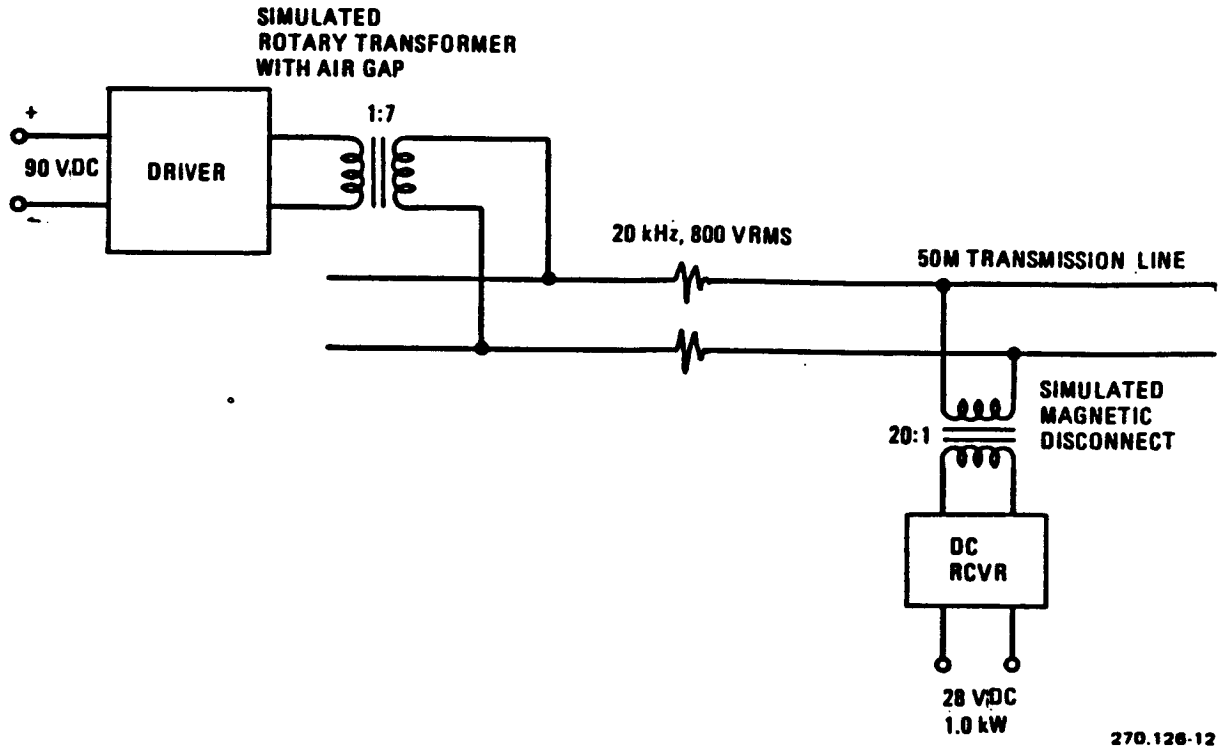


FIGURE 3-8. TEST CONFIGURATION 2: DRIVER-TRANSMISSION LINE-DC RECEIVER

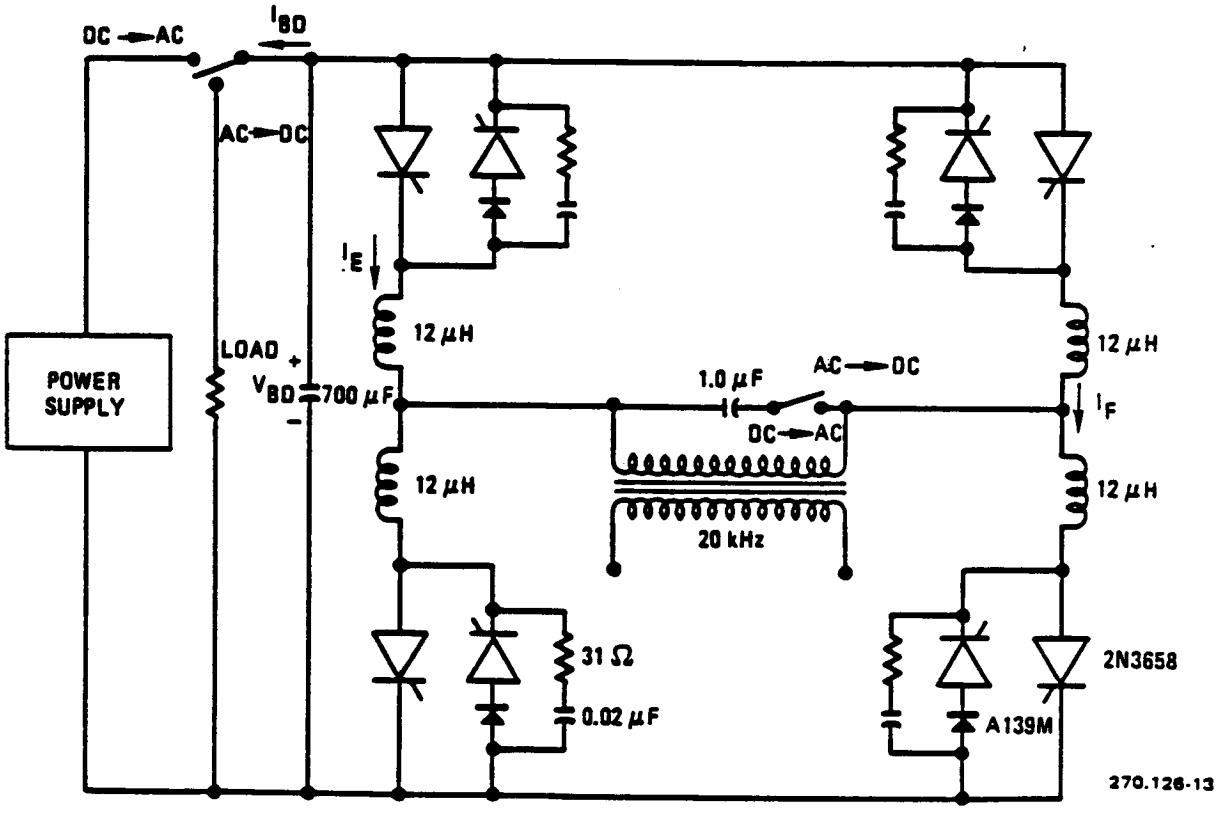


FIGURE 3-9. BIDIRECTIONAL MODULE SCHEMATIC

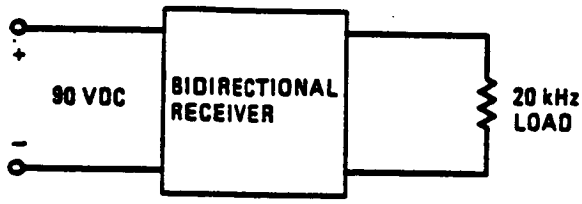


FIGURE 3-10. CONFIGURATION 3: BIDIRECTIONAL MODULE (DC-TO-AC MODE)

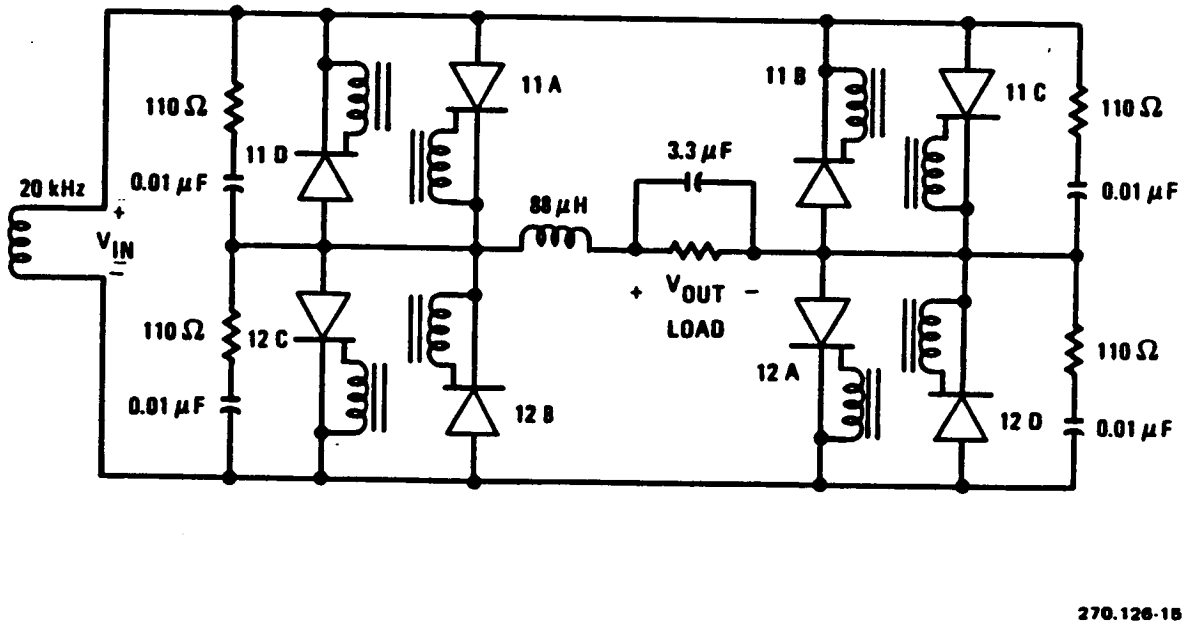


FIGURE 3-11. AC RECEIVER SCHEMATIC

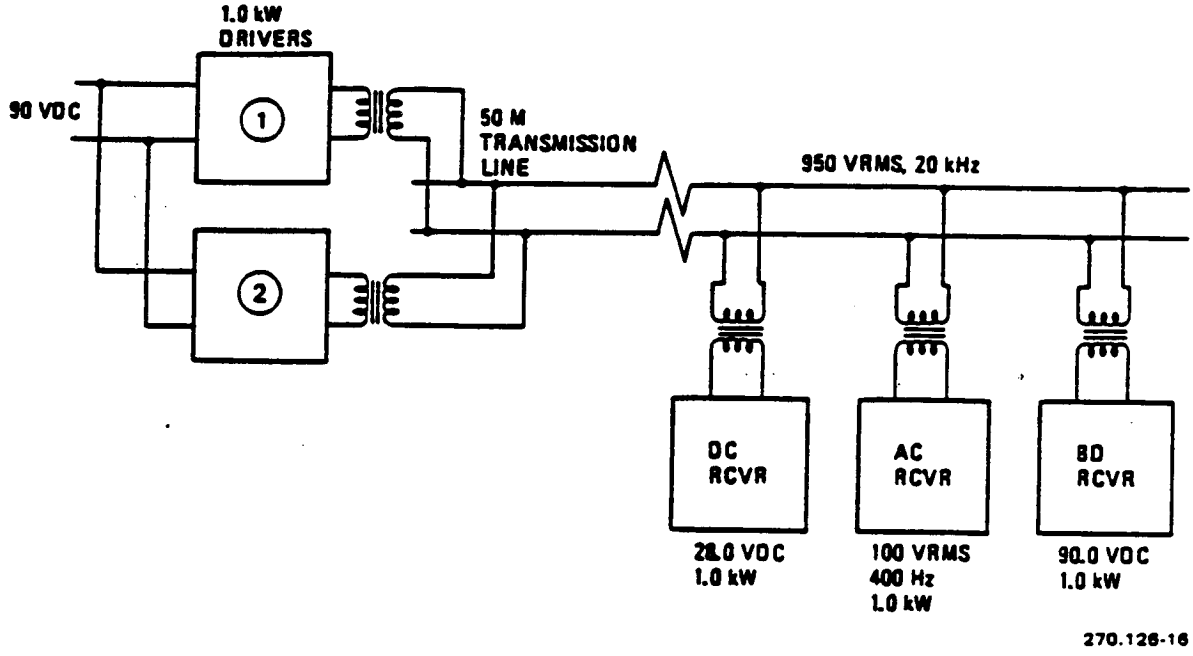
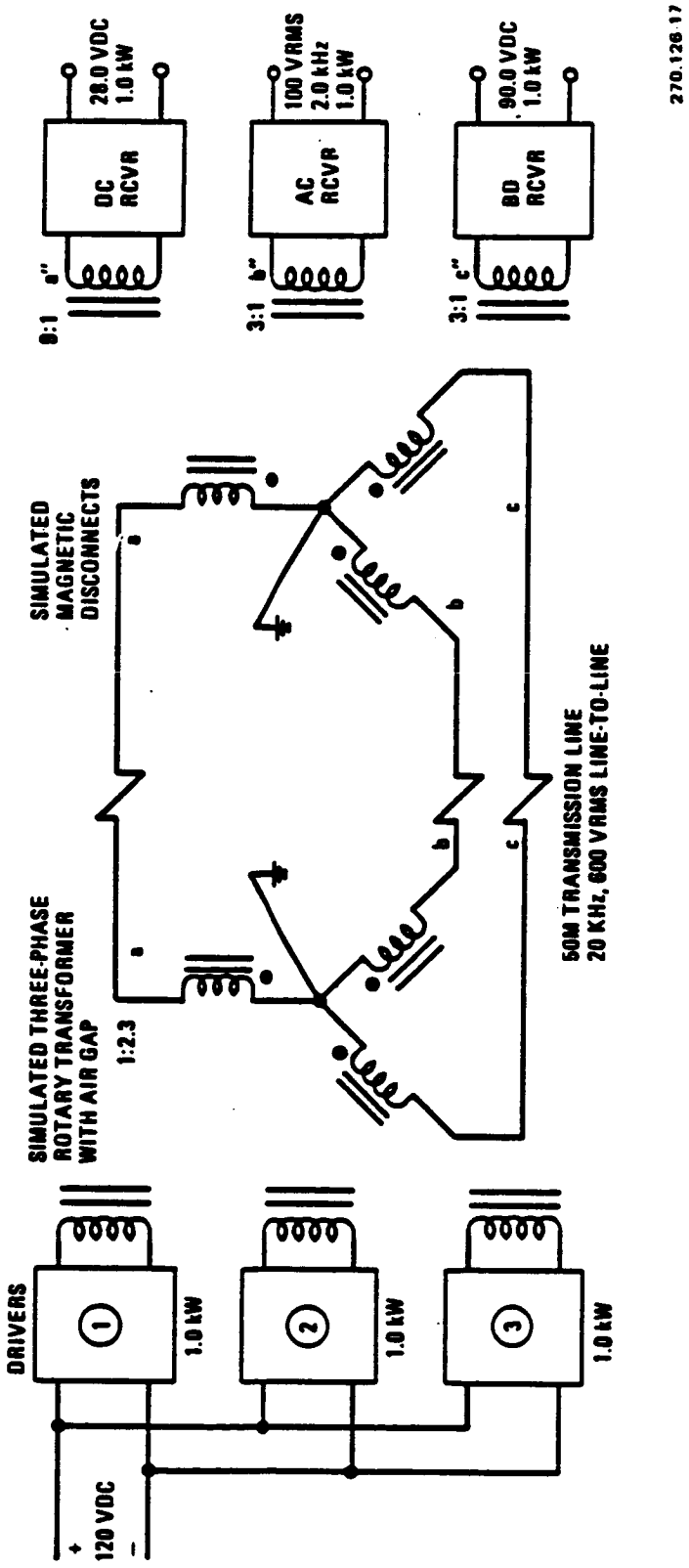


FIGURE 3-12. CONFIGURATION 4: TWO DRIVERS-TRANSMISSION LINE-THREE RECEIVERS

FIGURE 3-13. CONFIGURATION 5: THREE-PHASE DRIVERS - TRANSMISSION LINE - THREE RECEIVERS



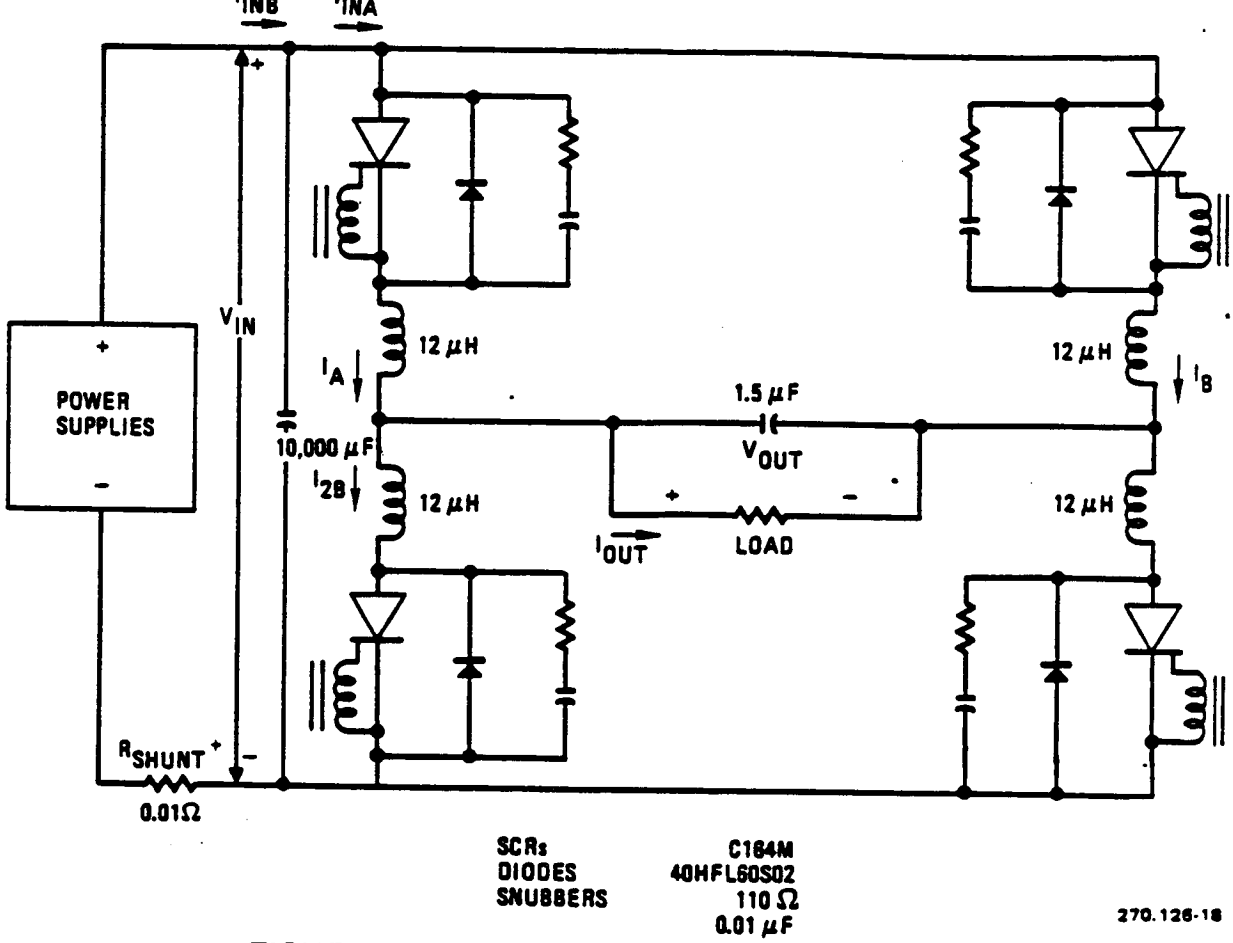


FIGURE 3-14. 2.0 KW INVERTER SCHEMATIC

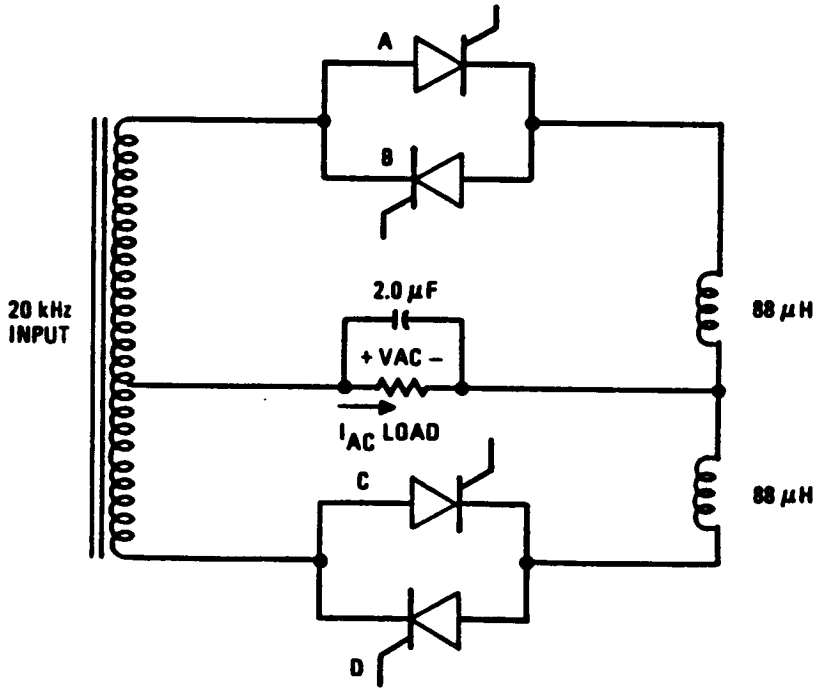
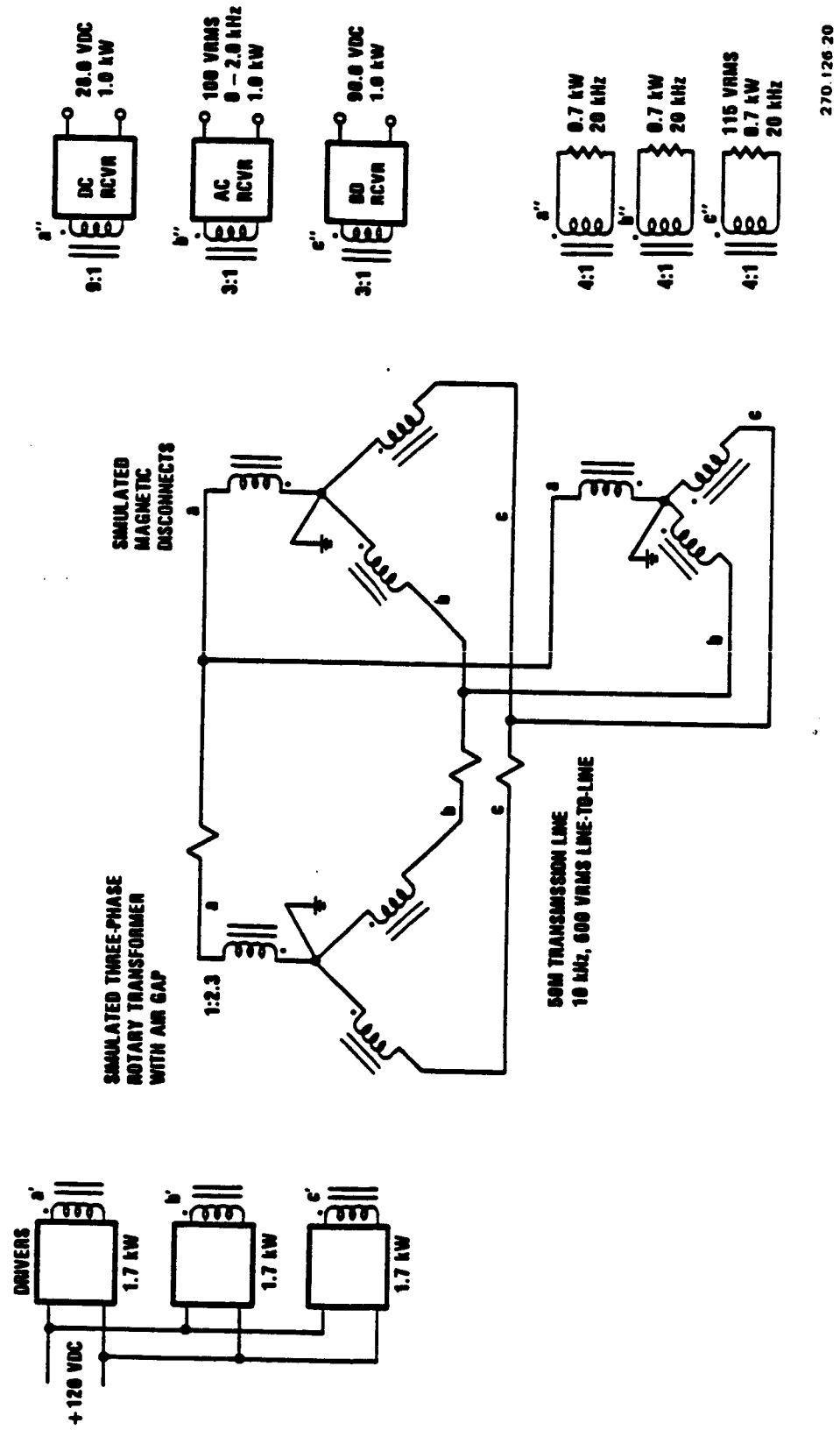


FIGURE 3-15. VARIABLE-VOLTAGE, VARIABLE-FREQUENCY AC RECEIVER SCHEMATIC

FIGURE 3-16. CONFIGURATION 6: THREE-PHASE DRIVER - TRANSMISSION LINE - THREE RECEIVERS AND 2.0 KW OF RESISTIVE LOADS



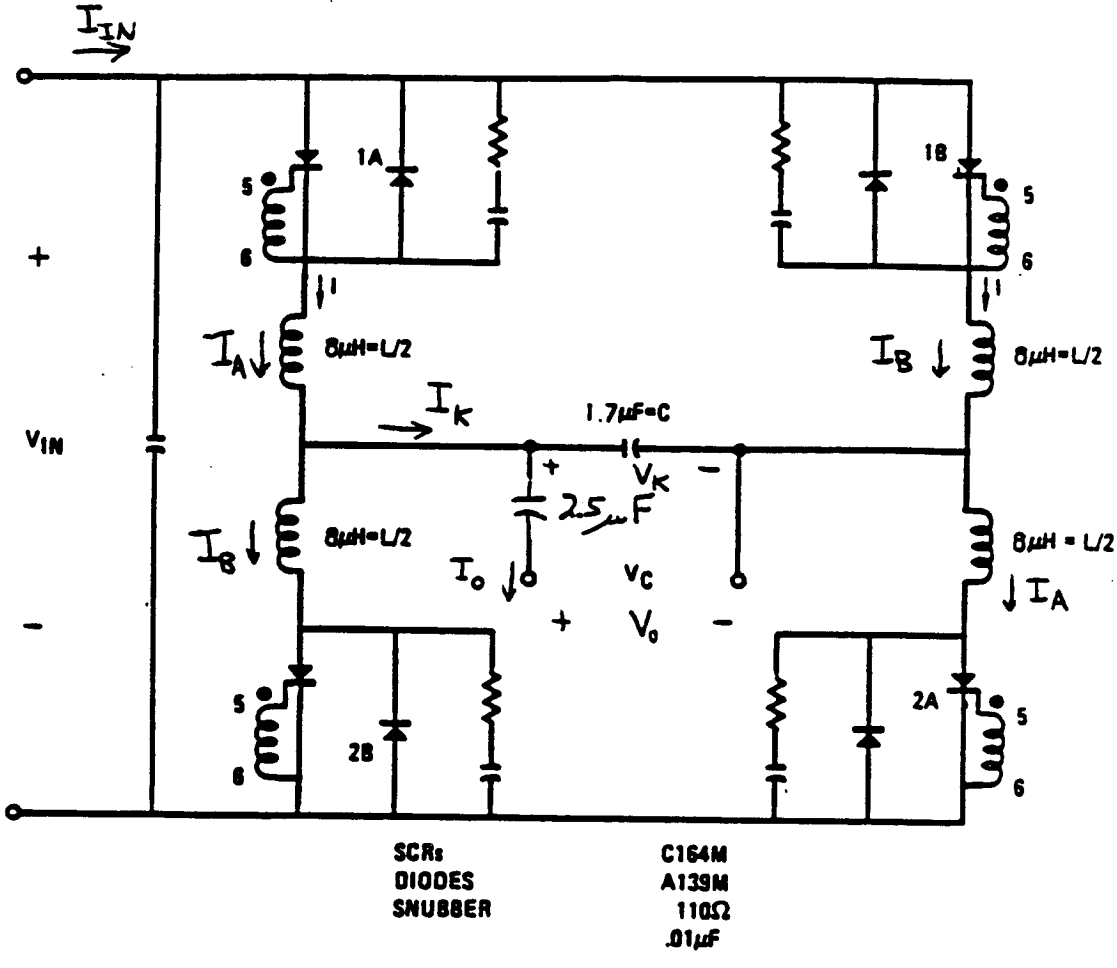
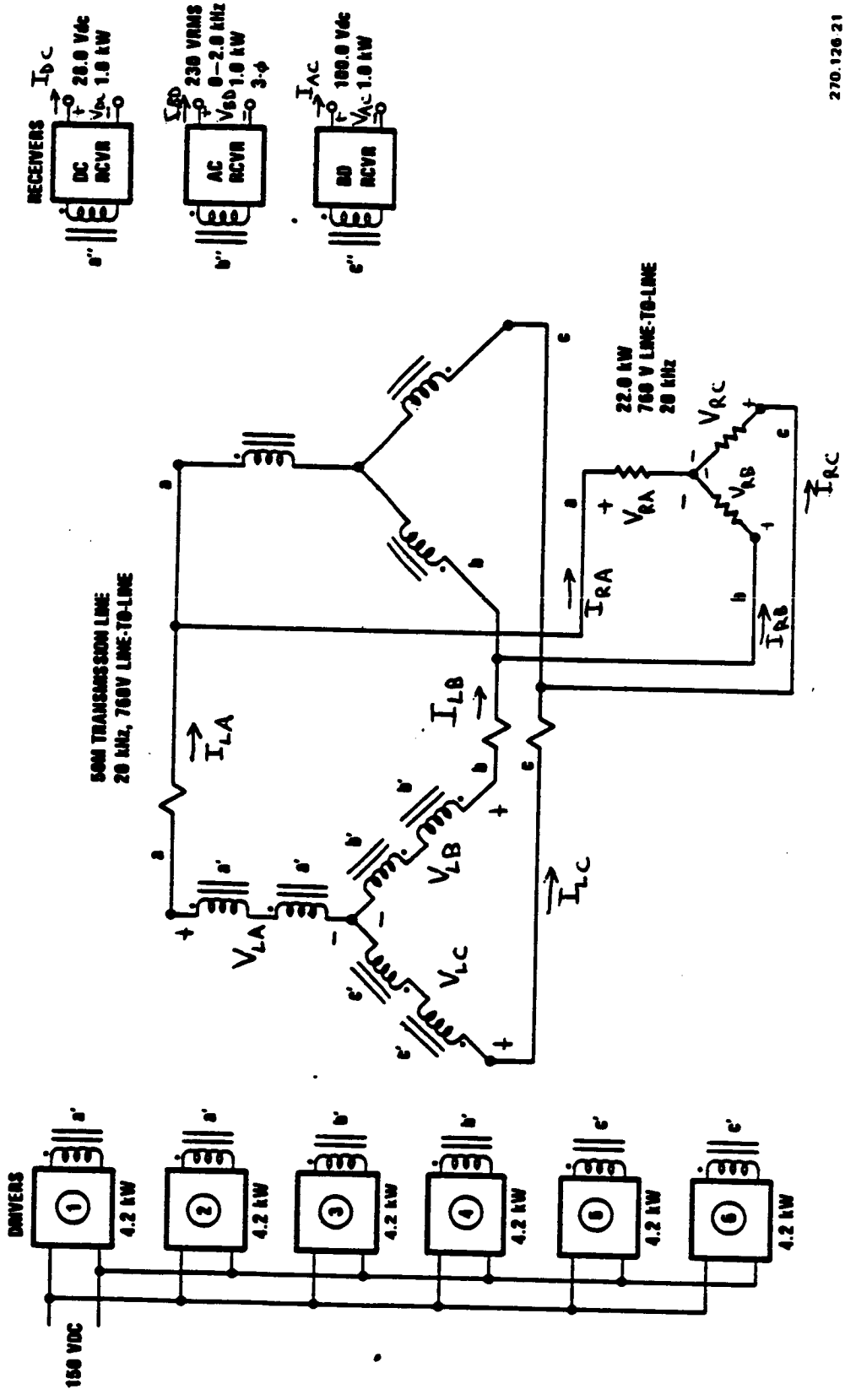
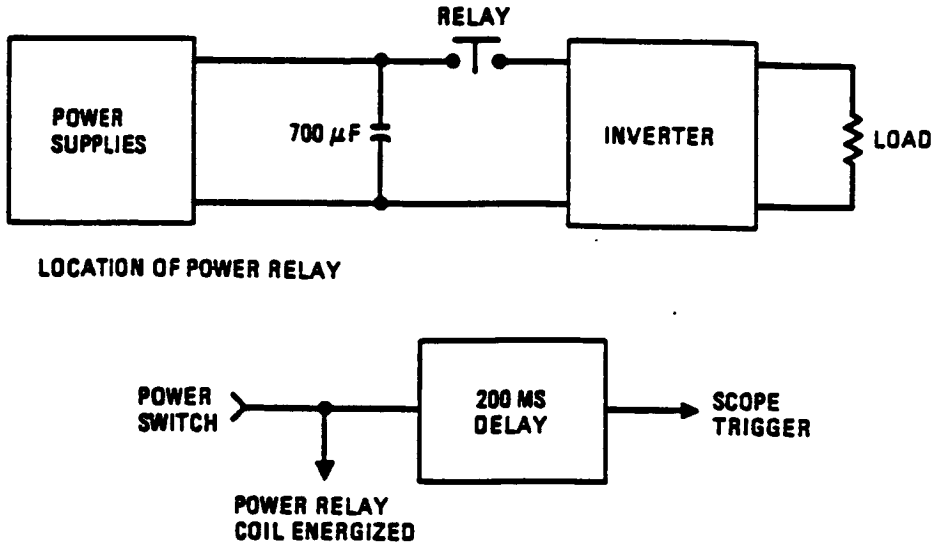


FIGURE 3-17 4.2 KW INVERTER SCHEMATIC

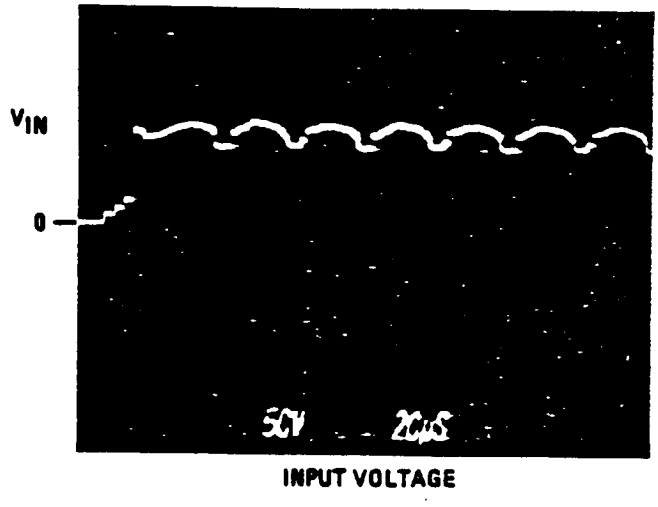
FIGURE 3-18. CONFIGURATION 7: 25 KW, THREE-PHASE DRIVER - TRANSMISSION LINE - THREE RECEIVERS AND RESISTIVE LOADS





270.126-22

FIGURE 4.1-1. START UP CIRCUIT FOR CONFIGURATION 1



INPUT VOLTAGE

270.126-23

FIGURE 4.1-2. INVERTER INPUT VOLTAGE

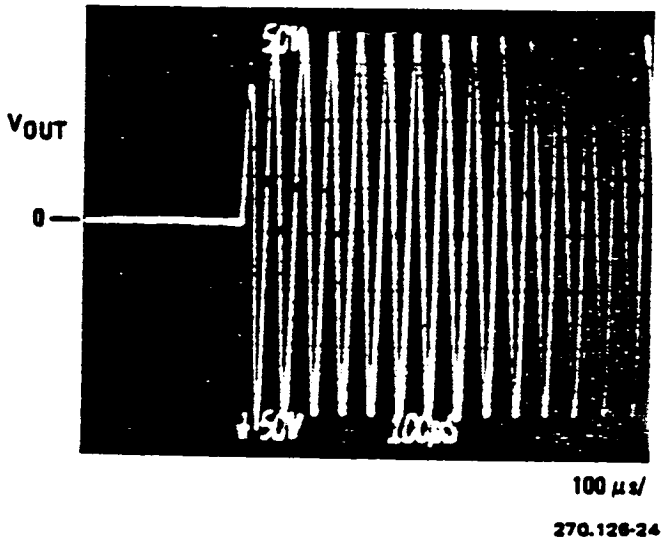


FIGURE 4.1-3. INVERTER OUTPUT VOLTAGE FOR 570W CASE

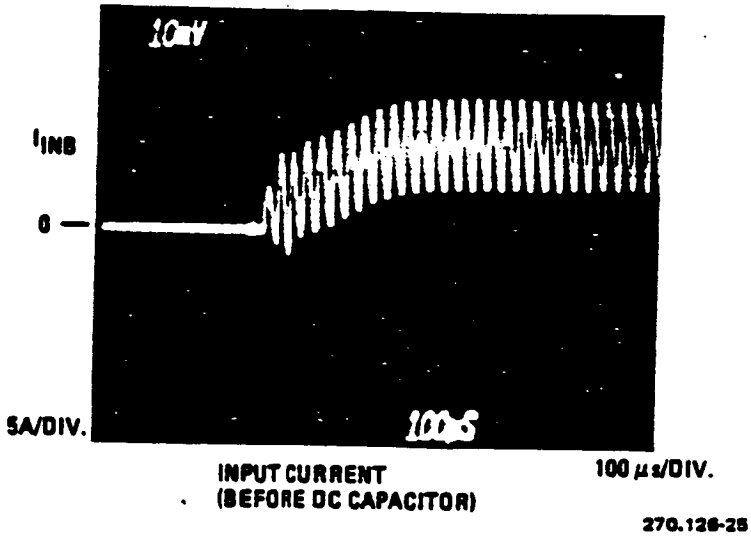


FIGURE 4.1-4. DC POWER SUPPLY OUTPUT CURRENT FOR THE 570W CASE

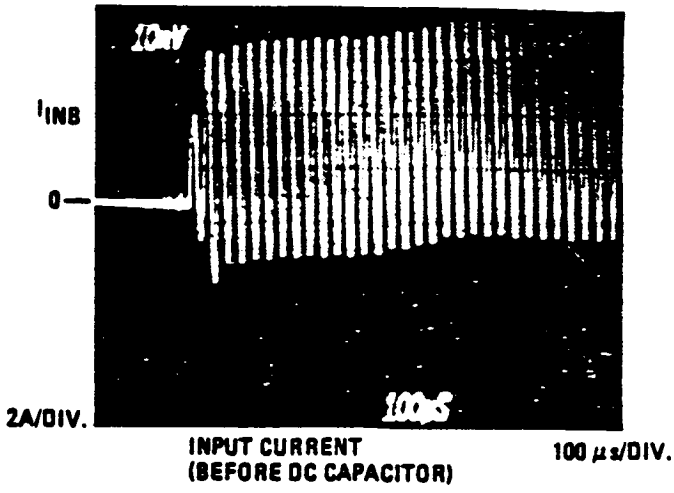


FIGURE 4.1-5. DC POWER SUPPLY OUTPUT CURRENT FOR THE 130W CASE AT START UP

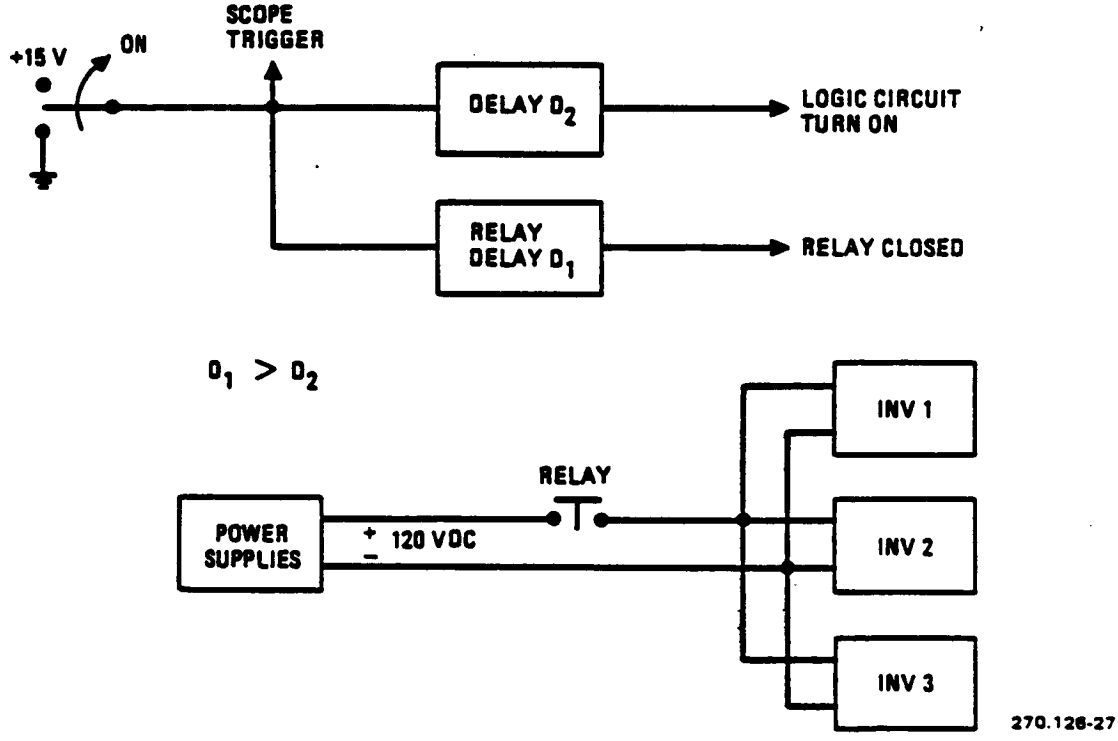


FIGURE 4.1-6. "LOGIC FIRST" START UP CIRCUIT

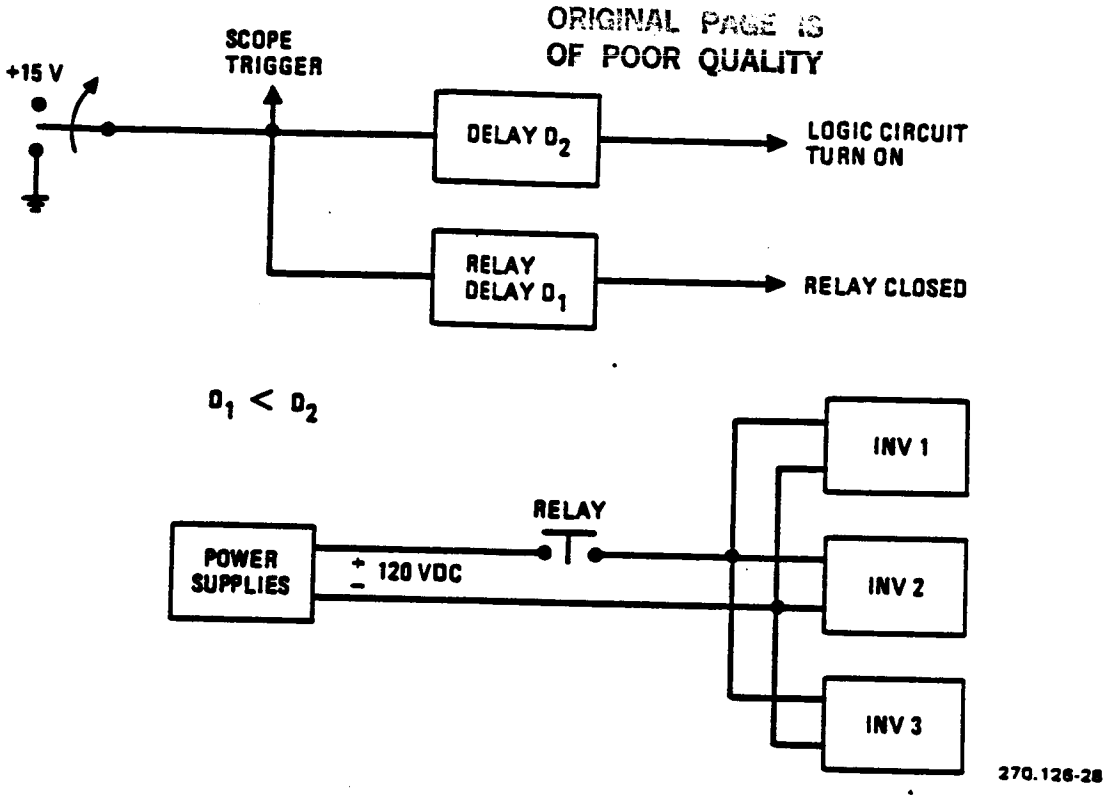


FIGURE 4.1-7. "RELAY FIRST" START UP CIRCUIT

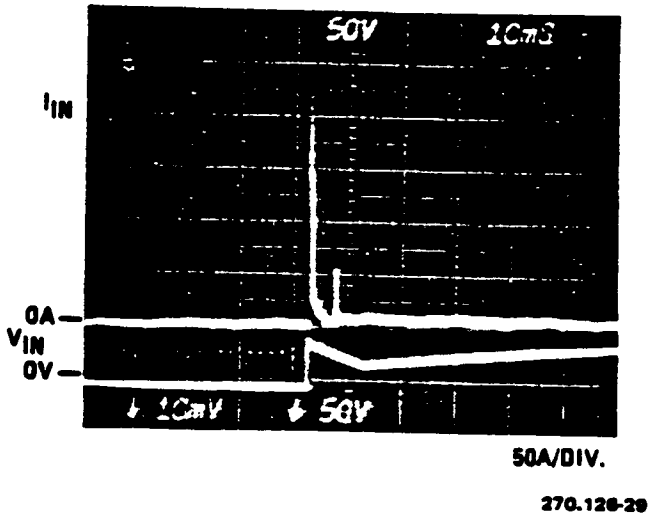
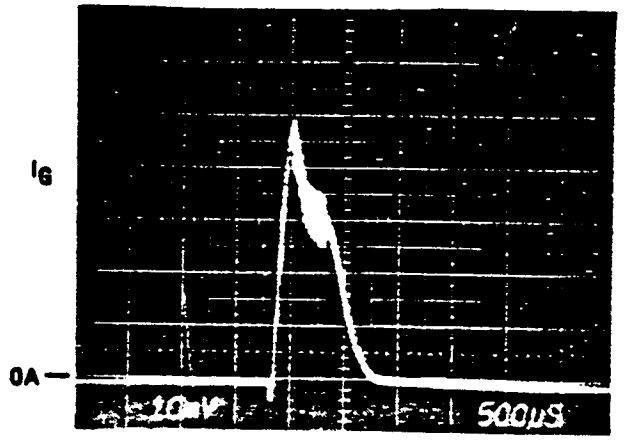


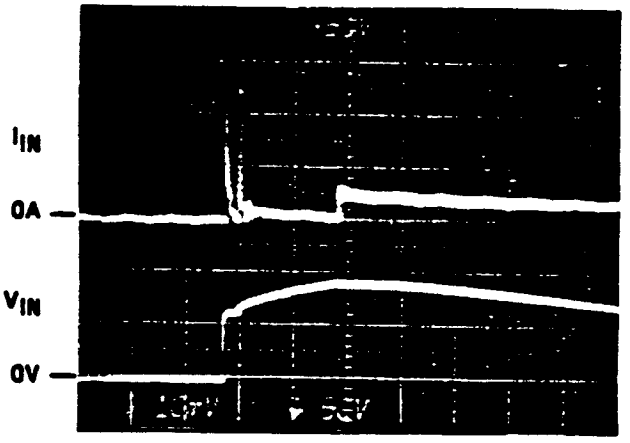
FIGURE 4.1-8. INVERTER INPUT CURRENT AT START UP



SCALE: 50A/DIV

270.126-30

FIGURE 4.1-9. INVERTER NUMBER 3 LEG CURRENT AT START UP



20 MS/

INPUT VOLTAGE AND CURRENT SCALE: 20A/

270.126-31

FIGURE 4.1-10. INPUT CURRENT AT START UP

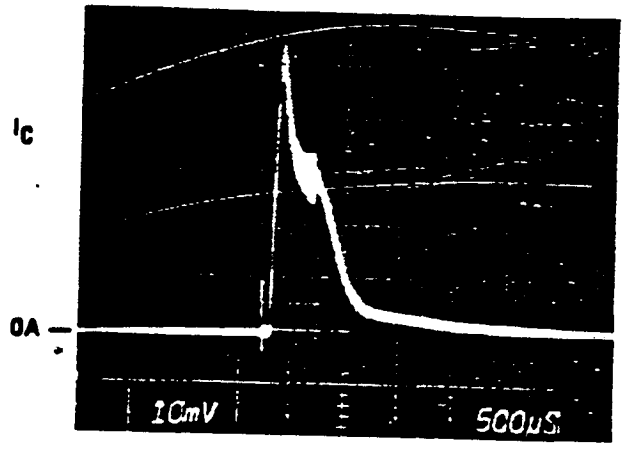


FIGURE 4.1-11. INVERTER 2 LEG CURRENT AT START UP

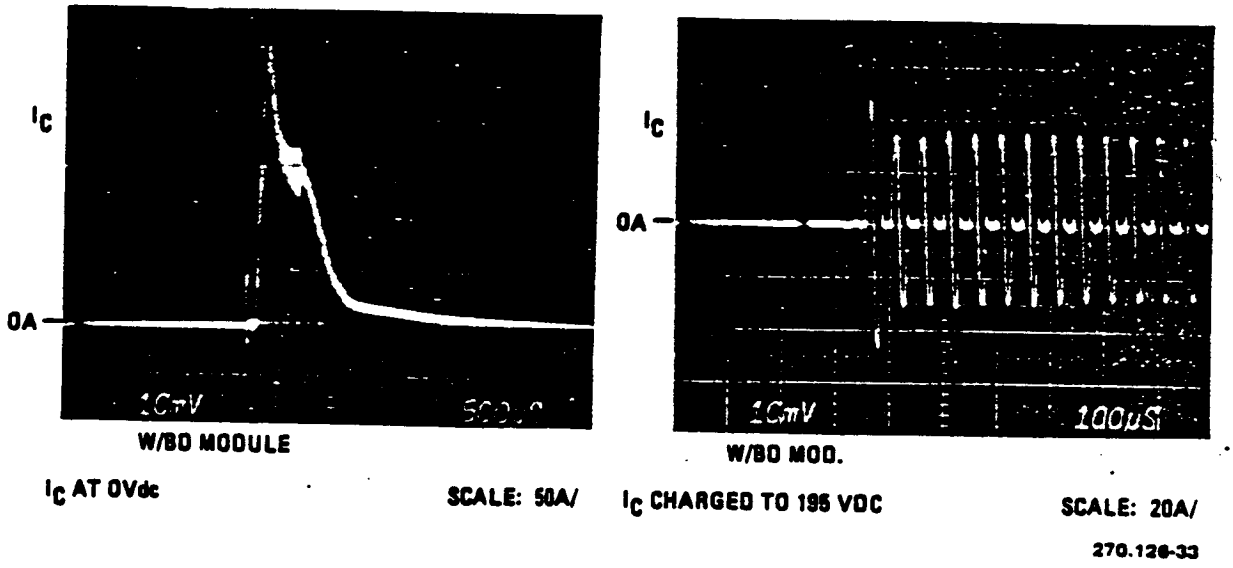


FIGURE 4.1-12. INVERTER 2 LEG CURRENT WITH THE FILTER CAPACITOR OF THE BIDIRECTIONAL MODULE CHARGED AND DISCHARGED

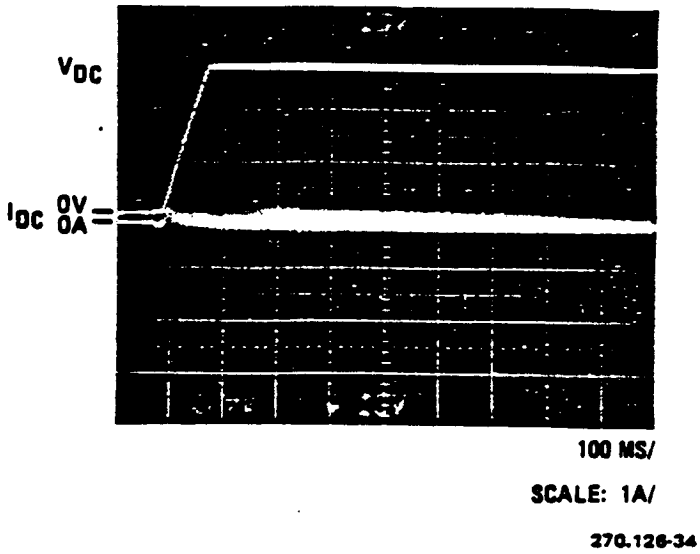


FIGURE 4.1-13. DC RECEIVER OUTPUT VOLTAGE AT START UP

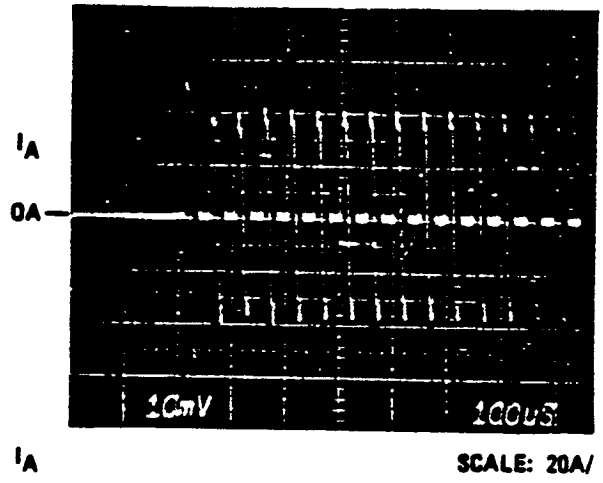


FIGURE 4.1-14. INVERTER 1 LEG CURRENT AT START UP FIGURE 4.2-22. THE SCHEMATIC FOR UNCOMPENSATED PHASOR REGULATION.

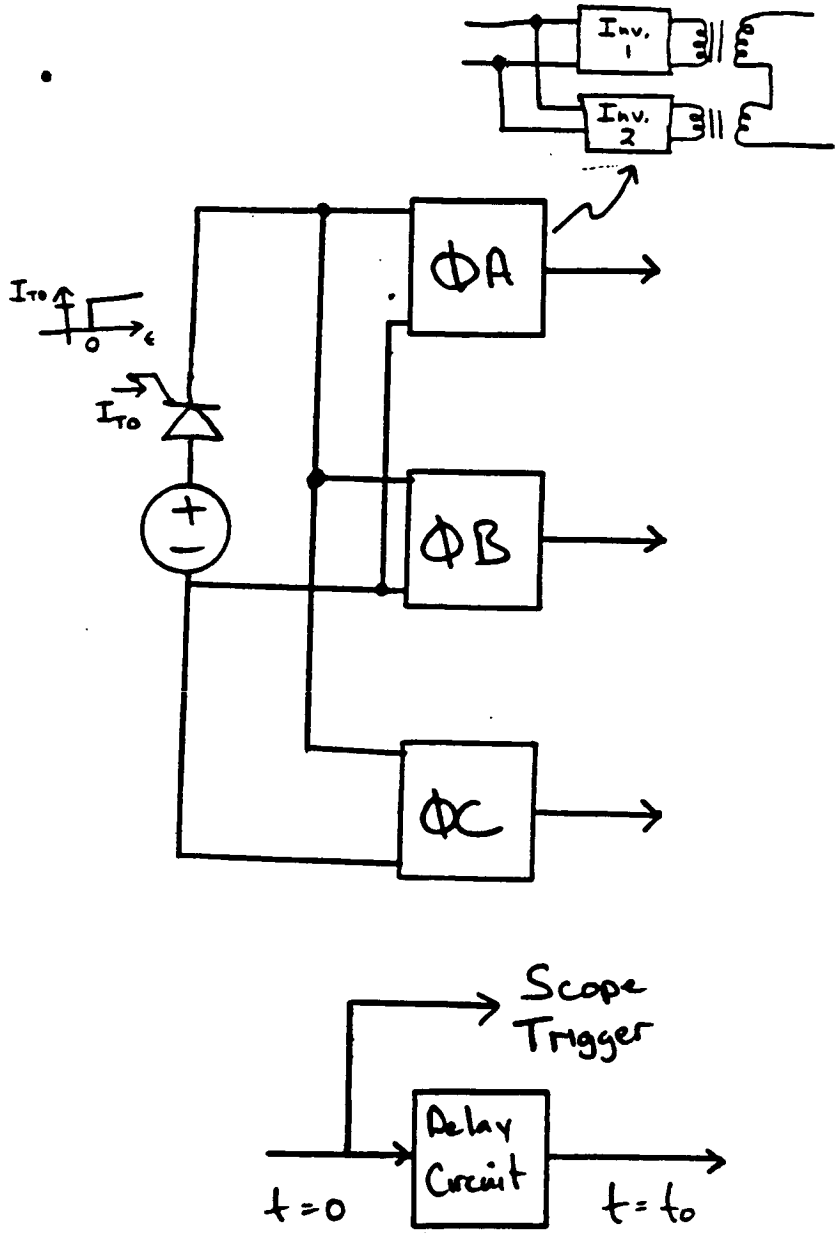
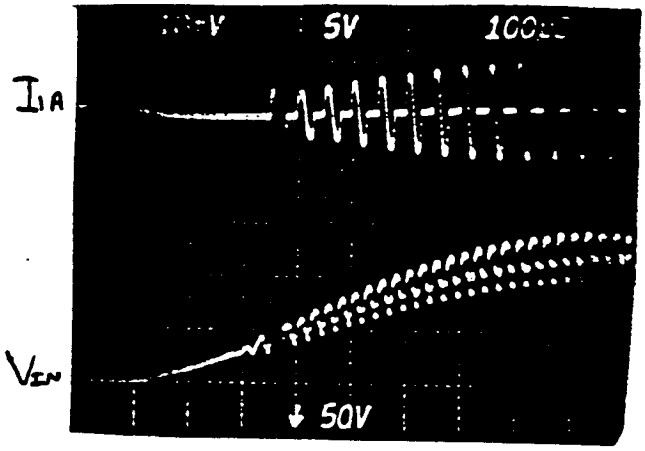
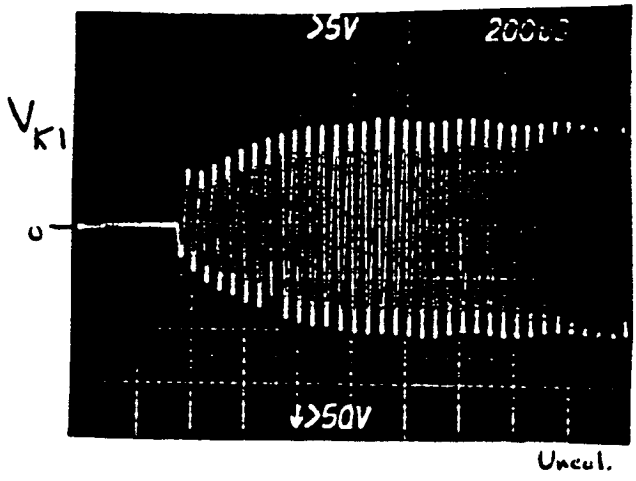


FIGURE 4.1-15. CIRCUIT USED TO STEP START THE SYSTEM.





Inverter | Output Voltage

FIGURE 4.1-16. INVERTER LEG CURRENT, OUTPUT VOLTAGE, AND INPUT VOLTAGE AT START UP.

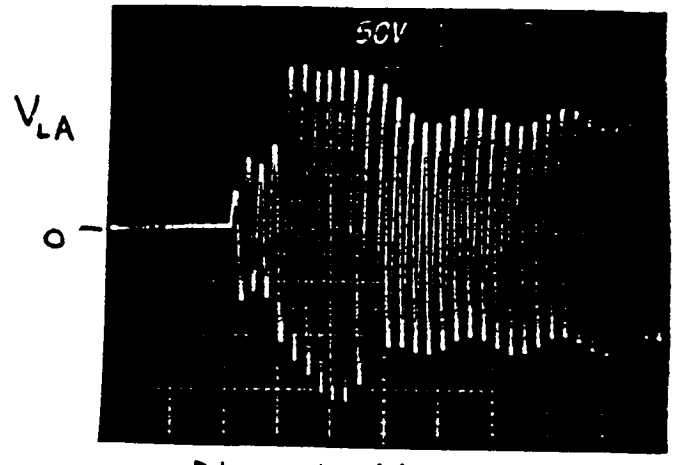
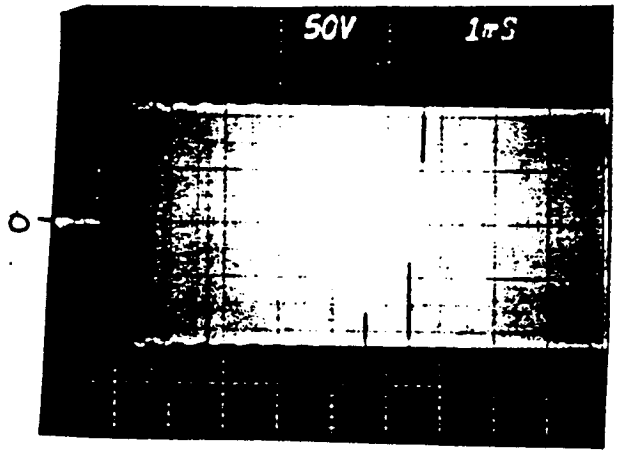


FIGURE 4.1-17. PHASE A BUS VOLTAGE AT STARTUP WITH NO LOAD.



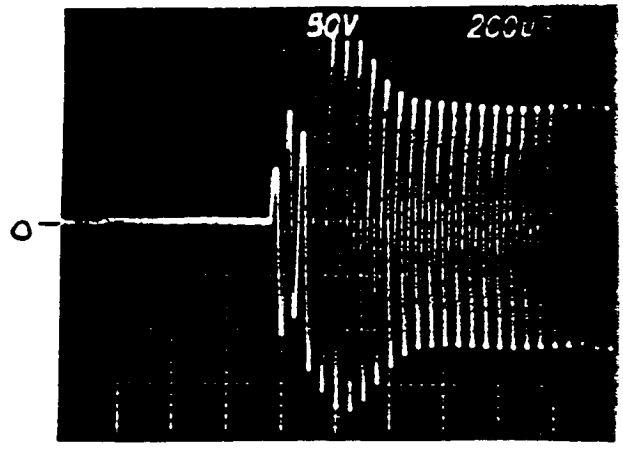
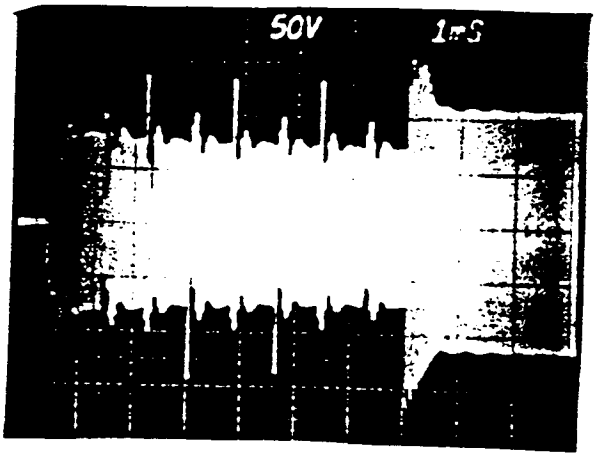
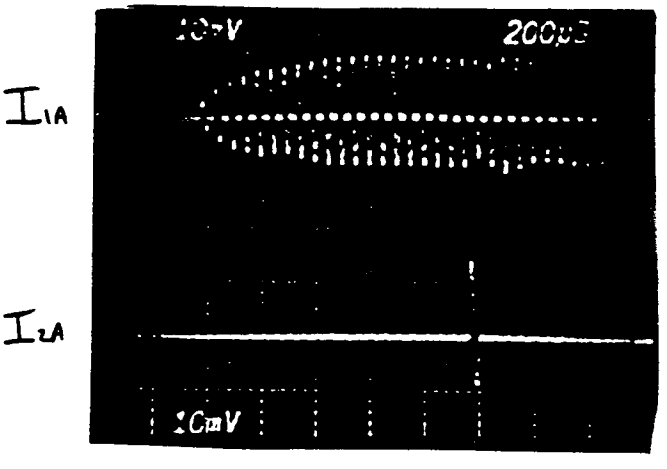


FIGURE 4.1-18. THE PHASE A BUS VOLTAGE STARTS SMOOTHLY WITH NO OSCILLATIONS WITH A 10% SYSTEM LOAD.



V_{LA}

Scale: 320V/Div



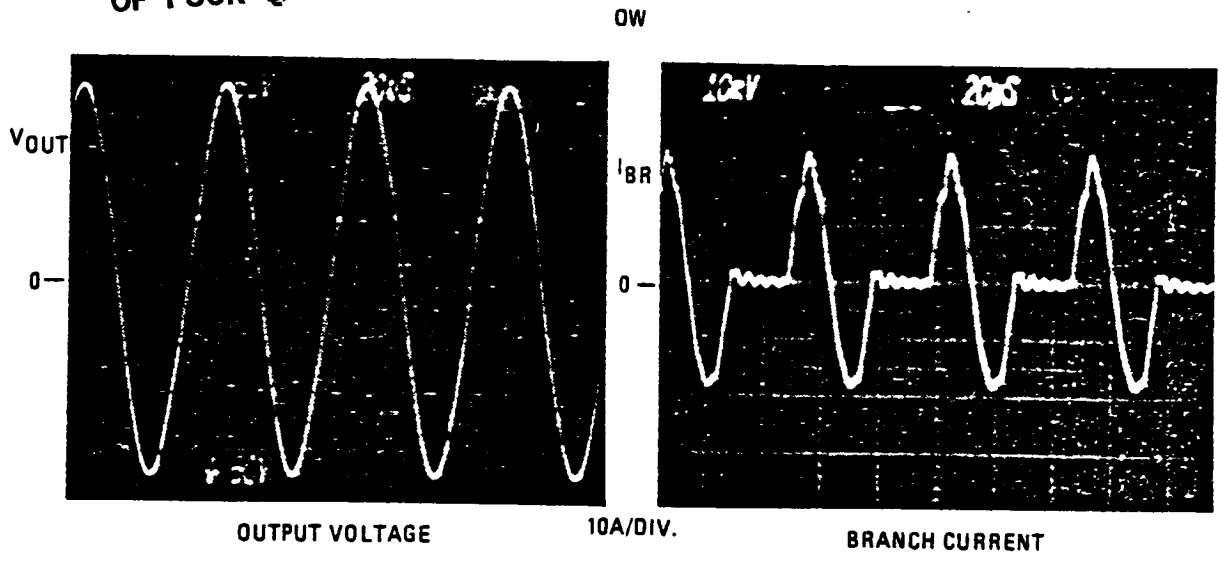
I_{1A}

I_{2A}

Scale: 50A/Div

FIGURE 4.1-19. THE PHASE A BUS VOLTAGE AND INVERTER LEG CURRENTS SHOW INVERTER 2 CONTINUALLY TRYING TO RESTART

ORIGINAL PAGE IS
OF POOR QUALITY



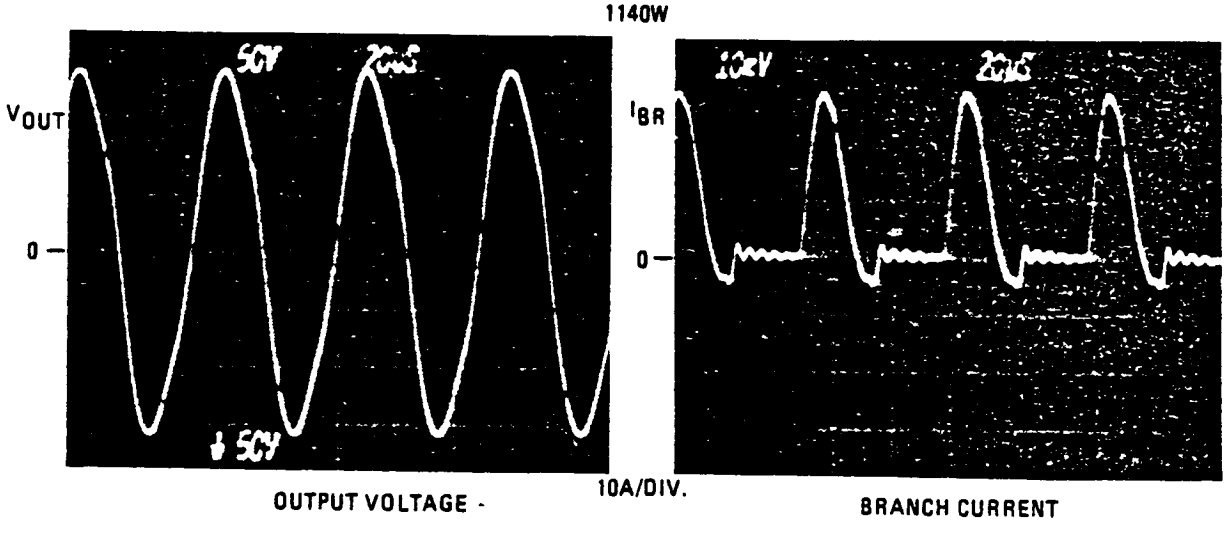


FIGURE 4.2-1. INVERTER LEG CURRENT WITH NO LOAD AND A 1.1KW LOAD

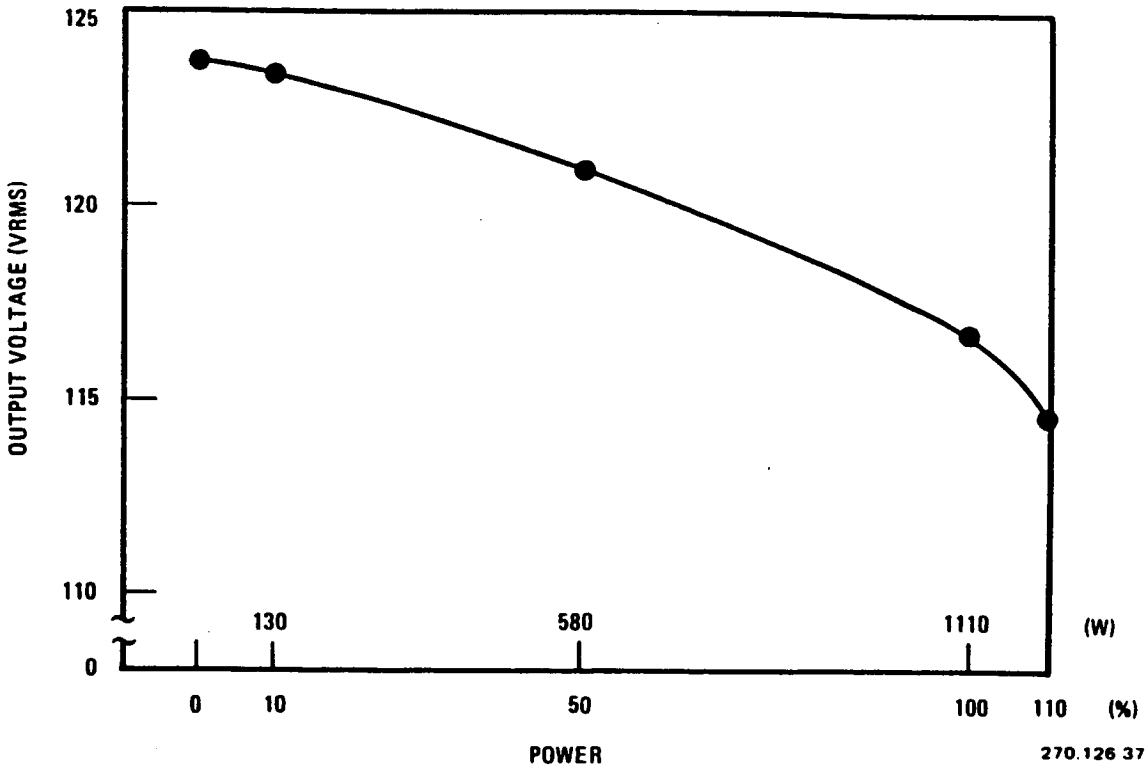


FIGURE 4.2-2. OUTPUT VOLTAGE VERSUS LOAD POWER

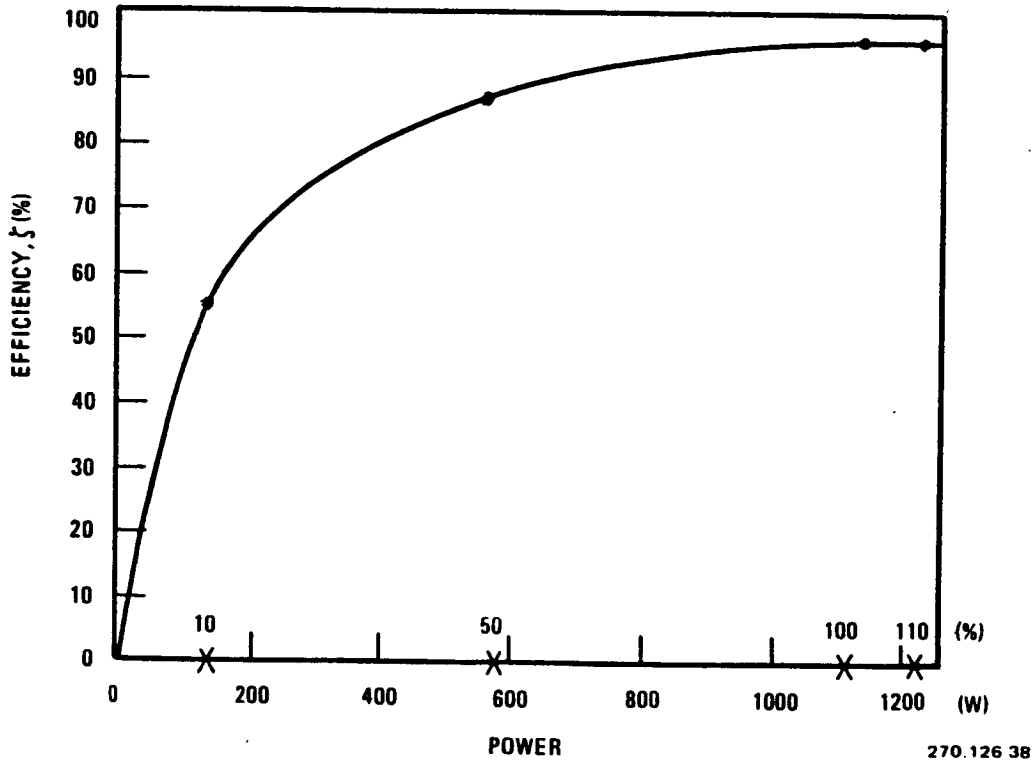
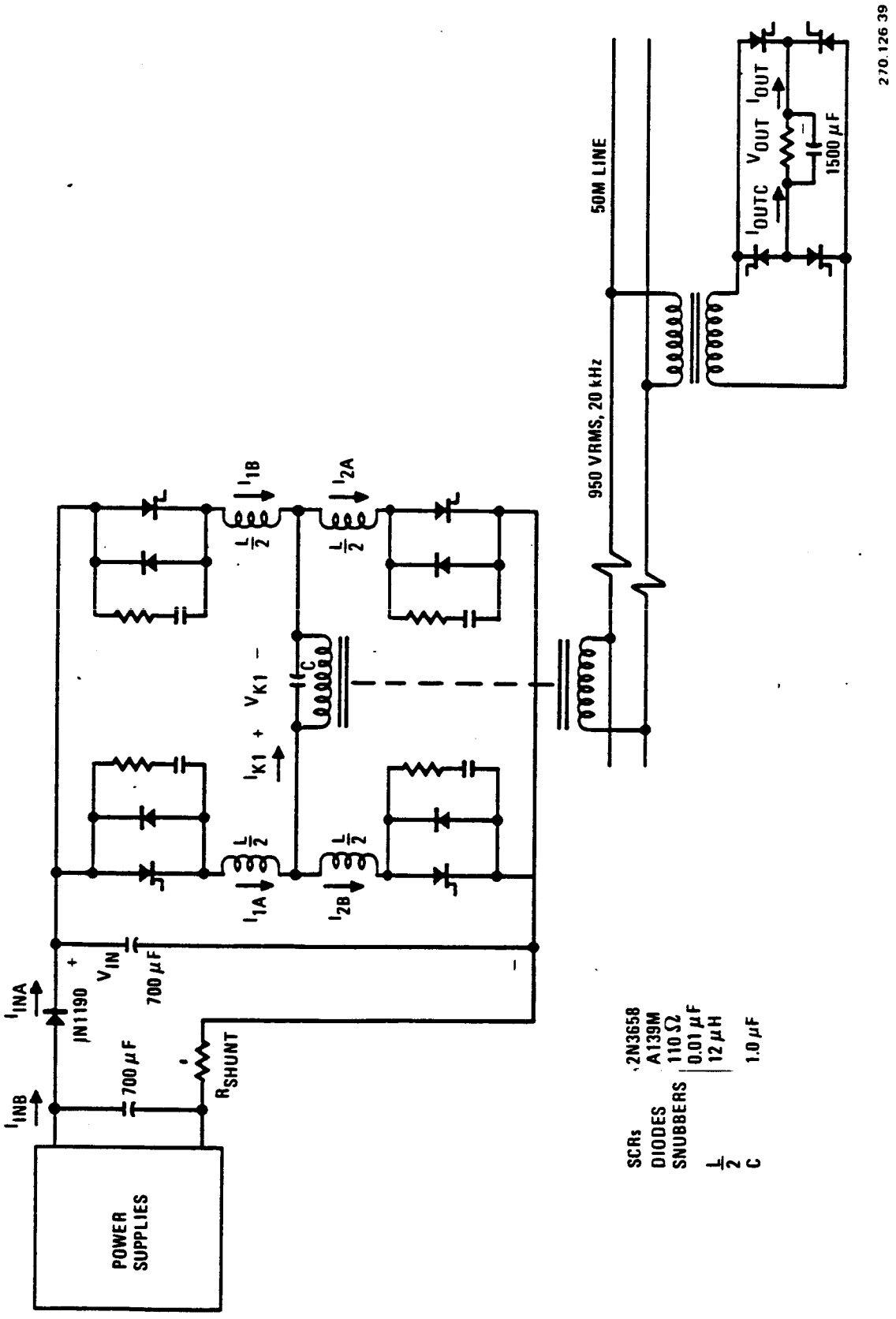


FIGURE 4.2-3. EFFICIENCY VERSUS LOAD POWER

FIGURE 4.2-4. DRIVER-TRANSMISSION LINE - DC RECEIVER SCHEMATIC



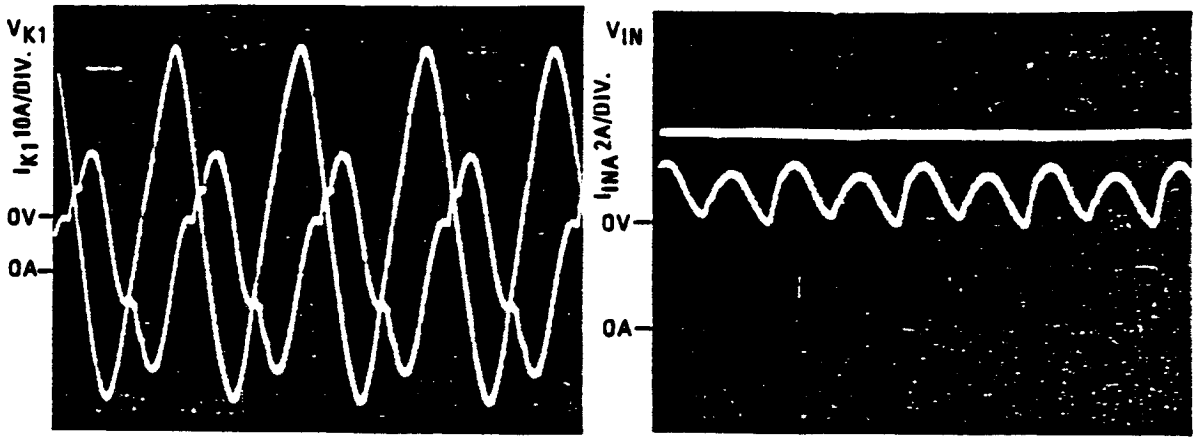


FIGURE 4.2-5. INVERTER PARAMETERS WITH 410W DC RECEIVER LOAD

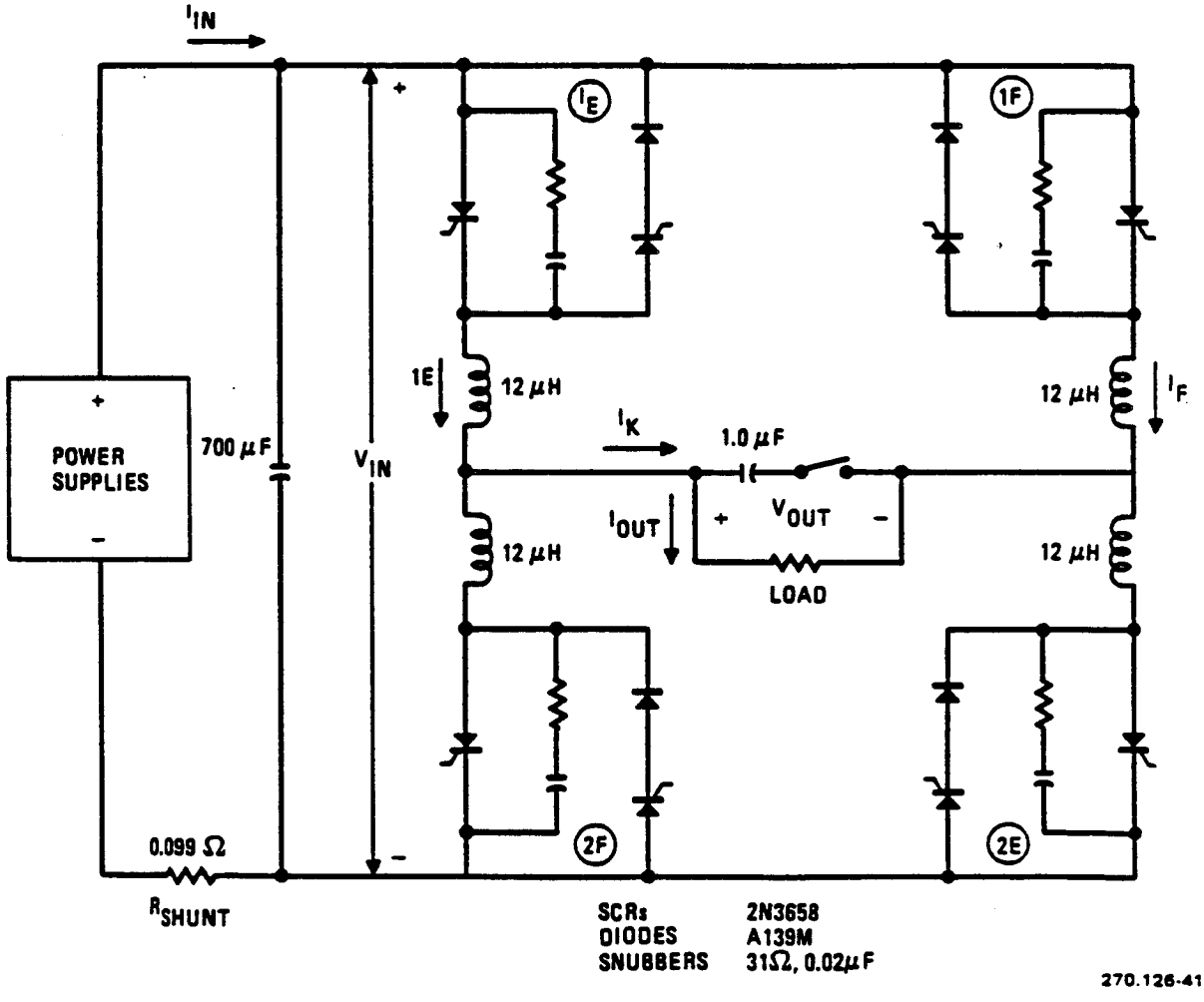


FIGURE 4.2-6. BIDIRECTIONAL MODULE SCHEMATIC

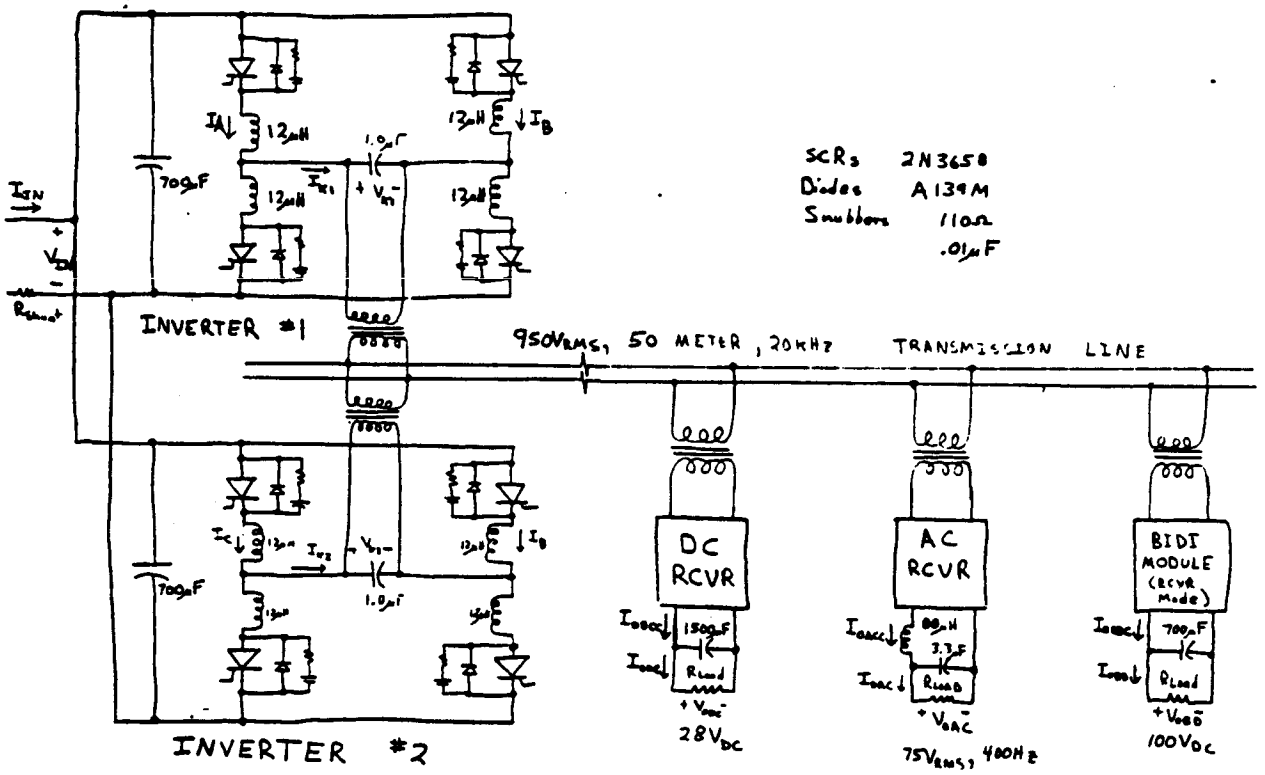


FIGURE 4.2-7. DUAL DRIVER SYSTEM SCHEMATIC

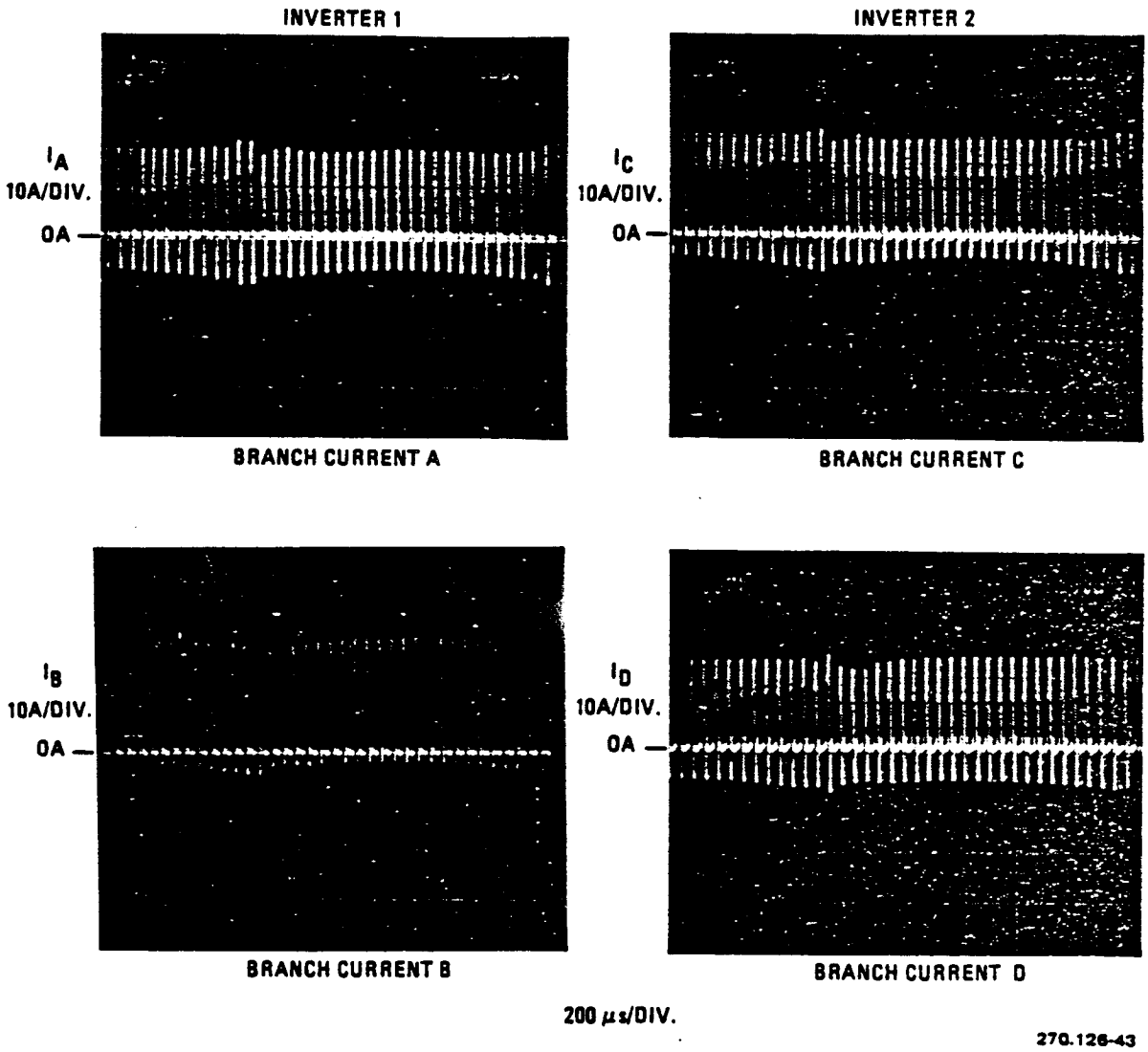


FIGURE 4.2-8. LEG CURRENTS OF THE DRIVERS

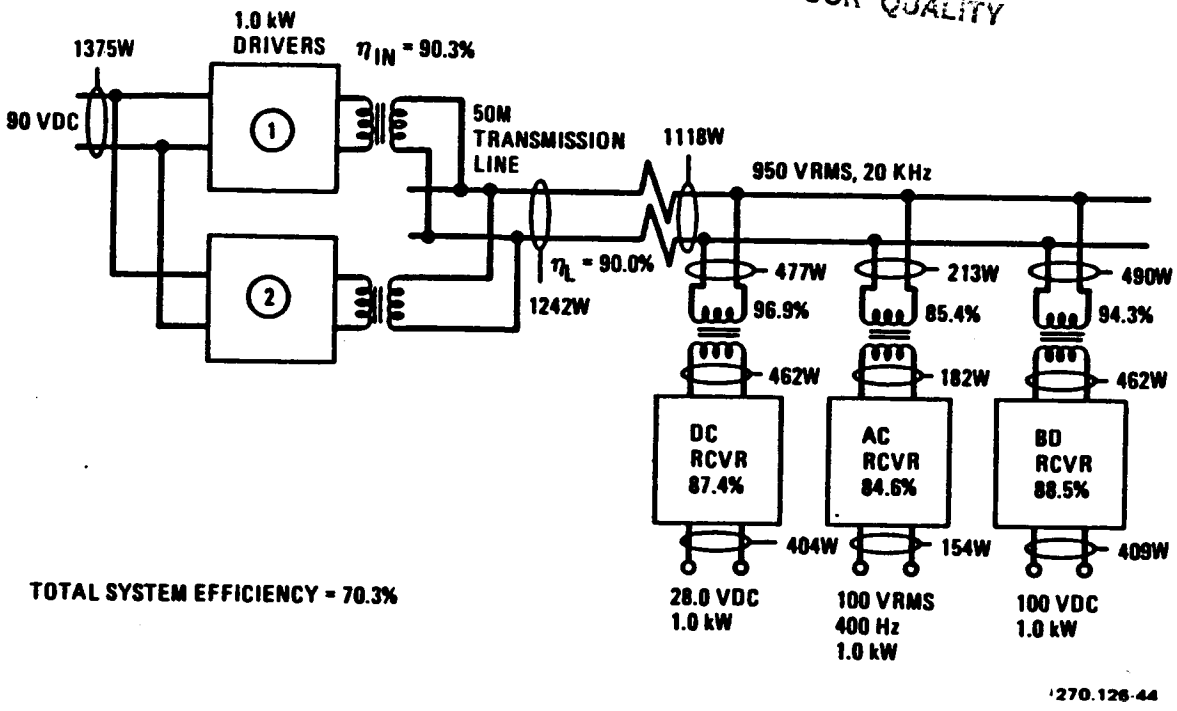
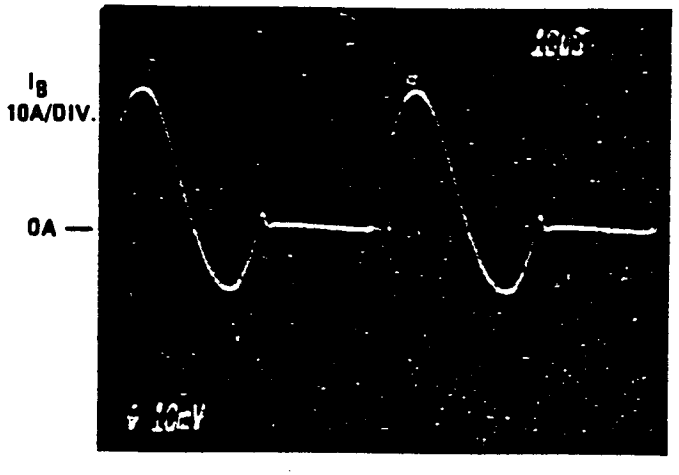


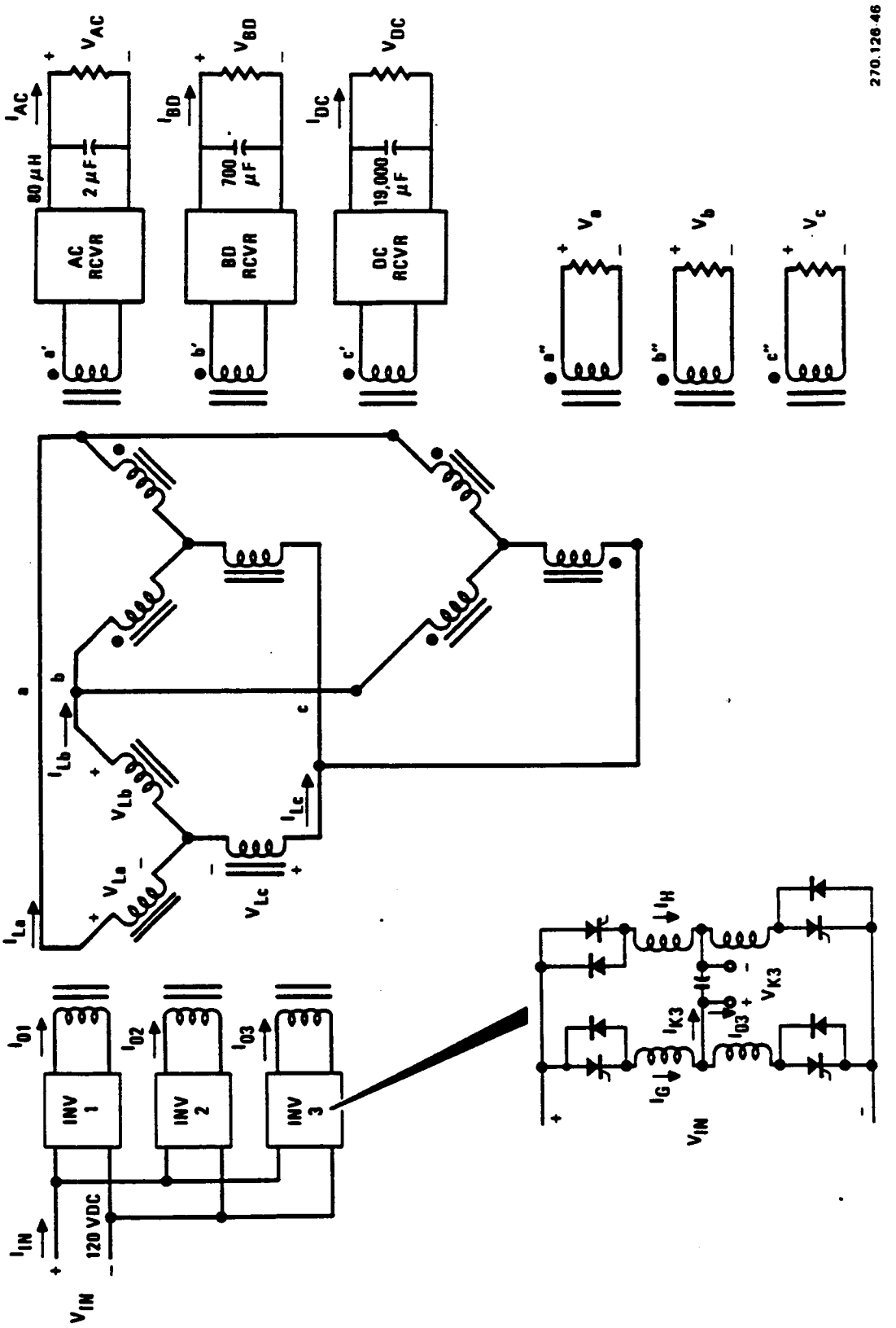
FIGURE 4.2-9. POINT-BY-POINT EFFICIENCY MEASUREMENTS ON THE SINGLE-PHASE SYSTEM BREADBOARD



270.126-45

FIGURE 4.2-10. INVERTER LEG CURRENT

FIGURE 4.2-11. 5.0 KW, THREE-PHASE SYSTEM SCHEMATIC



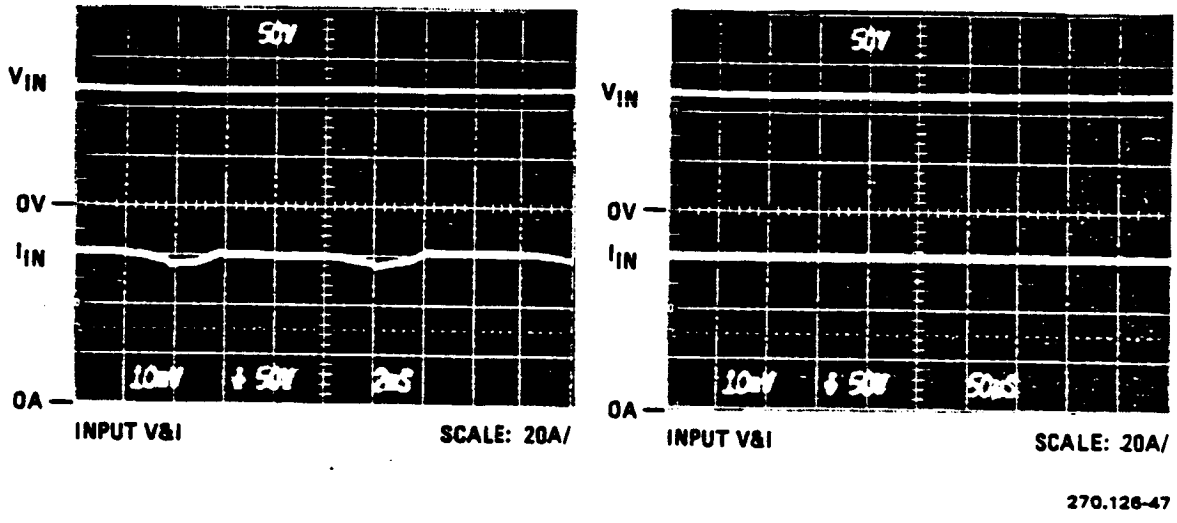


FIGURE 4.2-12. SYSTEM INPUT VOLTAGE AND CURRENT

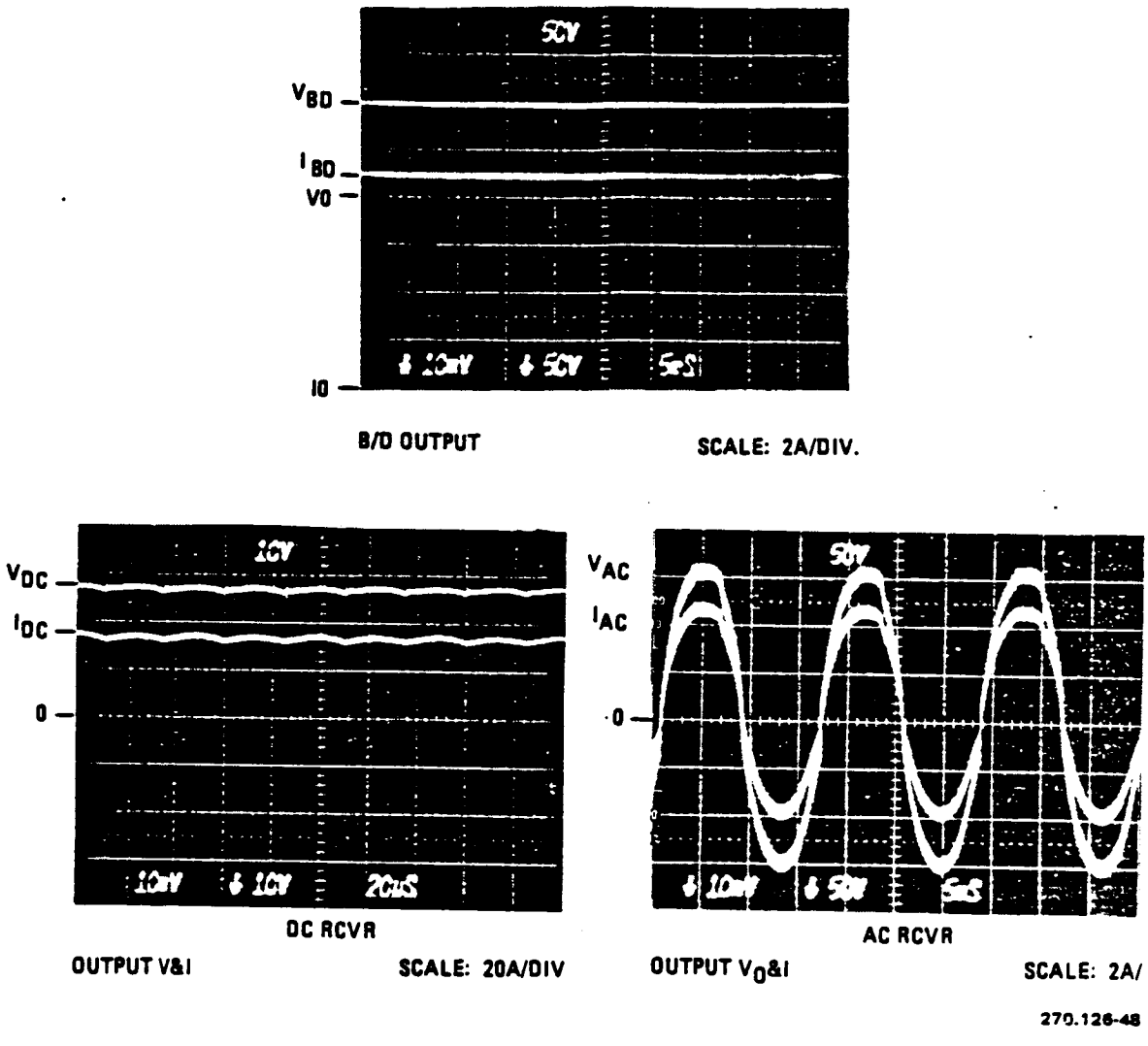


FIGURE 4.2-13. OUTPUT WAVEFORMS OF THE THREE RECEIVER MODULES

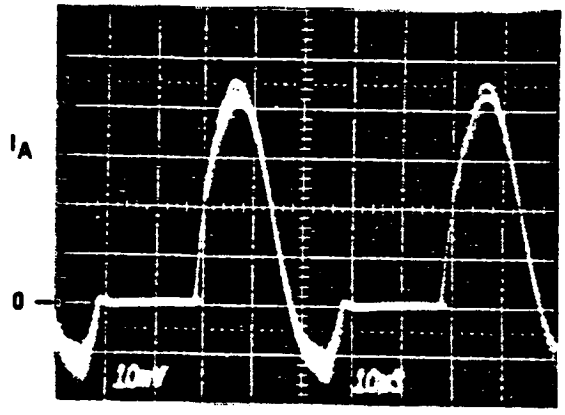


FIGURE 4.2-14. INVERTER 1 LEG CURRENT WITH 1,520W LOAD

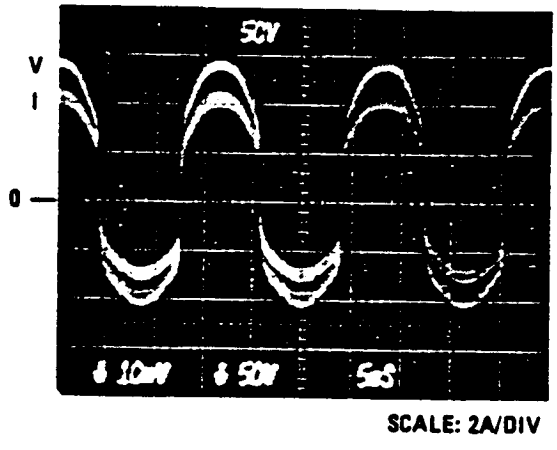


FIGURE 4.2-15. UNMODIFIED VARIABLE-FREQUENCY, VARIABLE-VOLTAGE AC RECEIVER MODULE OUTPUT

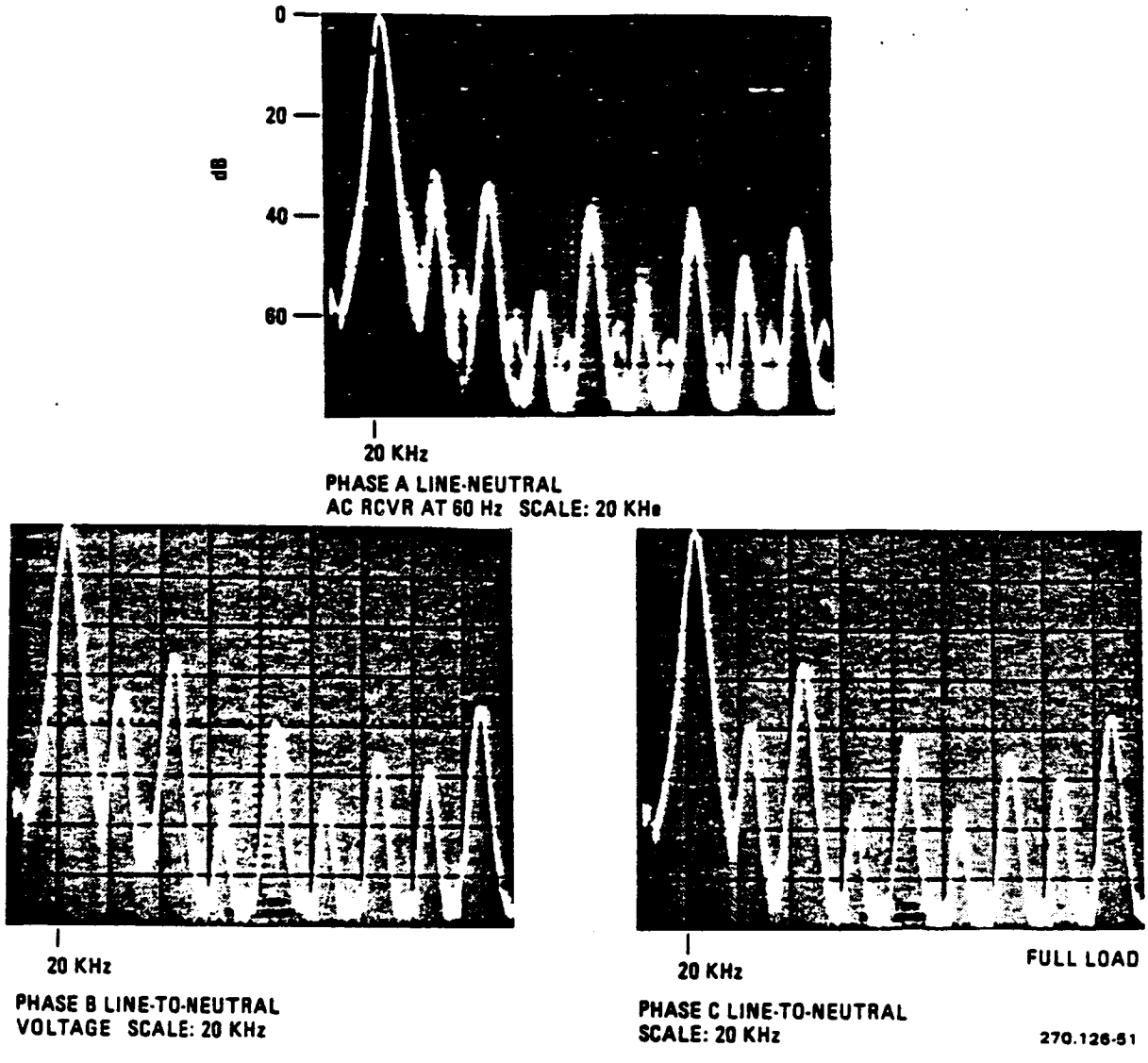


FIGURE 4.2-16. HARMONIC FREQUENCY COMPONENTS ON EACH PHASE OF THE BUS

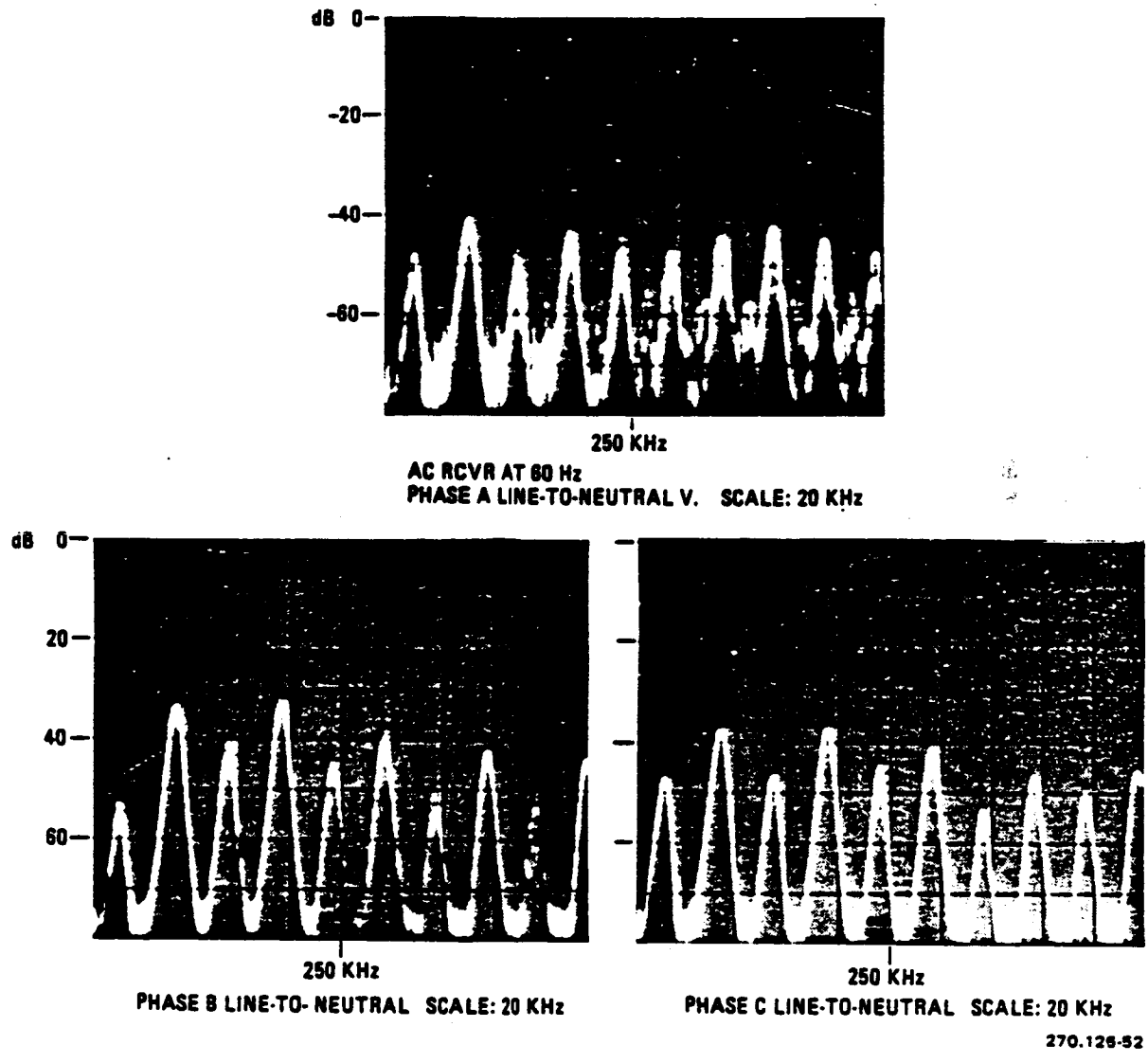


FIGURE 4.2-17. HIGH FREQUENCY COMPONENTS ON THE BUS

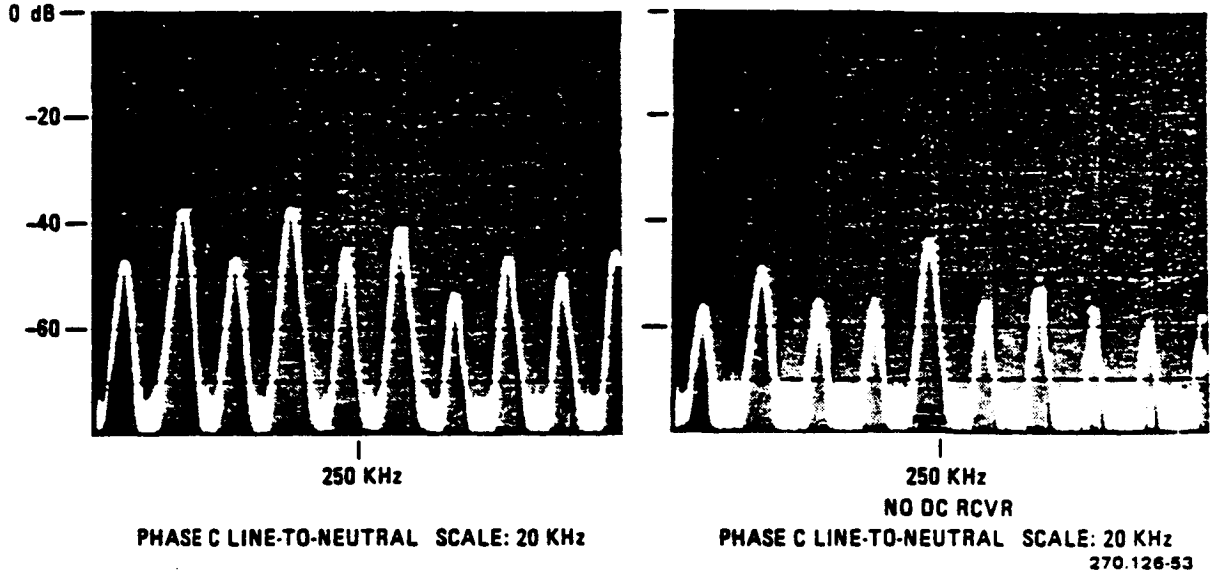


FIGURE 4.2-18. PHASE C FREQUENCY COMPONENTS WITH AND WITHOUT THE DC RECEIVER

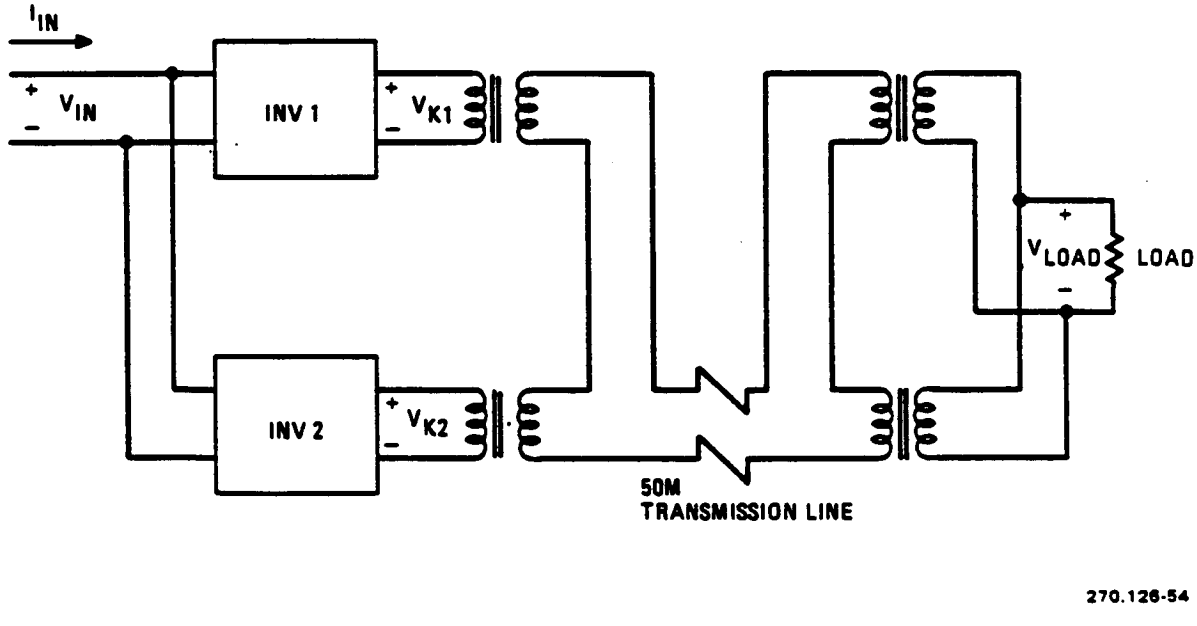


FIGURE 4.2-19. TEST CIRCUIT USED TO REGULATE THE INVERTERS

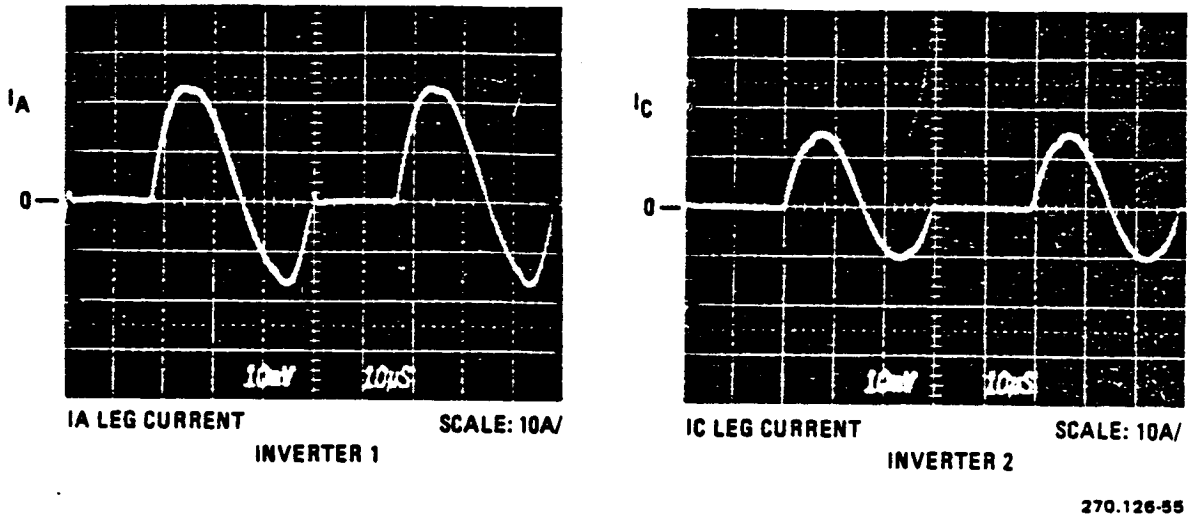


FIGURE 4.2-20. LEG CURRENTS OF THE REGULATED INVERTERS

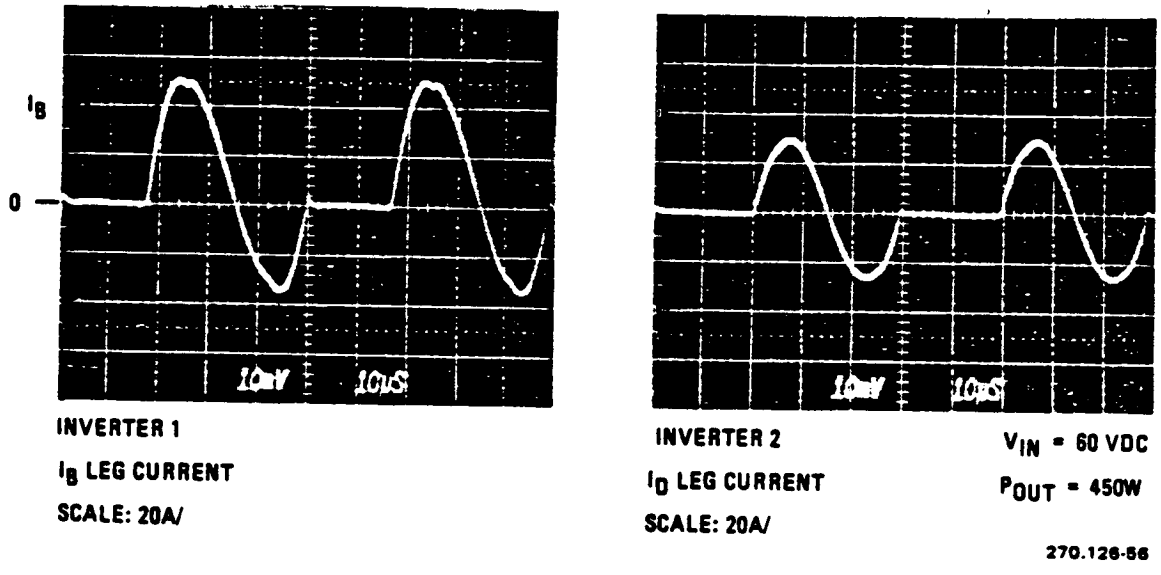


FIGURE 4.2-21. LEG CURRENTS IN THE REGULATED INVERTERS AT A HIGHER POWER LEVEL

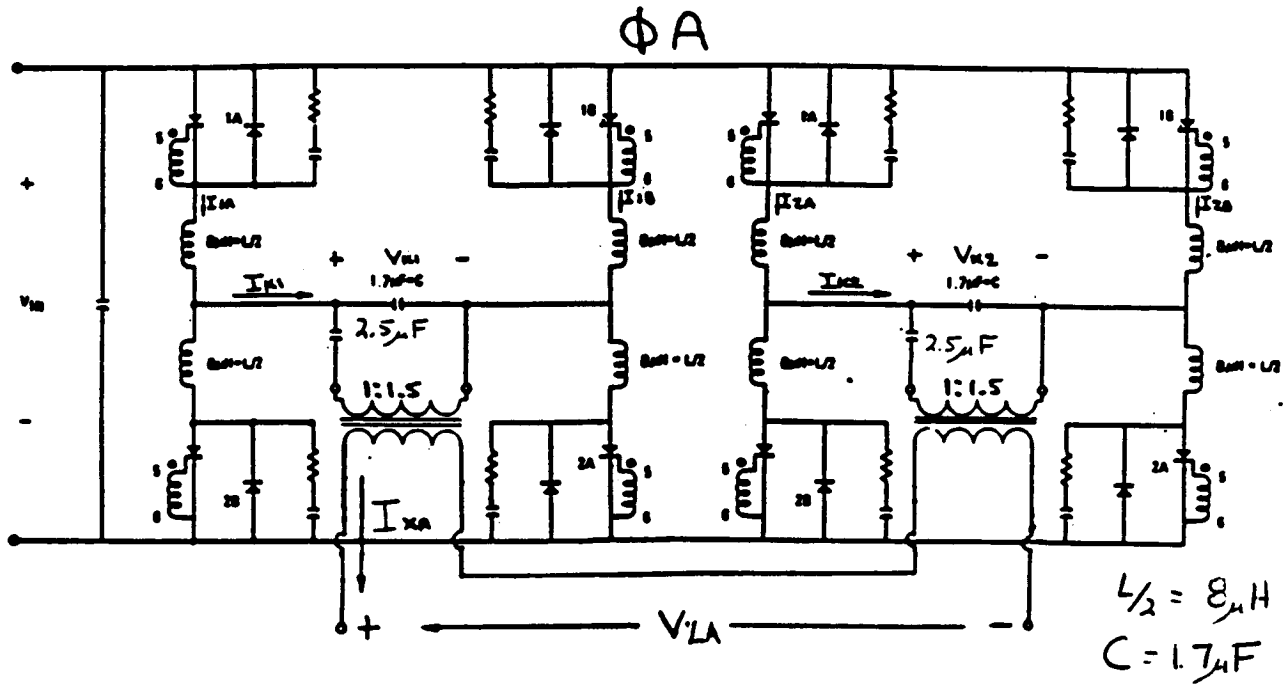


FIGURE 4.2-22 THE SCHEMATIC FOR UNCOMPENSATED PHASOR REGULATION

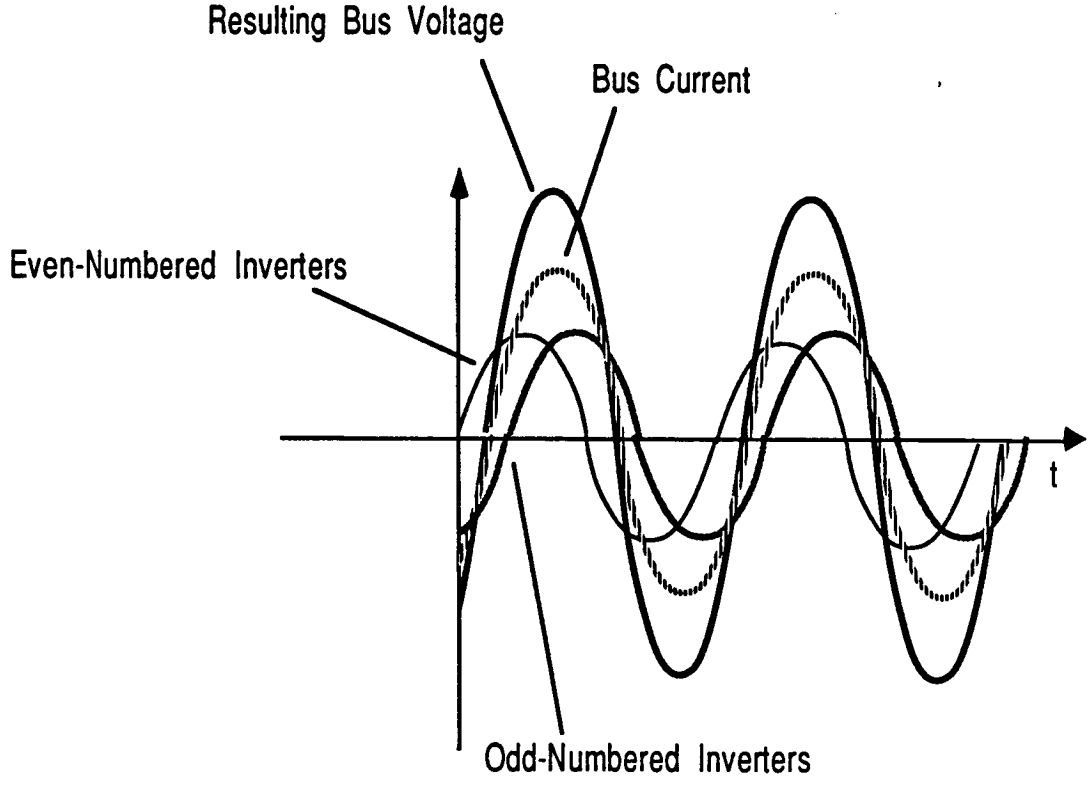
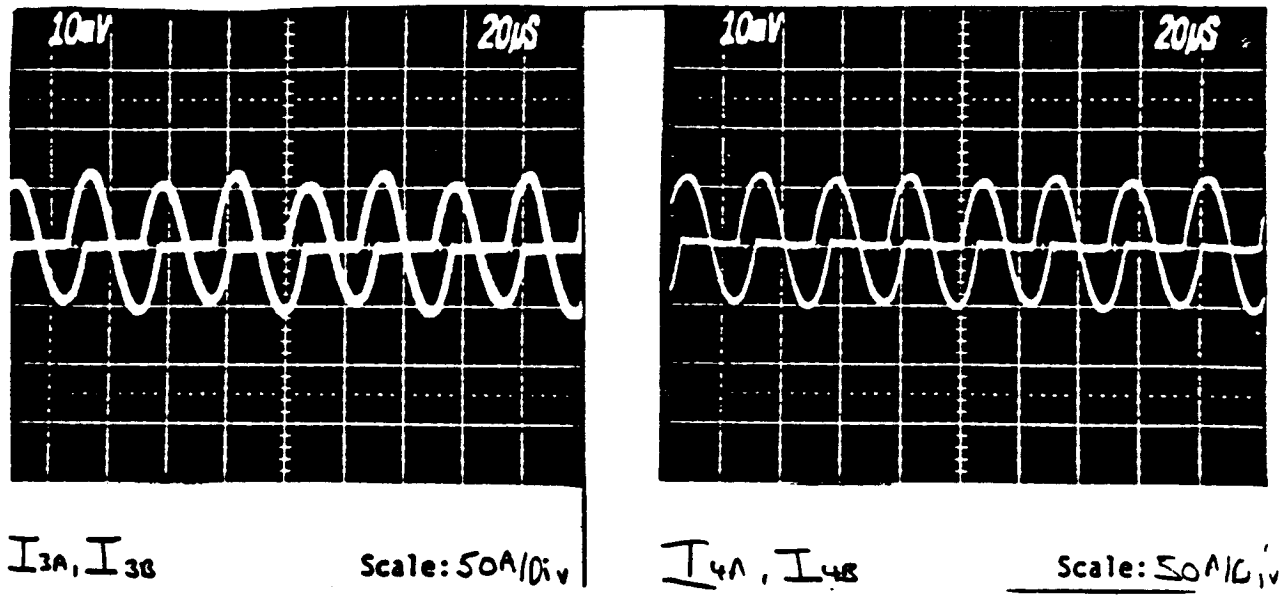


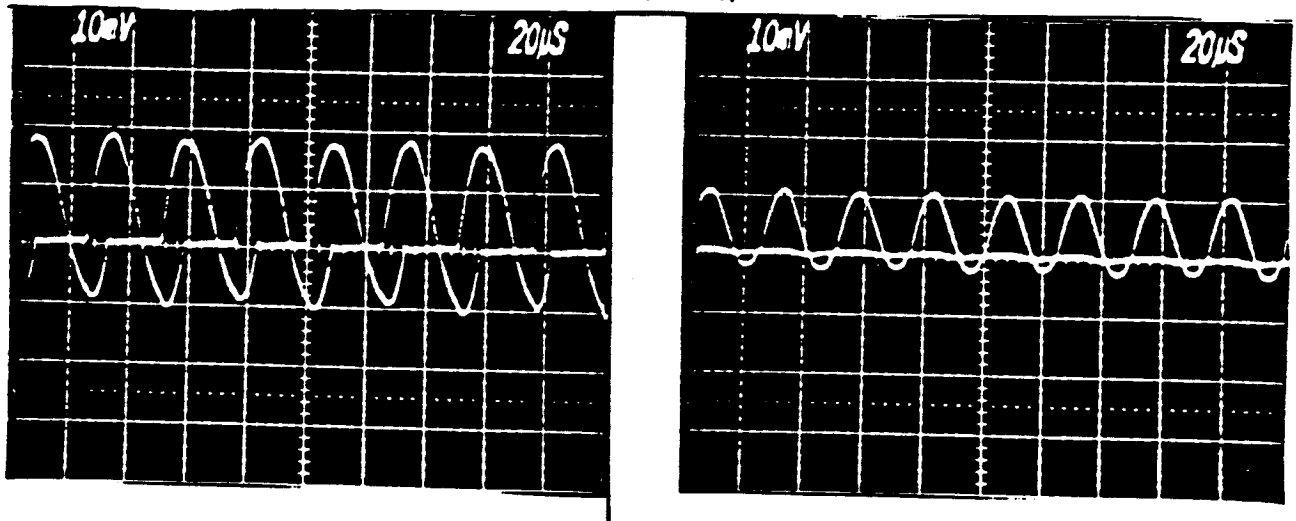
FIGURE 4.2-23. THE BUS VOLTAGE IS REGULATED BY VARYING THE PHASE ANGLE BETWEEN TWO INVERTERS AND SUMMING THE RESULT.

No Load



I_{3A}, I_{3B} Scale: 50A/Div I_{4A}, I_{4B} Scale: 50A/Div

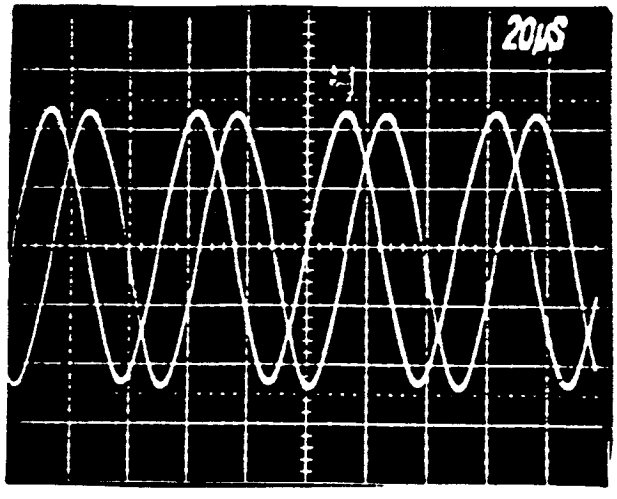
Full Load



I_{3A}, I_{3B} Scale: 50A/Div I_{4A}, I_{4B} Scale: 50A/Div

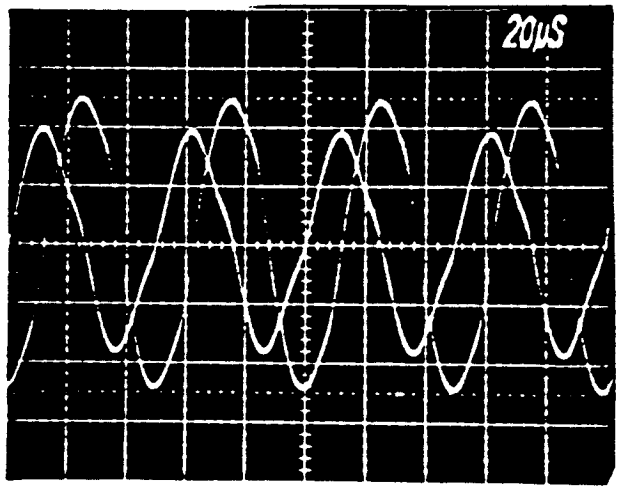
FIGURE 4.2-24. INVERTER LEG CURRENTS FOR THE UNCOMPENSATED CASE.

No Load



V_{K3}, V_{K4} Scale: Uncal V

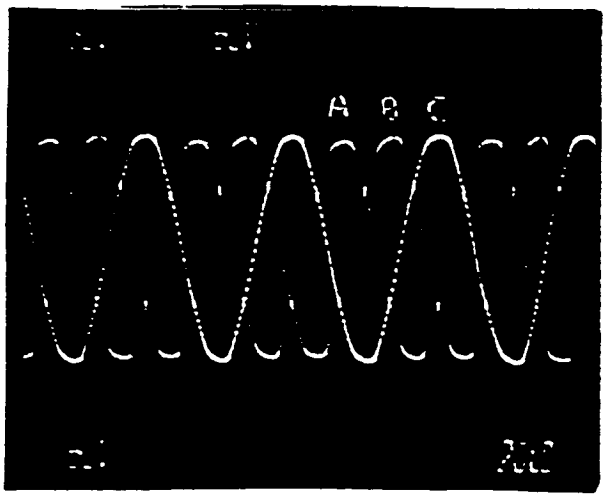
Full Load



V_{K3}, V_{K4} Scale:

FIGURE 4.2-25. THE PHASE SHIFT BETWEEN THE INVERTER OUTPUT VOLTAGES FOR THE UNCOMPENSATED CASE.

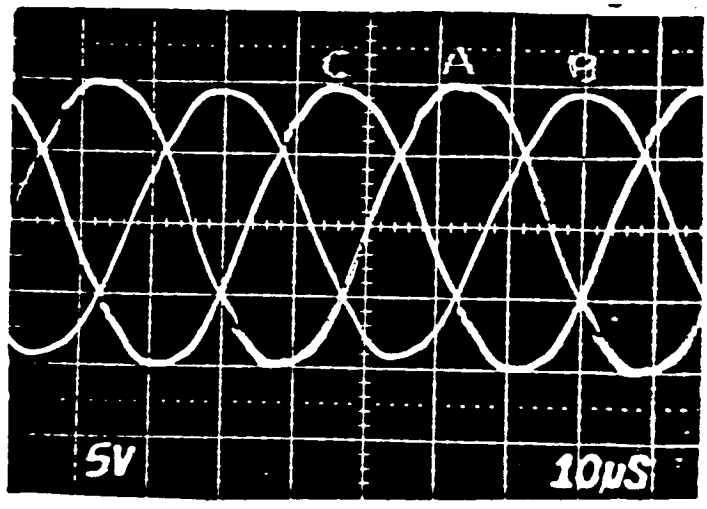
No Load



V_A, V_B, $+V_C$

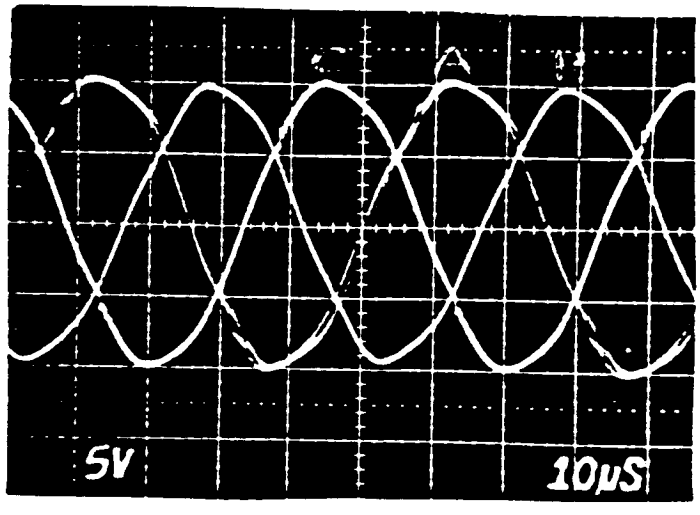
Scale: 320 V/Div

50% Load



Scale: 320 V/Div

Full Load



Scale: 320 V/Div

FIGURE 4.2-26. BUS VOLTAGES FOR THE UNCOMPENSATED CASE.

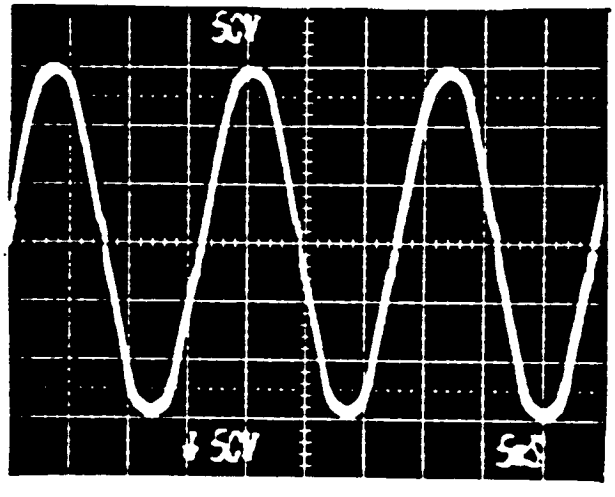


FIGURE 4.2-27. AC RECEIVER OUTPUT VOLTAGE FOR THE UNCOMPENSATED CASE.

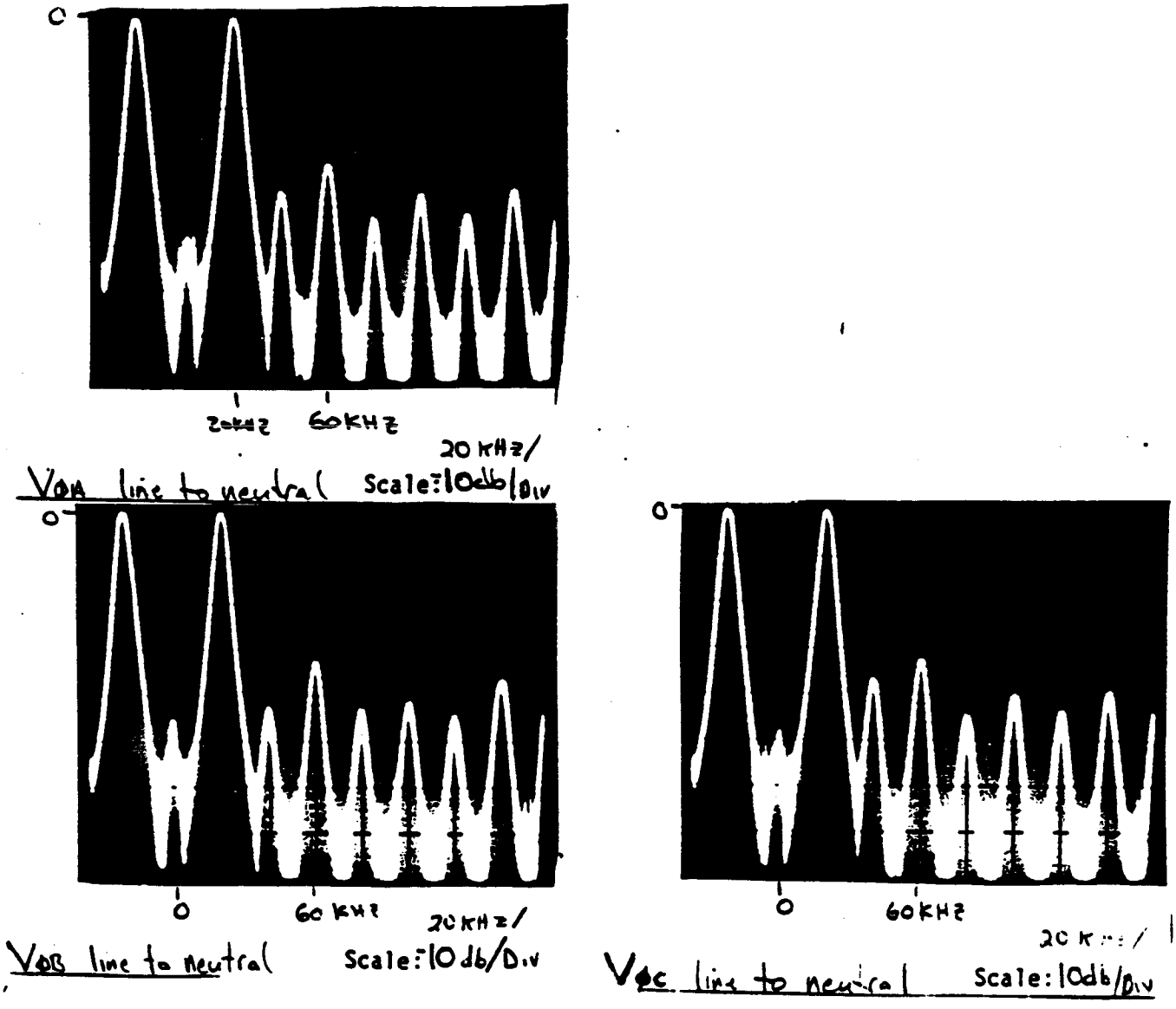


FIGURE 4.2-28. FREQUENCY COMPONENTS ON THE BUS FOR THE UNCOMPENSATED CASE AT NO LOAD.

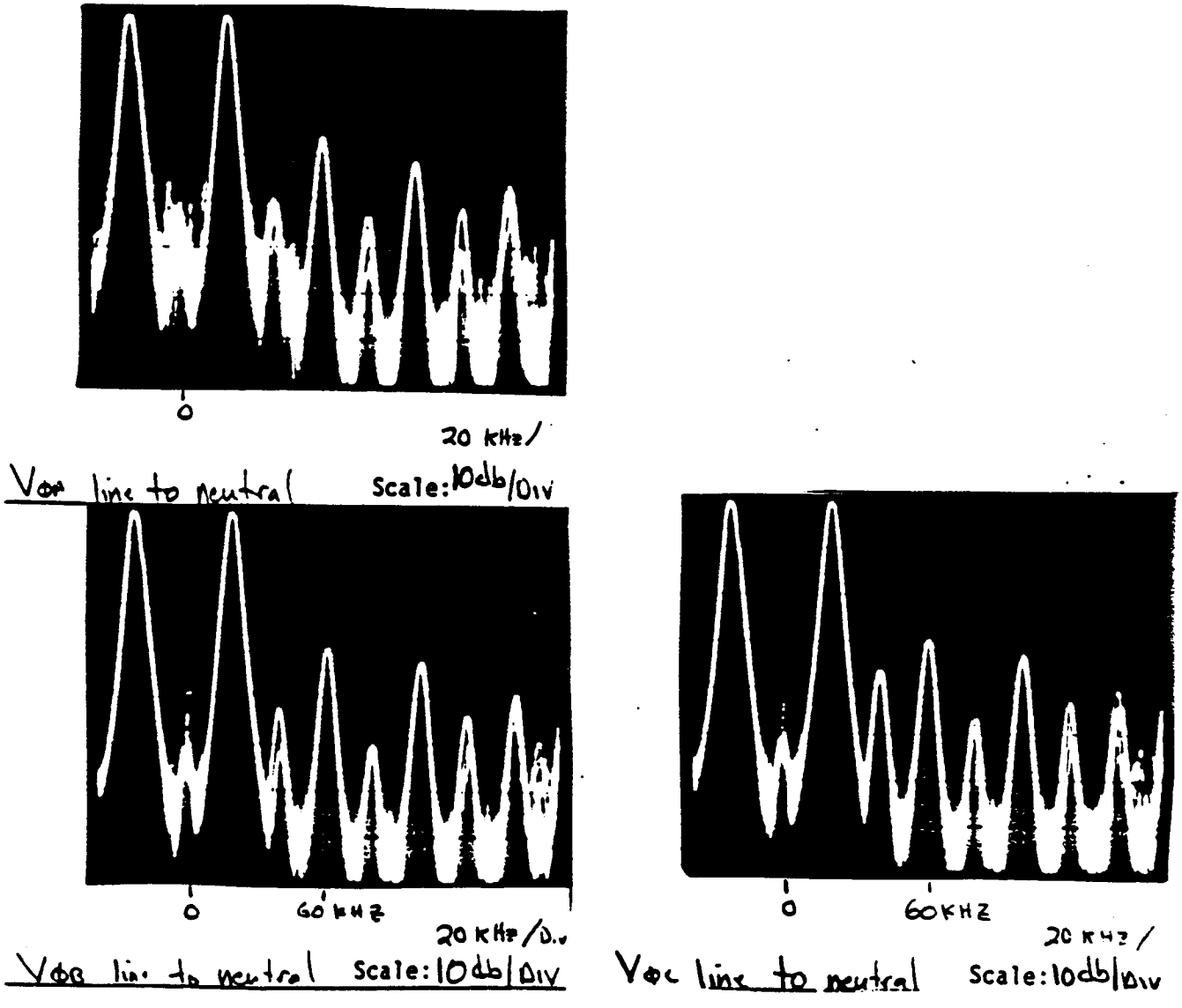


FIGURE 4.2-29. FREQUENCY COMPONENTS ON THE BUS FOR THE UNCOMPENSATED CASE AT FULL LOAD.

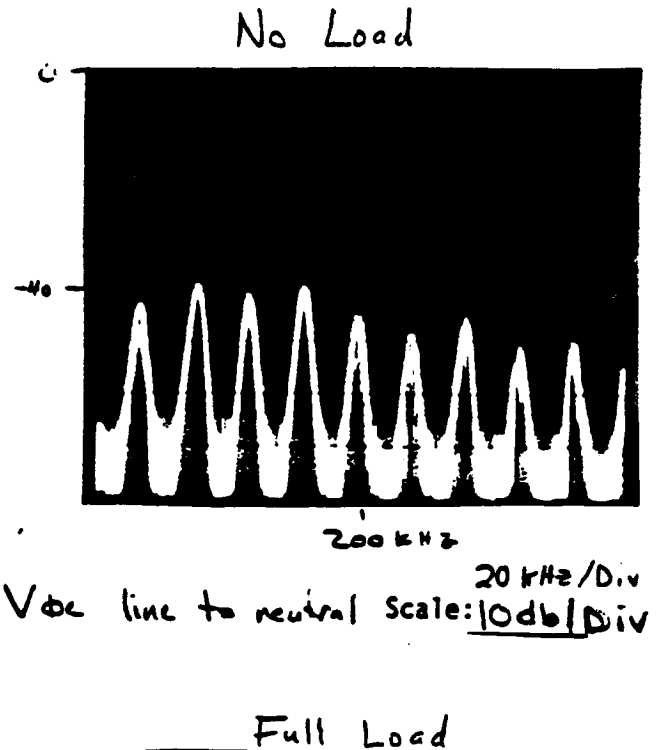


FIGURE 4.2-30. HIGH FREQUENCY COMPONENTS ON THE BUS FOR THE UNCOMPENSATED CASE.

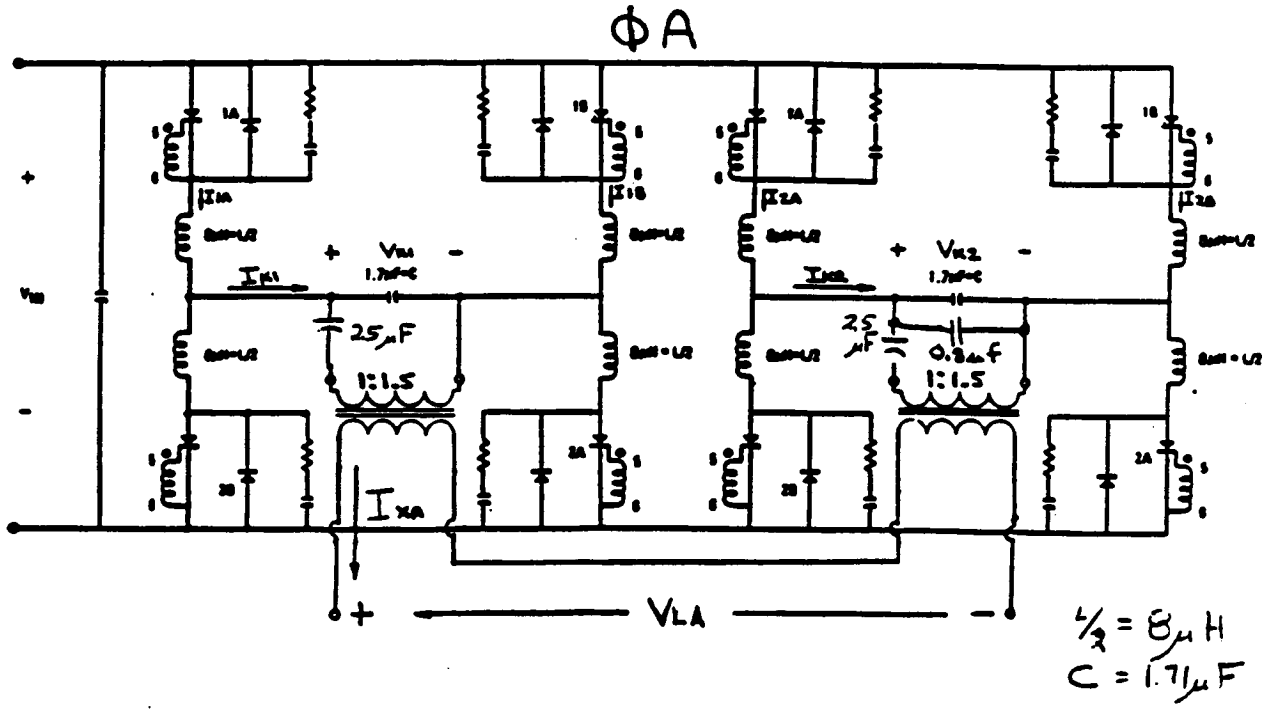


FIGURE 4.2-31. SCHEMATIC FOR CAPACITIVE COMPENSATION PHASOR REGULATION.

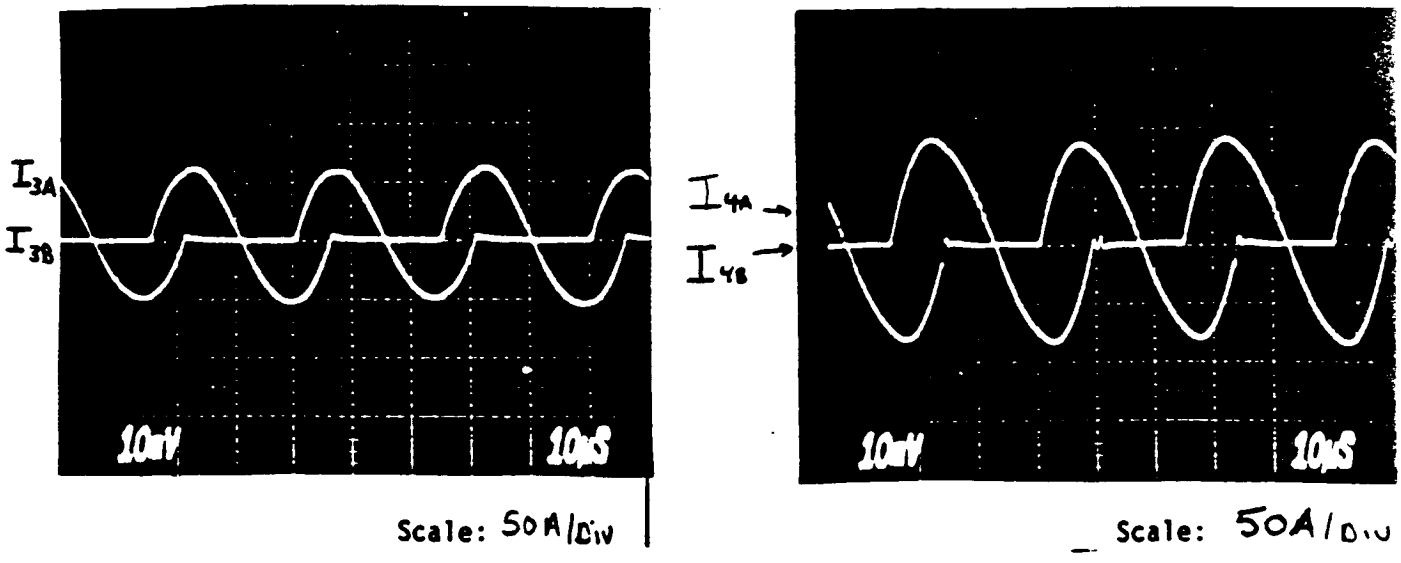


FIGURE 4.2-32. INVERTER LEG CURRENTS FOR THE CAPACITIVE COMPENSATION CASE AT NO LOAD.

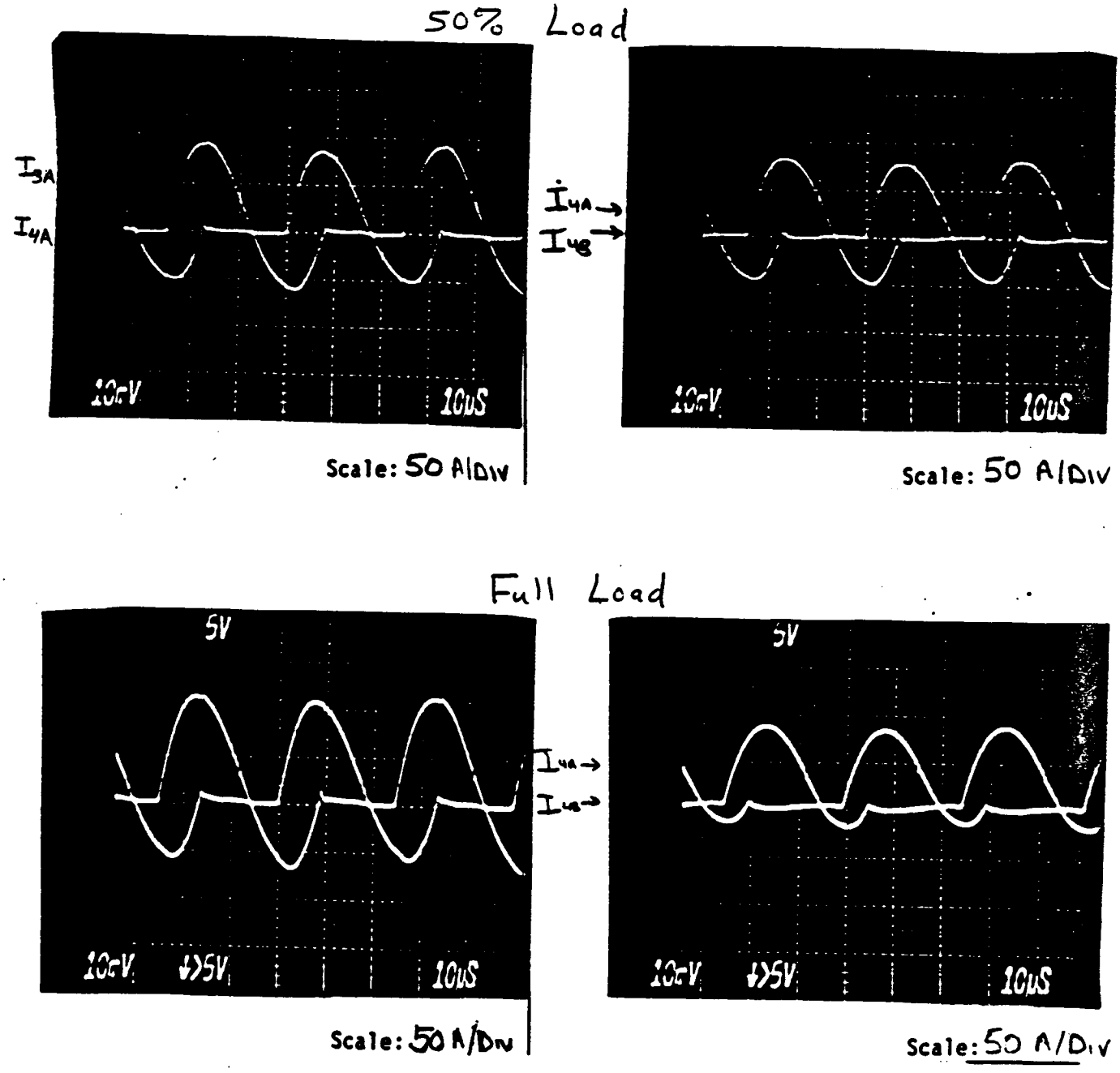
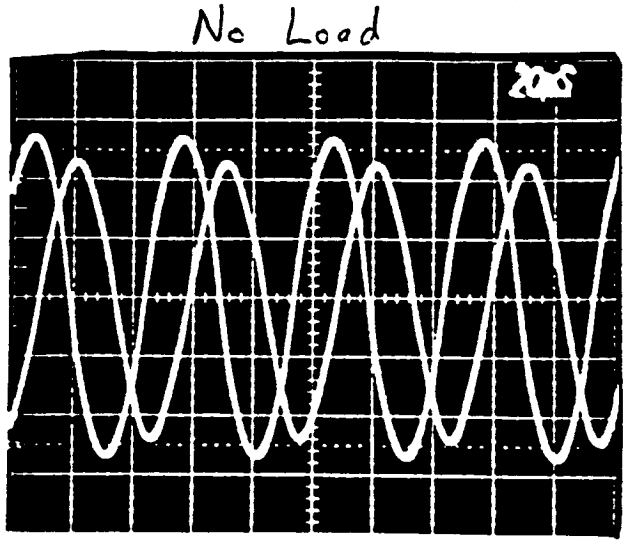
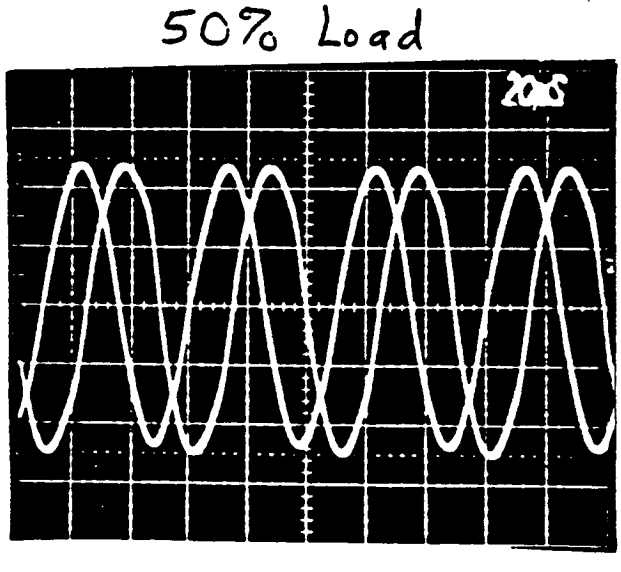


FIGURE 4.2-33. INVERTER LEG CURRENTS FOR THE CAPACITIVE COMPENSATION CASE AT 50% AND FULL LOAD.





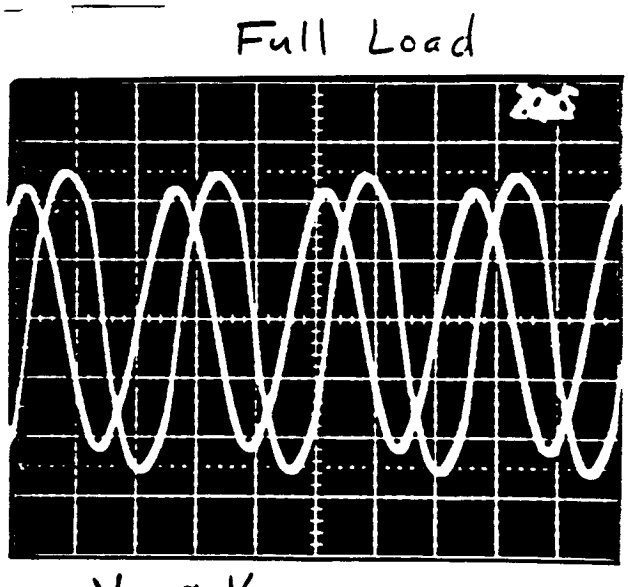
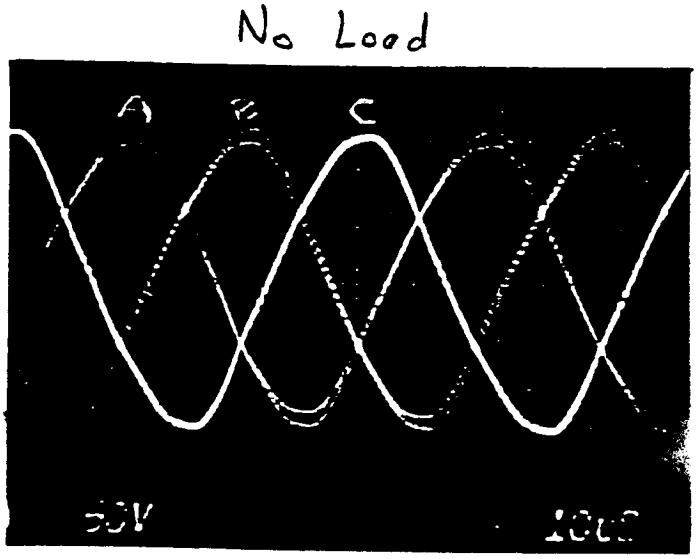
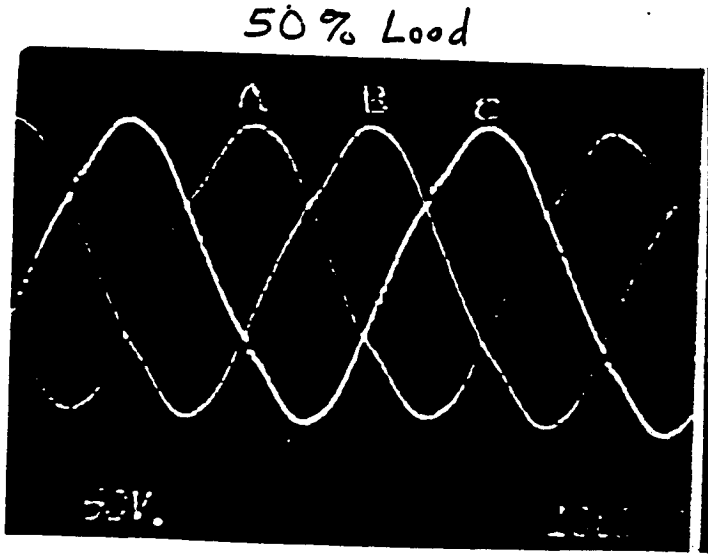


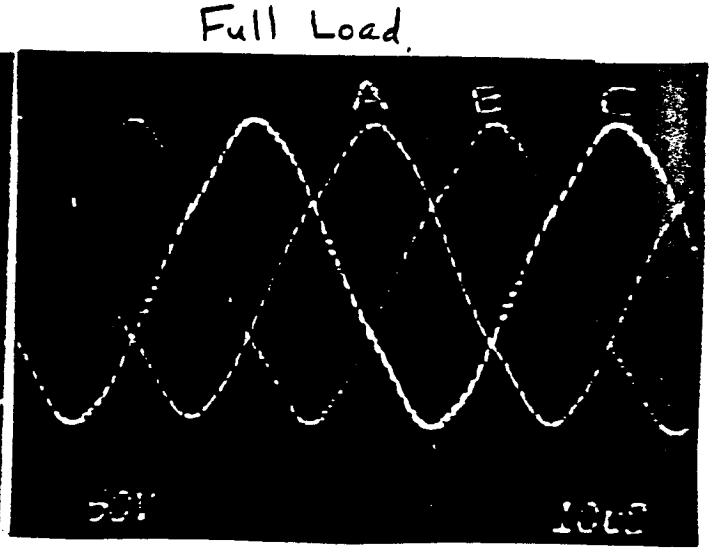
FIGURE 4.2-34. INVERTER OUTPUT VOLTAGES FOR THE CAPACITIVE COMPENSATION CASE.



Scale: 320 V/Div



Scale: 320 V/Div



Scale: 320 V/Div

FIGURE 4.2-35. BUS VOLTAGES FOR THE CAPACITIVE COMPENSATION CASE.

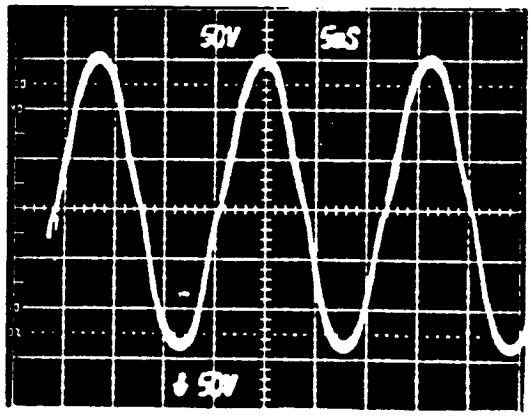


FIGURE 4.2-36. AC RECEIVER OUTPUT VOLTAGE FOR THE CAPACITIVE COMPENSATION CASE.

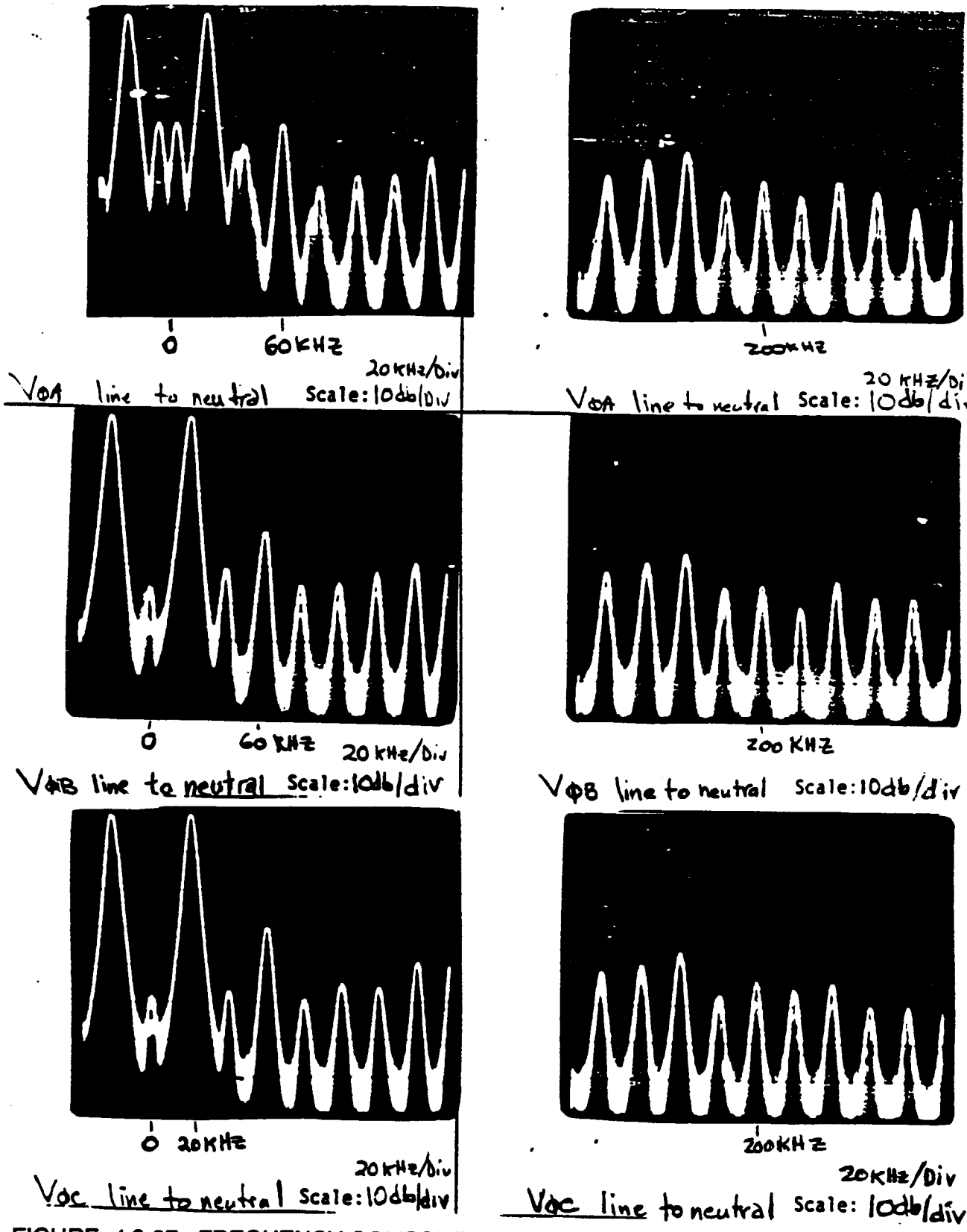
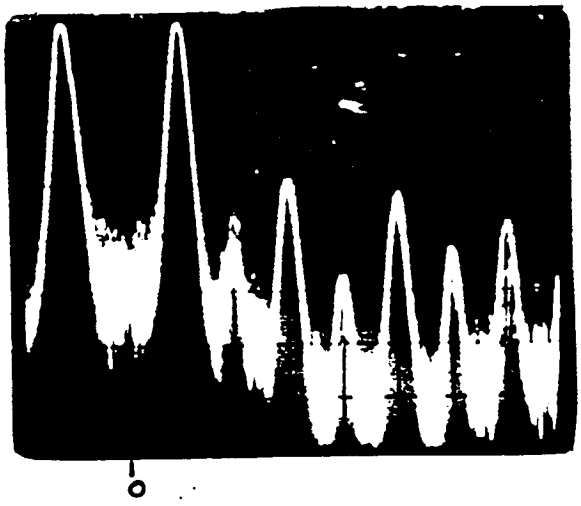
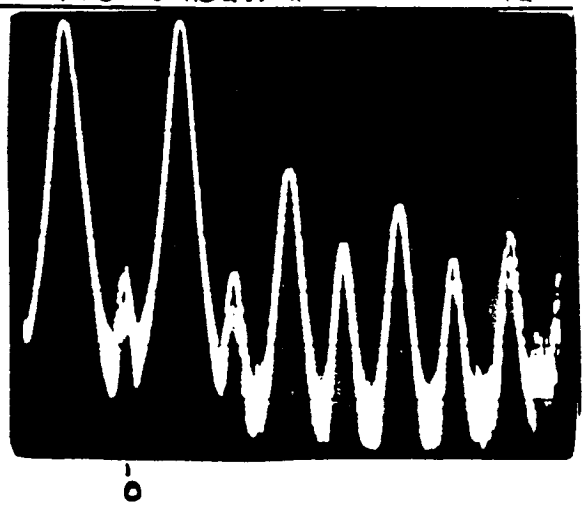


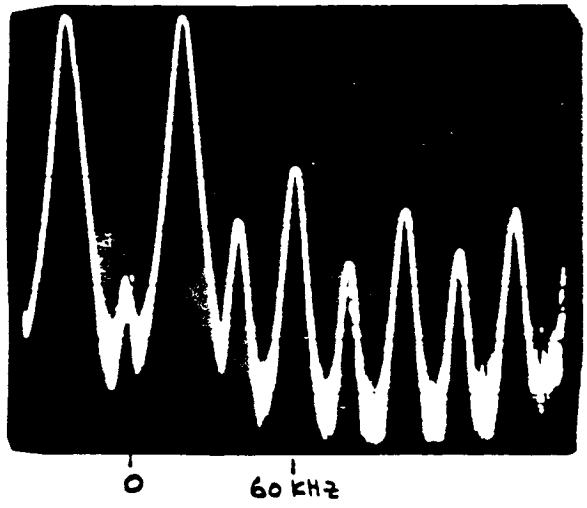
FIGURE 4.2-37. FREQUENCY COMPONENTS ON THE BUS FOR THE CAPACITIVE COMPENSATION CASE AT NO LOAD.



V_{oA} line to neutral Scale: 10 db/div

20 KHz/Div.

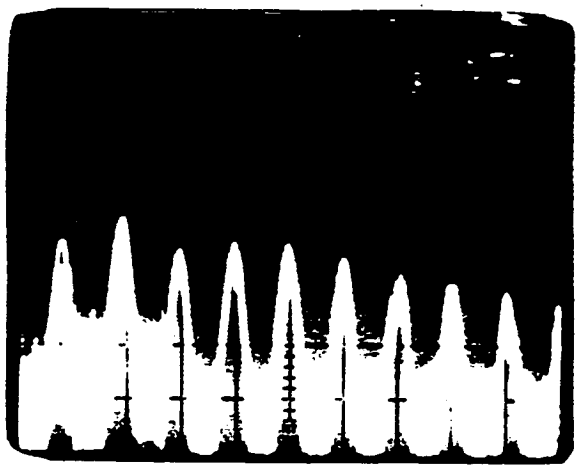




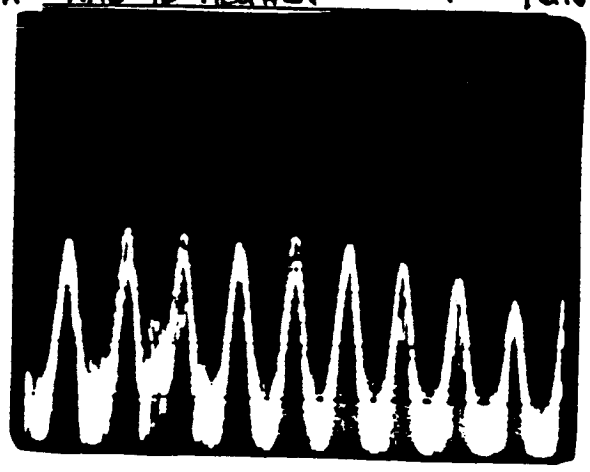
V_{oB} line to neutral Scale: 10 db/div

V_{oC} line to neutral Scale: 10db/div

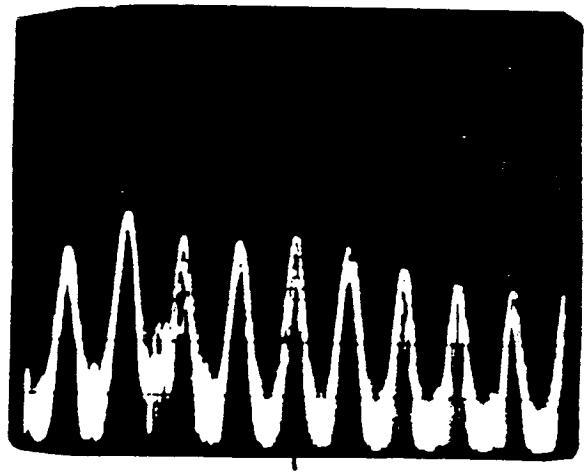
FIGURE 4.2-38. FREQUENCY COMPONENTS ON THE BUS FOR THE CAPACITIVE COMPENSATION CASE AT FULL LOAD.



$V_{\phi A}$ line to neutral Scale: 10 db/div



$V_{\phi B}$ line to neutral Scale: 10 db/div



$V_{\phi C}$ line to neutral Scale: 10 db/div

FIGURE 4.2-39. HIGH FREQUENCY COMPONENTS ON THE BUS FOR THE CAPACITIVE COMPENSATION CASE AT FULL LOAD.

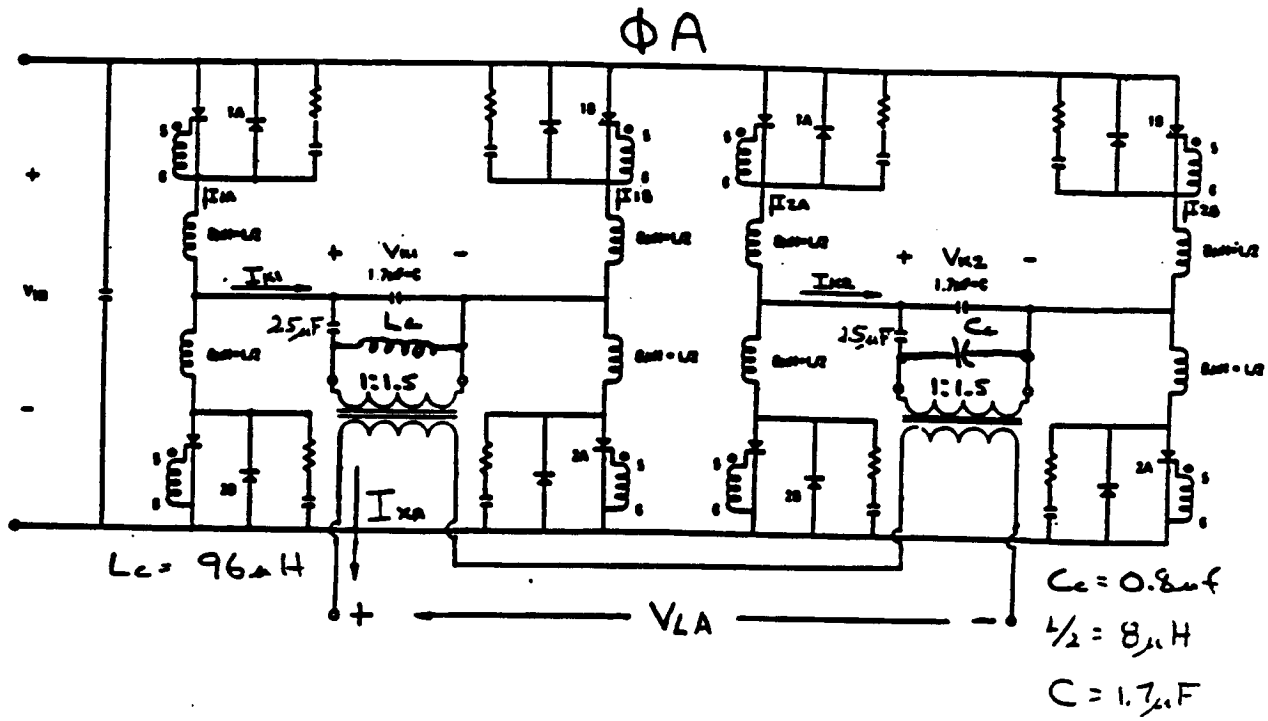


FIGURE 4.2-40. SCHEMATIC FOR INDUCTIVE AND CAPACITIVE COMPENSATION PHASOR REGULATION.

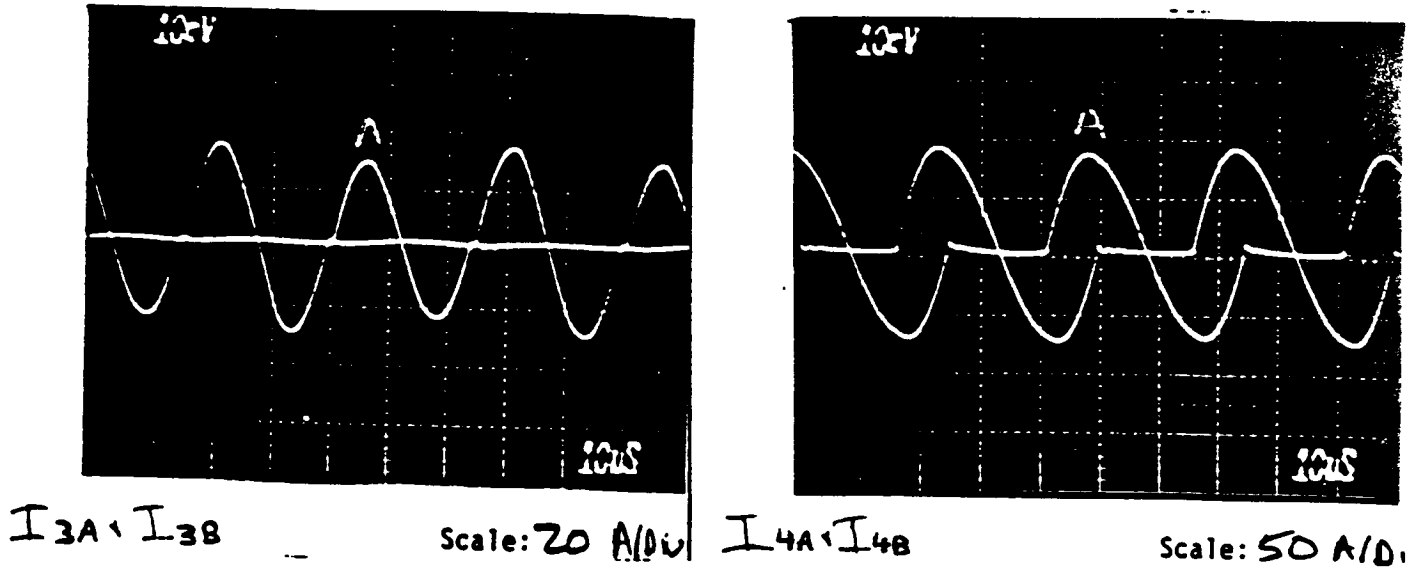
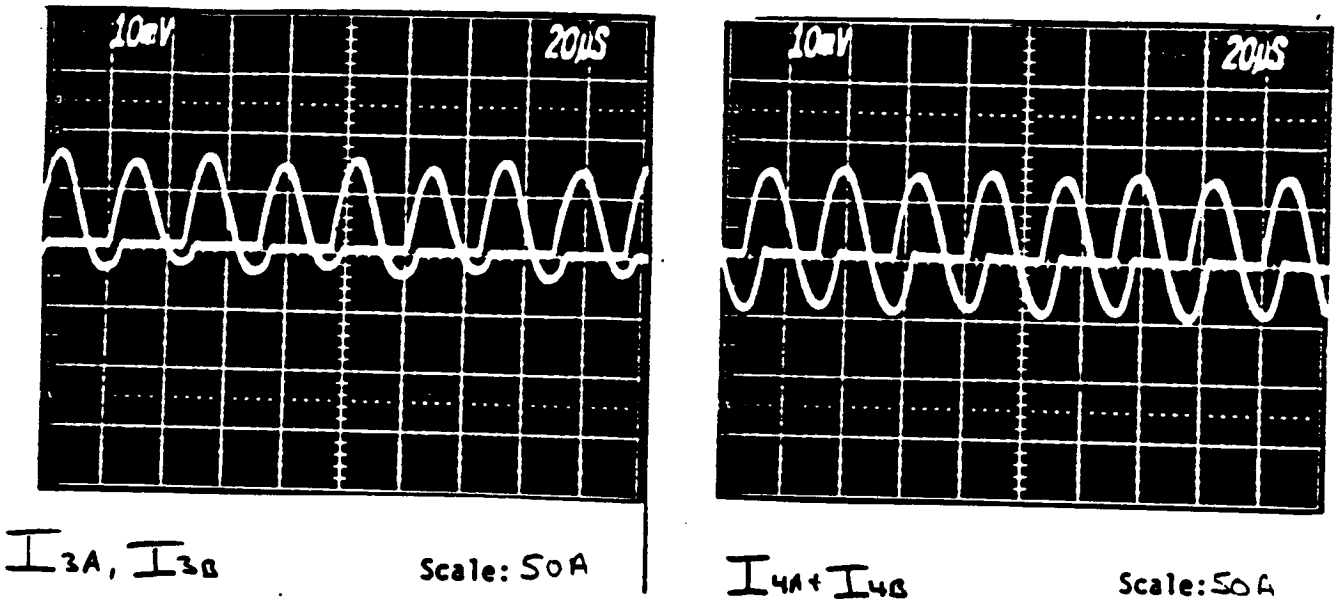


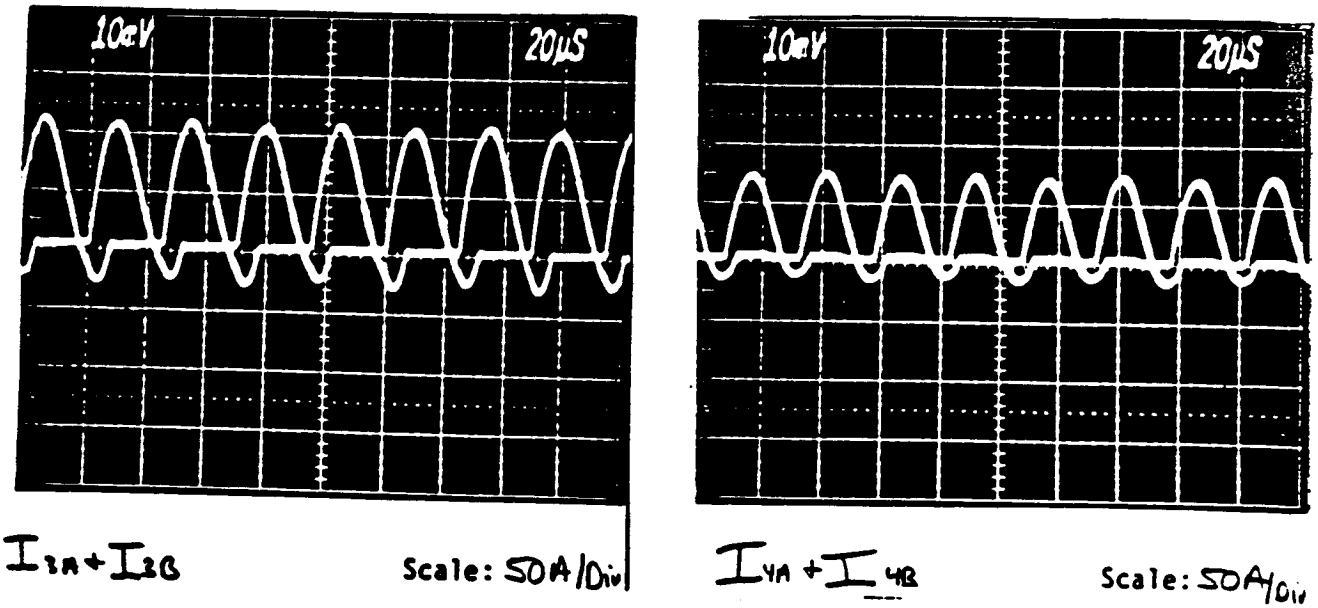
FIGURE 4.2-41. INVERTER LEG CURRENTS FOR THE INDUCTIVE AND CAPACITIVE COMPENSATION CASE AT NO LOAD.



I_{3A}, I_{3B} Scale: 50A

$I_{4A} + I_{4B}$ Scale: 50A

FIGURE 4.2-42. INVERTER LEG CURRENTS FOR THE INDUCTIVE AND CAPACITIVE COMPENSATION CASE AT 50% LOAD.



$I_{3A} + I_{3B}$ Scale: 50A/Div

$I_{4A} + I_{4B}$ Scale: 50A/Div

FIGURE 4.2-43. INVERTER LEG CURRENTS FOR THE INDUCTIVE AND CAPACITIVE COMPENSATION CASE AT FULL LOAD.

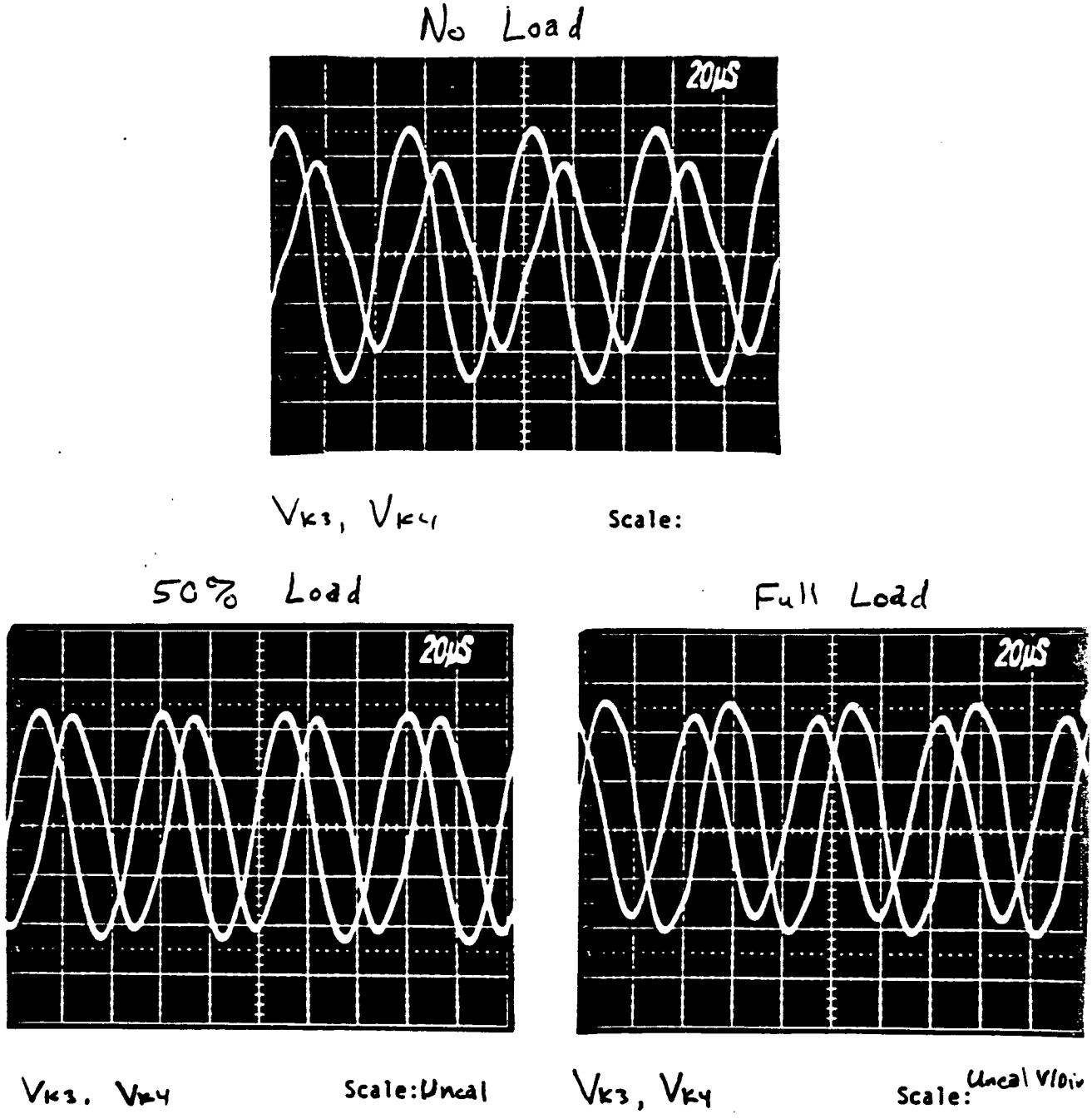
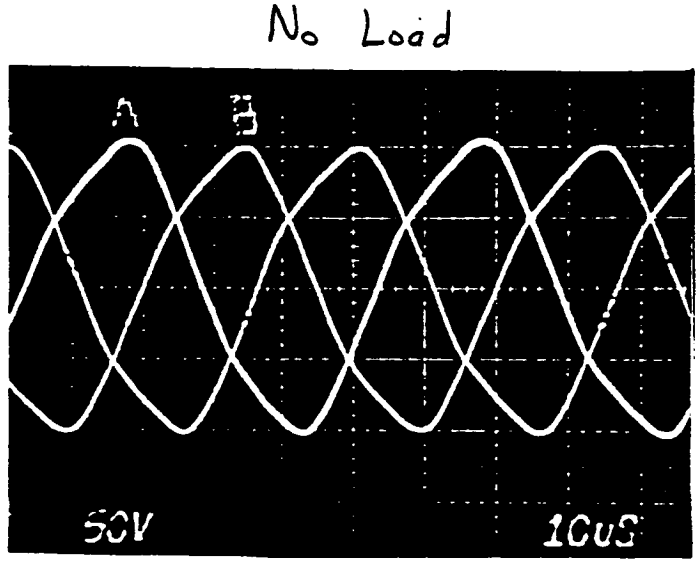


FIGURE 4.2-44. INVERTER OUTPUT VOLTAGES FOR THE INDUCTIVE AND CAPACITIVE COMPENSATION CASE.



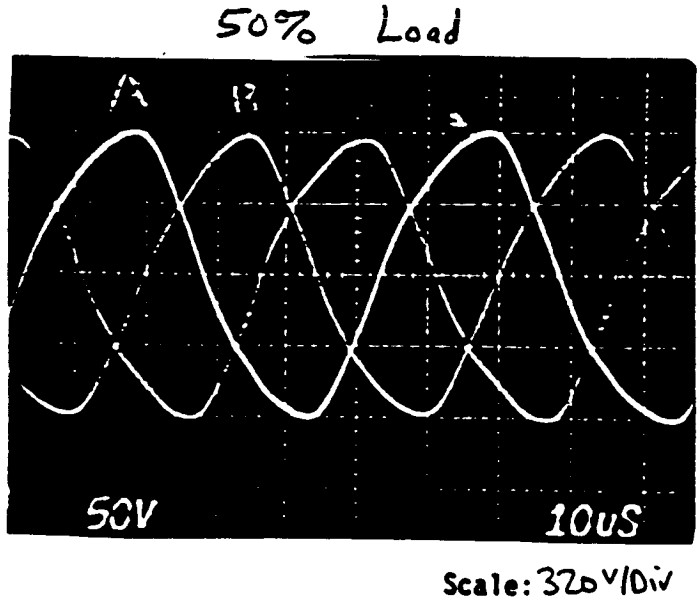


FIGURE 4.2-45. BUS VOLTAGES FOR THE INDUCTIVE AND CAPACITIVE COMPENSATION CASE AT NO LOAD AND 50% LOAD.

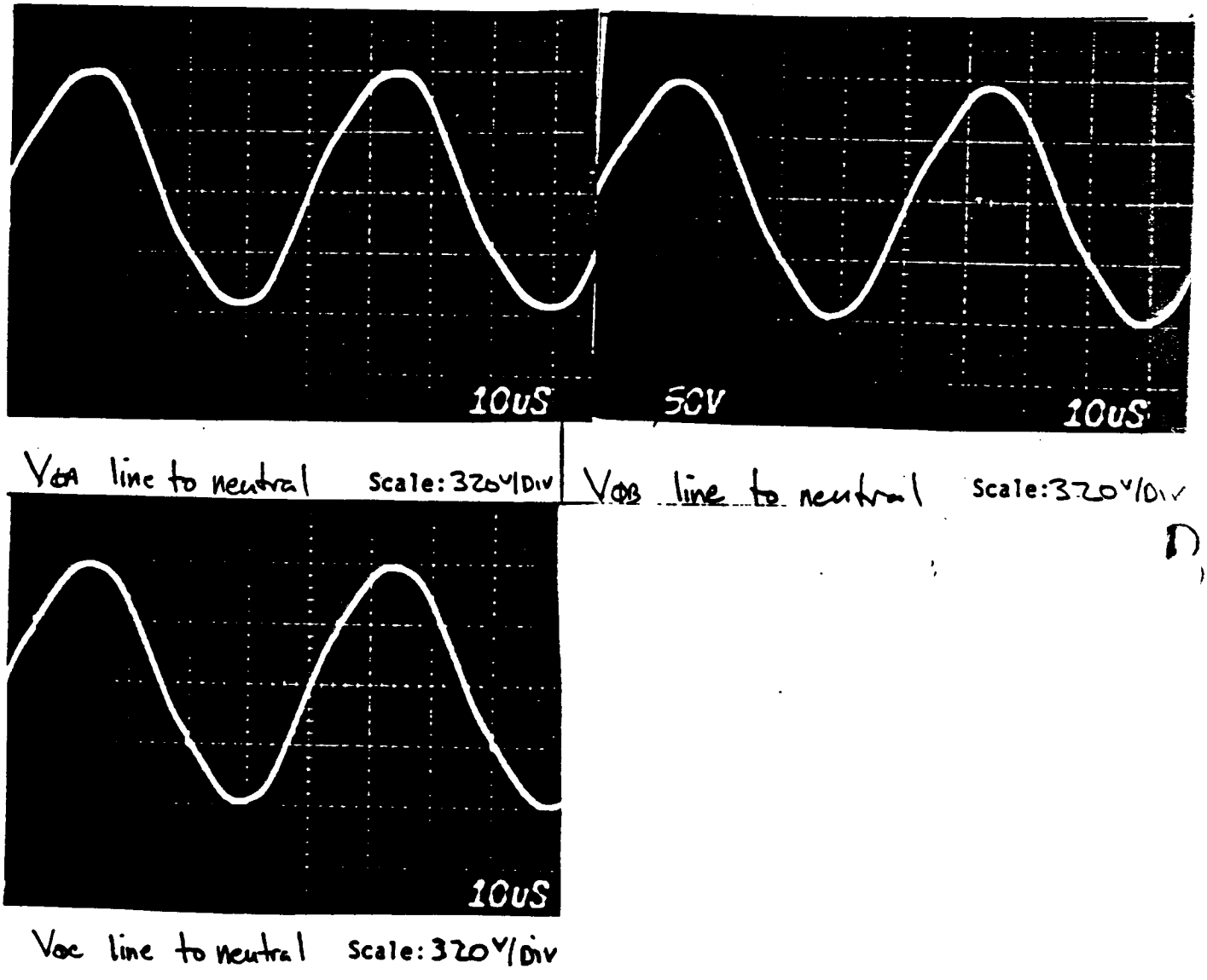
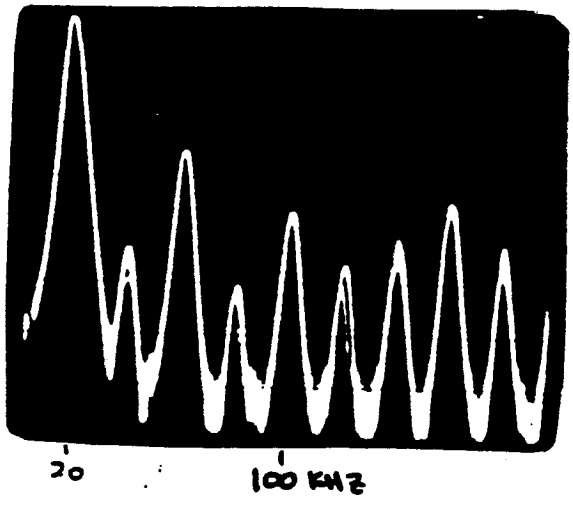
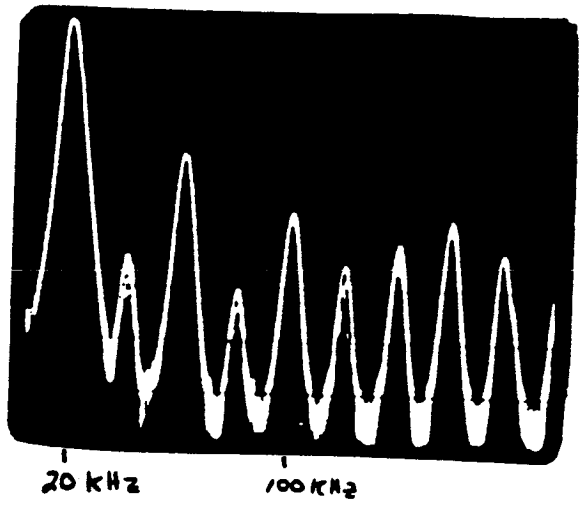


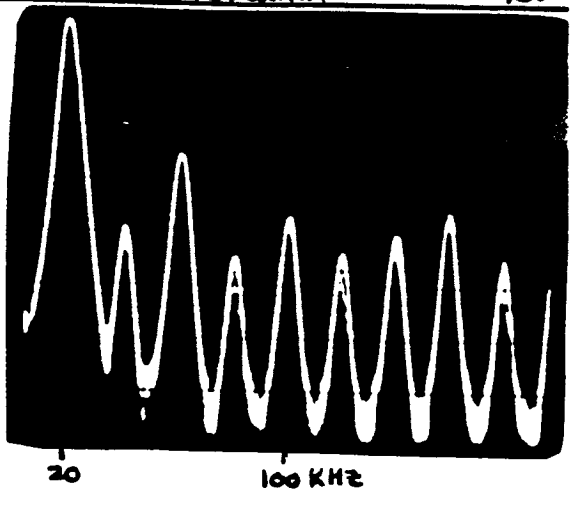
FIGURE 4.2-46. BUS VOLTAGES FOR THE INDUCTIVE AND CAPACITIVE COMPENSATION CASE AT FULL LOAD.



20 KHz/Div

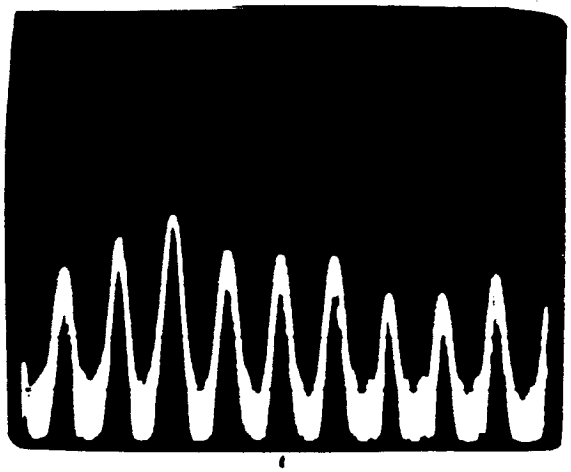


Vca line to neutral Scale:10db/div



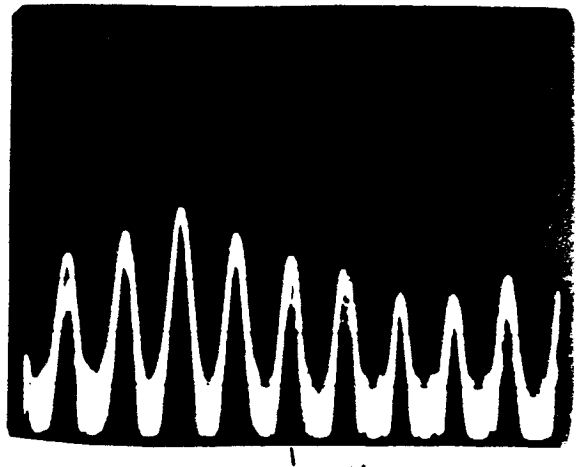
VcB line to neutral Scale: 10db/div

FIGURE 4.2-47. LOW FREQUENCY COMPONENTS ON THE BUS FOR THE INDUCTIVE AND CAPACITIVE COMPENSATION CASE AT NO LOAD.

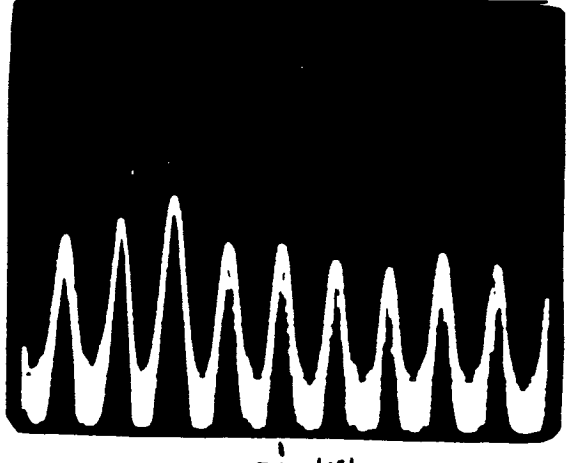


Vca line to neutral Scale: 10 db/div

20 KHz/Div.



Vbc line to neutral Scale: 10db/Div



Vab line to neutral Scale: 10 db/ div

FIGURE 4.2-48. HIGH FREQUENCY COMPONENTS ON THE BUS FOR THE INDUCTIVE AND CAPACITIVE COMPENSATION CASE AT NO LOAD.

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OF POOR QUALITY

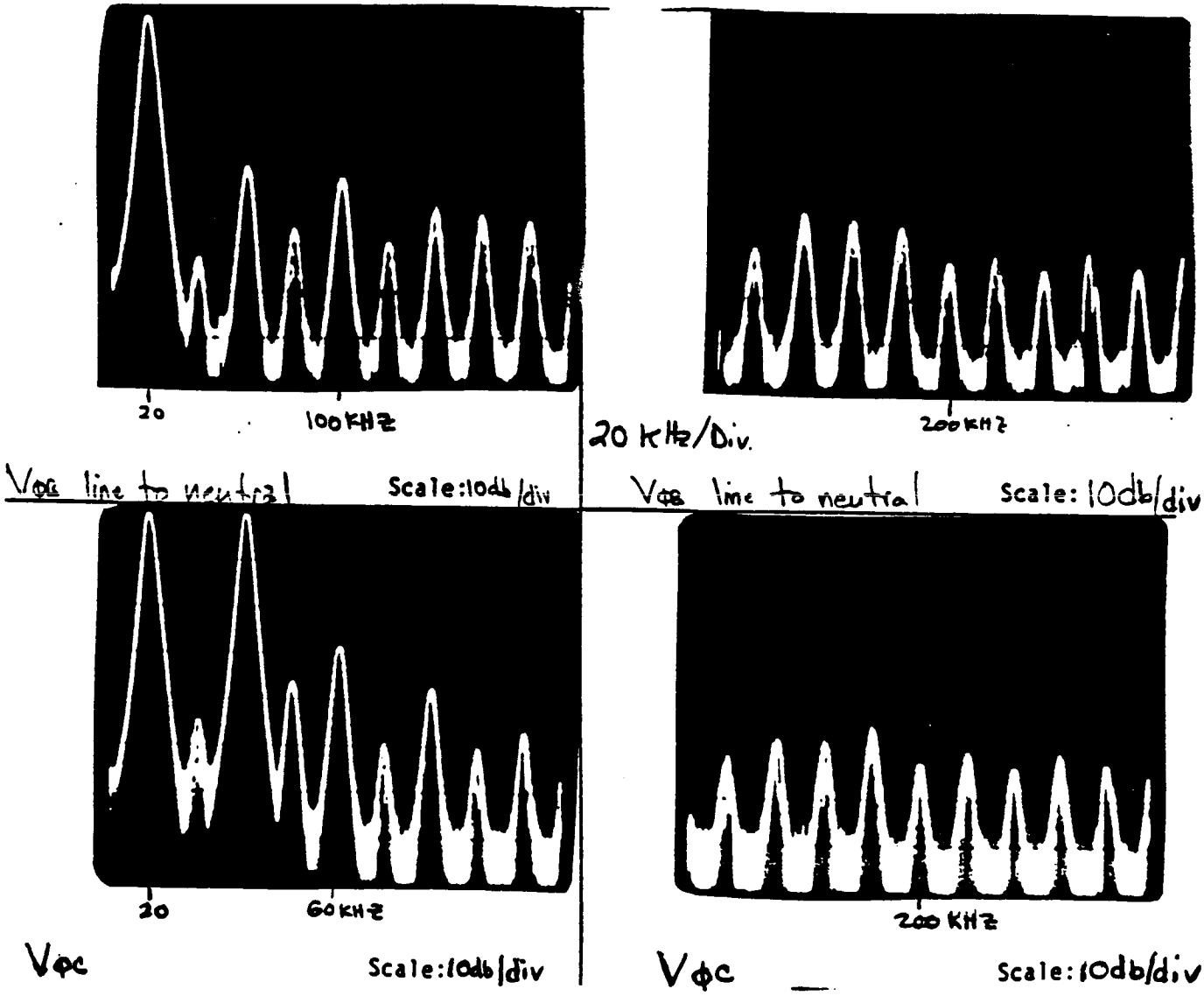


FIGURE 4.2-49. FREQUENCY COMPONENTS ON THE BUS FOR THE INDUCTIVE AND CAPACITIVE COMPENSATION CASE AT FULL LOAD.

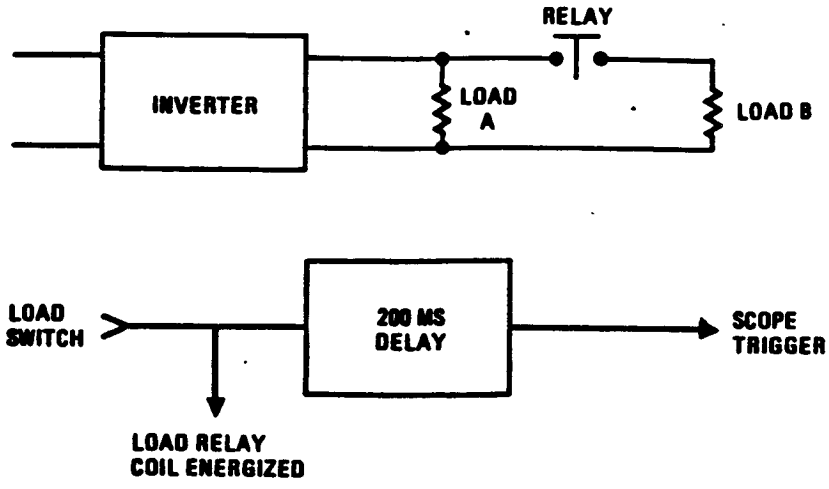


FIGURE 4.3-1. TEST CIRCUIT TO MEASURE TRANSIENT LOAD RESPONSE OF A SINGLE INVERTER MODULE

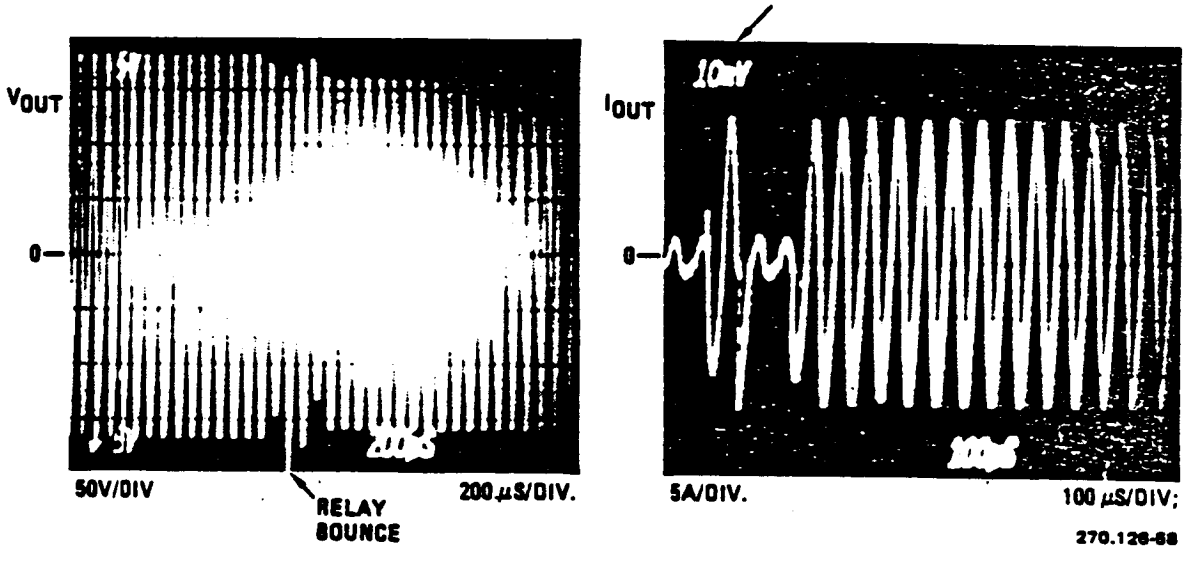


FIGURE 4.3-2. INVERTER OUTPUT VOLTAGE AND CURRENT AS THE LOAD IS SWITCHED FROM 130W TO 1110W

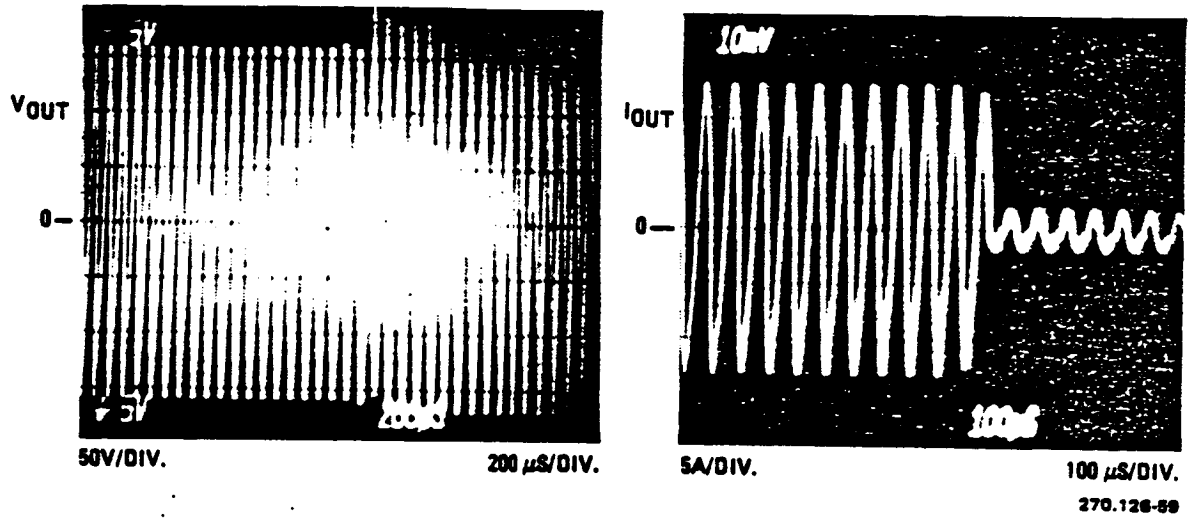


FIGURE 4.3-3. INVERTER OUTPUT VOLTAGE AND CURRENT AS THE LOAD IS SWITCHED FROM 1110W TO 130W

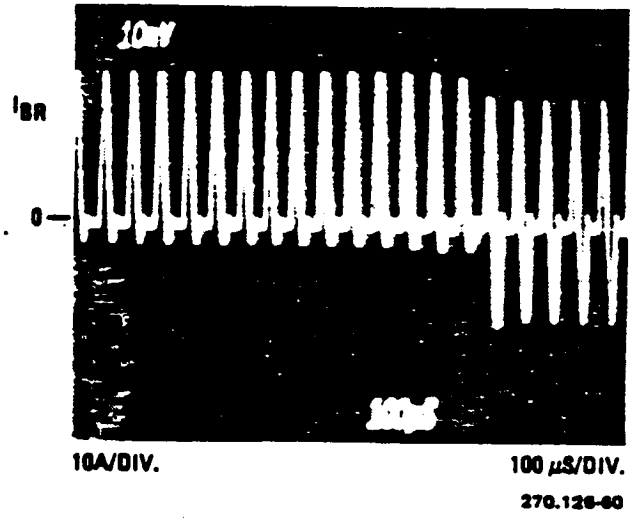


FIGURE 4.3-4. INVERTER LEG CURRENT AS THE LOAD IS SWITCHED FROM 1110W TO 130W.

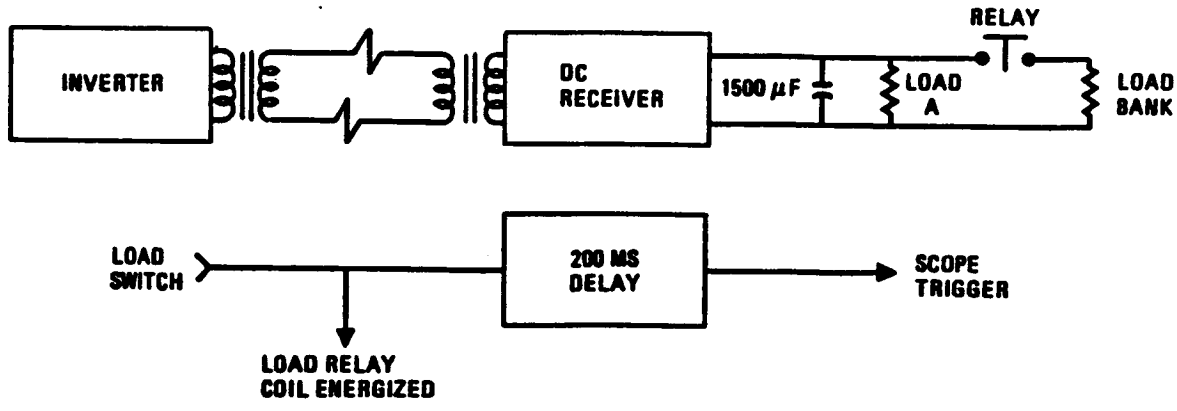


FIGURE 4.3-5. TEST CIRCUIT USED TO SWITCH THE LOADS ON THE DC RECEIVER AND MEASURE THE SYSTEM RESPONSE

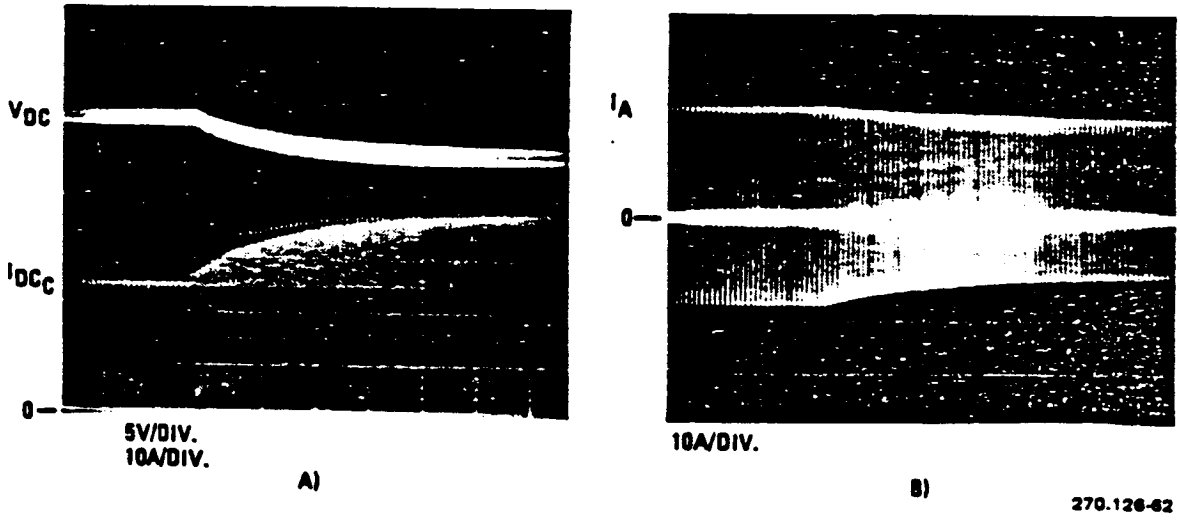
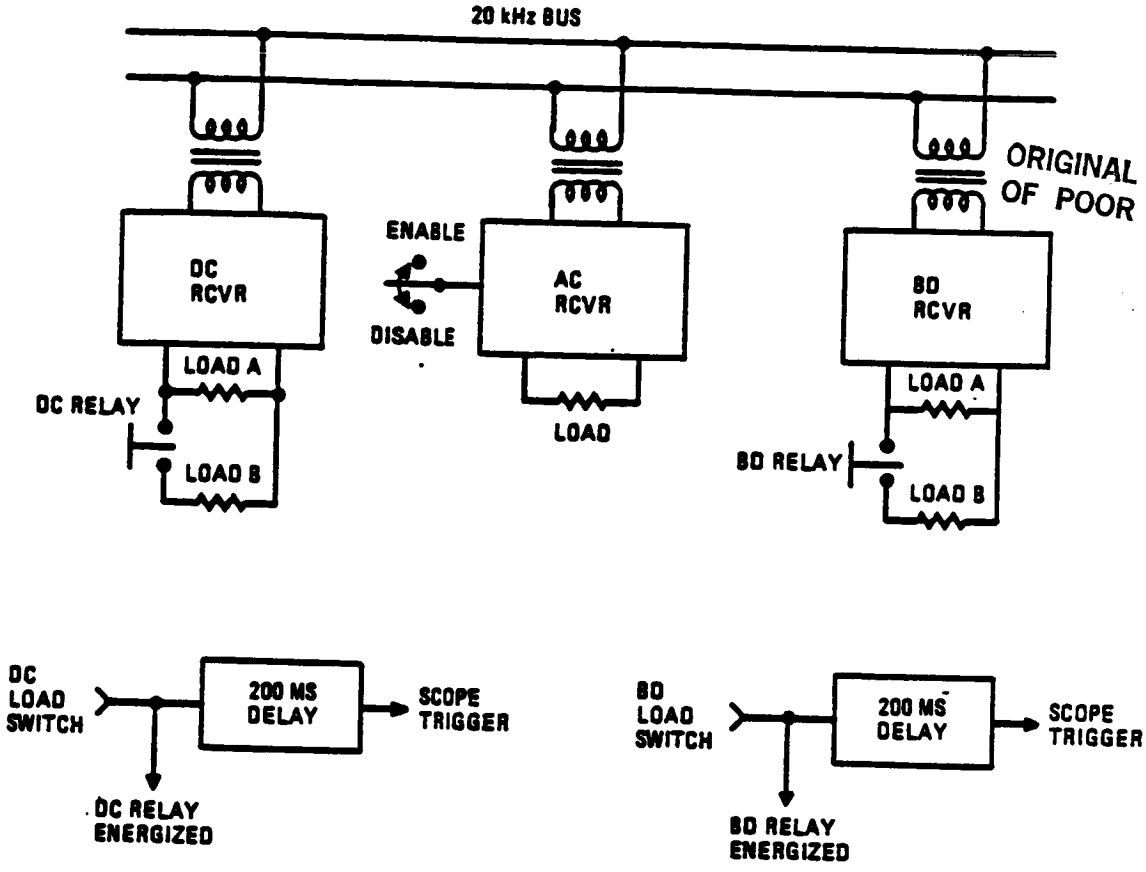
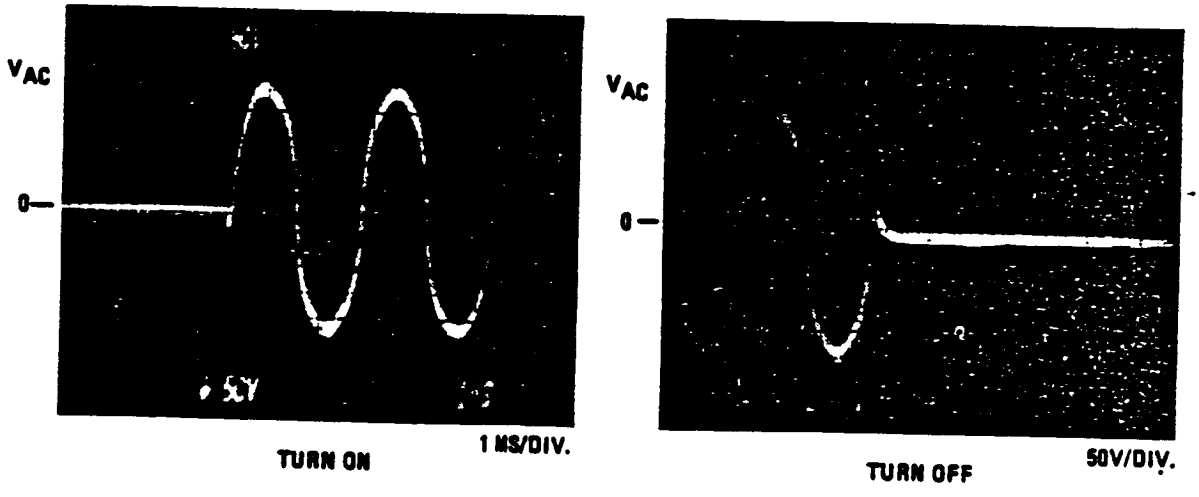


FIGURE 4.3-6. OUTPUT VOLTAGE AND FILTER CURRENT OF DC RECEIVER (A) AND INVERTER LEG CURRENT (B) AS THE LOAD IS SWITCHED FROM 180W TO 410W



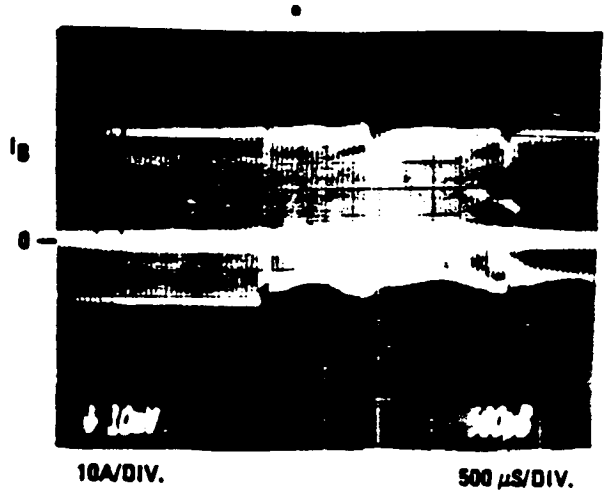
LOAD SWITCHING IS DONE FOR EACH RECEIVER WHILE THE TWO OTHER RECEIVERS MAINTAIN 50% LOADING.

FIGURE 4.3-7. TEST CIRCUIT USED TO MEASURE TRANSIENT LOAD RESPONSE OF THE DUAL-INVERTER, SINGLE-PHASE SYSTEM BREADBOARD



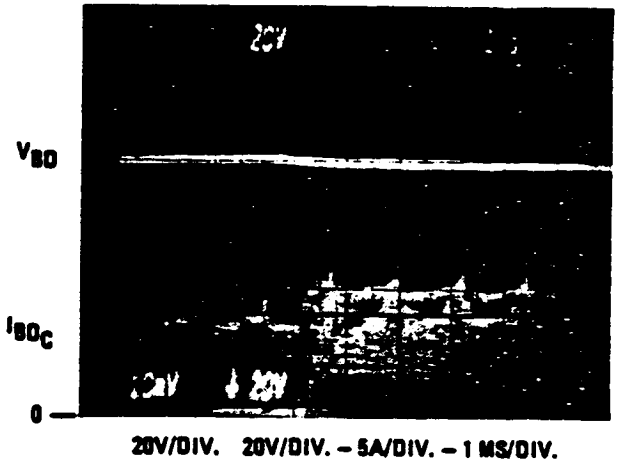
270.128-64

FIGURE 4.3-8. OUTPUT VOLTAGE OF THE AC RECEIVER AS IT IS SWITCHED ON AND OFF THE BUS.



270.126-65

FIGURE 4-3.9. BRANCH CURRENT OF INVERTER 1 AS THE AC RECEIVER IS SWITCHED ON



270.126-66

FIGURE 4.3-10. OUTPUT VOLTAGE AND FILTER CURRENT OF THE BIDIRECTIONAL MODULE (AC-TO-DC MODE) FOR A 210 TO 410W LOAD CHANGE.

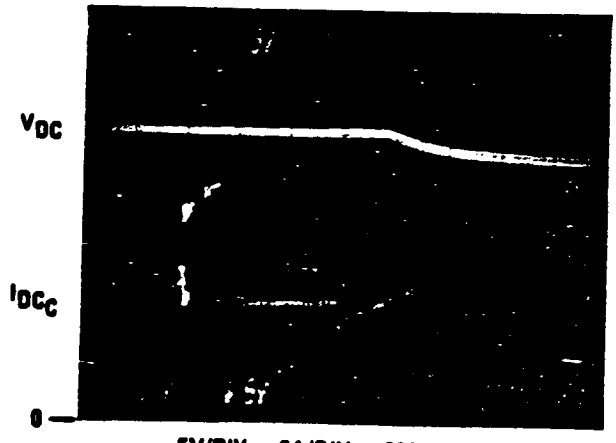
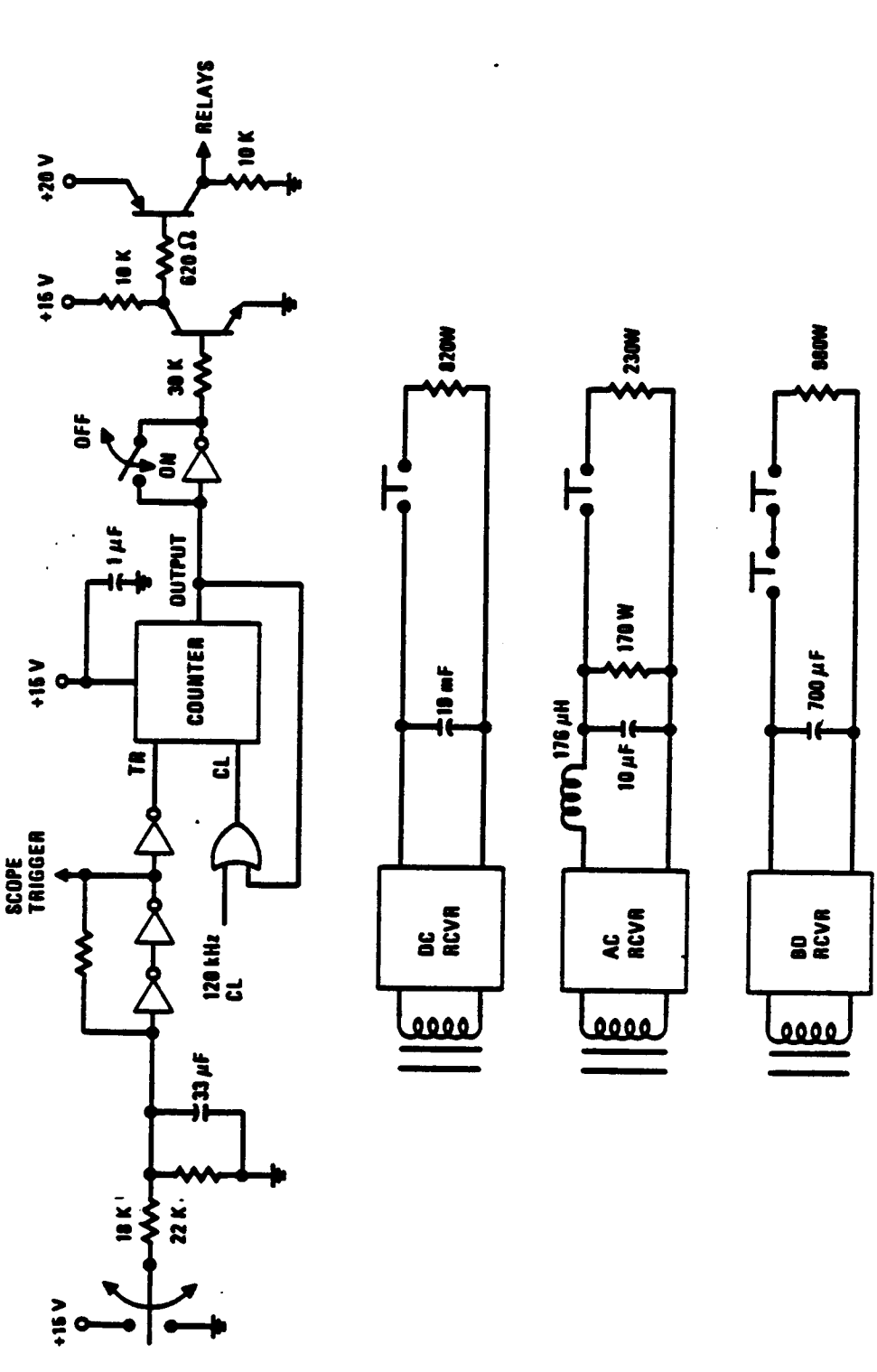


FIGURE 4.3-11. OUTPUT VOLTAGE AND FILTER CURRENT OF THE DC RECEIVER AS THE LOAD IS ABRUPTLY INCREASED FROM 200W TO 400W.

FIGURE 4.3-12. TRANSIENT LOAD RESPONSE TEST CIRCUIT FOR THE THREE-PHASE SYSTEM BREADBOARD



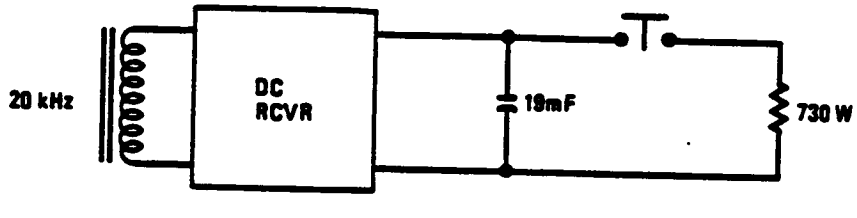


FIGURE 4.3-13. TEST CIRCUIT USED TO MEASURE THE SYSTEM RESPONSE TO A LOAD CHANGE ON THE DC RECEIVER

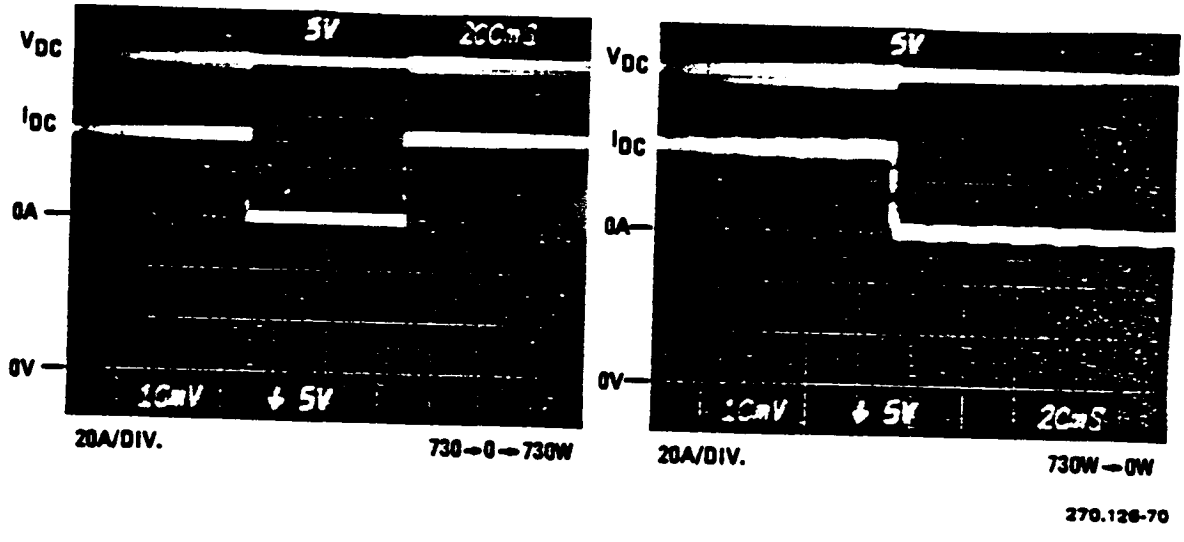
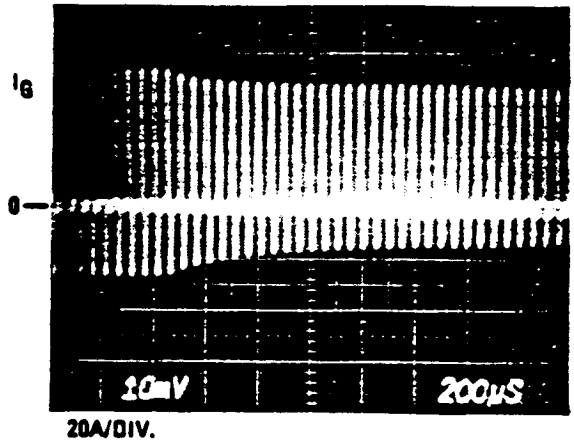
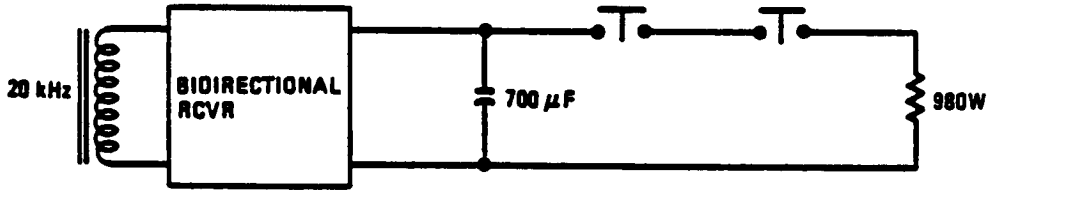


FIGURE 4.3-14. OUTPUT VOLTAGE AND CURRENT OF THE DC RECEIVER MODULE AS THE LOAD IS SWITCHED BETWEEN 0.0 AND 730W



270.126-71

FIGURE 4.3-15. LEG CURRENT OF INVERTER NUMBER 3 WHEN THE LOAD IS SWITCHED FROM 0.0 TO 730W



270 126-72

FIGURE 4.3-16. CIRCUIT USED TO GATHER LOAD-SWITCHING DATA ON THE THREE-PHASE SYSTEM AS THE LOAD ON THE BIDIRECTIONAL MODULE IS CHANGED ABRUPTLY

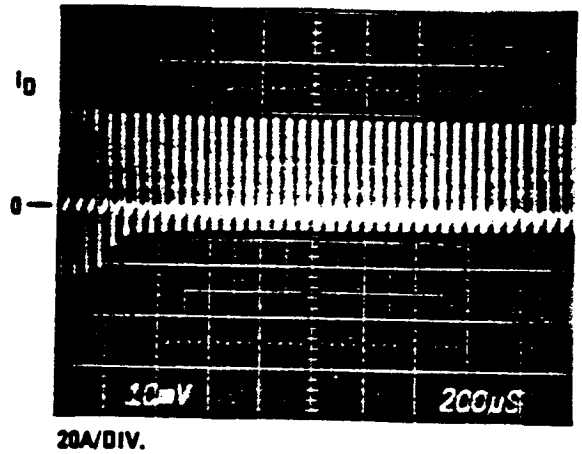


FIGURE 4.3-17. RESPONSE OF THE LEG CURRENT OF INVERTER 2 AS THE LOAD ON THE BIDIRECTIONAL MODULE IS SWITCHED FROM 0.0 TO 980W

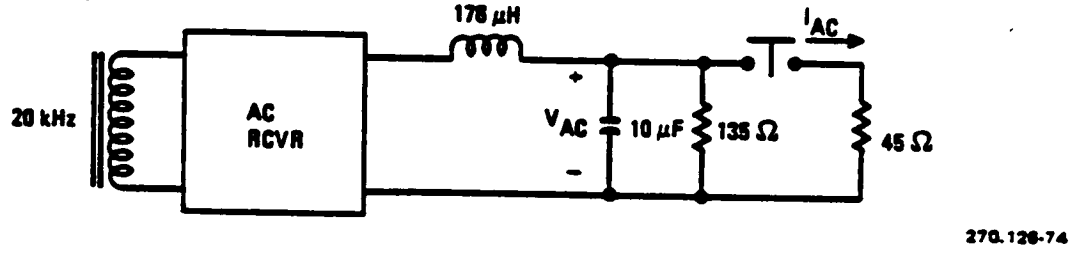
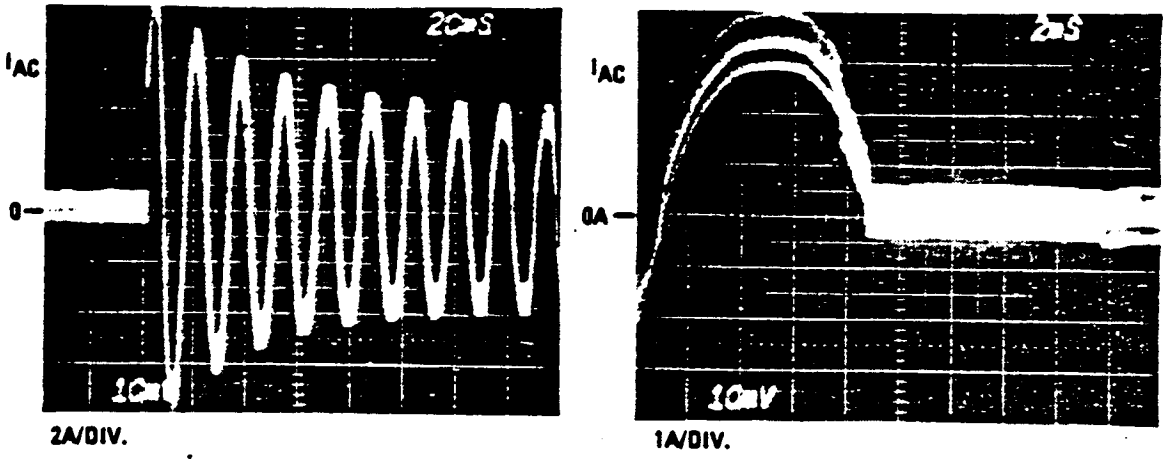
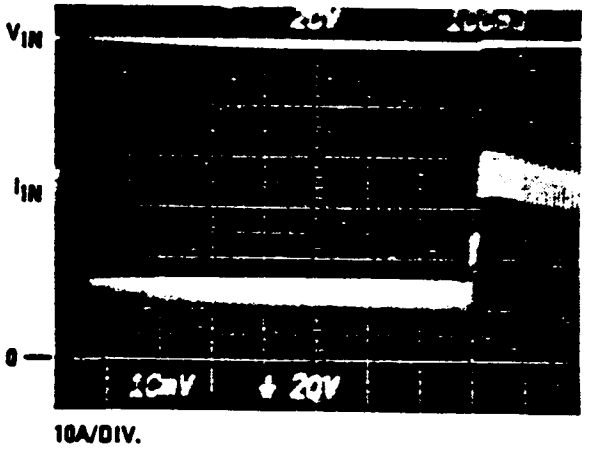


FIGURE 4.3-18. CIRCUIT USED TO GATHER DATA ON THE SYSTEM RESPONSE TO LOAD CHANGES ON THE AC RECEIVER MODULE



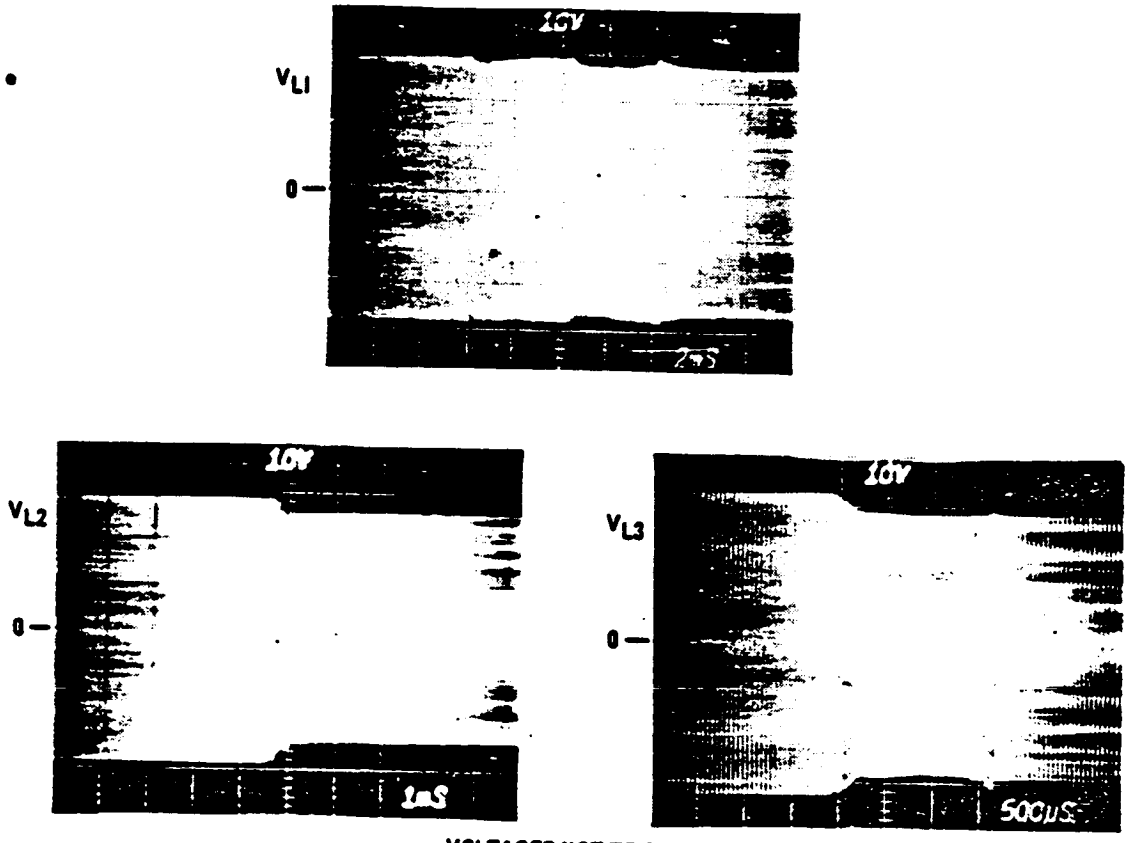
270.126-75

FIGURE 4.3-19. OUTPUT CURRENT OF THE AC RECEIVER MODULE AS 230W OF LOAD ARE ADDED OR REMOVED



270.126-76

FIGURE 4.3-20. SYSTEM INPUT VOLTAGE AND CURRENT AS THE LOADS ON ALL THREE RECEIVER MODULES ARE SWITCHED SIMULTANEOUSLY

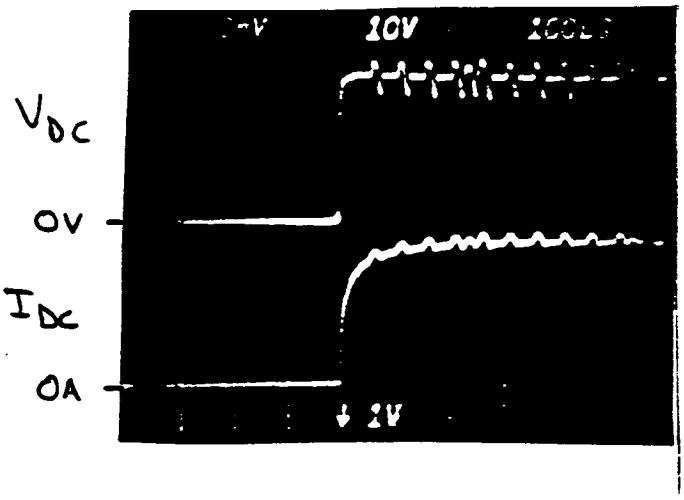


VOLTAGES NOT TO SCALE

270.128-77

FIGURE 4.3-21. LINE-TO-NEUTRAL BUS VOLTAGES AS 2200W OF LOAD ARE ADDED TO THE SYSTEM

FIGURE 4.3-22. CIRCUIT USED TO SWITCH THE LOAD ON THE DC RECEIVER.



Scale: 10A/DIV

FIGURE 4.3-23. OUTPUT VOLTAGE AND CURRENT OF THE DC RECEIVER AS THE LOAD IS SWITCHED ON.

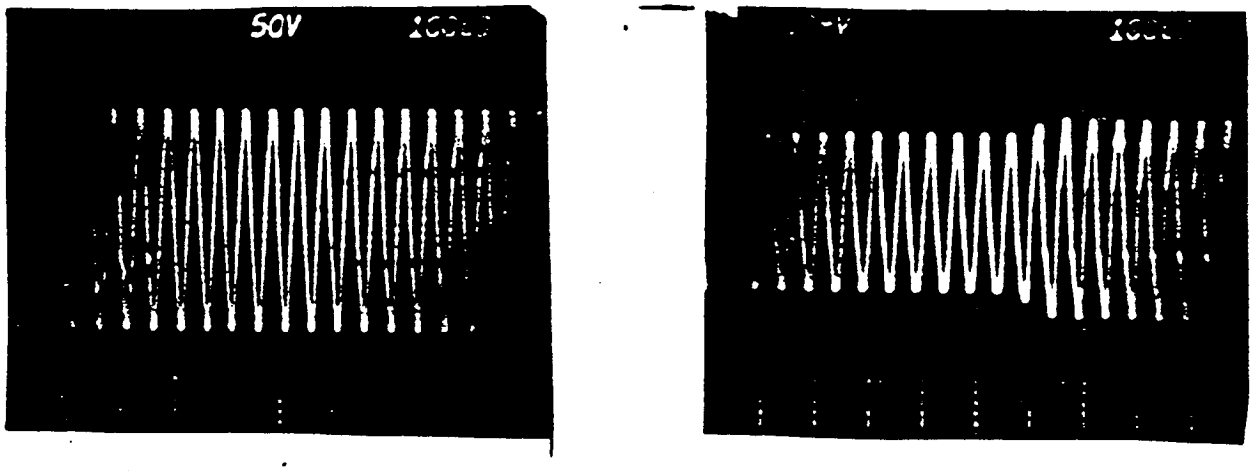


FIGURE 4.3-24. BUS VOLTAGE AND CURRENT AS THE DC RECEIVER LOAD IS SWITCHED ON.

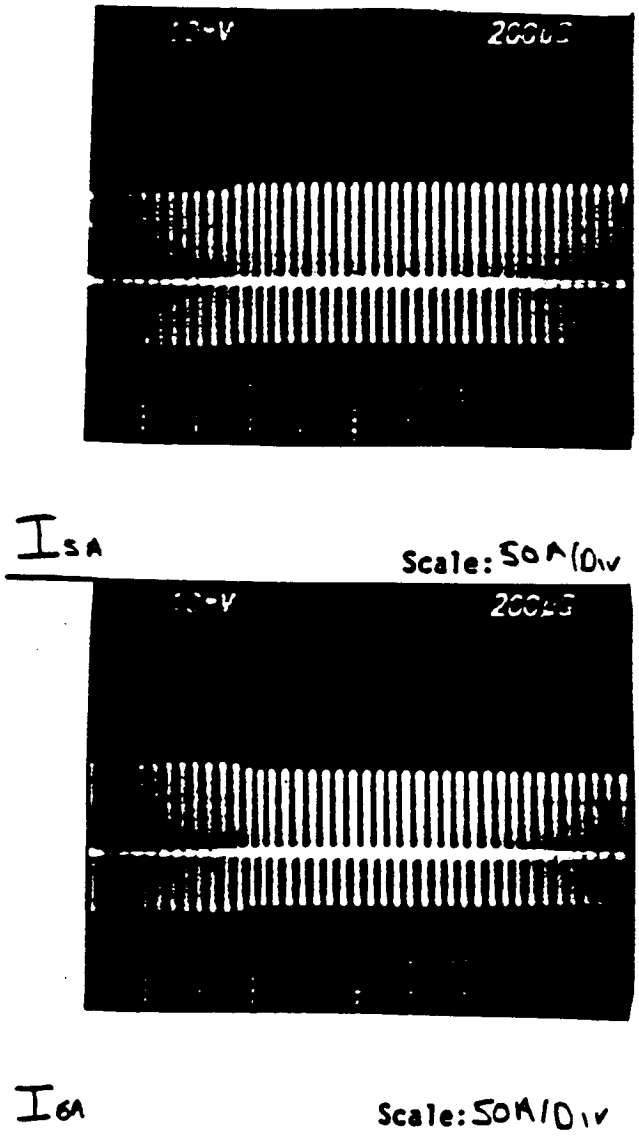


FIGURE 4.3-25. INVERTER LEG CURRENTS AS THE DC RECEIVER LOAD IS SWITCHED ON.

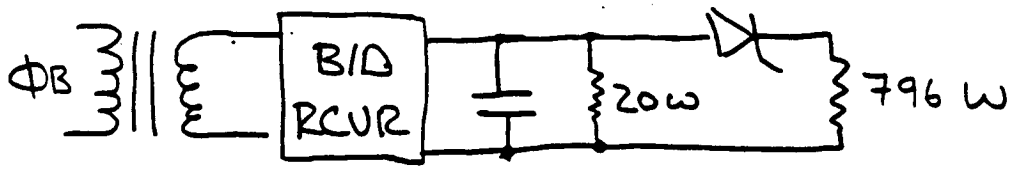


FIGURE 4.3-26. CIRCUIT USED TO SWITCH THE BIDIRECTIONAL MODULE LOAD.

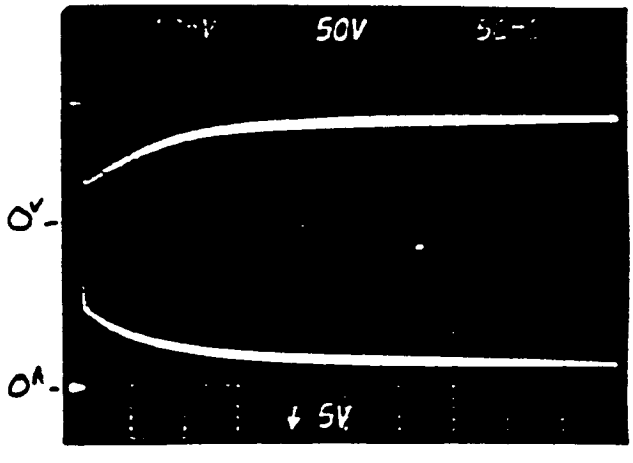


FIGURE 4.3-27. OUTPUT VOLTAGE AND CURRENT OF THE BIDIRECTIONAL MODULE AS THE LOAD IS APPLIED.

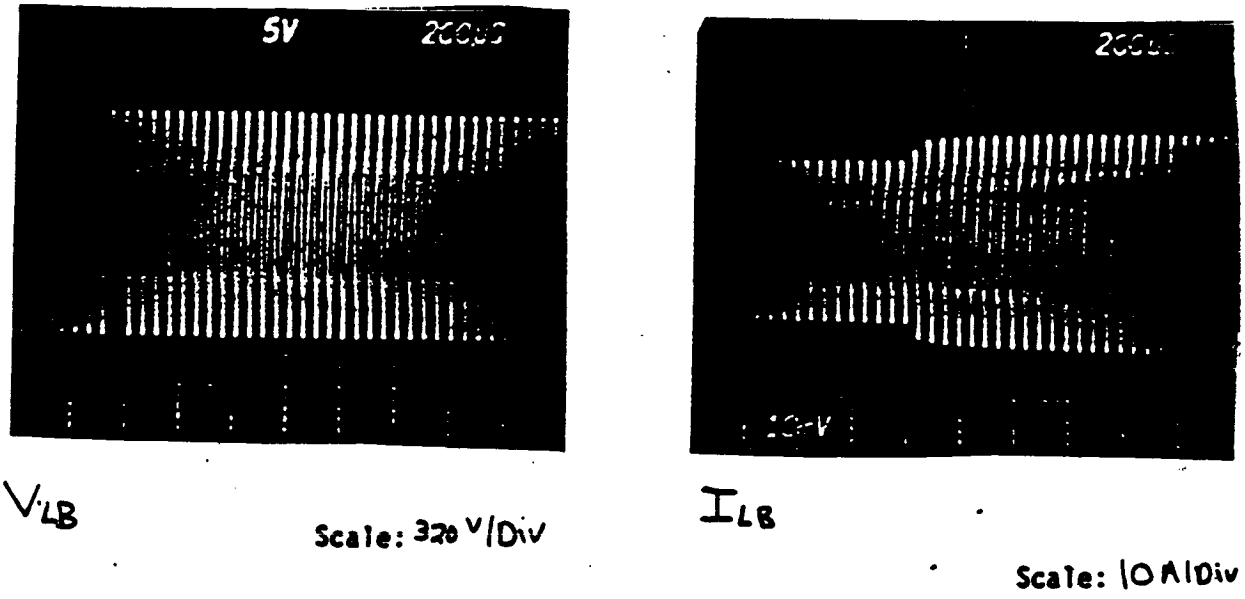


FIGURE 4.3-28. BUS VOLTAGE AND CURRENT AS THE LOAD IS APPLIED TO THE BIDIRECTIONAL MODULE.

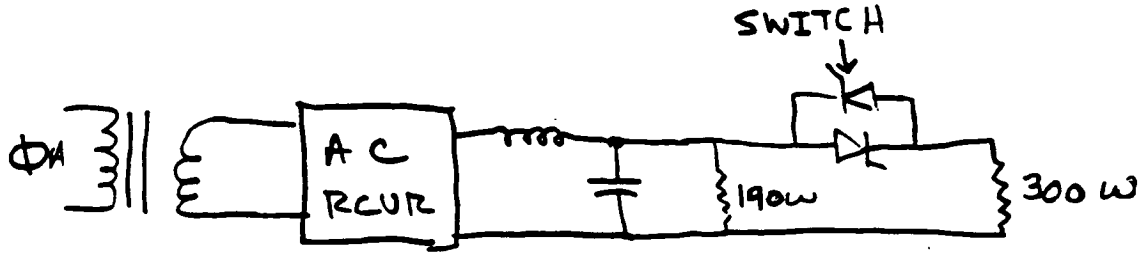
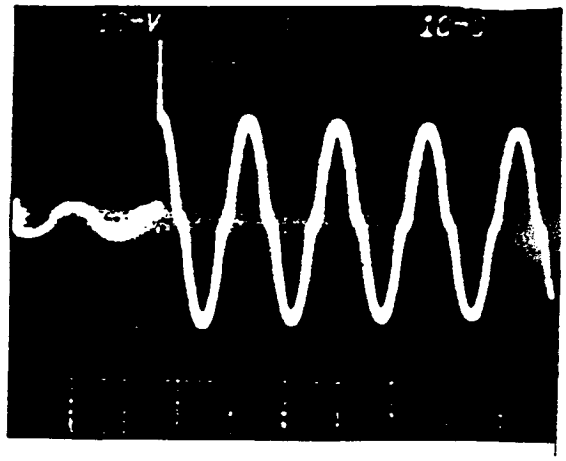


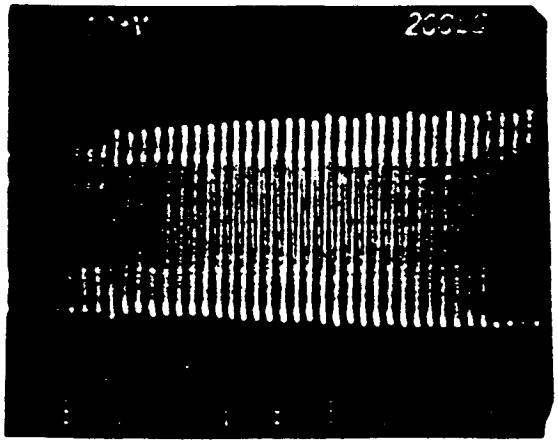
FIGURE 4.3-29. CIRCUIT USED TO SWITCH THE LOAD ON THE AC RECEIVER.

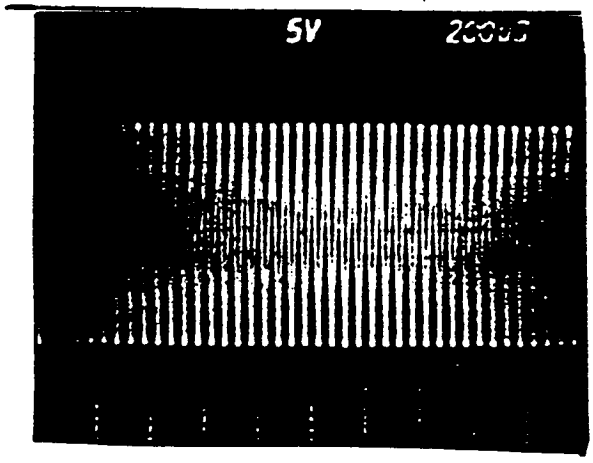


I_{AC}

Scale: 5A/div

FIGURE 4.3-30. OUTPUT CURRENT OF THE AC RECEIVER AS THE LOAD IS SWITCHED.





I_{LA}

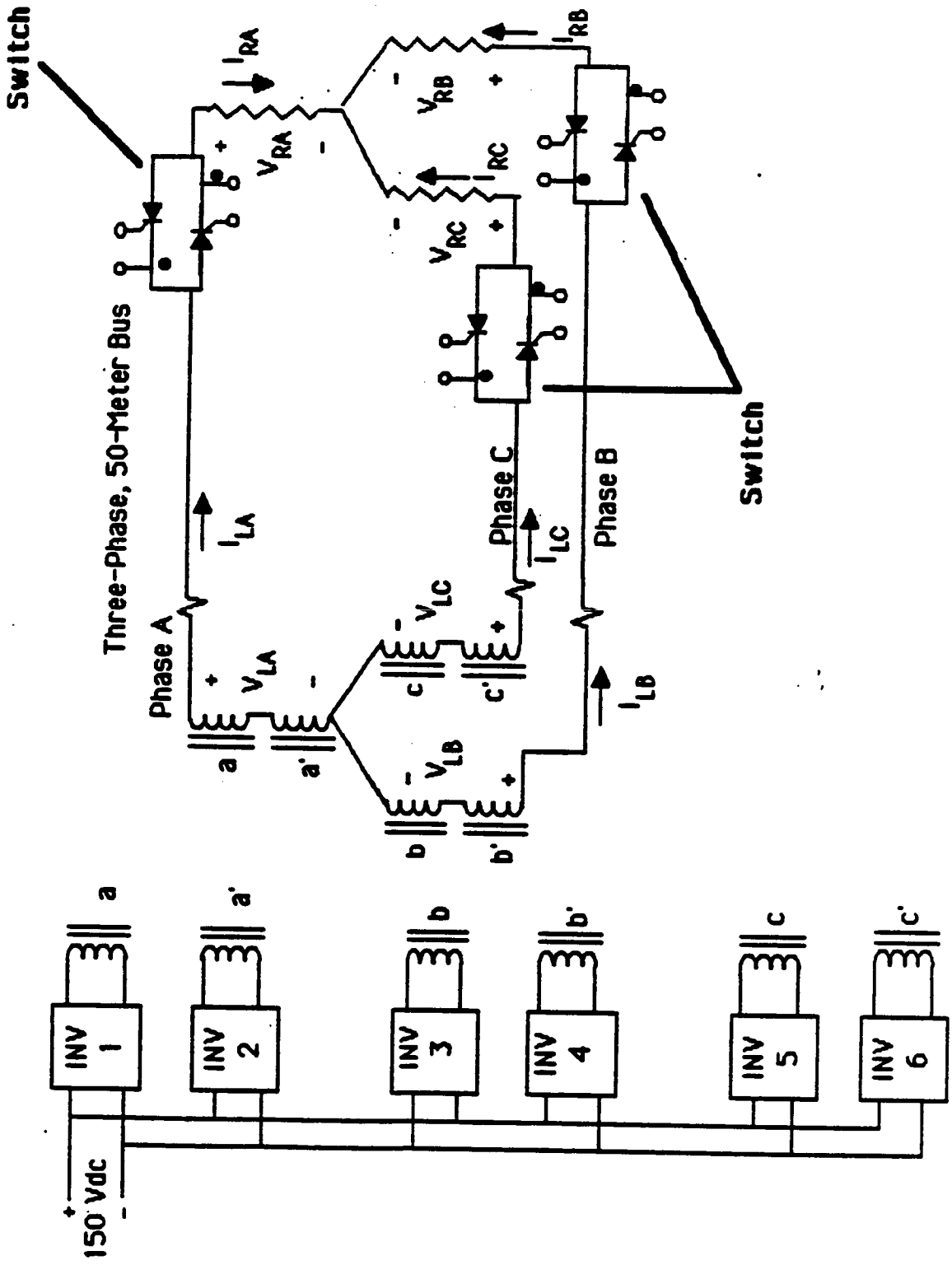
Scale: 10A/div

V_{LA}

Scale:

FIGURE 4.3-31. BUS VOLTAGE AND CURRENT AS THE LOAD IS APPLIED TO THE AC RECEIVER.

FIGURE 4.3-32. THE RESISTIVE LOAD WAS SWITCHED ONTO THE BUS WITH SCRS.



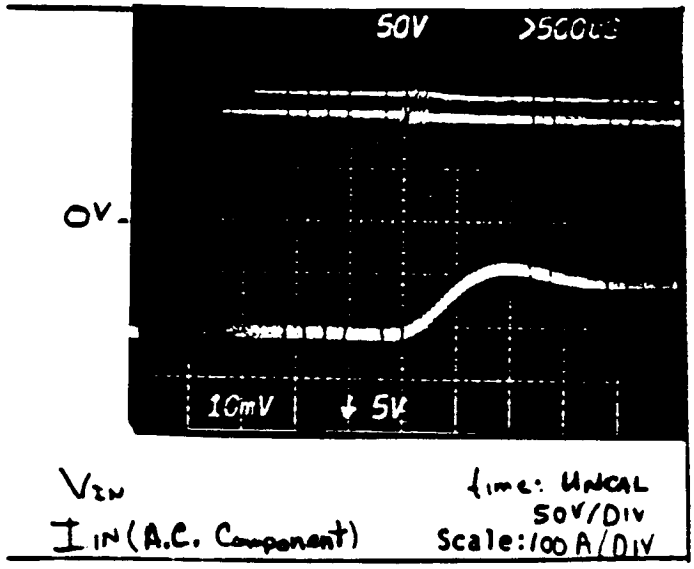


FIGURE 4.3-33. AC COMPONENT OF THE INPUT CURRENT AS THE THREE-PHASE LOAD IS APPLIED.

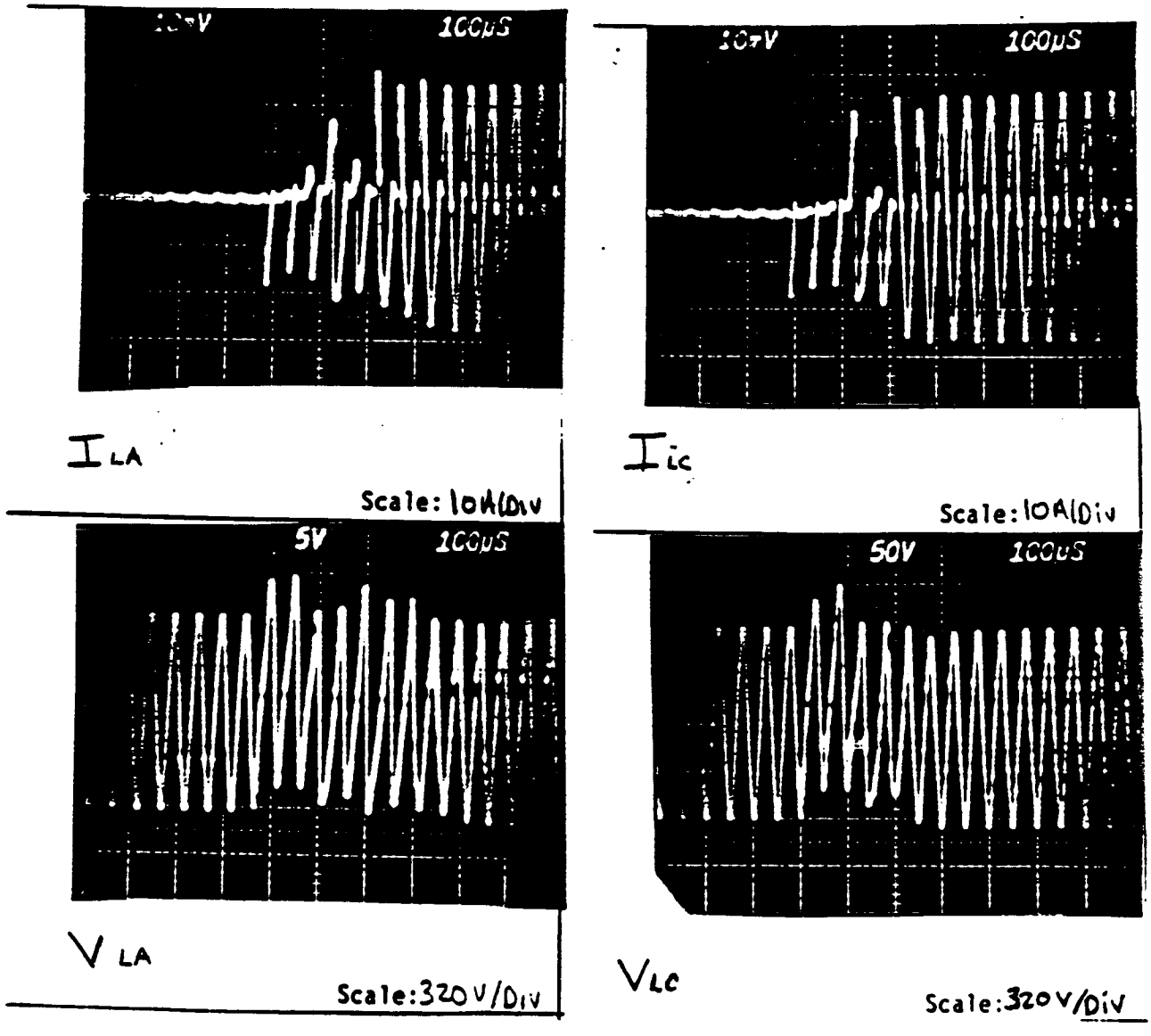


FIGURE 4.3-34. BUS VOLTAGE AND CURRENT AS THE THREE-PHASE LOAD IS APPLIED.

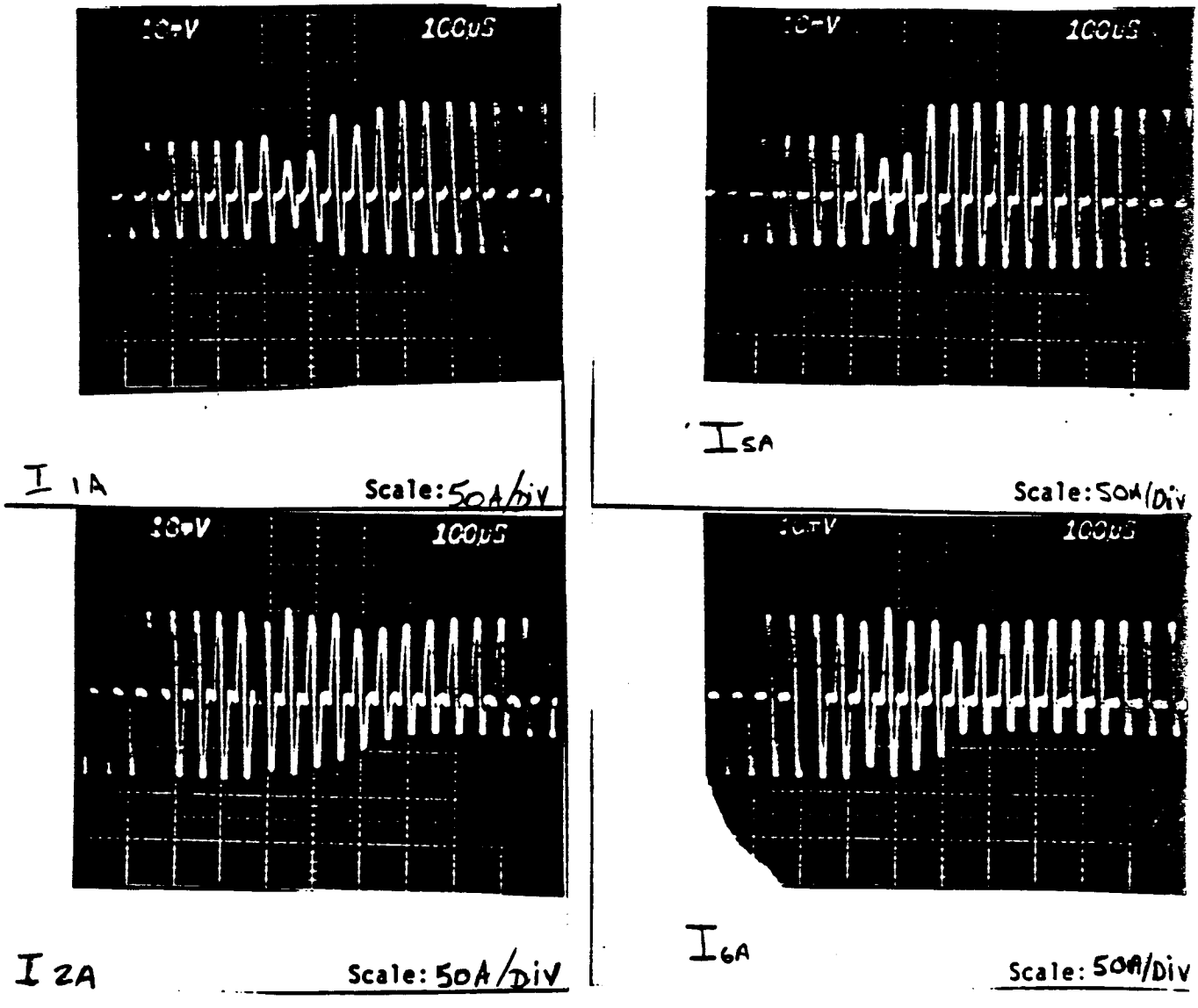


FIGURE 4.3-35. INVERTER LEG CURRENTS AS THE THREE-PHASE LOAD IS APPLIED.

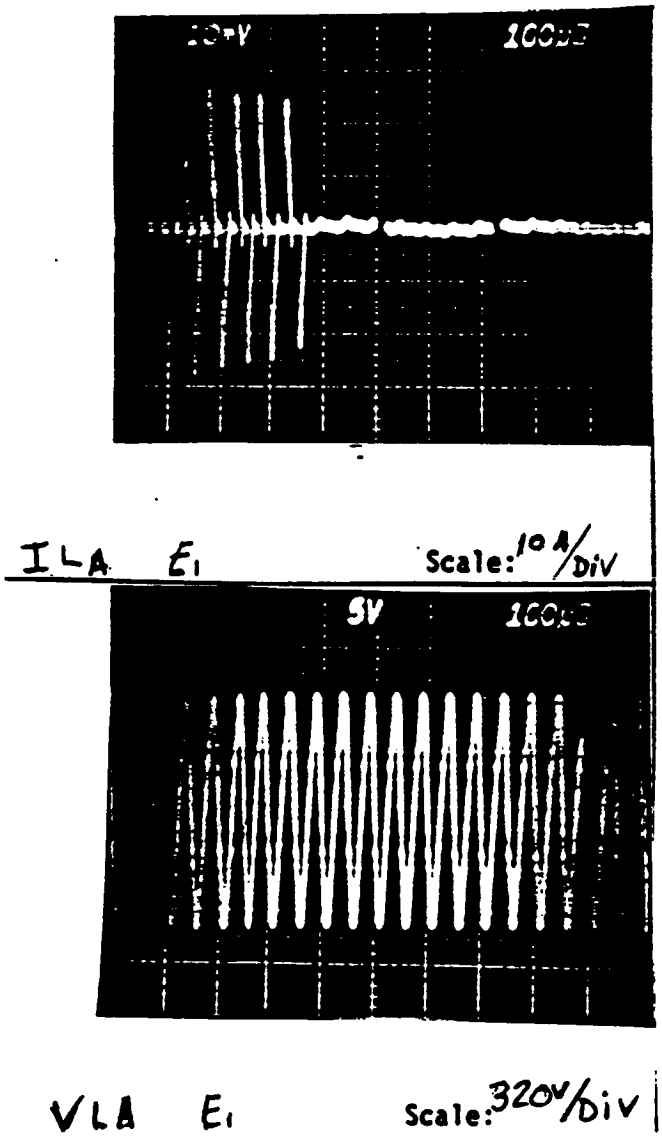


FIGURE 4.3-36. BUS VOLTAGE AND CURRENT AS THE THREE-PHASE LOAD IS REMOVED.

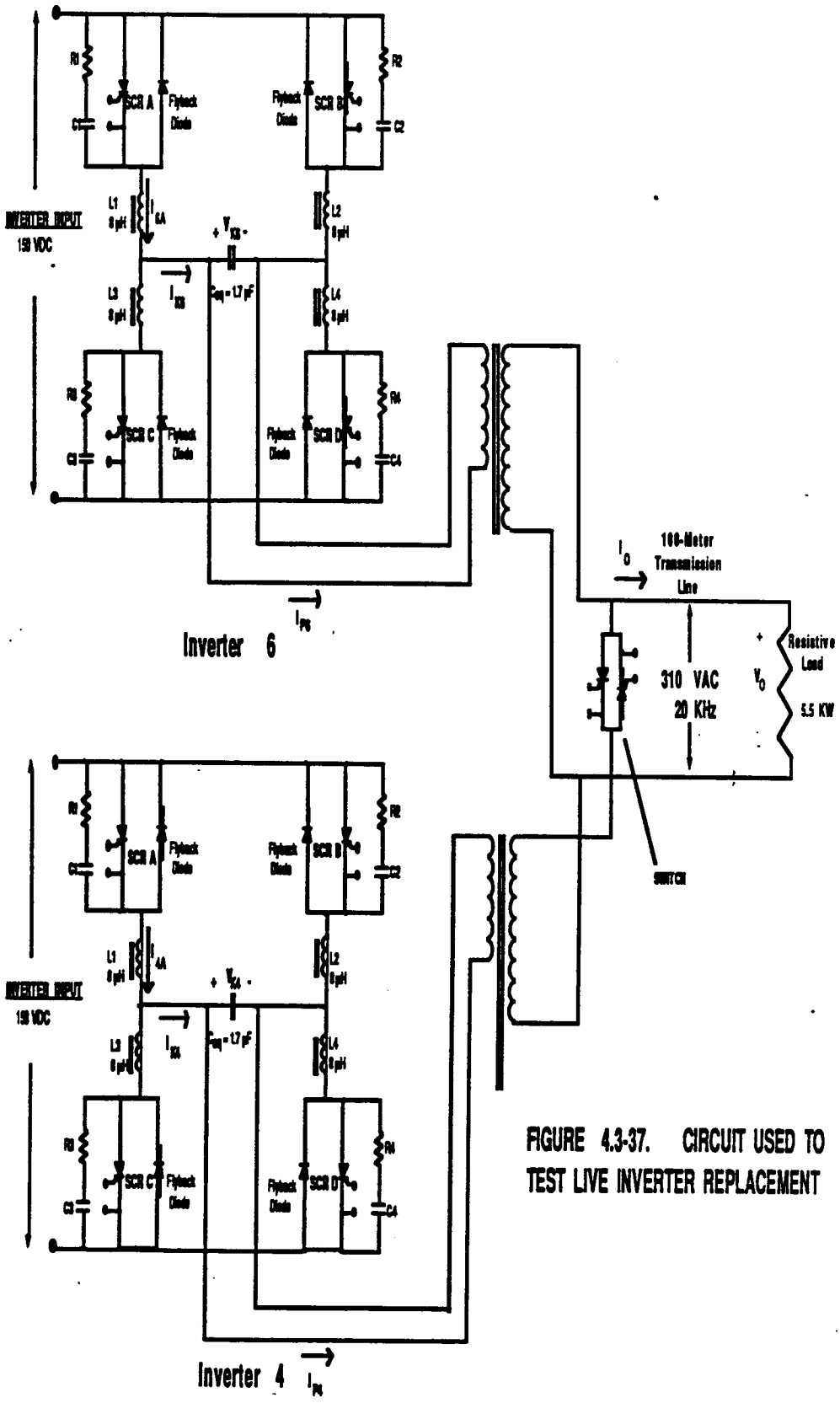


FIGURE 4.3-37. CIRCUIT USED TO TEST LIVE INVERTER REPLACEMENT

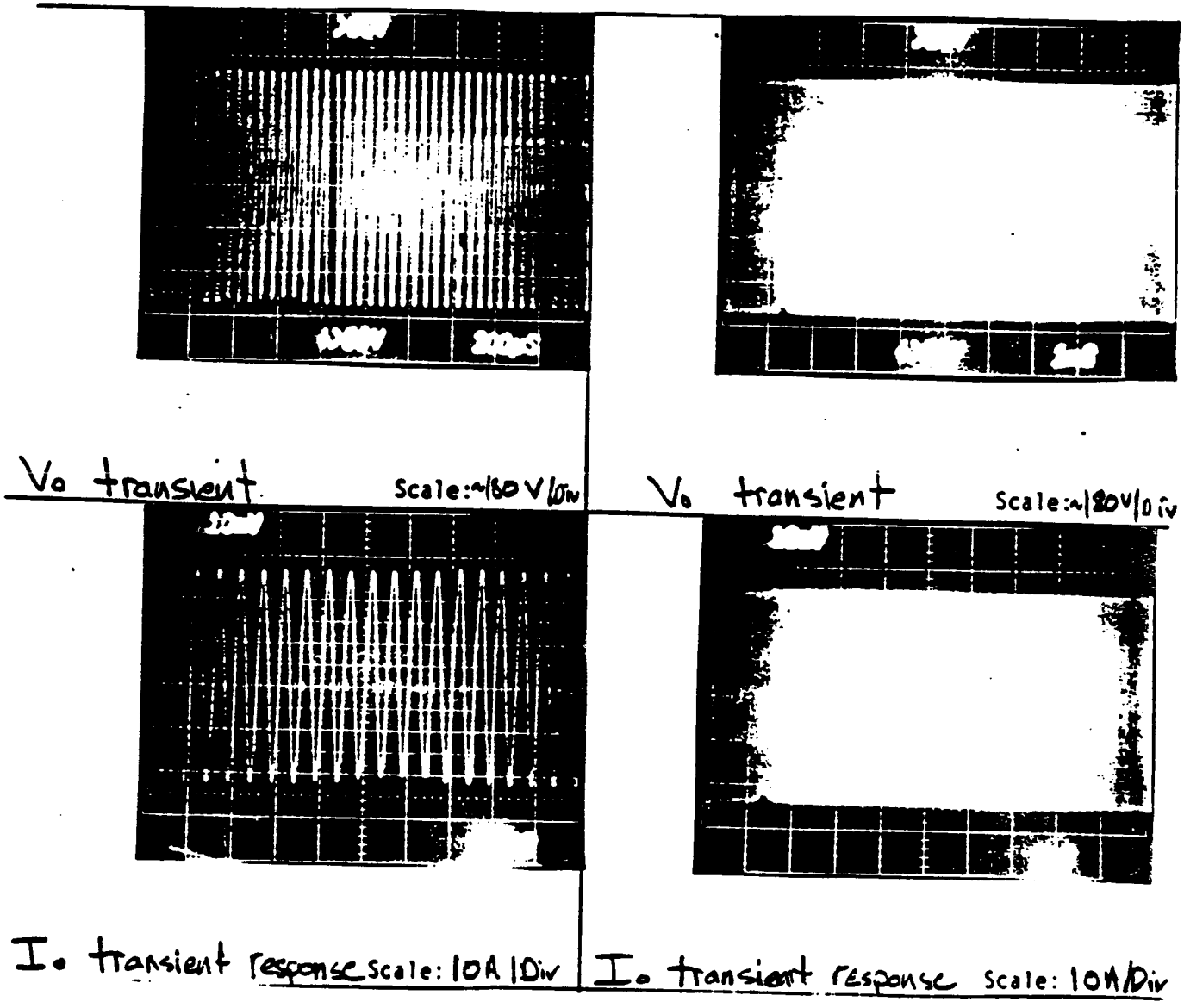


FIGURE 4.3-38. BUS VOLTAGE AND CURRENT AS THE INVERTER IS ADDED TO THE OPERATING BUS.

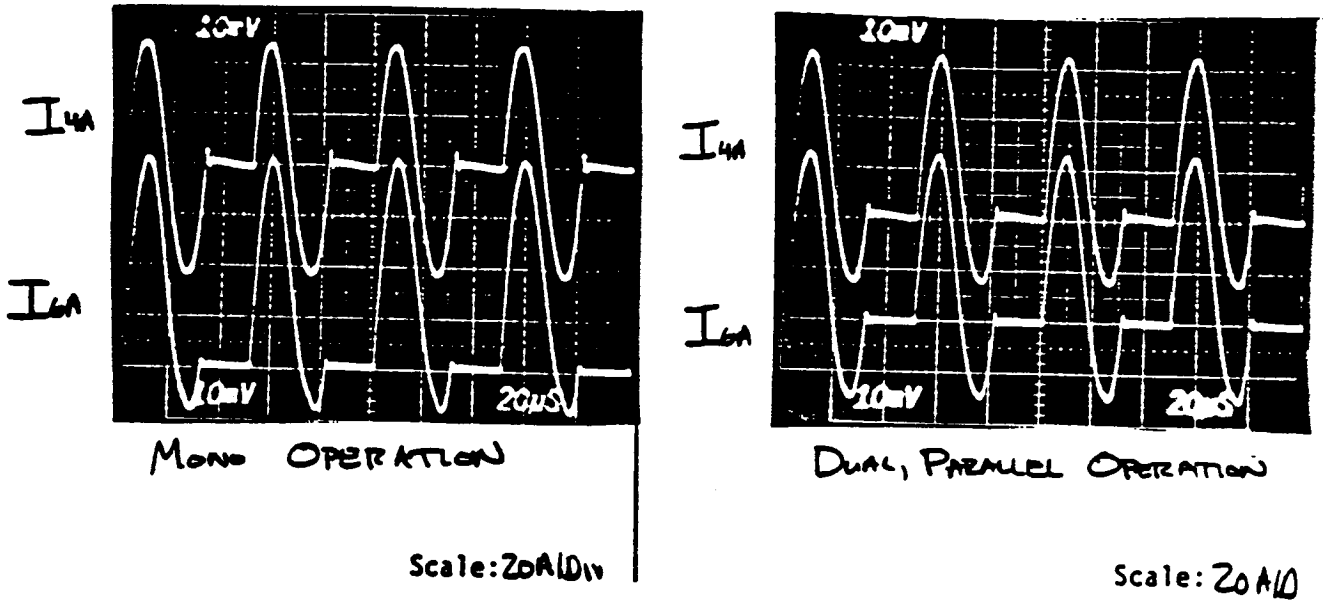


FIGURE 4.3-39. INVERTER LEG CURRENT AS INVERTER 4 IS ADDED TO THE OPERATING BUS.

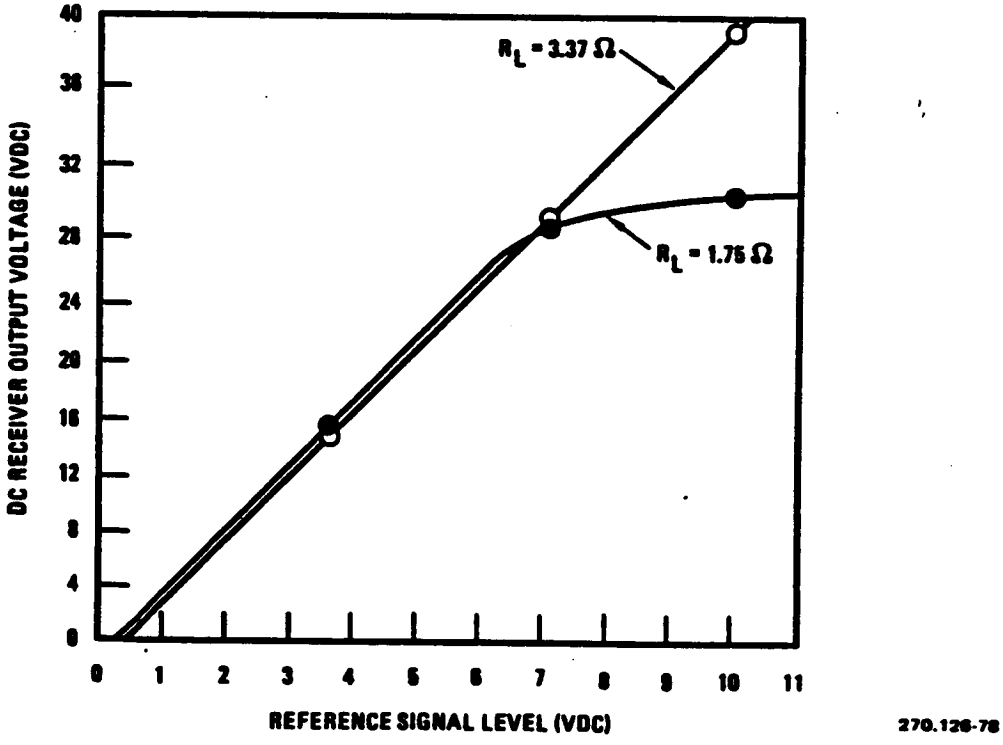


FIGURE 4.4-1. DC RECIEVER OUTPUT VOLTAGE VERSUS THE REFERENCE SIGNAL.

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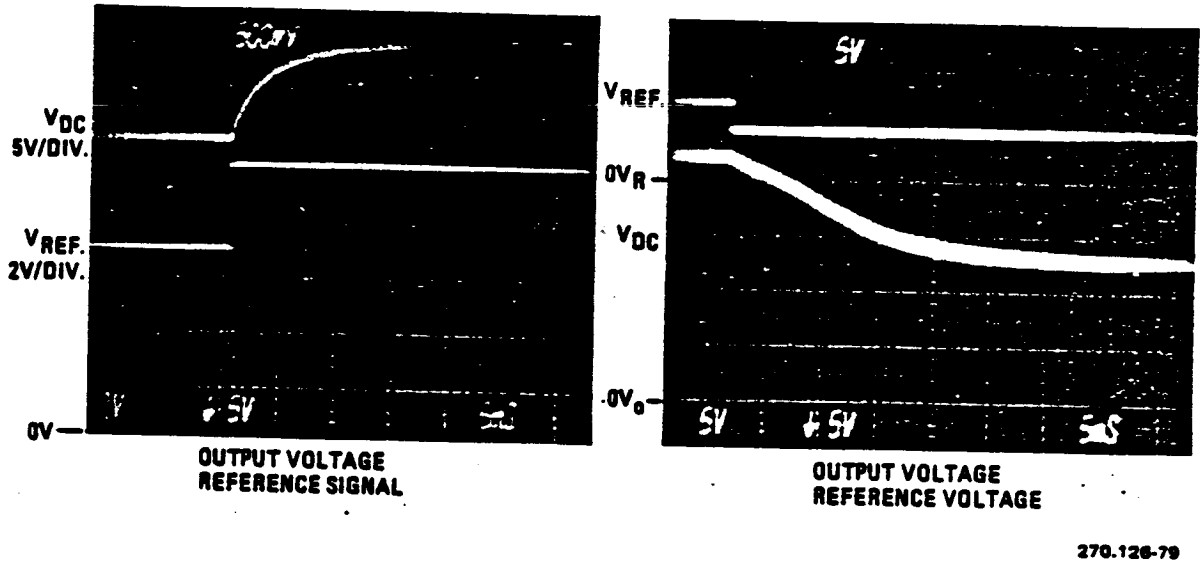

FIGURE 4.4-2. OUTPUT WAVEFORMS OF THE DC RECEIVER AS ITS REFERENCE SIGNAL IS CHANGED

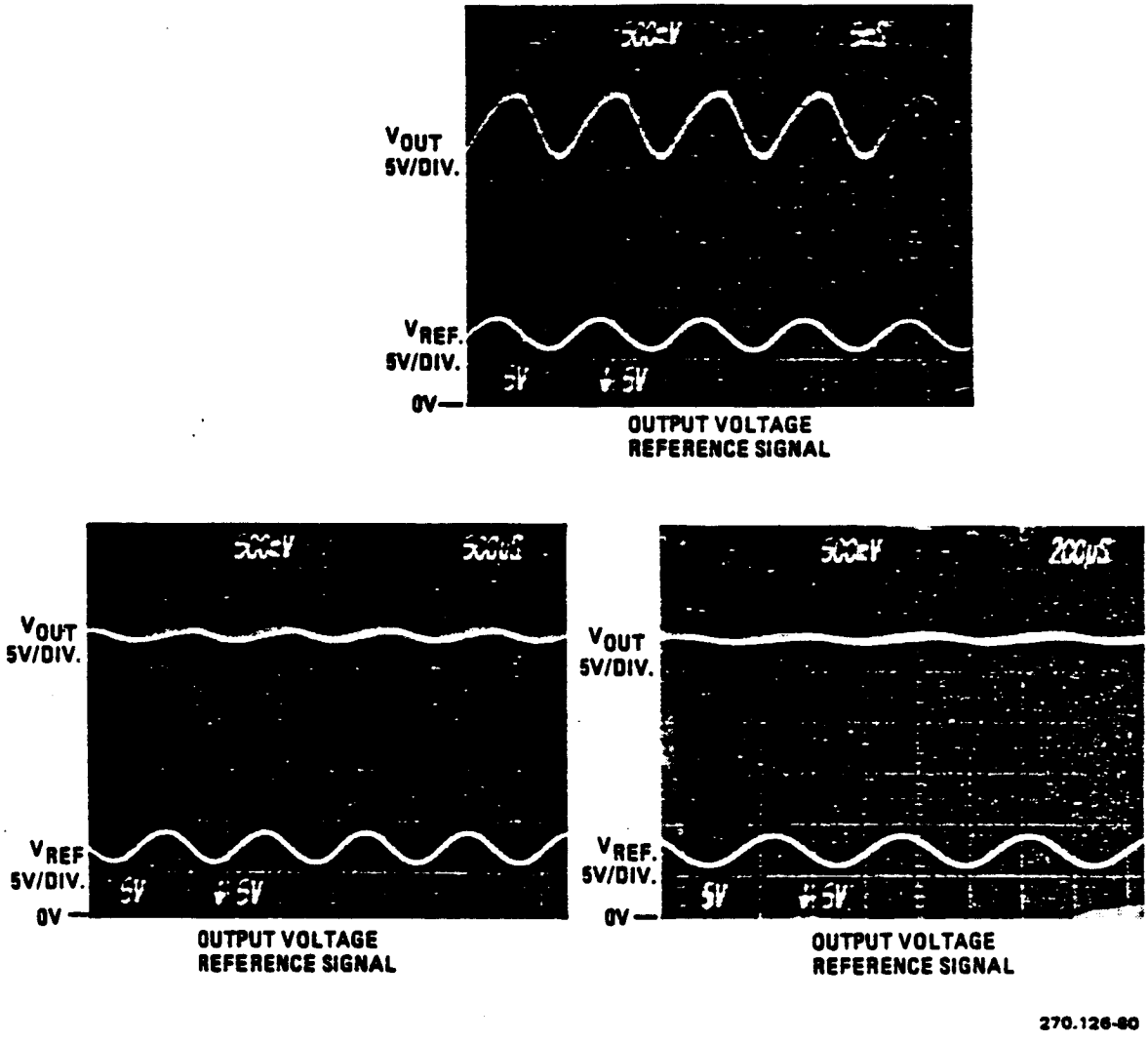

FIGURE 4.4-3. OUTPUT VOLTAGE OF THE DC RECEIVER WITH ITS REFERENCE SIGNAL MODULATED BY AN AC SIGNAL

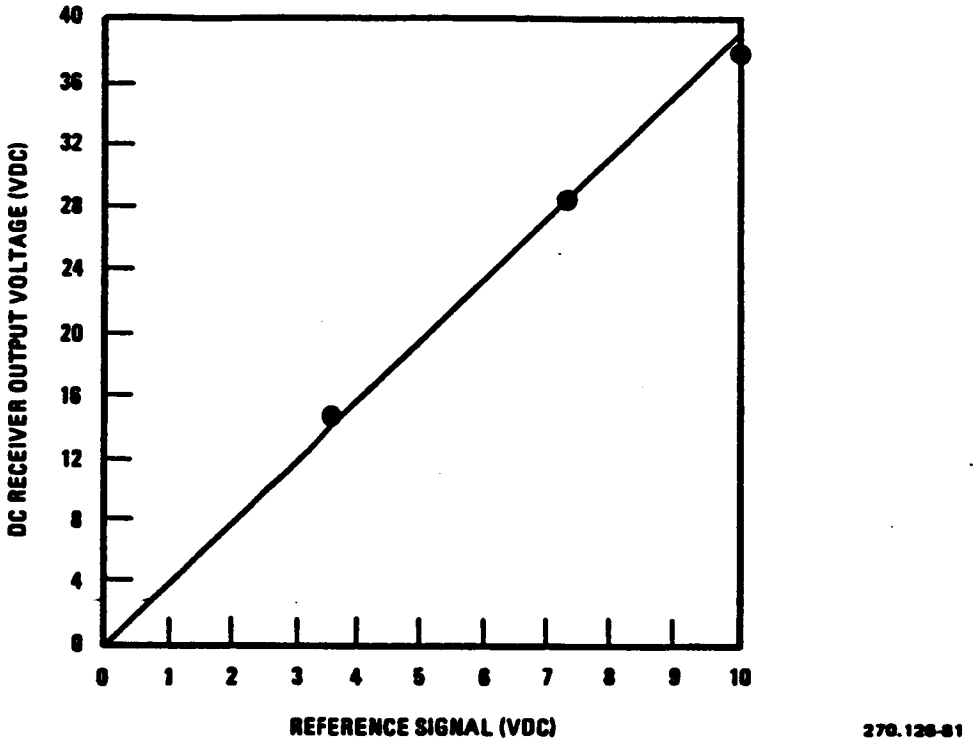

FIGURE 4.4-4. GAIN OF THE DC RECEIVER

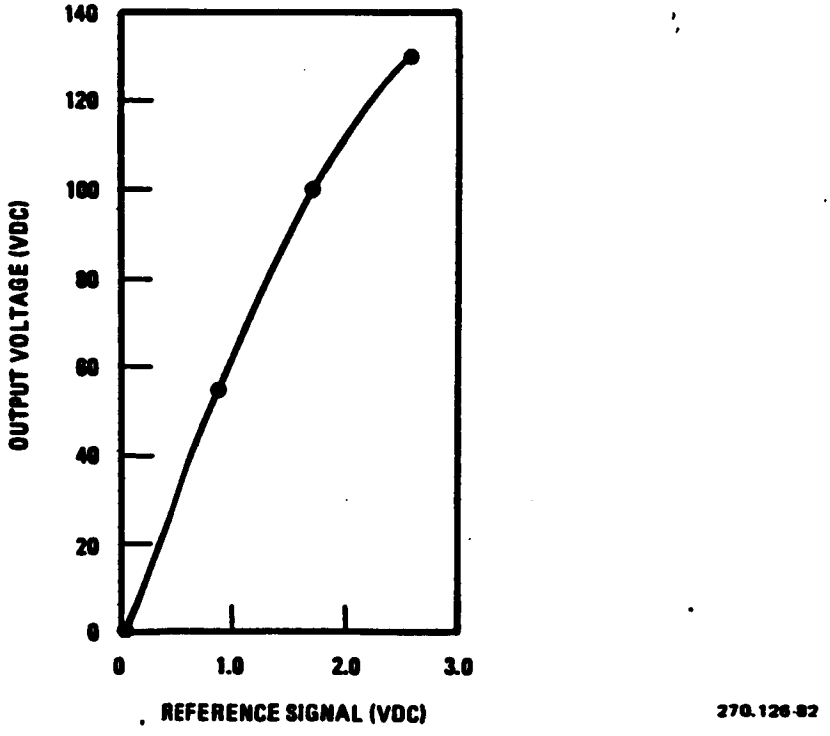

FIGURE 4.4-5. CONTROL SIGNAL GAIN OF THE BIDIRECTIONAL MODULE

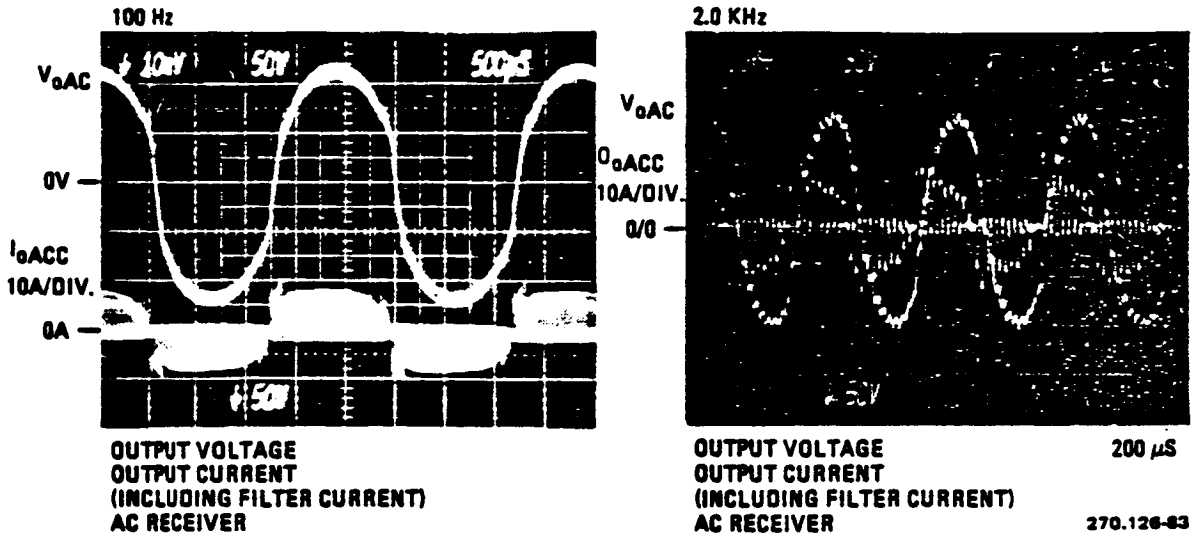

FIGURE 4.4-6. THE AC RECEIVER WITH A 100HZ AND 2.0KHZ REFERENCE SIGNAL

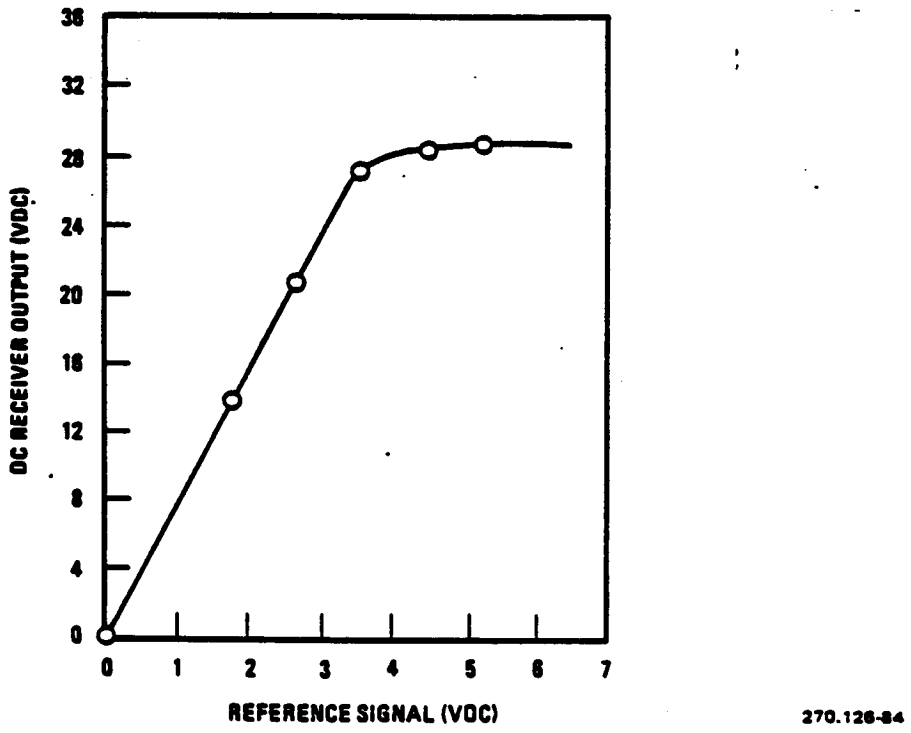

FIGURE 4.4-7. CONTROL SIGNAL GAIN OF THE DC RECEIVER

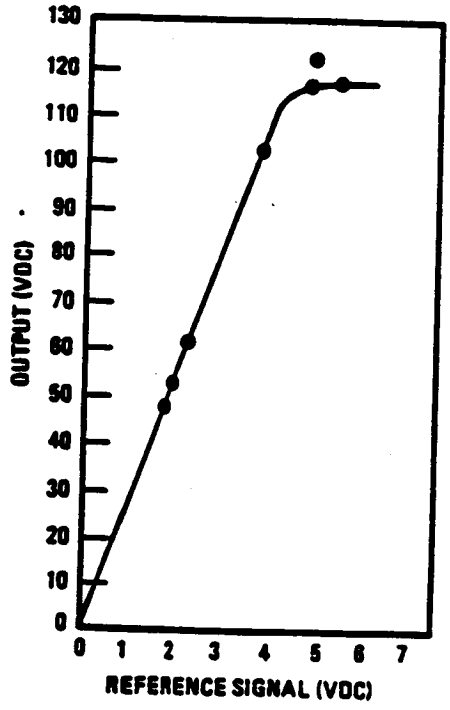

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FIGURE 4.4-8. CONTROL SIGNAL GAIN OF THE BIDIRECTIONAL MODULE

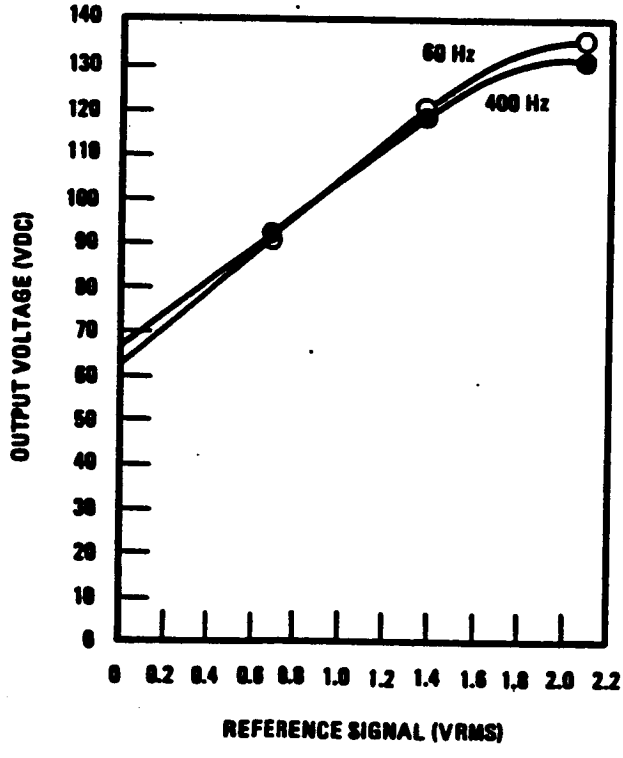

FIGURE 4.4-9. AC RECEIVER CONTROL SIGNAL GAIN

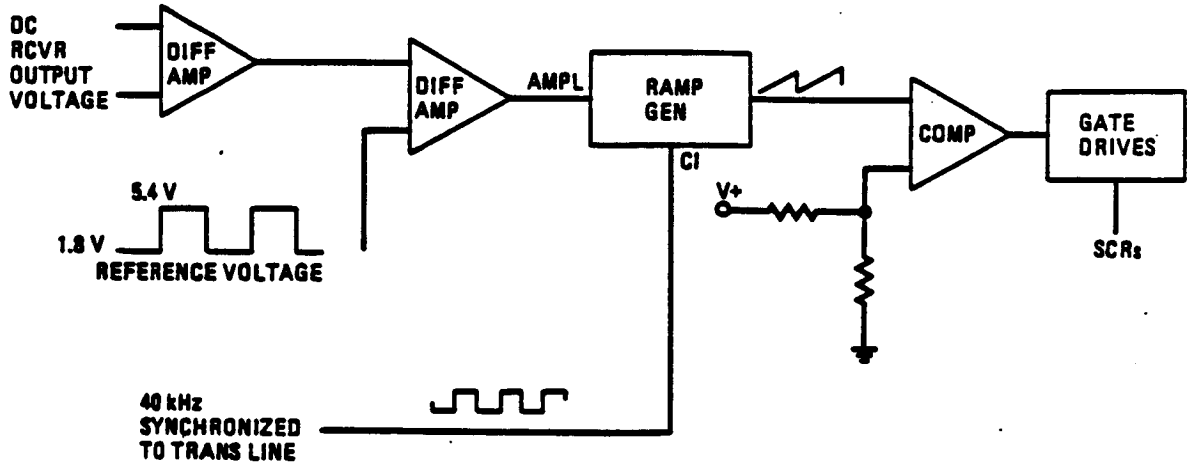

FIGURE 4.4-10. SIMPLIFIED DC RECEIVER CONTROL CIRCUIT BLOCK DIAGRAM AND TEST SIGNALS

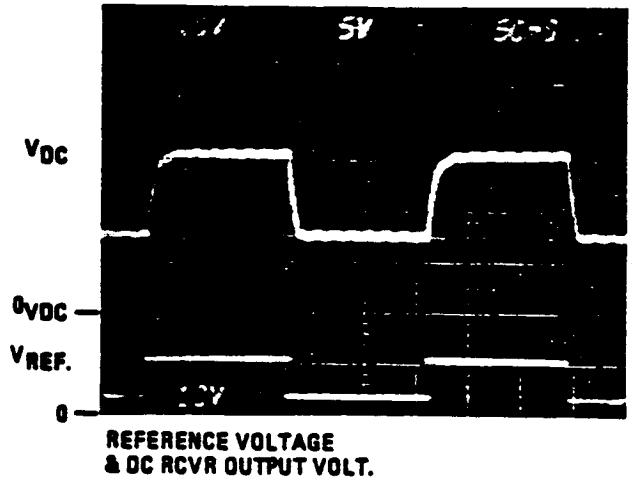

FIGURE 4.4-11. REFERENCE SIGNAL AND THE DC RECEIVER OUTPUT VOLTAGE

C-3

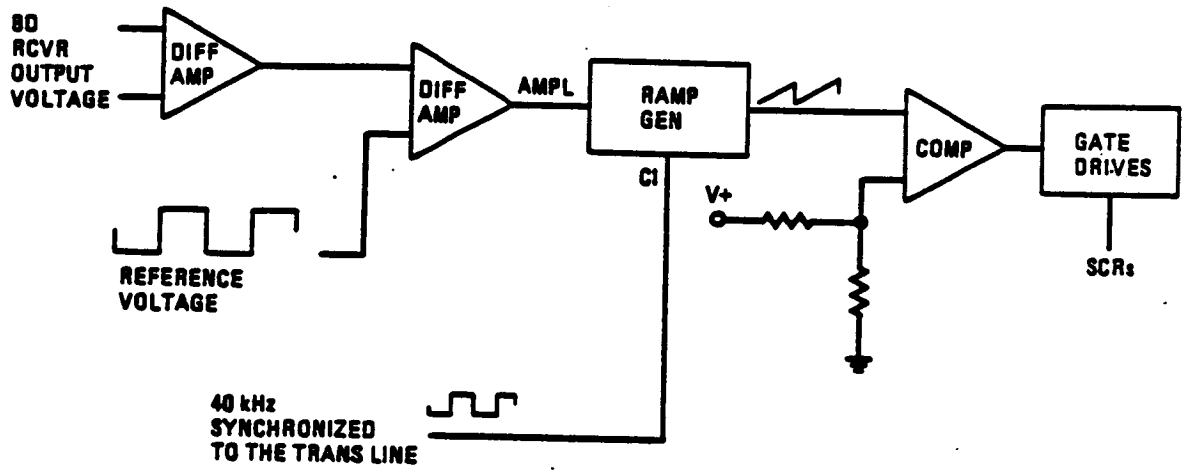

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FIGURE 4.4-12. SIMPLIFIED BIDIRECTIONAL MODULE CONTROL CIRCUIT SHOWING TEST SIGNALS

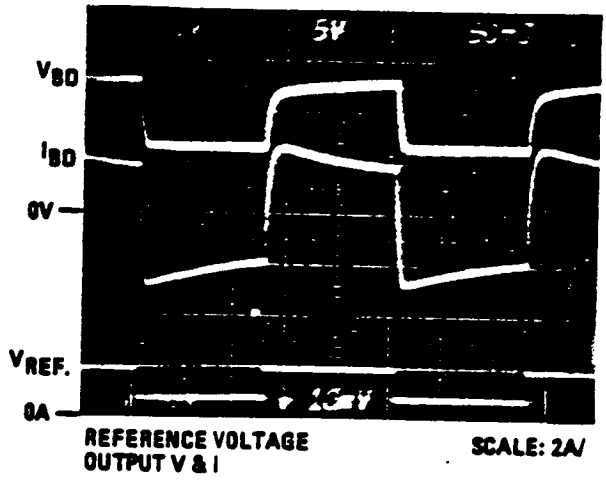

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FIGURE 4.4-13. REFERENCE SIGNAL AND BIDIRECTIONAL MODULE OUTPUT VOLTAGE

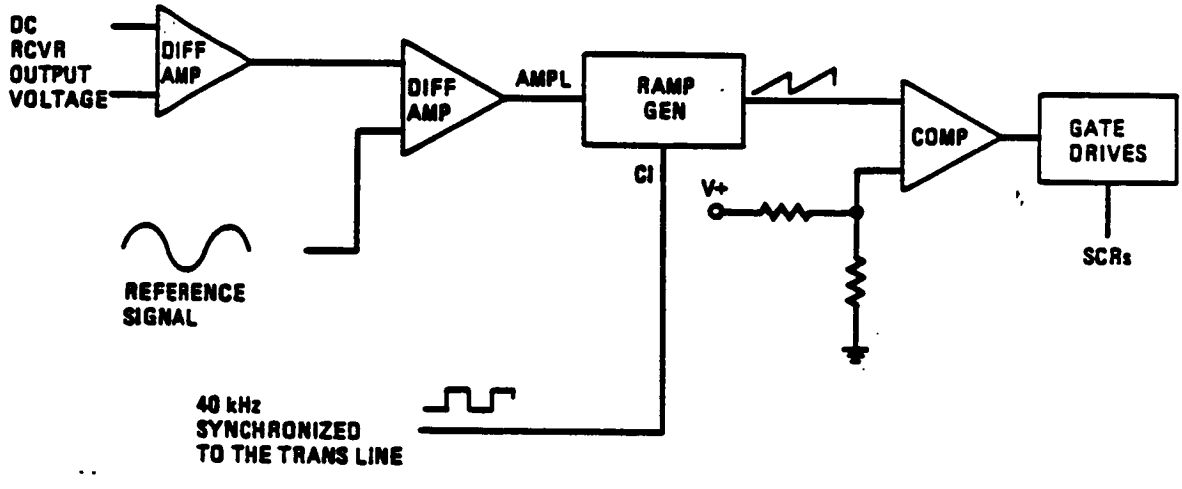
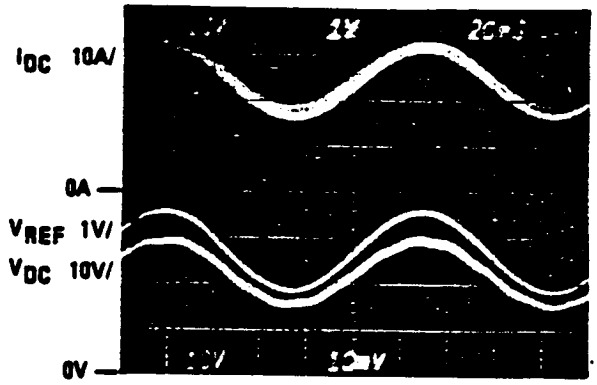
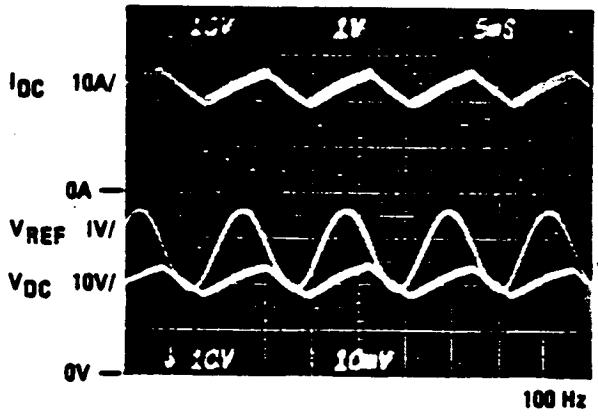


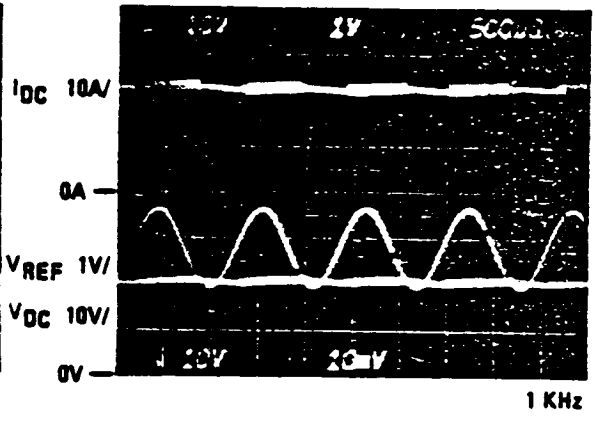
FIGURE 4.4-14. TEST CIRCUIT FOR FREQUENCY RESPONSE MEASUREMENTS ON THE DC RECEIVER



DC RCVR OUTPUT VOLTAGE
& CURRENT AND REFERENCE VOLTAGE



DC RCVR OUTPUT VOLTAGE & CURRENT
AND REFERENCE VOLTAGE



DC RCVR OUTPUT VOLTAGE & CURRENT
AND REFERENCE VOLTAGE

270.126-62

FIGURE 4.4-15. DC RECEIVER OUTPUT WAVEFORMS WITH 10HZ, 100HZ, AND 1.0KHZ MODULATION OF THE REFERENCE SIGNAL

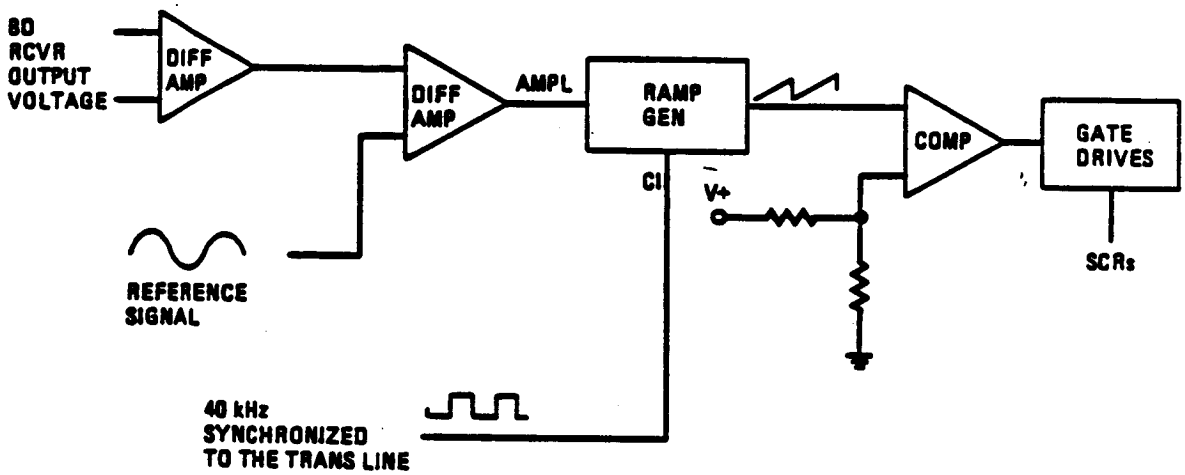


FIGURE 4.4-16. CIRCUIT USED TO MEASURE THE FREQUENCY RESPONSE OF THE BIDIRECTIONAL MODULE

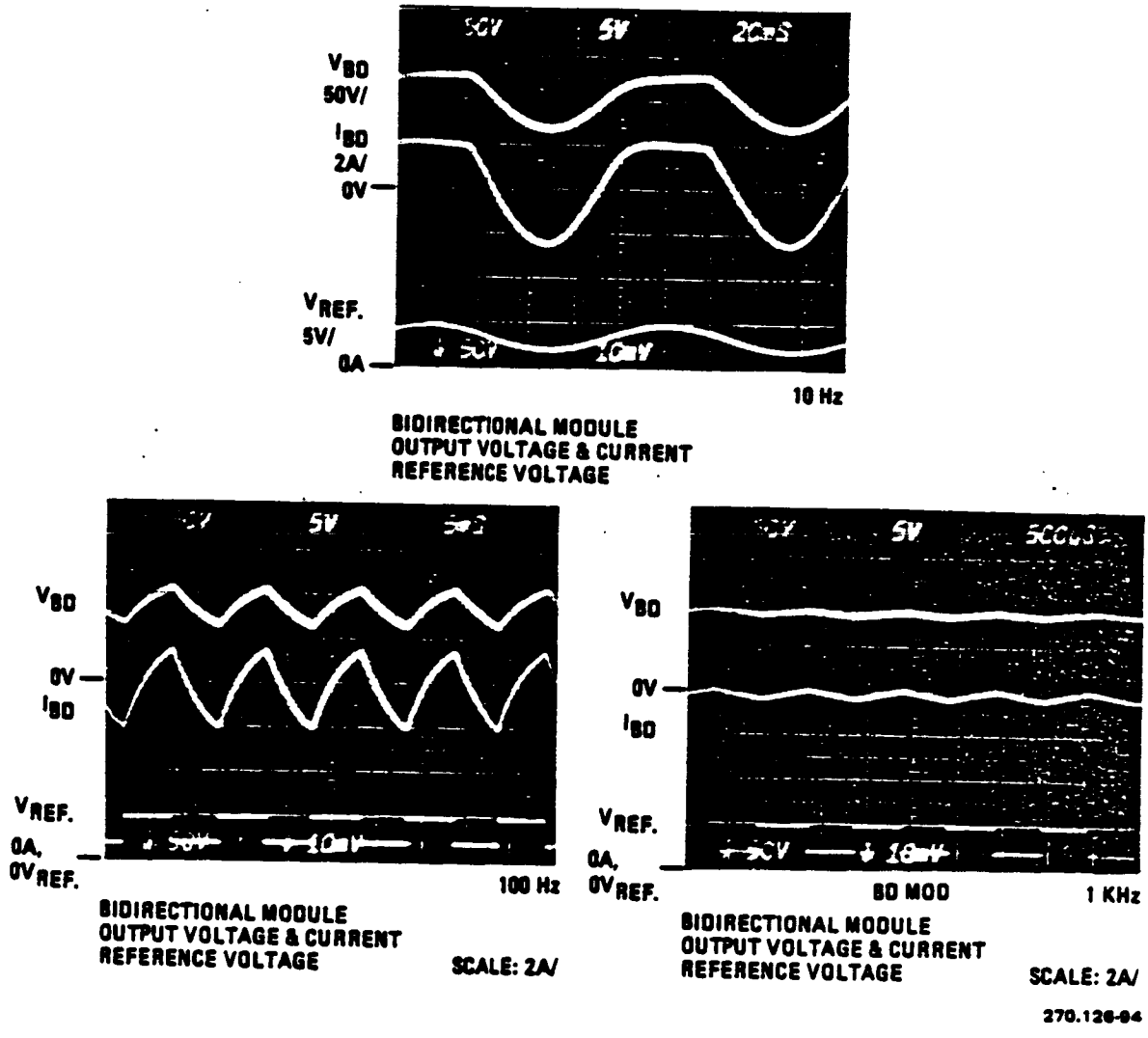


FIGURE 4.4-17. OUTPUT WAVEFORMS OF THE BIDIRECTIONAL MODULE WITH 10HZ, 100HZ, AND 1.0KHZ MODULATION OF THE REFERENCE SIGNAL

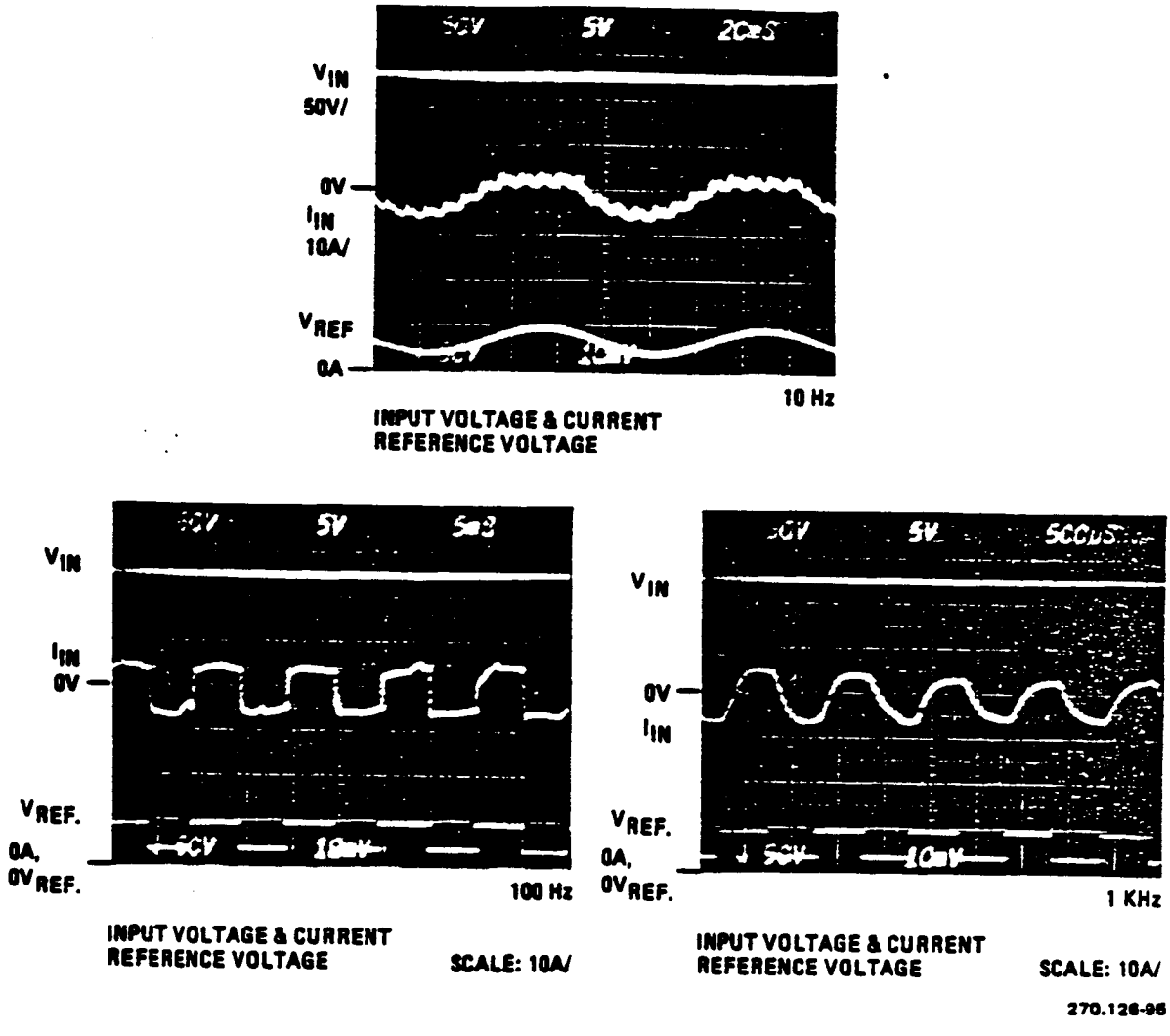


FIGURE 4.4-18. INPUT WAVEFORMS WITH THE REFERENCE SIGNAL OF THE BIDIRECTIONAL MODULE MODULATED BY 10HZ, 100HZ, AND 1.0KHZ SIGNALS

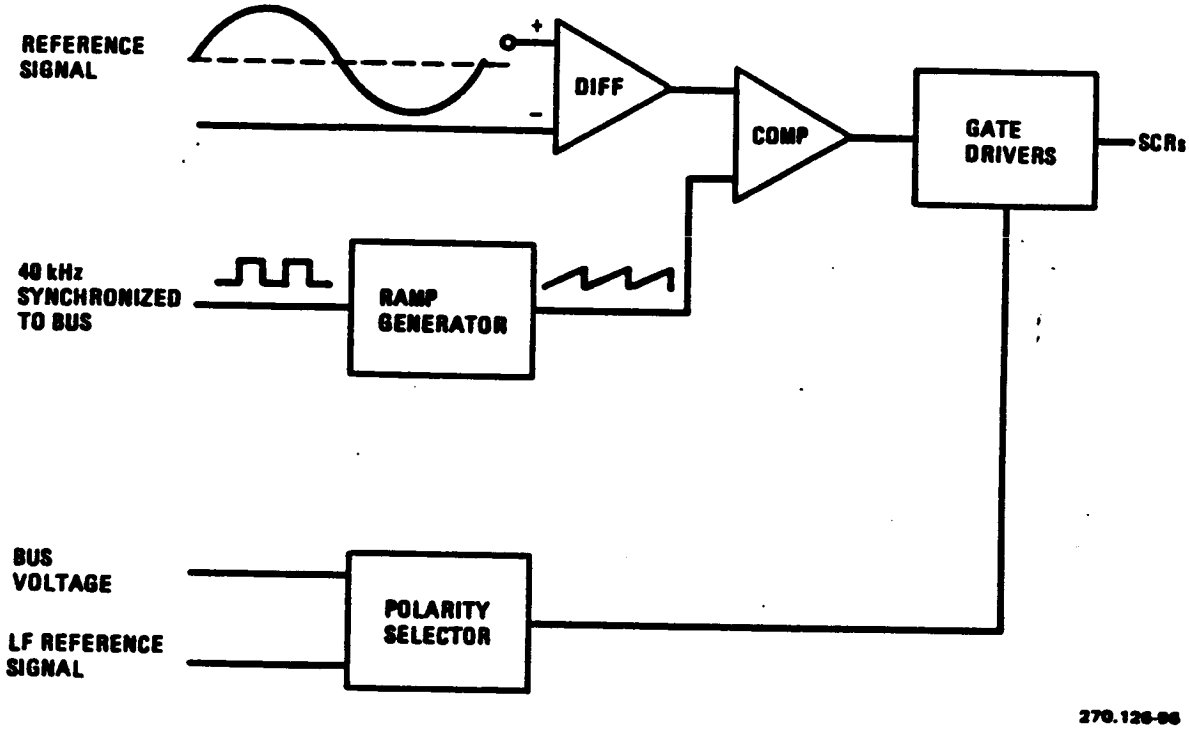


FIGURE 4.4-19. VARIABLE-FREQUENCY, VARIABLE-VOLTAGE RECEIVER CONTROLLER SCHEMATIC

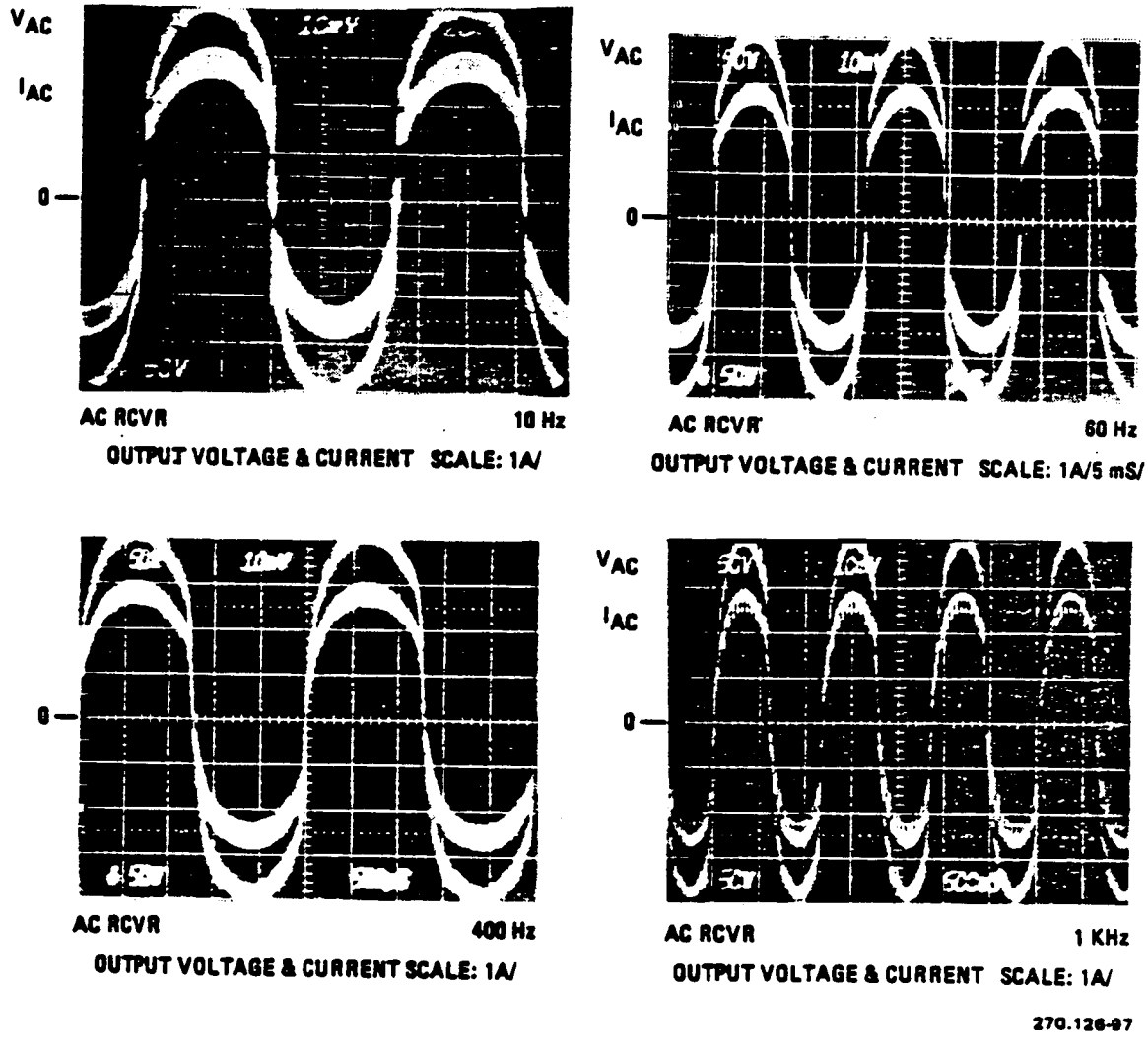


FIGURE 4.4-20. OUTPUT OF THE VARIABLE-FREQUENCY, VARIABLE VOLTAGE RECEIVER WHILE OPERATING AT 10HZ, 60HZ, 400HZ, AND 1.0KHZ

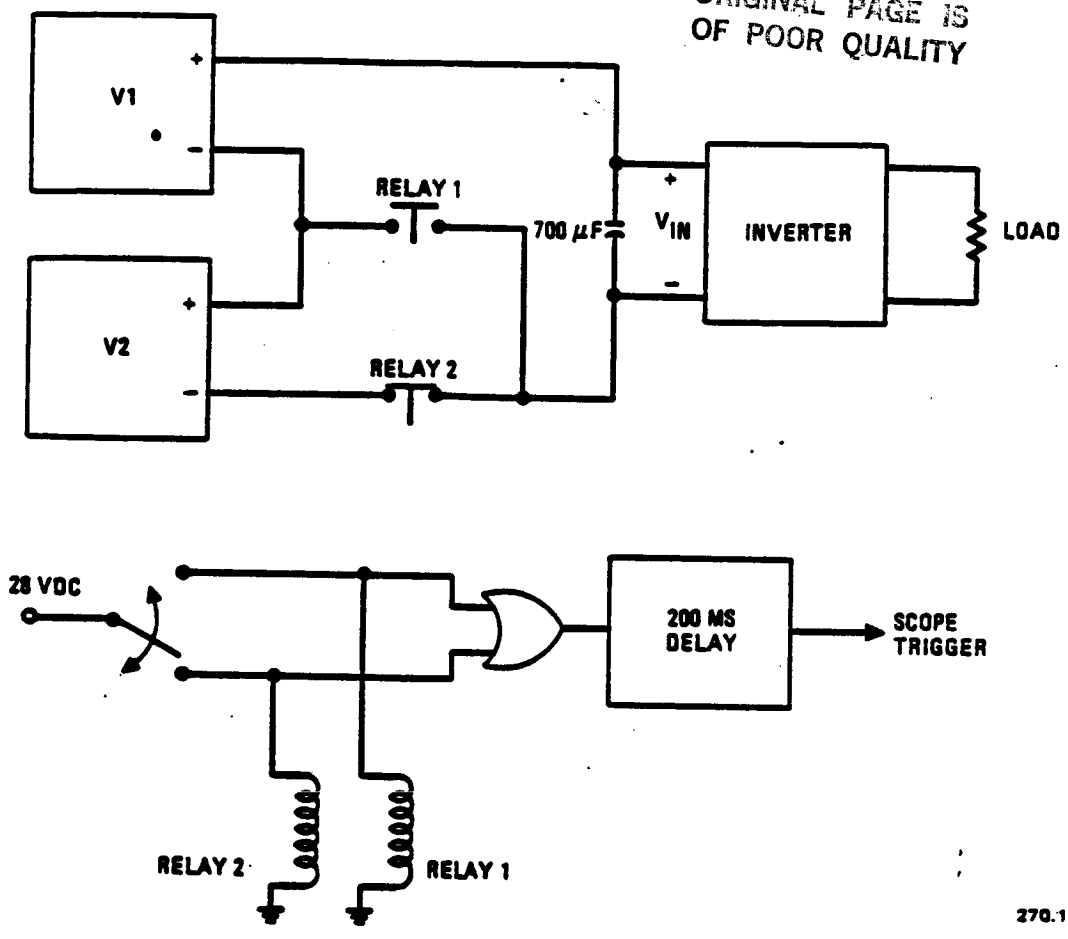


FIGURE 4.5-1. TEST CIRCUIT FOR POWER SUPPLY SENSITIVITY MEASUREMENTS OF THE DRIVER

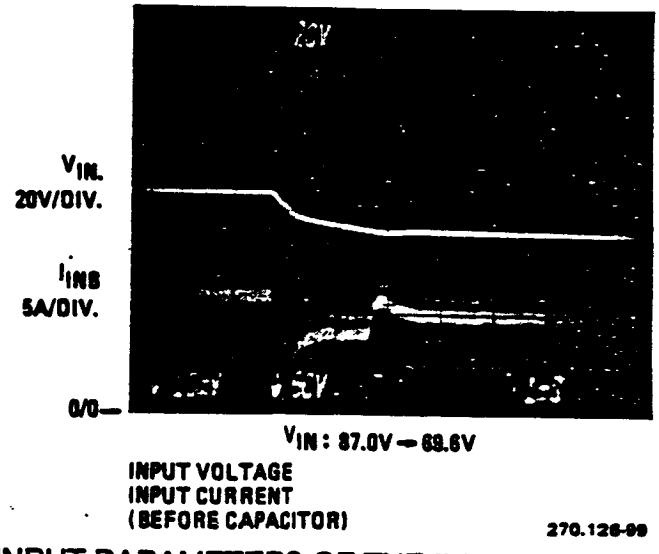
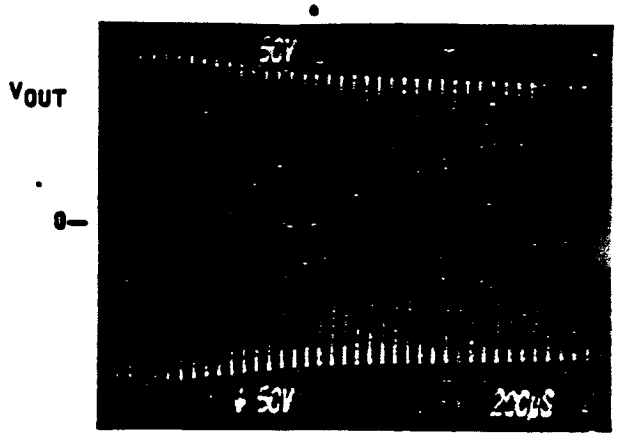


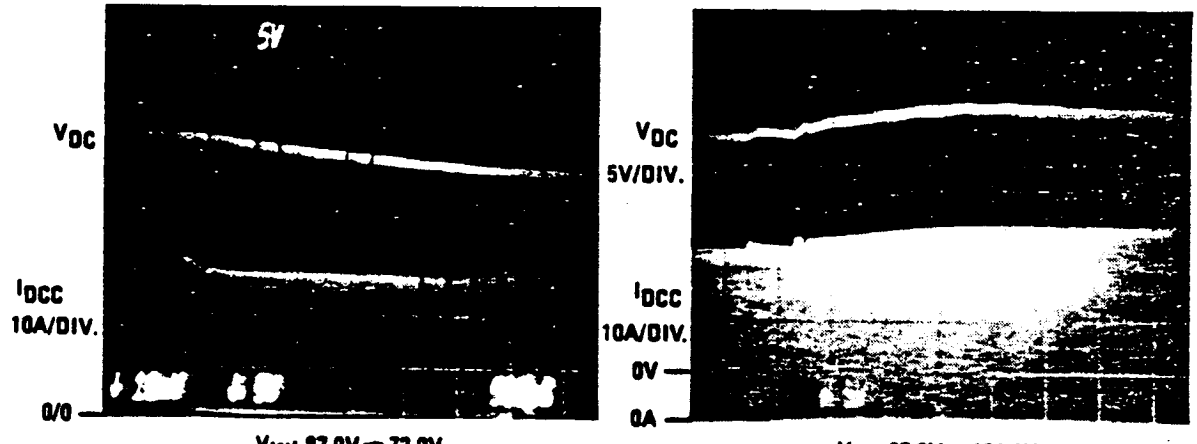
FIGURE 4.5-2. INPUT PARAMETERS OF THE INVERTER AS THE INPUT VOLTAGE IS SWITCHED FROM 87.0VDC TO 69.6VDC



OUTPUT VOLTAGE

270.126-100

FIGURE 4.5-3. INVERTER OUTPUT VOLTAGE AS THE INPUT VOLTAGE IS SWITCHED FROM 87.0VDC TO 69.6VDC



OUTPUT VOLTAGE
OUTPUT CURRENT
(INCLUDING FILTER CURRENT)

OUTPUT VOLTAGE
OUTPUT CURRENT
(INCLUDING FILTER CURRENT)

270.126-101

FIGURE 4.5-4. OUTPUT VOLTAGE OF THE DC RECEIVER AS THE INPUT VOLTAGE IS SWITCHED FROM 87.0VDC TO 72.0VDC AND 87.0 TO 104.4VDC

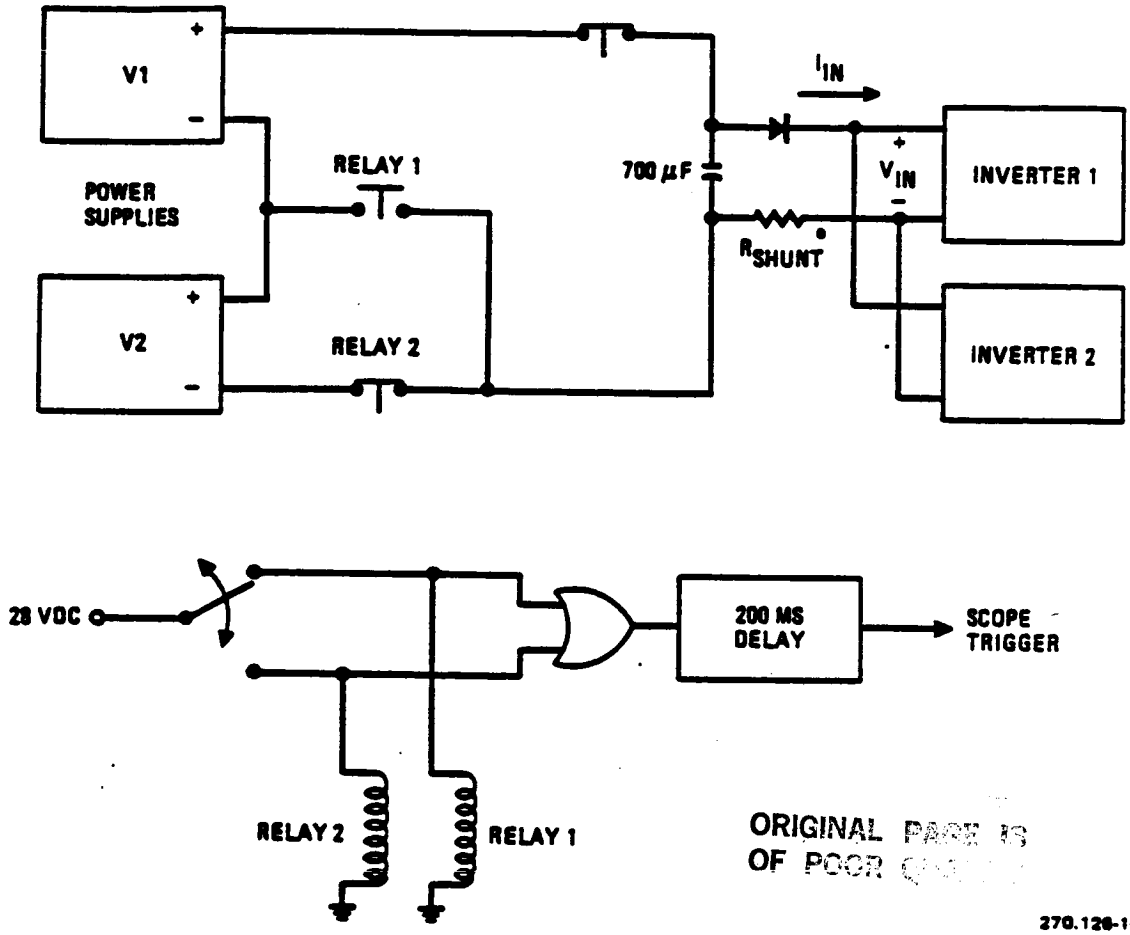


FIGURE 4.5-5. TEST CIRCUIT USED TO MEASURE THE POWER SUPPLY SENSITIVITY OF THE SINGLE-PHASE SYSTEM

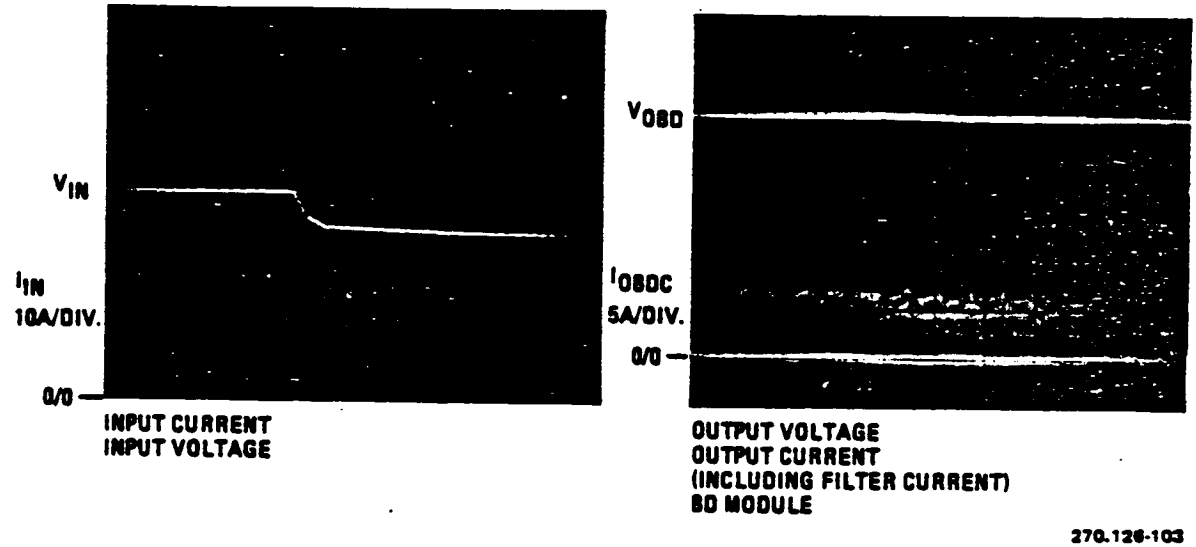


FIGURE 4.5-6. SYSTEM INPUT VOLTAGE AND BIDIRECTIONAL MODULE OUTPUT VOLTAGE FOR AN INPUT VOLTAGE CHANGE FROM 85VDC TO 68VDC

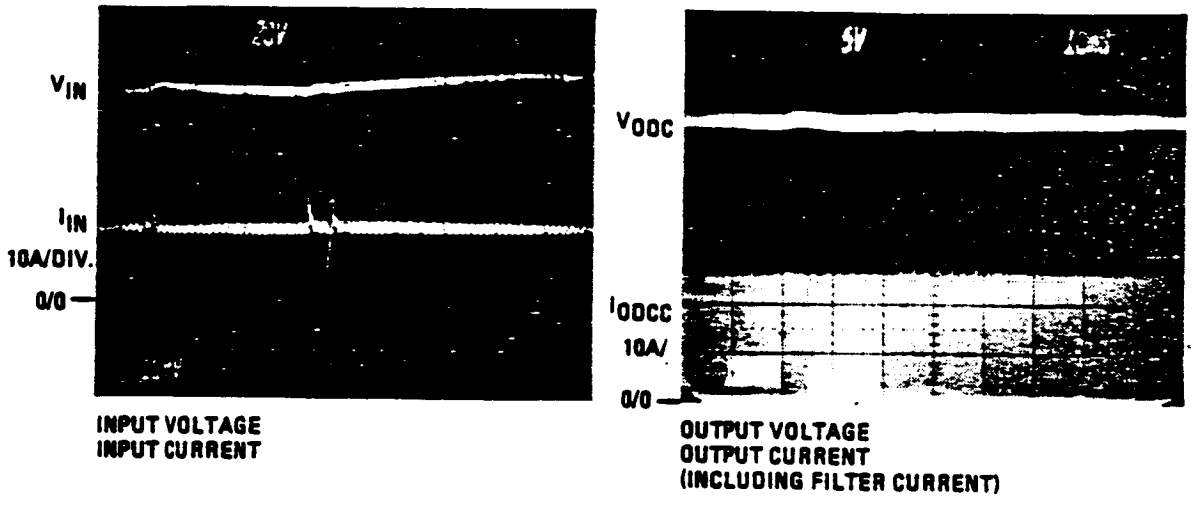


FIGURE 4.5-7. SYSTEM INPUT VOLTAGE AND DC RECEIVER OUTPUT VOLTAGE AS THE INPUT IS SWITCHED FROM 85VDC TO 102VDC

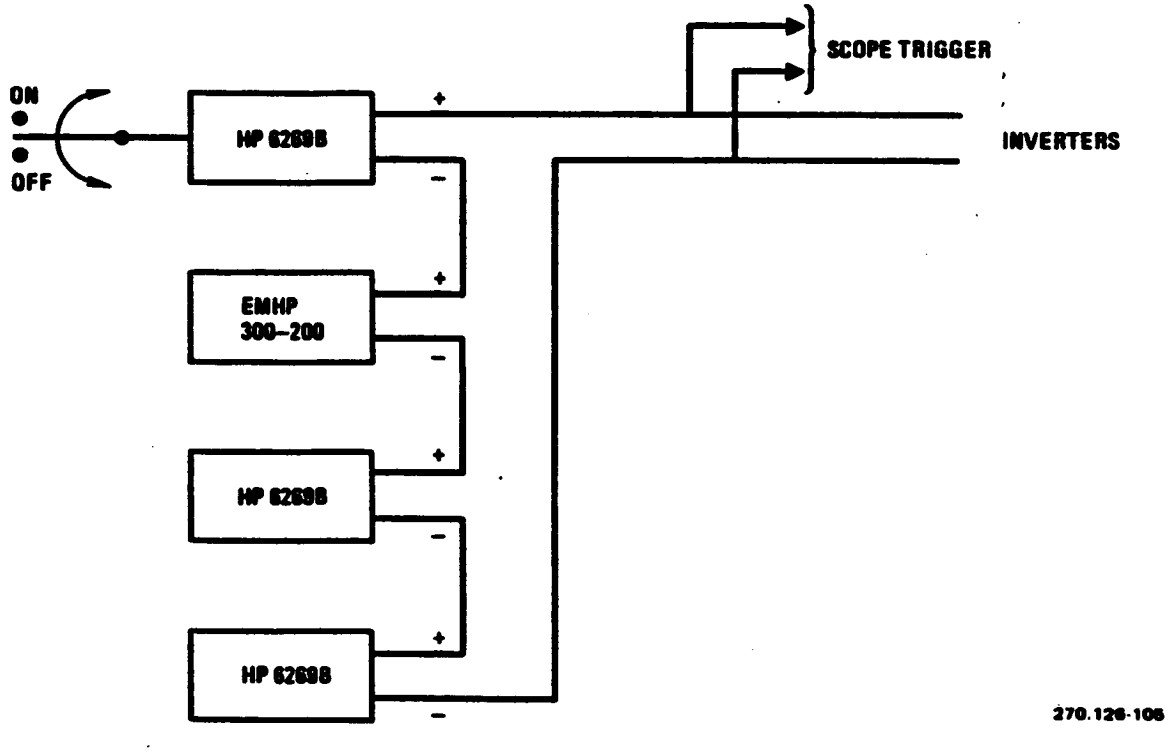


FIGURE 4.5-8. TEST SET UP FOR THE POWER SUPPLY SENSITIVITY MEASUREMENTS FOR THE THREE-PHASE SYSTEM

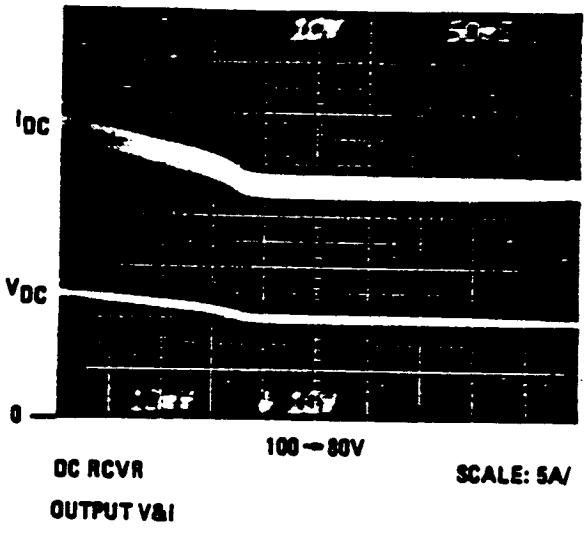


FIGURE 4.5-9. DC RECEIVER OUTPUT AS THE SYSTEM INPUT IS SWITCHED FROM 100VDC TO 80VDC

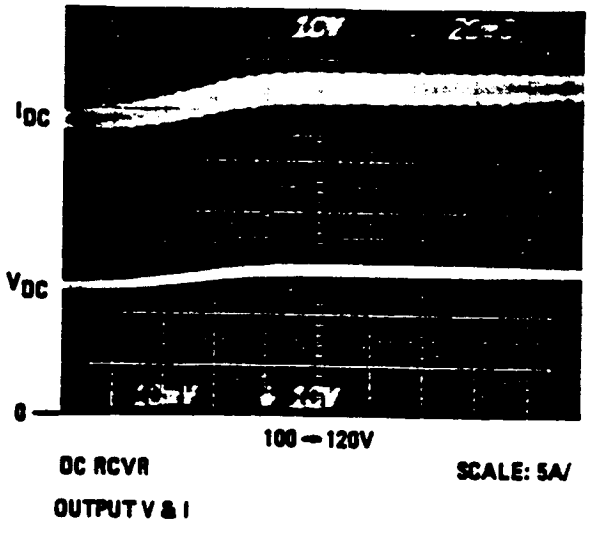


FIGURE 4.5-10. OUTPUT OF THE DC RECEIVER AS THE SYSTEM INPUT VOLTAGE LEVEL IS SWITCHED FROM 100VDC TO 120VDC

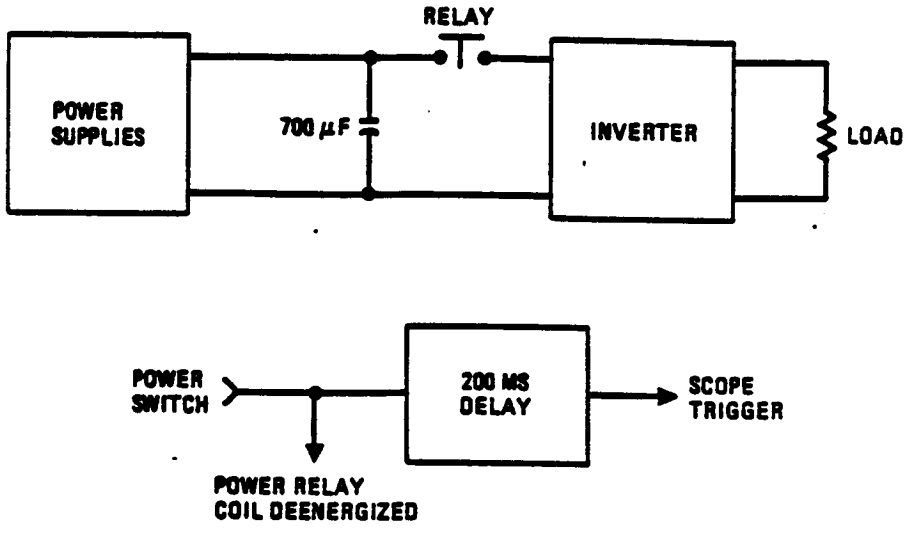


FIGURE 4.6-1. CIRCUIT USED TO GATHER DATA FOR THE SINGLE-INVERTER CASE OF POWER TURN OFF

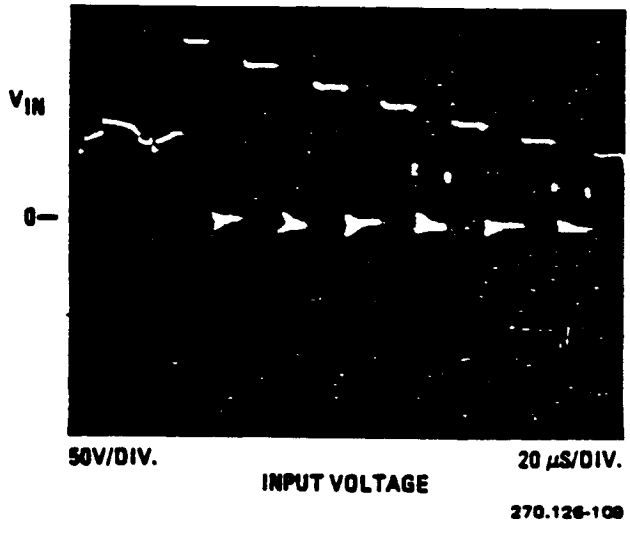


FIGURE 4.6-2. INPUT VOLTAGE AS THE POWER IS TURNED OFF

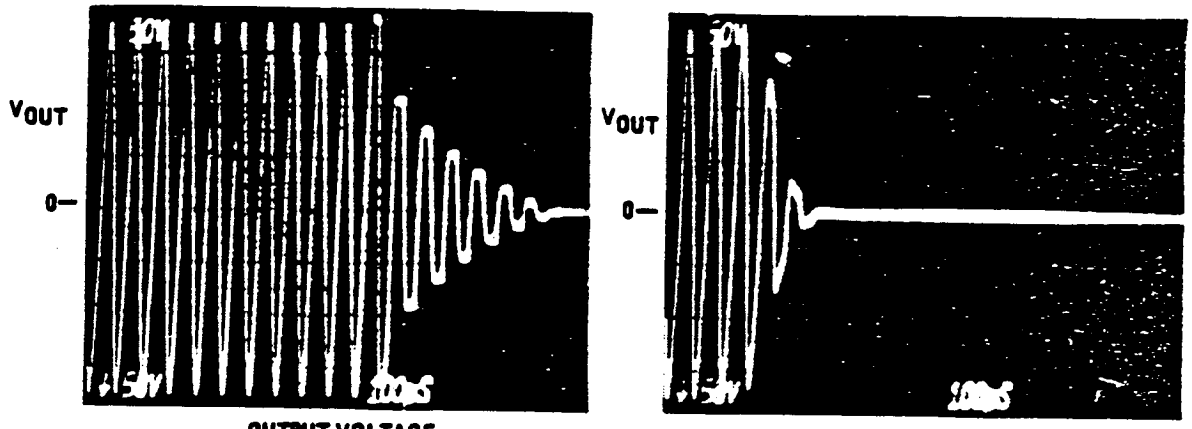


FIGURE 4.6-3. POWER TURN OFF OF A SINGLE INVERTER FOR THE 0.0 AND 580W CASES

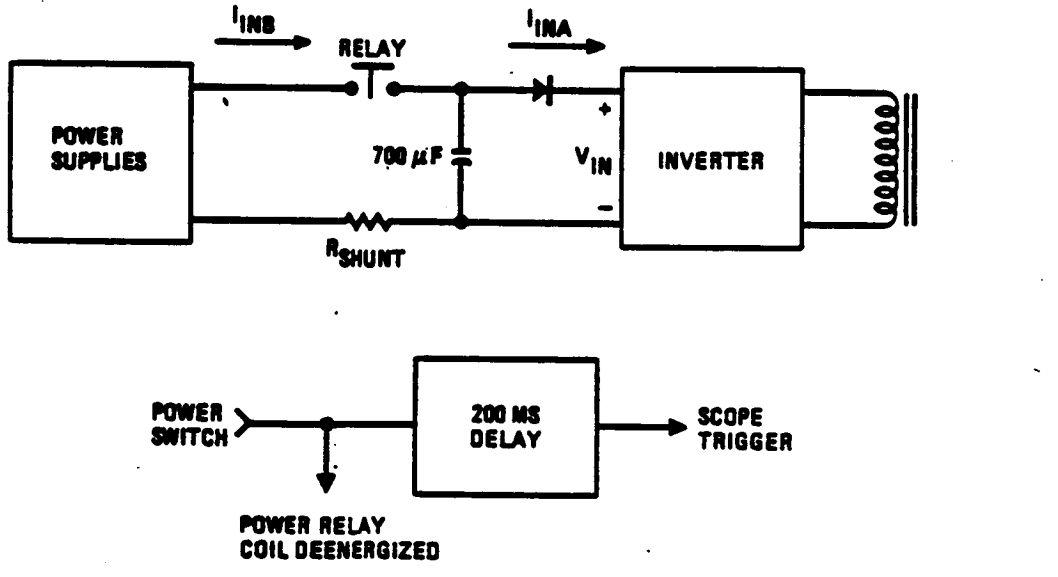


FIGURE 4.6-4. TEST CIRCUIT USED FOR THE POWER TURN OFF OF A SINGLE DRIVER AND RECEIVER

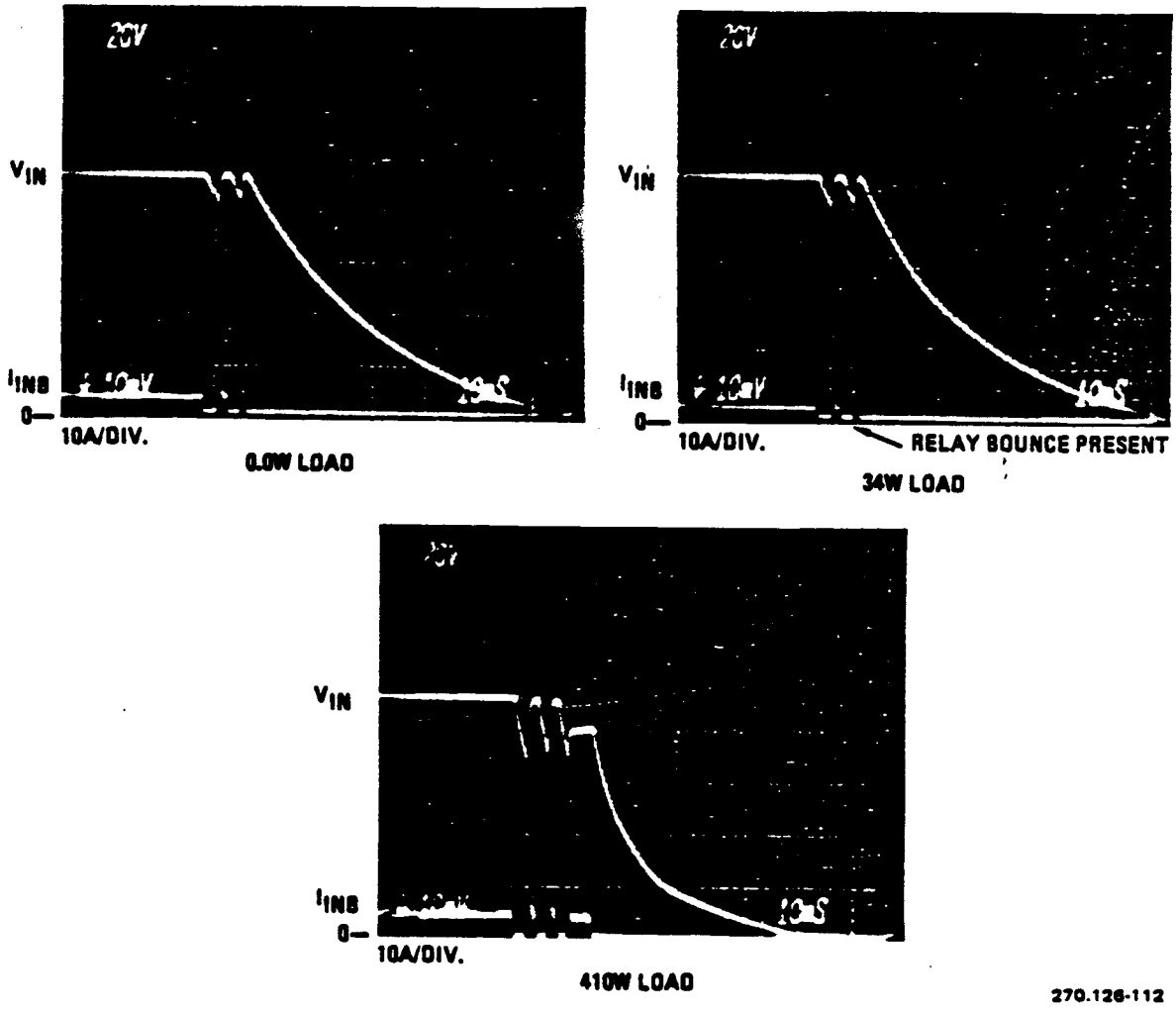


FIGURE 4.6-5. INPUT VOLTAGE AND RELAY CURRENT DURING POWER TURN OFF FOR A VARIETY OF DC RECEIVER LOADS

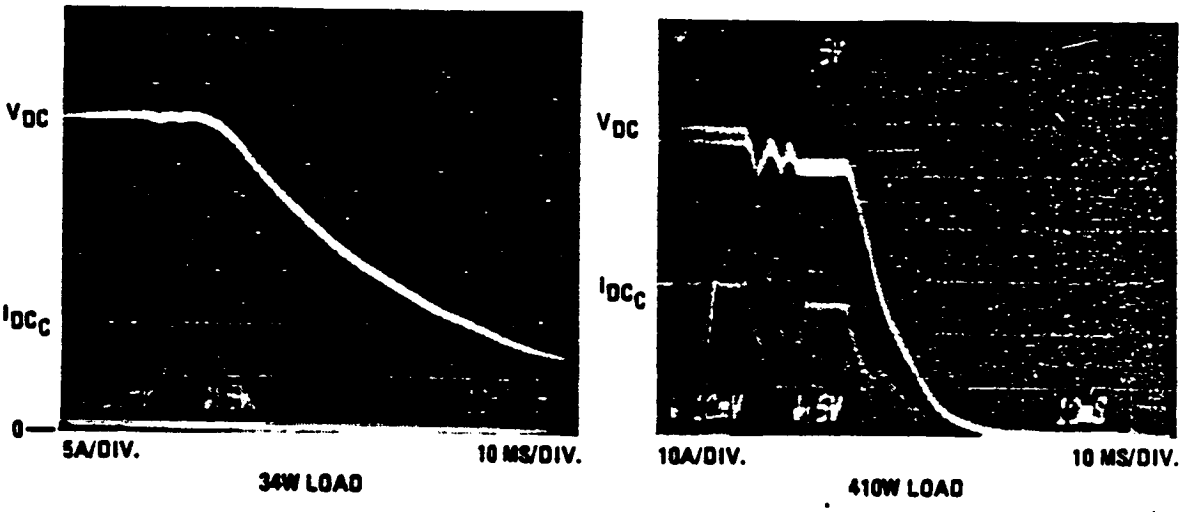


FIGURE 4.6-6. OUTPUT VOLTAGE AND FILTER CURRENT OF THE DC RECEIVER MODULE AS THE INPUT POWER IS REMOVED FOR TWO LOAD CONDITIONS

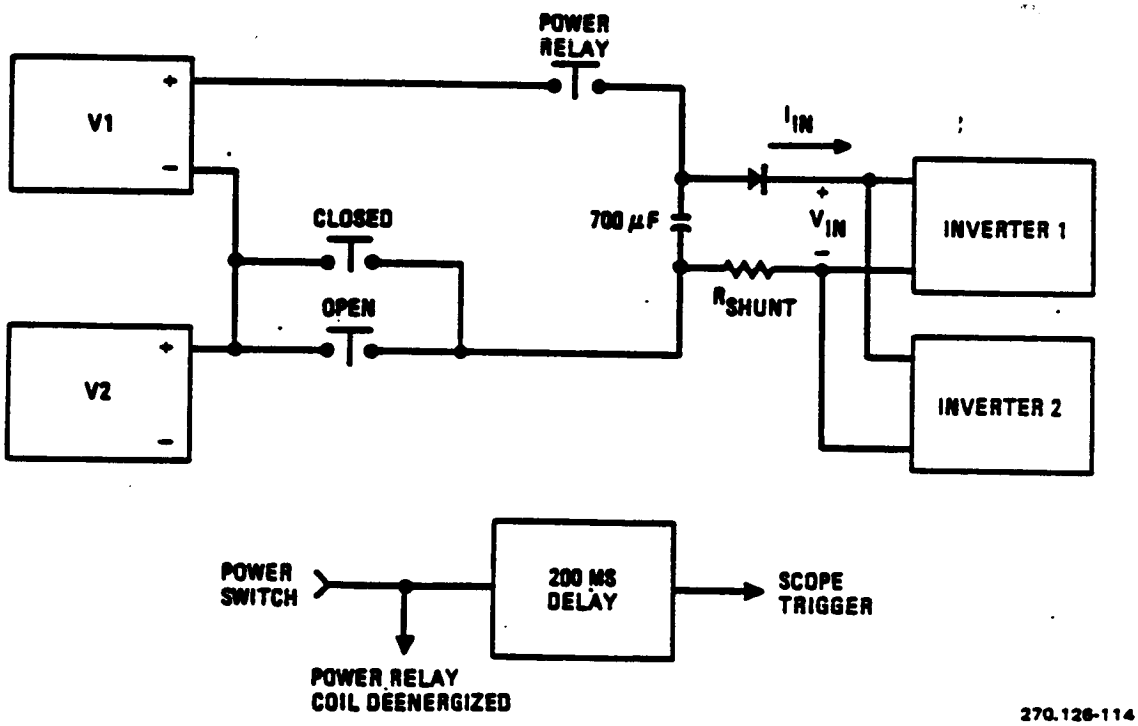


FIGURE 4.6-7. POWER TURN OFF TEST CIRCUIT FOR THE SINGLE-PHASE SYSTEM TEST CONFIGURATION

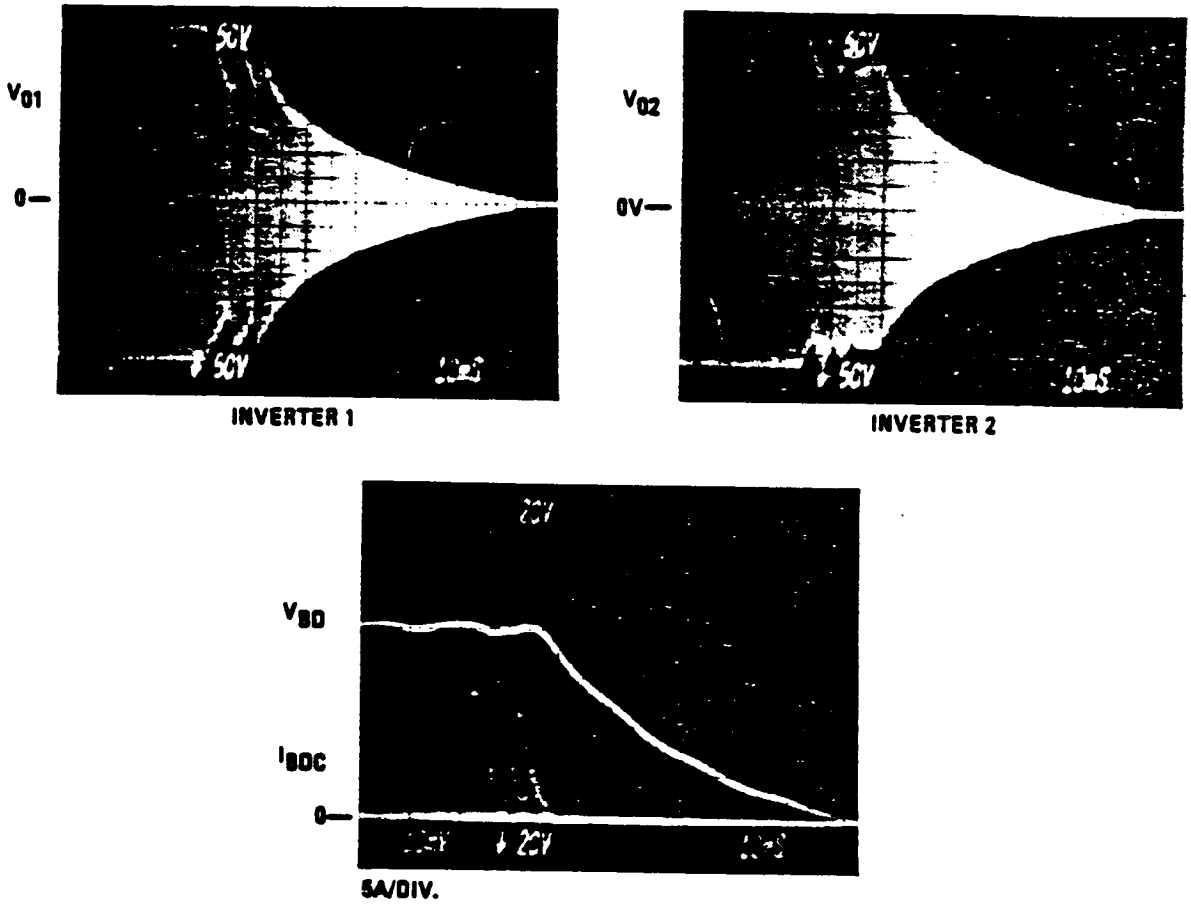


FIGURE 4.6-8. INVERTER OUTPUT VOLTAGES AND BIDIRECTIONAL MODULE OUTPUT VOLTAGE AND FILTER CURRENT DURING POWER TURN OFF

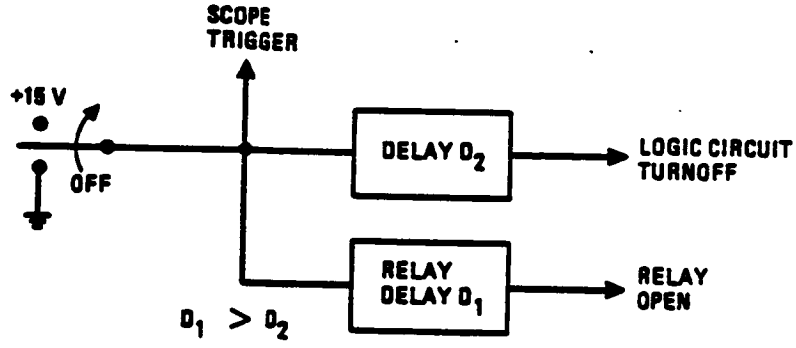


FIGURE 4.6-9. TIMING CIRCUIT TO OPEN SYSTEM INPUT RELAY FOR THE THREE-PHASE SYSTEM

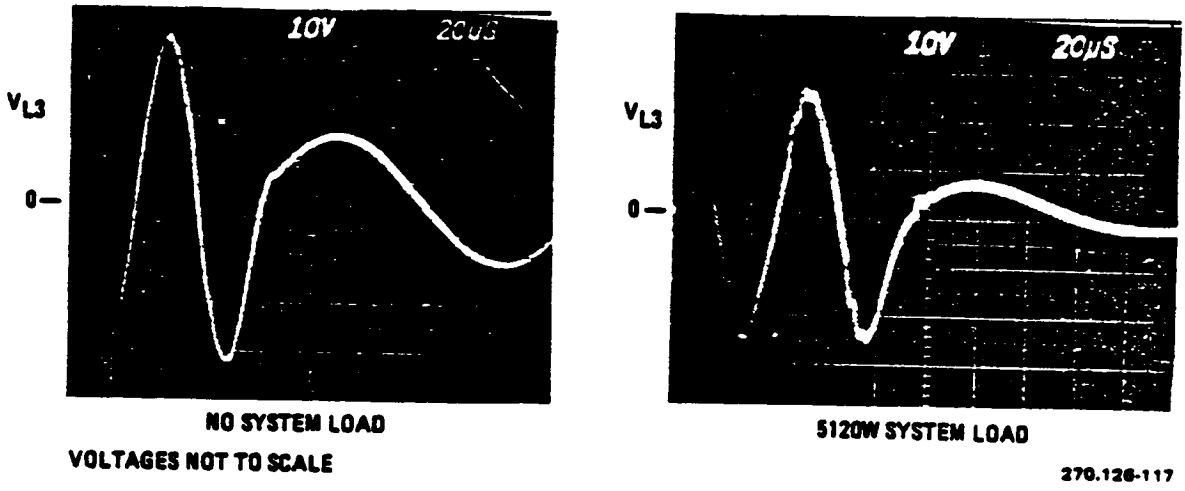


FIGURE 4.6-10. LINE-TO-NEUTRAL BUS VOLTAGE DURING POWER TURN OFF

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OF POOR QUALITY

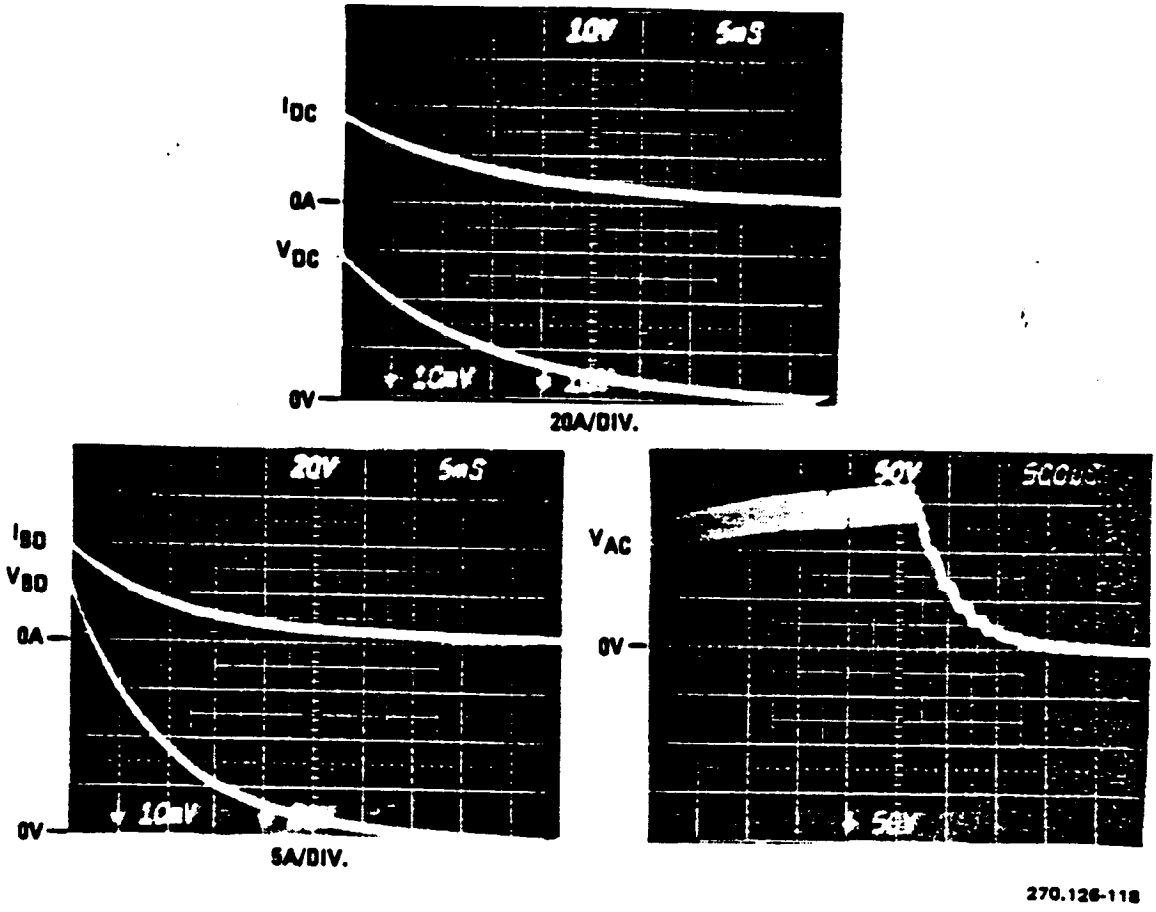
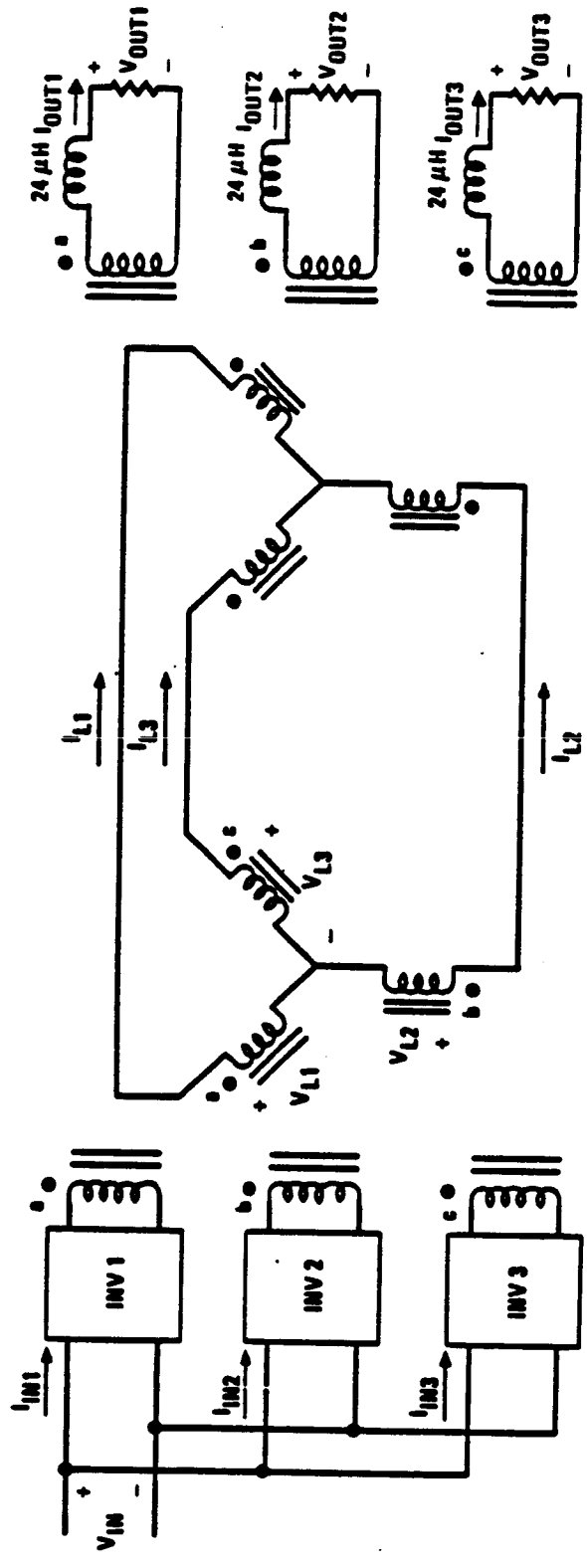


FIGURE 4.6-11. OUTPUTS OF THE RECEIVER MODULES DURING POWER TURN OFF

FIGURE 4.7-1. LEADING POWER FACTOR MEASUREMENT CIRCUIT



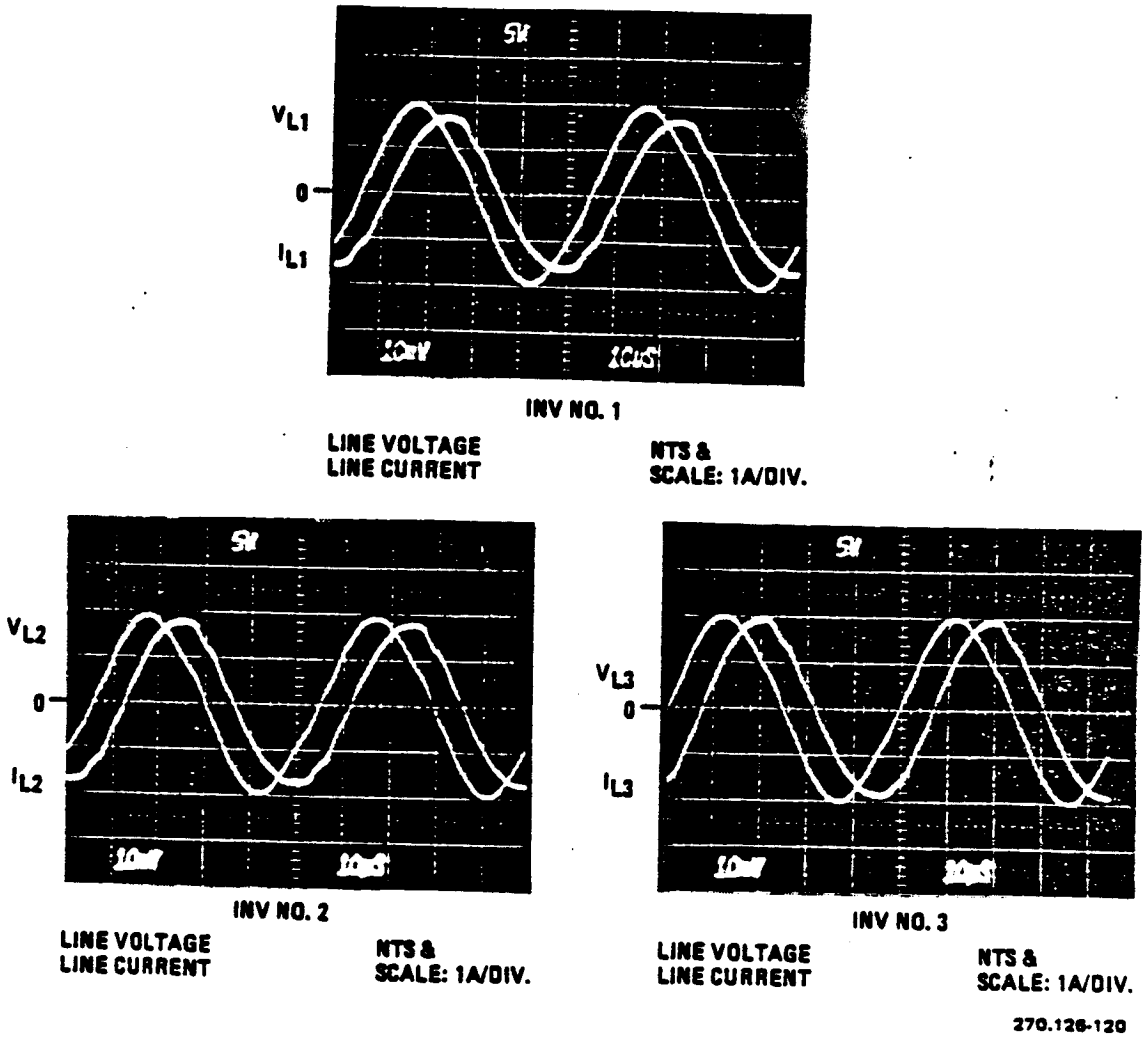


FIGURE 4.7-2. LINE VOLTAGES AND CURRENTS FOR LEADING POWER FACTOR

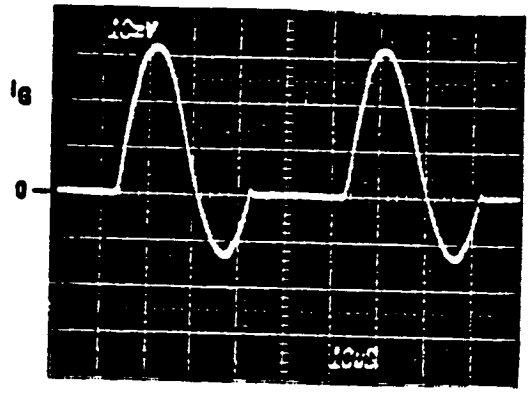


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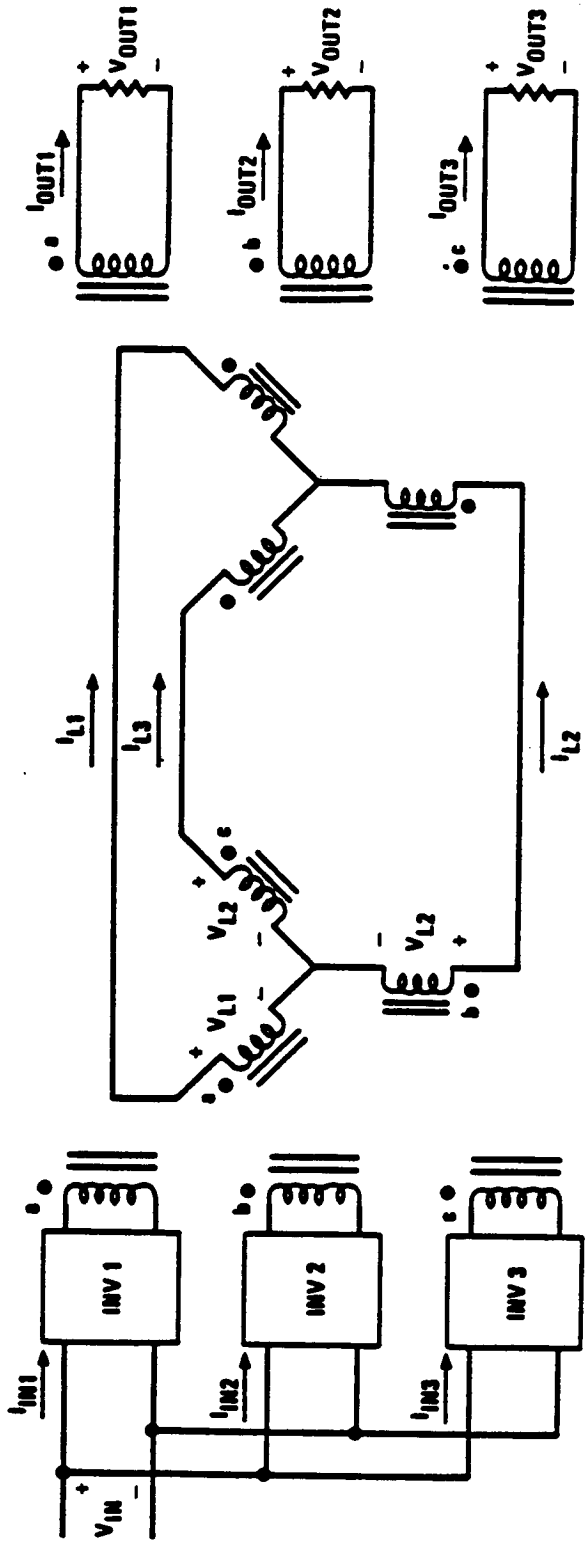
FIGURE 4.7-3. LEG CURRENT OF INVERTER NUMBER 3 WITH INDUCTIVE LOAD

FIGURE 4.7-4. SYSTEM ARRANGEMENT USED TO PRODUCE THE NOMINAL SYSTEM POWER FACTOR



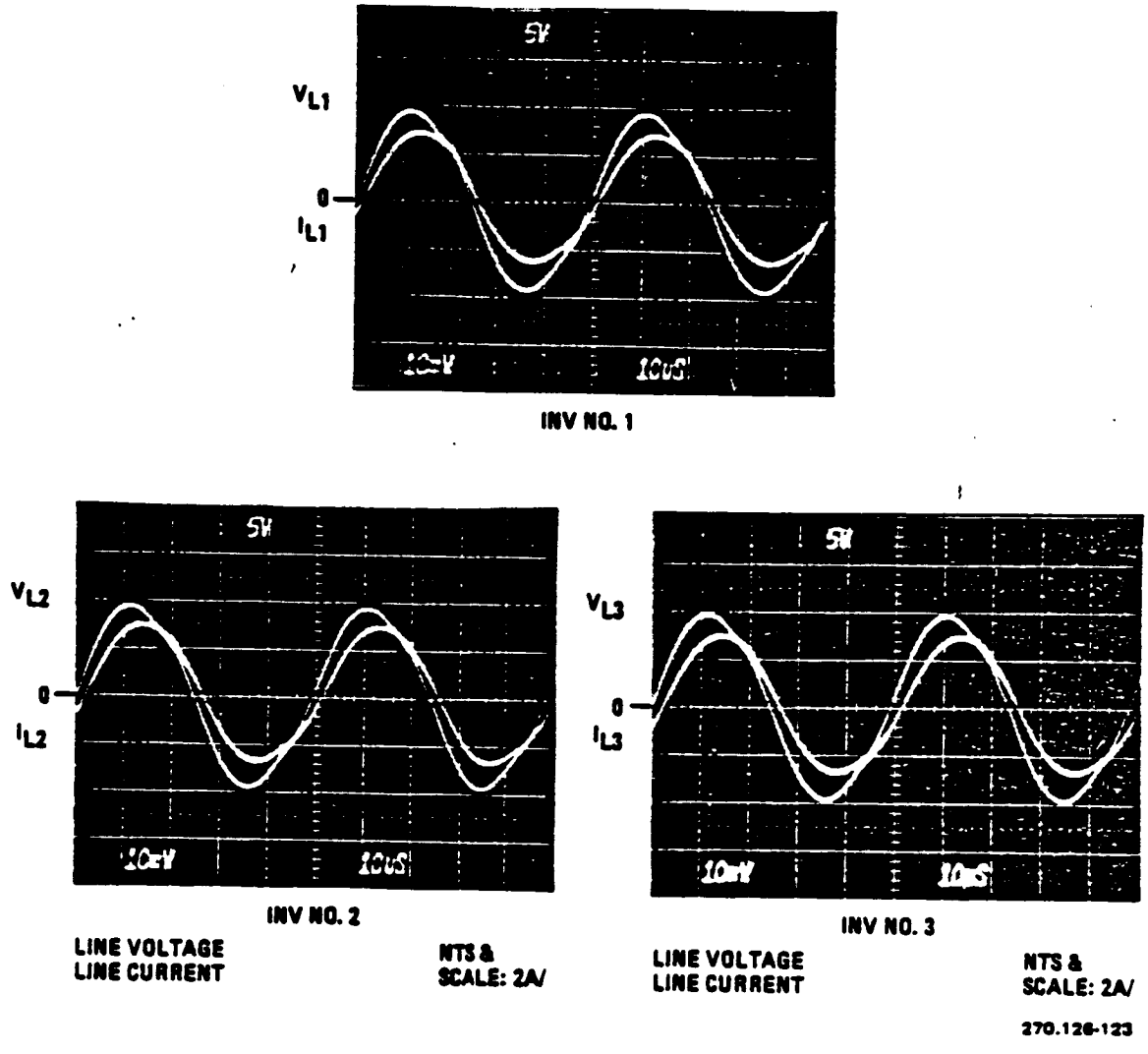


FIGURE 4.7-5. LINE VOLTAGES AND CURRENTS FOR NOMINAL POWER FACTOR CASE

ORIGINAL PAGE IS
OF POOR QUALITY

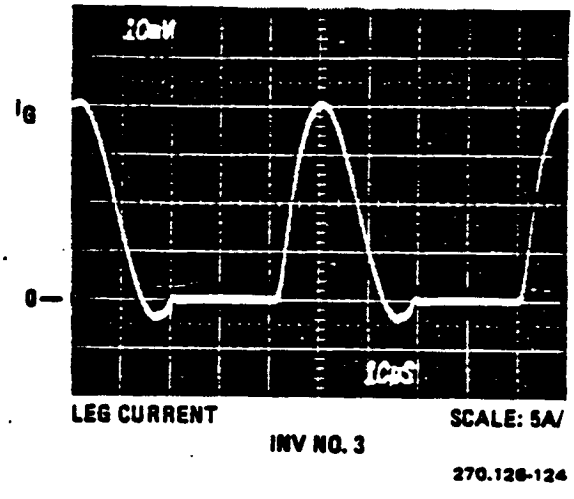
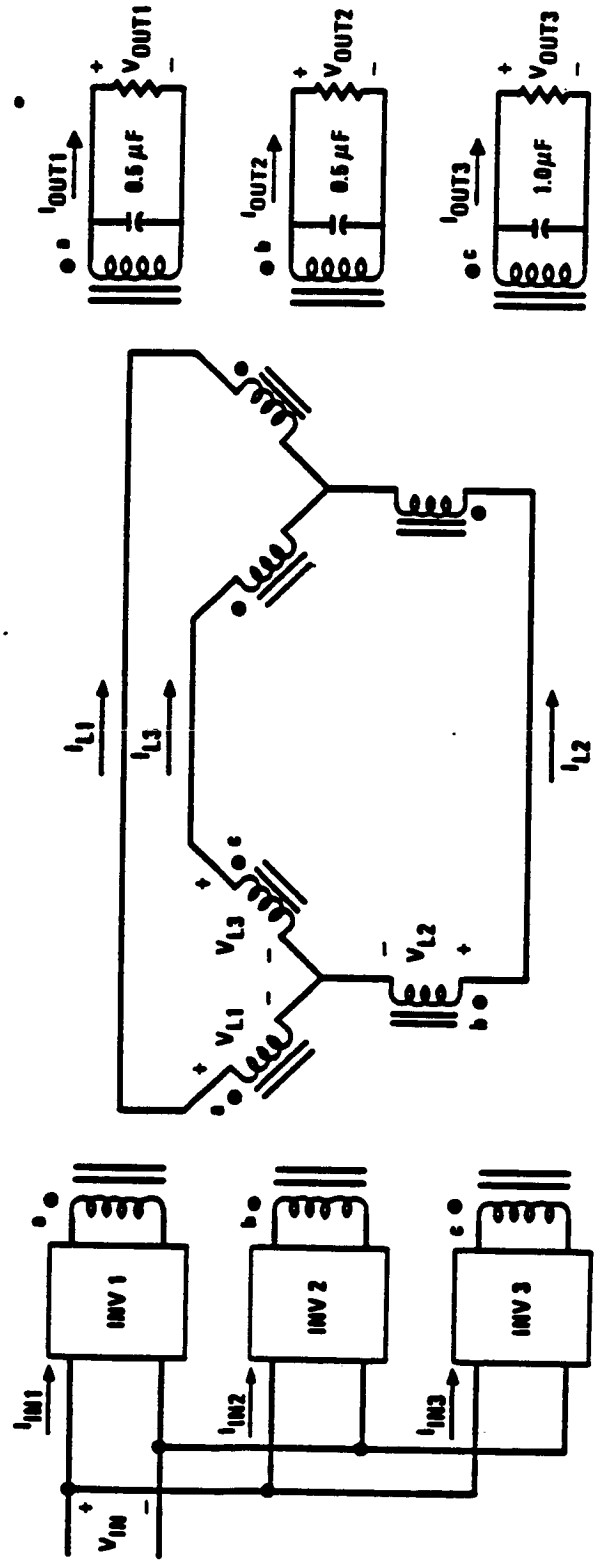


FIGURE 4.7-6. INVERTER NUMBER 3 LEG CURRENT FOR NOMINAL POWER FACTOR CASE

FIGURE 4.7-7. SYSTEM ARRANGEMENT TO PRODUCE UNITY POWER FACTOR ON THE BUS



ORIGINAL PAGE IS
OF POOR QUALITY

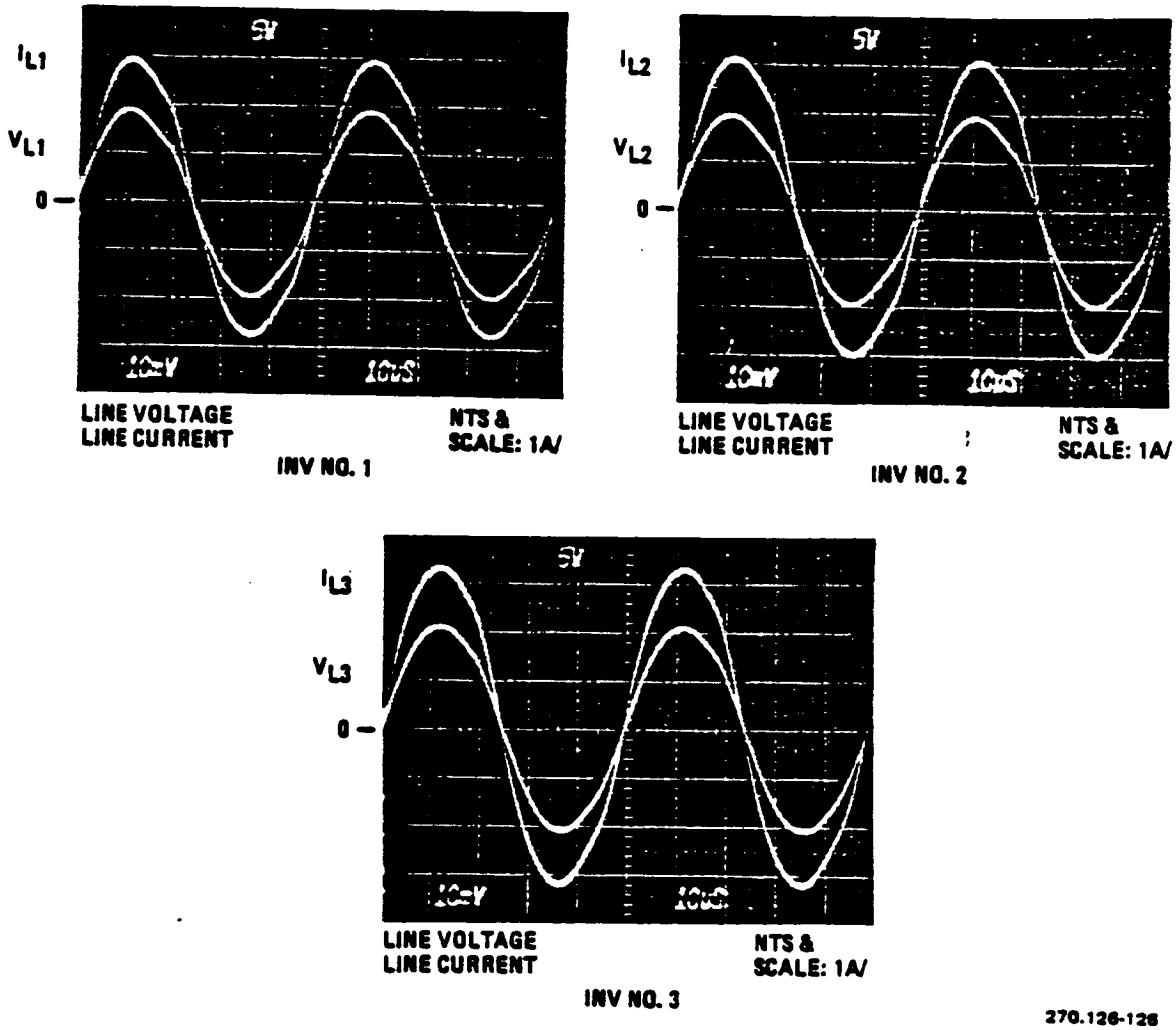


FIGURE 4.7-8. BUS VOLTAGES AND CURRENTS FOR THE UNITY BUS POWER FACTOR CASE

ORIGINAL PAGE IS
OF POOR QUALITY

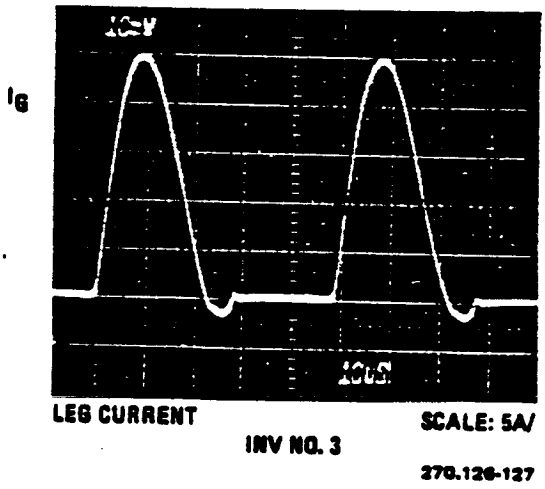
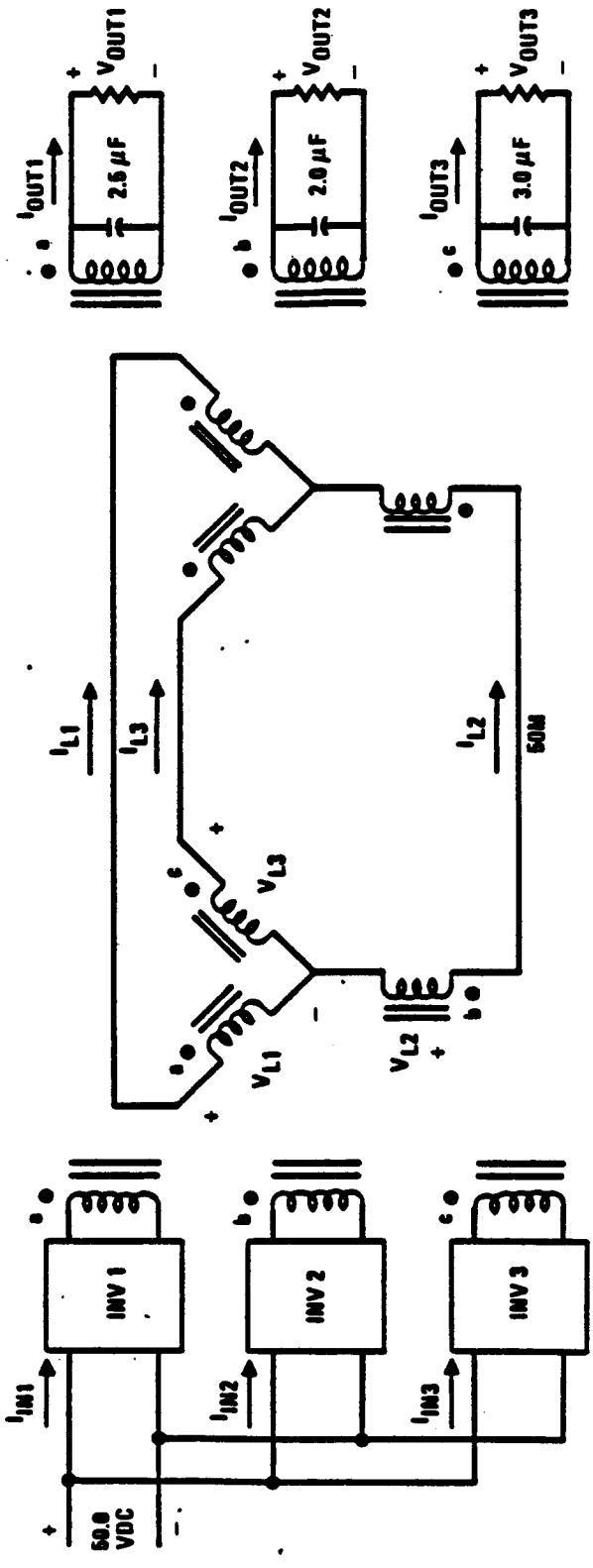


FIGURE 4.7-9. INVERTER NUMBER 3 LEG CURRENT FOR THE UNITY BUS POWER FACTOR CASE

FIGURE 4.7-10. SYSTEM ARRANGEMENT USED TO PRODUCE A LAGGING POWER FACTOR



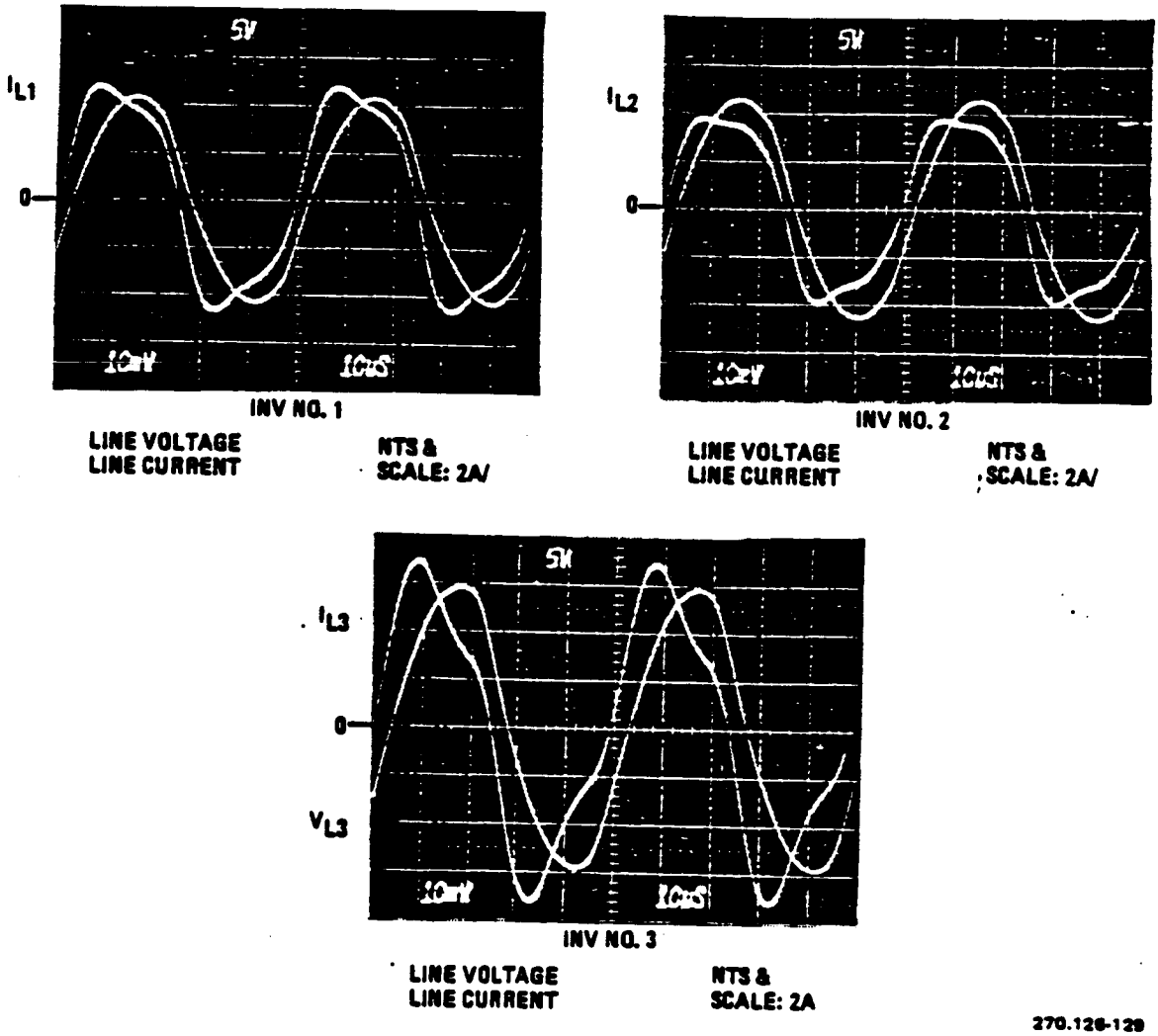


FIGURE 4.7-11. BUS VOLTAGES AND CURRENTS FOR THE LAGGING POWER FACTOR CASE

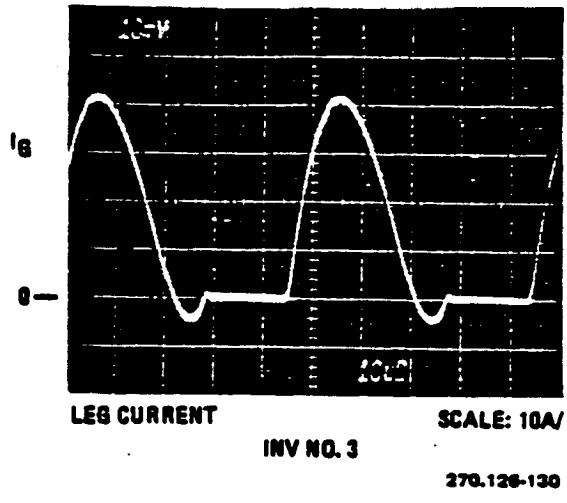
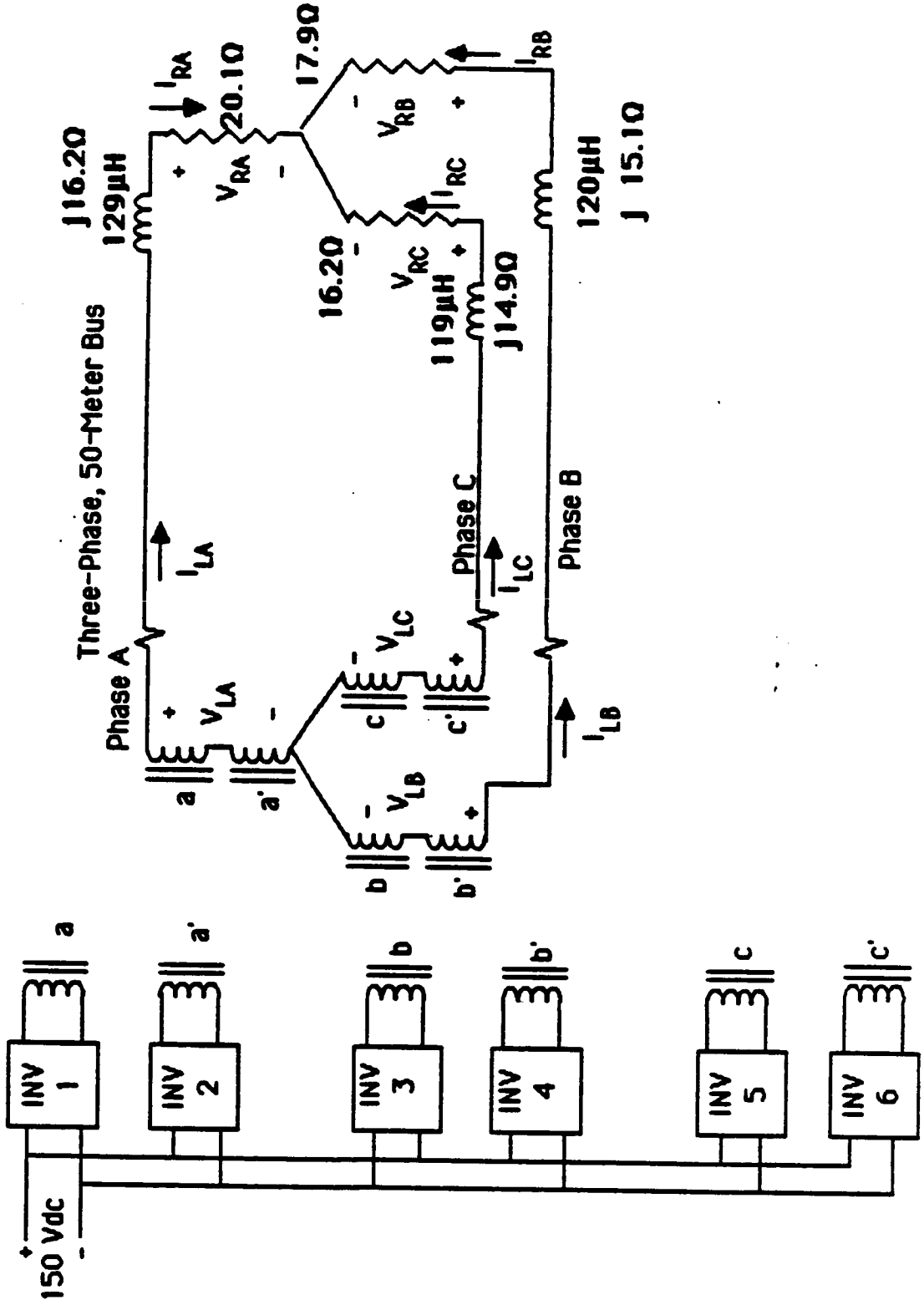


FIGURE 4.7-12. INVERTER NUMBER 3 LEG CURRENT FOR THE LAGGING POWER FACTOR CASE

FIGURE 4.7-13. INDUCTORS WERE ADDED TO THE BUS TO PRODUCE THE LAGGING POWER FACTOR



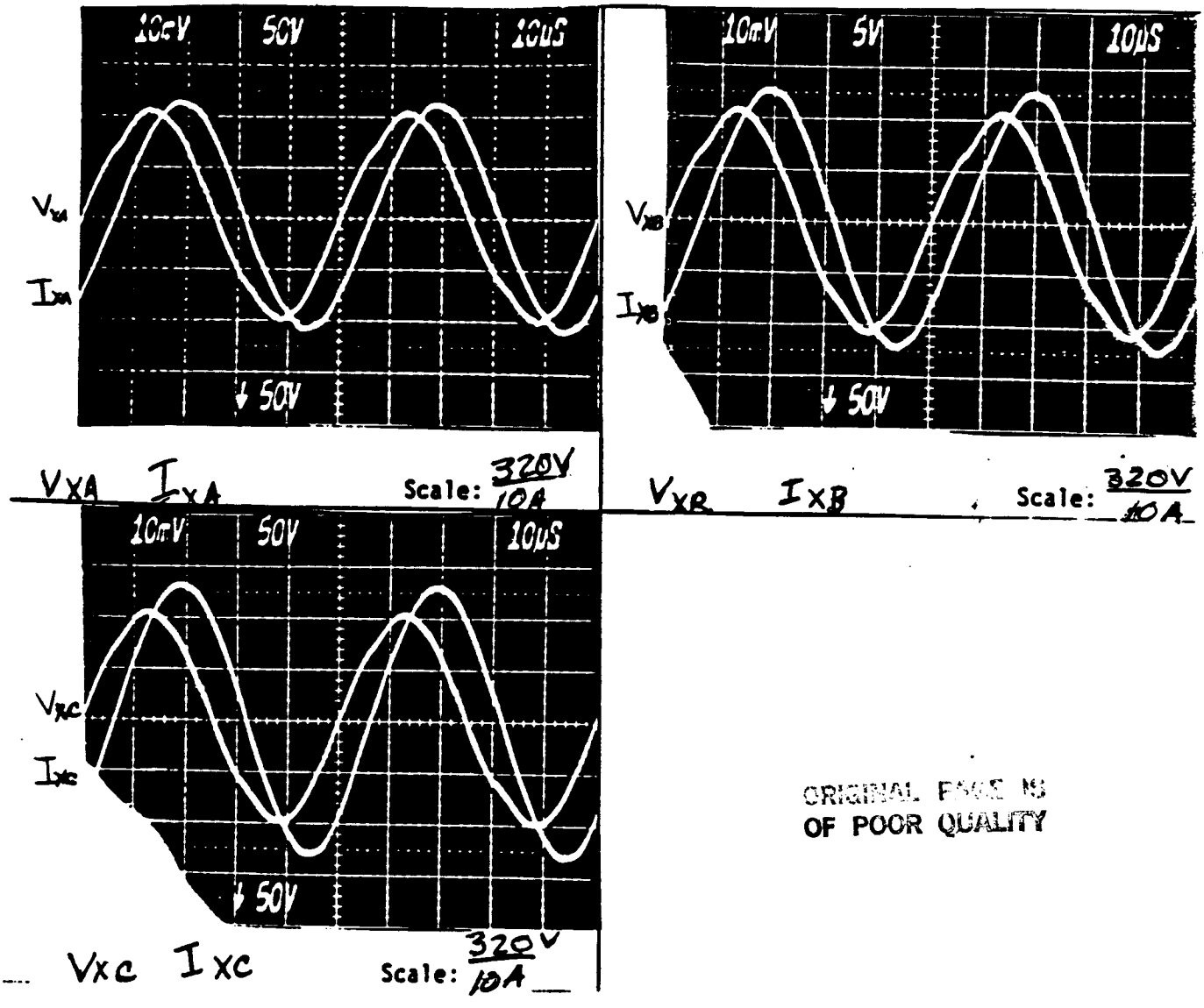
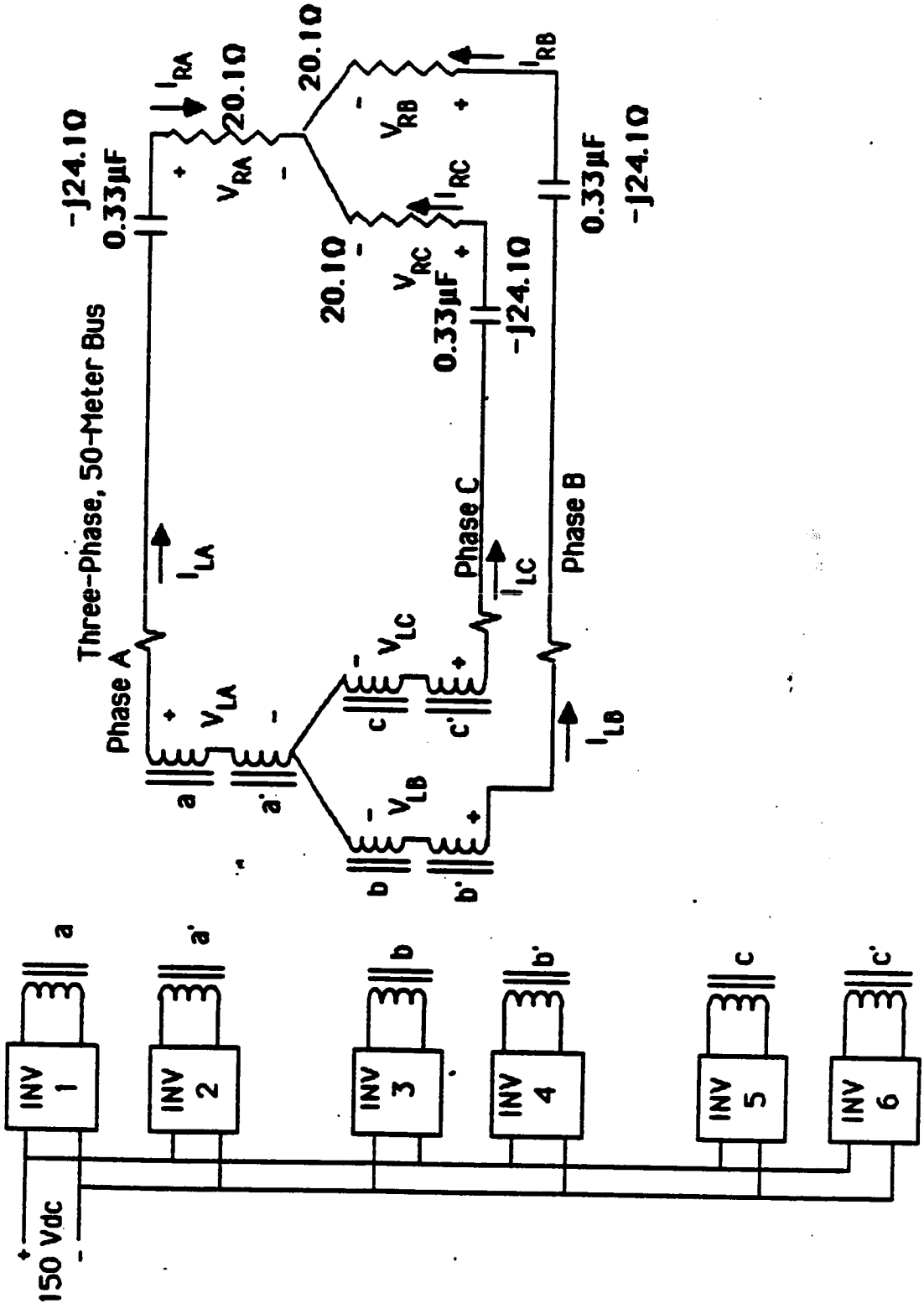


FIGURE 4.7-14. BUS VOLTAGES AND CURRENTS FOR THE 0.7 LAGGING POWER FACTOR LOAD

FIGURE 4.7-15. CAPACITORS WERE ADDED TO THE BUS TO PRODUCE THE LEADING POWER FACTOR



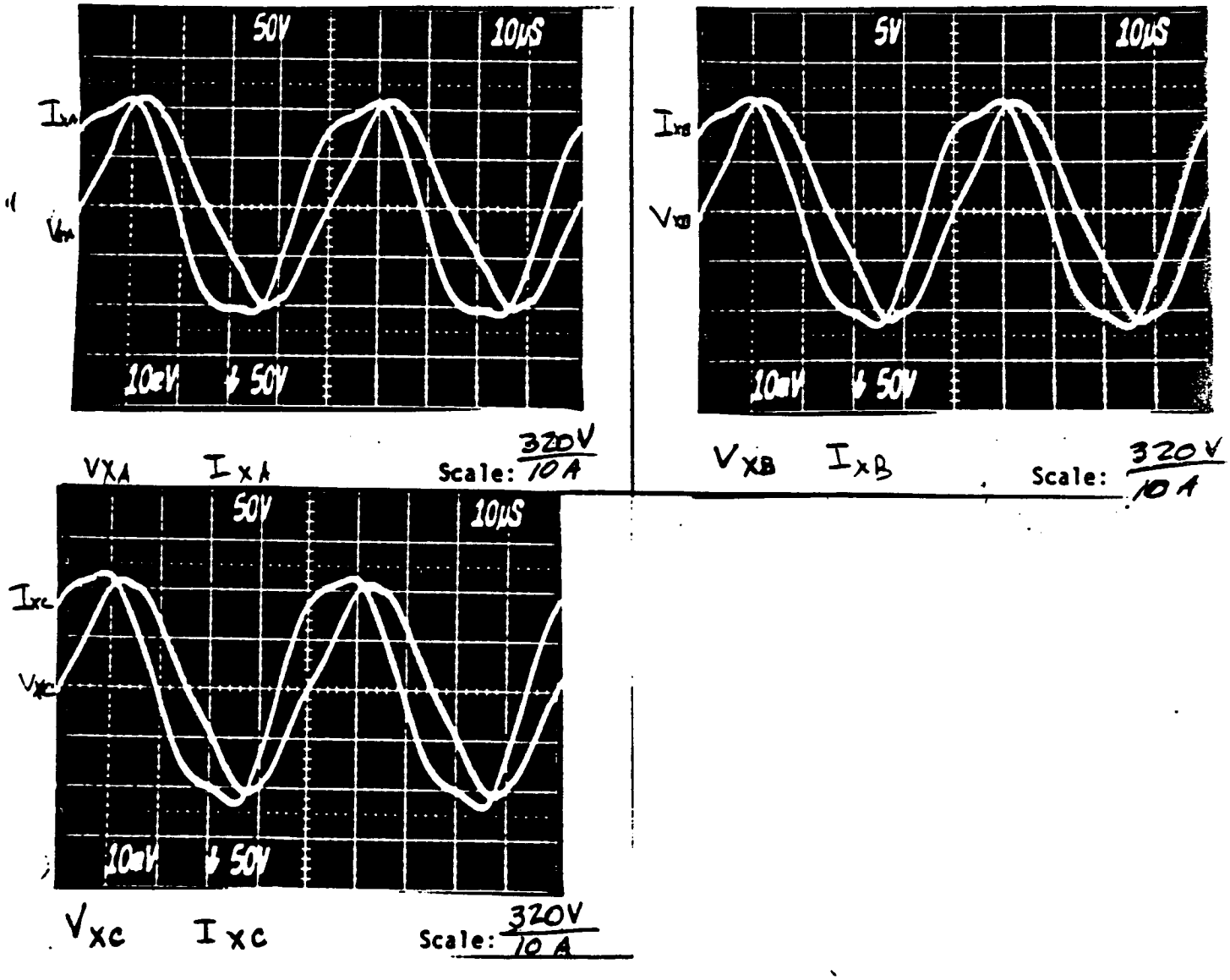
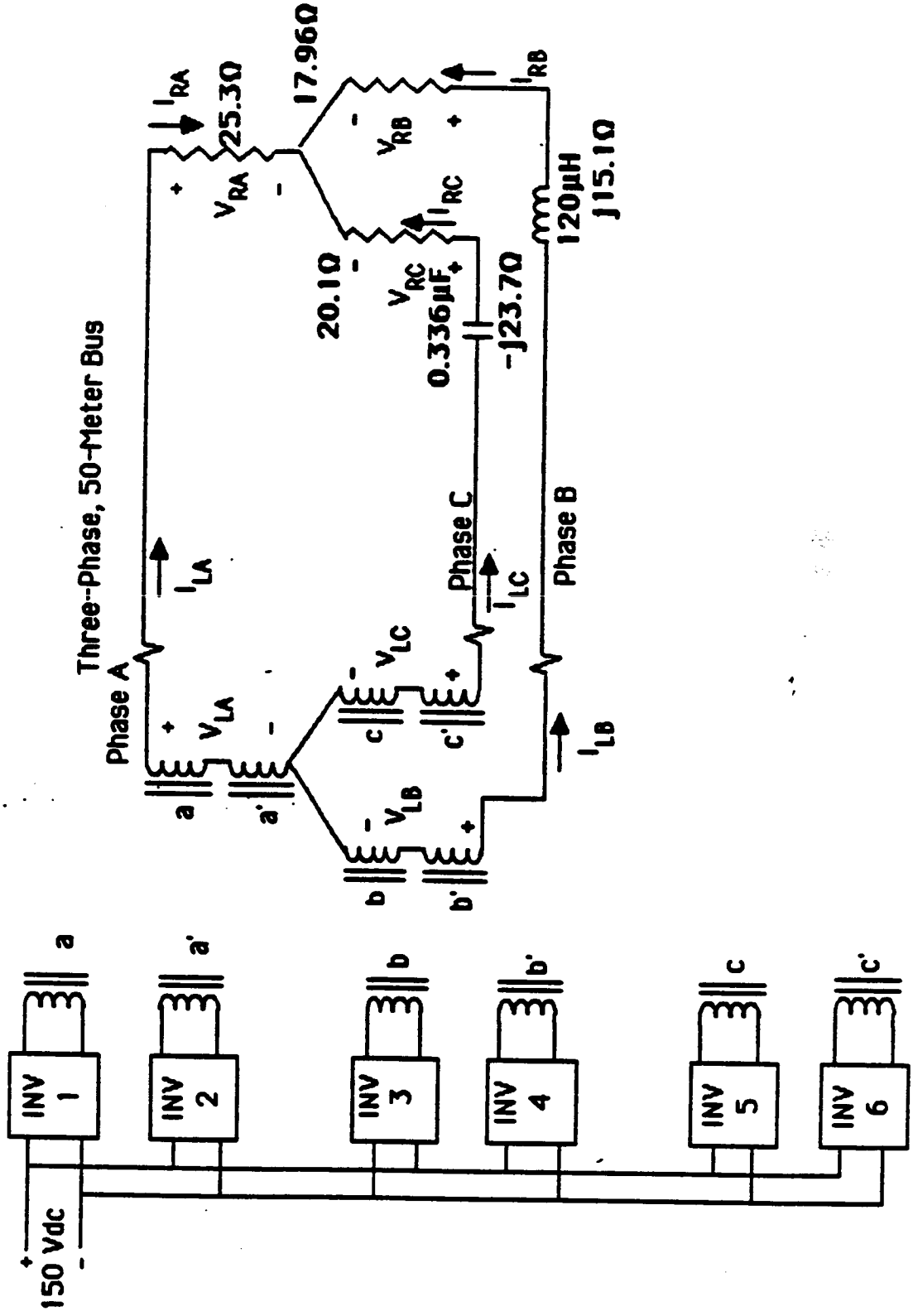


FIGURE 4.7-16. BUS VOLTAGES AND CURRENTS FOR THE 0.7 LEADING POWER FACTOR LOAD.

FIGURE 4.7-17. THE SYSTEM WAS OPERTATED WITH A DIFFERENT POWER FACTOR ON EVERY PHASE OF THE BUS FOR THIS TEST.



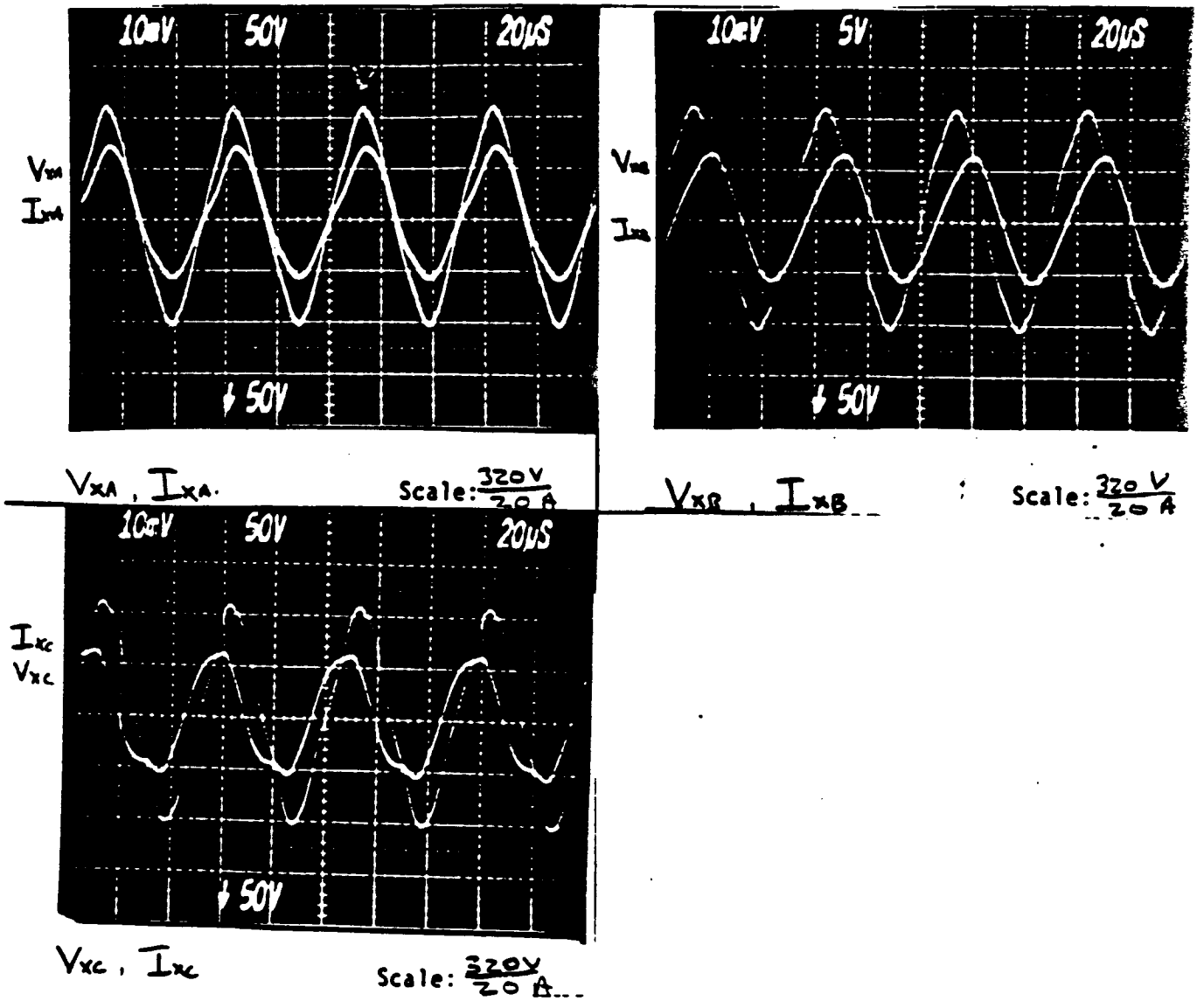


FIGURE 4.7-18. BUS VOLTAGES AND CURRENTS FOR THE UNBALANCED POWER FACTOR LOADS.

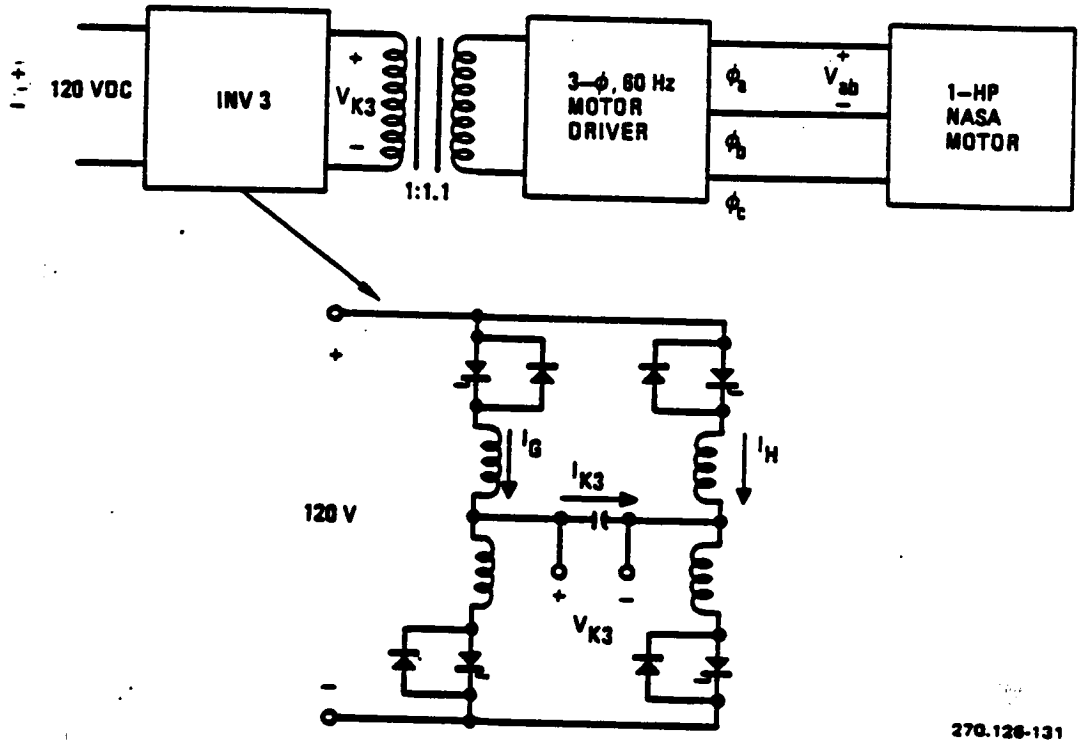


FIGURE 4.8-1. THREE-PHASE, 60HZ MOTOR TESTING CONFIGURATION

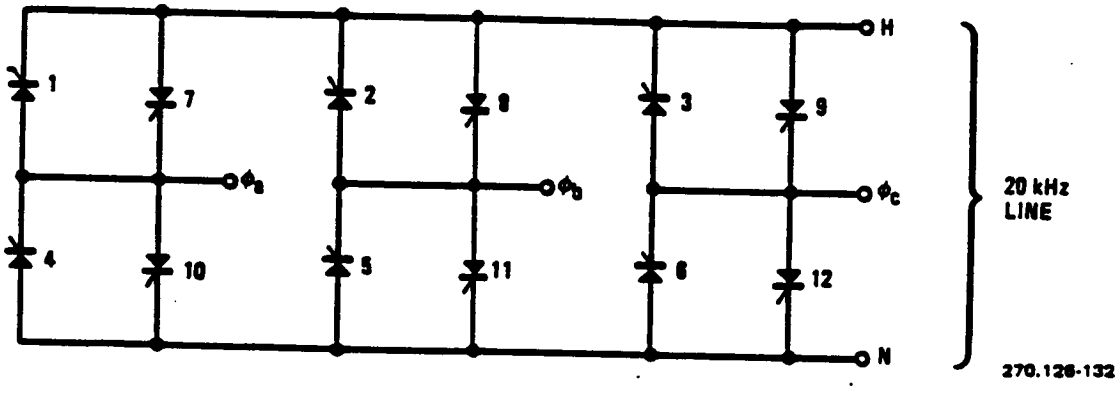
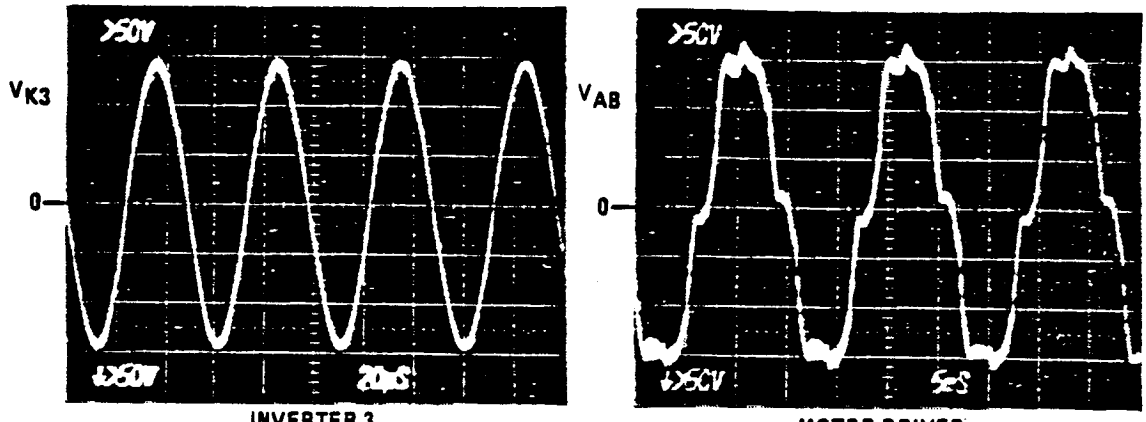


FIGURE 4.8-2. 20KHZ-TO-3 PHASE, 60HZ MOTOR DRIVER SCHEMATIC



INVERTER 3
OUTPUT VOLTAGE
SCALE: NOT TO SCALE

MOTOR DRIVER
OUTPUT VOLTAGE
SCALE: NOT TO SCALE

270.126-133

FIGURE 4.8-3. INVERTER OUTPUT VOLTAGE AND ONE PHASE OF THE MOTOR INPUT VOLTAGE FIGURE 2-3. 25.0-KW SYSTEM CONFIGURATION.

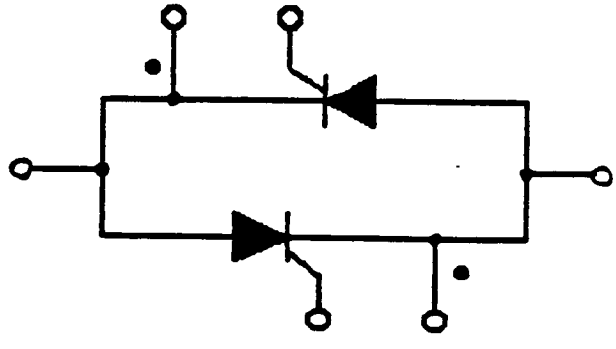
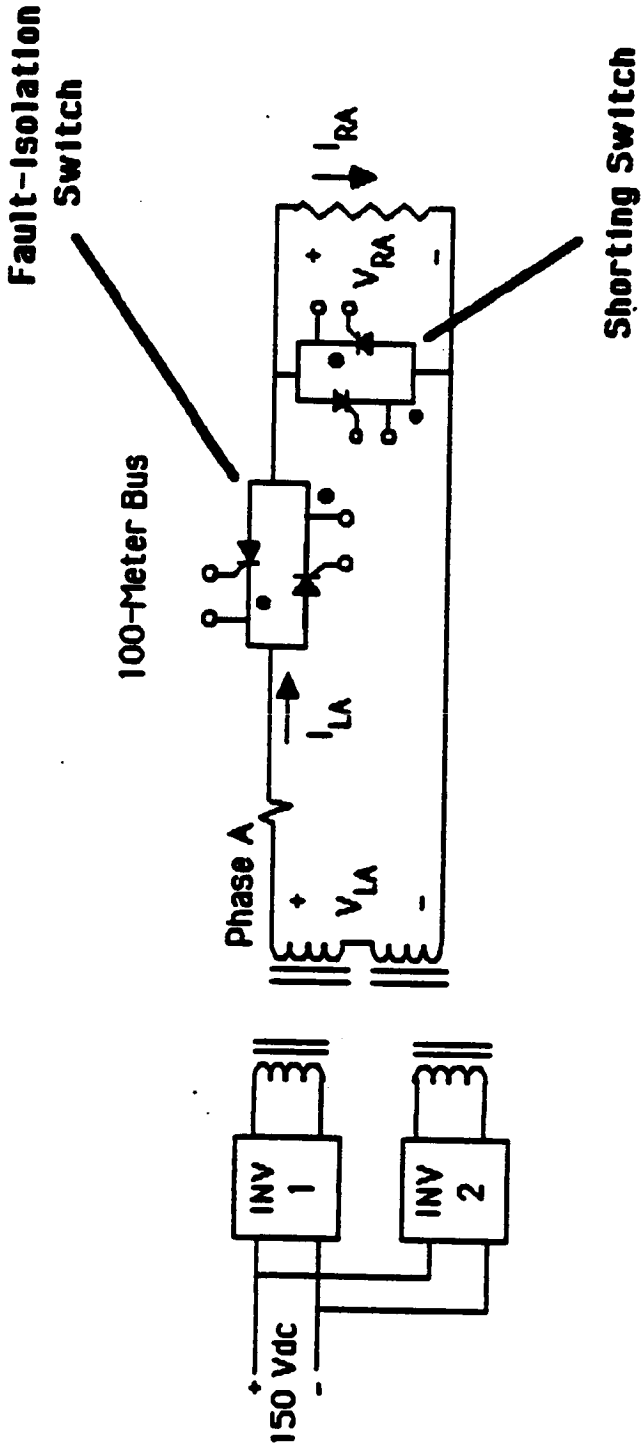


FIGURE 4.9-1. THE FAULT-ISOLATION SWITCH USES HIGH VOLTAGE SCRS.

FIGURE 4.9-2. THE FAULT-ISOLATION SWITCH SHORT CIRCUIT CLEARING ABILITY WAS TESTED WITH THIS CIRCUIT.



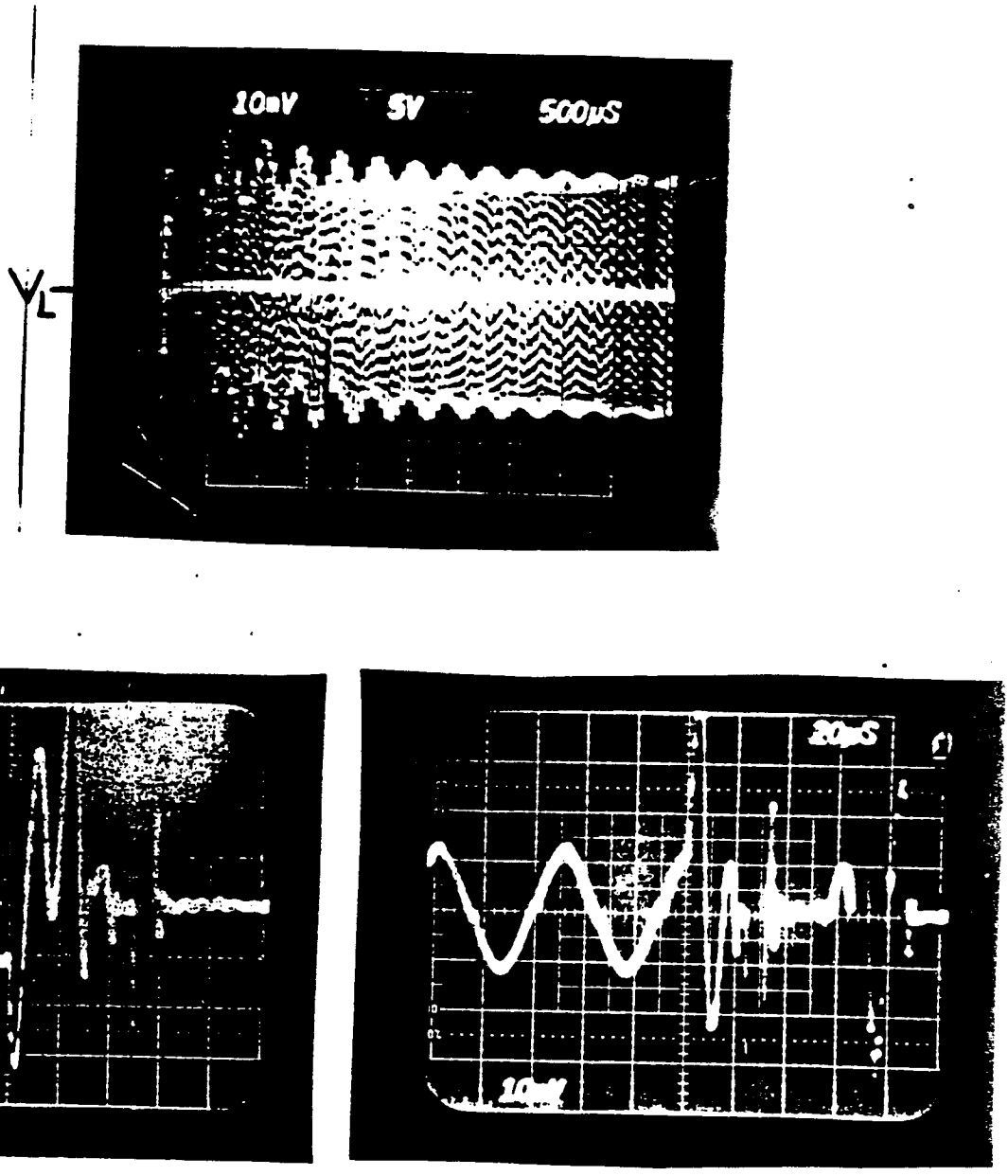


FIGURE 4.9-3. BUS VOLTAGE AND CURRENT AS A FAULT IS CLEARED FROM THE BUS.

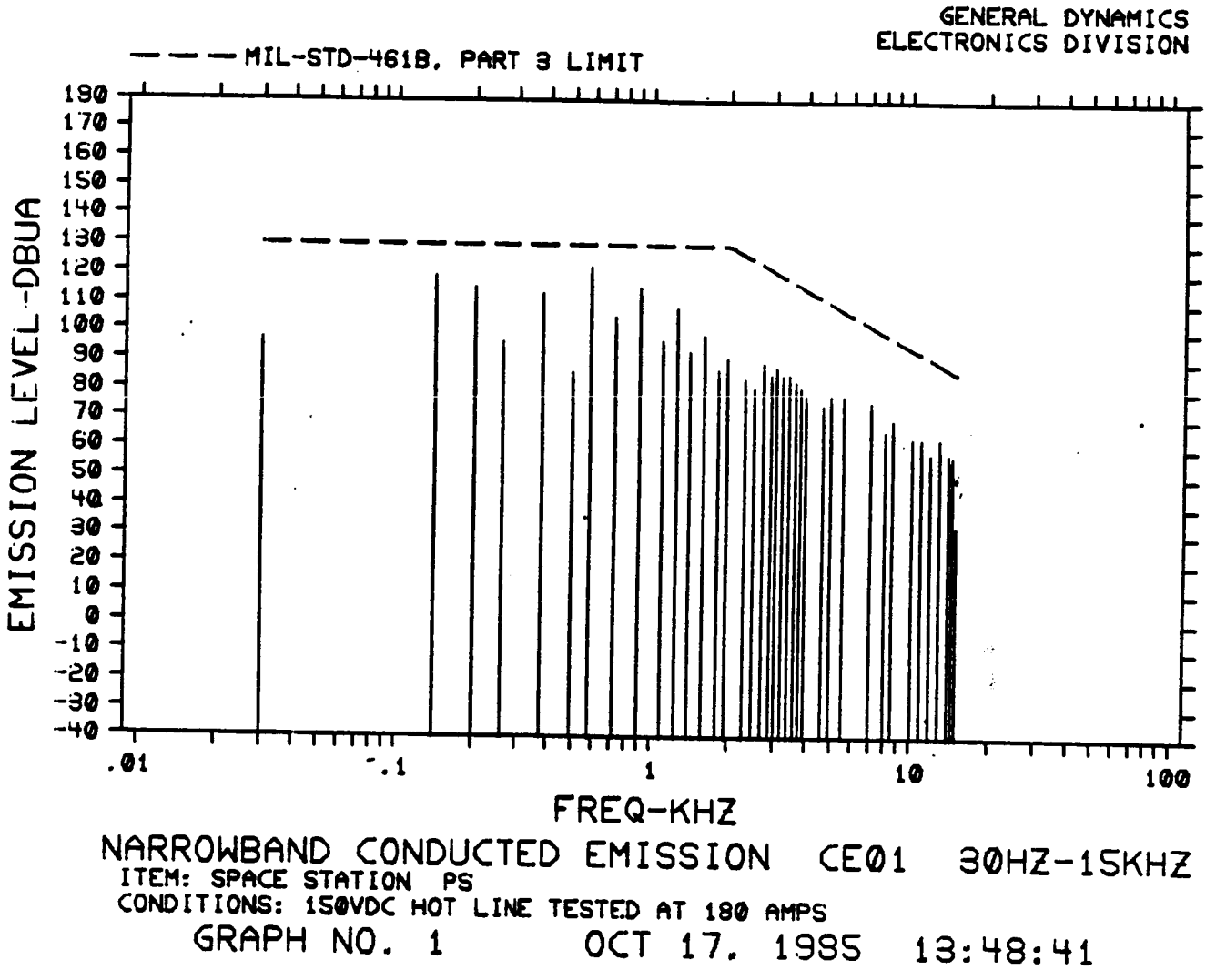


FIGURE 4.10-1. RESULTS OF THE CE01 EMI TEST ON THE DC INPUT LEADS.

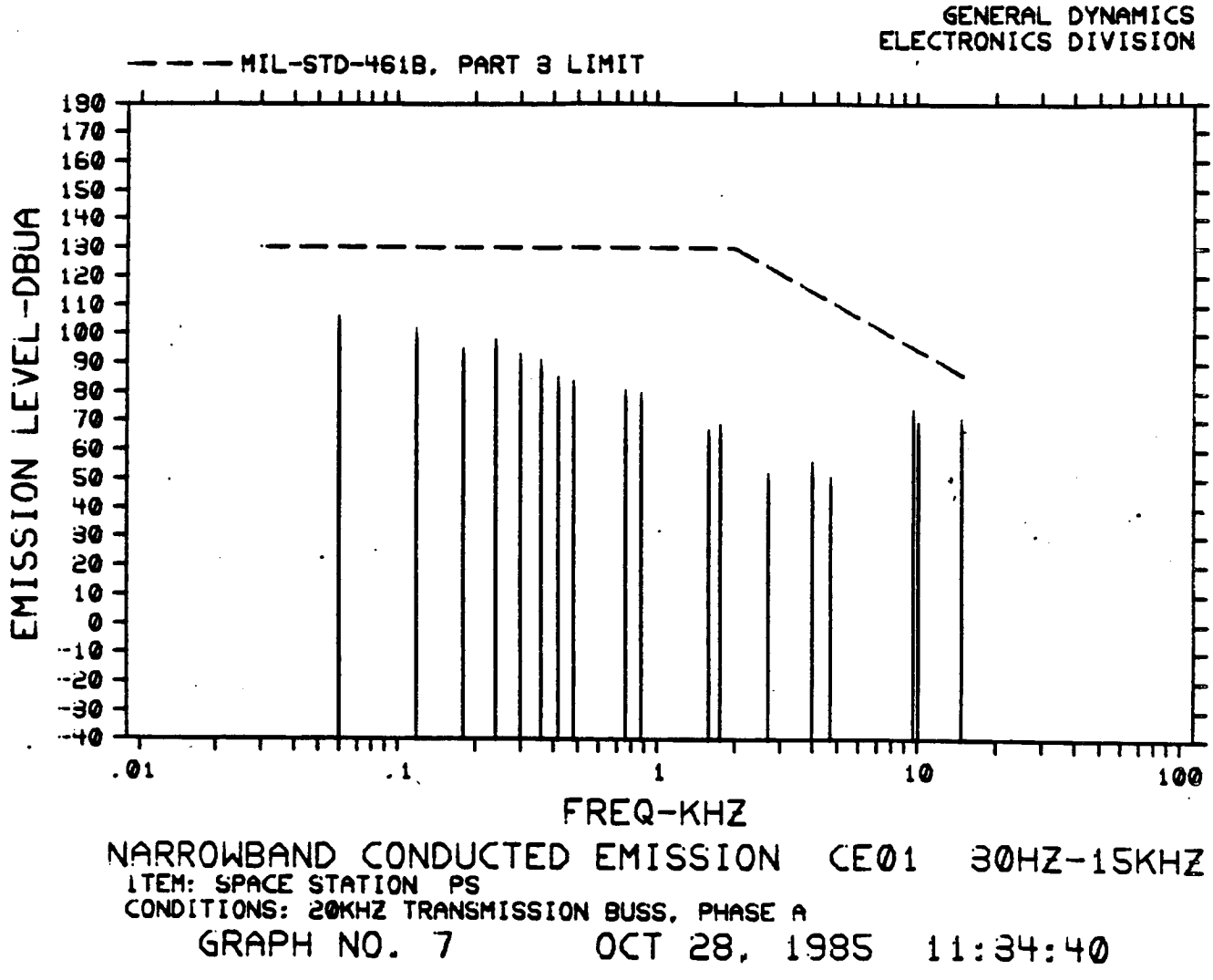


FIGURE 4.10-2. RESULTS OF THE CE01 EMI TEST ON PHASE A.

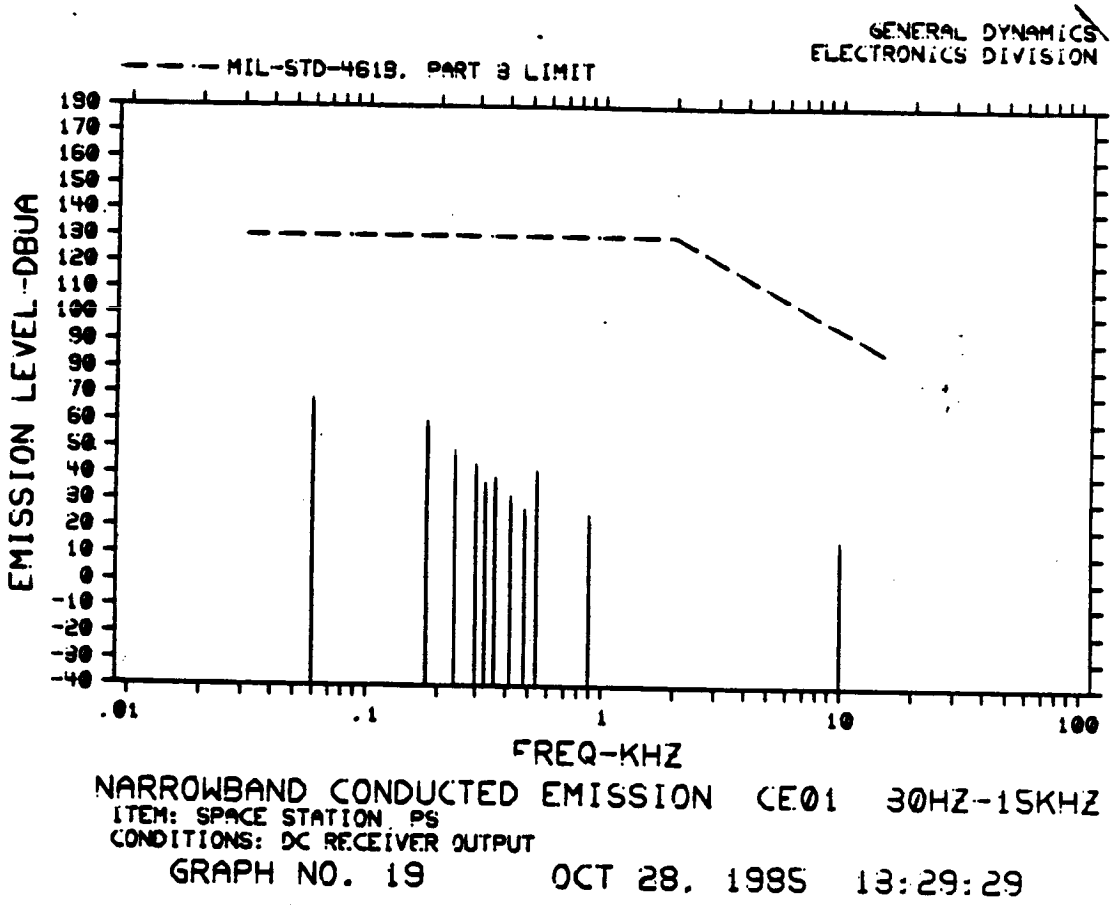


FIGURE 4.10-3. RESULTS OF THE CE01 EMI TEST ON THE DC RECEIVER OUTPUT.

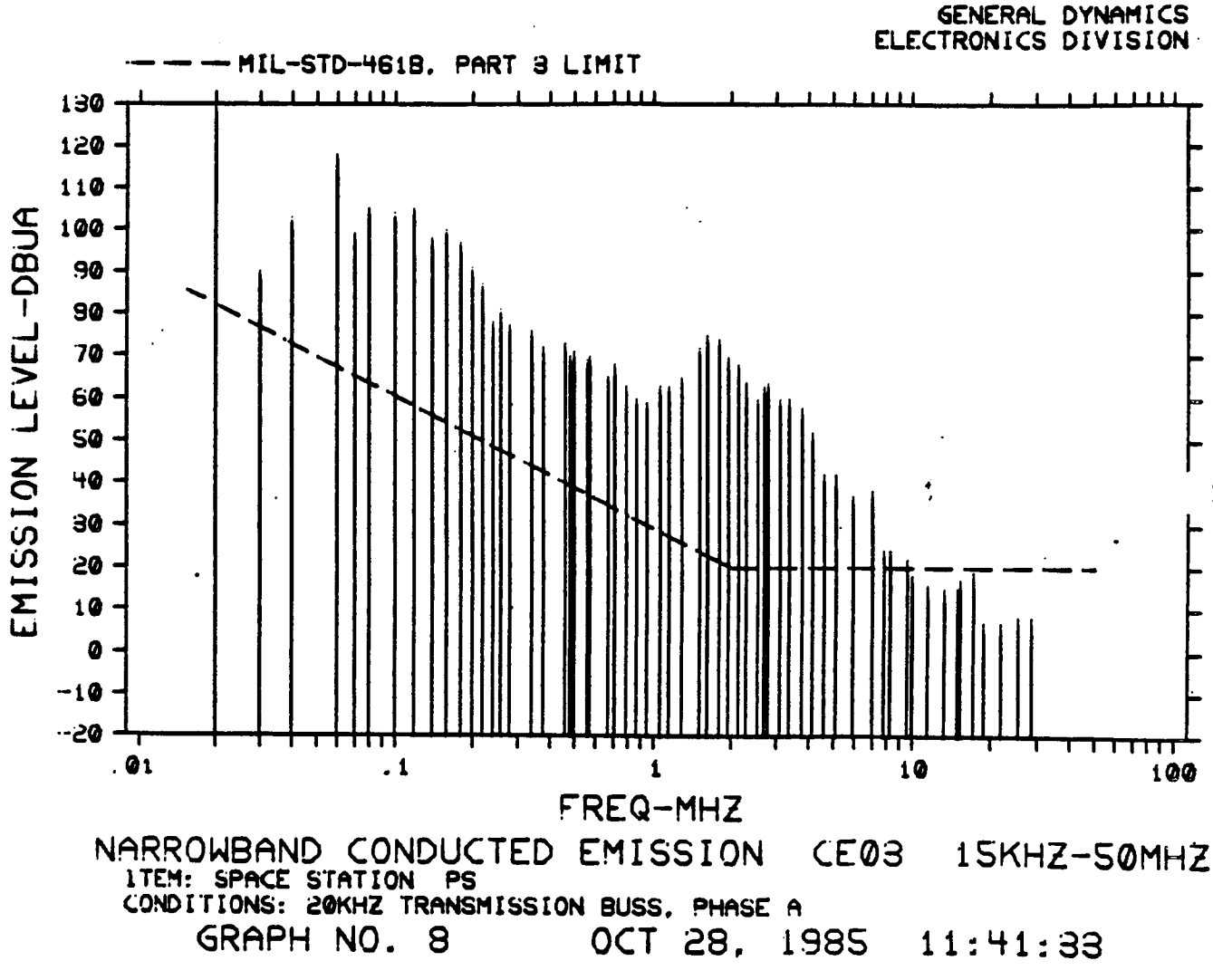


FIGURE 4.10-4. RESULTS OF THE CE03 EMI TEST ON PHASE A.

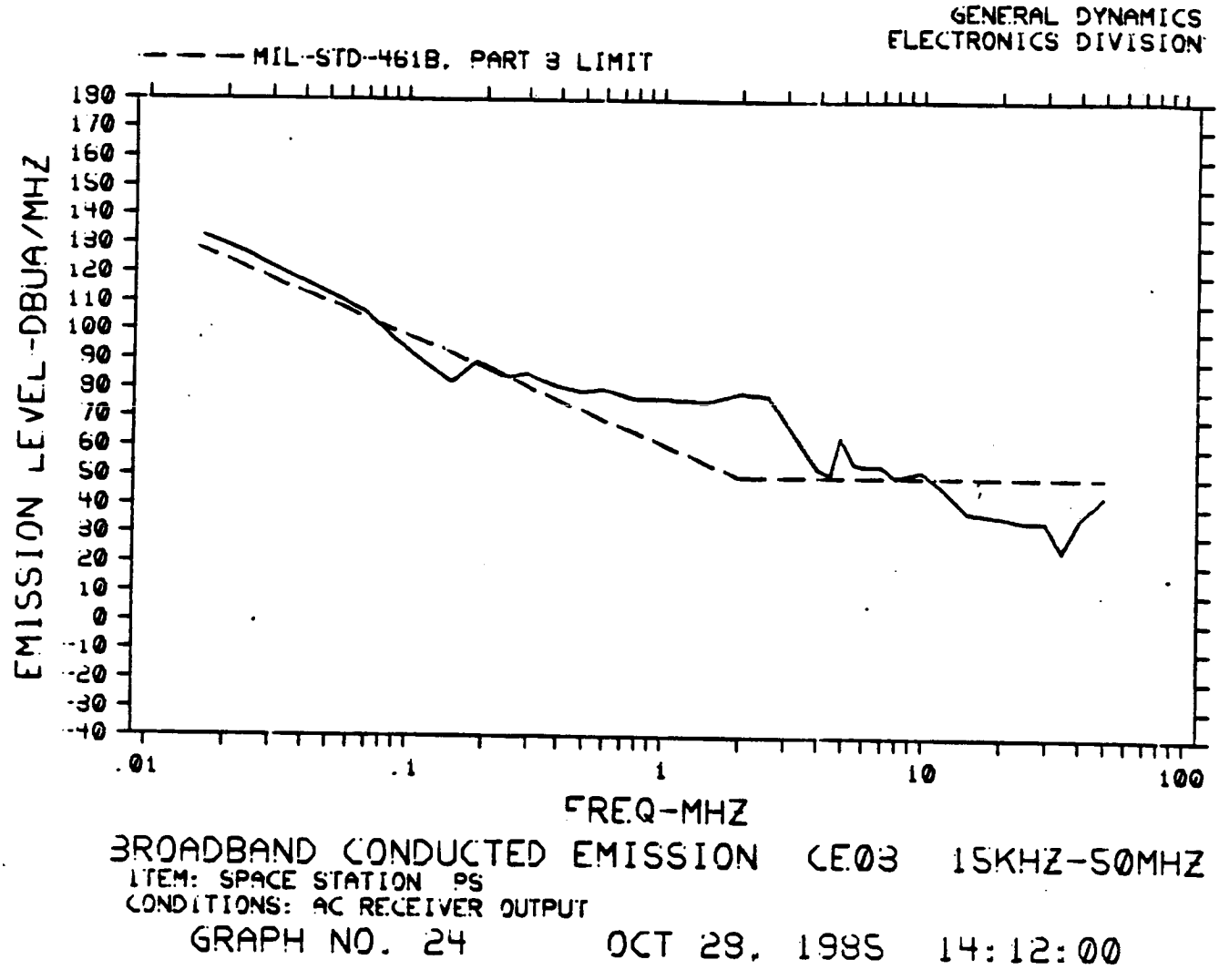


FIGURE 4.10-5. RESULTS OF THE BROADBAND CE03 EMI TEST ON THE AC RECEIVER.

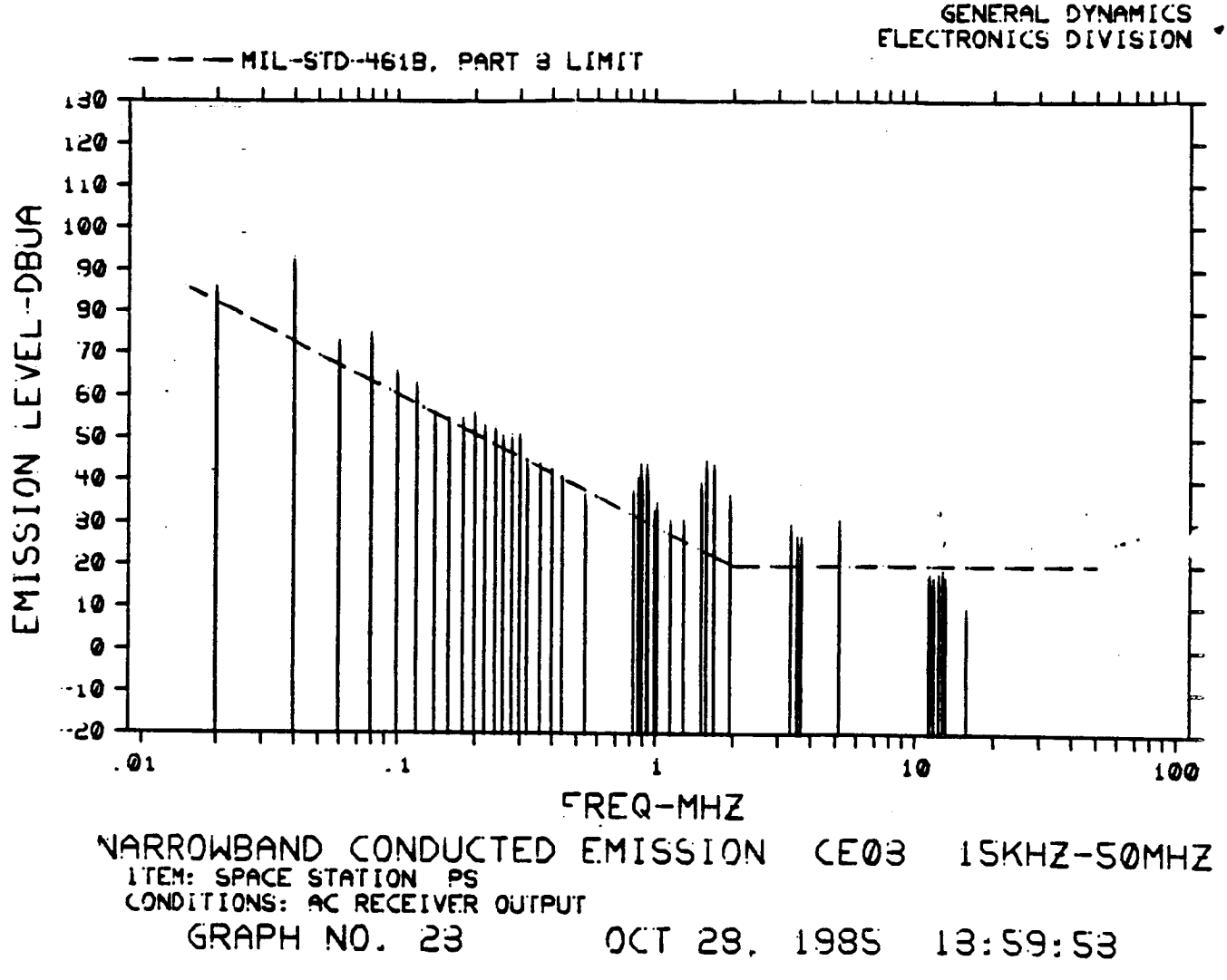


FIGURE 4.10-6. RESULTS OF THE NARROWBAND CE03 EMI TEST ON THE AC RECEIVER.