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AC Power System Testbed Final Report

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GENERAL DYNAMICS
Space Systems Division

Prepared for

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16. Abstract

The object of this program was to design, build, test, and deliver a high frequency (20-kHz) Power System Testbed which would electrically approximate a single, separable power channel of an IOC Space Station. This report describes that program, including the technical background, and discusses the results, showing that the major assumptions about the characteristics of this class of hardware (size, mass, efficiency, control. etc.) were substantially correct. This testbed equipment has been completed and delivered to LeRC, where it is operating as a part of the Space Station Power System Test Facility.

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AC Power System Testbed

Final Report

NAS 3-24399

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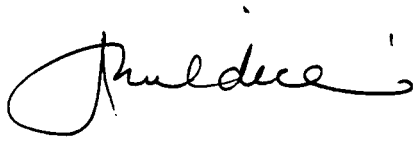
Approved by: 

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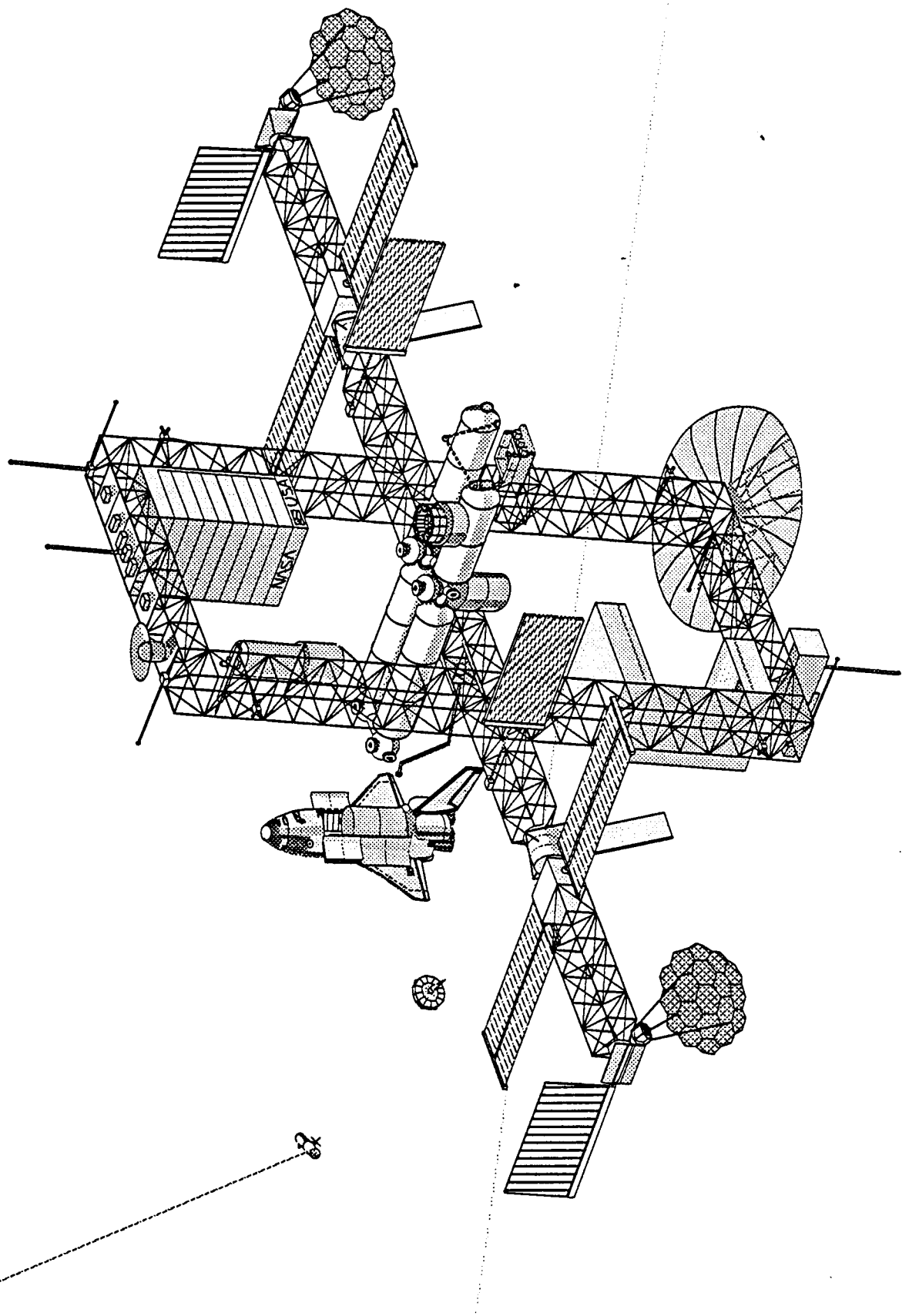

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1.0 Summary

The objective of this program was to design, build, test, and deliver a high frequency (20-kHz) Power System Testbed which would electrically approximate a single, separable power channel of an IOC Space Station. That testbed is diagrammatically pictured on Figure 1-1, and includes the following major elements:

- Six Inverter/Driver modules which can be operated to test and demonstrate the hardware required to interface DC sources (Solar Arrays) to the high frequency transmission bus system. They also act as the 20-kHz power sources to test other system components.

- A set of source control switches (RPC's) to test and demonstrate autonomous system fault protection.

- A transmission bus system to measure transmission parameters, characteristics, noise, and EMI performance to confirm analytical predictions.

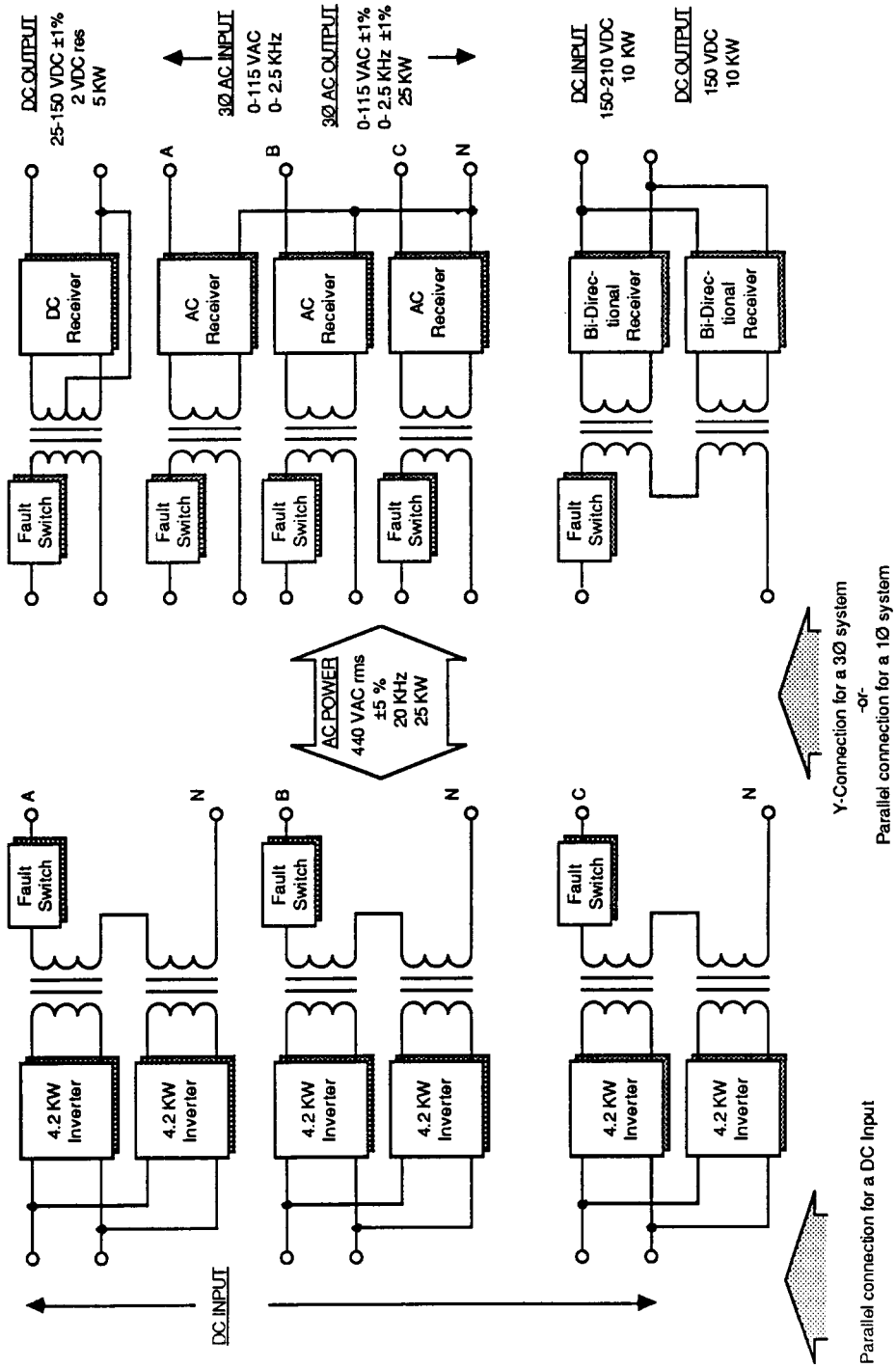
- A set of load control switches (RPC's) to show how the system will protect itself against load/user faults.

- A typical set of three high power user interface units to investigate and define the best techniques to interface with DC loads, low frequency AC loads and AC motors, and energy storage devices, such as batteries.

- A computer control system, including a MacIntosh™ terminal and supervisory interface, which commands imbedded processors in the power hardware, to demonstrate system control and computer interface designs, with technologies appropriate for actual Space Station hardware.

The design approach was to use "Mapham"-derived (Reference 1) series resonant, thyristor-switched, inverter/converter configurations of the type successfully designed and demonstrated by General Dynamics. New power stages are integrated with with a previously developed set of control modules, (NAS 3-23878, Reference 2) to construct the

Figure 1-1, Testbed Block Diagram



family of power processors required.

The hardware constructed and delivered is intended to be an electrical analog of a possible flight configuration, but the mechanical design is appropriate to the laboratory environment, and is not representative of spacecraft configurations. Bus lengths (50 to 100 meters) and losses for power transmission testing approximate worst cases expected on the current space station configuration, to provide high fidelity hardware modeling of an area that has traditionally been difficult to model with analytical techniques.

The test program was designed for two purposes. First it demonstrated that the complete, integrated set of hardware operated properly and performed its basic design functions. The second part of the program was used to evaluate and define the hardware performance on an engineering level, and provide the data required to properly design future systems. In addition, the test program integrated with another NASA development by providing full power tests of a GFP engineering model of a special, low inductance power bus. (Reference 3) Details of the entire test program and its results are published as a separate report. (See Reference 4)

Finally, the completed, tested hardware was delivered to the NASA Lewis Research Center, where it has been installed and tested in their Power System Test Facility, where it will be integrated with other major components of the Space Station Power System.

Contract Overview:

- **Overall Goal:** Construct a 20-kHz power system test bed representative of Space Station functions and sizes.
- **Contract Value:** $733K
- **Schedule:** Contract Start Date - January, 1985
  Hardware delivery - July, 1987

- **System Elements:**
  - Driver/Inverter Modules
  - Bus Control Switch Matrix
  - Power Bus
  - Load Control Switch Matrix
  - Variable Voltage DC Receiver Module
  - Variable Voltage, Variable Frequency AC Receiver Modules
  - Bidirectional Converter Receiver Module
  - Computer/System Controller and Software

2.0 Introduction and Background

2.1 Theory of Operation

The high-frequency power system technology addressed by this program generates its basic AC transmission link power by exciting an underdamped, series-resonant, L-C circuit. The power bus therefore becomes an integral part of the resonant link in the more-or-less usual resonant converter configuration, with the load interface modules forming the output stages. Therefore the power system for a vehicle is really one large, integrated, multiple-module resonant converter. Its range of proper underdamped operation is defined by the full load and no load system specifications.

While the basic configuration is a series resonant design, it is not the familiar "Schwarz" (Reference 5) type. This design places the load (reflected through the output transformer) in parallel with the resonant capacitor in the method proposed by Neville Mapham (Reference 1). Figures 2-1 and 2-2 show the two circuit approaches.

This gives us a system driver (inverter) that is essentially a voltage source as compared to the more usual "Schwarz" current source. This has obvious advantages for a power system. The line voltage is independent of the load (on a first order basis) and is tolerant of open circuits, obvious requirements for a utility system. In addition, the output frequency is clock-controlled, and independent of variations in the resonant circuit components, which is a significant development for this class of hardware.

The basic power output hardware configuration for a single driver is shown in Figure 2-3. Two or more such drivers are arranged in series, with different phase shifts between one another, to add and provide power output closed-loop regulation. (See Figure 2-4.) The control circuits noted (c) in the above figures are the subject of the contract described in section 2.2.

The pure load interface modules process the 20-kHz transmission bus power to create the required user power forms. In all cases, the process is basically a traditional AC rectification type. Output amplitude control is accomplished by pulse population or

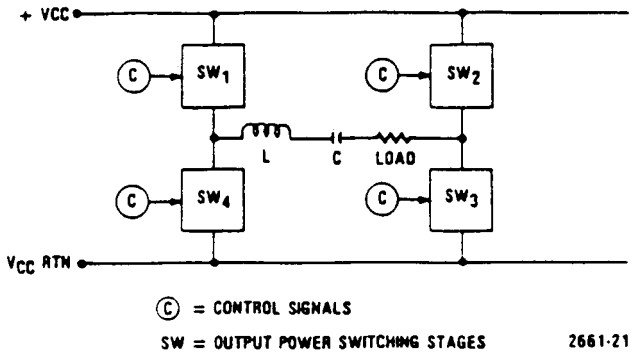


Figure 2-1, The Schwarz configuration has the load in series with the resonant circuit.

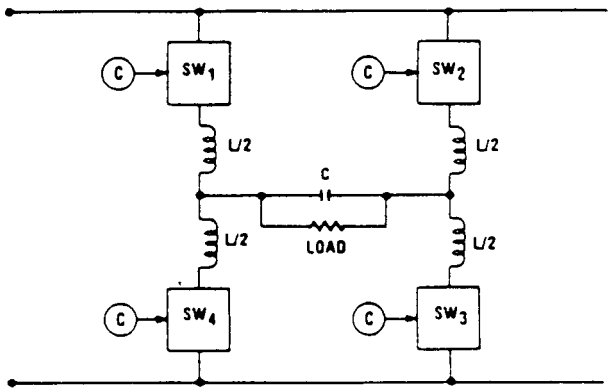


Figure 2-2, The Mapham circuit has the load in parallel with the resonant capacitor.

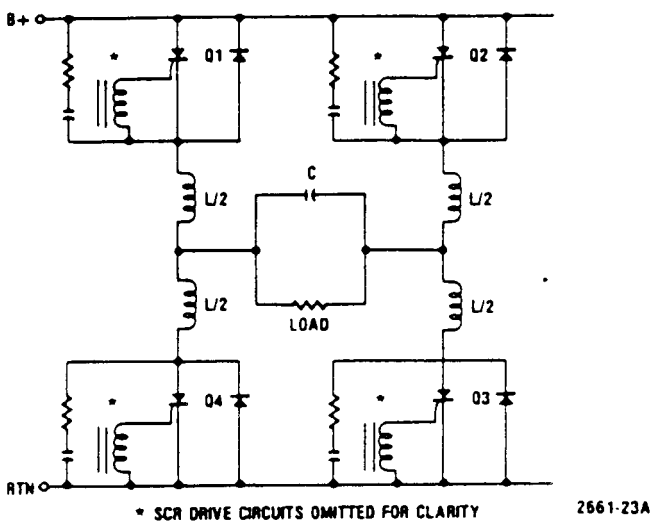


Figure 2-3, Basic Inverter Power Stage

phase delay control of individual 20-kHz half-sine pulses. The combination of amplitude control and individual pulse steering allow for the creation of a wide range of lower frequency AC outputs. Figures 2-5 and 2-6 show typical (simplified) receiver configurations for DC and low frequency AC outputs.

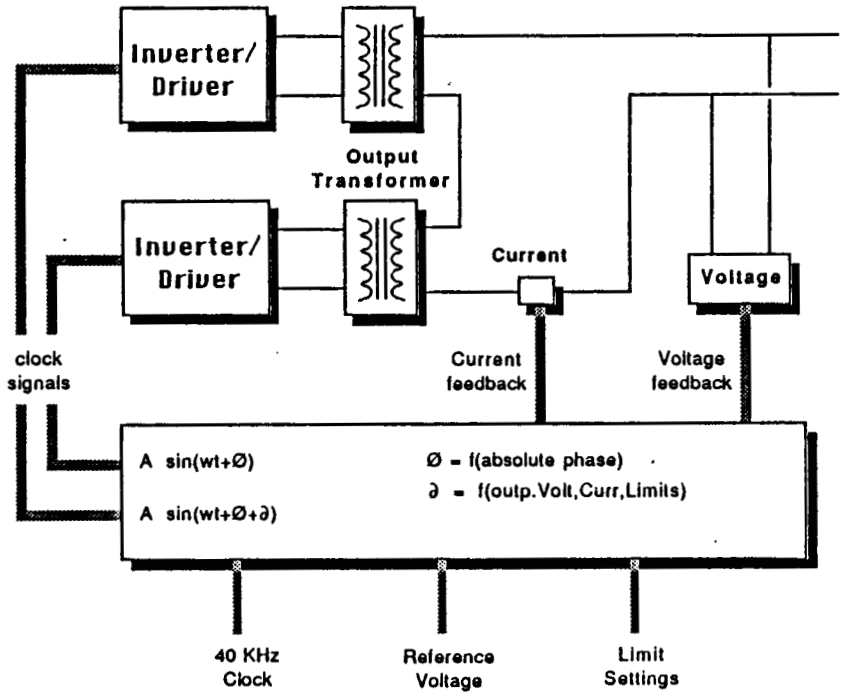


Figure 2-4, Basic Phasor Regulation Approach

The third receiver module takes advantage of the the inherent bilateral nature of this class of hardware to be both source and load interface. In the load interface mode, its thyristors are switched so that it looks just like the above-described DC receiver. In the source mode, its switches operate to make it an inverter.

Finally, there are many classes of loads that can use the 20KHz bus power directly. Simple transformer coupling can be used to supply lighting (both fluorescent and incandescent), resistance heaters, simple induction heaters, etc.

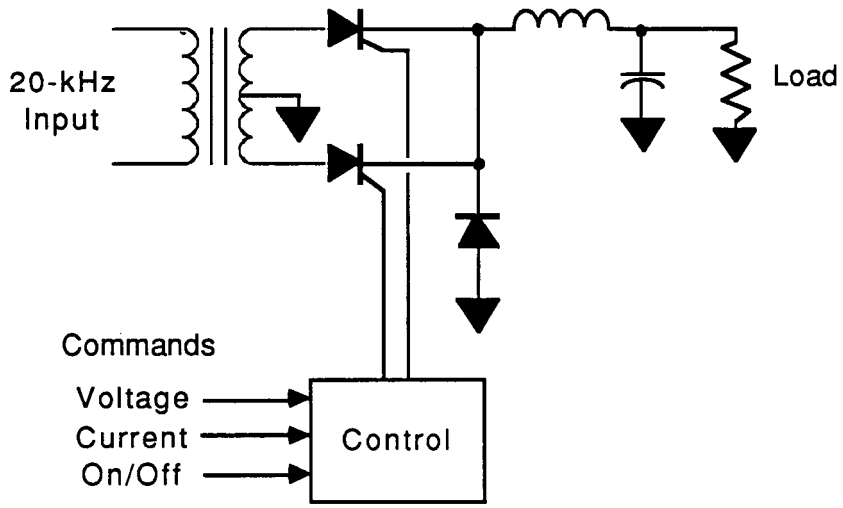


Figure 2-5, Typical DC Receiver output circuitry

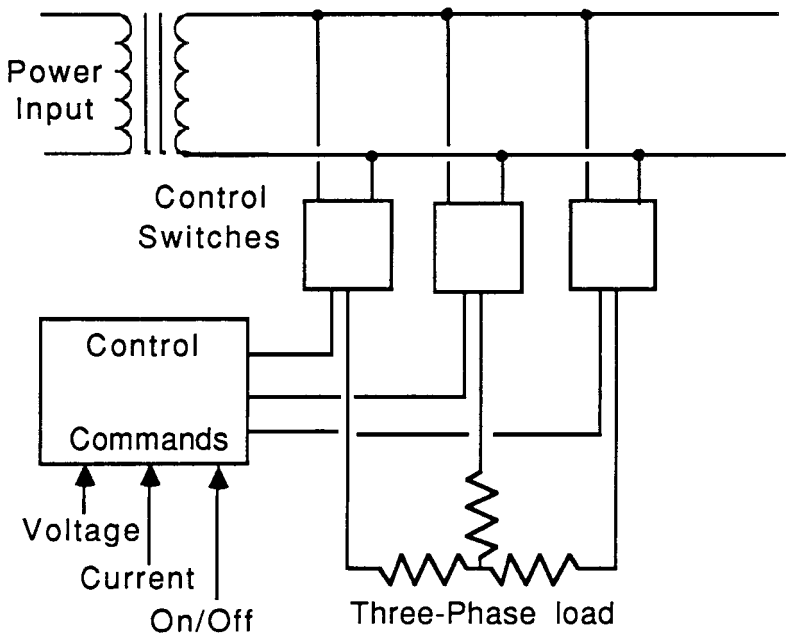


Figure 2-6, Three-phase, low frequency AC output circuitry

2.2 Control Circuit Development Program (NAS 3-23878)

Bidirectional Power Converter Control Electronics (BDPCCE)

This program was aimed at developing a family of control circuit designs for resonant technology, power processing hardware; which were appropriate to control the SCR driven power switching stages and series resonant networks of "Mapham" (Reference 1) derived inverter/converter configurations.

In general,the primary tasks included the following:

- Analyze the basic set of functions required to control a multi-phase bidirectional resonant power system.
- Create a set of basic designs to implement those functions.
- Build and test the basic designs
- Integrate and test the control hardware into high power breadboard/testbed systems.

Application specific power processor requirements addressed both source and load interfaces, and included regulating drivers/inverters/frequency-changers to provide high frequency (20-kHz) AC from DC or low frequency AC; and bidirectional interfaces from 20-kHz AC to DC or low frequency AC loads and users. The main functions were broken into two sections and defined as follows:

2.2.1. General

- Housekeeping
- Overload Protection

2.2.2. Application Specific

- Case 1: On-board battery charging from the high frequency bus.

- Case 2: Auxiliary ground power energizing the high frequency bus.
- Case 3: Variable speed motor/generator starting/running/generation to and from the high frequency bus.

Therefore, the control circuit designs developed by this program are the basic control modules required for the testbed hardware functions. See figure 2-7 for an example of the control modules used in an inverter configuration. Those designs were carried forward to be the controls for the testbed contract power stages. Reference 2 documents the details of the control development. As testing and troubleshooting of the testbed hardware progressed, some changes were required, and the schematics and hardware drawings presented in this report are the updated ones.

2.3 Overall Testbed Contract Tasks

2.3.1 Design and Development

The testbed hardware was designed to simulate a major portion of a typical Space Station power system. The 25-kW driver assembly was judged to approximate a single source "module". It could represent a solar array wing or single solar-thermodynamic source. The set of receiver modules represented the major classifications of load interfaces that might be required on a real station. DC outputs, at a wide range of values; three-phase AC outputs for motor operation and control; and a bidirectional module, to demonstrate a typical energy storage interface.

The major elements of the hardware design and development were accomplished prior to the start of this contract. Basic power component circuit designs were previously accomplished on IRAD programs and the control circuit designs were performed on the BDPCCE program described in Section 2.2. This program mainly addressed the system design details, not previously examined. System interactions, evaluated during the debugging and testing phases of the program, resulted in some redesigns of the previously-developed hardware, and those redesigns were included in the tasks accomplished on this development.

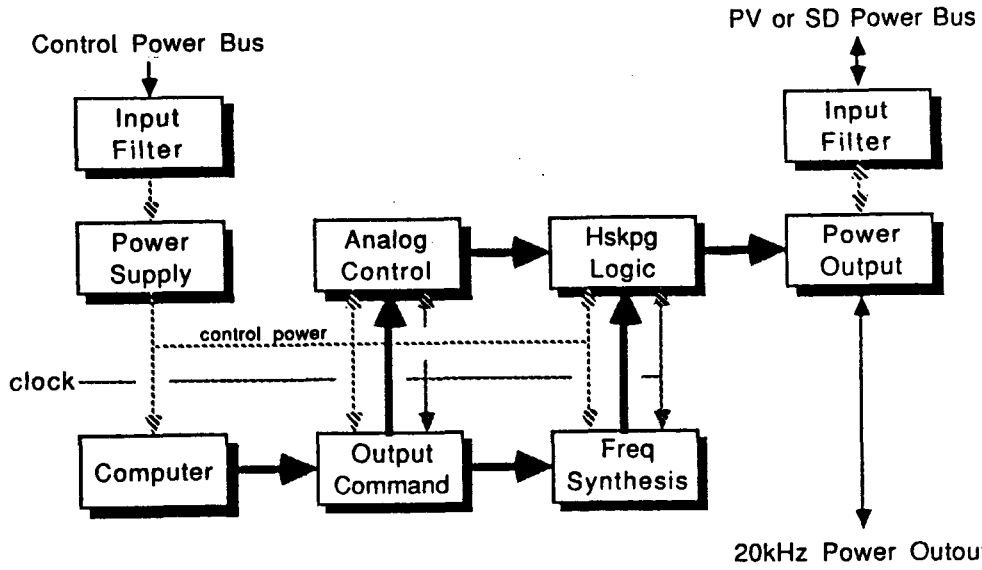


Figure 2-7, Basic Inverter Control

2.3.2 Fabrication

The fabrication task was to procure the appropriate hardware, and to actually construct the Testbed hardware to simulate a major portion of a typical Space Station configuration. It was construced in two modular groups (drivers and receivers), interconnected by a 50 meter power bus.

Because of the developmental nature of the hardware, construction and fabrication tasks were accomplished by Avionics technicians, working under the direct supervision of the design engineers.

2.3.3 Test

The test program actually operated on three separate levels.

First, the constructed hardware was debugged and tested as modules and subassemblies, and then assembled into a complete system for additional

debugging and verification testing.

Once proper operation was demonstrated, a series of engineering evaluation tests was performed to evaluate operational details and to define the engineering parameters required to design and build the final flight hardware for the actual Space Station power system. The resulting data is presented in later sections of this report.

Finally, an acceptance test was performed to verify that the hardware met all its requirements and was ready for delivery.

2.3.4 Delivery

The delivery task included the transfer of the hardware to NASA, Lewis Research Center in Cleveland, Ohio, and assistance to NASA to set up and operate the equipment in the Power Systems Test Facility at LeRC. The official acceptance test was performed after the installation in the NASA facility was complete.

3.0 Hardware Design and Development

3.1 Requirements Specification

3.1.1 Work Statement

The requirements for testbed operation are all contained in the contract work statement. Rather than repeat them in this text, a copy of the appropriate sections of the actual work statement is included as Appendix A of this report. Appendix B is a digest of the the hardware detailed requirements.

3.1.2 Requirements Changes

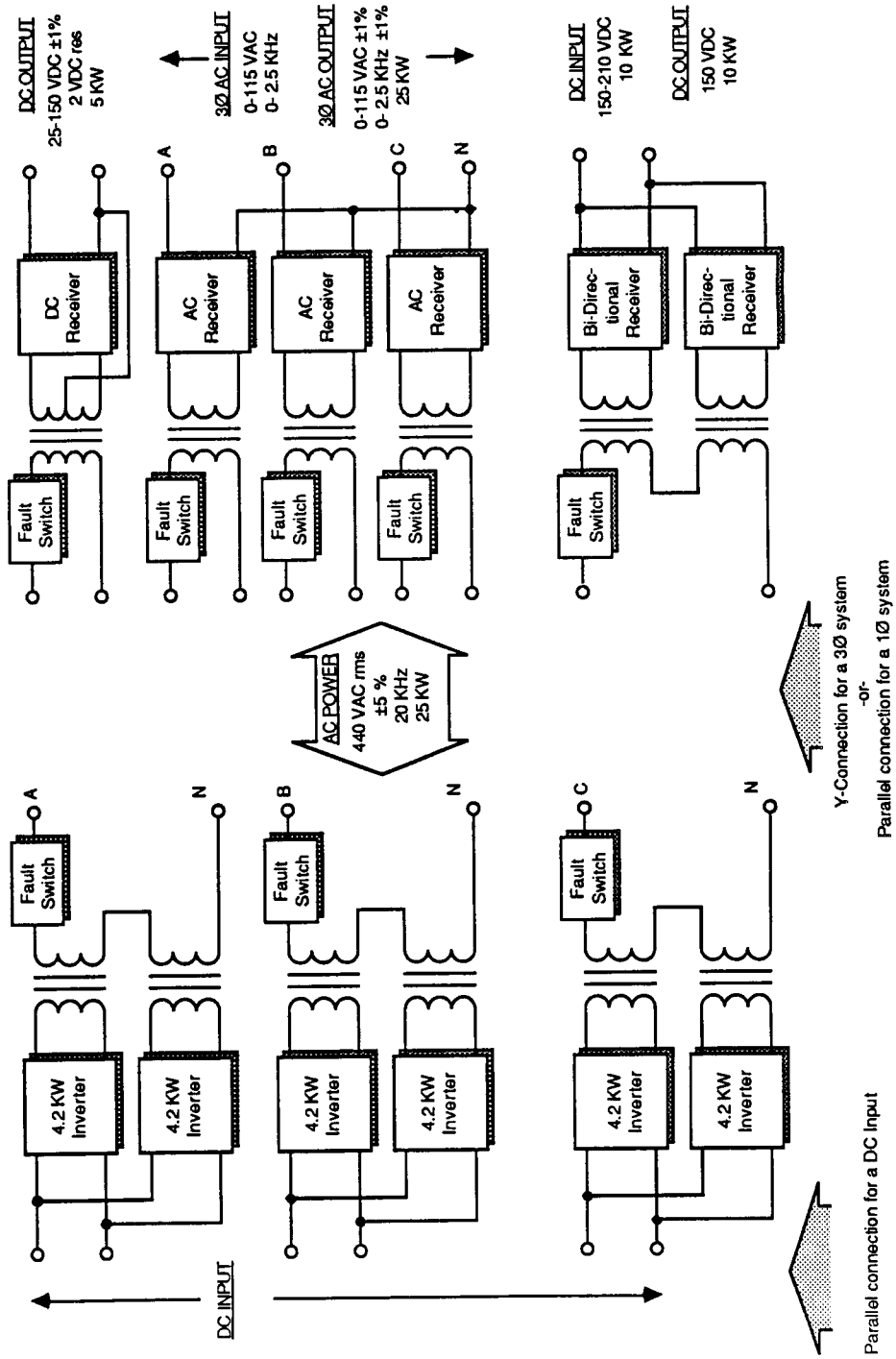
As the program evolved and the Space Station became better defined, some of the requirements for this testbed hardware changed. In addition, some hardware requirements were relaxed to avoid the unnecessary expenditure of resources to exactly meet some work statement detail, once the basic principle of operation had been defined and fully demonstrated. The last two columns of the tables of Appendix B show the subsequent deviations from the original requirements.

3.2 Overall System Design

Overall system design was based on earlier studies and breadboard programs (References 3,4,5,6) performed by NASA and General Dynamics. The primary goal was to provide a Space Station sized demonstration and engineering development testbed of a high-frequency (20-kHz) PMAD system.

That system (see Figure 3-1) included a set of regulating inverter modules to demonstrate multiple source modularity, paralleling, and load sharing, and a matching set of RPC's for fault management and switching. Provisions for RBI monitoring and control were also installed to be able to demonstrate reconfiguration algorithms, during the NASA phases of the testing.

Figure 3-1, Testbed Block Diagram



Fifty meter power distribution busses were included to evaluate transmission line parameters and phenomena.

A representative set of receiver (load interface) modules was also included to evaluate the system impacts of the various likely station loads and to determine any special design considerations or constraints for the users. A three-phase, variable frequency, variable voltage AC receiver and variable voltage DC module were constructed to evaluate low-frequency AC an DC output interfaces. The bidirectional receiver module was required to evaluate the energy storage interfaces and to provide for additional paralleling data when the sources are widely separated and of different character. RPC's were also included at the receiver module inputs to provide for fault isolation. As in the driver case, provisions for RBI monitoring and control were also installed to be able to demonstrate reconfiguration algorithms.

Full computer control, simulating Space Station type operation, was also a major requirement. Imbedded processors were included in both driver and receiver assemblies. Even though the exact type which will selected for the station flight application is not currently known, these imbedded processors were used to define, implement, and test the basic hardware interfaces, control algorithms, and software instructions applicable to this class of hardware. An operator interface was provided, using a MacIntosh™ computer, which communicated with the imbedded computers through a serial data bus, thereby simulating the EPS computer to imbedded computer link for overall command and data functions.

3.3 Predesign

The predesign phase for this program was not the usual evaluation of circuit options in response to requirements of a new design and development task. Since the primary control circuits were previously developed on the BDPCCE contract and the basic power circuit design came from previous IRAD work, this part of the task was reduced to evaluating those designs for appropriateness to meet the requirements of this deliverable testbed hardware, and for highlighting any areas where design changes might be required.

3.4 Control Design

3.4.1 Logic and Interfaces

Digital control functions and interfaces provide for all the basic control of power switch operation, including housekeeping, mode control, frequency synthesis, and clocking and timing. They are consistent with the operation and design developed in the Bidirectional Power Converter Control Electronics (BDPCCE) contract. See Reference 2 for a complete discussion of the design and operation of these circuit modules. Reference 7 is a more general discussion of the control of resonant power processors. Appendix C is a set of hardware schematics, which will show the actual circuits involved.

3.4.2 Analog Control

The output voltage regulation and limiting functions are the only analog control circuits in this hardware. The regulators function as first order closed-loop feedback controllers, with their references provided by computer D-to-A inputs, thereby providing all the flexibility of computer control, and the frequency response and stability of the first order analog system.

These basic designs were also developed in the Bidirectional Power Converter Control Electronics (BDPCCE) contract. See References 2 and 7 for a complete discussion of the design and operation of these circuit modules. Appendix C also contains these schematics.

3.4.3 Computers

See Figure 3-2 for a conceptual drawing of the computer system.

3.4.3.1 Computer System Control Primary Requirements

- Embedded Microprocessor Control
- Interfaces: RS-232, RS-422 serial data busses
- Monitor Analog Data
- Accept Data Bus Commands

- Serial Data Bus Input and Output
- Interface with Testbed Facility System at LeRC
- Self Check

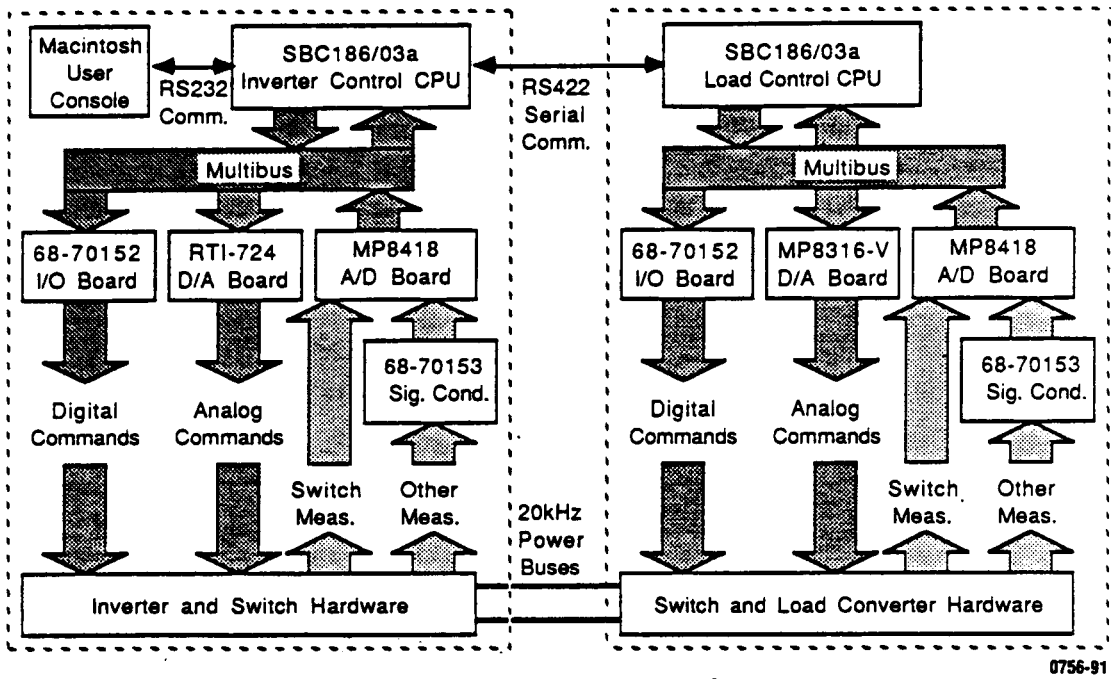


Figure 3-2, Computer System Block Diagram

3.4.3.2 System Control Design Features

- MacIntosh™ supervisory controller and operator interface
- Embedded 8086 type processors in source and load cabinets
- Programmed in Microsoft™ Basic and Intel PL/M™
- Controls all system functions and levels

3.4.3.3 Terminal/Supervisor - This hardware is a MacIntosh™ computer to provide an easy to learn, user-friendly operator interface that has a serial data bus output, simulating the EPS to imbedded computer interface on the Space Station. Full use of the MacIntosh operating environment is provided with pull-down menus, graphics command and monitoring screens and windows, and full mouse control.

Operation of the hardware is fully documented in the Operation and Service Manual provided as one of the deliverables with this equipment, and the reader is referred to that source if he wants additional detailed data.

3.4.3.4 Imbedded Processors - The imbedded computers are Intel SBC 186/03a single board computers, packaged in a Standard Bus card cage. They interface with four other Standard Bus compatible cards, which are the primary interfaces with the power processing hardware. A Burr-Brown™ digital-to-analog converter board provides the set of 16 analog references to be used by the control loops. A Burr-Brown™ analog-to-digital converter board provides 32 channels of analog data monitoring for the basic instrumentation functions. The set also includes two interface boards. An AC,RMS to DC converter board is used to condition the AC input data to a DC form readable by the A-to-D board. A discrete interface board adjusts the 5-volt computer logic signals to the 15-volt levels required by the CMOS system logic hardware, for on-off discretes, mode control commands, etc.

Operation of this hardware is also fully documented in the Operation and Service Manual provided as one of the deliverables with this equipment, and the reader is referred to that source if he wants additional detailed data.

3.4.4 Software

3.4.4.1 Terminal/Supervisor - This is software which runs the operator interface, issues the overall system commands, scales and displays system operating data, and monitors system operational status. It runs on the MacIntosh operator interface computer and is written in Microsoft™ Basic so that it can be easily understood and modified by the user, when he elects to change some aspect of the testbed operation. Figure 3-3 presents an overview of the software design.

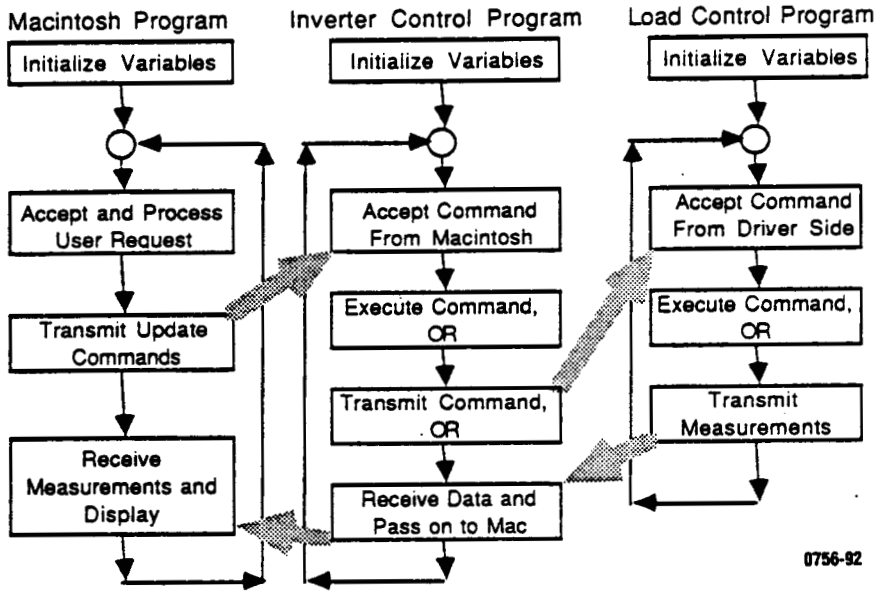


Figure 3-3, Software Block Diagram

This software is fully documented (including flow charts and listings) in the Operation and Service Manual provided as one of the deliverables with this equipment, and the reader is referred to that source if he wants additional detailed data about this software.

3.4.4.2 Imbedded Processors - Since the imbedded computers are Intel™ 8086 type processors, they were programmed in PL/M, a high level language specifically written for this computer version and its development system. As above, this software is fully documented (including flow charts and listings) in the Operation and Service Manual provided as on of the deliverables with this equipment, and the reader is referred to that source if he wants additional detailed data about this software.

3.5 Power Module/Circuit Design

Since the basic power circuit designs were created on IRAD programs and earlier conracts, the details of their design processes will not be recounted here. Additional information may be found in References 5 and 6. The following paragraphs will cover

the primary detailed requirements that the major items of testbed hardware meet, and each of the assembly's important design features.

3.5.1 Resonant Driver (Inverter)

See Figure 3-4 for a conceptual drawing of the inverter power stage.

3.5.1.1 Inverter Primary Requirements

- Input Voltage: 150 to 210-vDC
- Output Voltage: 440-vAC,RMS, ±5.0% single phase or three phase
- Output Power: 25.0-kW, total, maximum
- Output Frequency: 20.0-kHz ±0.1%
- Load Variation: 10% Load to Full Load

3.5.1.2 Inverter Design Features

- Utilizes resonant conversion (in basic "Mapham" configuration)
- "Utility" characteristics
- Phasor regulation for AC output control
- Multiple modules, operating in parallel
- Utilizes control designs from BDPCCE Contract, NAS 3-23878

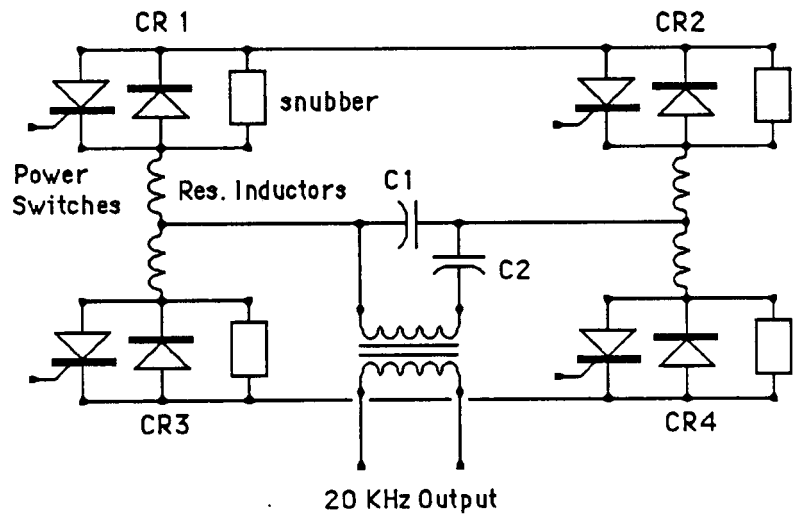


Figure 3-4, Driver/Inverter Power Stage

3.5.2 Source Switches (RPC)

See Figure 3-5 for a conceptual drawing of the switch elements.

3.5.2.1 Switch Matrix (RPC) Primary Requirements

- Turn-on and turn-off with computer/controller command, response less than 100-msec.
- Automatic turn-off based on voltage/current threshold
- Switched Voltage = 762-vAC,RMS ±5%
- Switched Current = 25-amp, AC, RMS max. (real)
- Response time (TBD) = 50-μsec, max.

3.5.2.2 RPC Design Features

- Antiparallel SCR's for series switch element
- Thresholds fully computer controlled
- Source and load switches are the same

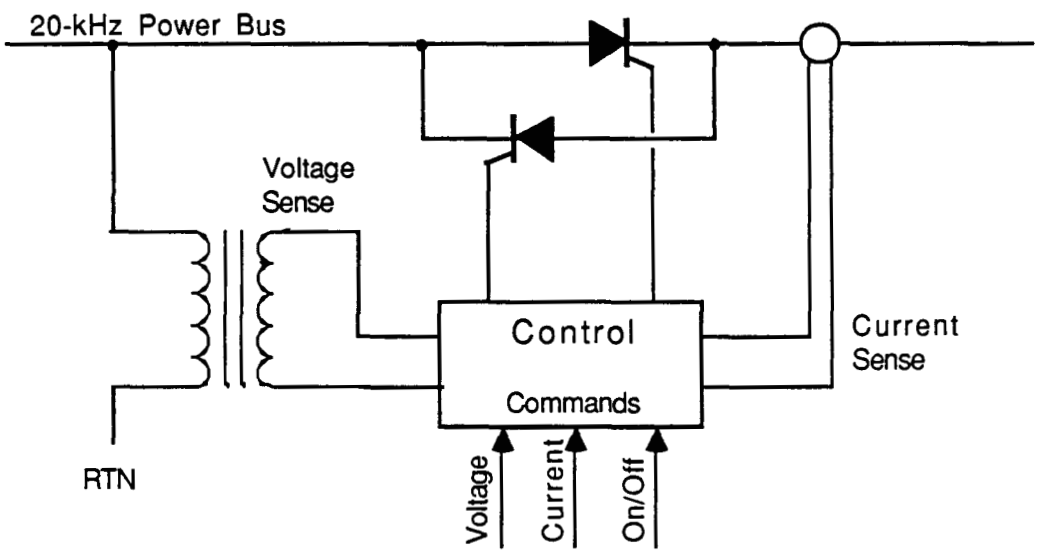
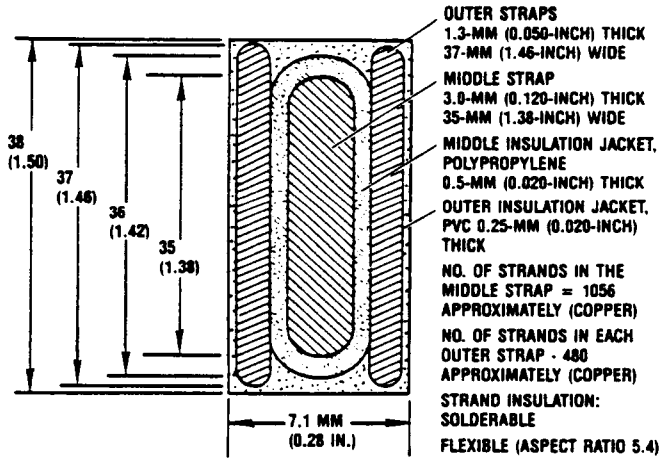


Figure 3-5, RPC Conceptual Schematic

3.5.3 Transmission line

The power bus design for this program focussed on two basic approaches; a twisted pair design done at General Dynamics and a stripline design from Induction General. See Figure 3-6 for a cross section of the NASA/Induction General configuration used in the evaluation testing. The table in the figure lists the important parameters of this design.



CALCULATED LINE PARAMETERS			
		WITH MAJOR INSULATION	
PARAMETER	UNIT	20 MILS	30 MILS
RESISTANCE (100°C)	MΩ/M	1.043	1.043
INDUCTANCE	μH/M	0.027	0.032
CAPACITANCE	μF/M	0.003	0.002
MASS	KG/M	1.102	1.103
LOSSES	WATTS/M	3.755	3.755
IX DROP	VOLT/M	0.203	0.241
CHARGING CURRENT	AMP/M	0.227	0.151
DIELECTRIC STRESSES	VOLTS/MIL	30	20

0756-88

Figure 3-6, Stripline Design Cross Section

3.5.3.1 Power Bus System Primary Requirements

- Three-phase, four wire; or Single-phase, six wire
- Length = 50 meters, minimum
- Voltage = 440-vAC, RMS,±5%

- Current = 25 amp, RMS (normal load)
  50 amp, RMS (fault operation)
- Allowable Losses = 0.5% of load (normal load)
  2.0% of load (fault operation)
- Terminations (TBD) = standard MIL- connectors
- Capacitance (TBD) = 0.30-nfarad/meter (twisted pair design)
- Inductance (TBD) = 0.35-μhenry/meter (twisted pair design)

3.5.3.2 Power Bus Design Features (twisted pair design)

- Shielded, twisted pair configuration
- Constructed of Litz Wire

3.5.4 Receiver Switches (RPC)

See Figure 3-5 .

3.5.2.1 Switch Matrix (RPC) Primary Requirements

- Turn-on and turn-off with computer/controller command, response less than 100-msec.
- Automatic turn-off based on voltage/current threshold
- Switched Voltage = 762-vAC,RMS ±5%
- Switched Current = 25-amp, AC, RMS max. (real)
- Response time (TBD) = 50-μsec, max.

3.5.2.2 RPC Design Features

- Antiparallel SCR's for series switch element
- Thresholds fully computer controlled
- Source and load switches are the same

3.5.5 DC Receiver

See Figure 3-7 for a conceptual drawing of the power output components.

3.5.5.1 Variable Voltage DC Receiver Module Primary Requirements

- Input Voltage = 440-vAC,RMS ±5%
- Input Current = 25-amp, RMS, max. (steady state)

- Input frequency = 20.0-kHz
- Output Voltage = 25 to 150-vDC ±1.0%
- Output Resolution = 2.0-vDC
- Output Power = 5.0-kW, max.
- Output Ripple = 1.0% (max), at full load

3.5.5.2 Variable Voltage DC Receiver Module Design Features

- Basic transformer/rectifier design
- Inductor-capacitor output filter
- Input power factor control
- Output is computer controlled

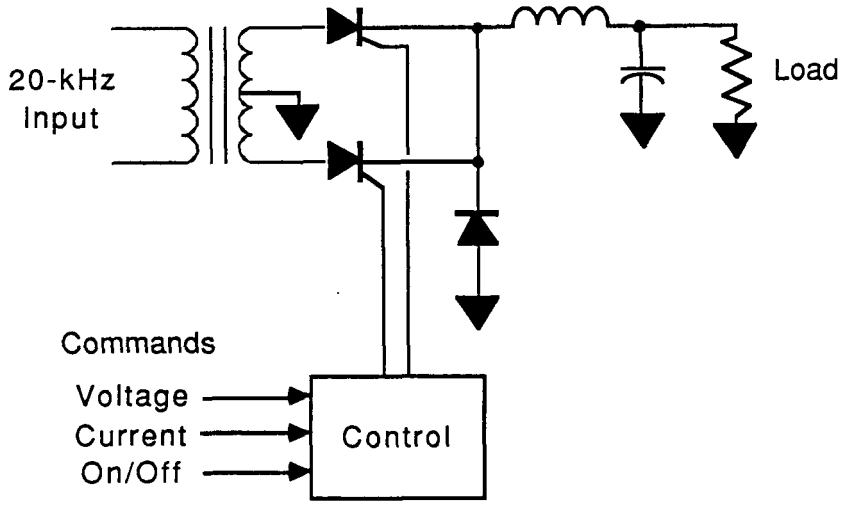


Figure 3-7, DC Receiver Power Output

3.5.6 AC Receiver

See Figure 3-8 for a conceptual drawing of the output connections.

3.5.6.1 Variable Voltage, Variable Frequency, AC Receiver Module Primary Requirements

- Input Voltage = 440-vAC,RMS ±5%
- Input Current = 25-amp, RMS, max. (steady state)
- Input frequency = 20.0-kHz
- Output Voltage = 0 to 115-vAC, RMS ±1.0%, three-phase, Y-connected
- Output Frequency = 13-Hz to 3.3-kHz
- Output Distortion = 5.0%, total, max. (at full load)
- Output Power = 25.0-kW, max.
- Load Power Factor = 0.5, max.

3.5.6.2 Variable Voltage, Variable Frequency AC Receiver Module Design Features

- Basic six-step design
- Inductor-capacitor input filter
- Input power factor control
- Output is computer controlled

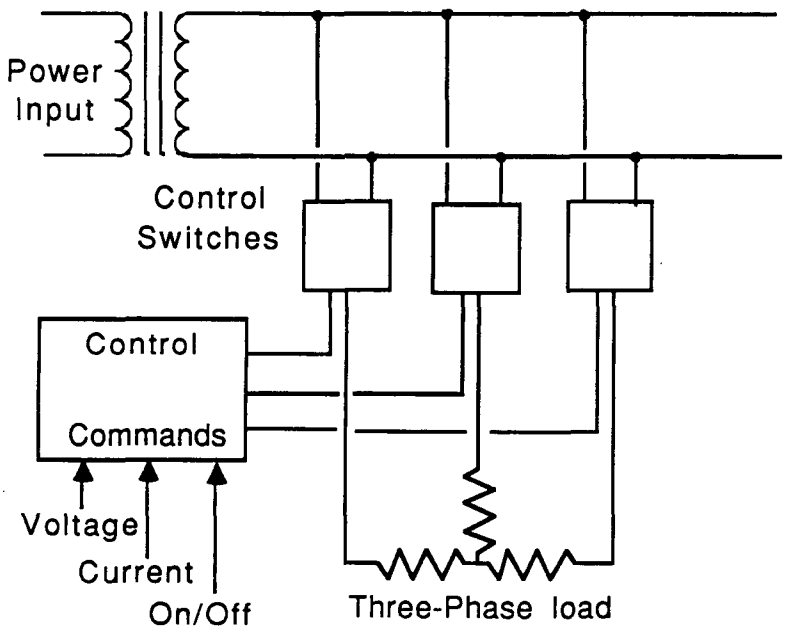


Figure 3-8, AC Receiver Output Switch Configuration

3.5.7 Bidirectional Receiver

See Figure 3-9 to verify the similiarty to the inverter design. The main difference in the power handling stage is that the "flyback" diodes are replaced by SCR's.

3.5.7.1 Bidirectional DC Receiver Module Primary Requirements

- Input/Output Voltage = 440-vAC,RMS ±5%
- Input/Output Current = 25-amp, RMS, max. (steady state)
- Input/Output frequency = 20.0-kHz
- Output/Input Voltage = 150-vDC ±1.0%
- DC Output Resolution = 2.0-vDC
- Output Power = 5.0-kW, max.
- DC Output Ripple = 1.0% (max), at full load

3.5.7.2 Bidirectional DC Receiver Module Design Features

- Basic inverter/bridge design
- Phasor regulation for AC output control
- Inductor-capacitor output filter
- Input power factor control
- Output is computer controlled

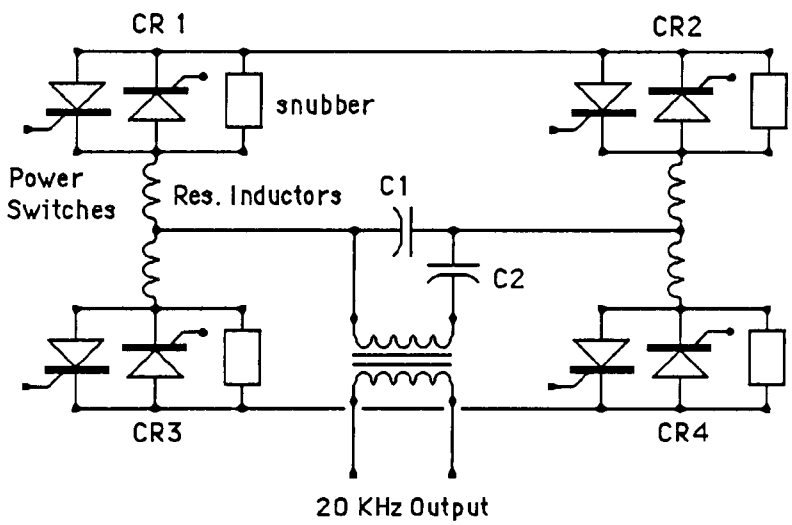


Figure 3-9, The Bidirectional Receiver is similiar to the Inverter.

3.6 Measurements and Instrumentation

3.6.1 Computer Measurements

All DC measurements are appropriately isolated and scaled to be compatible with the 0 to 10 volt range of the Burr-Brown standard bus analog-to-digital converter card. AC measurements are similarly isolated and scaled, but they are connected to the standard bus RMS converter card, where they are converted to scaled DC outputs, readable by the above A-to-D converter board.

High voltage AC measurements are taken through step-down transformers, and AC currents are measured through current transformers, designed specifically for the 20-kHz system frequency. These outputs are scaled and isolated with instrumentation amplifiers where required, and applied to the RMS signal conditioning board.

The high-voltage DC measurements are reduced to appropriate signal levels through a high-impedance resistive divider network, and the DC currents are measured from high-frequency, coaxial current shunts. Both are fed directly to the signal conditioning board.

The computer measurements are obtained from the outputs of the analog-to-digital board which converts the 0 to 10 volt,DC signals to digital values from 0 to 4095. The digital number are then read by the computer, and multiplied and scaled by the appropriate calibration factors. The final results are displayed in engineering units in the measurements window of the MacIntosh interface.

3.6.2 Direct Measurements

Instrumentation points are provided throughout the assemblies for direct readouts of system performance. These signals are intended for connection of appropriate laboratory instruments (input isolation, high voltage, high impedance, etc) and are not scaled, limited, or protected.

Their locations are shown on the appropriate drawings in the drawing and documentation package, supplied with the testbed hardware.

3.7 Mechanical Design

The mechanical design of the delivered hardware is consistent with the testbed operations planned for its final end use. It was placed in roll-out drawers, mounted in standard laboratory "19 inch" racks, enclosed in EMI protective outer cabinets. Control and direct measurement accessibility is from the front of the cabinets, and all inputs and outputs are via standard connectors, mounted on the back panels. Hinged doors provide physical protection and EMI integrity.

3.7.1 Modular Layout

Modules and sub-assemblies were divided based on functional electrical and electronic blocks.

Control wire-wrap and circuit boards were divided into functional blocks developed in the BDPCCE contract. Using this approach separates analog and logic functions into separate sub-assemblies. The logic functions are farther divided into functional blocks that can be common to several drivers or receivers, such as housekeeping, frequency synthesis, input/output, etc., to facilitate later development of a set of standard control blocks, using semi-custom-IC or PAL implementations.

Power devices and associated resonant components were grouped into functional blocks to assess component sizes and layout requirements, so as to provide preliminary information to packaging studies which evaluated and sized expected flight designs.

The actual modular breakdowns and their combinations to construct higher order functions can be examined in the complete report of Reference 2.

3.7.2 Driver Cabinet

The driver (inverter) assembly was housed in a three bay, six foot, standard 19 inch rack size, EMI compatible enclosure. (See Figure 3-10.)

Two bays contain the high power equipment and logic circuits. The inverter power stages and resonant circuit components are arranged with a regulating pair and its output control RPC in each of three roll-out drawers. All their output transformers are mounted in a fourth drawer, at the bottom of the cabinet. High power, 20-kHz connections from individual inverters to their respective output transformers, and from the transformers to the output connectors at the back panel of the cabinet are Litz wire, to minimize skin-effect losses.

The other bay mainly contains all the control circuitry and the imbedded computer for the inverter assembly. The 8086 type imbedded processor and its input and output boards are housed in their own "standard bus" card cage. The logic and control circuitry is assembled on wire-wrap and printed circuit cards, plugged into card cages and interconnected via conventional back-plane wiring and ribbon cables. Drive, feedback, and instrumentation signals are passed between cabinet sections through shielded, twisted-pair, cables. All input and output interfaces are terminated with conventional connectors on the cabinet back panels.

3.7.3 Receiver Cabinet

The basic mechanical arrangement of the receiver assembly is the same as the inverters, and the same basic cabinet type is used. However, because of the lower volume of equipment in the three receivers, the power components are housed in one bay of a two bay set. As in the inverters, all the control circuitry, including the receiver assembly imbedded processor, is housed in its own separate bay. (See Figure 3-11.)

Figure 3-10, Driver Cabinet

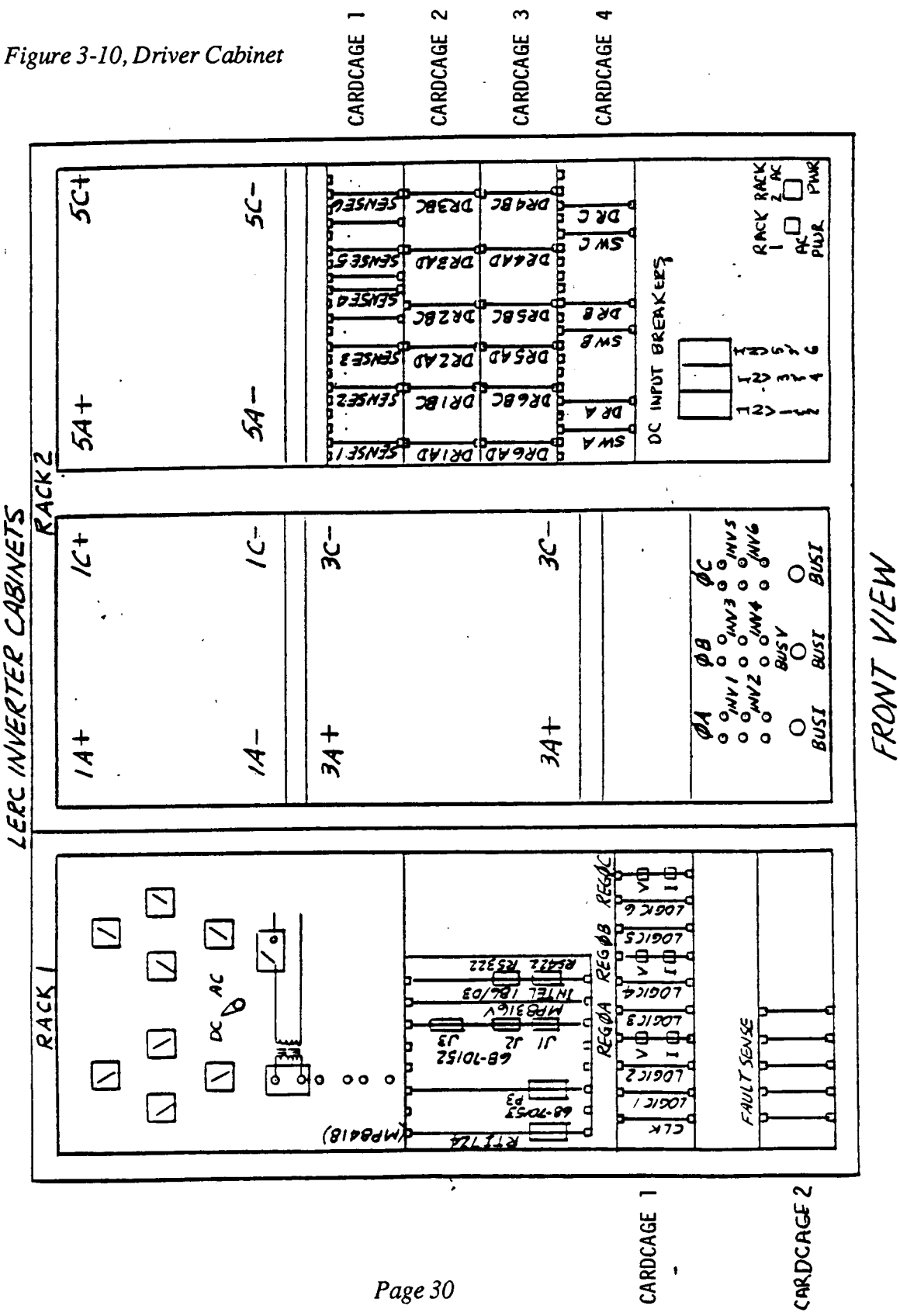
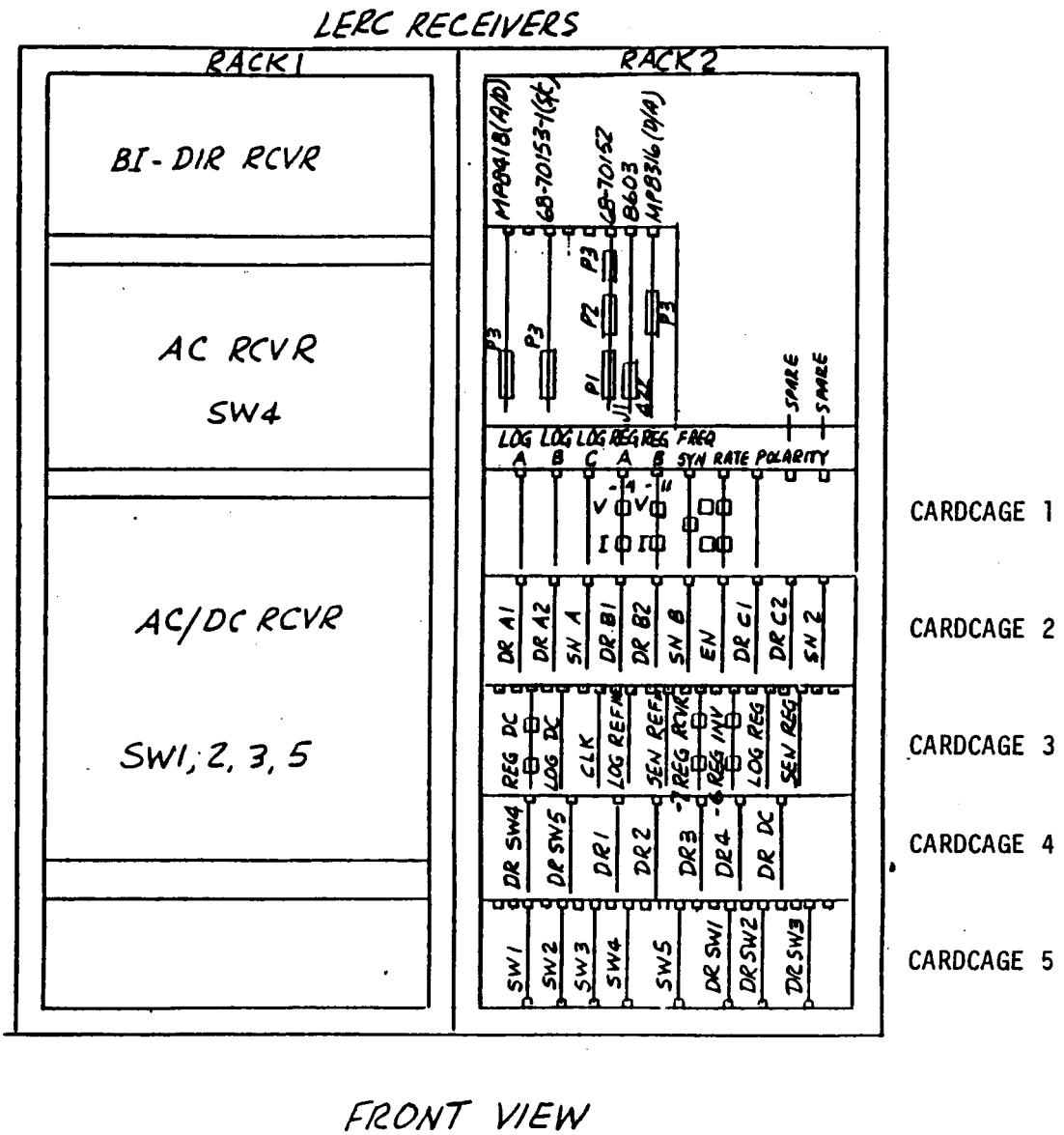


Figure 3-11, Receiver Cabinet



FRONT VIEW

4.3.3 Power Bus Systems

The testbed used two power bus systems during its test program. The first was constructed of round Litz wire, arranged in a set of three shielded, twisted pairs. In this way they could be used in a three-phase distribution configuration, in a single, single-phase bus, or in a paralleled, single-phase bus to verify parallel inductance reduction relationships. This bus system was used for the initial functional testing of the system.

The second bus system was designed and constructed for NASA LeRC by Induction General, and was a flat "stripline" configuration, using Litz braid, with the return enclosing the supply side of the line on both flat sides. (See Figure 3-6.) Because of its improved electrical characteristics, it was supplied to the testbed by NASA and used for all the evaluation and characterization testing.

3.7.4 Thermal Design

Thermal design was conventional for air-cooled, laboratory-type, rack mounted equipment, used in the normal air conditioned, 1-G, laboratory environment. Forced air cooling, using the ambient surrounding air, was chosen for all the cabinets. It was implemented by installing commercial, rack-mounted fans in the bottom of each cabinet, which blow air up through the cabinets and out vents in the cabinet tops.

An "outside-limit" type analysis was performed on the rack with the highest dissipation (inverter power rack) and a dual fan assembly, having an airflow of 300 CFM was selected. The same fan assembly was then used in all the racks, in the interest of commonality.

Cautionary Note: When operating the testbed at full load, the drawers should be in their full "in" positions and the doors should be closed to assure adequate cooling for all the power components.

4.0 Fabrication

4.1 Electronic Piece Parts

All parts used in the construction of this equipment were commercial grade. Integrated circuits were primarily 4000-series CMOS and LS type TTL (at the computer interfaces) in plastic packages. Magnetic components were custom-designed (mostly with ferrite cores, and wound with Litz wire) and and built to breadboard quality, and not potted. While resonant capacitors were selected to be low loss types, special purpose, high frequency, high power custom devices were not used.

4.2 Modules and Sub-assemblies

Wire-wrap circuit boards and power component assemblies were constructed by General Dynamics - Space Systems Division in our avionics assembly area, a special facility used for one-of-a-kind assemblies of this type. Printed circuit boards were manufactured and assembled to commercial standards by local subcontractors to reduce costs on higher quantity sub-assemblies.

4.3 Mechanical Assemblies

The majority of mechanical assembly items were commercial hardware, designed to be compatible with the cabinet/rack system selected. Standard catalog, forced-air heat sinks and power component mounting provisions were used. Standard card cages were selected for the control hardware rack. Small, special purpose parts, such as mounting brackets or protective shields were constructed in our development machine shop.

4.4 Integrated Assembly

Integration and assembly into the final configuration was accomplished in the Space Power Systems laboratory, using research and development type technicians, supervised by Space Power Group engineers.

4.5 Other Considerations

4.5.1 Laboratory Operations

All laboratory operations including part procurement, construction, and testing was controlled and supervised by Space Power Engineering personnel. Actual construction and test tasks were performed by Avionics engineering technicians and assemblers.

4.5.2 Quality Control

Quality standards for construction, inspection, and test were consistent with "good commercial practice". Conformance to these standards was monitored primarily by engineering, with the results observed by the Quality Department on a sample basis. No official monitoring or inspection by the Quality Control Department was required by the contract.

5.0 Testing and Discussion of Results

5.1 Test Plan

Since this hardware is intended for engineering development type operation, no formal, step-by-step test procedure was used for its operation and test. A basic test plan, defining the data that was required for proper evaluation was written, and is included in this report as Appendix D.

5.2 Module and Sub-Assembly Testing

Since the hardware for this program is basically one-of-a-kind, no formal sub-assembly test sets were built, and initial verification of proper operation for the various system modules and sub-assemblies was performed on an informal basis, using standard laboratory test equipment, arranged in breadboard type test setups.

5.3 Integrated System Functional Testing

Once proper operation was established for the system elements, they were interconnected into a system configuration. Functional testing and integration proceeded in a sequential fashion.

5.3.1 Inverters

The inverters were powered and no-load operation was verified for each sub-unit. They were then operated into resistive loads, interconnected and paralleled for shared operation into resistive loads, and the power transmission line attached with the resistive loads moved to its end. Finally, the driver-end RPC's were added to the system and their operation verified. When inverter operation was fully verified under these conditions, receiver modules were added to the system configuration.

During these tests, it became clear that the inverters did not properly share output

loads when paralleled at light loads. Evaluation of the control function for the phasor regulator showed that under some conditions of load and inverter output voltage command, some inverters could sink current supplied by the others. The regulator control circuitry was redesigned, and the control boards changed to improve control of current sharing and to prevent inverters from sinking current.

5.3.2 Switches (RPC's)

When the receivers were added to the system configuration, it was noted that the phase shifts caused by their filters, and the current distortions they reflected to the line caused improper operation of the system RPC's, both at the driver and receiver ends of the power bus. Switch control designs referred the turn-on to either line voltage or current, and there were times and load conditions which made neither the correct reference. Switch control designs were therefore changed to provide DC drives to the antiparallel SCR's of the switch outputs (making them independent of load phase and distortion) and the control boards were reworked to incorporate the new designs.

5.3.3 DC Receiver

When the DC receiver was added to the system configuration, it was noted that high frequency noise caused by the switching of its regulator reflected back to the power transmission system caused enough voltage modulation to cause interference with other receivers. Evaluation of the noise spectrum showed that the current noise was significantly above the requirements of any of the usual EMC specifications. A preliminary input filter was designed and installed, and the interference eliminated. It should be noted that while this design solved the problem for the testbed, the receiver still had unacceptably high third harmonic currents, and the low output impedance of the inverter-transmission line combination eliminated the interference as a problem for this case. Since this filter design would still not meet the requirements of MIL-STD-461 (and other specs), more work must be done for a flight configuration.

5.3.4 AC Receiver

This type of AC three-phase receiver provides for a minimum of current modulation on the 20-kHz power bus, and therefore has a minimum impact on system operation. However, its regulator does have some of the same switching noise shown in the DC receiver, and a similar input filter must be provided. The one in the testbed has the same characteristics and limitations that were described in the DC receiver case.

In addition, the wide range of output frequencies required by this module's specification works well with a motor load, where the load is effectively its own output filter; but wide-band filtering for passive loads is not very practical. Therefore, while the controls for AC receivers may be designed to provide a wide range of output frequencies, the actual range of low frequency AC outputs into passive loads will be limited by the filter requirements.

5.3.5 Bidirectional Receiver

As a DC receiver, the bidirectional receiver has the same high frequency noise/input filter requirements and limitations described in paragraph 5.3.3.

In the source (inverter) mode, this unit was operated from a master clock whose phase at the receiver matched the phase of the line voltage. The current sharing with the inverters could then be controlled by careful adjustment of the output voltage. This method of operation was possible because both inverters and BD receiver were two module phasor regulators powered from similar DC supplies and their phase shifts were about the same. For inverters with different numbers of sub-modules or with significantly different sources, it will also be necessary to add phase control to the regulator control functions. Figures 5-1 and 5-2 are not based on data from this program, but show current sharing (for this class of hardware) as a function of the clock phase and commanded output voltage, and therefore are applicable to this discussion.

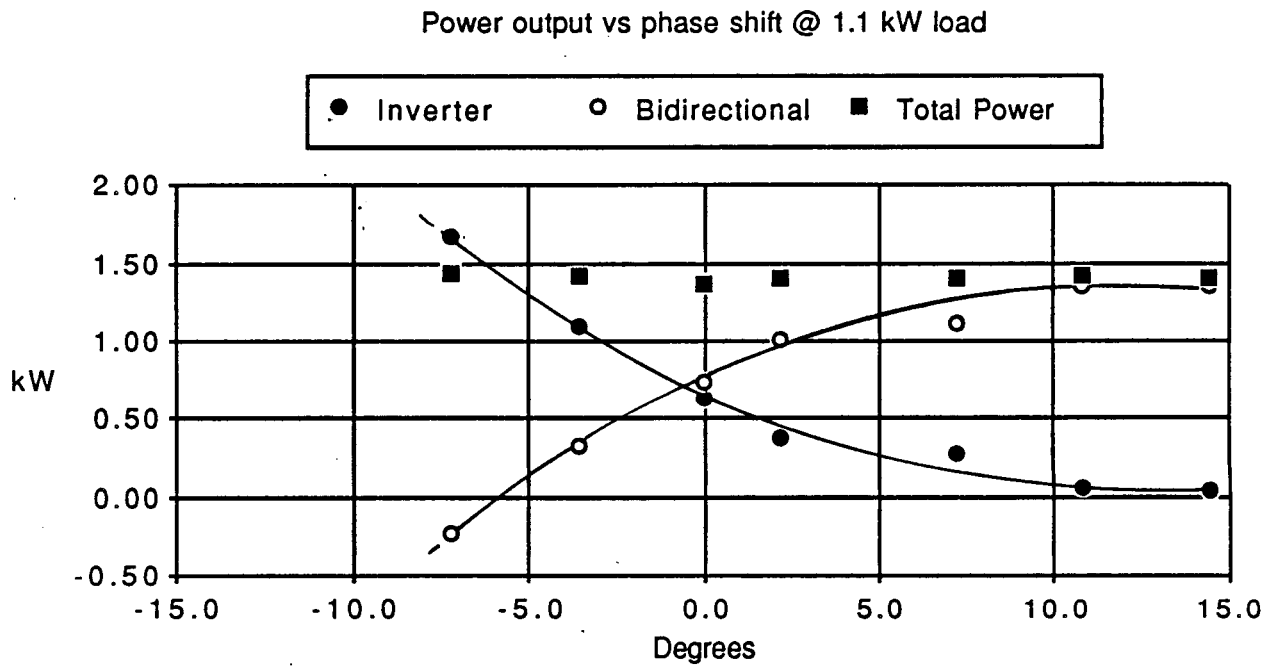


Figure 5-1

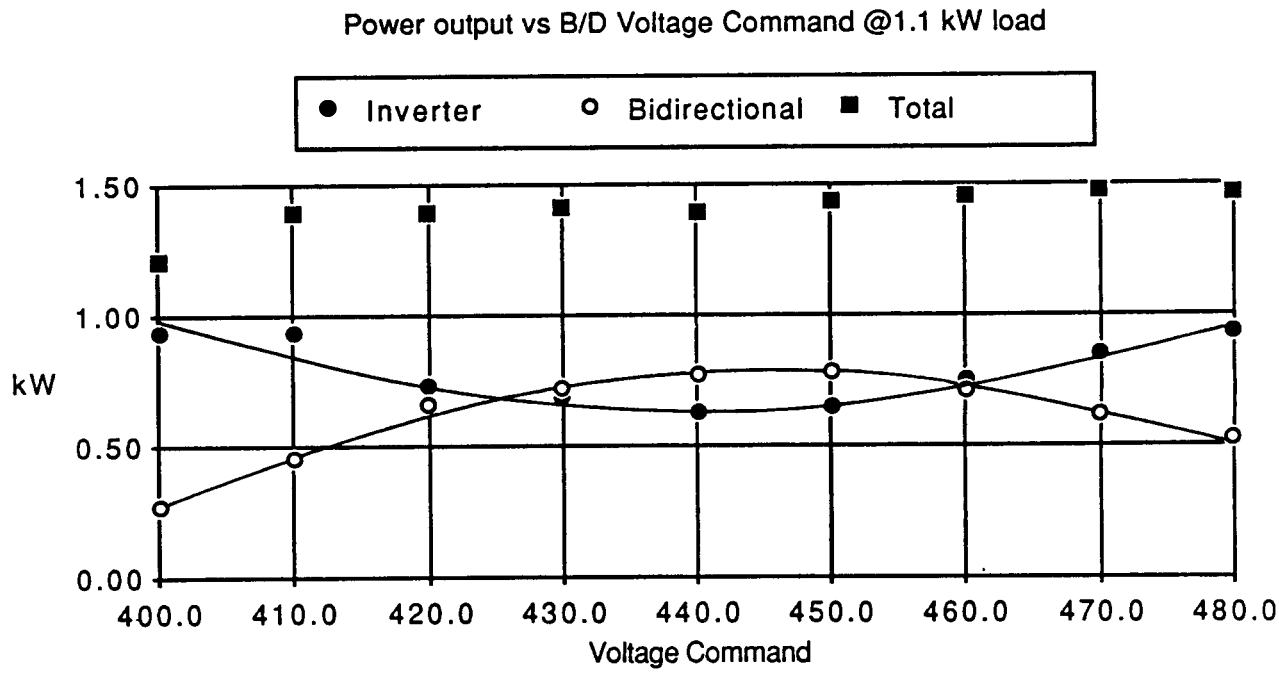


Figure 5-2

5.4 Evaluation and Characterization Testing

5.4.1. Test Procedure

The testing was performed in accordance with the NASA-approved test plan of Appendix D. Because of the engineering evaluation nature of the test program, no further detailed test procedure was used.

5.4.2. Test Results

In addition to the reduced data presented there, comprehensive engineering data was collected and reduced to provide a base for the design of Space Station flight hardware, and to provide a basis for the estimation of its performance.The detailed system configurations, test conditions, and test results are documented in a separate test report (Reference 8). That report also documents any changes that were made during the test or because of the test results, and includes system configuration drawings as appropriate. It also includes copies of the actual test data and waveform photographs.

5.4.3 Summary and Discussion of Important Test Results

a. Efficiency - Inverter efficiencies measured in the testbed averaged 88% for data taken at both General Dynamics and LeRC. Because of the testbed characteristics, this supports the conclusion that efficiencies approaching 95% (at full load) can be achieved for flight designs.

The testbed modules are required to supply 8.3-kW at full load. The actual capability of each regulating inverter is approximately 14-kW. Figure 5-3 shows typical inverter efficiency as a function of load. Important data points are that an inverter with a 20% overload capability will have an efficiency of 95% at full load and 96% at the overload point. Efficiency will be reduced to approximately 92% if it is loaded at the same point as the testbed inverters.

Test and analysis data indicates that snubber circuits in the testbed inverters

to limit dv/dt for the thyristors cost another 3% loss. This is mostly recoverable if energy recovery snubbers are used, or turn-off devices are used to replace the SCR's. Also, turn-off devices such as the IGT or MCT will have lower conduction losses, typically reducing inverter losses another 1%.

Therefore, the corrected efficiency for an improved design can be:

$$\eta = \eta_{meas} + loss_{loading} + loss_{snubber} + loss_{cond}$$

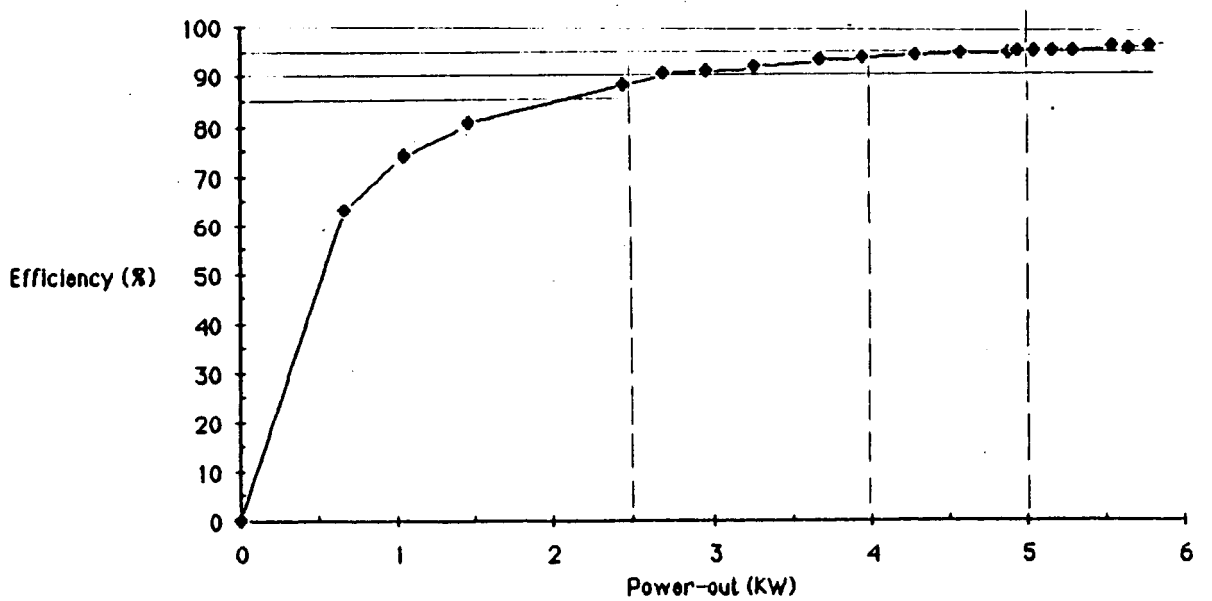


Figure 5-3, Efficiency is load dependent.

b. Power Transmission Bus Stability - Because of predictions and worries expressed in various papers and studies that said 20-kHz bus voltages would be out of control, as loads were attached at different points along long busses, bus voltage was measured for different loads to provide real data, and that data was supported by a computer analysis using the bus parameters measured on a 50 meter sample of the Induction General configuration.

Evaluation of the sample indicated that the bus will have a frequency response higher that 200-kHz. Since the 20-kHz line frequency is therefore at least an order of magnitude below the bus response, a valid model of the

bus can be constructed using a series of lumped parameter sections. This analysis used 5 meter sections and placed resistive, inductive, and capacitive loads at 25, 50, 75, and 100 meters. Figure 5-4 shows the results. The darker curves represent the locus of points for the various loads listed placed along the bus. The worst case occurs when the low power factor loads (+ or - 0.8) are connected at the end of the bus. The bus voltage is always within 10 volts of the nominal 440-vAC, for a worst-case variation of less than 2.5%. The experimental data is about 50% lower than the calculated data, indicating greater damping in the actual system.

It is therefore reasonable to conclude that the 20-kHz bus voltage is well behaved and predictable, with the worst-case excursion from the nomonal voltage less than ±2.5%, with no romote sensing or feedback.

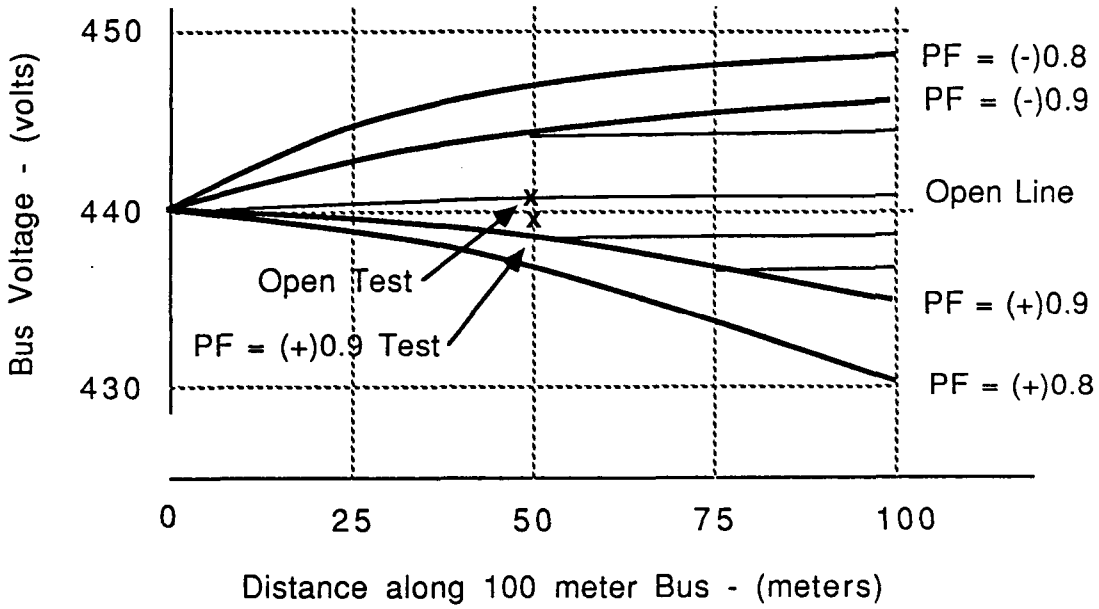


Figure 5-4, 100 Meter Bus voltages are stable and controlled.

c. Power Quality, Interference, and EMI - Power quality and interference between the various users that might be connected to the distribution bus system is a function of the amount of current distortion a

user is allowed to "put back" onto the bus, and the impedance (at the interference frequencies) of the inverters and bus supplying that user.

The test program evaluated voltage distortions for undistorted and highly distorted load currents to measure basic inverter distortion, interference levels, and output impedance as a function of frequency. The distortion data is summarized below:

- Basic inverter distortion is approximately 2.8% at full load
- Full receiver loads (when properly filtered) add only about 0.04% to the basic distortion
- Power bus impedance adds only 0.5% distortion to properly filtered receiver loads
- Low total source impedance near the 20-kHz power transmission frequency minimizes any effects from low order harmonic currents

Output impedance characteristics were measured by comparing the magnitude of output voltage at the harmonic frequencies of interest with the load current at the same frequency. Figure 5-5 shows the magnitudes of the impedances at the low harmonic frequencies, plotted on the calculated values. The log magnitude scale on the abscissa is referred to 10 ohms. As you would expect, good agreement is evident at the lower frequencies, and experimental data and calculated values start to deviate from one-another at the higher frequencies, where circuit strays, not used in the model, become more important.

The main significance of the data taken during this test is that if load input currents are filtered well enough to meet the requirements of the typical flight EMI/EMC specifications, the power bus voltage total harmonic distortion can be easily kept within 3% of the fundamental value.

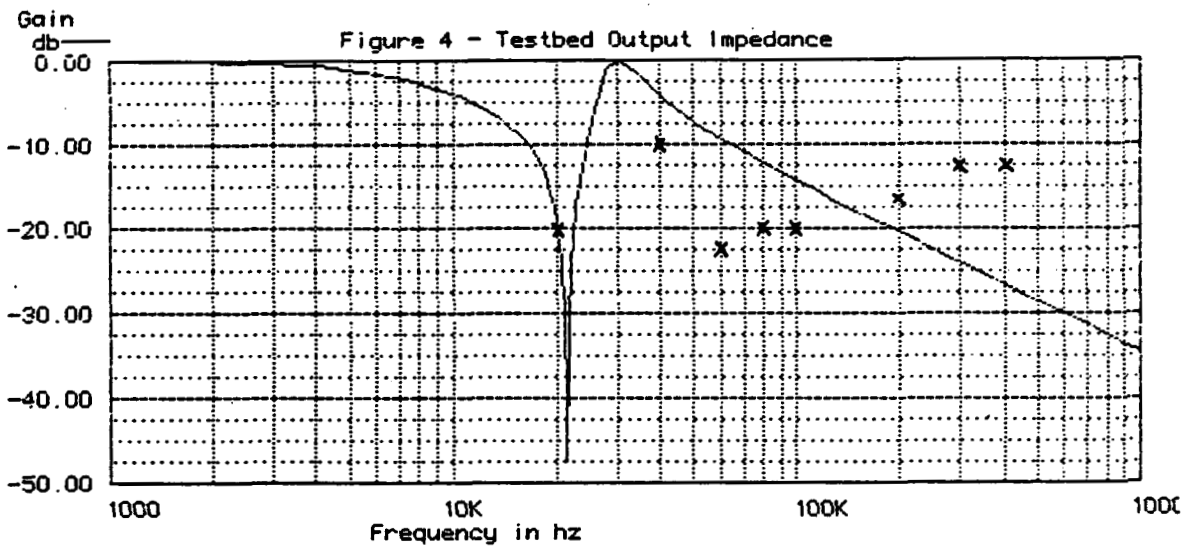


Figure 5-5, High Frequency output impedance is low.

d. Overloads and Short Circuits - The testbed has demonstrated that steady-state limits and overloads can be controlled by the active phasor regulation loops. A current limit phasor regulation loop provides positive control of the output current, and has a response time of approximately 30-mSeconds. The current control function is an analog loop, with computer controlled references, which allow for different fault control modes

- Hard limit for fault current, and shift critical loads to another bus
- Computer or operator elects to raise the limit and try to continue to power the loads
- Computer or operator elects to raise the limit to a value high enough to burn-out the fault, in an attempt to clear it.

Transient limiting, above the frequency of the regulation loop is provided by the series output capacitor in each invertr transformer primary. Its value is selected to allow the bridge to continue to operate (by keeping the natural resonant frequency safely above 20-kHz) even if the output is shorted. Obviously, it can then accomodate any loads less than a short circuit.

e. Low Power Factor Loads - Since low power factor loads usually reflect into the resonant network for this class of power processors, previous designs were intolerant of that type of load. This testbed's extrapolation of the basic technology resonant technology accommodates low power factor loads as follows:

Capacitive Loads:
- Are isolated by the series output capacitor.
- Frequency Effects are limited by the value of the series output capacitor, since adding capacitance in series results in lower total capacitance seen by the resonant network.
- There is no effect until the capacitive loads are large enough to become overloads and are actively limited by the regulation loop current limit.

Inductive Loads:
- Are partially isolated by the series output capacitor.
- Since an inductor is effectively a minus capacitor, it can effectively reduce the value of the series output capacitor, and if large enough, cancel its isolation and change the natural resonant frequency. A higher natural frequency increases output distortion. In the testbed, the capacitor is sized so that there are no frequency effects above Power Factors of 0.7
- Testing has shown that for very low inductive power factors (less than 0.5), possible driver logic inhibits can cause output failures.

5.5 Final Acceptance

The official, final acceptance test was performed at LeRC, after the testbed was shipped and installed, and returned to operating condition. The test was performed and proper operation was verified by LeRC personnel, using a detailed procedure written at LeRC, based on selected portions of the test plan. Those tests are documented in a LeRC report. (See Reference 9.)

6.0 Deliverables

6.1 Documentation

6.1.1 Engineering Drawings, Electrical and Schematics
Delivered with testbed hardware
6.1.2 Engineering Drawings, Mechanical
Delivered with testbed hardware
6.1.3 Engineering Drawings, Wiring Interconnection
Delivered with testbed hardware
6.1.4 Test Plan
Delivered and approved prior to testing
6.1.5 Test Report
Delivered herewith
6.1.6 Operating Procedures Manual
Delivered with testbed hardware
6.1.7 Final Report

6.2 Hardware

The following specific items, called out by the latest contract revision, comprise the AC Power System Testbed of this contract and were delivered to NASA LeRC in August of 1987.

6.2.1 Driver assembly Enclosure
6.2.2 Receiver Assembly Enclosure
6.2.3 Power Bus System
6.2.4 Inverter/Driver Modules
6.2.5 Load Control and Fault Isolation Switch Matrix
6.2.6 Driver/Bus Control Switch Matrix
6.2.7 Bidirectional Receiver
6.2.8 DC Receiver
6.2.9 Three Phase AC Receiver

6.2.10 System Controller
6.2.11 System Software

6.3 Installation and Checkout at LeRC

Installation and checkout of the hardware was accomplished in the AC Power System test facility at Lewis Research Center by NASA personnel, with assistance, as required, from General Dynamics/Space Systems Division, Space Power Systems engineering personnel. This has been verified by successful completion of the final acceptance test in the NASA facility, and a hardware demonstration as part of the final report on 20 October, 1987.

7.0 Conclusions and Recommendations

7.1 Conclusions

The following are the significant conclusions about this hardware, as demonstrated by this development, construction, and test program. They are divided into sections for each major testbed hardware element, and include the program's major accomplishments and lessons learned for each.

7.1.1 Inverters

The significant hardware developments that were proved in this program are:

- Overload control
- Regulation
- Output impedance control and its effects on interference
- Distortion and EMI/EMC compatibility
- Paralleling and current sharing
- Computer control capability and algorithms

Lessons learned which impact future hardware designs are:

- Turn-off type switches offer significant improvements in operation and performance in the areas of, Efficiency, Reliability, and Control.
- Regulator designs must be improved to include better line regulation and positive control of current sharing.
- Resonant network designs must be compensated to accommodate the maximum phasor separation at maximum load and maximum input voltage.
- Maximum efficiency occurs at full-load

7.1.2 Bus Control Switch Matrix and Load Control Switch Matrix

The significant hardware developments that were proved in this program are:

- RPC demonstration
- Overload control
- Less than 100-μsecond response

- Computer control capability and algorithms

Lessons learned which impact future hardware designs are:

- Turn-off type switches offer modest improvements in operation and performance for efficiency, reliability, and control.
- Semiconductor switch capacitance is an important design consideration for reactive load isolation.
- Load Power Factor-effects drive thyristor design implementations toward DC drives with synchronized turn-on and turn-off.

7.1.3 Transmission Lines

The significant hardware developments that were proved in this program are:

- Definition and identification of configuration dependent characteristics
- Regulation and stability demonstration
- Line impedance control and its effects on interference
- Distortion effects and EMI/EMC compatibility

Lessons learned which impact future hardware designs are:

- Stripline or flat configurations offer the best control of characteristics for long lines.
- Capacitance effects can be compensated, if necessary.
- High surface area configurations (Litz wire or foils) should be used to minimize losses in long lines.
- Conventional wiring can be used for short (inside station modules or units) interconnections.

7.1.4 Bidirectional Receivers

The significant hardware developments that were proved in this program are:

- Overload control (in both directions)
- Phase delay regulation (as a receiver)
- Output impedance control and its effects on interference (when used as a source)

- Distortion and EMI/EMC compatibility, both when used as a source, and reflected to the line when supplying a load
- Paralleling and current sharing with Inverters (when used as a source)
- Computer control capability and algorithms

Lessons learned which impact future hardware designs are:

- Same as inverters when used as a source (see Paragraph 7.1.3).
- Control of clock phase is required for different sources, either with positive phase control of a master clock input, or with a phase-locked loop, synchronized to the line.
- Clock phase can be used to control the operational mode, and change the character of the receiver's operation from source to load.

7.1.5 DC Receivers

The significant hardware developments that were proved in this program are:

- Overload control
- Phase-delay regulation
- Transformer-Rectifier-Filter configuration verified
- Input filter requirements defined
- Computer control capability and algorithms

Lessons learned which impact future hardware designs are:

- A critical value output inductor is required for 20-kHz input current control.
- A flyback diode is required to prevent the output filter from reflecting its power factor to the input.
- An input filter is required to limit the high frequency line current distortion for EMC and interference control.

7.1.6 Three-phase AC Receivers

The significant hardware developments that were proved in this program are:

- Overload control
- Regulation
- Basic motor control verified

- Distortion and EMI/EMC compatibility is controlled for the three phase configuration
- Twelve-step configuration (two-on/one-off and three-on states)
- Computer control capability and algorithms

Lessons learned which impact future hardware designs are:

- Pulse population modulation provides improved control and frequency resolution for the AC outputs.
- Phase delay regulation is possible and reasonable if pulse population does not have sufficient resolution.
- Population and regulation control approaches which use an AC reference voltage provide improved low frequency AC output control.

7.2 Recommendations

7.2.1 Testbed Related

a. Upgrade the testbed to include hardware (especially for the inverters) that incorporates turn-off type devices for the main power switching components. Use MCT's, IGT's, FET's, or bipolar transistors instead of SCR's, to improve efficiency and simplify drive and protection circuitry.

b. Upgrade the testbed regulator control boards to newer designs which include clock phase control for positive control of current sharing, and improved gain characteristics for improved bus voltage control performance.

7.2.2 Generic 20-kHz Hardware Related

a. Where possible hardware designs (especially for the inverters) that incorporate turn-off type devices for the main power switching components should be used. Use MCT's, IGT's, FET's, or bipolar transistors instead of SCR's, to improve efficiency and simplify drive and protection circuitry.

b. High surface area wiring configurations (Litz wire or flat foils) should be

used to compensate for skin effect in long power busses to minimize losses and/or conductor mass. Flat braid or stripline configurations provide the best management and control of line parameters. Conventional wiring may be used for short runs (inside modules or units) or low power applications. Twisted pair configurations will minimize interference and pickup in these conventional wiring applications.

c. RPC's and RBI's - must be designed to accommodate very low power factor loads, even though spec limits on users normally would control input power factors. Connecting to an unloaded power bus is probably the worst case (power factor < 0.1), even though it is a small load.

d. EMI/EMC - The intent of the classical EMI/EMC specifications (such as MIL-STD-461 and MIL-STD-462) should be applied to load interface hardware attached to the 20-kHz power bus. When they are required, the vehicle system power quality should be in the 3% THD range.

e. Transformers - Non-linear elements (switches, rectifiers, etc.) and transients in utility systems of this type can often cause AC unbalances which appear as a net DC term in the current. Therefore, even though this is an all AC system, transformers and other magnetic components should be designed to accommodate some reasonable percentage of DC to avoid saturation effects.

8.0 References

8.1 **"An SCR Inverter with Good Regulation, Sine-Wave Output"**; Neville Mapham; IEEE Transactions on Industry and General Applications; IGA-3, No.2, Apr-May, 1967.

8.2 **"Bidirectional Power Converter Control Electronics"** , Final Report; NASA CR 175070, NAS 3-23878; J.W.Mildice, General Dynamics - Space Systems Division.

8.3 **"Study of Power Management Technology for Orbital Multi-100kWe Applications"**; Final Report, NASA CR 159834; J.W.Mildice, General Dynamics, Convair Division

8.4 **"Study of Multi-Megawatt Technology Needs for Photovoltaic Space Power Systems"**; Final Report, NAS 3-21951; D.M.Peterson, General Dynamics, Convair Division

8.5 **"20-kHz, Proof of Concept Test Program"**; Final Report, NAS 3-22777; Loran J. Wappes, General Dynamics - Space Systems Division

8.6 **"Fault Tolerant AC Power Processing"**; Final Report, GDC-ERR-83-212; Loran J. Wappes, General Dynamics - Convair Division, December, 1983

8.7 **"Control Considerations for High-Frequency, Resonant Power Processing Equipment Used in Large Systems"**; J. W. Mildice, Proceedings of the IECEC, August 10-14, 1987 (NASA Technical Memorandum 98226; AIAA-87-9353)

8.8 **"Performance Test Report, LeRC AC Power System Testbed"**; Contract NAS 3-23878; R. Sundberg, General Dynamics - Space Systems Division, November, 1987

8.9 **"Acceptance Test Report for 20-kHz Power Testbed"**; Contract NAS 3-24399; Frederick J. Wolf, NASA LeRC, 30 September, 1987

8.10 **"Bidirectional Four Quadrant (BD4Q) Power Converter Development"**, Final Report, NASA CR 159660, F.C.Schwarz, Power Electronics Assoc. Inc.

8.11 **"Controllable Four-Quadrant AC to DC and AC Converter Employing an Integral High Frequency Series Resonant Link"**; U.S.Patent 4,096,557, June, 1978

8.12 **"A Practical Resonant Converter Using High Speed Power Darlington Transistors"**; Suridar R. Babu, General Electric Co., Auburn, NY, PCI March, 1982 Proceedings, pp 122-141

8.13 **"Advances in Series Resonant Inverter Technology and Its Effect on Spacecraft Employing Electric Propulsion"**; R.R.Robson, Hughes Research Labs, Malibu, CA, presented at AIA/UASS/OGLR 16th International Electric Propulsion Conference, November, 1982.

APPENDICES

Appendix A

Contract Work Statement

This Appendix is a copy of Section C of the contract for this program, "Description/Specification/Work Statement" for the AC POWER SYSTEM TESTBED. It is reproduced here to define the system baseline at the beginning of the program. See Appendix B for a digest of the subsequent contract changes.

PART I - THE SCHEDULE

Section C
Description/Specifications/Work Statement

AC POWER SYSTEM TESTBED

EXHIBIT A
STATEMENT OF WORK

I. Introduction

The Space Power Technology Division of the Lewis Research Center is establishing a Space Power Testbed facility to evaluate candidate power systems and components for space power and Space Station applications. The high frequency, resonant circuit driven, a.c. power system is a high priority candidate power system. The contractor has developed it to its present state where it is operational as a three-phase, high voltage, high frequency power system at a 5 kW power level. The intent of this program is to upgrade the system to a power capability of 25 kW for evaluation in the testbed. This a.c. power system is unique in that it inverts d.c. power from a solar array or other d.c. source to sinusoidal a.c. power at a high frequency and high voltage, and transmits this power through redundant transmission lines to diversified user loads. The combination of high voltage and high frequency in conjunction with essentially lossless power semiconductor switching results in high overall system efficiency and low overall system weight. The total system consists of a resonant driver stage that inverts the d.c. imput voltage to 20 kHz, 440 volts a.c. three-phase power at a power level of 25 kW, a bus control fault isolation switch matrix to connect the three-phase power to either or both redundant transmission lines, and a load control and fault isolation switch matrix to connect the user loads to the system. The load interface devices include an a.c.-to-variable voltage-d.c. converter that provides 5 kW of regulated d.c. power at a voltage level in the range from 25 to 150 volts, a.c. inverters to provide 25 kW of three-phase variable frequency, variable voltage, a.c. power at a voltage from zero to 115V rms line-to-neutral and frequency from zero to 2.5 kHz, and a bi-directional converter. The bi-directional converter function as a power receiver in the forward direction to convert the 20 kHz power to d.c. to charge an energy

storage battery and as a driver in the reverse power flow direction to provide 20 kHz a.c. power to the system from the battery. Control and protection of the entire system is supervised by a micro-computer. The system components are modular in nature thereby facilitating expansion to higher power levels.

This Statement of Work details the tasks to upgrade the system power level and produce the hardware for the testbed facility.

II. Objective

The objective of this work is to design, build, test and deliver a 25 kW high frequency a.c. testbed system for evaluation as a high priority candidate concept for the Space Station electric power system and other future space missions. System design will be based on the 20 kHz resonant inverter driven concept.

III. Scope

The work to be accomplished is the design, fabrication, test, and evaluation of a testbed resonant circuit driven, high voltage, high frequency a.c. power system as defined and specified under the requirements of this S.O.W. and to assist with the installation and initial operational checkout tests of the testbed at the LeRC. The resources to be furnished by the contractor consist of all personnel, services, materials, supplies, computational, fabrication, and test facilities necessary to perform the above types of work.

IV. Requirements

A. General System

1. The a.c. power system testbed shall consist of the following modular components:

a. A Type 1 inverter/transformer driver module to convert

simulated solar array d.c. voltage in the range of 150 to 300V d.c. to 25 kilowatts, three-phase a.c. power at 20 kHz frequency and rms line-to-neutral voltage of 440 volts

b. A Type 2 inverter/transformer driver module to convert 440V a.c. (line-to-line) three-phase, 60 Hz a.c. power to 25 kW a.c. power, three-phase, 20 kHz, 440V a.c. line-to-line neutral.

c. A source bus control fault isolation switch matrix for interconnection of the driver module output to both or either of two transmission busses.

d. Two redundant transmission power busses, each rated for 25K watts.

e. One user load control and fault isolation switch matrix for interconnection of user loads with the power busses.

f. System control, containing a microprocessor controller with analog and serial data bus input/output. The controller shall control the source and load matrix switches and provide overall fault tolerant and fault protective system operation. The microprocessor and associated software shall be compatible with and interface with the testbed facility control system at LeRC.

g. Five user load receiver modules:

(1) One bi-directional converter module to provide forward and reverse power flow between the a.c. system power power busses and an energy storage battery.

(2) One d.c. converter module to provide variable d.c. voltages of +25V d.c. to +150V d.c. from the 20 kHz, three-phase power busses.

(3) Three (3) three-phase variable voltage variable frequency a.c. modules to provide three-phase output power at variable frequency of 0 to 2.5 kHz and variable voltage of 0 to 115V a.c. rms, line-to-neutral. The output shall be four wire wye connected to interface with the three-phase power lines and neutral wire in the transmission busses.

2. The system shall function to convert the d.c. power from a simulated solar array or other d.c. source, or from a 60 Hz commercial power source, to 25 kW three-phase a.c. power at 20 kHz frequency and 440V a.c. rms line-to-neutral voltage. This power is to be transmitted through a bus control fault isolation switch matrix, two redundant three-phase, four-wire transmission line busses, and a load control and fault isolation switch matrix to the user load receiver modules described in g. above.

3. The system shall be designed for lightweight, high efficiency, and to provide autonomous, fail operational and fail safe (for internal system faults), and fail safe (for load faults) system operation. It shall be designed for minimum electromagnetic radiation and susceptibility in accordance with MIL STD 461. The system shall be modular to facilitate expansion to higher power levels.

B. System Component Modules

1.0 Three-Phase Driver/Inverter Modules -

Each module shall be a full-bridge type, series resonant inverter, operated in the voltage-source mode.

The three individual single phase modules which comprise a three-phase module shall be synchronized from a redundant external clock with appropriate three-phase drive pulses and with outputs interconnected at their output transformer secondaries to drive the three-phase bus system.

Electronic interface specifications include:

1.1 Module Type 1:

- Input voltage - 150V d.c. to 300V d.c.
- Power source impedance - power supply or power array.
- Output voltage - 440V a.c., rms ±5.0% (at the transformer secondary, line-to-neutral).
- Output power - 25.0 kW (total, three-phase) max., steady-state.
- Output frequency - 20.00 kHz ± TBD %, (TBD in Task 1).
- Load variation - 10% load to full load.
- Synchronization signal - compatible with CMOS logic levels 20.0 kHz ± TBD %, (TBD in Task 1).

1.2 Module Type 2:

- Input voltage - 440V a.c. (line-to-line), three-phase, 60 Hz, a.c.
- Power source impedance - standard commercial utility power.
- Other parameters are the same as module Type 1.

Type 2 modules and the a.c. modules of 5.2 will be capable of operating as a separate motor control unit.

2.0 Bus Control Switch Matrix -

Each element shall be an a.c. semiconductor remote power controller capable of connecting or disconnecting a driver module to/from the system power bus.

The control shall operate in one turn-on and two turn-off modes:

- Turn-on is to be from a system computer/controller command.

- Emergency turn-off is to be automatic, based on a combination of voltage and current sensed at the load module, and occurs in less than 1.0 cycle of the power bus frequency.
- Controlled turn-off from a system computer-controller command based on an evaluation of system performance shall occur in less than 100 m sec.

Electronic interface specifications include:

- Switched voltage: 762 vac., rms $\pm$ 5.0%.
- Switched current: 25.0 amp, rms, max. (real).
- Frequency: 20.0 kHz.
- Command inputs: Compatible with CMOS logic levels.
- * Maximum voltage drop for switch: TBD.
- * Reactive current: TBD, max.
- * Turn-on transient: TBD.
- * Response time: TBD.

*These parameters to be determined in Task 1 based on test results from the contractor's present breadboard system and verified by tests in subsequent tasks.

3.0 Power Busses -

The power busses shall be two parallel busses, sharing the loads under normal operating conditions, and each capable of operating to supply the full load requirement when operated alone. Each bus shall be a three-phase, 4-wire transmission line designed for minimum electromagnetic radiation and susceptibility.

Electronic interface specifications:

- Length: 50 meters.
- * Diameter: TBD.
- Voltage (line-to-neutral): 440V a.c., rms ± 5.0%.
- Current: 25.0 amp, rms (normal operation); 50.0 amp, rms (fault operation).
- Allowable losses (at 50 meters): 0.5% of load (normal operation); 2.0% of load (fault operation).
- * Terminations: TBD.
- * Capacitance: TBD.
- * Inductance: TBD.

* These parameters to be determined in Task 1 and verified by tests in subsequent tasks.

4.0 Load Control Switch Matrix -

Each element shall be an a.c. semiconductor remote power controller capable of connecting or disconnecting a load module to/from either or both system power busses.

The control operates in one turn-on and two turn-off modes:

- Turn-on shall be from a system computer/controller command.
- Emergency turn-off shall be automatic, based on a combination of voltage and current sensed in the switch, and shall occur in less than 1.0 cycle of the power bus frequency.
- Controlled turn-off from a system computer-controller command based on an evaluation of system performance shall occur in less than 100 m sec.

Electronic interface specifications include:

- Switched voltage: 762 vac., rms ± 5.0%.
- Switched current: 25.0 amp, rms, max.
- Frequency: 20.0 kHz.
- Turn-on transient: TBD.
- Maximum voltage drop for switch: TBD.
- Command inputs: Compatible with CMOS logic levels.

* These parameters to be determined in Task 1 and verified by tests in subsequent tasks.

5.0 Load Modules -

5.1 Variable Voltage D.C. Module:

Converts the bus outputs to regulated d.c. for general usage.

Electronic interface specifications:

- Input voltage: 440V a.c. rms ± 5.0%, line-to-neutral.
- Input current: 25.0 amp, rms, max., steady-state.
- * Transient input current: TBD.
- Input frequency: 20.0 kHz.
- Output voltage: +25.0 to +150.0V d.c. ± 1.0% (with 2.0V d.c. resolution).
- Output power: 5.0 kW, max.
- Output ripple: 1.0% max. (at full load).
- Control inputs: Compatable with CMOS Logic levels and interface specifications.

5.2 Variable Voltage, Variable Frequency A.C. Modules:

Convert the bus outputs to regulated a.c. variable frequency for general a.c. usage, including motor control.

Electronic interface specification:

- Input voltage: 440V a.c., rms ±5.0%, three-phase, line-to-neutral.
- Input current: 25.0 amp rms, max., steady-state.
- Transient input current: TBD.
- Input frequency: 20.0 kHz.
- Output voltage: zero to 115V a.c., rms (line-to-neutral) ±1.0%, three-phase.
- Output frequency: zero to 2.5 kHz ±1.0%.
- Output distortion: 5.0% max. total (at full load).
- Output power: 25.0 kW max.
- Load power factor: 0.5 max.
- Output ripple: 1.0% max. (at full load).
- Control inputs: Compatible with CMOS logic levels and interface specifications.

5.3 Bidirectional Converter Module:

Operates in two distinct modes:

1. As a d.c. receiver with output regulation control based on an external command from the system computer/controller, which may be based on battery pressure, battery current, battery voltage, or any combination of those parameters (when used as a battery charger).

2. As a system driver/inverter module operatiang from the battery that has been charged with outputs consistent with driver/inverter module requirements.

Battery characteristics:

- Fully charged voltage: TBD.
- * Discharged voltage (at TBD % DoD).
- Cell Capacity: TBD.
- * No. of series cells: TBD.
- * No. of parallel strings: TBD.
- Duty cycle: TBD.

* To be determined in Task 1 and verified, where applicable, by tests in subsequent tasks.

6.0 System Control -

System control shall be accomplished by one microprocessor to simulate source and load distributed control.

The basic processor controller type is a single "off-the-shelf" microcomputer board using a TM990-101 N-MOS processor from Texas Instruments.

Programming shall be in FORTH, a high-level compiled language especially well suited to this type of hardware control function.

All module interfaces shall have provisions for manual inputs so that functional system tests may be performed without active computer control.

System interfaces shall be capable of expansion to accept standard serial data bus inputs and specifications, including MIL-STD-1553, and IEEE 448 including fibre optic data transmission.

6.1 Microcomputer Software:

To implement two-level fault protection, the microcomputer software shall monitor analog data, accept data bus commands, and run a slack time foreground task that self-checks the microprocessor.

Specifically, the microprocessor shall be programmed to execute the tasks necessary for programmable fault tolerant control. These shall include:

- o 1,000 Hz task (switch control).
- o 25 Hz tasks (data bus polling/command response)
- o ≅ 1 Hz task voltage regulation and CPU status checking.

6.1.1 1,000 Hz Task - There shall be a real-time task completed every millisecond that monitors the bus current and voltage for excessive out-of-tolerance conditions. The programmability of this task shall provide software control over the algorithm used. For the deliverable breadboard, the algorithm shall generate a turnoff command if the switch current of a particular switch exceeds 100% of its rated current for 40 out of 50 milliseconds (40 out of 50 times the task is run). This high rate permits the software data filtering. The software switch detection and isolation approach controls the hardware using the same digital-to-analog converter outputs as is used by the hardware switch fault detector and isolator. To do this, a negative current limit shall be output. This will cause the hardware to ignore the line voltage and immediately shut off the switch.

6.1.2 25 Hz Task - The 25 Hz task monitors the instrumentation signals required by the finalized measurement list and outputs data on the data bus when polled by the system master controller.

6.1.3 Resident Foreground Task (≅ 1 Hz) - The resident foreground task is a slack time task that executes when the two higher priority tasks are idle. It accomplishes three functions:

- • Voltage level setting.
- • Bidirectional converter mode control.
- • Self test of the microcomputer.

The voltage level set commands the inverters to output a desired line voltage specified by a dac output. The bidirectional voltage control function specifies the required charging current that should be used to charge batteries, and the desired output voltage during discharge. It also specifies the mode of the converter. The self test function executes a memory sum and instruction test program that continuously validates microcomputer operation. Failure of the test sets flags and status bits, which are reported on the data bus to the system master controller.

6.2 Software Generation:

The higher level tasks (25 Hz, resident foreground) shall be programmed in E.L. FORTH code. E.L. FORTH is the Engineering Logic version of Forth Interest Group (FIG-Forth) configured for the Texas Instruments TM990 series of microcomputers. It is designed to function both as a powerful software development system and a comprehensive run-time support package. It is packaged in six TMS2716 EPROMs and is optimized for use in PROM-based, time-critical, interrupt-driven, monitor, and control applications.,

6.3 Monitor:

The monitor is a highly modified TIBUG type monitor. (TIBUG is a registered trademark of Texas Instruments,Inc.)

On power-up, the monitor checks HEX 3000 for a flag word. It will test the flag-word vectoring to a special entry to FORTH and cause the automatic implementation of an application program. The power-up sequence starts the two interrupt-driven tasks and then branches to a noninterrupt loop. FORTH is not accessible in this loop.

Each program is developed with E.L. FORTH in PROM and the application in RAM. When the program is completed, an additional routine is

written to establish the power-up linkages and sequences. The RAM image is burned into EPROM for installation in the finished system. Then the tasks are simply executed when power turn-on occurs.

6.4 Microcomputer Hardware:

The microcomputer consists of a TMS990-101 microprocessor, memory extension board, analog I/O boards, 9600 baud industrial data bus, chassis, power supply, and interconnecting cables. The intent is to demonstrate functional fault tolerance of the power system. Operationally, redundant RAD hard processing will be required, and data bus architecture will be changed. Compatible hardened equipment is available in the same T.I. family.

C. Mechanical Configuration

The system's mechanical configuration shall be composed of a driver assembly, bus system, and a receiver assembly. All chassis and modules shall be mounted in standard 19-inch racks and shall provide their own forced-air or convective cooling.

Transformers and other system interface hardware shall be configured to allow system rearrangement and operation as a single-phase system with the drivers operating in series or in parallel to supply 25.0 kW.

V. Specific Tasks

Tasks I - Requirements

The requirements in Section IV are preliminary in nature with several requirements and parameters to be determined in this task and to be verified by tests and/or experimentation in subsequent tasks.

1. The contractor shall perform those investigations, literature searches, discussions, reviews of test data from the present breadboarded power system, and/or further tests and experimentation with this present

breadboard power system, if necessary, to acquire the necessary data and information to update and finalize the requirements for the 25 kW system. The contractor shall also consider the inputs from LeRC personnel relative to the needs for proper and efficient operation in the LeRC testbed.

2. The contractor shall update and finalize the requirements for the 25 kW power system and submit three (3) copies of the finalized requirements to the NASA project manager for his review and approval.

Task II - Design

1. The contractor shall prepare preliminary circuit designs of the modules and switch matrices, the transmission line power bus, the microprocessor system controller and the required software for the two level fault protection and circuit monitoring to meet the finalized circuit requirements determined in Task I. The preliminary designs shall be based on analyses and tests of the existing low power system and, where necessary for critical areas, by special tests on discrete function breadboarded circuits.

2. Based on the above, the contractor shall finalize the designs including the means to interface the control system with the LeRC system and prepare engineering drawings and component parts lists of the designs and a description of the software program and its operation in the system. The drawings shall be prepared in accordance with Classification Level 1 of Military Specification MIL-D-1000B, dated October 28, 1977.

3. The contractor shall design the mechanical chassis and module assemblies and overall rack enclosures for the deliverable system hardware and prepare the following drawings for the finalized mechanical design:

(a) Outline, layout, and assembly drawings of each module, chassis, and rack enclosure.

(b) Interconnection wiring drawings of the modules, chassis, and enclosures.

(c) Identification of test points and their physical locations

The drawings shjall be prepared in accordance with Classification Level 1 of MIL-D-1000B as in paragraph 2 above.

4. The contractor shall submit three (3) copies of the drawings and descriptions specified in paragraphs 2 and 3 above to the NASA project manager for his review and approval. The contractor must receive this design approval before he can proceed with hardware fabrication.

Task III - Design Review

At the completion of Task II, and, as scheduled, in coordination with the NASA project manager, the contractor shall present a review of Tasks I and II at the Lewis Research Center for NASA personnel. The review shall be mainly a presentation of the design and discussions of the factors influencing the major decisions.

The contractor shall prepare a design review package for use by the participants at the design review meeting. This package shall contain the following as a minimum:

(a) A copy of the slides or vugraphs to be presented with a brief description of each.

(b) Schematic circuit drawings of the modules and the system and a description of their operation and the operation of the software program.

(c) A summary of the expected system performance characteristics, advantages, and limitations.

The contractor shall submit twenty (20) copies of the design review package to the NASA project manager one week prior to the scheduled review meeting. In addition, the contractor shall submit an agenda for the meeting to the NASA project manager two weeks prior to the scheduled meeting.

Task IV - Fabrication

1. The contractor shall procure the necessary materials and components to fabricate the driver and receiver assembly and the bus system. If early procurement of long-lead-time components is required to maintain schedule, approval to procure these components shall be requested from the NASA project manager prior to ordering.

2. The contractor shall fabricate the individual modules, chassis, and enclosures for the driver and receiver assemblies and the bus and control system in accordance with the approved designs.

Task V - Testing

1. The contractor shall prepare a test plan for complete power system performance testing and characterization. The tests shall verify proper system operation, fault tolerance and fault clearing performance, and that the system's performance meets the requirements determined in Task I. The tests shall include the following as a minimum:

a. System and individual module efficiency measurements.

b. Voltage regulation measurements.

c. Fault-protection tests.

d. Load variation tests including loads less than 10% of full load.

e. Frequency response tests.

f. Output voltage ripple measurements.

g. Startup tests.

h. Shutdown tests.

i. System voltage and frequency responses to step changes.

j. System operation with power factor loads from 0.5 power factor to unity power factor,

k. Motor startup and variable speed operation from a 60 Hz source with the Type 2 driver module.

l. Waveforms of critical voltage and current stresses.

m. Measurements to assess system electromagnetic radiation and susceptibility.

The test plan shall desdribe the testing techniques and identify the instruments to be used and their accuracies. Three copies (3) of the test plan shall be submitted to the NASA project manager for his review and approval prior to the start of the tests.

2. The contractor shall test the power system in accordance with the approved test plan.

3. In coordination with the NASA project manager, the contractor shall schedule and perform a demonstration test during the period the test setup is intact. The purpose of this test shall be to demonstrate the operation and performance of the a.c. power system testbed to the NASA project manager and other NASA personnel to provide a basis for acceptance.

4. The test data shall be analyzed to evaluate and characterize the power system performance. The test results, analyses, and evaluations shall be documented in a test report. The contractor shall submit twenty copies (20) of this report to the NASA project manager for review and distribution to NASA personnel.

In conjunction with the test report, the contractor shall also prepare an Operating Procedures Manual. This manual is to be used by LeRC personnel for installation, checkout, and operation of the testbed system. A draft copy of the manual shall be submitted to the NASA project manager for review; three copies of the finalized manual shall be delivered with the hardware.

Task VI - Installation and Checkout at LeRC

Following acceptance testing and delivery of the power system testbed hardware, software, and operating procedures, the contractor shall assist LeRC personnel with the installation and initial operational checkout of the testbed system at the Lewis Research Center.

Task VII - Final Program Review

After completion of the program and prior to publication of the final report, the contractor shall present a summary review of the complete program at the Lewis Research Center for NASA personnel.

The contractor shall prepare twenty (20) copies of a "handout" for distribution to the participants at the meeting. An agenda for the meeting shall be submitted to the NASA project manager two weeks (2) in advance of the scheduled review meeting.

Task VIII - Reporting Requirements

1. Technical, financial and schedular reporting shall be in accordance with the Reports of Work attachment which is hereby made a part of this contract.

2. The monthly report submission date shall be no more than ten (10) operating days after the closing date of the contractor's accounting month.

3. A maximum of twenty (20) copies of the Monthly Technical Progress Narrative will be required.

4. A maximum of six (6) copies of the NASA Form 533M, Monthly Contractor Financial Management Report and NASA Form 533P, Monthly Contractor Financial Mangement Performance Analysis Report will be required.

5. A maximum of twenty (20) copies of the Task III Design Review Package will be required.

6. A maximum of twenty (20) copies of the Task V Test Report will be required.

7. A maximum of twenty (20) copies of the Task VII Final Program Review "handout" will be required.

8. A maximum of one hundred fifty (150) copies of the Final Report will be required.

9. The International System of Units (SI Units) shall be used as primary units in all written reports including handouts for review and coordination meetings. Corresponding conventional units should be included in parentheses immediately following the primary units.

10. The reporting categories to be reported on the NASA Forms 533M and 533P are as follows:

Task I - Direct Costs/Manhours Schedule

Task II - Direct Costs/Manhours Schedule

Task III - Direct Costs/Manhours/Schedule

Task IV - Direct Costs/Manhours/Schedule

Task V - Direct Costs/Manhours/Schedule

Task VI - Direct Costs/Manhours/Schedule

Task VII - Direct Costs/Manhours/Schedule

Task VIII - Direct Costs/Manhours/Schedule

Total Contract Direct Costs/Manhours

Total Contrct Material Costs

Total Contract Overhead

Total Cost

Contractor Share

Government Share

11. The contractor shall report all columns of the NASA Form 533M. The contractor shall report cost and manhour estimates for the next two months in columns 8a and 8b. The contractor shall report only block 11 (a and b) of NASA Form 533P.

Contract values, as originally assigned by the contractor to the NASA Form 533M reporting categories, shall not be changed during the performance of this contract except by contract modification or under other conditions of the Reports of Work attachment paragraph A.2 (revisions to the Work Plan).

VI. Deliverable Items

The following is a listing of deliverable items from the contract:

A. Documentation

Work Plan

Finalized Requirements (3 copies) Task I

Engineering Drawings, Electrical Designs (3 copies) Task II

Engineering Drawings, Mechanical Designs (outlines, layout, assembly) (3 copies) Task II

Engineering Drawings, Wiring Interconnection (3 copies) Task II

Design Review Package (20 copies) Task III

Test Plan (3 copies) Task V

Test Report (20 copies) Task V

Final Program Review "handout" (20 copies) Task VII

Monthly Report - Each Month

Operating Procedures Manual (3 copies) Task V

Final Report (150 copies)

B. Hardware

Item	Quantity	Description
1	1	A wired driver assembly enclosure to accommodate 19-inch rack mounted modules.
2	1	A wired receiver assembly enclosure to accommodate 19-inch rack mounted modules.
3	1	Bus system consisting of two redundant 50-meter, 4-wire, 25 kW transmission lines.
4	1	25 kW, d.c. to 20 kHz, three-phase, Type 1, inverter driver module. (Contains three (3) single-phase inverter/transformer/driver submodules.)
5	1	25 kW, 60 Hz to 20 kHz, three-phase, Type 2, inverter driver module. (Contains a.c./d.c. converter and three (3) single-phase inverter/transformer/driver submodules, Type 2.)
6	1	25 kW, load control and fault isolation switch matrix.

Item	Quantity	Description
7	1	25 kW, driver/bus control switch matrix.
8	1	25 kW, bi-directional converter module with d.c. output voltage on user side.
9	1	5 kW, variable voltage d.c. module.
10	3	25 kW, variable voltage, variable frequency, three-phase a.c. output modules. (Each consists of three (3) single-phase submodules, for a total of nine submodules.) One three-phase a.c. output module to be used with item 5 for control of a three-phase motor. 25 kW.
11	1	System controller. (Consists of a microprocessor controller with data and control outputs.)
12	1	Complete system software.

Appendix B

Hardware/Software Requirements Digest

These tables list summarize the detailed contract requirements and show the changes to the original deliverables, as the program evolved as a result of new data, further definition of the Space Station system, and the test results on this program.

Digest of Requirements and Changes

WS Paragraph	Requirement	Spec Changes	Final Resolution
IV.B	**System Component Module Definition**		
IV.B.1.0	**Three-phase driver/inverter Modules**	...or single phase	OK
	General		
	• Full bridge, series resonant inverter, operated in the voltage source mode	NC	OK
	• Synchronized from a redundant, external clock	single, external clock	OK
	• Interconnected at their output transformer secondaries to drive the three phase bus. .	or paralleled for single phase	OK
IV.B.1.1	**Module Type 1**	Universal Module,Type 1 operation .	OK
	Inputs		
	• 150 to 300 VDC	NC	150 to 210 VDC
	• power supply or (solar) array	NC	OK
	Outputs		
	• 440 VAC,RMS, ±5.0%, (L-N) . . . . . (at the transformer secondary)	NC	OK
	• 25 KW, total, max.	NC	OK
	(three phase, steady state)	(or single-phase)	OK
	•20 KHz ± TBD . . . . . (TBD from task 1)	NC; TBD = 0.1%	OK
	• Load variation = 10% to full load	NC	OK
	Synchronization Signal		
	• compatible with CMOS logic	NC	OK
	• 20 KHz ± TBD . . . . . (TBD from task 1)	NC; TBD = 0.1%	OK

Digest of Requirements and Changes

WS Paragraph	Requirement	Spec Changes	Final Resolution
IV.B.1.2	**Module Type 2**	Type 2 operation	Delete Type 2 Requirement
	Type 2 modules and the AC modules of 5.2 will be capable of operating as a separate motor control unit.	Universal modules in Type 2 operation... . . . . NC	
	Inputs		
	• 440 VAC, (L-L), three phase	208 VAC, ...	
	• 60 Hz	NC	
	• Standard commercial utility power	NC	
	Outputs		
	• 440 VAC,RMS, ±5.0%, (L-N) . . . . . (at the transformer secondary)	NC	
	• 25 KW, total, max. . . . . (three phase, steady state)	NC	
	• 20 KHz ± TBD . . . . . (TBD from task 1)	NC; TBD = 0.1%	
	• Load variation = 10% to full load	NC	
	Synchronization Signal		
	• compatible with CMOS logic	NC	
	• 20 KHz ± TBD . . . . . (TBD from task 1)	NC; TBD = 0.1%	
IV.B.2.0	**Bus Control Switch Matrix** Each element is an AC Semiconductor RPC capable of connecting a driver module to/from the power bus.	NC	OK
	• connect to either of two transmission busses	delete	OK

Digest of Requirements and Changes

WS Paragraph	Requirement	Spec Changes	Final Resolution
	Turn-on mode (1)		
	• System computer/controller command	NC	OK
	Turn-off mode (1)		
	• Emergency/automatic	NC	OK
	• Based on current/voltage sensed at the load module	NC	OK
	• Occurs in less than 1 cycle of the power bus frequency	NC	OK
	Turn-off mode (2)		
	• System computer/controller command	NC	OK
	• Occurs in less than 100 msec.	NC	OK
	Electronic interface specifications		
	• Switched voltage = 762 VAC,RMS ±5%	NC	OK
	• Switched current = 25 amp, AC,RMS, max,(real)	NC	OK
	• Frequency = 20.0 KHz	NC	OK
	• Command inputs = compatible with CMOS Logic	NC	OK
	* Max voltage drop = TBD		
	* Reactive current = TBD, max.	NC; TBD = 25 amp	OK
	* Turn-on transient = TBD	Not applicable, turn-on at zero voltage	OK
	* Response Time = TBD	NC; TBD = 50 µseconds	OK
	(*) These parameters to be determined in task 1, based on breadboard tests		

Digest of Requirements and Changes

WS Paragraph	Requirement	Spec Changes	Final Resolution
IV.B.3.0	**Power Busses**		
	Two parallel busses, sharing loads under normal operating conditions, each capable of supplying full load when operated alone. . . .	single Bus	OK
	• three phase, four wire	...or single phase, six wire	OK
	• designed for minimum electromagnetic radiation and susceptibility	NC	twisted, shielded, pair
	Electronic Interface Specifications		
	• Length = 50 meters	100 meters	OK
	• Diameter = TBD	NC	2.0 cm.
	• Voltage (L-N) = 440 VAC,RMS, ± 5.0%	NC	OK
	• Current Normal operation = 25 amp,RMS	NC	OK
	Fault operation = 50 amp, RMS		
	• Allowable losses (at 50 meters)		
	Normal operation = 0.5% of load	NC	0.68%
	Fault operation = 2.0% of load	NC	1.36%
	* Terminations = TBD	NC; TBD = std MIL- connectors . . .	OK
	* Capatance = TBD	NC	0.30 nFarad/meter
	* Inductance = TBD	NC	0.35 µHenry/meter
	(*) These parameters to be determined in task 1 and verified by tests in subsequent tasks.		

Digest of Requirements and Changes

WS Paragraph	Requirement	Spec Changes	Final Resolution
IV.B.4.0	**Load Control Switch Matrix**		
	Each element is an AC Semiconductor RPC capable of connecting a load module to/from either or both of the power busses. . . .	...connecting a load module to/from the single power bus. . . .	OK
	• Modes and requirements same as "Bus Control Switch Matrix"		
IV.B.5.0	**Load Modules**		
IV.B.5.1	**Variable voltage DC module**		
	• Converts the bus outputs to regulated DC for general useage.	NC	OK
	Electronic Interface Specifications		
	• Input volyage = 440 VAC,RMS ±5.0% (L-N) . .	NC	OK
	• Input current = 25 amp,RMS, Max. (steady state)	NC	OK
	* Transient input current = TBD		
	• Input frequency = 20.0 KHz	NC	OK
	• Output voltage = +25 to +150 VDC ±1.0% . . .		
	• Output resolution = 2.0 VDC	NC	OK
	• Output power = 5.0 KW, max	NC	OK
	• Output ripple = 1.0% max. (at full load)	NC	OK
	• Control Inputs = Compatable with CMOS logic levels and interface specifications . . .	NC	OK

Digest of Requirements and Changes

WS Paragraph	Requirement	Spec Changes	Final Resolution
IV.B.5.2	**Variable voltage, variable frequency AC modules**		
	• Converts bus outputs to regulated AC, variable frequency for general AC useage, including motor control.	NC	OK
	Electronic Interface Specifications		
	• Input volyage = 440 VAC,RMS ±5.0% (L-N)	NC	OK
	• Input current = 25 amp,RMS, Max. (steady state)	NC	OK
	* Transient input current = TBD		
	• Input frequency = 20.0 KHz	NC	OK
	• Output voltage = 0 to 115 VAC,RMS ±1.0% (L-N), three phase	NC	OK
	• Wye-connected	NC	OK
	• Output frequency = 0 to 2.5 KHz ±1.0%	NC	13 Hz to 3.3 KHz
	• Output distortion = 5.0% max, total (at full load)	NC	OK
	• Output power = 25.0KW, max	NC	OK
	• Load power factor = 0.5 max	NC	OK
	• Output Ripple = 1.0% max (at full load)	Delete ripple spec	OK
	• Control Inputs = Compatable with CMOS logic levels and interface specifications	NC	OK

Digest of Requirements and Changes

WS Paragraph	Requirement	Spec Changes	Final Resolution
IV.B.5.3	**Bidirectional Converter Module**		
	1. Receiver mode		
	• DC receiver	NC	OK
	• Output regulation control based on external commands from the system computer/controller	NC	OK
	2. Driver mode		
	• System driver/inverter module	NC	OK
	• Operation from battery charged above.	NC	OK
	• Outputs consistant with Driver/Inverter module requirements	NC	OK
	Battery characteristics		
	* Fully charged voltage = TBD	Operated from a DC supply	OK
	* Discharged voltage = TBD	Operated from a DC supply	OK
	* Cell capacity = TBD	not applicable	
	* No. of series cells = TBD	not applicable	
	* No. of parallel strings = TBD	not applicable	
	* Duty cycle = TBD	not applicable	
	(*) to be determined in task 1 and verified, where applicable, by subsequent tests.		

Digest of Requirements and Changes

WS Paragraph	Requirement	Spec Changes	Final Resolution
IV.B.6.0	**System Control**	MacIntosh terminal/ supervisor; two imbedded	
	• One microprocessor	microprocessors	OK
	• single board, TM 990-101 type	8086	OK
	• Programming in forth	Intel PL/M & Basic	OK
	• Module interfaces shall have provisions for manual inputs		
	• Interfaces capable of expansion to accept	NC; with appropriate	
	o MIL-STD-1553, serial data bus	added interface hardware	OK
	o IEEE 448, (incl. fiber optic bus)		
IV.B.6.1	**Microcomputer software**		
	• two level fault protection	No software fault protection	OK
	• monitor analog data	NC	OK
	• accept data bus commands	NC	OK
	• Serial data bus input/output	NC	OK
	• Interface with testbed facility system at LeRC	RS-232 or -422 busses with Commercial Comm. software	OK
	• slack time self check	self check on start-up only	OK
	• programmible fault tolerant control	Non Redundant	OK
IV.B.6.1.1	1000 Hz task (many details)	Intent accomplished with MacIntosh/8086	
IV.B.6.1.2	25 Hz task (many details)	system/software. This example is for	
IV.B.6.1.3	approx. 1 Hz task (many details)	information purposes only.	

Digest of Requirements and Changes

WS Paragraph	Requirement	Spec Changes	Final Resolution
IV.B.6.2	**Software generation**		
	• higher level tasks = FIG-Forth	μ Soft Basic & Intel PL/M.	OK
	• EPROM based	Disk and EPROM based	
IV.B.6.3	**Monitor**		
	• TIBUG type	not applicable for this system/software	
IV.B.6.4	**Microcomputer hardware**		
	• TMS990-101	8086 imbedded processors	OK
	• memory expansion board	not required	
	• analog I/O boards	NC	OK
	• 9600 baud industrial data bus	NC	OK
	• Chassis	NC	OK
	• power supply	NC	OK
	• interconnecting cables	NC	OK
	• demonstrate functional fault tolerance	Delete, simplex system	OK
	• compatable hardened equipment	NC	Compatable with Harris 8086 hardened processor
IV.C.	**Mechanical configuration**		
	• Driver assembly	NC	OK
	• Bus system	NC	OK
	• Receiver assembly	NC	OK
	• standard 19 inch racks	NC	OK
	• Internal forced air or convective cooling	NC	OK

Digest of Requirements and Changes

WS Paragraph	Requirement	Spec Changes	Final Resolution
	Transformers and other interface hardware reconfigurable to allow single phase or three phase operation.	NC	OK
	• series or parallel	Parallel for 440 v operation	OK
	• 25.0 KW	NC	OK
IV.A.3	**System design requirements**		
	• lightweight	NC	OK
	• high efficiency	No specific req't,to be measured during system testing	OK
	• Fail Operational/Fail Safe (for system Faults)	change to Fail Safe only	OK
	• Fail safe (for load faults)	NC	OK
	• minimum EMI radiation & susceptability in accordance with MIL-STD-461	No specific req't, to be measured during evaluation testing	OK
	• modular to facilitate expansion	NC	OK

Appendix C

Electrical Hardware Schematics

The drawings presented in this Appendix are a selected subset of the total documentation provided for this testbed. They are provided to illustrate the basic circuit designs used for the various system modules. The total drawing package was provided in print and electronic form with the hardware, when it was delivered.

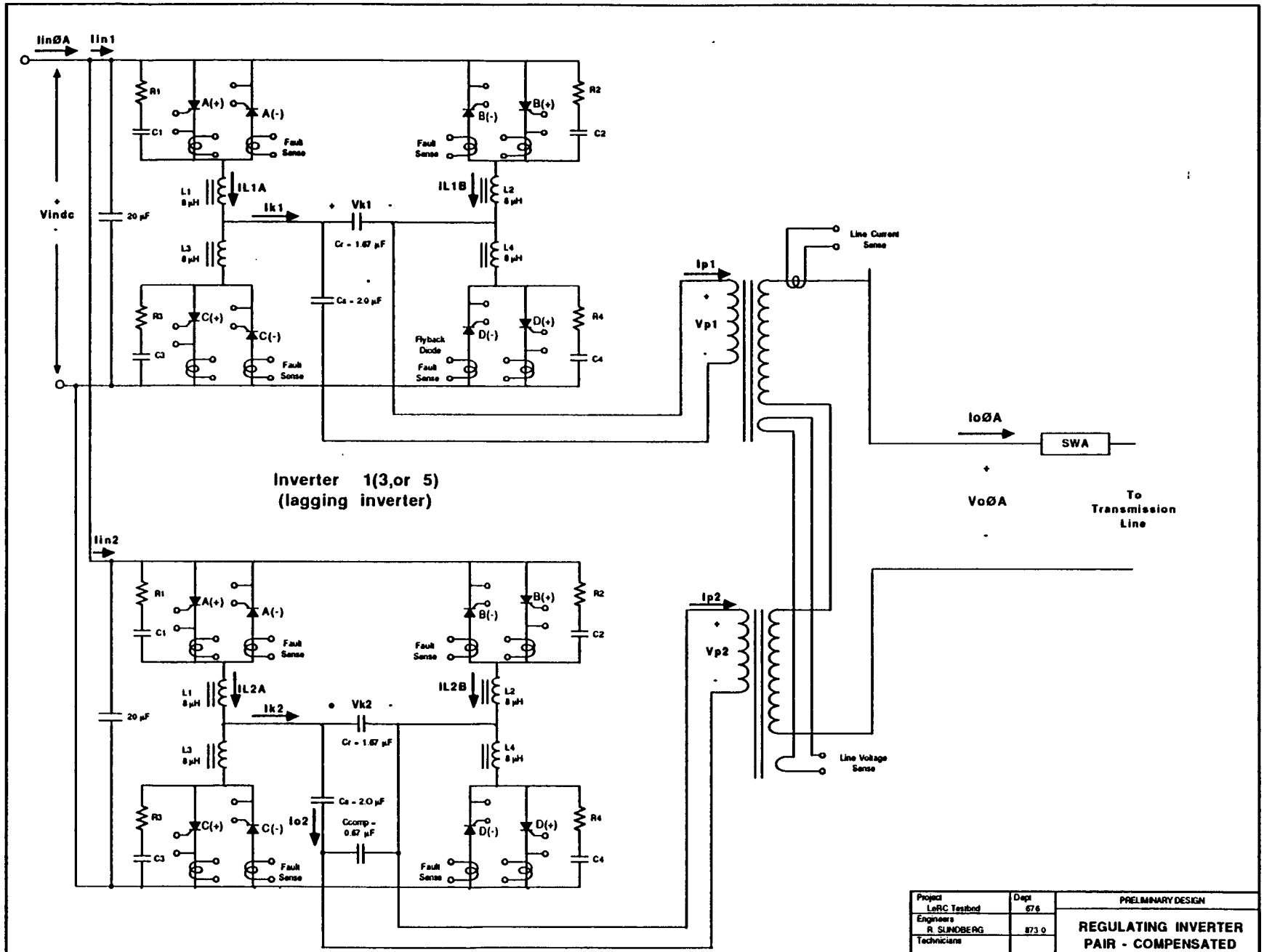
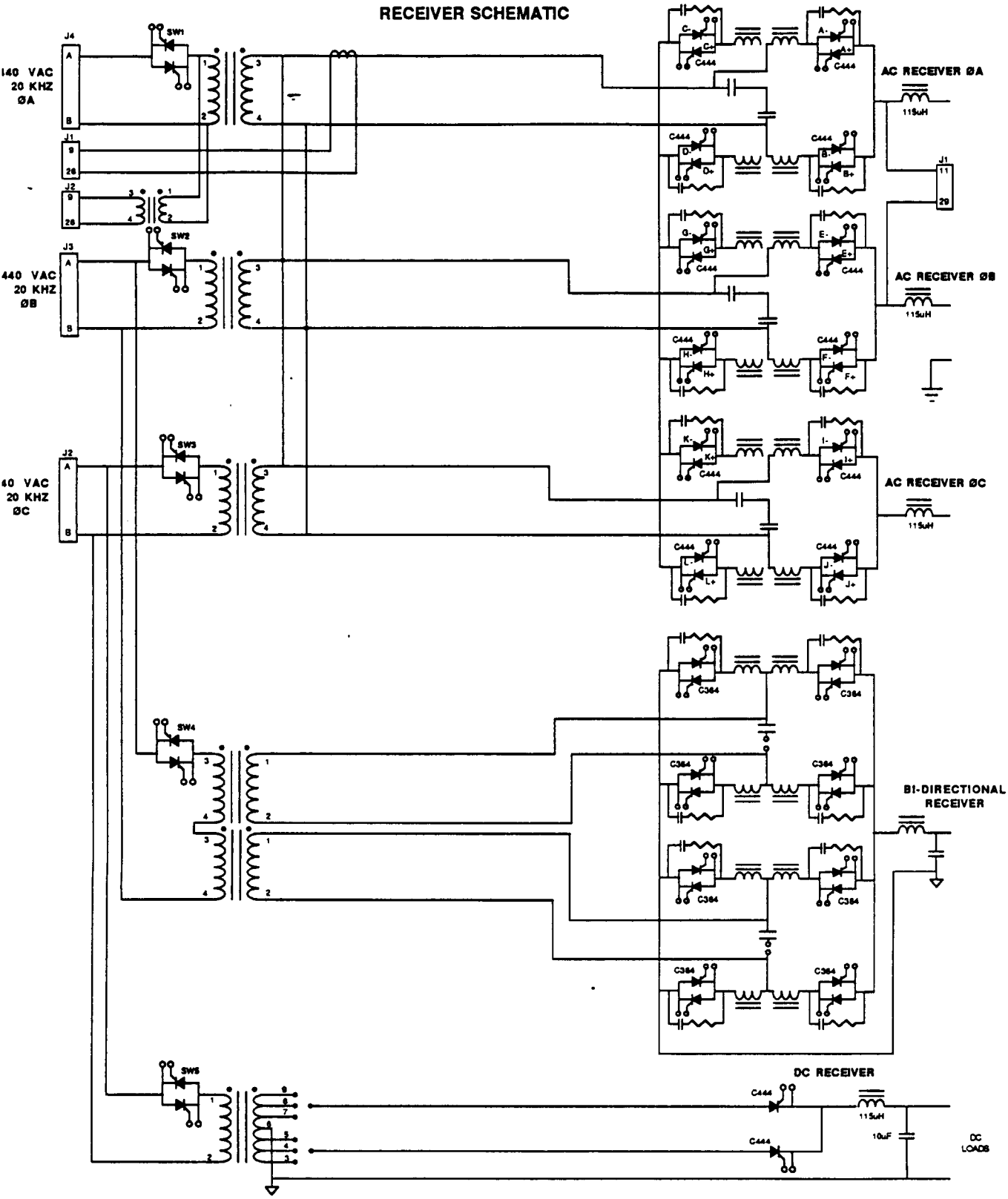
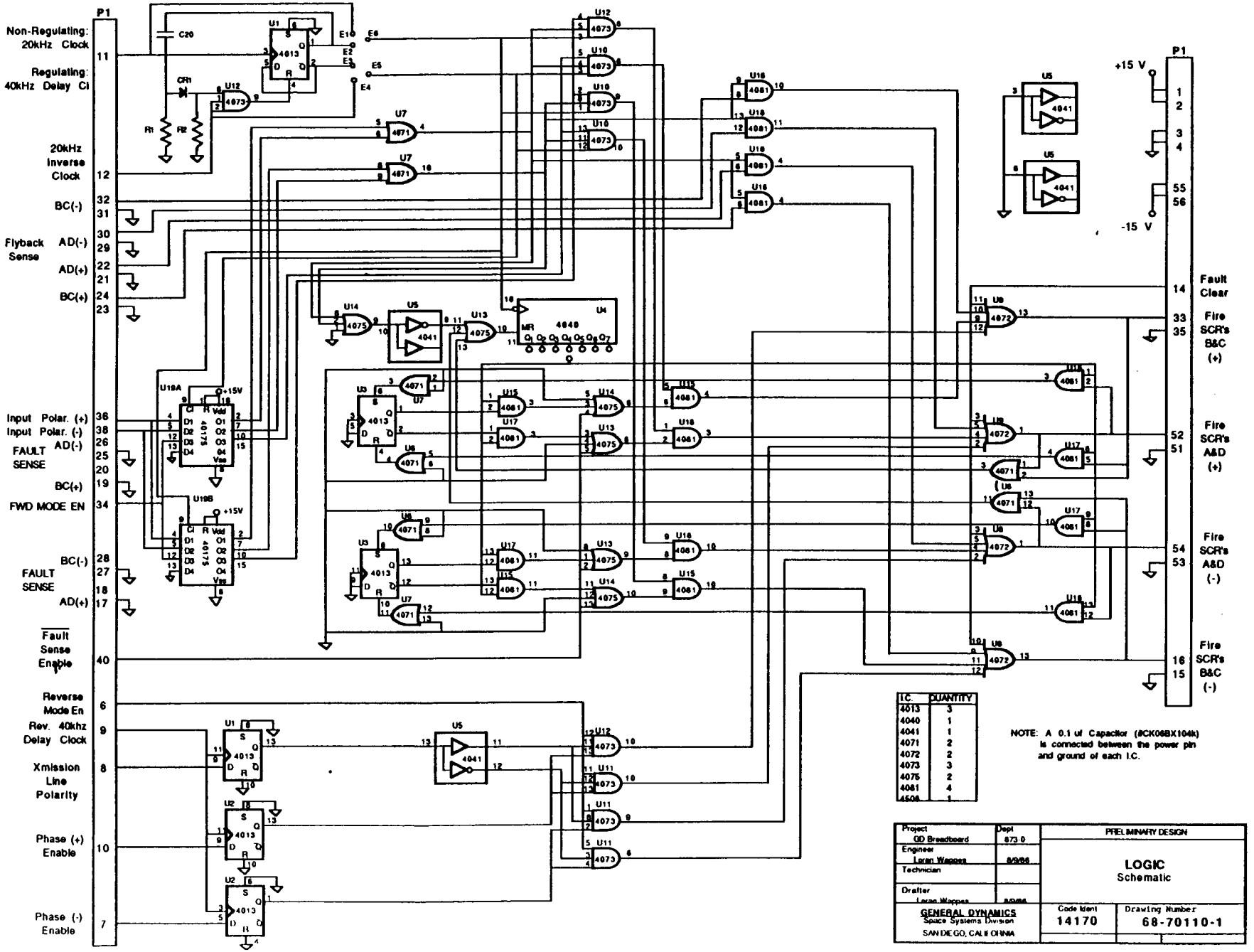


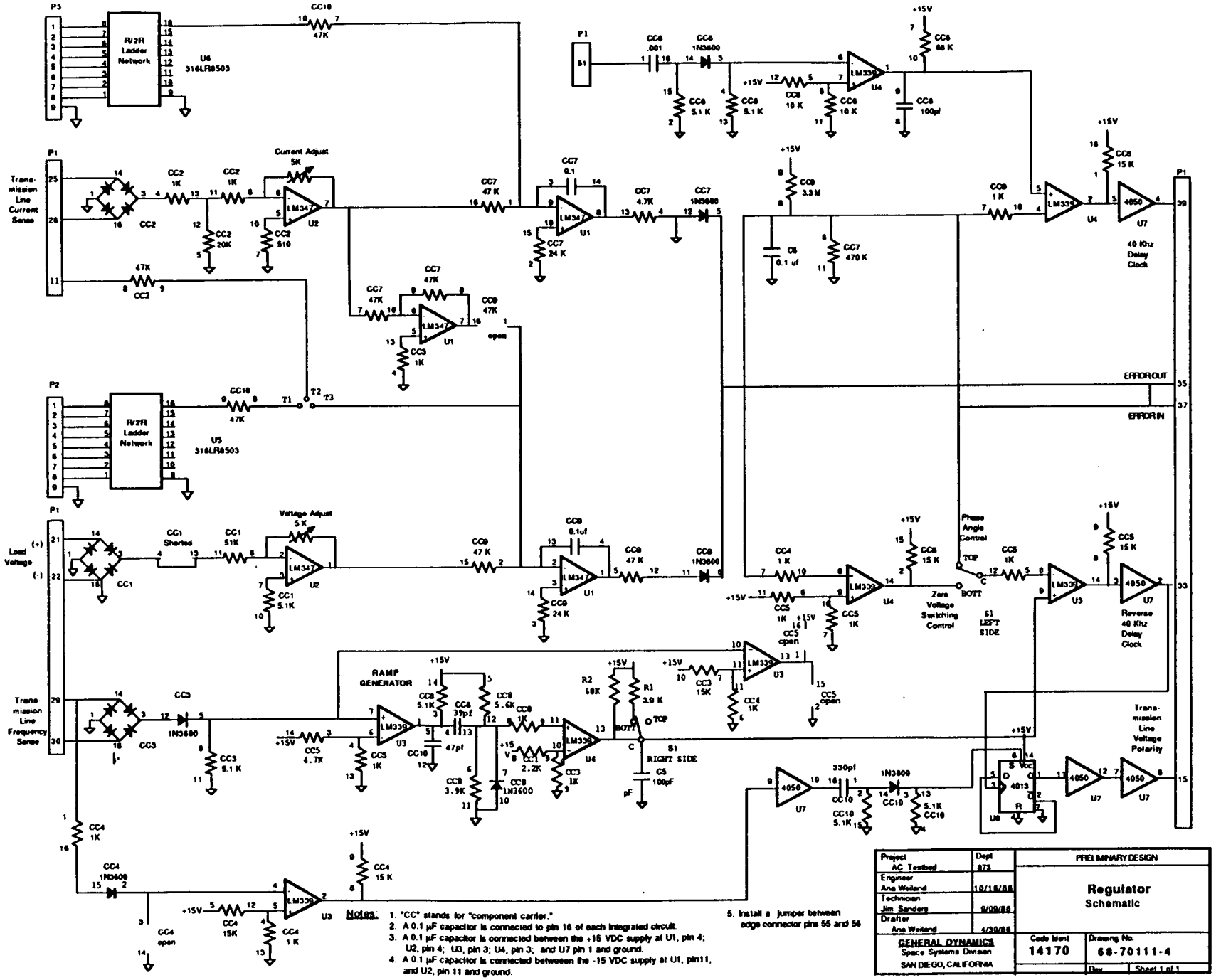
Figure A2 - Compensated Inverter pair

Project: LeRC Testbed	Dept: 676	PRELIMINARY DESIGN
Engineers: R. SUNDBERG	873.0	REGULATING INVERTER PAIR - COMPENSATED
Technicians		Schematic
Drafter: R. SUNDBERG		5/5/87
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA		Code Ident: 14170 — Drawing No. — Rev. — Sheet 1 of 1



Project: AC Testbed	Dept: 873	PRELIMINARY DESIGN
Engineer: Ana Weiland	8/22/86	RECEIVER SCHEMATIC WIRING DIAGRAM
Technician: Jim Sanders	8/22/86	
Drafter: Ana Weiland	4/30/86	
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA	Code Ident: 14170	68-70190-0
		Rev. Sheet 1 of 1


P1
Non-Regulating: 20kHz Clock
11
Regulating: 40kHz Delay Cl
20kHz Inverse Clock
12
BC(-)
32
31
Flyback Sense
AD(-)
30
29
AD(+)
22
21
BC(+)
24
23
Input Polar. (+)
36
Input Polar. (-)
38
FAULT SENSE
AD(-)
26
25
BC(+)
20
19
FWD MODE EN
34
BC(-)
28
27
FAULT SENSE
AD(+)
18
17
Fault Sense Enable
40
Reverse Mode En
6
Rev. 40khz Delay Clock
9
Xmission Line Polarity
8
Phase (+) Enable
10
Phase (-) Enable
7
C20
CR1
R1
R2
E1
E2
E3
E4
E6
E5
+15 V
-15 V
Fault Clear
14
Fire SCR's B&C (+)
33
35
Fire SCR's A&D (+)
52
51
Fire SCR's A&D (-)
54
53
Fire SCR's B&C (-)
16
15
I.C. QUANTITY
4013 3
4040 1
4041 1
4071 2
4072 2
4073 3
4075 2
4081 4
4506 1
NOTE: A 0.1 uf Capacitor (8CK06BX104k) is connected between the power pin and ground of each I.C.
Project GD Breadboard
Dept 673-0
Engineer Loran Wappes 8/3/96
Technician
Drafter Loran Wappes 8/3/96
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA
PRELIMINARY DESIGN
LOGIC Schematic
Code Ident 14170
Drawing Number 68-70110-1



Notes:

1. "CC" stands for "component carrier."
2. A 0.1 μF capacitor is connected to pin 16 of each integrated circuit.
3. A 0.1 μF capacitor is connected between the +15 VDC supply at U1, pin 4; U2, pin 4; U3, pin 3; U4, pin 3; and U7 pin 1 and ground.
4. A 0.1 μF capacitor is connected between the -15 VDC supply at U1, pin11, and U2, pin 11 and ground.
5. Install a jumper between edge connector pins 55 and 56

Project: AC Testbed	Dept: 873	PRELIMINARY DESIGN
Engineer: Ana Weiland	10/18/88	Regulator Schematic
Technician: Jim Sanders	9/09/88	
Drafter: Ana Weiland	4/30/88	
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA	Code Ident: 14170	Drawing No.: 68-70111-4
		Rev. / Sheet 1 of 1

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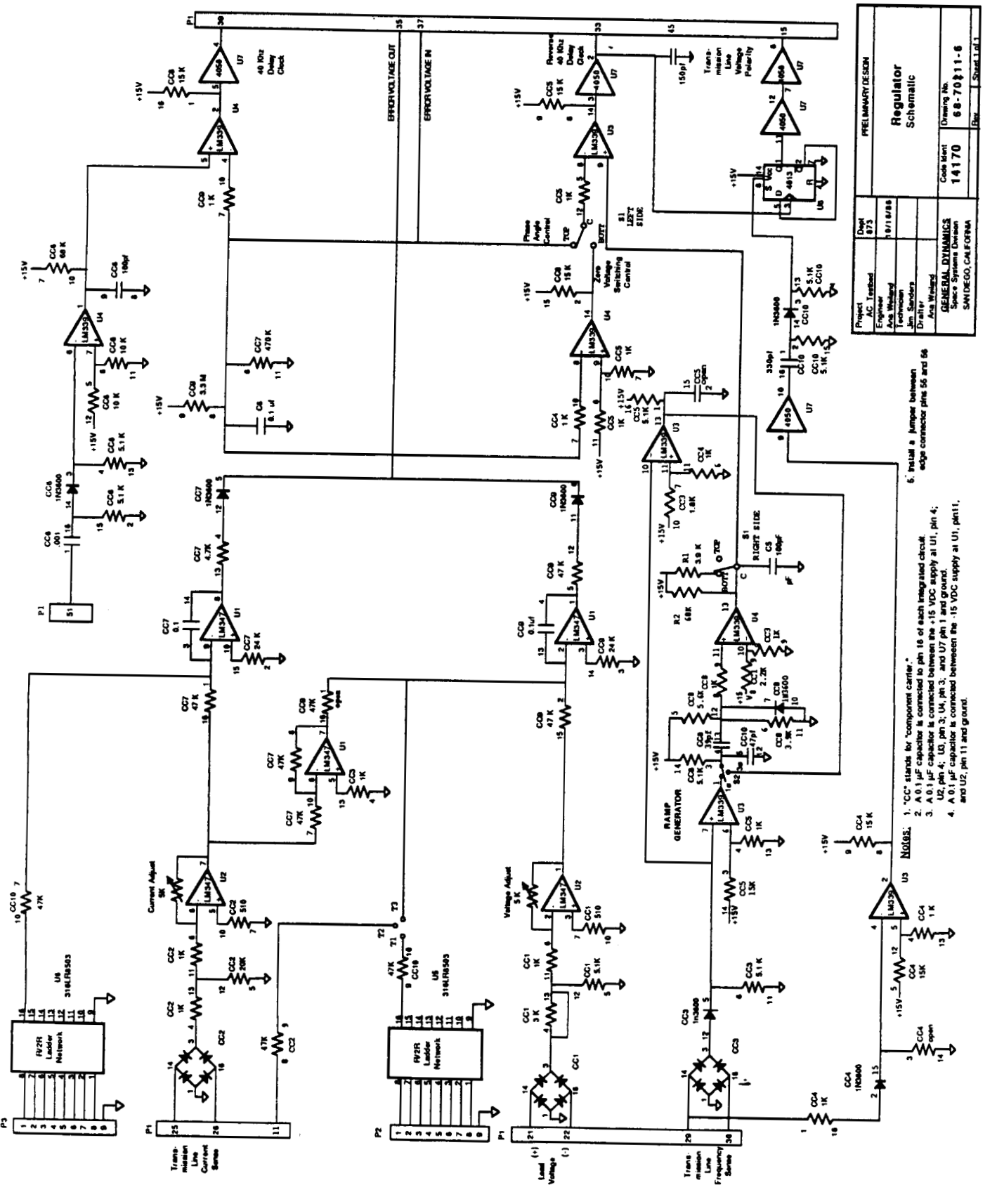

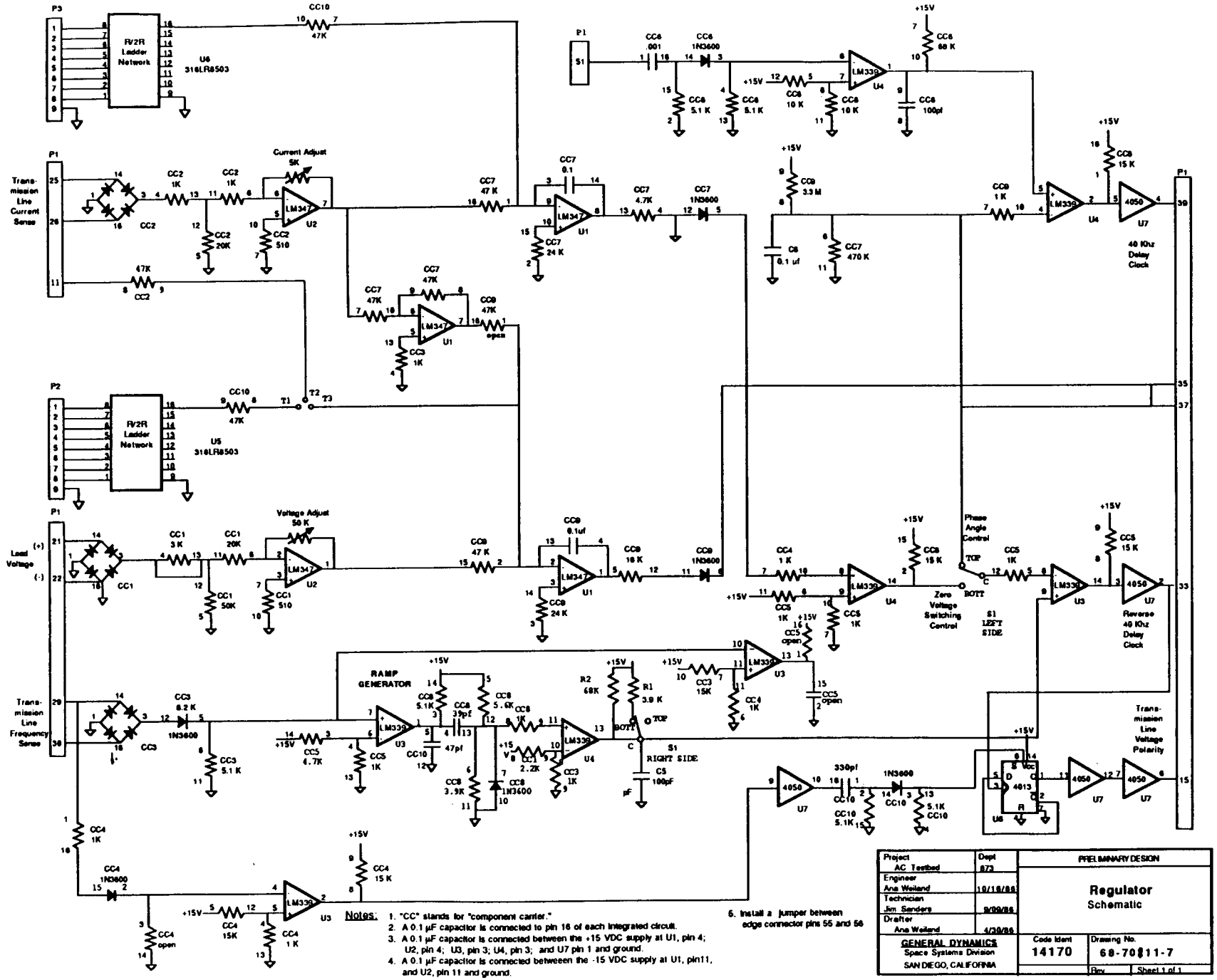

Notes:

1. "CC" stands for "component carrier."
2. A 0.1 μF capacitor is connected to pin 16 of each integrated circuit.
3. A 0.1 μF capacitor is connected between the +15 VDC supply at U1, pin 4; U2, pin 4; U3, pin 3; U4, pin 3; and U7 pin 1 and ground.
4. A 0.1 μF capacitor is connected betweeen the -15 VDC supply at U1, pin11, and U2, pin 11 and ground.
5. Install a jumper between edge connector pins 55 and 56

Project: AC Testbed	Dept: 873	PRELIMINARY DESIGN
Engineer: Ane Weiland	10/18/86	Regulator Schematic
Technician: Jim Sanders	9/09/86	
Drafter: Ane Weiland	4/30/86	
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA	Code Ident: 14170	Drawing No.: 68-70811-7
		Rev. / Sheet 1 of 1

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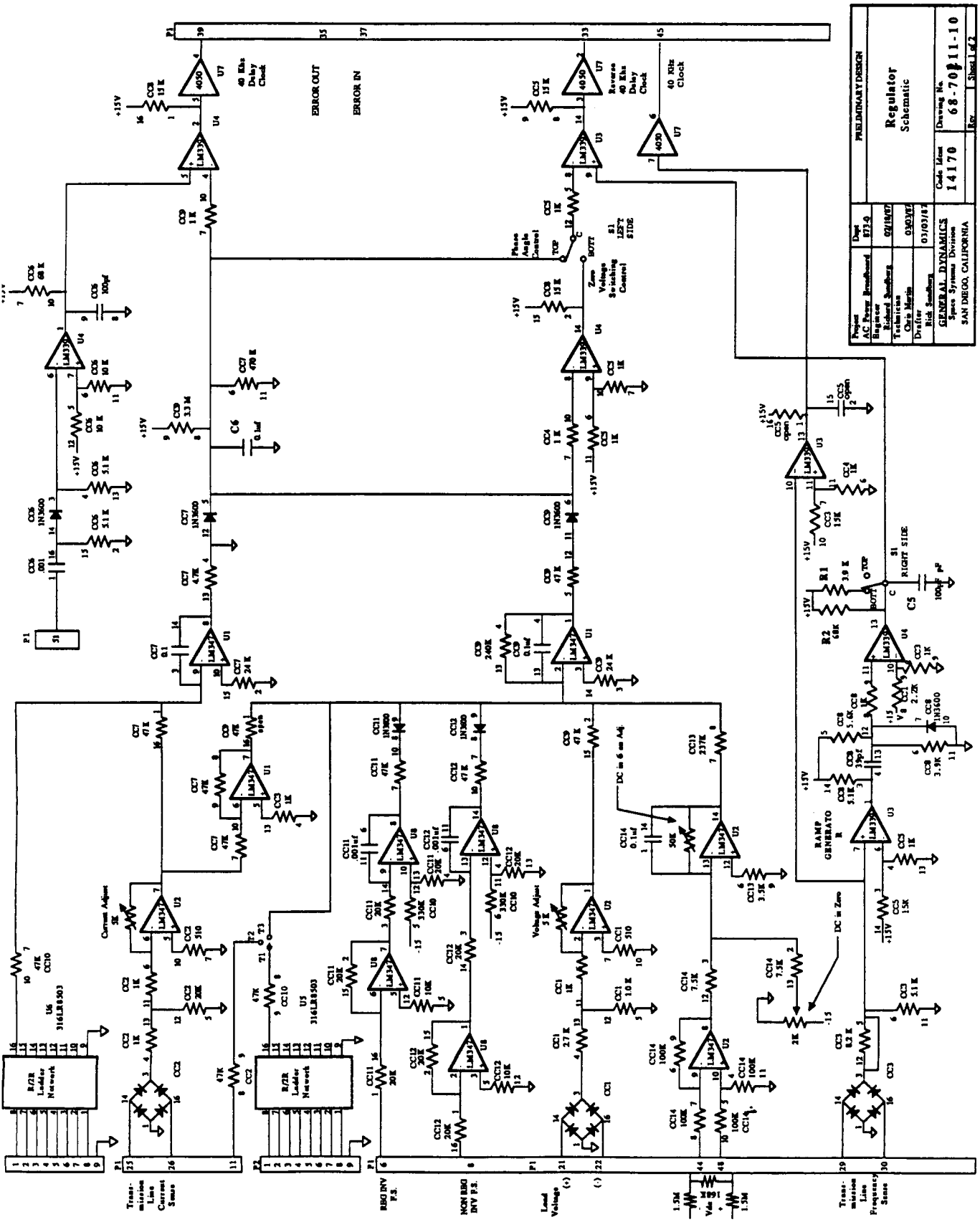
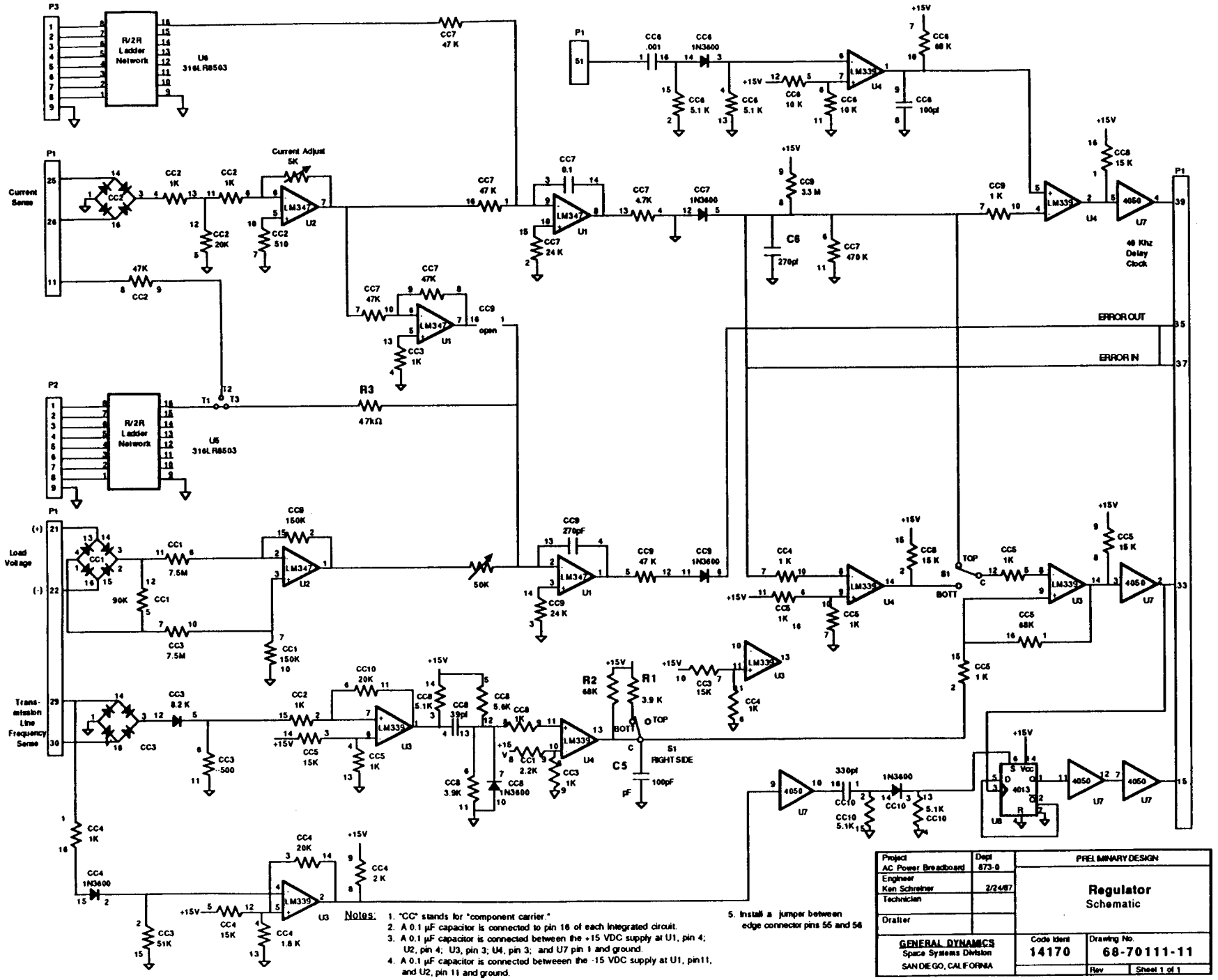
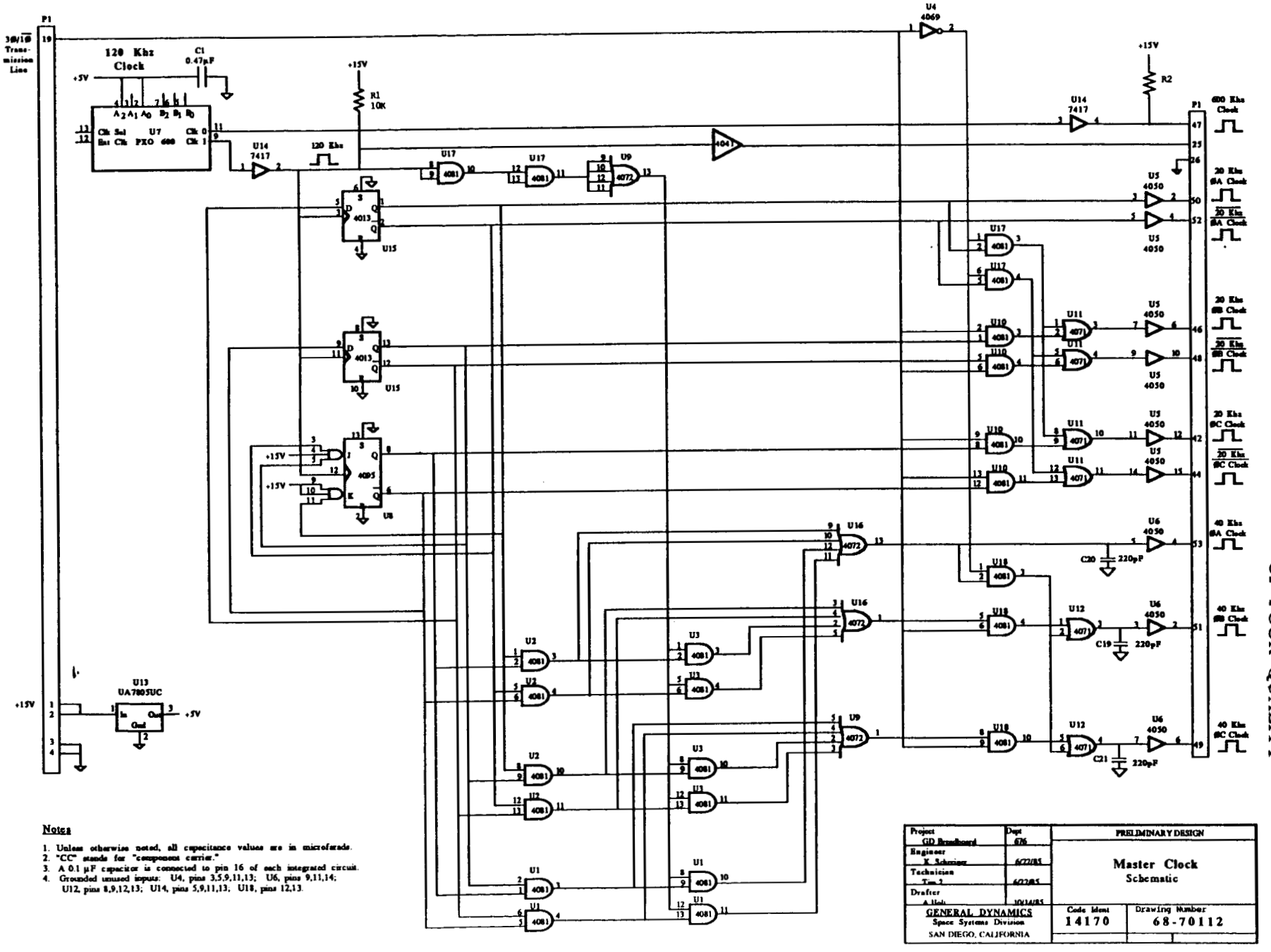




Notes:

1. "CC" stands for "component carrier."
2. A 0.1 µF capacitor is connected to pin 16 of each integrated circuit.
3. A 0.1 µF capacitor is connected between the +15 VDC supply at U1, pin 4; U2, pin 4; U3, pin 3; U4, pin 3; and U7 pin 1 and ground.
4. A 0.1 µF capacitor is connected betweeen the -15 VDC supply at U1, pin11, and U2, pin 11 and ground.
5. Install a jumper between edge connector pins 55 and 56

Project: AC Power Breadboard	Dept: 873-0	PRELIMINARY DESIGN
Engineer: Ken Schreiner	2/24/87	**Regulator** Schematic
Technician:		
Drafter:		
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA	Code Ident: 14170	Drawing No.: 68-70111-11
		Rev / Sheet 1 of 1



Notes

1. Unless otherwise noted, all capacitance values are in microfarads.
2. "CC" stands for "component carrier."
3. A 0.1 μF capacitor is connected to pin 16 of each integrated circuit.
4. Grounded unused inputs: U4, pins 3,5,9,11,13; U6, pins 9,11,14; U12, pins 8,9,12,13; U14, pins 5,9,11,13; U18, pins 12,13.

Project: GD Breadboard	Dept: 676	PRELIMINARY DESIGN
Engineer: K. Schreiner	6/27/85	Master Clock Schematic
Technician: Tim J.	6/27/85	
Drafter: A. Holt	10/14/85	
GENERAL DYNAMICS Space Systems Division, SAN DIEGO, CALIFORNIA	Code Ident: 14170	Drawing Number: 68-70112

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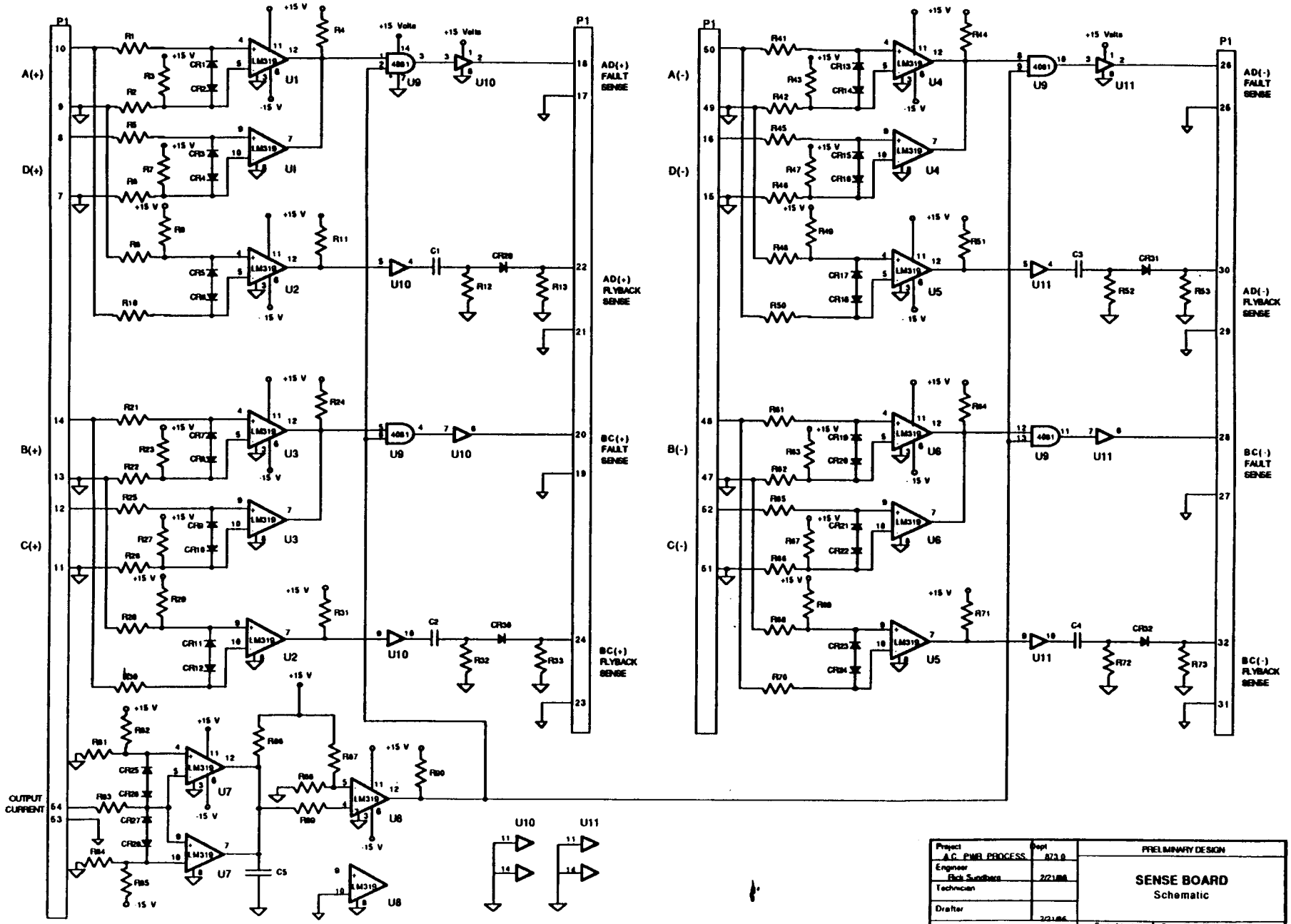
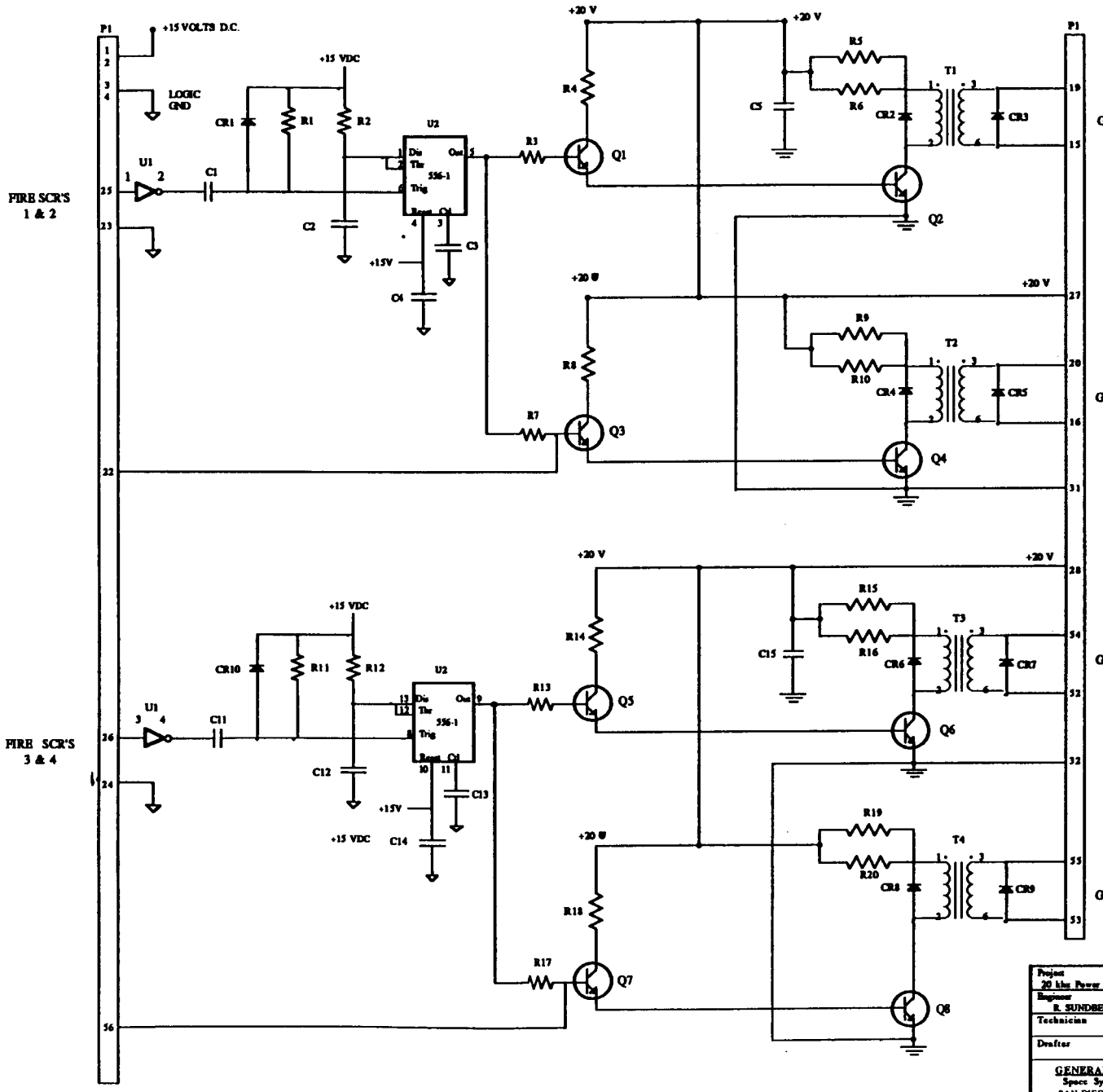


Project: A.C. PWR PROCESS	Dept: 873.0	PRELIMINARY DESIGN
Engineer: Rick Sundberg	2/21/86	SENSE BOARD Schematic
Technician		
Drafter	2/21/86	
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA	Code Ident: 14170	Drawing No.: 68-70113



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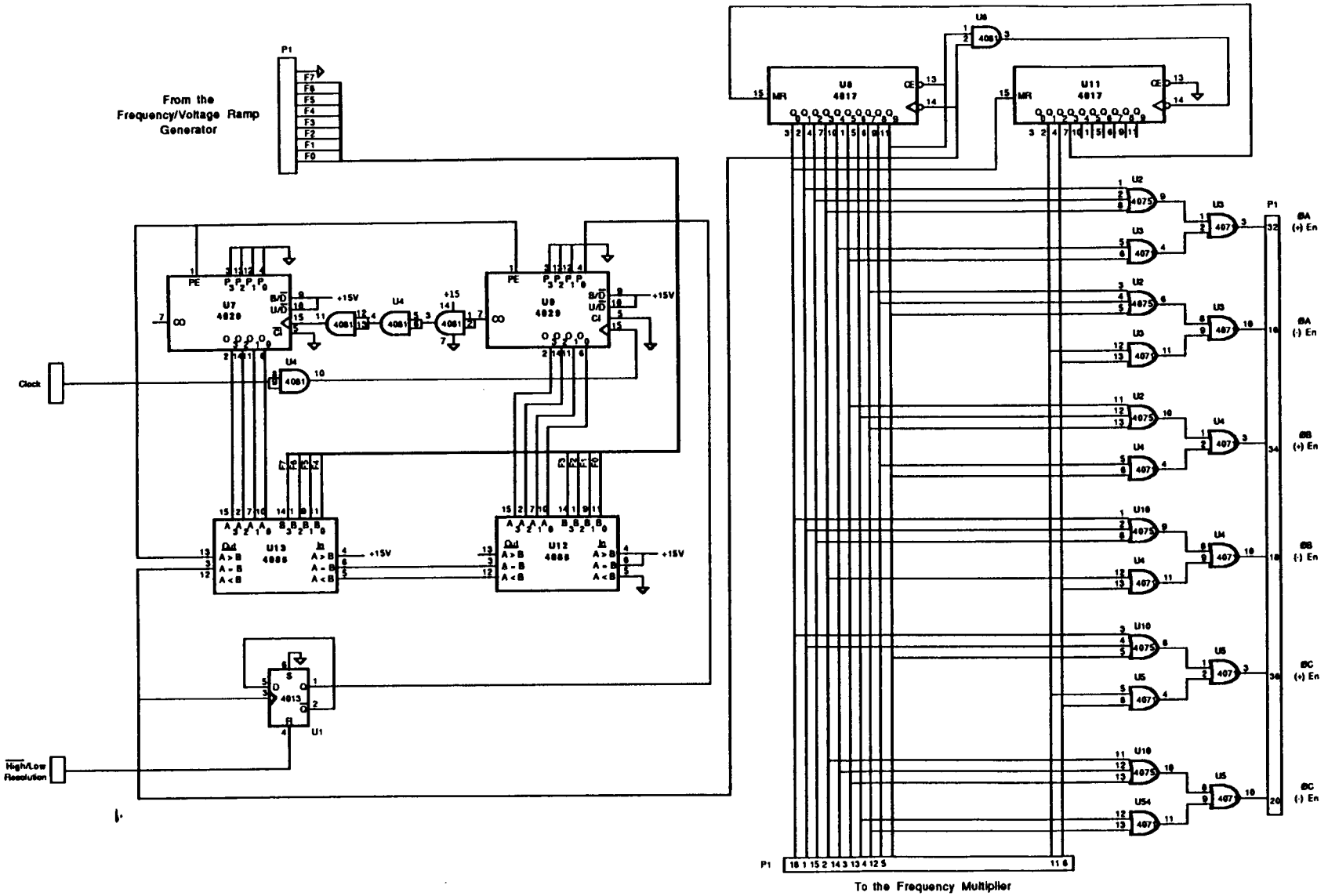
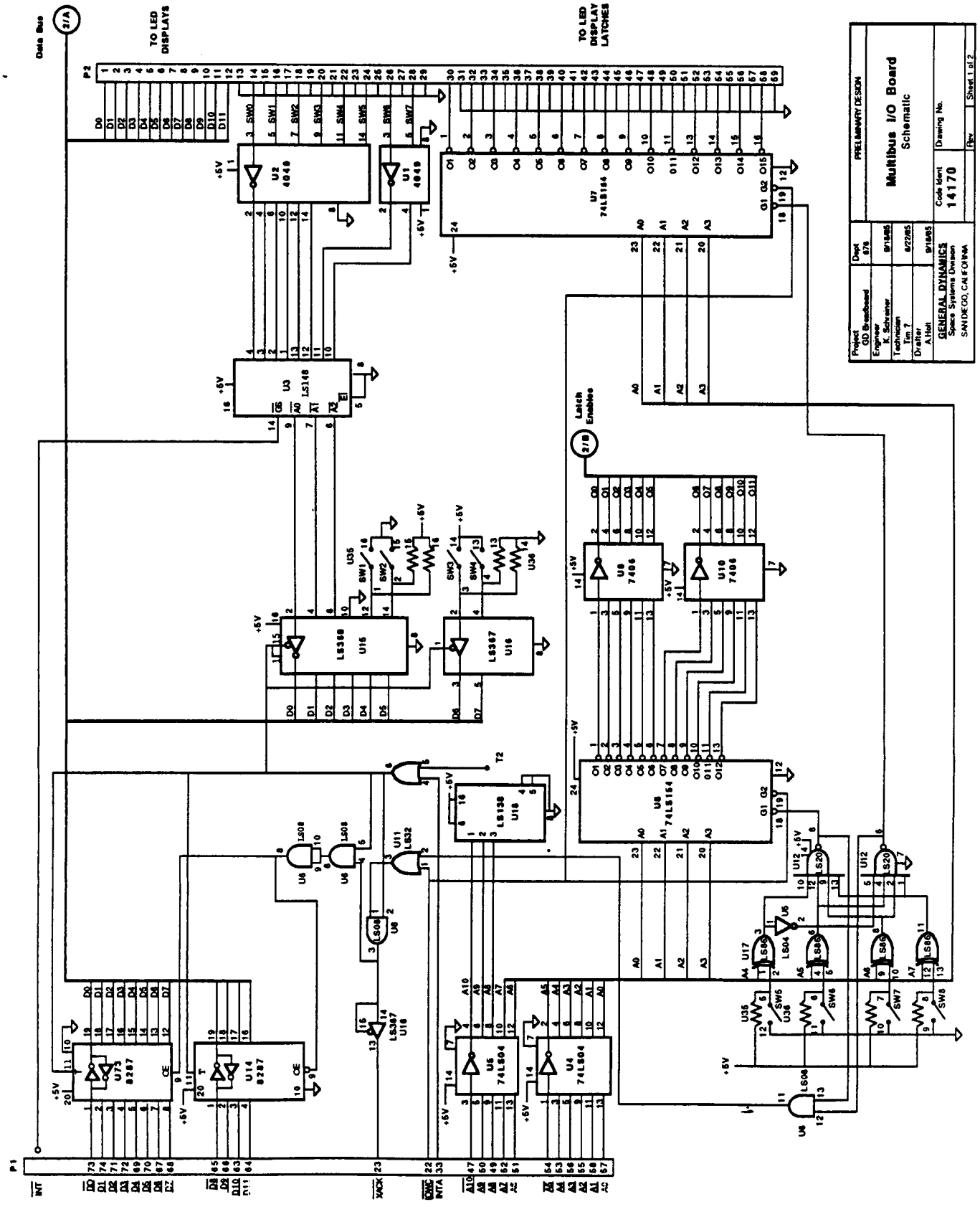
Notes:

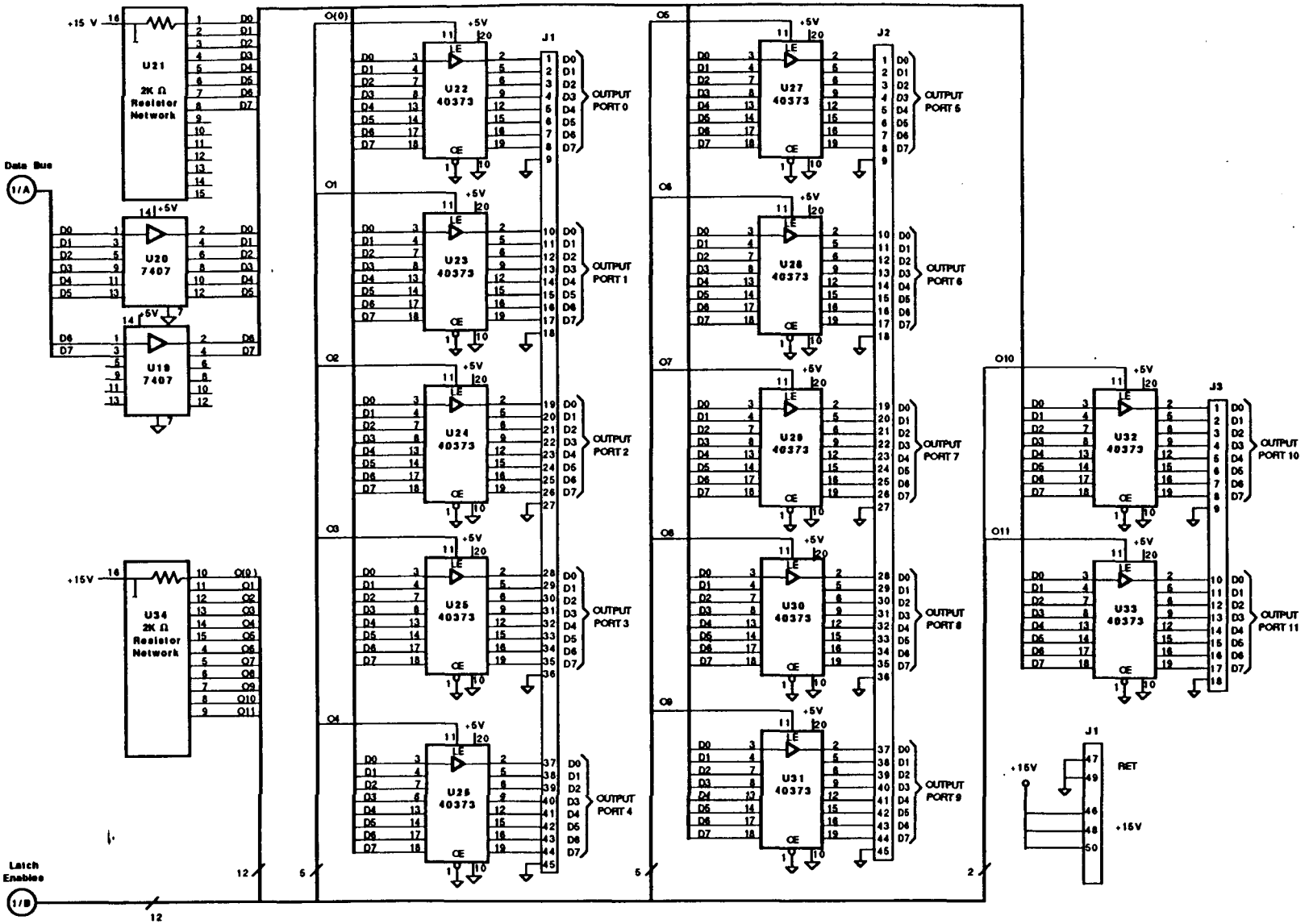
1. 20 Volt Power Supply Input Leads rated for 3 amps D.C.
2. All IC's connected to +15 volts and logic ground at pins 14 and 7 respectively.
3. A 1uf Power Supply Bypass Capacitor is placed between pins 14 and 7 on each IC.
4. For Questions, Please contact Rich Sundberg at 7-3105.
5. All four 2N3506 transistors are mounted with a Thermalloy 2211B heat-sink.

Project: 20 khz Power System	Dept: 376	PRELIMINARY DESIGN
Engineer: R. SUNDBERG	1/10/86	QUAD SCR Drivers Schematic
Technician		
Drafter		
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA	Code Ident: 14170	Drawing No.: 68-70114-2
	Rev	Sheet 1 of 1

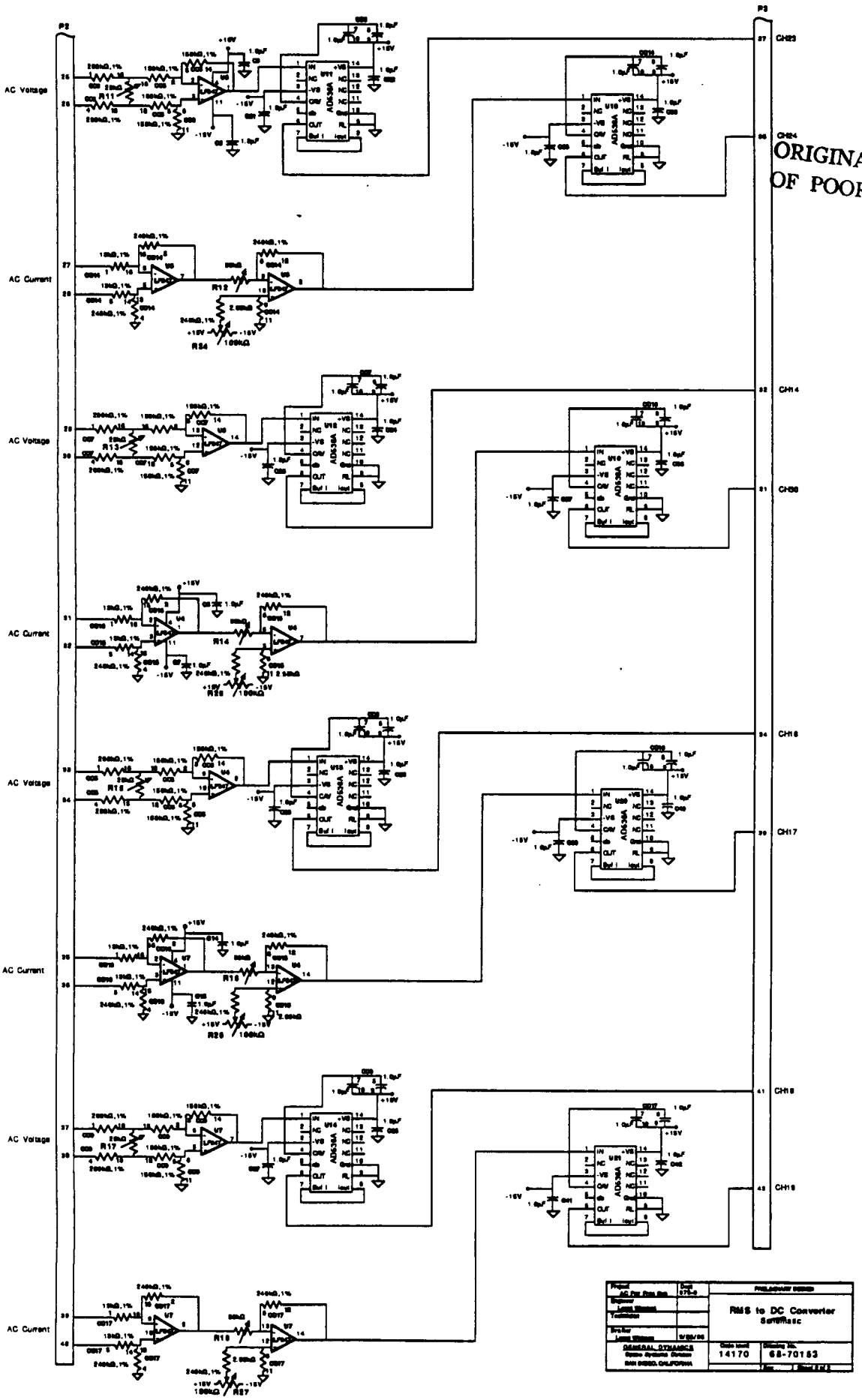


Project	Dept	PRELIMINARY DESIGN
AC Testbed	873-9	
Engineer		**Frequency Synthesizer** Schematic
Technician		
Drafter	12/9/85	
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA	Code Ident 14170	Drawing No. 68-70115
		Rev. Sheet 1 of 1





Project: GD Breadboard	Dept: 873-0	PRELIMINARY DESIGN
Engineer: K. Schreiner	9/18/85	**Multibus I/O Board** Schematic
Technician: Tim T	9/22/85	
Drafter: S.HETPAS	7/18/86	
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA	Code Ident: 14170	Drawing No.
		Rev / Sheet 2 of 2



Project: AC Pwr Proc Brd	Dwg: 075-0	PRELIMINARY DESIGN
Engineer: James Wilkins		RMS to DC Converter Schematic
Technician		
Drafter: James Wilkins	9/20/95	
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA	Cage Code: 14170	Drawing No.: 68-70163
		Rev: Sheet 2 of 3

LeRC RS422 Pin Assignments

	Driver Cabinet						Receiver Cabinet		
	Computer Cable		Reconfiguration Cable		RS422 T-Line		Computer Cable		
Signal	186/03 26-Pin	Int. Panel 37-Pin	Int. Panel 37-Pin	Rear Panel 37-Pin	Rear Panel 37-Pin	Rear Panel 37-Pin	Rear Panel 37-Pin	186/03 26-Pin	Signal
-	1	1	-	-	-	-	-	-	-
-	2	20	-	-	-	-	-	-	-
-	3	2	-	-	-	-	-	-	-
TR(A)	4	21	21	22	22	22	22	6	DM(A)
TR(B)	5	3	3	4	4	4	4	7	DM(B)
DM(A)	6	22	22	21	21	21	21	4	TR(A)
DM(B)	7	4	4	3	3	3	3	5	TR(B)
-	8	23	-	-	-	-	-	-	-
-	9	5	-	-	-	-	-	-	-
CS(A)	10	24	24	26	26	26	26	14	RS(A)
CS(B)	11	6	6	8	8	8	8	15	RS(B)
RT(A)	12	25	25	30	30	30	30	22	TT(A)
RT(B)	13	7	7	12	12	12	12	23	TT(B)
RS(A)	14	26	26	24	24	24	24	10	CS(A)
RS(B)	15	8	8	6	6	6	6	11	CS(B)
RD(A)	16	27	27	29	29	29	29	20	SD(A)
RD(B)	17	9	9	11	11	11	11	21	SD(B)
-	18	28	-	-	-	-	-	-	-
-	19	10	-	-	-	-	-	-	-
SD(A)	20	29	29	27	27	27	27	16	RD(A)
SD(B)	21	11	11	9	9	9	9	17	RD(B)
TT(A)	22	30	30	25	25	25	25	12	RT(A)
TT(B)	23	12	12	7	7	7	7	13	RT(B)
-	24	31	-	-	-	-	-	-	-
RC	25	13	13	13	13	13	13	25	RC
-	26	32	-	-	-	-	-	-	-

Appendix D

Test Plan

This test plan is included with this report to show the reader what tests were actually performed, and thereby provide a perspective for the significant test results described in Section 5.4.3. In addition to the reduced data presented there, comprehensive engineering data was collected and reduced to provide a base for the design of Space Station flight hardware, and to provide a basis for the estimation of its performance.

A complete discussion of the testing and the data, along with the actual data sheets and photographs, is included in the test report (Reference 8) which was published separately.

PERFORMANCE TESTING AND CHARACTERIZATION TEST PLAN

CONTRACT NAS3-24399

LeRC AC POWER SYSTEM TESTBED

REVISION B

JANUARY 26, 1987

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L. WAPPES

APPROVED BY
J. MILDICE

1.0 SCOPE

This test plan provides the requirements for the testing of the AC Power System Testbed to be designed and constructed by General Dynamics / Space Systems Division and delivered to NASA / Lewis Research Center. It describes the device under test, tests to be performed, instrumentation to be used, and parameters to be measured. The tests are designed to measure and investigate system performance parameters to verify correct operation of the 25 kW AC Power System Testbed. Data will be recorded and correlated to achieve an integrated description of the system operation.

2.0 DEVICE UNDER TEST

The device to be tested is an ac power system testbed that uses the resonant ac power approach devoloped by General Dynamics. The testbed is representative of a Space Station power system and includes: dc-to-ac inversion, high voltage and high frequency ac power transmission, fault-isolation switches, distributed payload power processing and computer control. A description of the testbed follows.

Six single-phase, 4.2 kW inverter modules will be configured to deliver 25 kW to the 20 kHz bus as shown in the system block diagram in Figure 2-1. These driver modules can be operated from a 150 to 200 Vdc. For each inverter module there is a corresponding transformer that steps up the output of the inverter to the bus voltage (440 Vrms, line to neutral). The inverters, transformers and the bus are reconfigureable so that either single-phase or three-phase power distribution is possible.

Three load interface modules will be connected via step-down transformers to the bus 100 meters from the system drivers. The first of these modules is the dc receiver module that will convert 20 kHz ac power to dc power over a voltage range of 25 to 150 Vdc and a maximum power capability of 5.0 kW. The second module is an ac reciever and converts single-phase 20 kHz ac power to variable-voltage, variable-frequency three-phase power. Its output has a voltage range of 0.0 to 115 Vrms, and frequency range of 14 Hz to 3.33 kHz, and a maximum capability of 25.0 kW. The last receiver module is a bidirectional module. It converts 20 kHz power to dc power and the reverse. It has a dc voltage of 150 and a power capability of 10.0 kW in either direction of power flow.

Fault-isolation switches will be located between the bus and every power module so that a fault in any module or its transformer can be isolated from the system (see Figure 2-1). The switches will have fault detection capability. System conditions will also be monitored by the system computer controller which will also have the ability to open any of the fault isolation switches should conditions warrant.

All of the reciever module outputs will have closed-loop feedback control to regulate output voltages and frequencies. The output voltages will be sensed and compared to a reference voltage to produce an error signal. The error signal will be minimized by either modifying the firing angle of the SCRs or omitting some 20 kHz pulses. The bus voltage will also be regulated locally. The voltage and frequency references used in the local module regulation will be provided by the computer.

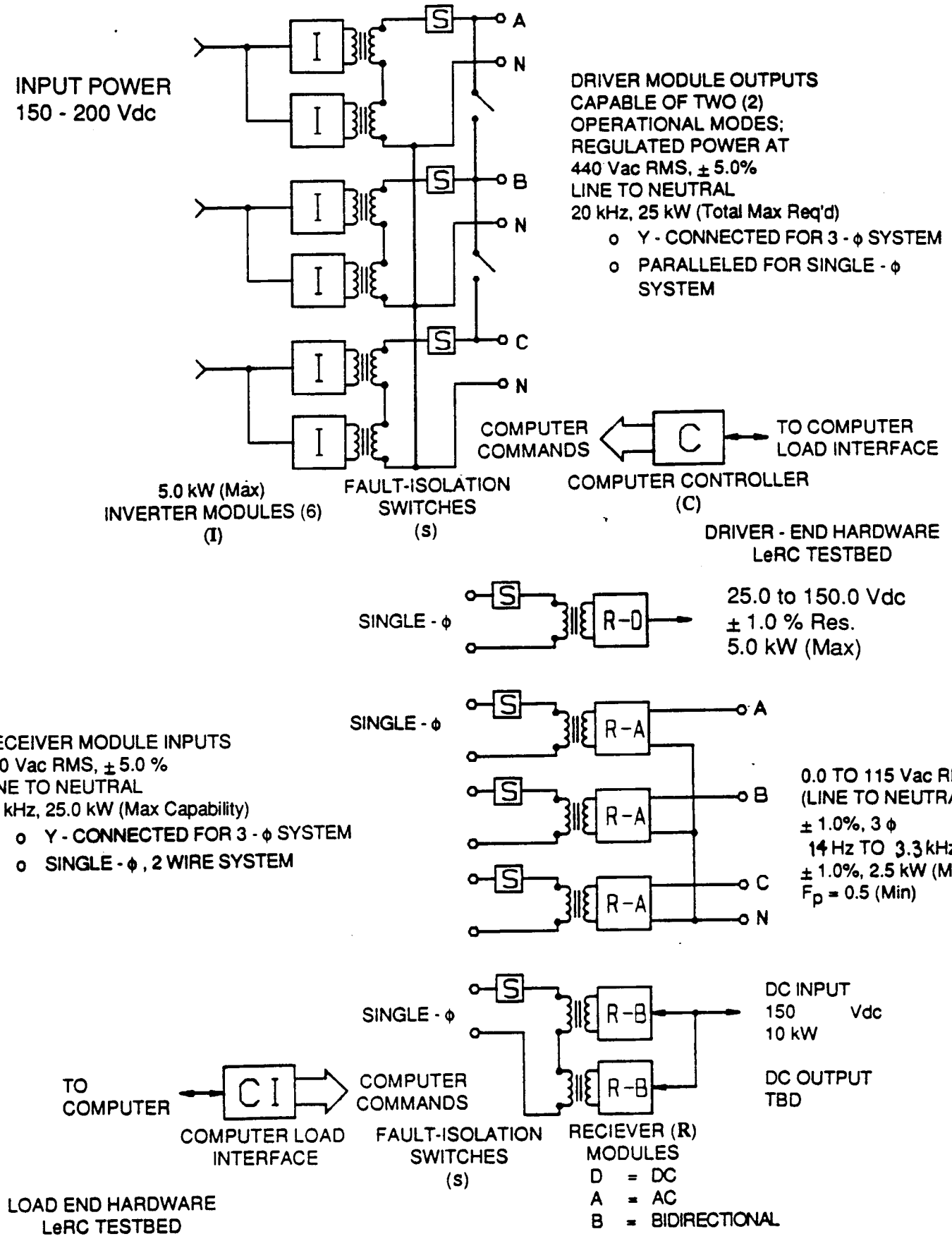


FIGURE 2-1. AC TESTBED BLOCK DIAGRAM.

2.1 ELECTRICAL PERFORMANCE

2.1.1 SYSTEM POWER

25.0 kW maximum.

2.1.2 BUS VOLTAGE

440 Vrms, line to neutral (single-phase or three-phase).

2.1.3 INPUT POWER

150 to 200 Vdc

2.1.4 OUTPUTS

a. 25 to 150 Vdc, 5.0 kW
b. 0.0 to 115 Vrms, 14 Hz to 3,33 kHz, 25 kW maximum
c. 150, 10.0 kW maximum, bidirectional

2.2 MODULAR BREAKDOWN

The modular arrangements of the system configuration are shown in the block diagram of Figure 2-1.

2.2.1 DRIVERS

The resonant drivers are synchronized to a common clock and operate at 20 kHz. The inverters have closed-loop voltage regulation. A schematic is shown in Figure 2-2.

2.2.2 SYSTEM BUS

The bus will be capable of being configured as a three-phase or single-phase line. It will be 100 meters in length and operate at 20 kHz and with a line voltage of 440 Vrms (440 Vrms, line to neutral voltage in the three-phase case).

2.2.3 LOAD MODULES.

Three types will be tested:

2.2.3.1 DC RECEIVER MODULE.

This module will convert 20 kHz power from the bus to dc with an output voltage range of 25.0 to 150.0 Vdc. The module is equipped with output voltage regulation. The output voltage is sampled and compared to a reference voltage to create an error signal. The control electronics for this module minimizes this error signal by either modifying the SCR firing angle or by omitting more or fewer 20-kHz pulses. See Figure 2-3.

2.2.3.2 THREE-PHASE, AC RECEIVER MODULE.

This 25.0-kW module converts single phase, 20-kHz power to variable-frequency, variable-voltage, low-frequency power. The output voltage and frequency are regulated by sampling the module output, comparing it to a voltage level, and producing and error signal. The error signal is then minimized by modifying the firing angle of the SCRs or by omitting more or fewer 20-kHz pulses from the transmission line. In this way, the output of the module can range from 0.0 to 115 Vrms and 14 Hz to 3.33 kHz. See Figure 2-4.

2.2.3.3 BIDIRECTIONAL, DC RECEIVER MODULE.

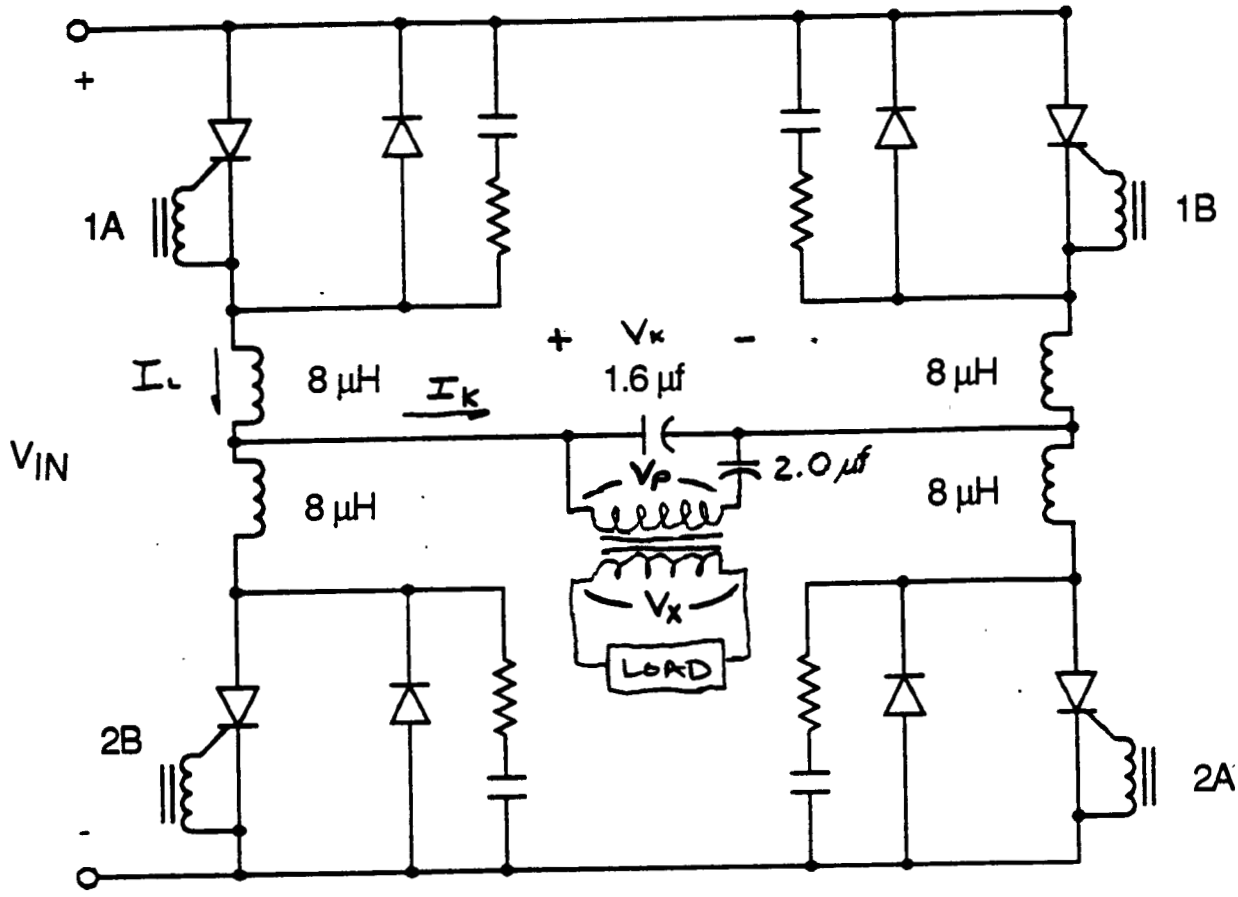
This 10.0-kW module is capable of bidirectional power flow between the 20-kHz bus and a 150-Vdc source or load. The module has voltage regulation on its output regardless of whether the output is the bus or a dc load. The regulation is attained by sampling the output, comparing it to a predetermined reference level, and producing an error signal between the two. The error signal is then minimized. See Figure 2-5.

2.2.4 FAULT-ISOLATION SWITCH.

These switches will be placed between every system power module and the bus and will be capable of isolating the module from the bus in case of a fault in a module or transformer. See Figure 2-6. The control circuitry of the switches monitors the voltage of the bus and current into the module. If either of these parameters exceeds a prescribed value, the switch will be opened and the module and its transformer removed from the bus. The switch can also be operated from the system controller computer.

2.2.5 SYSTEM CONTROLLER COMPUTER.

The computer will monitor system voltages, currents, and frequencies of the driver modules, the receiver modules, and the bus.



SCRs	C364M
SNUBBERS	110 Ω
	.01 µF

FIGURE 2-2. DRIVER MODULE.

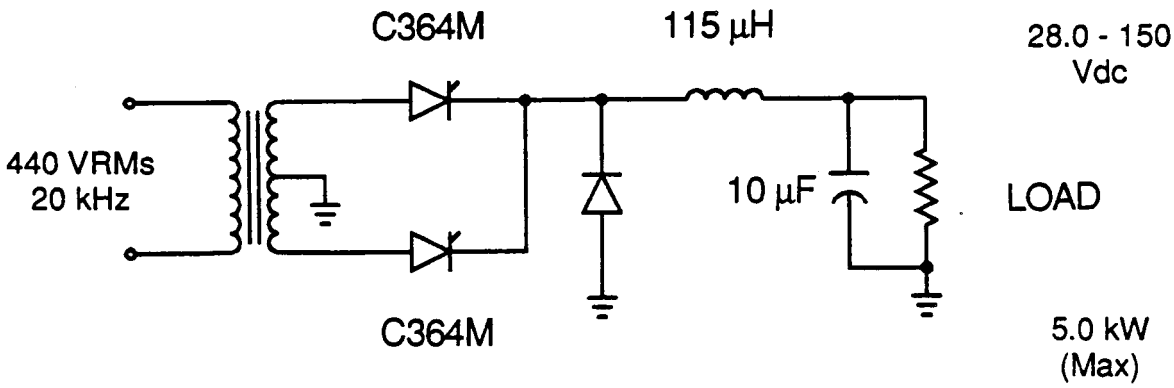


FIGURE 2-3. DC RECIEVER SCHEMATIC.

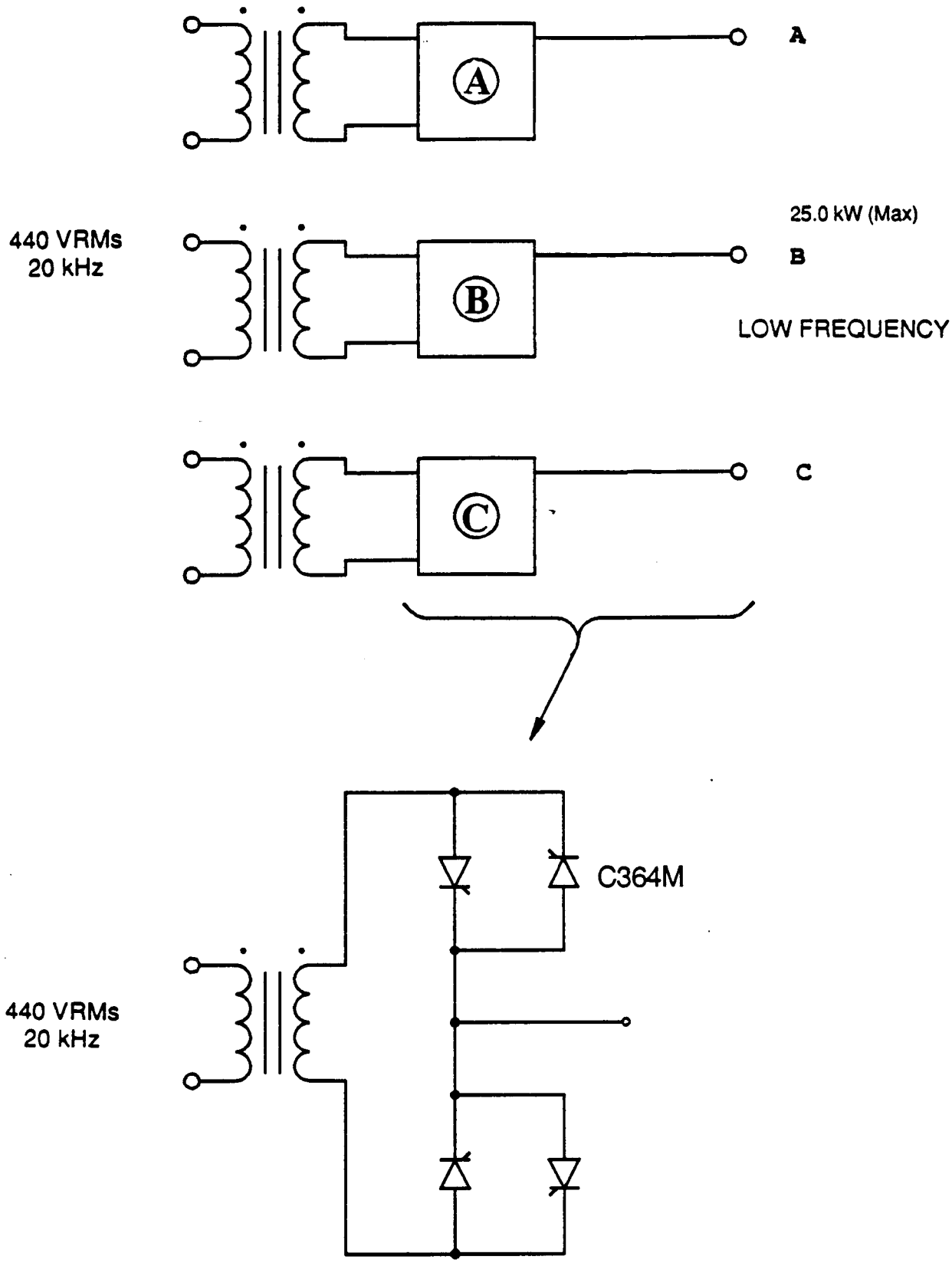


FIGURE 2-4. THREE-PHASE, AC RECEIVER SCHEMATIC.

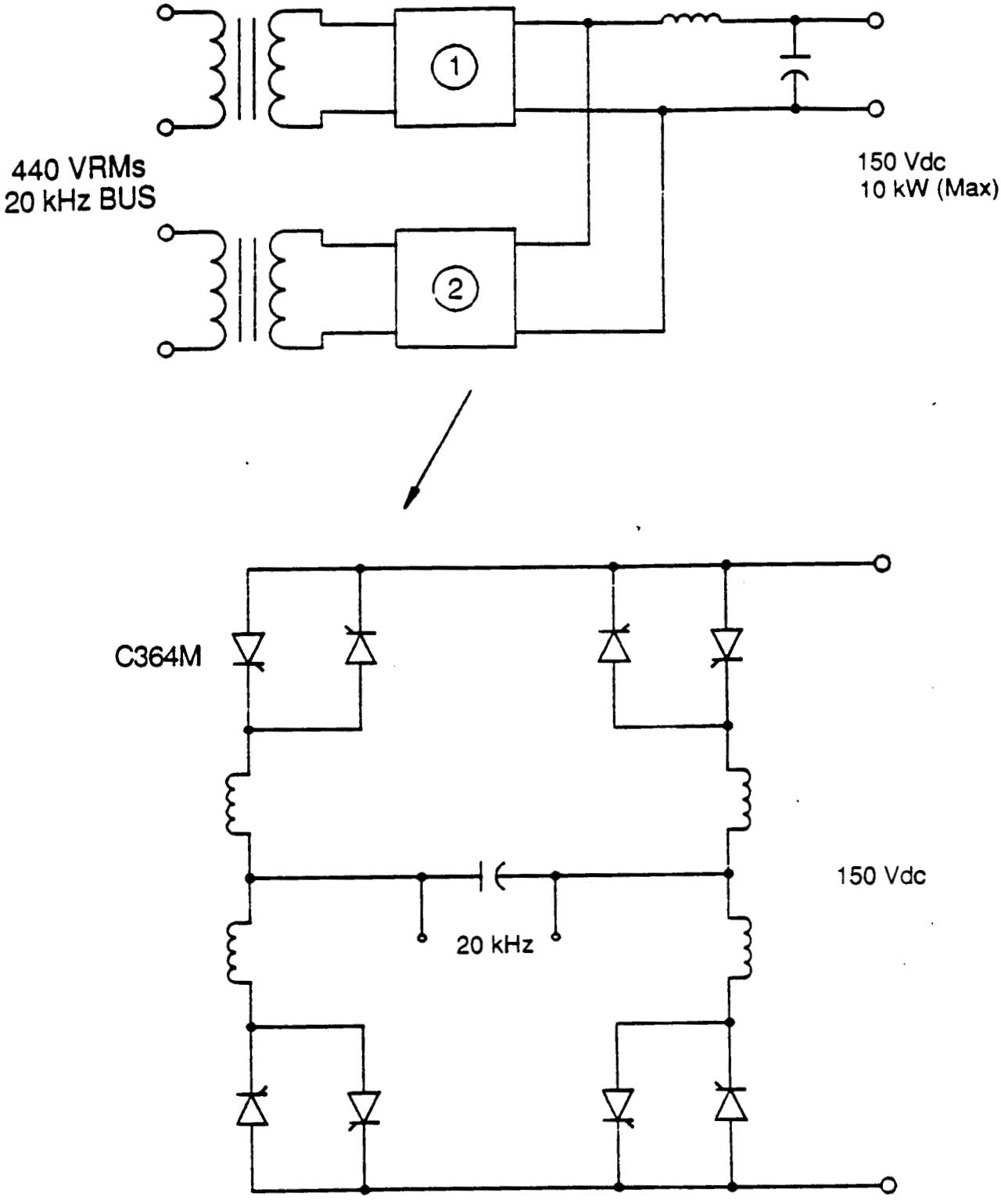


FIGURE 2-5. BIDIRECTIONAL RECEIVER SCHEMATIC.

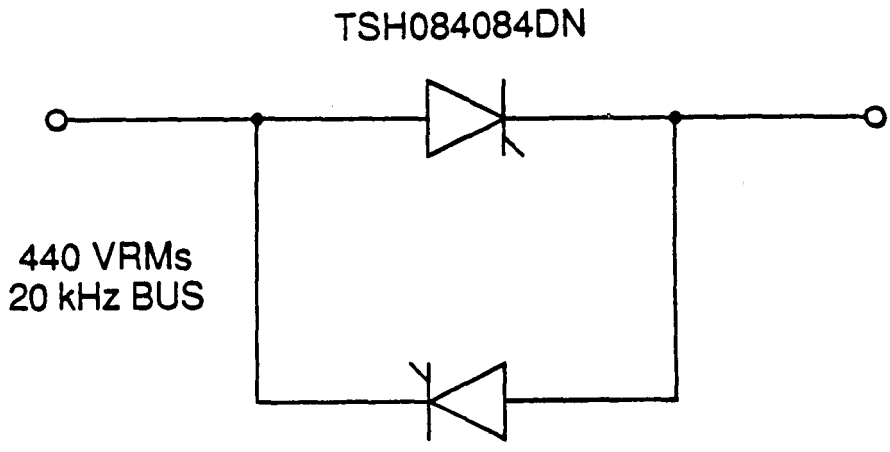


FIGURE 2-6. FAULT-ISOLATION SWITCH CONFIGURATION.

INSTRUMENT DATA SHEET

MEASUREMENT EQUIPMENT	MANUFACTURER	MODEL NO.	CALIBRATION CONTROL NO.	CALIBRATION DATE	CALIBRATION DUE

FIGURE 3-1. INSTRUMENT DATA SHEET.

3.0 TESTING

3.1 INSTRUMENTATION

All test measurements will be performed using instrumentation maintained and calibrated in accordance with General Dynamics and DCAS procedures for engineering laboratory equipment. Evidence of such calibration will be provided on the "Instrument Data Sheet" (Figure 3-1) by recording the appropriate calibration log numbers and dates in the spaces provided. Other detailed data will be provided documenting each instrument as shown in Figure 3-1.

Steady-state analog data (such as voltage, current, power, etc.) will be recorded manually from laboratory instruments such as the Clarke-Hess 255 V-A-W meter and the Fluke 8810A digital multimeter. Transient or waveform data will be recorded photographically, directly from oscillosdcope faces and presented as annotated photo-reproductions with scale factors and test conditions included. The measurement instruments to be used and the accuracy of each is listed in Table 3-1.

3.2 TESTS

The individual tests, parameters, and measurements specified to fulfill this test plan are documented in matrix form in Tables 3-2 and 3-3. In general, eight major types of tests will be performed on the testbed.

3.2.1 START UP

The system input waveforms and bus waveforms as well as the output waveforms of each receiver module will be monitored as the system is started. This will test will be run while the system is loaded for dc inputs.

3.2.2 STEADY-STATE OPERATION

Steady-state system measurements will be made for four system cases:

a. LIGHT LOAD:

DC Receiver: 500 W
Bidirectional DC Receiver: 1.0 kW
V/F AC Receiver: 2.5 kW

b. BALANCED LOAD:

DC Receiver: 5.0 kW
Bidirectional DC Receiver: 8.0 kW
V/F AC Receiver: 8.0 kW

c. AC RECEIVER LOAD:

DC Receiver: OFF
Bidirectional DC Receiver: OFF
V/F AC Receiver: 25.0 kW
(The three inverter pairs will be synchronized and placed in parallel)

d. RECEIVER TEST:

DC Receiver: 5.0 kW
Bidirectional DC Receiver: 10.0 kW
V/F AC Receiver: 25.0 kW

(This test will measure the performance of the receivers to determine if they meet the specifications.)

TABLE 3-1. MEASUREMENT INSTRUMENTS

INSTRUMENT		DESCRIPTION	WORST CASE ACCURACY
Clarke-Hess 255		Volt-Amp-Watt Meter	Volts/Amps: ±0.2% of reading Power: ±0.5% of reading
Fluke	80I-600	AC Current Probe	±1.5% of full scale ±0.5% of reading
HP 3466A		DMM	True RMS: ± 1.0% of reading DC: ±0.04% of reading
HP 4275A		L-C-R Meter	±0.1% of reading
HP 5315A		Universal Counter	±0.005% of reading
Fluke	8810A	DMM	DC Volts: ±0.01% of reading True RMS: ±0.4% of reading Ave. AC Volts: ±1.0% of reading
SRI	900083	Ammeter	±1.0% of reading
Tektronix	DM501A	DMM	±0.1% of reading
Tektronix	DM502A	DMM	±0.2% of reading
Tektronix	A6303/AM503	Current Probe/Ampifier	±3.0% of reading
Tektronix	A6302/AM503	Current Probe/Ampifier	First 100ns: ±5.0% of reading After 100 ns: ±3.0% of reading
Tektronix	7104	Oscilloscope	Vertical: ±1.0% of reading Horizontal: ±1.0% of reading
Tektronix	7603	Oscilloscope	Vertical: ±1.0% of reading
Tektronix	7633	Oscilloscope	Vertical: ±1.0% of reading
Tektronix	7104/7A24/ P6062	Oscilloscope/Amplifier/ V. Probe	±5.0% of reading
Tektronix	7104/7A26/ P6062	Oscilloscope/Amplifier/ V. Probe	±4.0% of reading
Tektronix	7104/7A18/ P6062	Oscilloscope/Amplifier/ V. Probe	±4.0% of reading
Tektronix	7104/7A29/ P6062	Oscilloscope/Amplifier/ V. Probe	±5.0% of reading
Tektronix	7603/7A18/ P6062	Oscilloscope/Amplifier/ V. Probe	±5.0% of reading

TABLE 3-1 (Continued)

INSTRUMENT		DESCRIPTION	WORST CASE ACCURACY
Tektronix	7633/7A18/ P6062	Oscilloscope/Amplifier/ V. Probe	±5.0% of reading
Tektronix	7633/7A24/ P6062	Oscilloscope/Amplifier/ V. Probe	±5.0% of reading
Tektronix	7633/7A26/ P6062	Oscilloscope/Amplifier/ V. Probe	±5.0% of reading
HP 334A		Distortion Analyzer	0.1% full scale
HP 8566A		Spectrum Analyzer	Frequency: ±2% full scale Amplitude: ±2% of reading

TABLE 3-2. KEY

SYMBOL	PARAMETER MEASURED	INSTRUMENT
VS	Steady-State Voltage	Voltmeter
IS	Steady-State Current	Ammeter
VT	Transient Voltage	Oscilloscope-Camera
IT	Transient Current	Current Probe-Oscilloscope-Camera
PS	Steady-State Power	V-A-W Meter
n	Efficiency	Calculation from PS
T	Total Harmonic Distortion	Distortion Analyzer
f	Frequency	Frequency Counter
I_L	Inverter Resonant Inductor Current	Current Probe-Oscilloscope-Camera
V_K	AC Resonant Tank Voltage of Inverter	Oscilloscope-Camera
V_X	Secondary Transformer Voltage	Oscilloscope-Camera
I_X	Secondary Transformer Current	Current Probe-Oscilloscope-Camera

TABLE 3-2. KEY

SYMBOL	PARAMETER MEASURED	INSTRUMENT
VS	Steady-State Voltage	Voltmeter
IS	Steady-State Current	Ammeter
VT	Transient Voltage	Oscilloscope-Camera
IT	Transient Current	Current Probe-Oscilloscope-Camera
PS	Steady-State Power	V-A-W Meter
n	Efficiency	Calculation from PS
T	Total Harmonic Distortion	Distortion Analyzer
f	Frequency	Frequency Counter
I_{Leg}	Inverter Resonant Inductor Current	Current Probe-Oscilloscope-Camera
I_K	AC Resonant Tank Current of Inverter	Current Probe-Oscilloscope-Camera
V_K	AC Resonant Tank Voltage of Inverter	Oscilloscope-Camera
V_X	Secondary Transformer Voltage	Oscilloscope-Camera
I_X	Secondary Transformer Current	Current Probe-Oscilloscope-Camera
V_P	Primary Transformer Voltage	Oscilloscope-Camera

Steady-state system measurements will be made throughout the system according to Table 3-3. The results will be compared against the electrical specifications of the testbed listed in Table 3-4 for each of the four cases previously described. Measurements will be made of the transmission frequency. Power will be measured at various points throughout the system, so that efficiency can be determined for each system module. The input and output voltages and currents of each of the modules will be recorded, which will include the recording of the output voltage ripple of the receiver modules. Each of the receiver modules will be be tested individually with the inverters and compared with the electrical specifications of the receivers listed in Table 3-5.

The waveforms of the internal voltages and currents of the driver modules will be photographed. Load and line voltage regulation will be measured on the bus and load voltage regulation will be measured on each of the receiver module outputs. Both forward and reverse power delivery will be demonstrated on the bidirectional and ac receiver modules. This test will also record the waveforms of critical voltage and current stress such as current peaks, voltage peaks, dv/dt, and di/dt experienced by the semiconductor components.

3.2.3 TRANSIENT LOAD RESPONSE

The change to the input and output waveforms of the system modules as well as the internal waveforms of the driver modules will be photographed as the receivers are added to and removed from the system abruptly. The receivers will be switched at full load. The voltage and frequency of the bus as well as the output voltage of the receiver modules will be monitored during the load switching to determine the effect.

3.2.4 FAULT CONTROL TESTING

The system input voltage and current, bus voltage and current, and the outputs of the three receiver modules will be monitored as faults are placed on various locations on the testbed system. Both bus and user faults will be simulated. Two levels of fault protection will be tested.

A. Fault-Isolation Switches - The fault-isolation switches will be commanded from the computer to react to a voltage below the nominal and a current above the nominal settings. A load exceeding these values will be placed on the bus causing the switches to sense an overload condition and open.

B. Inverter Current Limiting - In the same way, the commanded current limit value will be reduced for the inverters. A load exceeding this current value will be placed on the bus with the fault-isolation switches off causing the inverters to lower the output voltage to keep the current within the setting.

3.2.5 POWER FACTOR OPERATION

Loads with power factors of 0.7 lagging and 0.7 leading will be applied to the bus to determine the system response. The bus will be loaded to the full 8.5 kVA for both parts of this test.

3.2.6 MOTOR OPERATION

The output of the ac receiver module will be connected to the 1.0-Hp induction motor and will be tested for its ability to start and operate the motor at variable speeds.

3.2.7 EMI TESTING

A spectrum analyzer will be used to measure the harmonic components on the bus of the system testbed. The harmonic components will be measured on both ends of the bus. This will be done for two cases:

A. Resistive Loads
B. Receiver Loads
   DC Receiver: 5.0 kW
   Bidirectional Receiver: 8.0 kW
   AC Receiver: 8.0 kW

3.2.8 POWER TURN OFF

The response of the power system to having the input power removed will be measured. The input and output voltages and currents of each module and the bus will be monitored as will the internal voltages and currents of the driver modules while the system is loaded to 25.0 kW and the power removed.

3.3 SUMMARY

At the completion of the testing, proper operation of the AC Power System Testbed will have been verified. The testbed has the following components.

3.3.1 DRIVER MODULES

The voltage-regulated bus power will be provided by six, resonant inverter modules each operating at 4.2 kW. Each module will operate from either a dc or 60-Hz ac source.

3.3.2 BUS

A 100-meter bus will distribute 25.0 kW of 20 kHz power to the loads at 440 Vrms. The bus is configurable and can be operated as either a 440-Vrms, single-phase line or a wye-connected, 440-Vrms (line to neutral) bus.

3.3.3 FAULT-ISOLATION SWITCH

High-voltage bus switches are located between the bus and each power module and are capable of detecting and removing bus or module faults from the system.

3.3.4 RECEIVER MODULES

a. One unidirectional load module for a 5.0-kW, dc load.
b. One bidirectional load module for a 10.0-kW, dc load or source.
c. One load module for a 25.0-kW, three-phase, ac load.

3.3.5 COMPUTER CONTROLLER

The microprocessor will monitor the system bus for fault conditions and also determine the level of system voltages and frequencies.

TEST / MEAS. PT.	POWER TURN ON	STEADY-STATE OPERATION				TRANSIENT LOAD RESPONSE	FAULT CLEARING	POWER FACTOR OPERATION	MOTOR OPER.	EMI TESTING	POWER TURN OFF
		DC IN MIN LOAD	DC IN BAL LOAD	DC IN 25KW AC	RECEIVER TEST						
SYSTEM INPUT	YT,IT	YS,IS PS,n	YS,IS PS,n	YS,IS PS,n	n	YT,IT	YT,IT	YS,IS	YT,IT YS,IS	EMI	YT,IT
INVERTER	$Y_{K,}\ ^{I}{}_{L}$	$Y_{K,}\ ^{I}{}_{L}$ PS,n	$Y_{K,}\ ^{I}{}_{L}$ PS,n	$Y_{K,}\ ^{I}{}_{L}$ PS,n	n	$Y_{K,}\ ^{I}{}_{L}$	$Y_{K,}\ ^{I}{}_{L}$	$Y_{K,}\ ^{I}{}_{L}$ $Y_{P,}\ ^{I}{}_{K}$	$Y_{K,}\ ^{I}{}_{L}$		$Y_{K,}\ ^{I}{}_{L}$
BUS	YT,IT	YS,IS PS,n	YS,IS PS,n	YS,IS PS,n	n	YT,IT	YT,IT	YS,IS	YT,IT YS,IS	EMI	YT,IT
DC RECEIVER		YS,IS PS,n	YS,IS PS,n		YS,IS PS,n	YT,IT	YT,IT			EMI	
BIDIRECTIONAL DC RECEIVER		YS,IS PS,n	YS,IS PS,n	YS,IS PS,n	YS,IS PS,n	YT,IT	YT,IT			EMI	
AC RECEIVER		YS,IS PS,n	YS,IS PS,n	YS,IS PS,n	YS,IS PS,n	YT,IT	YT,IT		YT,IT YS,IS	EMI	

TABLE 3-3. TEST PLAN MATRIX

TABLE 3-4. TESTBED ELECTRICAL SPECIFICATIONS

PARAMETER	NOMINAL	SPEC. RANGE	MEASURED
Input Voltage (DC)	150 Vdc	150-300 Vdc	
Input Voltage (AC)	208 Vrms	198-218 Vrms	
Bus Voltage (Inverter End)	440 Vrms	418-462 Vrms	
Bus Voltage (Receiver End)	440 Vrms	418-462 Vrms	
Bus Volt. Drop (End to End)			
Bus Frequency	20.0 kHz	19.8-20.2 kHz	
DC RECEIVER			
Output Volt. Range	150 Vdc	25-150 Vdc	
Output Cur (150V)	33.3 Adc	33.3 Adc Max.	
Output Pwr(150V)	5000 W	5000 W Max	
AC RECEIVER			
Output Voltage(Line-to-Line)	200 Vrms	0-200 Vrms	
Output Cur (200V)	72.5 Arms	72.5 Arms Max	
Output Pwr (200V)	25.0 kW	25.0 kW Max	
BIDIRECTIONAL RECEIVER RECEIVING MODE			
Output Voltage	150 Vdc	143-158Vdc	
Output Current	67 Adc	67 Adc Max.	
Output Power	10.0 kW	10.0 kW Max.	

TABLE 3-5. TESTBED REVEIVER ELECTRICAL SPECIFICATIONS

PARAMETER	NOMINAL	SPECIFICATION	MEASURED
DC RECEIVER			
Outout Volt. Range	150 Vdc	25-150 Vdc	
Output Cur (Full Load-150V)	33.3 Adc	33.3 Adc Max.	
Output Pwr(Full Load-150V)	5000 W	5000 W Max	
Output Ripple (Full Load)	----	1.0%	
Input Current (Full Load)	12.0 Arms	25.0 Arms Max.	
AC RECEIVER			
Outout Volt. Range(L-L)	200 Vrms	0-200 Vrms	
Output Cur. (Full Load 200V)	72.5 A rms	72.5 A rms Max	
Output Pwr (Full Load 200V)	25.0 kW	25.0 kW Max	
Output Ripple (Full Load)	---	1.0% Max.	
Input Current (Full Load)	60 A rms	75 A rms	
Output Distortion (Full Load)	1.0 %	5.0 % Max.	
Outout Frequency Range	14-3300Hz	14-3330 Hz	
Load Power Factor	1.0	0.5 Max.	
BIDIRECTIONAL RECEIVER			
RECEIVING MODE			
Outout Voltage	150 Vdc	143-158 Vdc	
Outout Cur. (Full Power)	67 Adc	67 Adc Max.	
Outout Power (Full Load)	10.0 kW	10.0 kW Max.	
INVERTING MODE			
Bus Voltage	440 Vrms	418-462 Vrms	
Bus Frequency	20.0 kHz	19.8-20.2 kHz	

Measurement / Parameter	CALIBRATED @	MONITOR
DRIVER		
DC VOLTAGE A IN		
DC CURRENT A IN		
DC VOLTAGE B IN		
DC VOLTAGE B IN		
DC VOLTAGE C IN		
DC VOLTAGE C IN		
SW A--VOLTAGE		
SW A--CURRENT		
SW B--VOLTAGE		
SW B--CURRENT		
SW C--VOLTAGE		
SW C--CURRENT		
RECEIVER		
DC--VOLTAGE		
DC--CURRENT		
B/D--VOLTAGE		
B/D--CURRENT		
VAC--VOLTAGE		
VAC--CURRENT		
SW 1--VOLTAGE		
SW 1--CURRENT		
SW 2--VOLTAGE		
SW 2--CURRENT		
SW 3--VOLTAGE		
SW 3--CURRENT		
SW 4--VOLTAGE		
SW 4--CURRENT		
SW 5--VOLTAGE		
SW 5--CURRENT		

TABLE 3-6. COMPUTER MONITOR CALIBRATION TABLE