HIGH DATA RATE MODEM SIMULATION FOR THE
SPACE STATION MULTIPLE-ACCESS COMMUNICATIONS SYSTEM

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ABSTRACT

The communications system for the Space Station will require
a space-based multiple-access component to provide communi-
cations between the space-based program elements and the
station.   A study was undertaken to investigate two of the
concerns of this multiple-access system, namely, the issues
related to the frequency spectrum utilization and the possi-
bilities for higher-order (than QPSK) modulation schemes for
use in possible modulators and demodulators (modems).

As a result of the investigation, may key questions about
the frequency spectrum utilization were raised.   At this
point, frequency spectrum utilization is seen as an area
requiring further work.

Simulations were conducted using a computer-aided communica-
tions system design package to provide a straw-man modem
structure to be used for both QPSK and 8-PSK channels.
Areas of further work on the modem design are identified.

INTRODUCTION

The Space Station (SS) will have a Multiple-Access Communi-
cations System (MACS) as one of its subsystem elements.   The
general structure and requirements of the MACS have been
described in [1].   The MACS will be responsible for the
space-to-space segment communications as part of the overall
SS communications system.   The MACS will need to interface
with the on-station communications networks and the space-
to-ground communications network.

The following will all be users of the MACS at one time or
another:

        a) NSTS (space shuttle),
        b) Orbital Transfer Vehicle (OTV),
        c) Orbital Maneuvering Vehicle (OMV),
        d) Flight Telerobotic Servicer (FTS),
        e) Extra-Vehicular Activity/Extravehicular Mobility
           Unit (EVA/EMU),
        f) Co-Orbiting Platform (COP),
        g) Free-Flyer (FF),
        h) Mobile Servicing Centre (MSC)

Each of these users will have different data requirements by data type and data rate. The types and rates which have been identified for use on the MACS are as follows:

a) audio, command (CMD), telemetry (TLM) and user data channels each at 128 Kbps,
b) video channels at 22-25 Mbps,
c) heads-up displays (HUD) at 400 Kbps
d) emergency safety link (ESL) at a rate to be determined but most likely with an upper limit of 128 Kbps.

A matrix showing the SS elements with their associated data types and rates is given in Table 1.

PROJECT OBJECTIVES

Of the broad possible areas of MACS design, it was decided to concentrate on the possibilities for using higher-order modulation schemes for digital data transmission and the associated frequency planning to be used with such a scheme.

In the area of frequency planning, an investigation of the required bandwidth for the data channels was to be performed and a possible strategy for the MACS was to be developed. Also, areas of concern relating to the frequency plan were to be identified.

For the higher-order modulation study, a candidate modem structure which could be used in the SS environment and simulated via the available computer-aided design software was to be provided. This candidate modem would then be used as the basis for more detailed further study.

FREQUENCY PLAN

In order to plan the spectrum, an assessment of the total data needs from all users is needed. Next, a survey of the available choices needs to be made and then identify candidate placements for the MACS frequency spectrum.

FREQUENCY SPECTRUM UTILIZATION

To develop the frequency plan, an accounting of the the data-link requirements is made from the data presented in Table 1. Based upon these estimates, the forward and return

Table 1. Data requirements for Space Station Multiple Access Communications System users.

User	# Links	Max Range	Forward	Type	Return	Type
FF	0(8)	2000 Km	CMD	NB	TLM	NB
			Data	NB	Data	NB
					Video	WB
COP	0(1)	2000	CMD	NB	TLM	NB
					Video	WB
NSTS	1(2)	37	Audio	NB	Audio	NB
			Data	NB	Data	NB
OMV	1(2)	37(185)	CMD	NB	TLM	NB
					Video	WB
EMU/ EVA	2(4)	1	Audio	NB	Audio	NB
			HUD	MB	TLM	NB
					Video	WB
MSC	1(1)	0.1	CMD	NB	TLM	NB
					(3)Video	WB
FTS	1(1)	0.1	CMD	NB	TLM	NB
			ESL	NB	(4)Video	WB
OTV	0(1)	185	CMD	NB	TLM	NB
					Video	WB

Notes: The number of links shows the initial configuration with the possible growth in parenthesis; the link type of NB corresponds to 128 Kbps, MB to 400 Kbps, and WB to 25 Mbps. Data taken from [2] and [3].

link requirements for Initial Operating Conditions (IOC) and projected growth (Growth) are summarized as follows:

      a) forward links will require for IOC(Growth)
          1) 8(31) 128-Kbps links,
          2) 2(4) 400-Kbps links,
          3) no forward video links (at present);
     b) return links will require for IOC(Growth)
          1) 9(34) 128-Kbps links,
          2) no requirement fpr 400-Kbps links,
          3) 10(16) 25-Mbps links.

There is no requirement for 100% availability on all links simultaneously. This leads to a suggested frequency plan as shown in Figure 1 where a design limitation of 300 MHz total bandwidth was used. This plan assumes that there will be some form of time-division access to the wide-band video channels. This plan will also allow for all of the medium-band and narrow-band channels, i.e., 400-Kbps and 128-Kbps, respectively, to be accomodated. In planning this spectrum utilization an assumption was made that a spectrally-efficient form of modulation would be found so that the up-to 100-Mbps data sources would occupy the same spectral bandwidth as a 25-Mbps source would.

FREQUENCY-BAND SELECTION

Based on [3], Ku-Band (12-18 GHz) was used as the frequency band for placement of the MACS. However, Ku-Band is presently heavily allocated by international agreement as shown in [5]. Another possible frequency band to be used for the MACS is Ka-Band (27-40 GHz). This spectral band is presently not heavily allocated. However, there may be problems related to directivity of antennas among other areas for this to be a realistic contender at this time.

MODEM DESIGN

The second phase of this project was to consider candidate modem structures for higher-order modulation applications.

While Quadrature Phase Shift Keying (QPSK) is considerd to be quite standard in many current applications, the required video data links push the design into the area of greater spectral efficiency. This is then the motiviation behind looking at higher modulation orders. In this section, the design drivers for a MACS modem and the modem structures investigated during this project are presented.
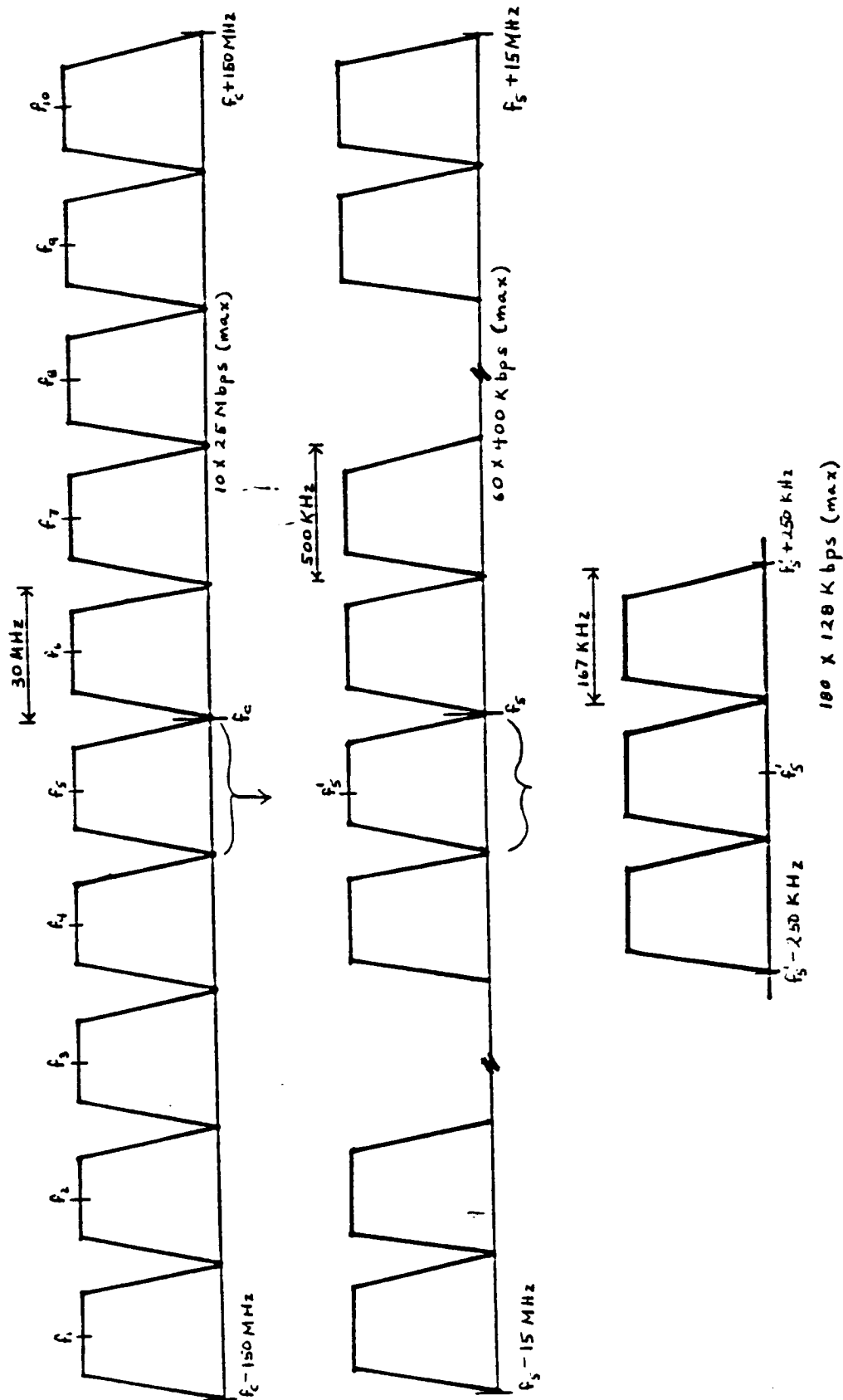
Figure 1. Candidate spectrum utilization for forward and return links. Assumes a spectral efficiency of 83.3% would be used in the modem realization.

DESIGN DRIVERS

The design drivers on the selection of modem for the MACS are

a) a basic compatability with current technology which would allow existing QPSK sources to make some use of the MACS,
b) the design should allow for an evolution from QPSK to be made in a controlled growth environment,
c) the theoretical Bit Error Rate (BER) performance should not intrinsically require extensive data or symbol coding to achieve a design specification of 10**-5,
d) the modem package should not tend towards requiring extensive amounts of signal processing equipment to do its job, i.e., be portable and battery operated.

With these ground rules, selection of a higher-order modulation scheme and candidate modulators and demodulators proceeded.

SELECTION OF MODULATION FORMAT

There are two basic modulation schemes which can reasonably be developed based upon a QPSK structure: some form of higher-order PSK modulation or Quadrature Amplitude Modulation (QAM). This is because mathematically, QPSK can be seen as being either a case of M-ary PSK or M-ary QAM. This then rules out some form of Frequency Shift Keying (FSK) being considered.

It can be shown [6] that the M-ary PSK and M-ary QAM both have theoretical spectral efficiencies of ℓ /2 bits/sec/Hz where

$$\ell = \log_2(M).$$

Therefore, there is no intrinsic preference for an overall modulation scheme based upon theoretical efficiency arguments.

The required energy-per-bit to noise-power ratio (Eb/No) to achieve a specified BER performance for the different M-ary PSK and QAM modulation formats is illustrated in [7]. Theoretically, QPSK requires an Eb/No of 13 dB at the specified BER and one would like to stay as close to this as possible. The next higher orders of PSK and QAM above QPSK are 8-PSK and 16-QAM which require an Eb/No of 18 dB and 20 dB, respectively. Above that, it would appear that we would require significant amounts of coding to close the link and subsequently cut the data throughput so the search for an

appropriate higher modulation scheme stops here. At this
level, the basic goal of providing enough video channels for
the MACS can be met with a combination of frequency- and
time-division multiplexing. Since 8-PSK modulation would
appear to require less power to close the link, it was
decided to concentrate on it for this study.

CANDIDATE MODULATORS

It has been shown [8] that M-ary PSK modulators can be built
by cascading stages of QPSK modulation. If $\log_2(M)$ is not
evenly divisible by four, then some form of data mapping
must be provided to synthesize the full signal constella-
tion. A candidate modulator to do just this was proposed to
NASA/JSC [9]. This modulator had the additional feature of
allowing switching so that it could be run as either a
standard QPSK modulator or as an 8-PSK modulator. As orig-
inally presented, this modulator had the basic QPSK channels
and the added channels reversed. The mapping was modified
to correct this condition. The resulting signal constella-
tion and mapping function are shown in Figure 2.
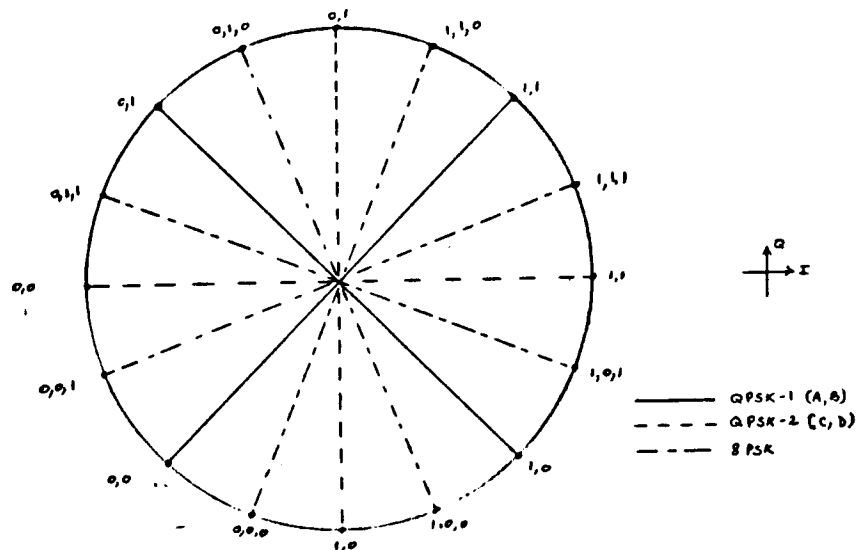
CANDIDATE DEMODULATORS

A possible demodulator for the 4/8-PSK modulator described
above was also provided to NASA/JSC [9]. This demodulator
was basically the inverse process of the modulator and
contains two phase-staggered QPSK demodulators. While this
structure shows every reasonable probability of working, it
was decided to investigate the possibility of making this
structure simpler and possibly even allowing one coherent
demodulator work for both QPSK and 8-PSK. A literature
search was performed to identify candidate demodulators and
they are as follows:

    a) Polarity Costas Loop [10]
    b) combined Squaring/Quadrupling Loop [11]
    c) Tanlock Loop [12].

The Polarity Costas Loop (PCL) structure is an extension of
the typical Costas Loop structure for demodulating QPSK
signals but with the hard limiters replaced by multi-level
limiters. The resulting demodulator is only slightly more
complicated than a normal QPSK demodulator. However, the
PCL will require a tight Automatic Gain Control (AGC) to
work properly. Since the MACS will probably require an AGC
this is not seen as being too stringent of a drawback.

The combination of a squaring/quadrupling loop, while simi-
lar to QPSK demodulators, would essentially require two de-
modulators in one package to have switchable 4- and 8-PSK.

(a)

Input Data			Modulator Input				Data Recovery Logic		
							d1	d2	d3
d1	d2	d3	A	B	C	D	sgn(I)	sgn(Q)	|I|>|Q|
0	0	0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	1	0	1	0	1	0
0	1	1	0	1	0	0	0	1	1
1	0	0	1	0	1	0	1	0	0
1	0	1	1	0	1	1	1	0	1
1	1	0	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1

to QPSK #2
to QPSK #1
Added data Channel
Permanent data Channels

(b)

Figure 2. The 8-PSK signal constellation and data mapping. (a) The two QPSK signal constellations and the resulting 8-PSK constellation. (b) The three-to-four-bit data input and output mapping (octal mapping).

The tanlock loop, while being a very efficient digital phase-locked loop for tracking M-ary PSK signals, may have some implementation problems because arctangent functions would need to be synthesized at high data rates. However, the tanlock loop does offer more immunity to input signal gain variations than does the PCL.

MODEM STRAW-MAN DESIGN

Based upon the available choices at this time for a modem structure the following components were chosen upon which to perform simulations:

a) the 4/8-PSK modulator with signal constellation correction,
b) the Polarity Costas Loop demodulator for in-phase (I) and quadrature-phase (Q) channel extraction,
c) a data extractor which recovers the data channels from the I and Q outputs of the PCL and has a data synchronizer with data clock recovery.

The PCL was chosen because of its ability to extract both QPSK and 8-PSK from a signal. The data extractor performs the decoding logic and then is followed by a data clock extractor and synchronizer. The data clock extractor was developed by TRW and used in the simulator without modification. The data synchronizer was a set of sample-and-hold circuits synchronized to the data clock extractor. The block diagrams for these components will be given below when the simulations are described in more detail.

SIMULATION RESULTS

Basic simulations of the candidate modem structure were performed during the project period using the Computer-Aided Design (CAD) system available within the Tracking and Communications Division of JSC. In this section we will describe the simulation environment and the models used in the simulation runs.

SIMULATION ENVIRONMENT

The CAD system used to perform the simulations is a commercially-available product known as the Block Oriented System Simulator (BOSS) [13] which runs on a Digital Equipment VAX Station II workstation. For these simulations, version 1.1 of BOSS was used. BOSS is a menu-driven package using both a mouse and keyboard entries to develop and document system modules. The philosophy of BOSS is to develop standard modules at the block-diagram level and then used these

modules to construct larger modules until an end-to-end
system is designed. BOSS provides a variety of basic
blocks. If a more complicated module is needed then these
basic blocks along with any other blocks the user has
created may be combined to build new blocks. Eventually,
the blocks are combined to form the end-to-end system.

Simulations of the system proceed by having the user specify
simulation duration, time step, and any necessary parameters
to make the modules work properly. Usually, the module
parameters specified at simulation time are those design
parameters, e.g. filter bandwidth, which one is trying to
optimize for the system. Prior to starting the simulation,
"probes" on signal paths may be specified for data collec-
tion. Families of simulations may then be run to optimize
parameters and to generate signal plots for documentation
and anlaysis.

MODEM BLOCK DIAGRAMS

The candidate test system consisted of a 8-PSK transmitter
module and the combination PCL and data recovery modules for
a receiver. The combined system is shown in Figure 3 while
the modulator and demodulator subsystems are shown in Figure
4. At this point, no system noise sources were introduced.
The 8-PSK transmitter consisted of a three-channel random
data source (with each channel seeded with different star-
ting numbers), the candidate 4/8-PSK modulator (set for 8-
PSK only), and an output bandpass filter. The block dia-
gram for the 4/8-PSK modulator is illustrated in Figure 5.
The output bandpass filter was set for first-order Butter-
worth characteristics and a single-sided bandwidth of five
times the data rate which effectively gave an "infinite-
bandwidth" system.

The receiver consisted of the PCL demodulator followed by a
data recovery module. The block diagrams for these modules
are illustrated in Figure 6. Internal to the data recovery
module is the TRW-developed data transition tracking loop
which was used to produce data outputs at constant relative
phase.

SIMULATION RUNS

During the time of this project, only one type of simulation
was able to be performed. This simulation passed 25 bits
through the test system to verify correct operations of the
components on the simulator. Although the system was set
for 8-PSK only, the correct operation of the demodulator
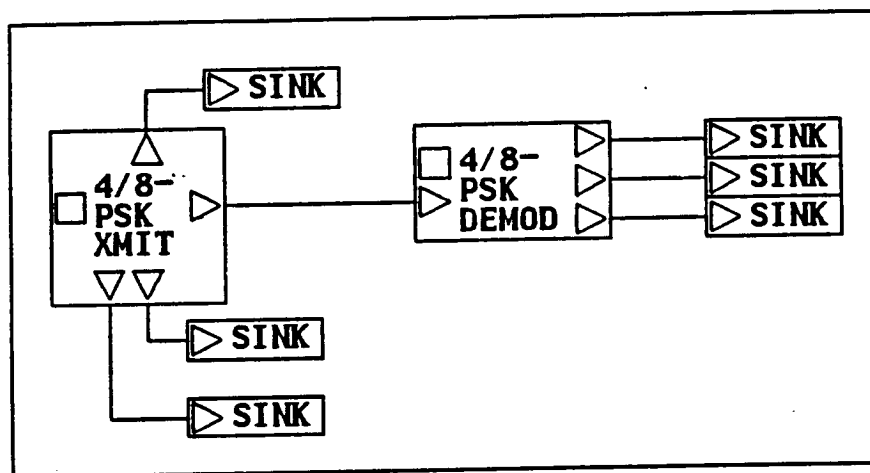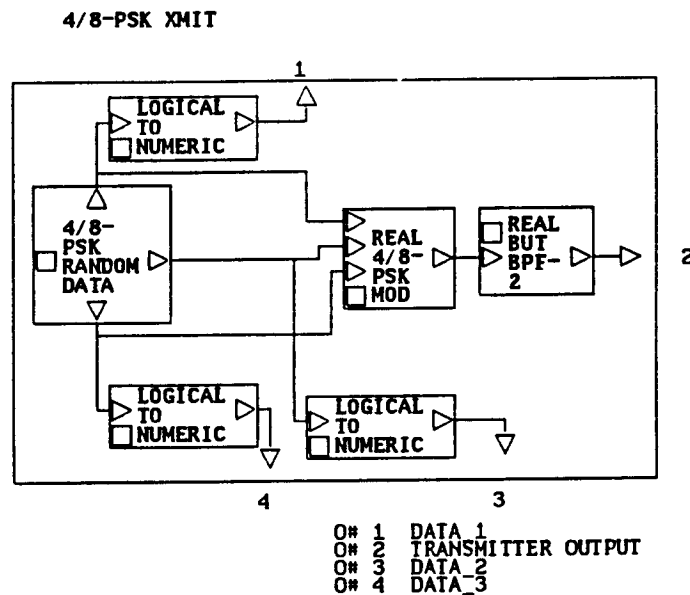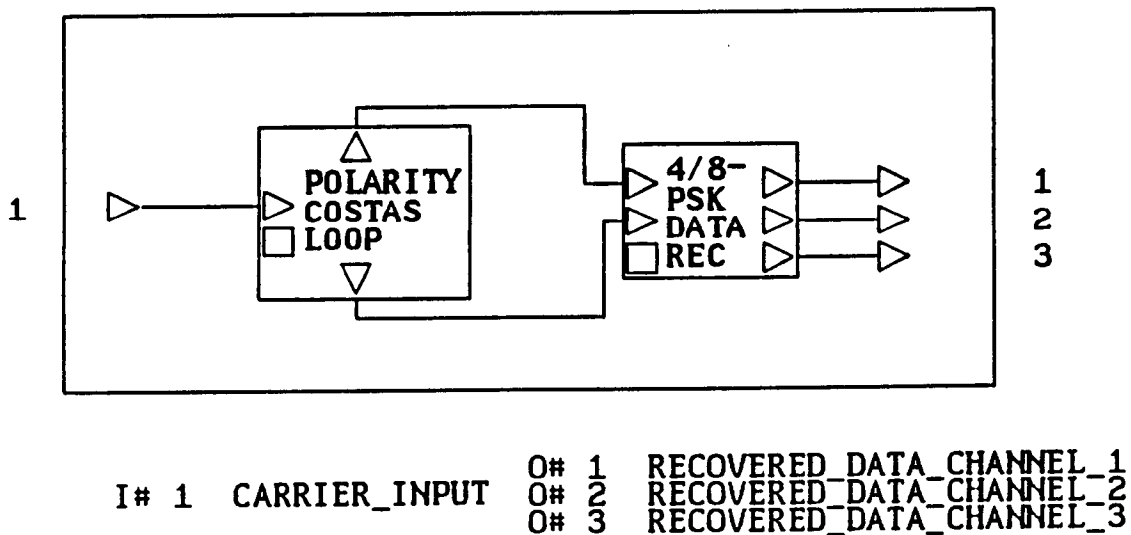shows that it can also be used to demodulate QPSK as well.

4/8-PSK_TEST_SYSTEM

Figure 3. The 4/8-PSK test system block diagram used for the BOSS simulations.

4/8-PSK XMIT


```
O# 1   DATA_1
O# 2   TRANSMITTER OUTPUT
O# 3   DATA_2
O# 4   DATA_3
```

(a)

4/8-PSK DEMOD

I# 1   CARRIER_INPUT

```
O# 1   RECOVERED_DATA_CHANNEL_1
O# 2   RECOVERED_DATA_CHANNEL_2
O# 3   RECOVERED_DATA_CHANNEL_3
```

(b)

Figure 4. The expanded modulator and demodulator block dia-
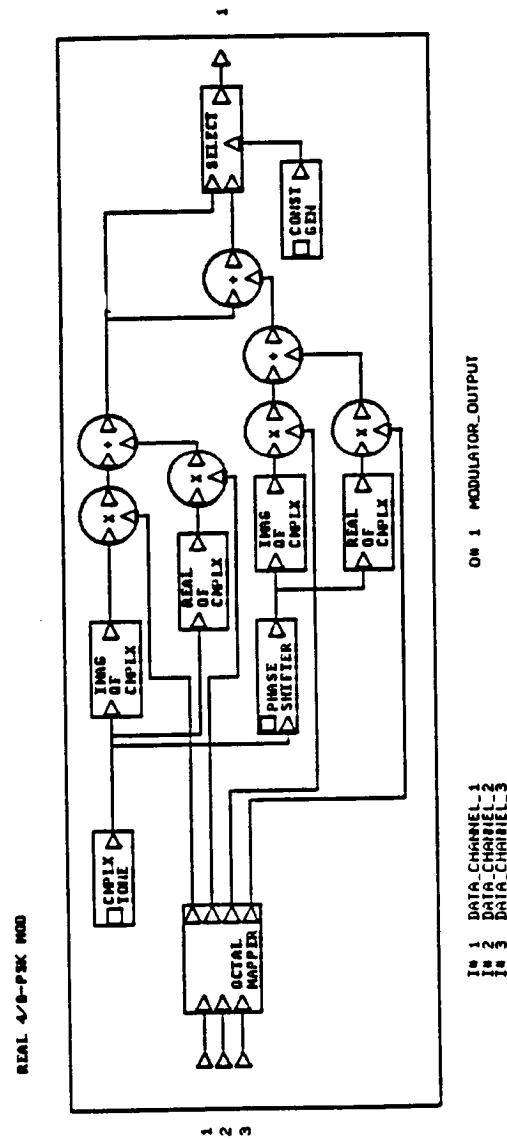gram used for the BOSS simulations. (a) the modulator. (b)
the demodulator.

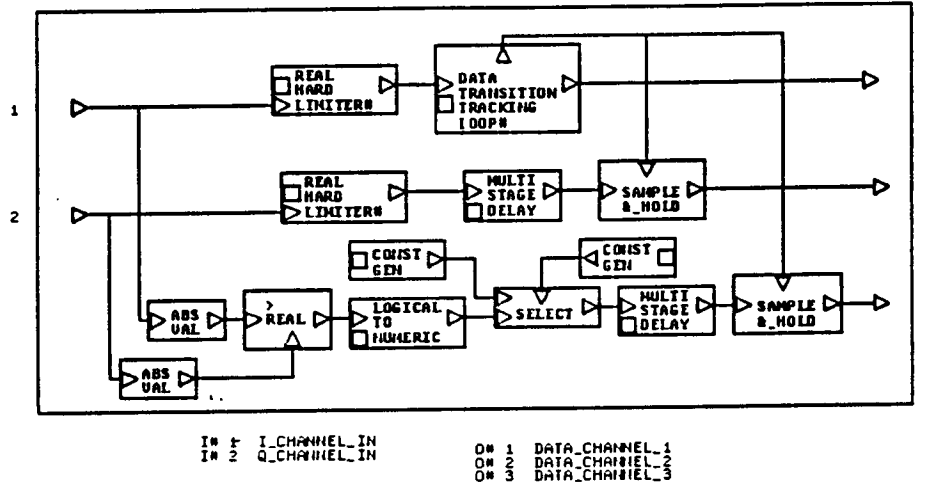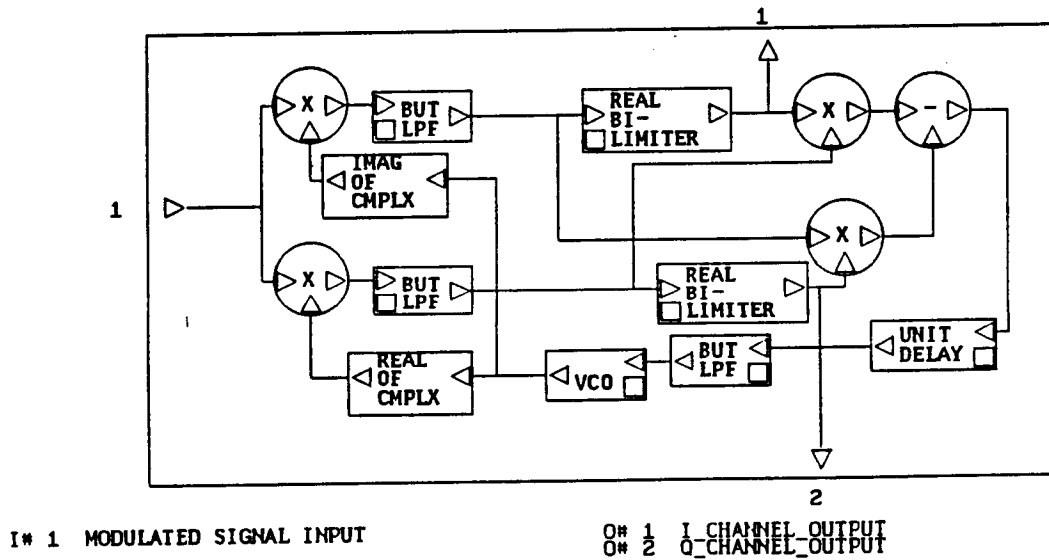REAL 4/8-PSK MOD

OK 1 MODULATOR_OUTPUT

I# 1 DATA_CHANNEL_1
I# 2 DATA_CHANNEL_2
I# 3 DATA_CHANNEL_3

Figure 5. The expanded block diagram for the 4/8-PSK modulator used for the BOSS simulations.

4/8-PSK DATA REC

REAL HARD LIMITER#

DATA TRANSITION TRACKING LOOP#

REAL HARD LIMITER#

MULTI STAGE DELAY

SAMPLE &_HOLD

CONST GEN

CONST GEN

ABS VAL

> REAL

LOGICAL TO NUMERIC

SELECT

MULTI STAGE DELAY

SAMPLE &_HOLD

ABS VAL

1
2
3

I# 1 I_CHANNEL_IN
I# 2 Q_CHANNEL_IN

O# 1 DATA_CHANNEL_1
O# 2 DATA_CHANNEL_2
O# 3 DATA_CHANNEL_3

(a)

POLARITY COSTAS LOOP

X

BUT LPF

REAL BI- LIMITER

X

—

IMAG OF CMPLX

1

X

BUT LPF

REAL BI- LIMITER

X

REAL OF CMPLX

VCO

BUT LPF

UNIT DELAY

1

2

I# 1 MODULATED SIGNAL INPUT

O# 1 I_CHANNEL_OUTPUT
O# 2 Q_CHANNEL_OUTPUT

(b)

Figure 6. The BOSS simulation receiver structure. (a) the Polarity Costas Loop structure, (b) the 4/8-PSK Data Recovery Module.

15-15

FINDINGS

In this section, we will summarize the major findings of this project in the areas of frequency spectrum usage and simulation of the candidate modem.

FREQUENCY UTILIZATION

Based upon the brief look at the frequency planning issue, no obvious choice for a location in Ku-Band was found to place the MACS. What was found is that there are areas which still need to be worked on to give a better understanding of the design issues. These issues include the following points:

a) what will be the optimum spectral placement of the MACS based upon
   1) non-interference with Tracking and Data Relay Satellite System (TDRSS) links used by SS and others,
   2) non-interference with allocated satellite services,
   3) link power budget and expected interference with and from ground sources;
b) will the spectrum need to be broken onto forward and return bands and if so what will need to be their relative widths;
c) are there any spectral shaping constraints, e.g., from the FCC, which must be adhered to and which may affect the design;
d) how many intermidiate frequencies and what type of signal gain control will be needed in the transmitters to multiplex the low and high data rates;
e) might a different frequency band be better, e.g., Ka-Band or might a split be preferable where the near users requiring low directivity use Ku-Band and the far users employ the intrinsic directivity of Ka-Band.

SIMULATION RESULTS

In the second area, the baseline infinite-bandwidth candidate modem system with no noise was able to be constructed to verify the correct operation of all of the sub-components. There are further studies which need to be performed to extend the design. The types of simulations which need to be performed are as follows:

a) linear channel simulations to assess the effects of finite bandwidth and Gaussian noise on the modem performance;
b) simulations to assess effects of non-linearities in

the expected channel due to
1) amplifier performance,
2) multipath and fading in the channel,
3) adjacent and co-channel interference;
c) the effects of AGC performance on the demodulation
performance of the PCL.

These simulations should also be run with other demodulation
techniques not studied here to determine the most robust
design.

There is also a need for a study to determine the optimum
method for running a detailed simulation. Rough estimates
of the required computer time to run a detailed simulation
indicate substantial fractions of a year may be necessary.
There exist techniques [14] to cut this down by orders of
magnitude in linear systems. How these techniques may be
incorporated into BOSS and how they may be extended to non-
linear channels needs to be investigated.

CONCLUSIONS

The overall conclusions of this study are as follows:

a) the issue of the frequency plan for the MACS is not
yet settled, however, needs to be done soon because
it will affect the design of the modems used and
affect the way in which the MACS is managed;
b) the 4/8-PSK modulator with associated PCL and data
recovery functions can make an initial modem struc-
ture for further study; there are many design is-
sues to be settled but it represents a reasonable
start because the combination holds out the promise
of increased spectral efficiency over QPSK, it can
be an evolutionary design, and the same demodulator
can be used for both QPSK and 8-PSK.

As pointed out in the Findings above, both areas have fur-
ther issues to be studied.

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