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MICROPROCESSOR CONTROL AND NETWORKING FOR THE AMPS BREADBOARD

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ABSTRACT

Future space missions will require more sophisticated power systems. This sophistication necessarily implies higher costs and more extensive crew and ground support involvement. In order to decrease this human involvement, as well as protect and most efficiently utilize this important resource, NASA has undertaken major efforts to promote progress in the design and development of autonomously managed power systems. Two areas being actively pursued within this effort are autonomous power system (APS) breadboards and knowledge-based expert system (KBES) applications. APS breadboards are viewed as a requirement for the timely development of knowledge-based systems. Not only will they serve as final testbeds for the various KBES applications within this domain, but they will in fact play a major role in the knowledge engineering phase of their development.

The current power system breadboard designs are of a distributed microprocessor nature. The distributed nature, plus the need to connect various external computer capabilities (i.e., conventional host computers and symbolic processors), places major emphasis on effective networking.

This paper presents the communications and networking technologies for the first power system breadboard/test facility in the agency. Primary emphasis is on the the task of networking the host computer into the system.

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INTRODUCTION

As the exploration of space continues missions become much more complex and much longer in duration. Future missions such as Space Station, spaced-based radar, communication and surveillance satellites, strategic defense initiative (SDI) systems and military aircraft will thus require more sophisticated and intricate electrical power systems (EPS). Space power is an extremely precious resource. The fact that almost every subsystem, especially those that support the human elements for manned missions, is dependent on power plus the fact that space power has historically cost about $1000.00/KWH versus $.05 per terrestial KWH has placed space power high on NASA's priority list of research efforts. As was learned from Skylab, for which 15-18 ground support personnel were required to augment extensive crew involvement for an 8KW system, a major effort had to be directed toward autonomously managed electrical power systems.

Automating activities ordinarily performed by humans was seen as the primary means of reducing both airborne and ground support efforts and costs. Additionally, more fully autonomous power systems (as well as other subsystems) will be a necessity for deeper unmanned exploration of space where missions will require decisions and actions in "real-time". The time lags incurred with data transmission and remote intervention will not be acceptable in allocating and protecting the precious electrical power resources. In 1978, therefore, the Office of Aeronautics and Space Technology at NASA Headquarters directed NASA to undertake efforts towards accomplishing such autonomy. Since that directive various NASA efforts in conjunction with several contractors (including Martin Marietta, Rockwell/Rocketdyne, Boeing, TRW, Hughes and Ford Aerospace) and Universities (among them Auburn, University of Tennessee, Tennessee Tech.,University of Alabama- Huntsville,Vanderbilt and Carnegie Mellon) have made much progress in the realm of space power automation.

It was realized early on in power system investigations that autonomous systems would require a certain amount of embedded intelligence to supplement the already proven more conventional computer approaches. Thus much of the current research effort is focussed on artificial intelligence techniques. More specifically these efforts are directed toward the application of expert and knowledge-based systems (ES/KBS) technologies in such application areas as: energy storage management, power management (i.e. generation, monitoring and allocation), load management (i.e. prioritization and scheduling) and fault management (i.e. prediction, detection and advisement/recovery) [1].

The term "expert system" (ES) refers to a software system which performs a complex, well defined task using the same input information and problem solving strategies as a human expert. Additionally, an

expert system possesses the capability to make accessible to the user the reasoning logic it uses to perform the task. It is implied that the expertise captured by such a system has its origins in the experience that one or more humans have accumulated while performing a given problem solving task. The term "knowledge-based system" (KBS) refers to a software system much like an expert system but which implements a body of problem solving knowledge which may come from any of several sources including text books, humans(in the form of expertise or more general experiential knowledge) or others.

It is important in the domain of space power system applications to draw the distinction between these two types of systems. The reason for this is that this is a very young domain and "experts" with experience managing space power systems do not exist. However, the experience of humans working in this arena coupled with more general knowledge about power subsystems and components make it possible to develop what for the purposes of this paper will be referred to as knowledge-based systems expert systems (KBES).

Though few doubt the important role that KBES approaches will play in space power automation the domain is one which offers more complex challenges than those to which the technology has already been successfully applied. One of the approaches to overcoming some of these challenges is the development and utilization of fairly realistic power system breadboards and test beds on which KBES technologies can be developed and validated. With such facilities many of the tasks of knowledge engineering can be performed and the archiving of expert problem solving knowledge necessary for autonomous operation can proceed at a much more rapid rate than through actual mission experience alone [2,3].

This report deals with the current efforts of the Electrical Power Branch at Marshall Space Flight Center to complete the operationalization of the Autonomously Managed Power System (AMPS). More specifically, it will be concerned with the networking of the various AMPS components with primary emphasis on networking the host computer system. It was these efforts in which the author participated while on the NASA/ASEE fellowship.

OBJECTIVES

The objectives of this work included:

1. Become familiar with the software and networking environments of the AMPS breadboard.

   a. compile pertinent documentation available at MSFC for attaining such familiarity.

   b. procure/request all additional documentation.

   c. become familiar with proposed host computer system (i.e., hardware, operating system and networking capabilities).

2. Installation of NCR Tower communications board.

3. Evaluation of extent of previously perceived incompatibilities in connecting the NCR Tower host to the AMPS breadboard.

4. Proposal of solution strategy for software modification and development.

5. Undertake implementation of accepted solution strategy.

THE AUTONOMOUSLY MANAGED POWER SYSTEM (AMPS)

Amps Overview

The Space Power Distribution System Technology program commenced in 1978 as an overview study to define and assess multi-hundred kilowatt photovoltaic electrical power system concepts and technology development requirements. Based upon the study an integrated system-level approach to technology development was taken to encompass the following three tasks:

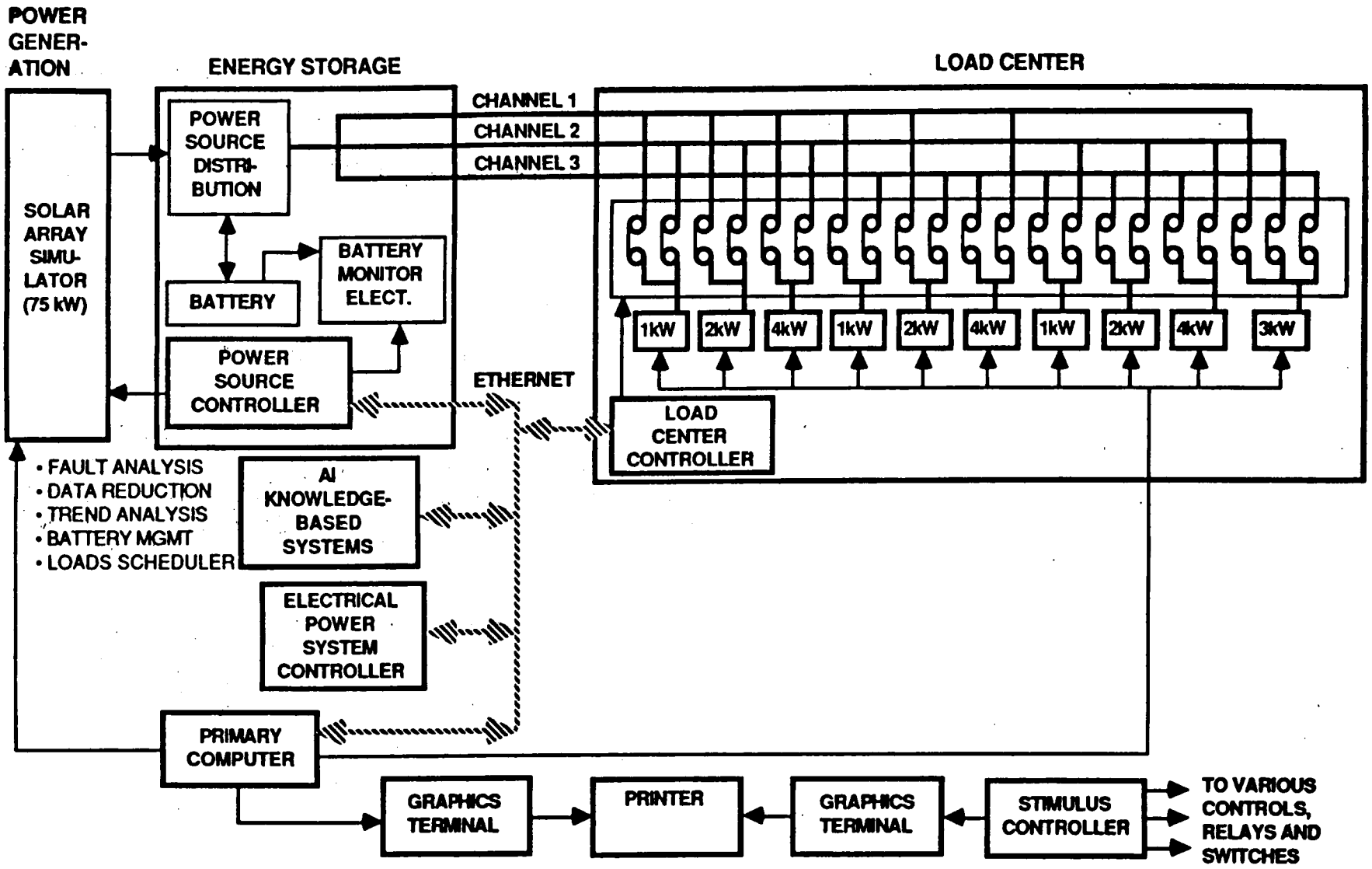
1. To define a reference 25Ø kilowatt electrical power system concept for low earth orbiting satellites which will be used to identify the related technology development needs and provide an investment criteria and payback assessment tool to guide the selection of technology development options.

2. To pursue the technology needs for the autonomous management of electrical power systems by developing selected controller hardware for a power management subsystem and the related algorithms of the power management subsystem.

3. To design, develop, and assemble a test bed that simulates a representative portion of the autonomously managed power system and the interfacing power sources, energy storage, and loads.

The result of these efforts has been the delivery, by the TRW Defense & Space Systems Group, of the autonomously managed power system test facility/broadboard (AMPS) to Marshall Space Flight Center Electrical Power Branch test facility [4,5].

The AMPS breadboard (Figure 1) is an end-to-end electrical power system with a power generation simulator, energy storage simulator and a power management and distribution system. AMPS is the result of direction by NASA Headquarters to address long-term, high power needs for future low earth orbit spacecraft. The system is representative of a multichannel, multikilowatt, utility-type power system and provides important new capabilities for demonstrating the feasibility of new technologies including knowledge-based expert systems. The power management portion of AMPS has three embedded micro-processor based controllers networked with Ethernet. This management area performs data collection and control functions required for autonomous operation and is therefore the area which will ultimately interface (via the Ethernet) with future ES/KBS developments. Potential ES/KBS include fault management, battery management, data reduction, trend analysis, state-



Figue 1 Autonomously Managed Power System

of-health monitoring and payload contingency scheduling. The breadboard is being connected to a host computer environment to include a graphics terminal and color ink-jet printer.

The current phase of the AMPS effort entails the actual development and testing of the proof-of-concept breadboard. The breadboard consists of:

- one 24 kilowatt load center;
- a 75 kilowatt solar array simulator (Power Generation);
- a 168 cell, 189 ampere hour, 240 volt nickel-cadmium battery with associated electronics (Energy Storage);
- a power management and distribution system consisting of three power channels (16 kilowatt total) and a load center with 21 load buses with associated switches and 24 kilowatts of load;
- a host computer system consisting of a primary computer (NCR Tower XP), two graphics terminals (Tektronics 4125P and 4105A), a color ink-jet printer (Tektronics 4691), and a stimulus controller (a second Tower XP);
- and the internal distributed controllers.

The Power Management System (PMS) is the "internal brains" of the actual breadboard and consists of three subsystem controllers and associated interface technology. The Power Source Controller (PSC) controls the power generation solar array simulator (SAS) and the energy storage system [6]. The Load Center Controller (LCC) is responsible for the load center while the Electrical Power System Controller (EPSC) functions as the breadboard interface to the outside world (host computer system) and is hierarchically above the PSC and the LCC [7,8]. The three internal controllers transmit all messages in the broadcast mode. These controllers utilize the FORTH computer language (using PolyForth) and are functional within their areas of domain as well as networked. At this time, no controller requests data or sends commands to the EPSC. Software for these controllers will continue to be developed in-house at MSFC and potentially by contractors.

Current efforts and those in which the author was involved under the summer fellowship are focused on attaching the NCR Tower XP multi-tasking host computer (which employs Multibus and has an installed ENP-30 communications board) to the Ethernet to allow the user to input commands to the breadboard for control and testing purposes and to receive data from the breadboard in order to monitor breadboard performance. The Tektronix 4125P graphics terminal, which functions as the user station, must be able to easily utilize the data received from the Tower and the Tower must be able to easily take data from the 4125P to send out over Ethernet. These two computers are currently physically

connected. The NCR Tower XP specifications are provided below:

- Processor/memory controller II (MC 68Ø1Ø CPU)
- Seven Multibus I/O slots
- 1 MB error correcting RAM memory
- one 5-1/4" flexible disk drive (1 MB)
- one cartridge tape drive (45 MB)
- one 8-channel HPSIO controller
- Unix V operating system
- C compiler
- FORTRAN/77 compiler
- menu driven software for system reconfiguration

The next several sections of this report will be primarily concerned with providing a more detailed description of the microprocessor and communications hardware and software of the Power Management Subsystem. For a detailed discussion of the other hardware components and their configuration in the AMPS breadboard the reader is referred to references.

Power Management System

The power management subsystem (PMS) as presented in Figure 2 consists of three microprocessor based controllers that communicate by means of an Ethernet LAN and functions to monitor and control the complete electrical power system from generation to load. This allows efficient and predictable performance of monitoring, processing, controlling and recording functions. The PMS is a decentralized processing system consisting of the three microprocessor based controllers plus I/O circuitry, command and display interfacing hardware and a data bus. The power source controller (PSC) and the load center controller (LCC) each perform functions related to their respective centers. The PSC performs the processes and procedures required to operate the power source and energy storage devices and their associated power electronics hardware. The LCC collects load current, load voltage, switch status and switch temperature data from each remote power controller. The third controller, the electrical power system controller (EPSC), performs subsystem level functions such as energy planning and allocation, load assignments, and command and data interfacing to the host computer. The I/O circuitry connects the controllers to temperature, voltage, current and status sensors as well as to the various power control circuits.

The configuration of the elements in the PMS is shown in block diagram form in Figure 3. As can be seen each controller contains a microcomputer board and communication board. These boards are Motorola 68ØØØ based and offer the availability of a high level language (FORTH). Additionally the PSC and LCC contain the necessary digital and analog I/O boards to accomplish their previously described functions. The controller components communicate via a parallel data bus which supports multiple processors and a large number of commercially available board level products. The communication board along with the data bus

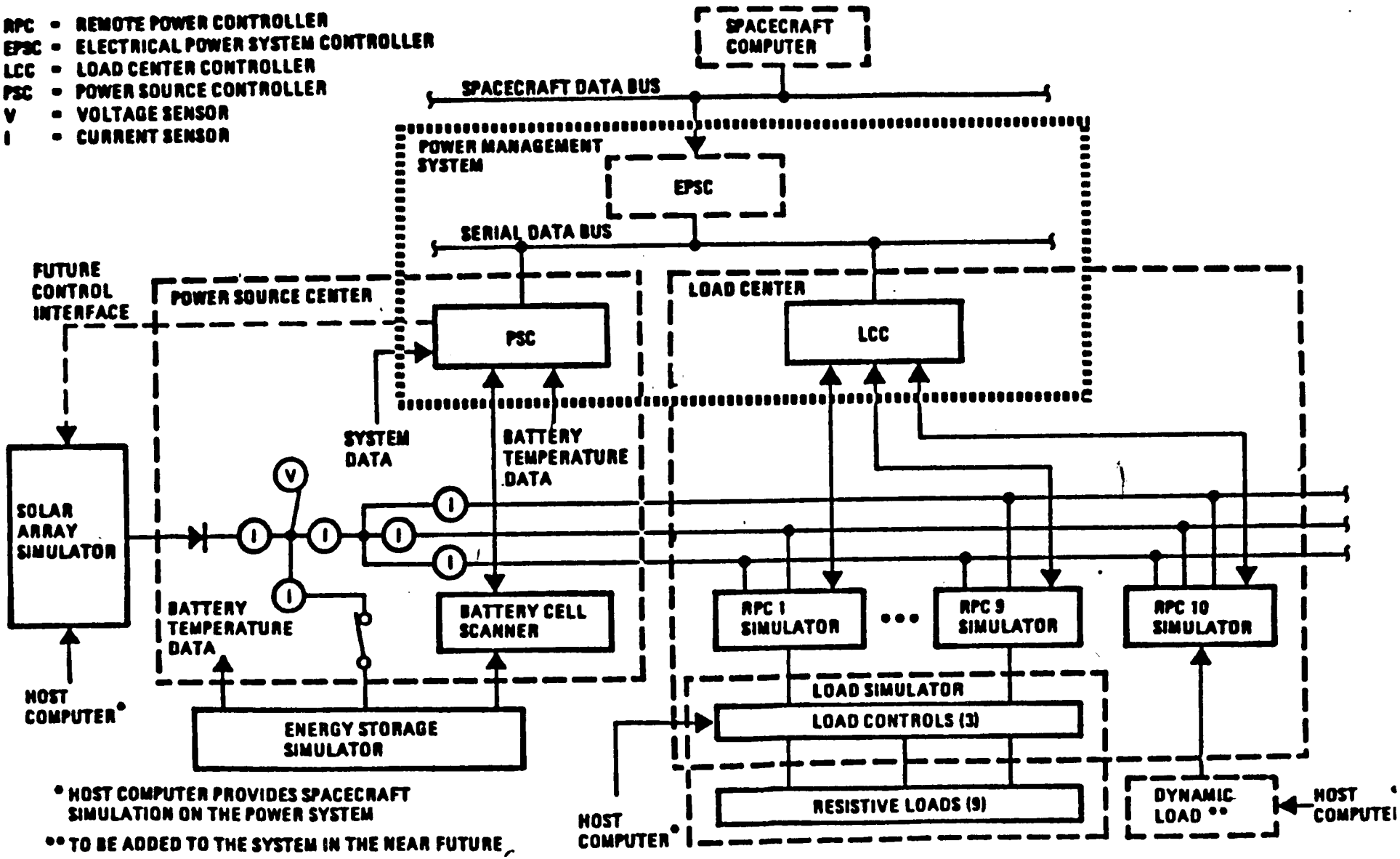


Figure 2 AMPS Hardware and Configuration

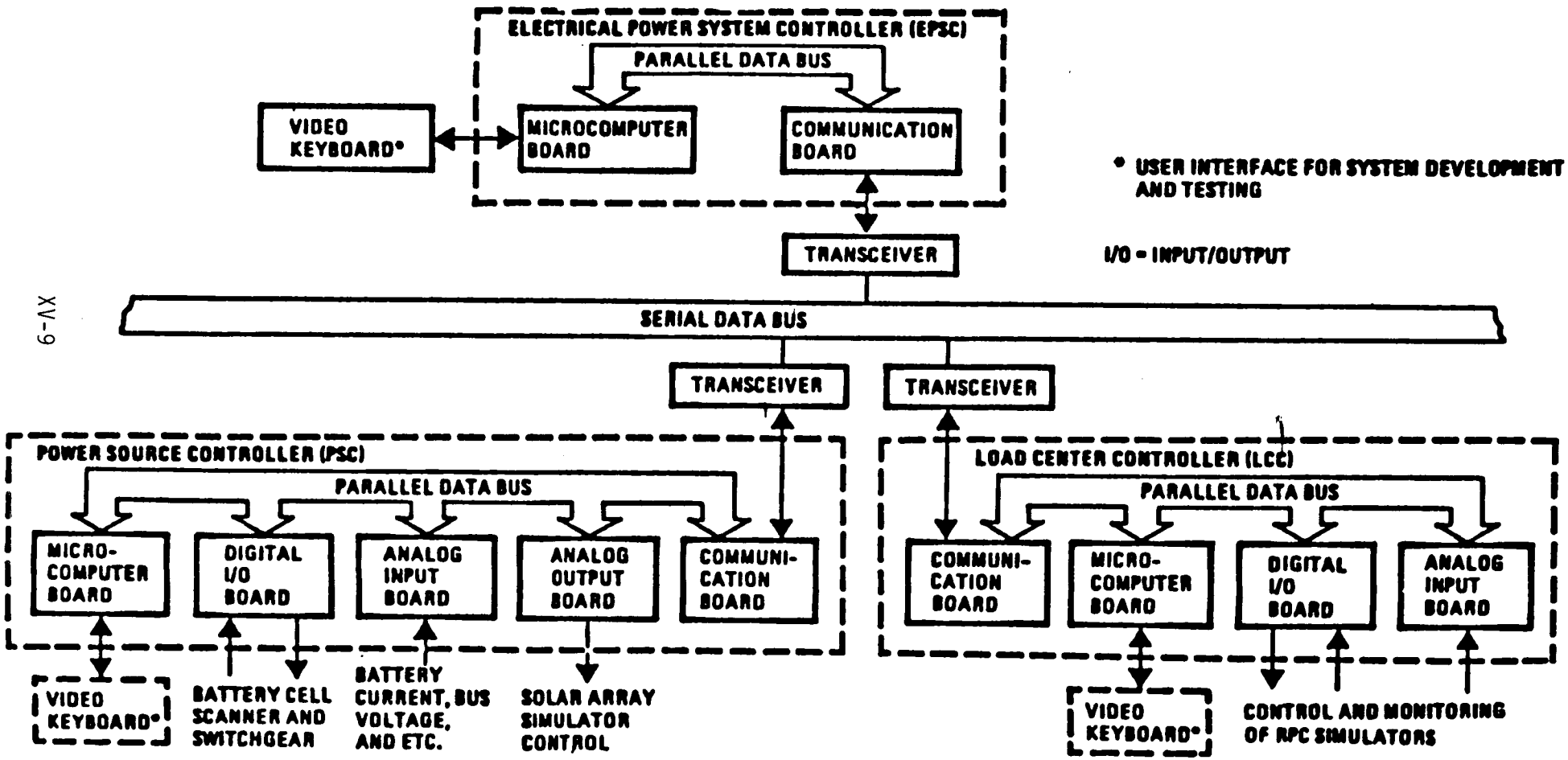


Figure 3 Block Diagram of the Power Management System

transceiver provides the ability to exchange information between the controllers and host computer along the CSMA-CD serial data bus. In the current system all messages are broadcast and each controller determines applicability of messages by decoding.

The microprocessor is a Motorola 68000-R12 12.5 MHz (16/32 bit) MSBC1 processor. The board implements full address range (16 megabytes, 24 bits) and bus arbitration for single and multi-master systems and has been designed for compatibility with existing Multibus products. The board contains 256 Kbytes of dual-port RAM and 32 Kbytes of EPROM along with four serial I/O ports that can be used for interfacing with peripheral equipment.

Ethernet Node Processor

The Ethernet Node Processor communications board is a model ENP-30 manufactured by CMC and is a high performance communications processor[9]. It provides the physical interface and logic necessary for attaching information processing devices to the Ethernet LAN to allow a high speed exchange of information. The ENP30 provides the communication interface between the MSBC1 and the AMPS LAN. Functionally, the ENP30 in the EPSC must process messages that are generated and formatted in the MSBC1 and transmit these messages over the LAN. If a response to the LAN message is required, the ENP30 must process the incoming message from the LAN and deliver it to the MSBC1. Each ENP contains node-specific software, as well as industry standard protocol software for exchanging information throughout the network. The ENP architecture includes an MC68000 microprocessor unit (MPU), a local area network controller for Ethernet (LANCE), a 128 Kbyte dual-access DRAM for buffering in-coming and outgoing messages and application software, a 32 Kbyte EPROM for protocol processing and debug code, and a bus interface circuity for connection to a host information processing system. The MPU responsibilities include moving commands and data to and from system memory, responding to and generating system bus interrupts, executing, upper layers of the selected protocol, and running the communications firmware, the K1 Kernel [10]. The ENP30 communicates with the other PSC components through the IEEE-796 backplane. Communications to the Ethernet data bus is accomplished through a serial interface adapter (SIA) which performs encoding/decoding necessary for interfacing the LANCE to Ethernet. Features of the ENP-30 include:

- 10 MHz MC 68000 MPU
- 128k or 512 byte dual-access DRAM with parity and no wait states
- Up to 64 k bytes EPROM (2 sockets)
- MULTIBUS (IEEE 796) A24:D16 master and slave interface for Host to ENP communications
- Node address PROM contains a world-wide unique address issued by Xerox Corporation.
- A programmable interrupt for protocol software timing.
- Local Area Network Controller for Ethernet (LANCE)

- Buffer management structures in shared local RAM
- DMA to shared local RAM
- Line access protocol (CSMA/CD)
- Extensive diagnostics and error reporting

- Serial Interface Adaptor (SIA)
  -Manchester encoding/decoding
  -Transceiver cable interface
- Dual RS-232 Asynchronous Serial Communication Ports (DUART)
- MULTIBUS interrupt (NBVI)
- MULTIBUS to onboard processor interrupts

The software for each of the controllers resides in the MSBC1 and the ENP 3Ø boards and was developed in FORTH. Figure 4 provides a reprentative controller block diagram (in this case for the EPSC). The FORTH software required for system operation was burned into EPROM and resides on the MSBC1 board. The ENP3Ø and the MSBC1 boards execute concurrently and asynschronously. These two processor boards communicate to each other by placing command, addresses, data, etc. into a shared memory area called the global data area. This global data area is physically located on the MSBC1 board and is accessed by the ENP3Ø through the Multibus using TCP/IP protocols.

ENP3Ø Software Description

The major software elements in the ENP3Ø are shown in Figure 5. The K1 Kernel software operates the local area network controller for Ethernet (LANCE) and performs the Ethernet protocols. As such, the Kernel and the LANCE provide the communications capability between the network's physical medium (the coaxial cable) and the ENP3Ø board. The remaining software in Figure 5 establishes the communications between the ENP3Ø and the MSBC1 and is referred to henceforth, as the applications protocol software. The applications protocol software (APS) which is available on the ENP-3Ø boards of the three PMS controllers is written in FORTH and performs TCP/IP protocols.The ENP-3Ø software performs the following functions: (1) manage received messages from the Kernel to the processor board (MSBC1). (2) Manage transmitted messages from the MSBC1 to the Kernel. (3) Manage MSBC1 network status request commands to the Kernel. (4) Manage the ENP-3Ø activity counter which allows the MSBC1 to determine if the ENP-3Ø software is executing.

The Kernel was supplied by the manufacturer and resides in firmware on the ENP3Ø board in MC68ØØØ assembler code. The operation of the Kernel is to provide the function for interfacing the network media to the user application (ie., ENP3Ø software). The ENP Kernel is responsible for initializing LANCE and the application programs during startup. During ongoing operations the Kernel handles all communications between LANCE chips and the higher level ENP applications.

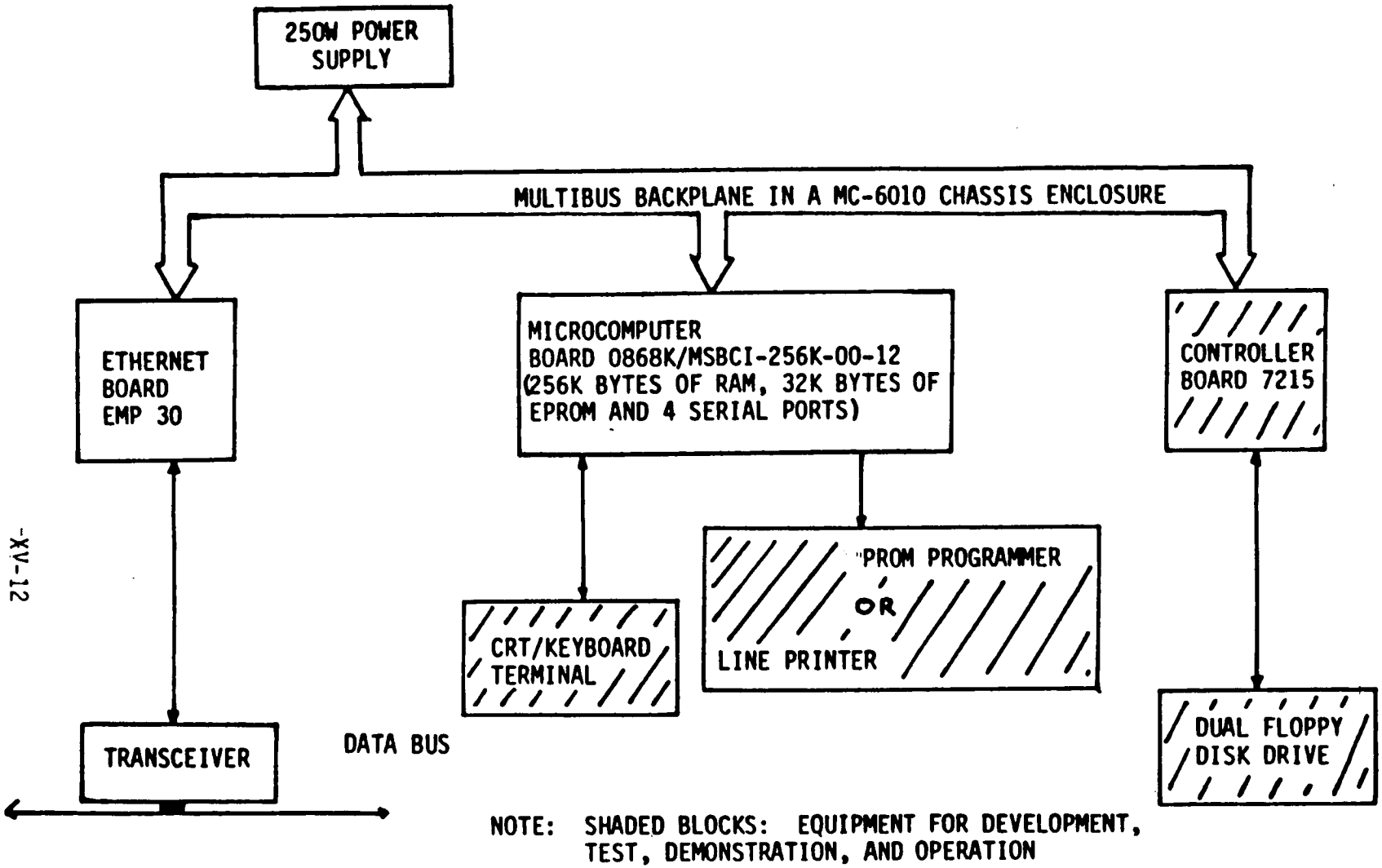


Figure 4 Electrical Power Subsystem Controller Block Diagram

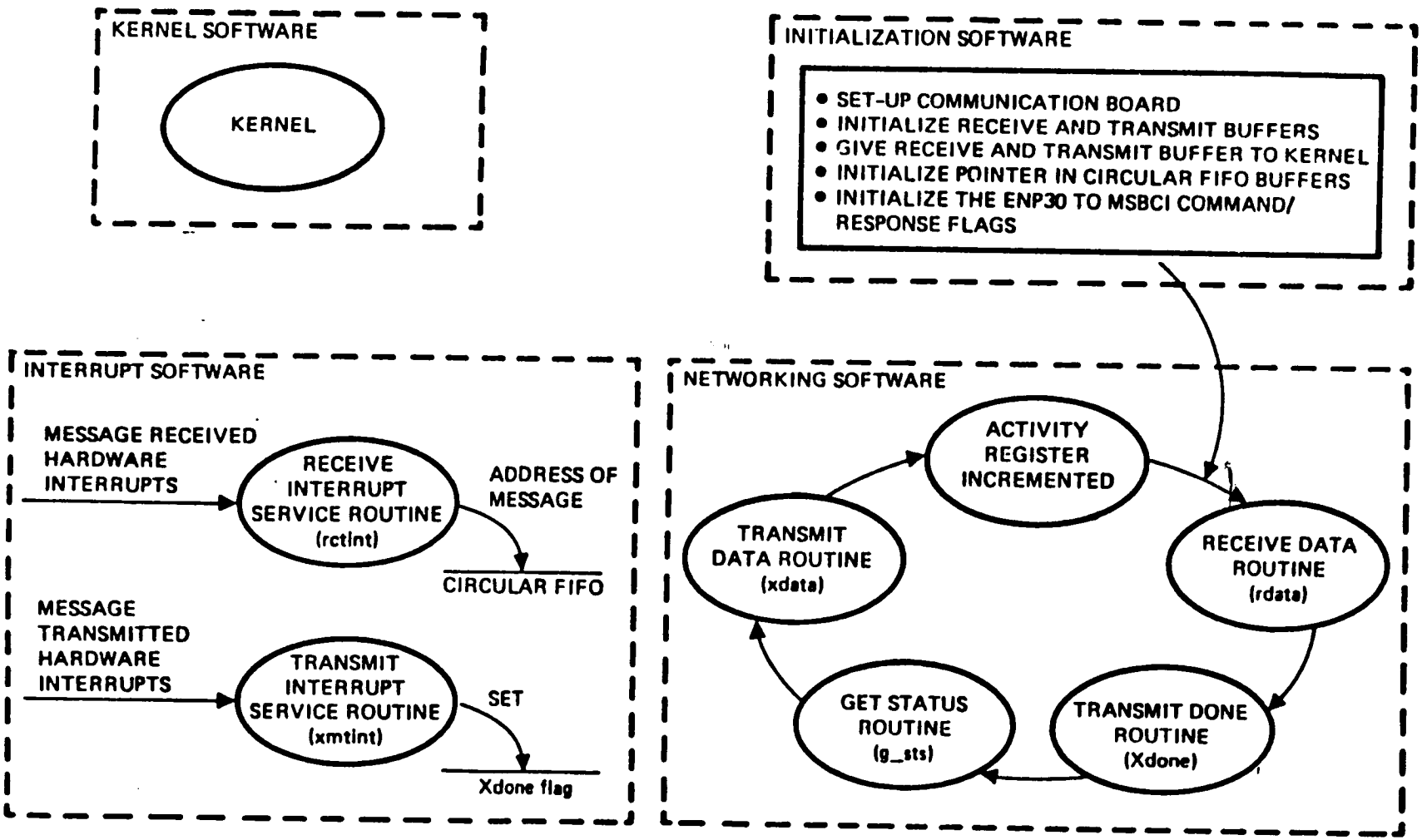


Figure 5 ENP30 Software

Networking the NCR Tower Host Computer

In order to connect the NCR Tower host to the network an ENP-30 communications board was procured from CMC and installed. The Tower ENP-30, like those in the PMS controllers, has the assembler language K1 Kernel software resident in ROM. Consequently, the Tower ENP-30 can be Ethernetted to the AMPSW microprocessor. However, addressing incompatabilities must be overcome and additional software must be generated in order to use the Tower operating system as a host system. As can be seen from Figure 6 the Tower operating system uses 16 bit addressing while the LAN, ENP-30 boards and AMPS microprocessors use switchable 20/24 bit addressing. To overcome this problem software (NET.C) was developed to extend the Tower operating system with a 20/24 bit addressing environment. The software interrupts the suffix and prefix functions thus allowing the Tower to transmit and receive 20/24 bit data to and from the ENP-30. To allow the Tower to serve as the host computer for AMPS its ENP-30 must also mirror the TCP/IP APS protocol software. This capability must therefore be provided by developing the necessary software in RAM on the Tower ENP-30. This involves converting the TCP/IP software which was developed in FORTH by TRW into C for compatibility with the Tower environment. All necessary documentation has been obtained and these efforts have been initiated. Upon completion of these efforts a thorough test and debug effort will be conducted.

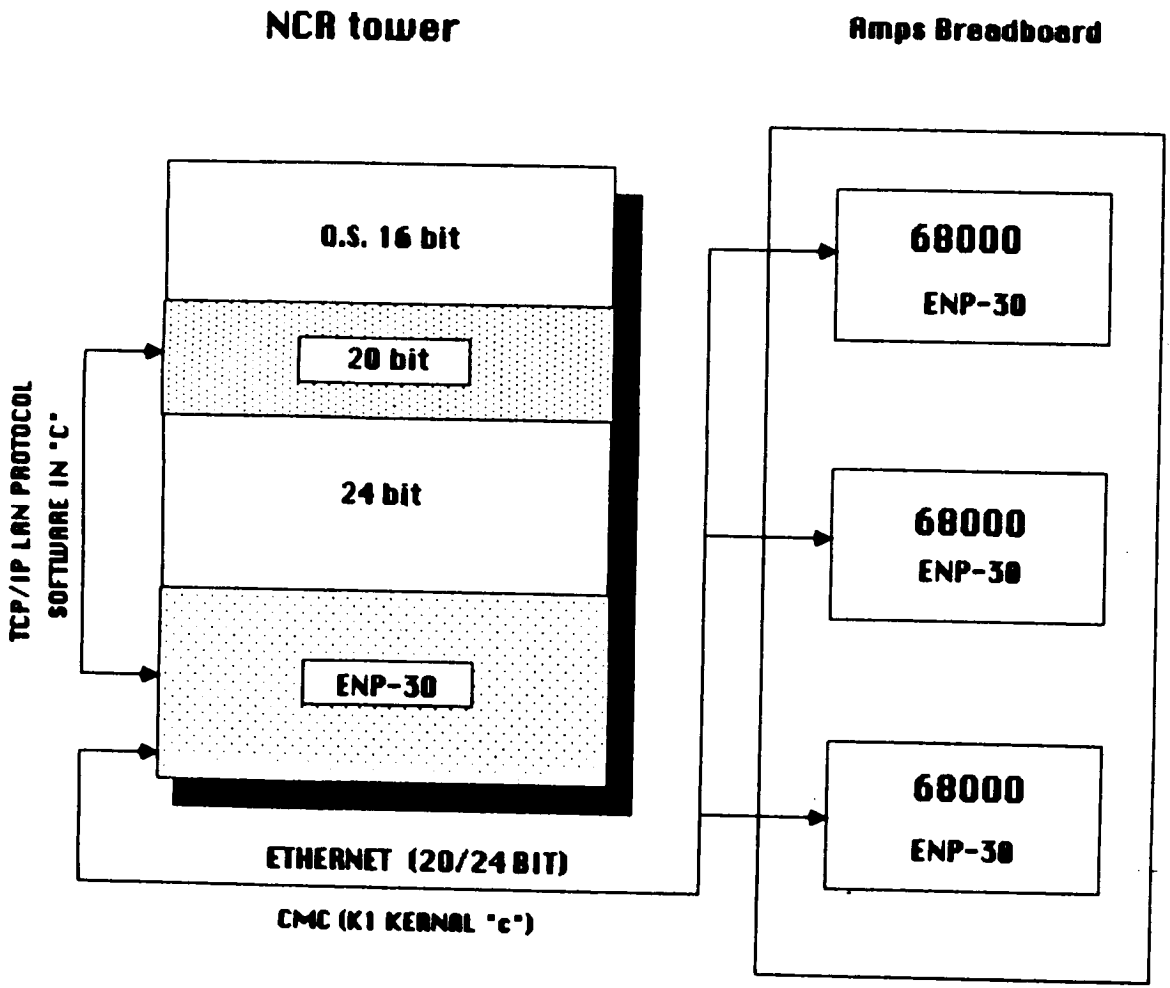


Figure 6 - NCR TOWER Reconfiguration

CONCLUSIONS AND RECOMMENDATIONS

Knowledge-based expert systems will play a major role in autonomous power systems for future space missions. Electrical power system breadboard and testbeds, in turn, will play a major role in the timely development of such systems. The ability to conduct knowledge engineering, validate reasoning mechanisms and update and expand knowledge bases requires the existance of realistic breadboards and testbeds. It will be necessary, therefore, for the various NASA agencies involved in these efforts to assure that the development of such realistic facilities is given prime consideration.

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