MODEM FOR THE LAND MOBILE SATELLITE CHANNEL

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ABSTRACT

This paper describes a modem which has been developed and implemented using a digital signal processor (DSP) for a land mobile satellite demonstration system. The requirements of this digital modem were determined by the characteristics of the land mobile satellite channel. This paper discusses the algorithms which implement the DPSK demodulator. Included is an algorithm which estimates symbol timing independent of carrier phase without the use of a square-law nonlinearity.

INTRODUCTION

The land mobile satellite demonstration system and experimental propagation results are discussed in [1] and [2]. This paper discusses the modem developed for this system. Data communications using small, low-gain antennas on the land mobile satellite channel presents new and interesting challenges to the digital modem designer. Operation with a marginal carrier-to-noise ratio requires that processing techniques achieve the highest possible efficiency. Frequency offsets due to Doppler and oscillator drift are significantly larger than the symbol rate and must be tracked to minimize detection losses. On the forward link, maintaining synchronization in the harsh shadowing and mutipath fading land mobile satellite environment is critical. Consideration of all these factors is necessary in the context of the signal processor real-time throughput constraints.

The modulation selected for the land mobile satellite demonstration system is differentially coherent phase-shift keying (DPSK) at a 200-bit per second data rate with no forward error correction. DPSK modulation provides a compromise among power efficiency, tolerance to shadowing and multipath fading, fast acquisition time, and simplicity. Spectral efficiency is not a consideration for this low data rate system.

Power efficiency was a major consideration since a low-gain, omnidirectional antenna is a requirement. An omnidirectional antenna will not effectively discriminate between direct-path signal energy and reflected signal energy. With Doppler shift, these multipath signals can cause random variations in the signal amplitude and phase. The concern for the land mobile satellite channel is that the multipath fading characteristic may be too severe to allow effective maintenance of the carrier phase estimate for coherent demodulation. Since DPSK only requires an estimate of the carrier frequency, its performance is less sensitive to phase errors caused by the multipath fading enviroment. In addition, an automatic frequency control (AFC) loop has a wider pull-in frequency range and will achieve lock faster than a conventional Costas loop. Coherent PSK is more power efficient in a nonfading channel; however, this advantage diminishes rapidly as phase errors are introduced by multipath fading.

Optimum filtering of the received signal prior to differential detection is necessary to maximize power efficiency. In this modem design, the quantized signal is filtered by an integrate-and-dump operation after the carrier frequency ambiguity has been narrowed by an FFT-based coarse frequency algorithm. An integrate-and-dump approaches a matched filter

when the internally generated reference is in-phase with the received waveform. The integrators must be dumped at the end of each symbol interval to reduce intersymbol interference [3].

In the demodulator, a digital data transition tracking loop estimates symbol timing independent of carrier phase. The symbol timing estimator adjusts the integration window to align the integrate and dumps with received data symbol boundries prior to AFC loop lock. Once the dump clock is synchronized, intersymbol interference is minimized and the AFC loop acheives lock. The signal loss due to small post-FFT frequency errors, when integrating over the symbol interval, is small and can be expressed by [4]:

$$\text{Signal Loss (dB)} = 20 \text{ Log } (1/T\Delta L\pi * \sin(T\Delta L\pi)) \quad (1)$$

where T = symbol period
ΔL = frequency error

Differential detection and AFC loop updates subsequent to the integrate and dump filters are performed at the data rate. Decimation from the 6K Hz input sampling rate to the data rate is provided by the synchronized dump clock and greatly decreases the real-time processing load on the signal processor.

The purpose of this paper is to give a brief description of the digital signal processor used to implement the modem functions and to summarize the demodulator algorithms.

SIGNAL PROCESSOR

The DSP employed to implement the modem functions is a Texas Instruments TMS32020. The TMS32020, analog-to-digital converter, digital-to-analog converter, and programmable sampling clock are all implemented on a board manufactured by Atlanta Signal Processors (ASP) and contained in a Compaq PC. The ASP board also provides an interface between the TMS32020 and the Compaq via dual port RAM.

All of the algorithms which implement the modem functions are performed by one TMS32020. Implementation of these algorithms in software allows a very flexible architecture which can be optimized to changing design requirements. No high-level language was available for the TMS32020 at the project start, so all of the software modules are written in assembly language. Real-time context switching and scheduling is provided by a TMS32020 executive also developed for this modem application.

Computation on the quantized samples is based on a fixed-point, 2's complement representation. Since the TMS32020 provides a 16-bit architecture, the 12-bit samples from the analog-to-digital converter are processed in Q15 format. This means the most significant bit is a sign bit and the decimal point is to the left of the 15 least significant bits. Additional resolution is required by the FFT-based coarse frequency algorithm after squaring the FFT result to obtain the power spectral density. The power spectral density result is processed in Q31 double precision format.

DPSK MODEM

Figure 1 shows a functional block diagram of the DPSK demodulator. The DPSK differential encoding function is performed at baseband in the TMS32020; however, modulation, frequency translation, and filtering required prior to transmission are performed in hardware.

NUMERICALLY CONTROLLED OSCILLATOR

The primary computational element of the numerically controlled oscillator (NCO) is an accumulator. The size of the accumulator, the sampling rate, and the magnitude of the instantaneous phase added to the accumulator determine the rate at which the accumulator rolls over and thus the frequency output from the NCO. The least significant 6 bits of the accumulator

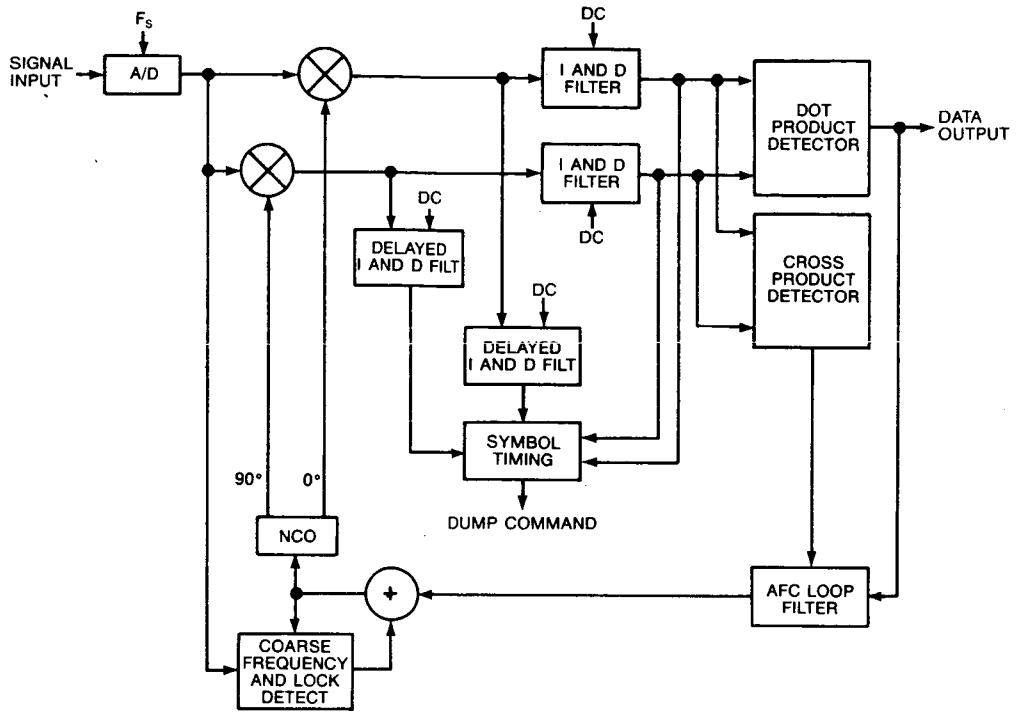

Fig. 1. Block diagram of DPSK demodulator

address fine look-up locations and the next most significant 6 bits address coarse look-up for sine and cosine. The actual quadrant of the accumulated phase is represented by the most significant 2 bits of the 14 bit accumulator.

The NCO uses the addition trigonometric identities;

$$\cos(A+B) = \cos A\cos B - \sin A\sin B \quad \text{and}$$

$$\sin(A+B) = \sin A\cos B + \cos A\sin B$$

to minimize the number of table look-up locations required to generate sine functions and cosine functions. The look-up table contains 64 locations for each of the following functions: coarse sine (sinA) and cosine (cosA), and fine sine (sinB) and cosine (cosB). The quantized look-up angles are represented in the first quadrant as:

A: coarse = $0 \rightarrow \pi/2$
B: fine = $0 \rightarrow \pi/128$

INTEGRATE AND DUMP FILTERS

The I and Q signals generated by multiplying the digitized signal with the NCO outputs are filtered by integrate-and-dump filters. In order to avoid intersymbol interference, the integrators (accumulators) must be reset (dumped) at the end of each symbol interval. A symbol timing algorithm samples both the I and Q channels to deliver a symbol timing error which is used to drive a first-order digital data transition tracking loop. When the error is driven to zero, the integrators are reset at the end of each symbol interval and the time-varying integrate and dump filters are synchronized to the received data symbols.

SYMBOL TIMING ALGORITHM

The symbol timing algorithm determines the reset time of the integrate-and-dump filters and thus symbol synchronization. Figure 2 shows a functional block diagram of the symbol timing algorithm. The error signal for symbol timing is based on the observation that when a non-return to zero (NRZ) data transition occurs, the integral (ignoring the effects of inter-symbol interference (ISI) and channel noise) from one-half symbol before the transition to one-half symbol after the transition should be zero. This is also true for the integral of a sinusoidal signal that experiences a 180 degree phase shift.

A transition detector determines whether a transition has occurred, and, if so, calculates the direction of the transition. This information, along with delayed integrator outputs, is input to a data transition discriminator which calculates the symbol timing error [5].

$$E_n = [I_n - I_{n-1}]^*(I_{n-1/2}) + [Q_n - Q_{n-1}]^*(Q_{n-1/2}) \tag{2}$$

This error signal is used to drive a first-order digital data transition tracking loop. The loop filter equation can be represented as:

$$\tau_{n+1} = \tau_n + E_n \tag{3}$$

A variable loop gain allows fast symbol synchronization during acquisition while providing for a narrow loop bandwidth during tracking. This algorithm derives a symbol timing error independent of carrier phase without the use of a square-law nonlinearity.

DOT AND CROSS-PRODUCT DETECTORS

A dot-product detector estimates the value of the data bit by differential detection of the I and Q integrate and dump outputs. The dot-product detector is implemented by multiplying the I signal delayed by one symbol (one sample at the decimated rate) with the I signal. This result is added to the product of the Q signal delayed by one symbol multiplied by the Q signal. The sign of the dot-product result is the NRZ detected data bit.

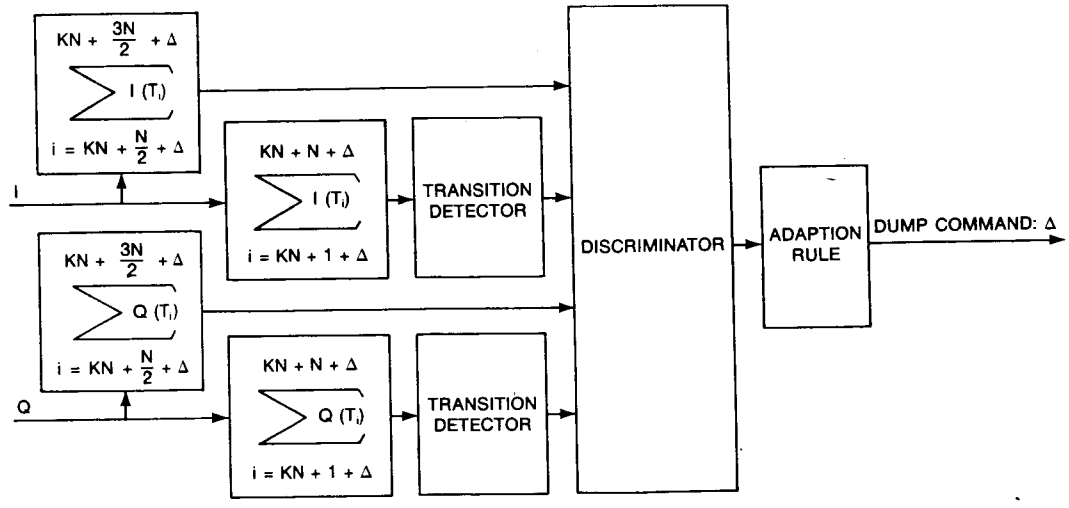

Fig. 2. Digital data transition tracking loop block diagram

A cross-product detector multiplies the I signal by the Q signal delayed by one symbol. This result is subtracted from the product of the Q signal multiplied by the I signal delayed by one symbol. The cross-product detector result is an estimate of the difference between the frequency of the received signal and the NCO output. The sign of this frequency estimate is a function of the received data phase. Dependency on the data phase is eliminated by multiplying the cross-product estimate of the NCO frequency offset by the NRZ detected data bit. The result is an error term that is proportional to the NCO frequency offset and is represented by the noise-free discriminator characteristic shown in Figure 3 [6].

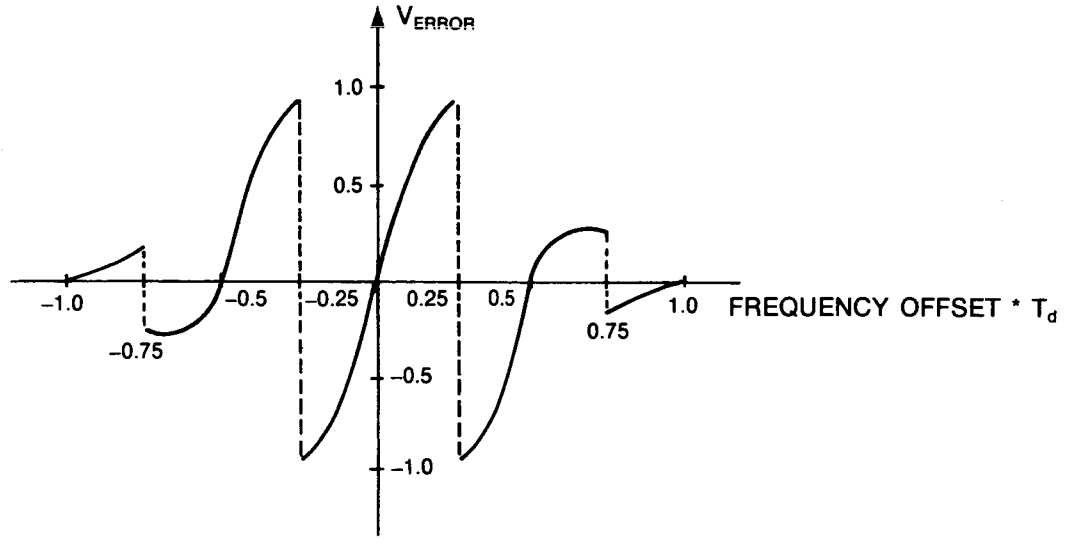

Fig. 3. Noise-free discriminator characteristic Td = $\frac{1}{\text{data frequency}}$

AUTOMATIC FREQUENCY CONTROL LOOP FILTER

The cross-product detector error estimate is filtered by a lead-lag recursive filter and fed back to the NCO. The transfer function for the one-pole filter in the S domain is:

$$F(s) = K_L(1 + a/s) \tag{4}$$

Using the bilinear transform to convert to the z domain, the difference algorithm may be written:

$$u_n = u_{n-1} + (K_L a T_d/2)e_{n-1} + K_L(1+aT_d/2)e_n \tag{5}$$

The AFC loop filter determines the dynamic performance of the AFC loop. The gain and bandwidth of the AFC loop are specified by the filter coefficients K_L and a (as in equations (4) and (5)) [7].

COARSE FREQUENCY ESTIMATE AND LOCK DETECT

The cross-product detector characteristic given in Figure 3 shows the pull-in range of the AFC loop to be less than 50 Hz with a 200-Hz data rate. An algorithm that employs an FFT estimates the frequency of the received signal at the input to the digital demodulator.

Loss of AFC loop lock is determined by comparing the coarse frequency estimate to the frequency output of the NCO. If their difference exceeds the cross-product detector pull-in range for a specified number of trials, this coarse frequency estimate is added to the AFC filter output (fine frequency) and the sum determines the NCO frequency output.

CONCLUSION

Tests of the DPSK modem are continuing as the land mobile satellite demonstration results are reviewed. Initial tests on the demodulator were performed to approximate its stability and performance. These tests indicate an implementation loss of about 1 dB with digitally generated, white Gaussian noise added to the received signal.

The symbol timing and AFC loops have shown a high resistance to the effects of shadowing and multipath fading. On a trip from Waterloo, Iowa, to Cedar Rapids, Iowa, during two-way communication via the INMARSAT satellite, the AFC loop of the land mobile satellite system remained locked despite the most harsh shadowing conditions. Although this demodulator is optimized for fast carrier acquisition, its performance appears to be very robust once synchronization is achieved.

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