NASA CONTRACTOR REPORT 177 446

Development of 30 μm Extrinsic Silicon Multiplexed Infrared Detector Array
Final Report

G. Orias
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Development of 30 μm Extrinsic Silicon Multiplexed Infrared Detector Array
Final Report

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A Subsidiary of Hughes Aircraft Company
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Prepared for
Ames Research Center
under Contract NAS2-12110

National Aeronautics and
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ABSTRACT

This report describes the results of the contract development effort performed in the design and fabrication of two (2) each 58 × 62 antimony doped silicon hybrid detector arrays for NASA-Ames Research Center, Moffett Field California. This work was performed under NASA Contract No. NAS2-12110 at Santa Barbara Research Center, Goleta, California. The report contains a brief description of the detector development, test equipment, tests performed and summary of results obtained.

PREFACE

This report describes the development effort performed by the Santa Barbara Research Center , Santa Barbara, California and the Industrial Electronics Group Technology Center of Hughes Aircraft Company. This development covers the unique work necessary to complete two (2) each antimony doped silicon (Si:Sb) hybrid detector arrays for the NASA-Ames Research Center, Moffett Field, California. The primary effort centered upon the fabrication of 58 × 62 two dimensional detector arrays of Si:Sb infrared detector material and the testing required once mounted or hybridized to the Hughes Aircraft CRC-228 detector readout multiplexing assembly. The detector performance of Si:Sb as applied to discrete element detectors is well understood and has been demonstrated in a number of flight hardware programs. The detectors, as previously used in discrete element focal plane arrays, were significantly larger and typically few in any one array or application. In this development the detector unit cell size is slightly less than 0.003 in. square. These detectors are fabricated as a 3596 element array which after completion are then connected and mounted (hybridized) to the above readout chip. In this application a new and unique use of this infrared material is approached in order that its performance may be measured and evaluated as to its ability to meet the needs of future space infrared astronomy projects.

The work was performed at Santa Barbara Research Center and the Industrial Electronics Group of Hughes Aircraft at Carlsbad, California over the period of March 1985 through June 1986. The program manager was D. Campbell. Many other persons at SBRC and IEGTC made significant contributions and they are: Ken Razor who headed up the IEGTC phase of the project,

Steve Gaalema who advised and assisted with the test effort at IEGTC. Dick Nielson was responsible for the backup and more successful detector development at SBRC. Jim Myrosznyk who fabricated the SBRC detectors, Jim Fulton who handled the cryogenic phase of chip and dewar setups and Geoff Orias who performed the lions share of all the testing of the arrays and is the primary author of the technical content of this report.

1.0 INTRODUCTION and TECHNOLOGY REVIEW

The objective of the development effort presented herein is twofold: The first objective is to produce and demonstrate a two dimensional detector array of antimony doped silicon. This array would be made up of detectors of approximate pixel size which could be used in applications such as the Space Infrared Telescope Facility (SIRTF). The second is to investigate the performance of Direct Readouts (DRO), with multiplexing capability as used in conjunction with cold detectors of extrinsic silicon doped for observation in the ~20 to 30 μm infrared band. The detector material chosen for this area of development was antimony doped silicon selected from a boule of material grown at the Hughes Malibu Research Laboratories, which had been used successfully on other discrete focal plane programs, of which the overall characteristics were known. The Readouts were selected from existing technology fabrication as developed by the Industrial Electronics Group, Technology Center of Hughes Aircraft at Carlsbad, California. The device selected is referred to as a 228 DRO chip. Although not a state of the art device, in that this particular chip was not specifically engineered for low temperature operation (i.e., less than 10K operation), it was chosen for its overall record of performance and size as a suitable test bed for the development effort to be accomplished. A similar design would or could be employed as the readout multiplexing device for flight hardware. Its design architecture (inter-element aspect ratios), however, would be appropriately engineered to provide superior performance specifically at the low temperatures required.

2.0 PROJECT DEVELOPMENT

The project development was begun with SBRC supplying the detector material to the IEGTC division of Hughes Aircraft with instructions for fabricating a detector array which would be constructed and then hybridized

and tested at the Carlsbad facility. Due to numerous difficulties compounded by uncertainties in test results reported, a backup effort was begun at SBRC in order to insure a maximum opportunity of success. The devices produced at both the Carlsbad Hughes facility and a Santa Barbara Research are presented in this report. Although not covered in depth under the scope of this current contract, additional testing should be performed in order to obtain a better evaluation and comparison of the detectors produced at IEGTC and SBRC. These detectors, although produced from the same detector materials, were fabricated by two unique processes of which the simpler of the two (SBRC's), appears with the limited data taken, to result in quieter performance. (The SBRC method divides implanted sheets into detector elements using a trench etch procedure. The Carlsbad method uses a discrete implantantion scheme combined with an oxide mask.)

3.0 DETECTOR FABRICATION

The antimony doped silicon hybrid FPA's consist of antimony doped silicon arrays and silicon readout integrated circuits (ROIC) with 58 rows and 62 columns for a total of 3596 detectors. Each element is 76 x 76 μm, by 0.5 mm thick. A 2 in. diameter antimony doped (4 E+15 atoms/cc) extrinsic silicon wafer was processed into photoconductive arrays for the NASA-Ames contract. The double sided, polished wafer had degenerate transparent contacts implanted into both sides using phosphorous ions. Sputtered aluminum was deposited on both of the implanted surfaces and then delineated, by means of wet chemical etching, into discrete detector contacts on one side and windows on the opposite side. Trenches were then etched into the silicon by means of reactive ion etching in order to isolate the aluminum contacts from each other. Indium bumps were deposited on the aluminum contacts to provide electrical continuity to the readout chip (see Figure 1). Finally the detector chip was hybridized electrically and mechanically to the direct readout (DRO) multiplexer chip.

4.0 READOUT DESCRIPTION

The silicon readout integrated circuit employed in the Si:Sb hybrid assembly is a CRC-228 DRO switched FET multiplexer developed by the Hughes Industrial Electronics Group Technology Center. This DRO is an n-channel

Si:Sb Detector Array

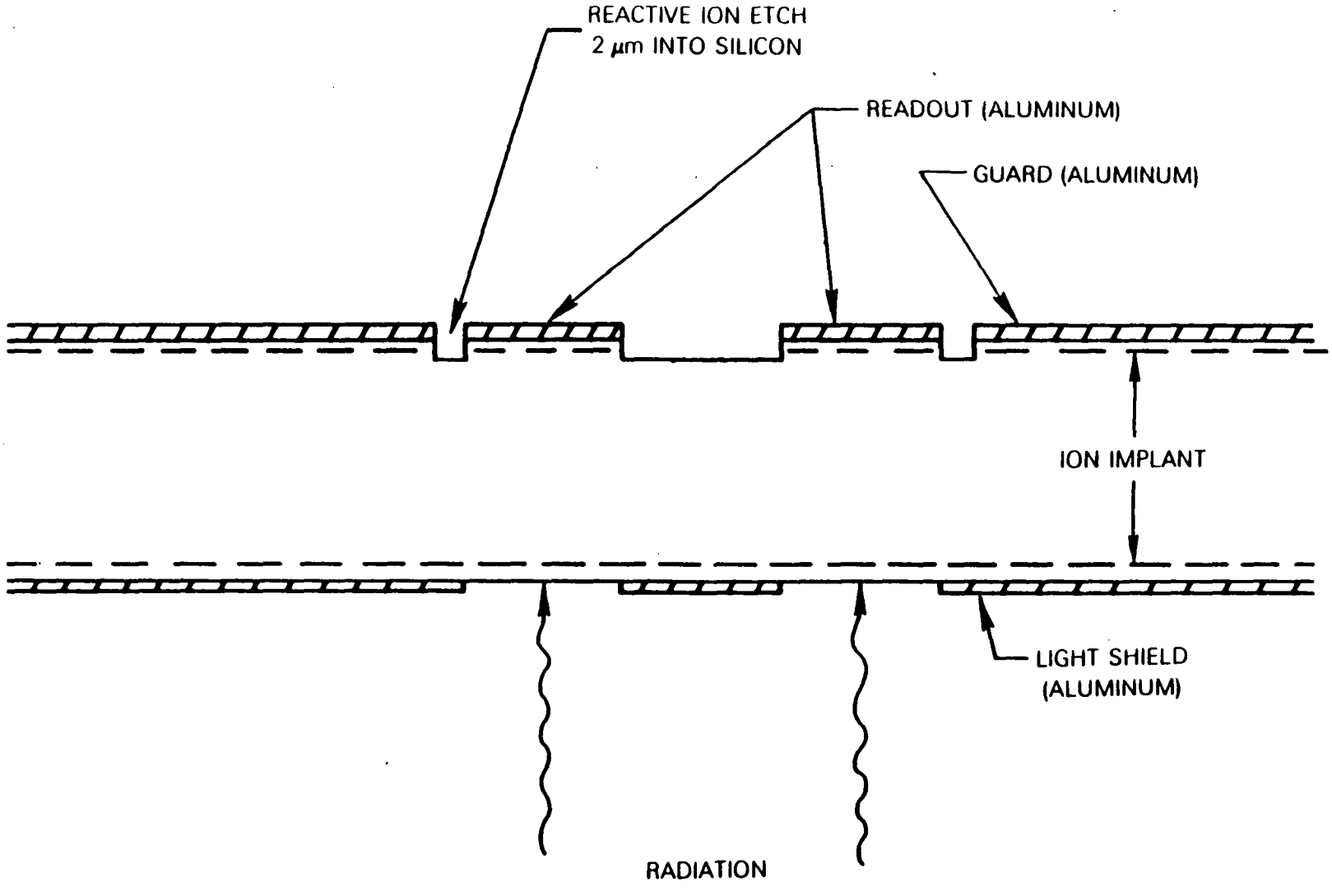


Figure 1

Si:Sb Bonding Diagram

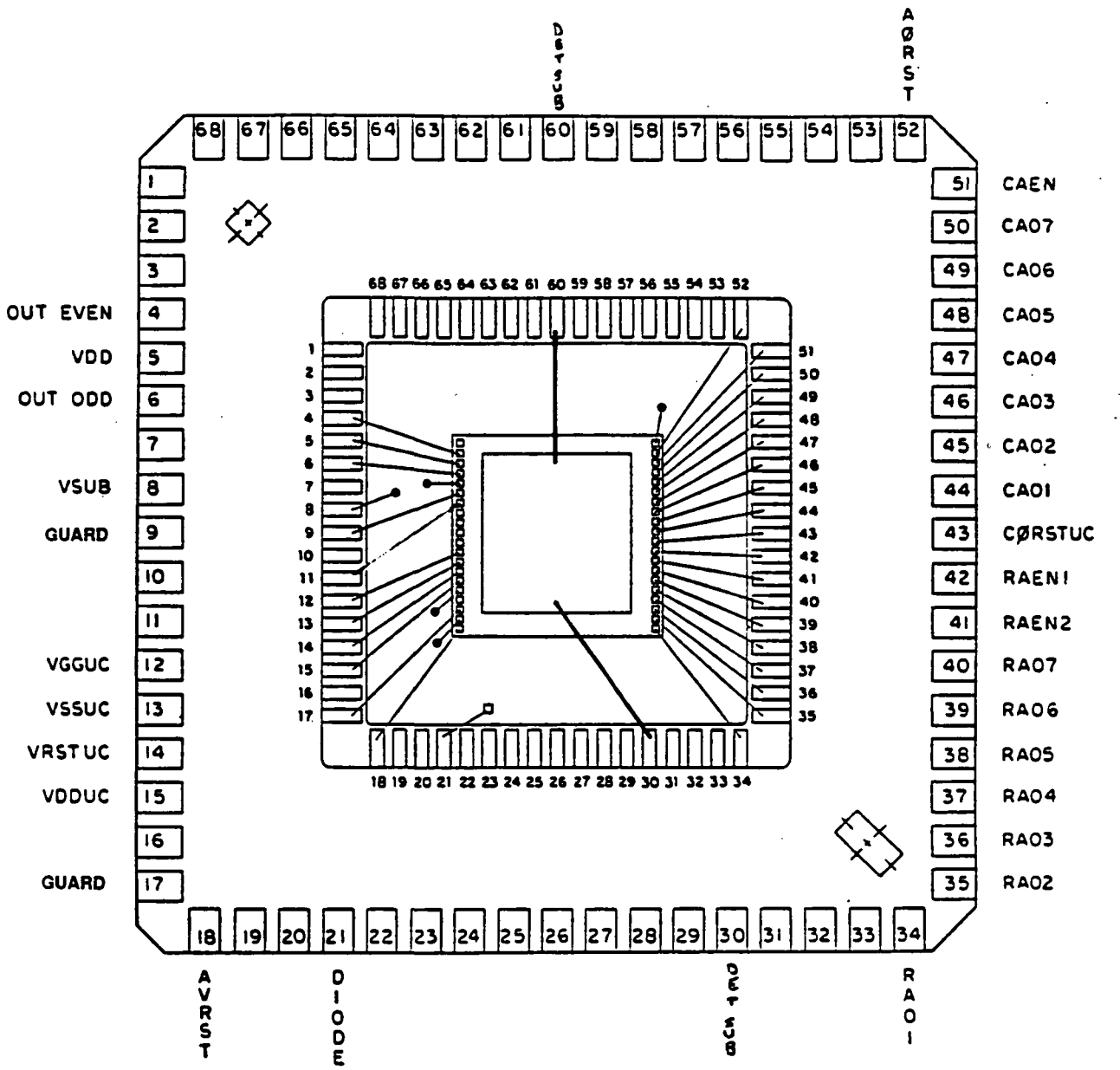


Figure 2

MOSFET switching device with two parallel outputs and is packaged on a 68-pin leadless carrier (see Figure 2). After hybridization, it is expected that the nodal capacitance of the array is 0.1pF. The well capacity has been estimated to be 1.25×10^6 electrons. Unit cell pairs, which can be accessed in any order, are selected by means of an X,Y addressing scheme using row and column address clocks. Each unit cell of the DRO has a reset switch and a source follower for each detector. In addition, there is an output source follower for each of the two outputs to drive the output lines (see Figure 3).

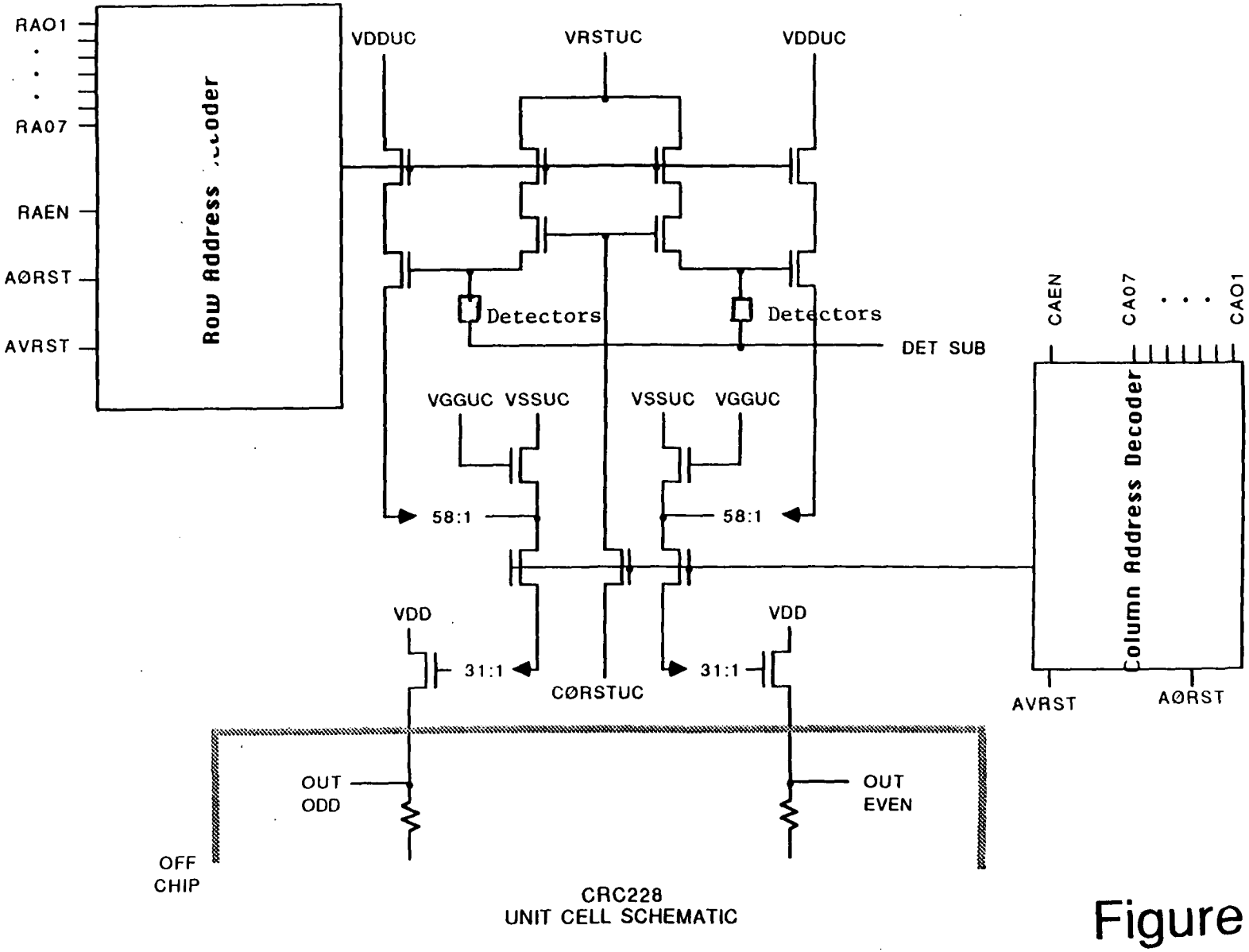
5.0 TEST SET DESCRIPTION

The test set used for data acquisition was the Two Dimensional Focal Plane Array (2DFPA), drive electronics in conjunction with Infrared Focal Plane Array Test Station No. 4 (IFPATS 4). The 2DFPA drive electronics was designed specifically to operate a CRC-228 and is comprised of four main parts: the computer interface electronics (CIE), the dewar interface electronics (DIE), a Macintosh computer, and a buffer amplifier. The CIE is programmed by the Macintosh and generates the timing for the ROIC and provides frame synchronization and data valid signals to IFPATS 4. The DIE has bias and clock drivers that connect directly to the ROIC and also performs analog signal processing of the output signals. The Macintosh computer acts as a control computer and is used for setting integration times, digital to analog converter (DAC), controlled biases, and analog signal processing options. The buffer amplifier has a gain of 50 with offset and is used to buffer the ROIC outputs to the dewar interface electronics. IFPATS 4 includes an 8 MHz, 4 channel, 12-bit analog to digital convertor (ADC), a dedicated HP-1000 computer, a Floating Point Systems AP-120B array processor, a Lexidata visual display monitor, and various video and graphic output devices. Analog data from the dewar interface electronics goes into the ADC in IFPATS 4. Typically 100 frames of data are measured and stored in the array processor and then averaged. Performance parameters are calculated from the averaged data and displayed on the Lexidata display, video terminal, or line printer. The data can be stored on a hard disk for future reference.

6.0 DEWAR CONFIGURATION/DESCRIPTION

The dewar employed is an 8 in. Janis dewar (see Figure 4). The calculated back-ground inside the dewar was reduced to 2.6 E+6 photons/cm^2-sec using a short-

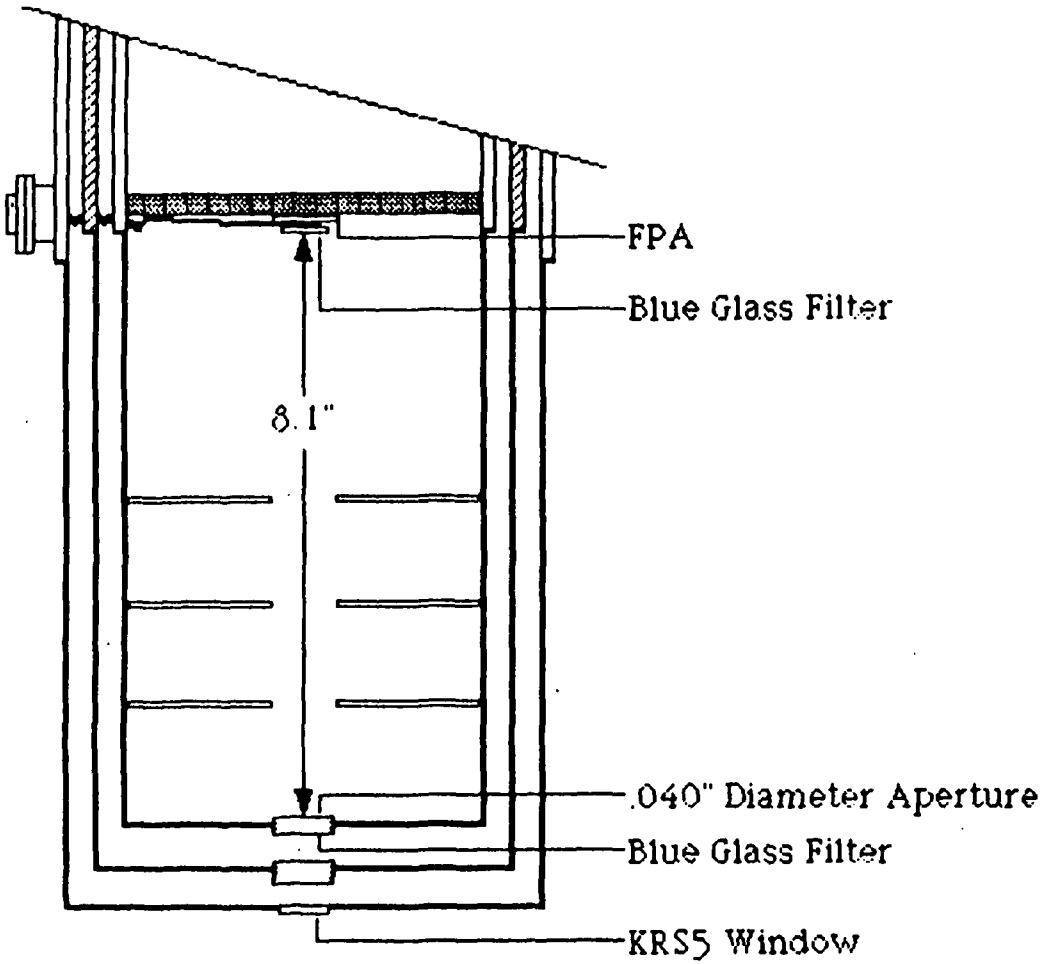
CRC-228 Unit Cell



CRC228
UNIT CELL SCHEMATIC

Figure 3

Si:Sb Test Dewar Setup



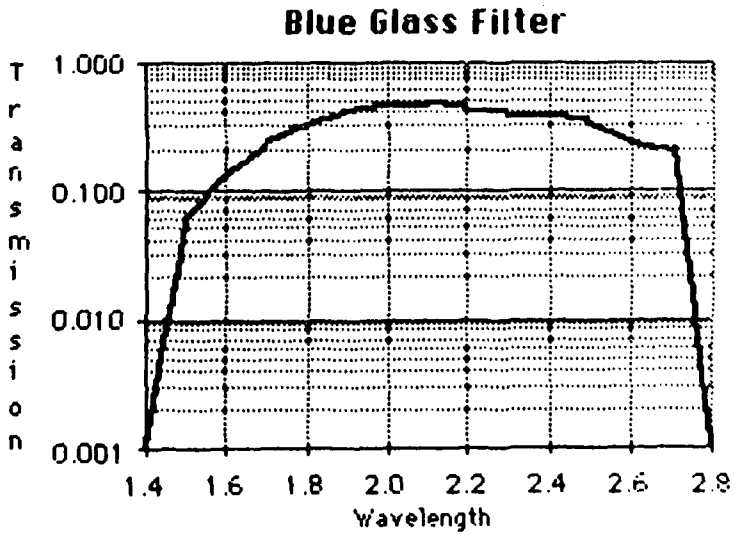


Figure 4

wavelength spectral filter and a pinhole aperture to limit the field of view.

The Janis dewar is evacuated to a pressure of 1 E-6 torr prior to cool-down. The inner jacket is cooled with liquid helium and the outer jacket is cooled with liquid nitrogen. The temperature inside the dewar can be raised with a heater located in the cold stage under the FPA and can be lowered by pumping over the helium reservoir with a vacuum pump. The temperature of the 58 x 62 hybrid array was monitored by means of a thermistor epoxied to the 68-pin leadless carrier (see Figure 2). During our testing we were able to vary the temperature from 3.4 K to 15K. A blackbody calibrated for 800 and 500K was used as an infrared source. When the blackbody shutter is opened the photon flux at the FPA becomes 8.05 E+11 photons/cm^2 sec for an 800 K blackbody and 7.21 E+9 for a 500K blackbody. In watts/cm^2 this corresponds to 1.07 E-7 and 9.54 E-10 respectively. These values were calculated based on the dimensions of the dewar, the spectral bandpass of the filters, and the relative response of the detectors (see Figure 5). A summary of these calculations is given in Table 1 and Table 2. The NEP data in this report has been extrapolated to performance at the peak wavelength. A factor of 100 was used to convert the performance at 2 μm to that at the peak wavelength. This factor may be incorrect because the spectral response for a 0.5 mm thick detector array has not been measured.

7.0 TESTING

A total of four FPA's were tested at Santa Barbara Research Center. Three of the FPA's were manufactured at SBRC (S/N 001, 002, and 003) and the fourth (S/N CB) was manufactured at Carlsbad. In our initial set up a background problem in the dewar quickly became apparent. The FPA was at the correct temperature but was saturating.

The cause for the high background was determined to be heat radiation from the cabling inside the dewar. A second blue glass filter was attached directly to the nano-connectors mounted on the 68-pin leadless carrier and sealed optically with epoxy and Black Velvet paint. This method was successful in reducing the background to the desired level.

S/N 001, the first Si:Sb hybrid made at SBRC, was the initial FPA assembly characterized. Measurements performed on S/N 001 were signal as a function of bias, NEP as a function of bias, and noise as a function of bias. The bias and

Si:Sb Spectral Response

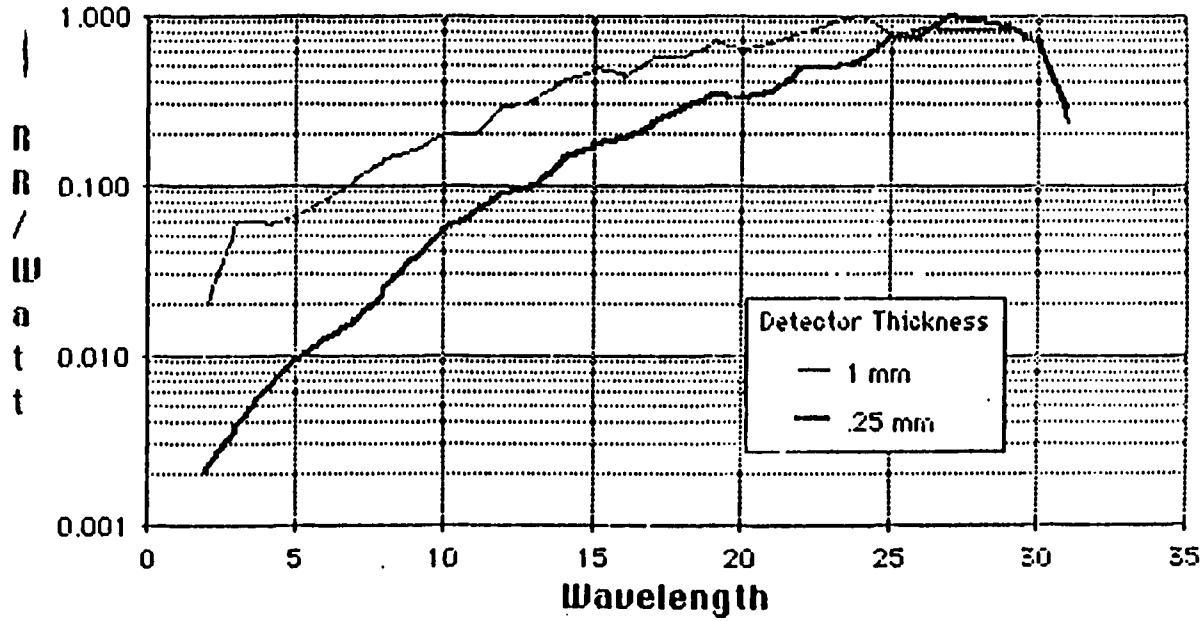


Figure 5

Radiometric Summary Sheet
800 Kelvin

Flux Calculations

	Blackbody Watts	Chopper Watts	Blackbody Photons	Chopper Photons
Total	2.32E+00	4.59E-02	7.79E+19	4.11E+18
Integral	3.21E-01	4.05E-06	4.00E+18	5.73E+13
∫ x Transmission	1.75E-02	5.71E-08	1.98E+17	7.18E+11
∫ x T x Rel. Response	1.75E-02	5.71E-08	1.32E+17	4.31E+11
∫ x T x RR x FOV	1.07E-07	3.48E-13	8.05E+11	2.63E+06

Integral limits are from 1.5 to 3 with intervals of .1 microns.
Blackbody temperature = 800 °K Chopper temperature = 300 °K

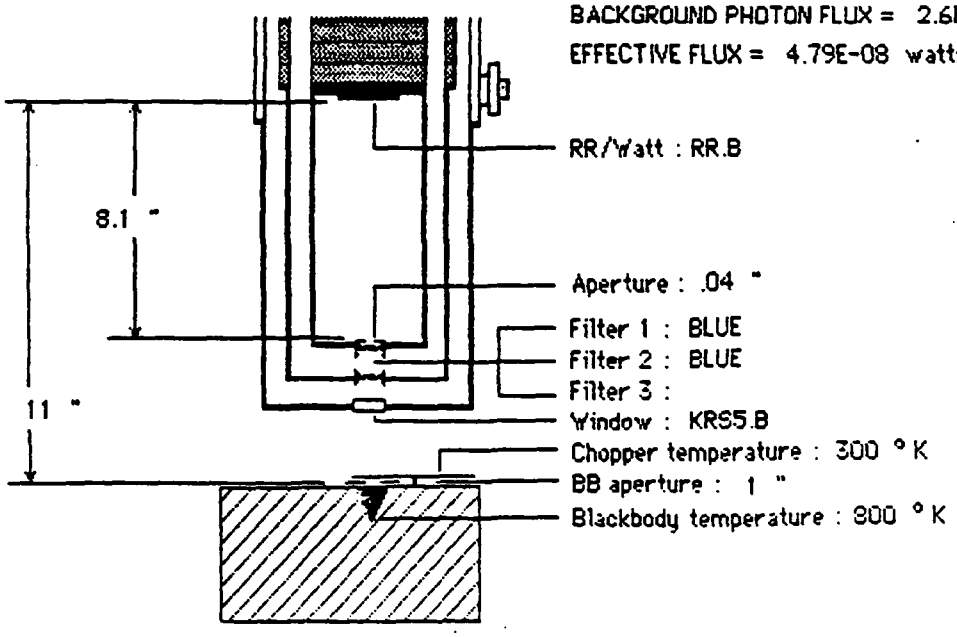
Field of View

	Aperture	Distance	(degrees)	(x factor)
Internal	.04	8.1	5.66E-01	6.10E-06
External	1	11	1.04E+01	2.07E-03

Background and Signal Flux

$$Q_{bk} = \int_{\lambda_1}^{\lambda_2} Q' \times T \times RR \, d\lambda \times \left(\frac{r}{D}\right)^2 = 2.63E+06 \text{ ph/cm}^2\text{/s}$$

$$H_{eff} = \int_{\lambda_1}^{\lambda_2} W \times T \times RR \, d\lambda \Big|_{T_{Ch}}^{T_{BB}} \times \left(\frac{r}{D}\right)^2 \times .45 = 4.79E-08 \text{ watts/cm}^2$$



BACKGROUND PHOTON FLUX = 2.6E+06 ph/cm^2/s
EFFECTIVE FLUX = 4.79E-08 watts/cm^2

Table 1

Radiometric Summary Sheet
500 Kelvin

Flux Calculations

	Blackbody Watts	Chopper Watts	Blackbody Photons	Chopper Photons
Total	3.54E-01	4.59E-02	1.90E+19	4.11E+18
Integral	4.56E-03	4.05E-06	6.13E+16	5.73E+13
∫ x Transmission	1.56E-04	5.71E-08	1.87E+15	7.18E+11
∫ x T x Rel. Response	1.56E-04	5.71E-08	1.18E+15	4.31E+11
∫ x T x RR x FOV	9.54E-10	3.48E-13	7.21E+09	2.63E+06

Integral limits are from 1.5 to 3 with intervals of .1 microns.
Blackbody temperature = 500 ° K Chopper temperature = 300 ° K

Field of View

	Aperture	Distance	(degrees)	(x factor)
Internal	.04	8.1	5.66E-01	6.10E-06
External	1	11	1.04E+01	2.07E-03

Background and Signal Flux

$$Q_{bk} = \int_{\lambda_1}^{\lambda_2} Q^{\lambda} \times T \times RR \, d\lambda \times \left(\frac{r}{D}\right)^2 = 2.63E+06 \text{ ph/cm}^2\text{/s}$$

$$H_{eff} = \int_{\lambda_1}^{\lambda_2} W \times T \times RR \, d\lambda \Big|_{T_{Ch}}^{T_{BB}} \times \left(\frac{r}{D}\right)^2 \times .45 = 4.29E-10 \text{ watts/cm}^2$$

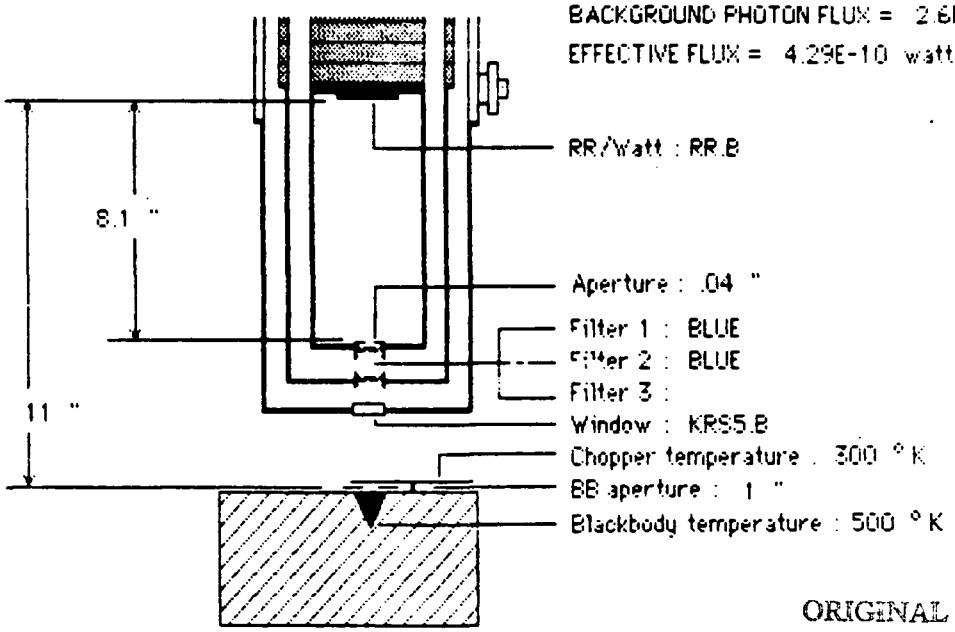


Table 2

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Si:Sb 001 Signal in Volts

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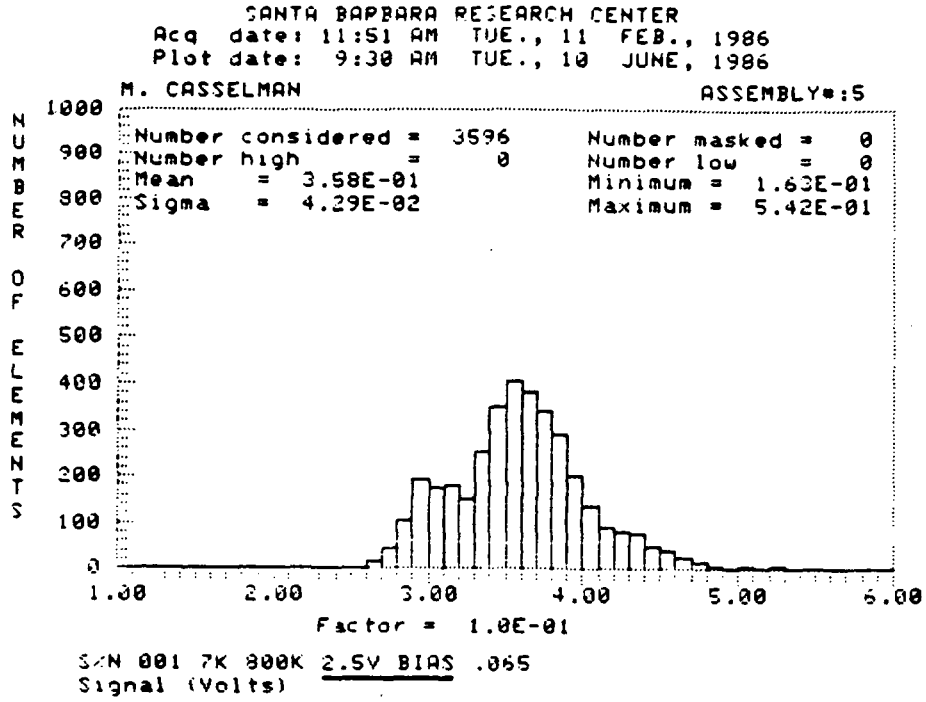


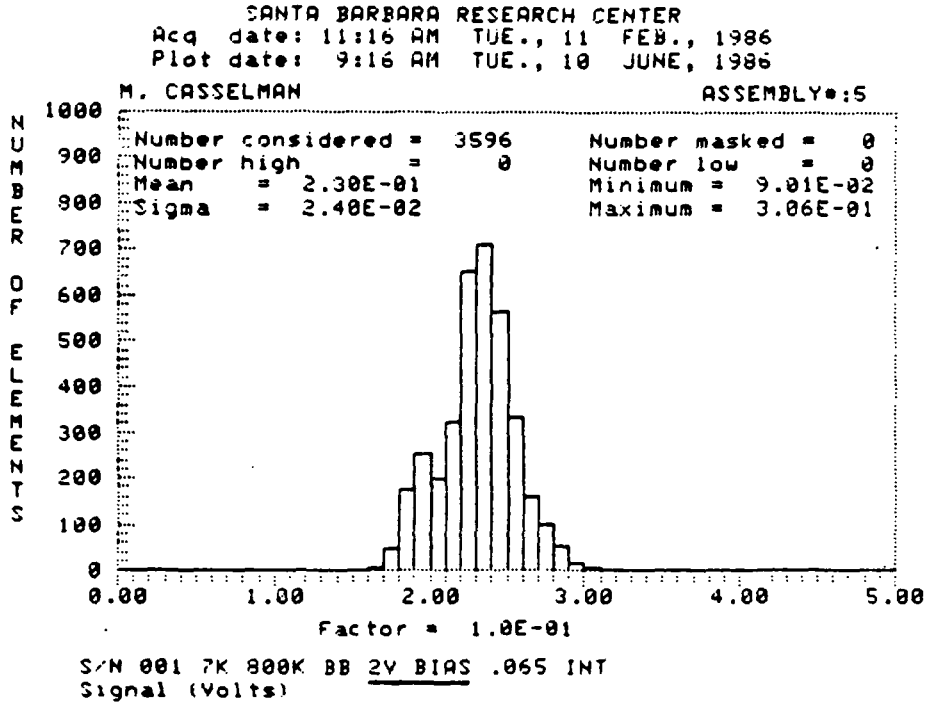
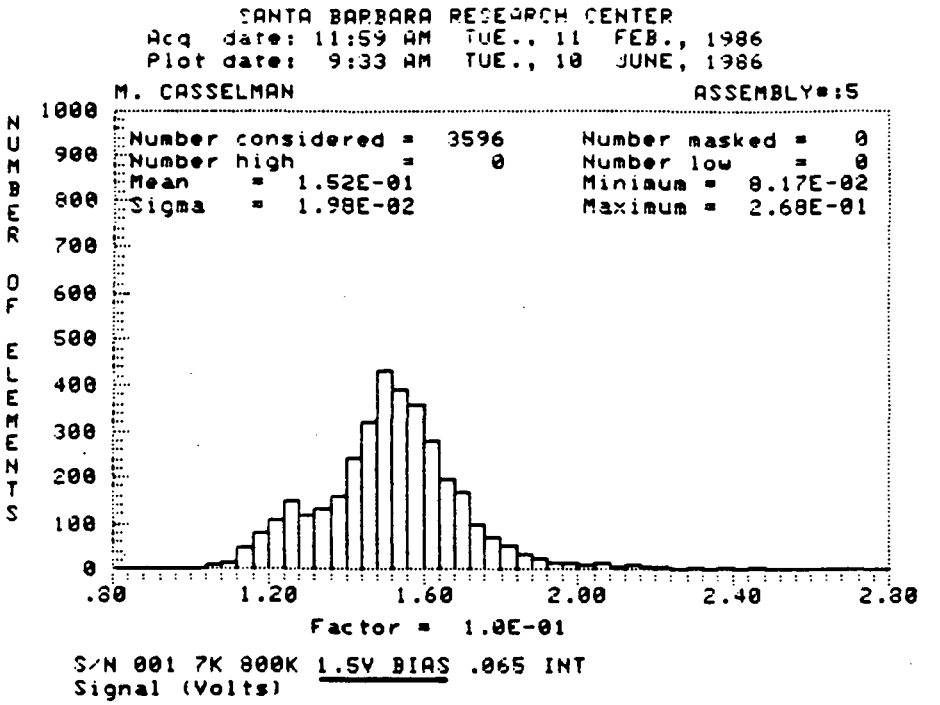


Figure 6

Si:Sb 001 Signal in Volts



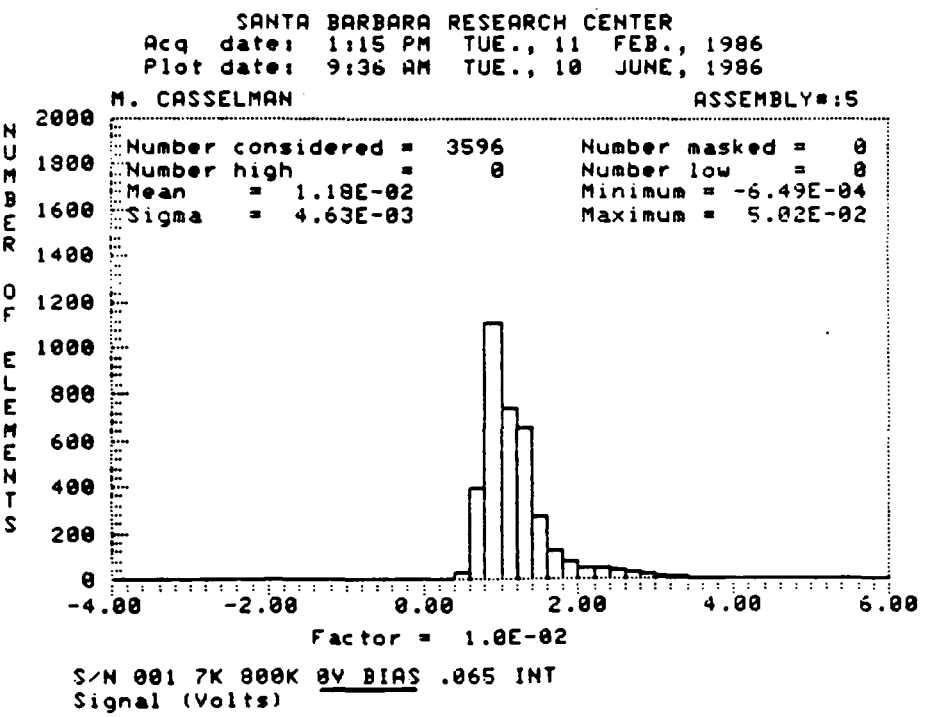


Figure 7

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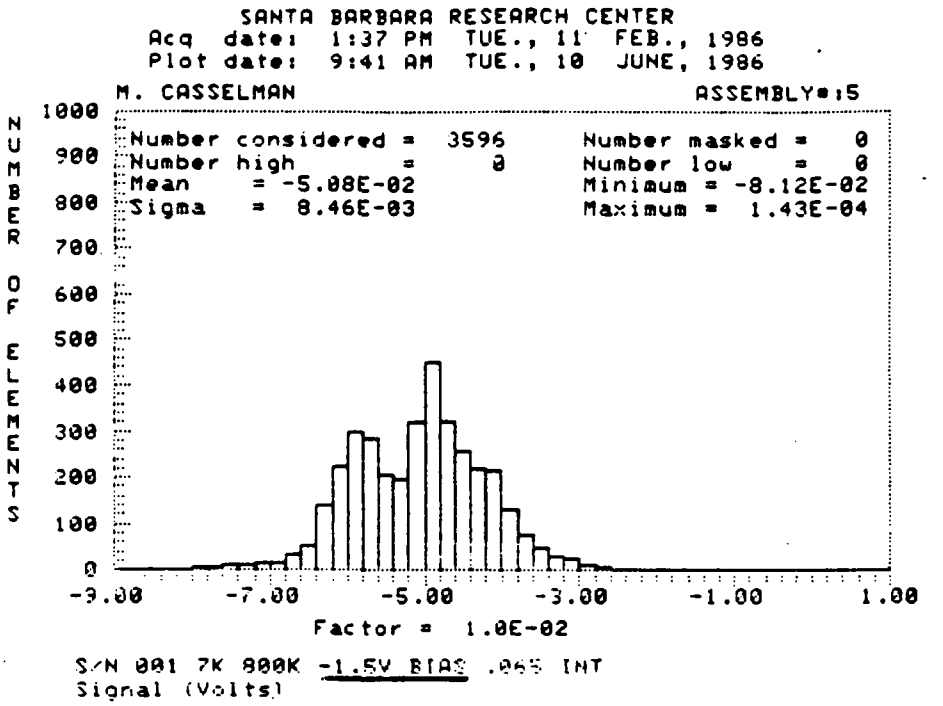
Si:Sb 001 Signal in Volts



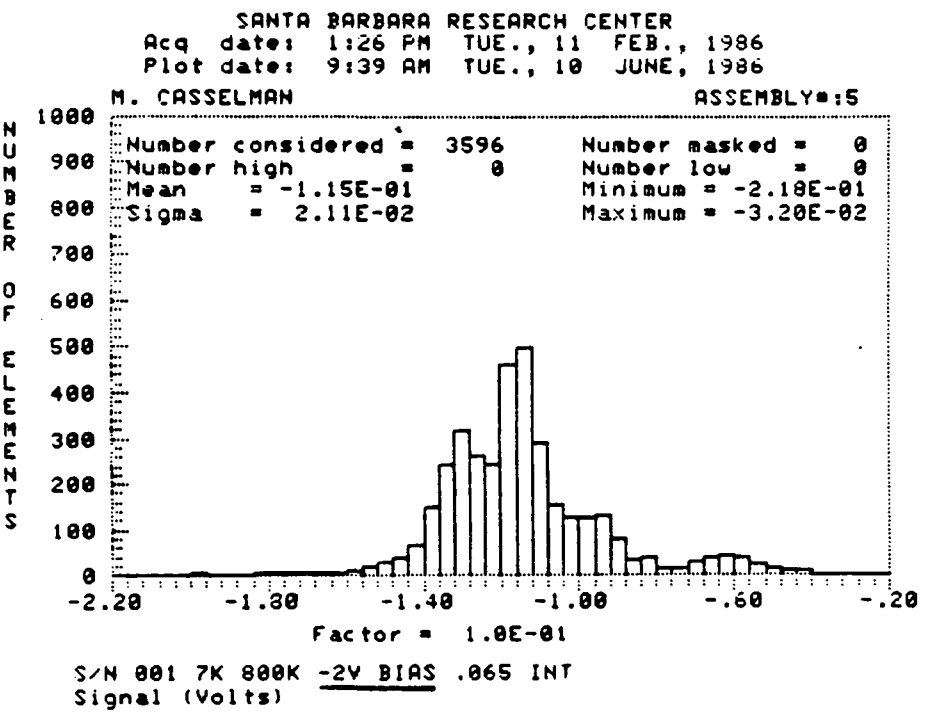


Figure 8

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Si:Sb 001 Signal in Volts

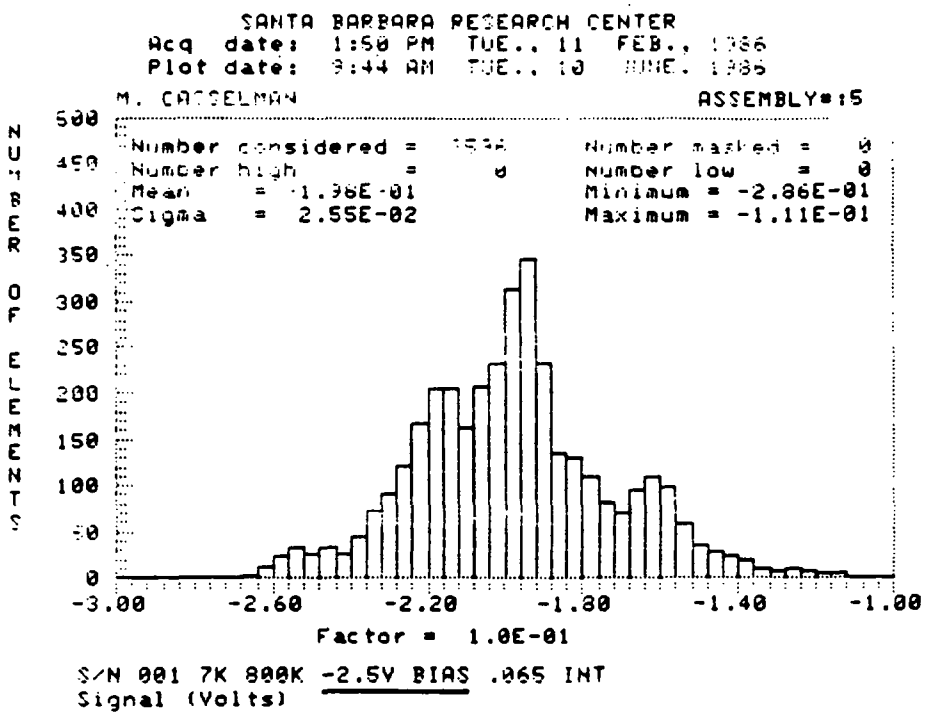


Figure 9

Si:Sb 001 Signal vs. Bias

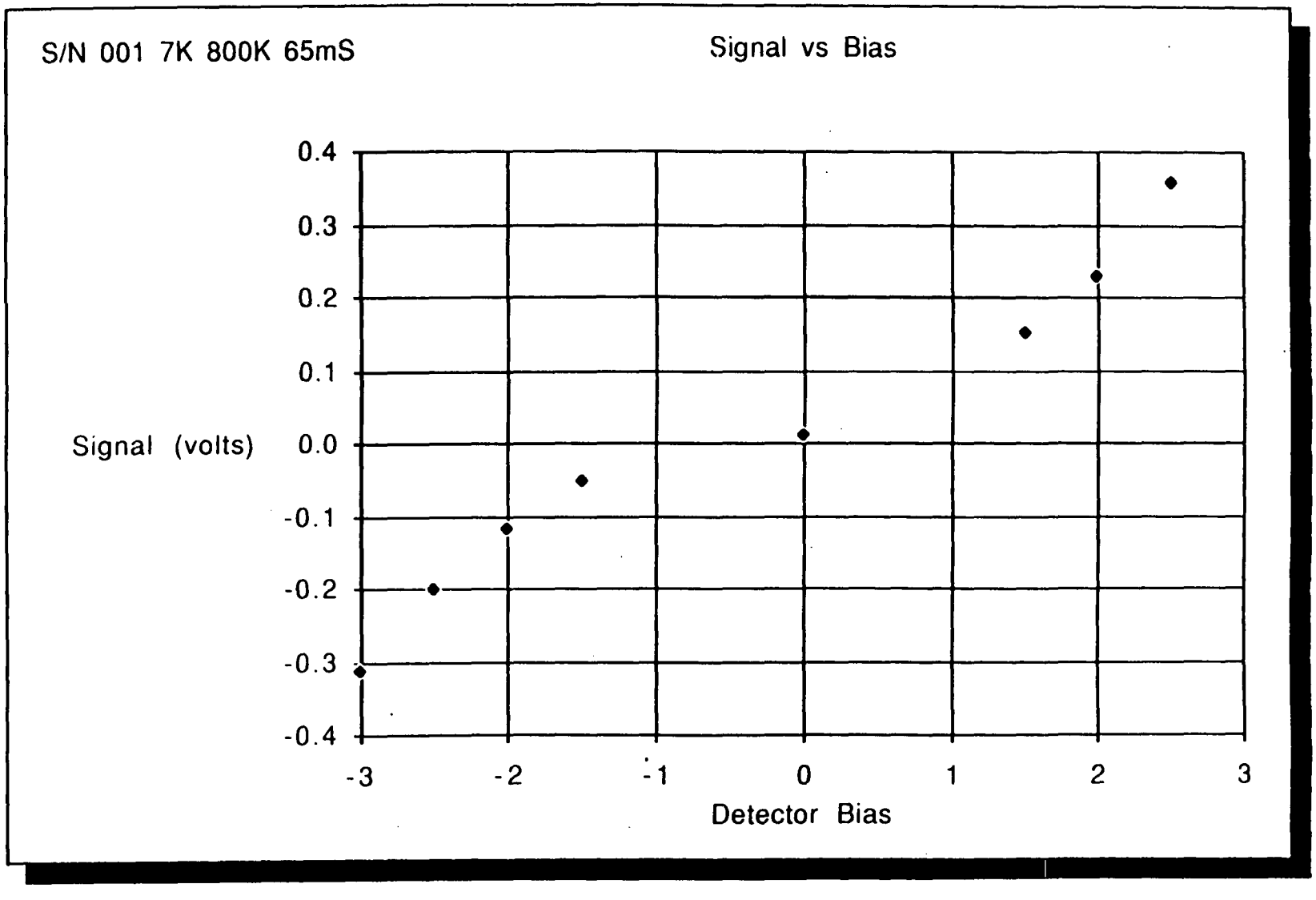


Figure 10

clock voltage settings used for the three arrays tested are listed in the Appendix. These values were chosen on the basis of previous experience, and not as the result of an optimization for the Si:Sb arrays.

Figures 6 through 9 show histograms of the signal for detector biases ranging from -2.5V to +2.5V. The relationship between output signal and detector bias is shown in Figure 10. As is expected, increasing detector bias, increases the photoconductive gain, causing more signal. One item to note is that the curve should go through the origin of the graph and be symmetrical but not around the origin. This is due to the method by which the detector is biased. The detectors are biased through reset MOSFET's. These MOSFET's have a slight threshold voltage. Thus when VRST (bias), is set to 2.0V and Det Sub is set to 2.0V, a small bias may still be present on the detectors. The data appears to be centered around approximately -30 mV which is a reasonable threshold voltage.

Figure 11 shows two important parameters. The first is NEP versus detector bias and the second is the noise versus detector bias. Because this data was taken with the shutter open, there is significant contribution from the photon shot noise. The graph shows an interesting feature of the array: apparently the NEP is significantly better for a negative detector bias than for a positive one. Figure 10 shows that the responsivity increases are roughly the same for positive and negative biases. But, Figure 11 shows that the "light on" noise increases faster for positive biases than negative biases. This results in an increase in NEP for positive biases. The data in Figure 12 show that the NEP calculated using "light off" noise decreases with increasing bias. This suggests that "light on" noise increases with increasing detector bias while "light off" noise remains roughly the same. This is due to the noise being readout noise dominated and not detector dominated.

Santa Barbara Research Center FPA S/N 002 turned out to be a rather poor hybrid. The detector array was probably as good as that of S/N 001 and 003 but the ROIC had extensive "column" problems. Uniformity was very poor and the data itself was difficult to interpret. Data from that part is not included with this report.

Difficulties were also encountered during the testing of S/N 003. At room temperature in the dewar, it appeared that one of the row address clocks

Si:Sb 001 NEP vs Bias

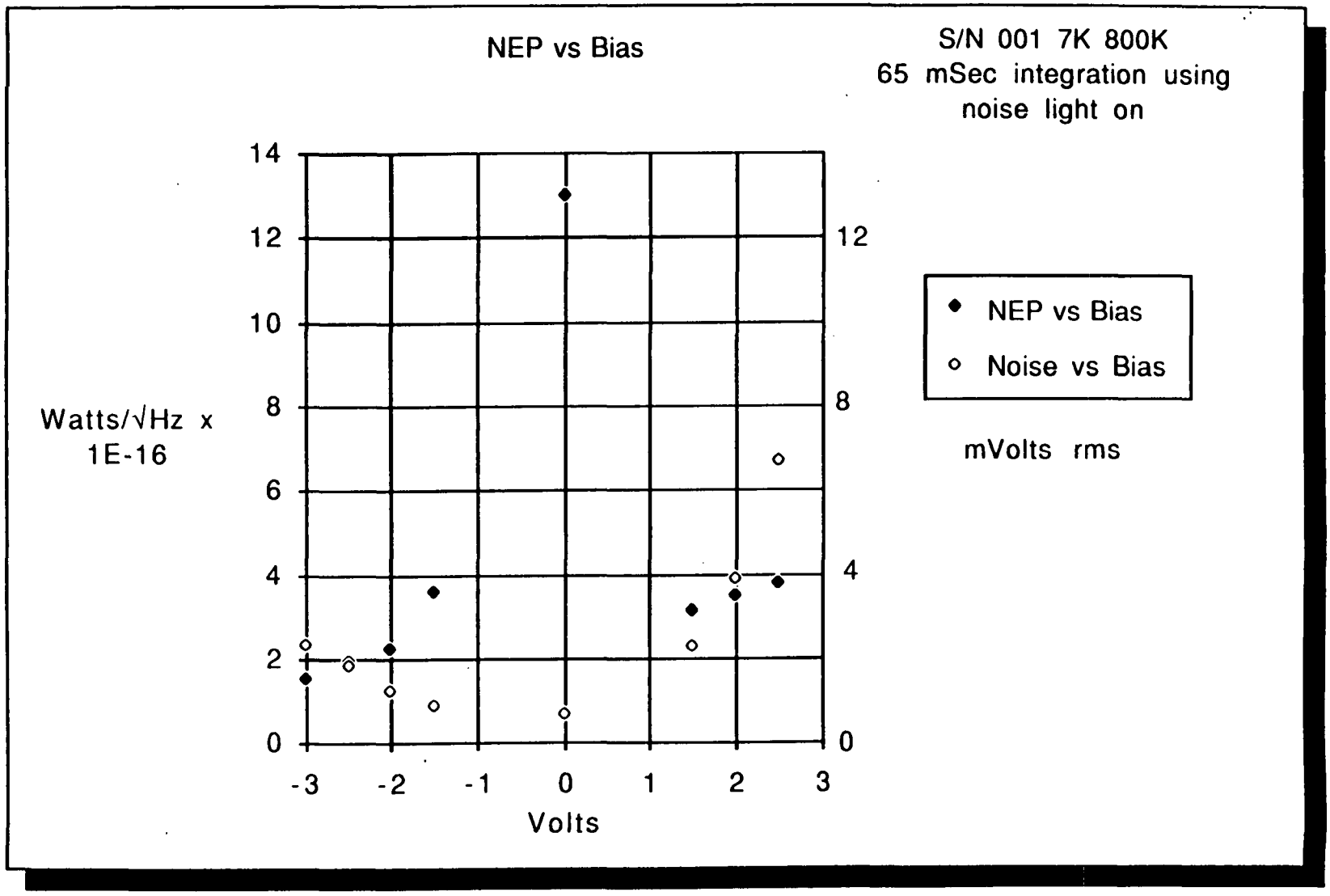
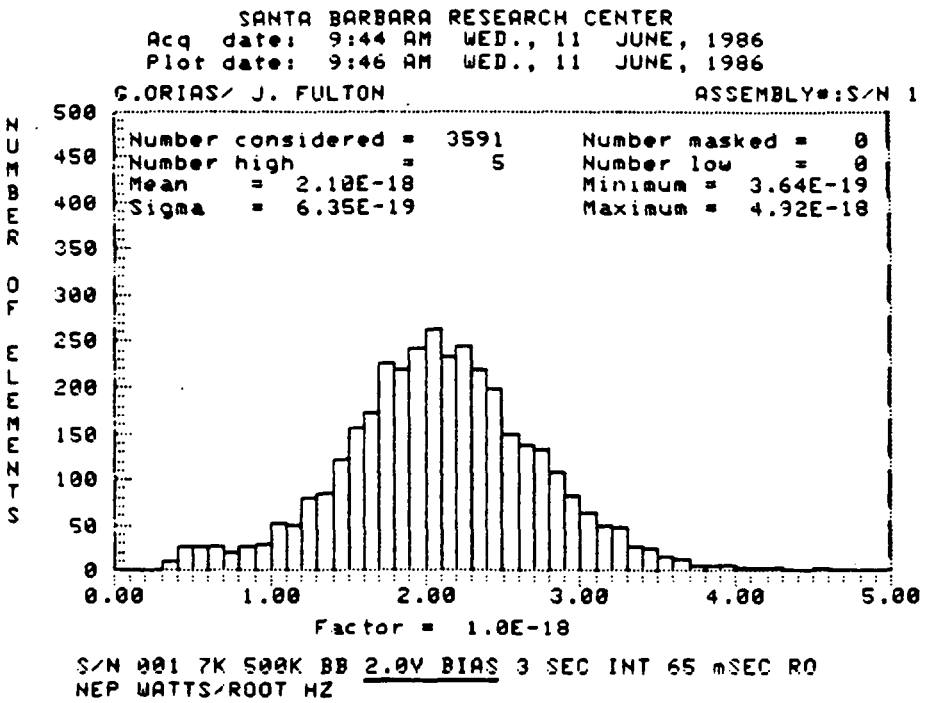


Figure 11

Si:Sb 001 NEP (500 Kelvin)



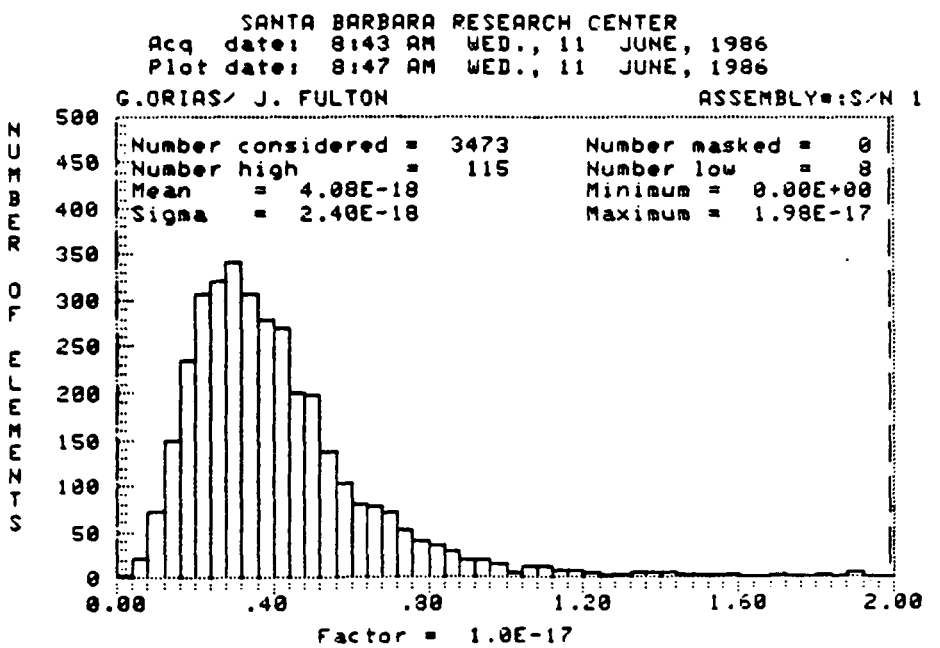


Figure 12

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was open. No fault could be found with the connector or cabling so the array was cooled. During testing the clock remained open. The array was warmed to room temperature and examined, but no problems were visible with the bond wires. The array was then operated in a "break-out box" at room temperature. During this test, the array performed exactly as expected and exhibited no opens. It is assumed at this time that the FPA is fine and that there was a set-up problem in the dewar.

S/N 003 was the first FPA to be cooled below 5K. A chip temperature of 4K was achieved by means of attaching a roughing pump to the helium well. Figures 13 and 14 show the signal and noise measured at 5 and 4K. The detectors that were open are not considered in the data (cf. "number masked" in Figure 13, for example).Figure 15 shows the results of a measurement of the signal as a function of temperature from 4 to 12K, with an integration time of 130 ms. The expected increase in signal is very apparent in this graph. Figure 16 is a graph of the noise versus temperature. This graph shows that either the noise is independent of temperature until the FPA becomes warm (11 to 12K) or that the FPA may become quieter with temperature, and we were measuring system noise. The test set noise floor is less than 100 μV. Figure 17 shows the NEP for S/N 003. The value compares favorably with the value measured for S/N 001 at the same conditions.

S/N CB was the only hybrid tested that was manufactured at Carlsbad. This FPA was less uniform than S/N 001 or 003. The array had operational difficulties which appeared to be related to the guard voltage. An unusual guard voltage of 1.8V succeeded in keeping the peripheral detectors from saturating but did not help their responsivity. Approximately 80 percent of the array was operable with the 20 percent being composed entirely of the outer lying detectors. Signal was measured at chip temperatures of 3.2 and 5K (see Figure 18) and this data shows the expected increase of signal with increasing temperature. Low response coupled with higher noise produced an array with poorer NEP than 001 and 003 (see Figure 19).

8.0 SUMMARY

In summary, S/N 001 and 003 are excellent hybrids. Assuming that S/N 003 does not have a row clock problem, they both have operabilities in excess of 90

percent while maintaining excellent uniformity. (The uniformities for the detectors within each array tested were within 15% of their median values.) The NEP data for the two hybrids is very good but there is some uncertainty as to whether they are that good. Converting the signal into a responsivity while using the same wavelength conversion factor of 100 yields a responsivity which is 6 to 10 times too large. Uncertainties in the responsivity are due to not knowing the exact sense capacitance and not having a spectral response curve of the detector.

S/N CB is also a good hybrid with no functional difficulties. It has high operability (80 percent) but poorer uniformity (50 percent). The responsivity is lower than that of S/N 001 and 003 and it appears to have higher noise.

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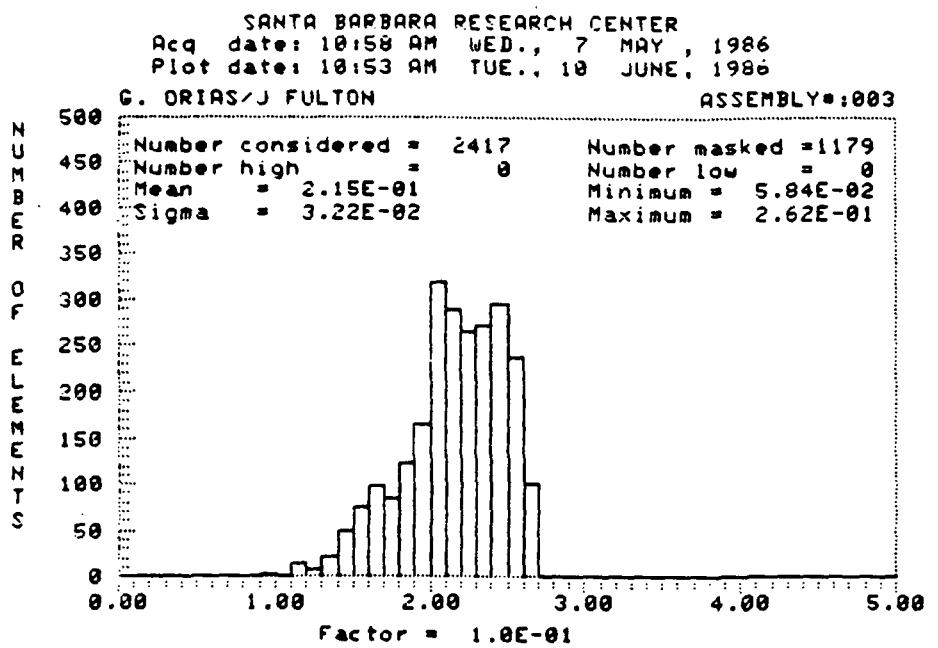
Si:Sb 003 Signal (5 Kelvin)



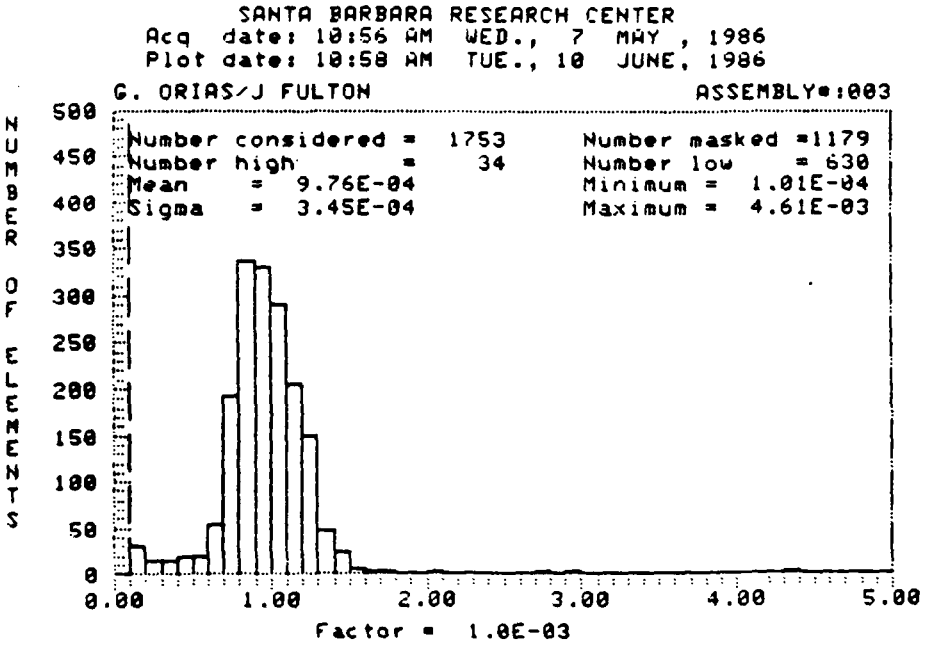


Figure 13

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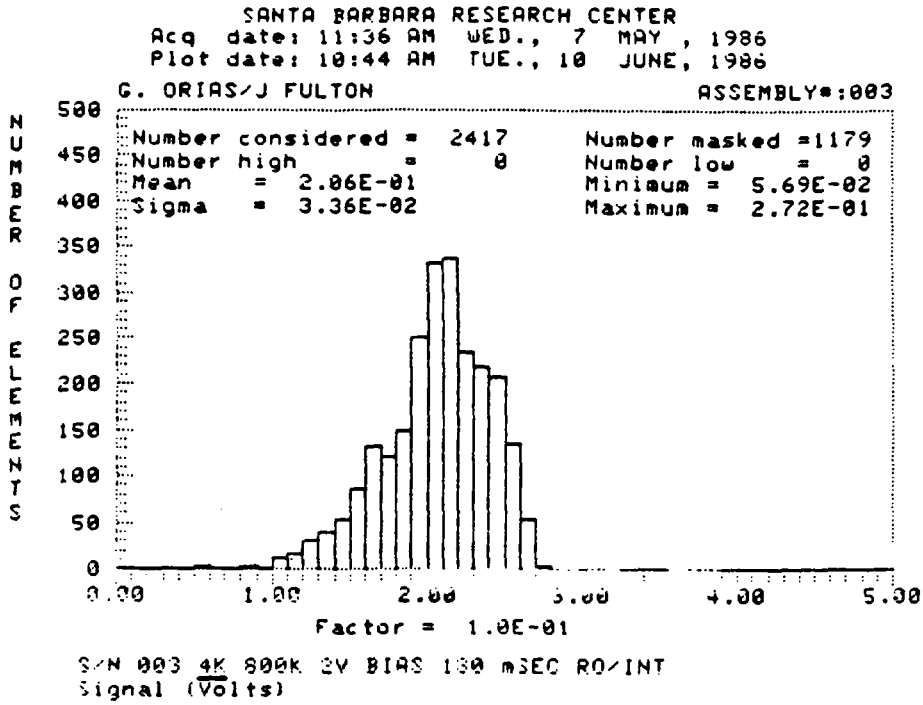
Si:Sb 003 Signal (4 Kelvin)



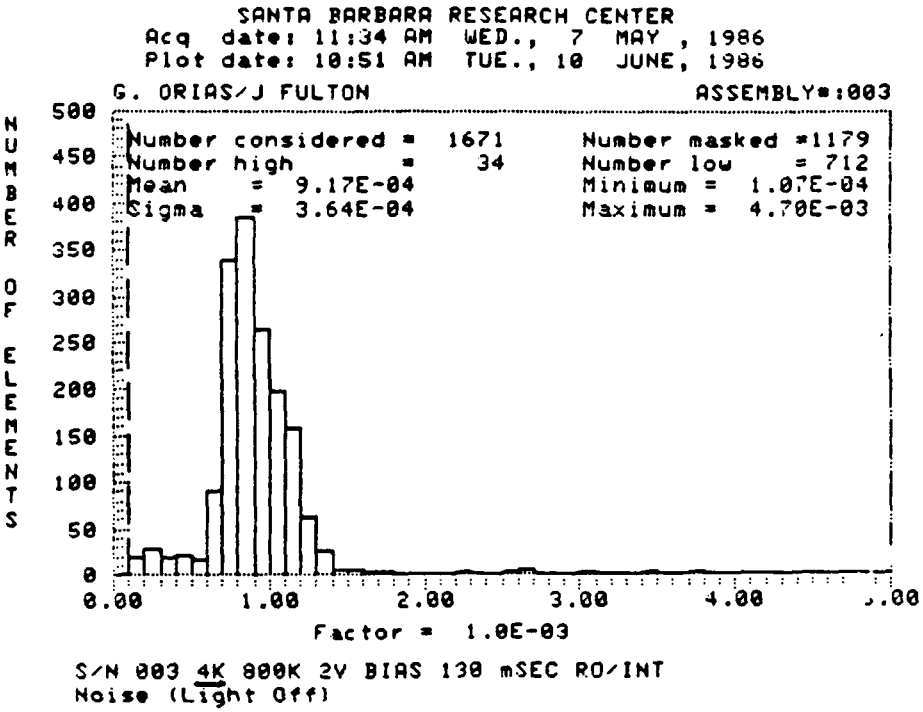


Figure 14

Si:Sb 003 Signal vs. Temperature

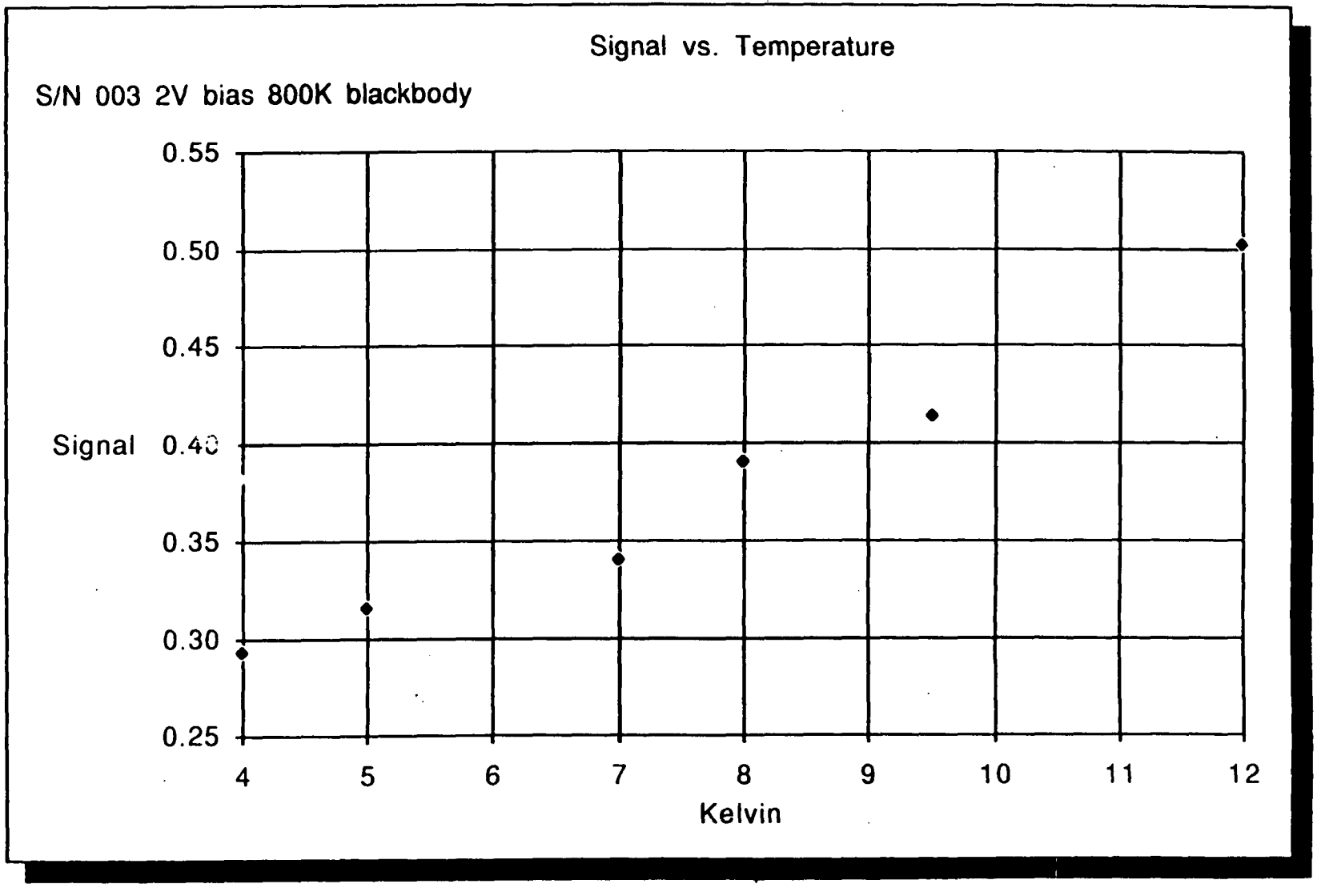


Figure 15

Si:Sb 003 Noise vs. Temperature

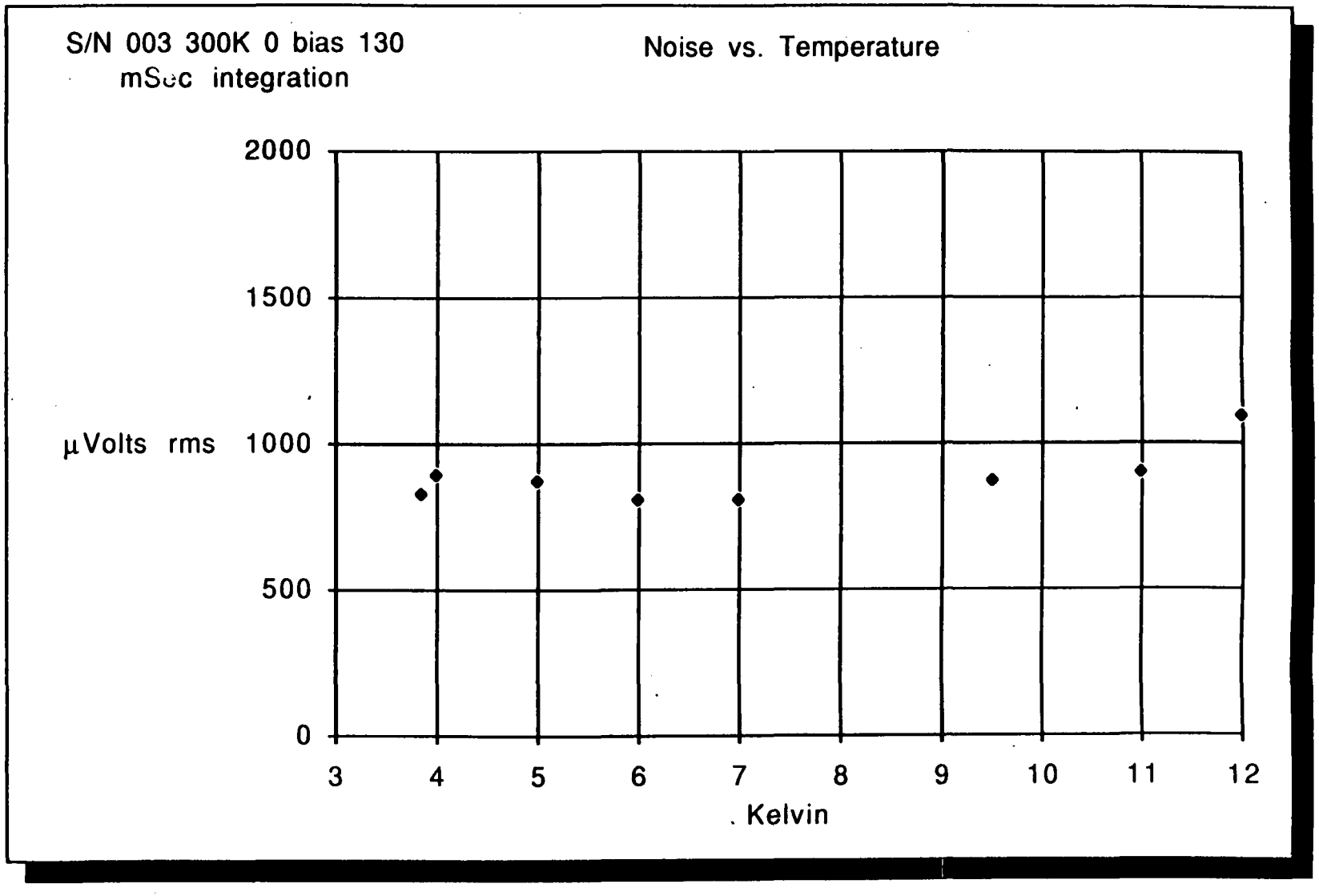


Figure 16

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Si:Sb 003 NEP (800 Kelvin)

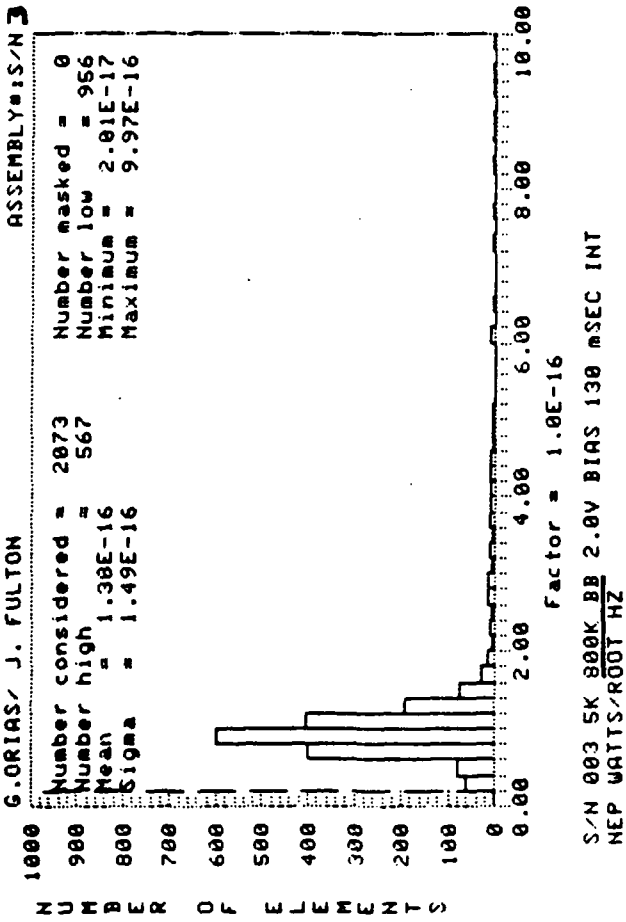

Figure 17

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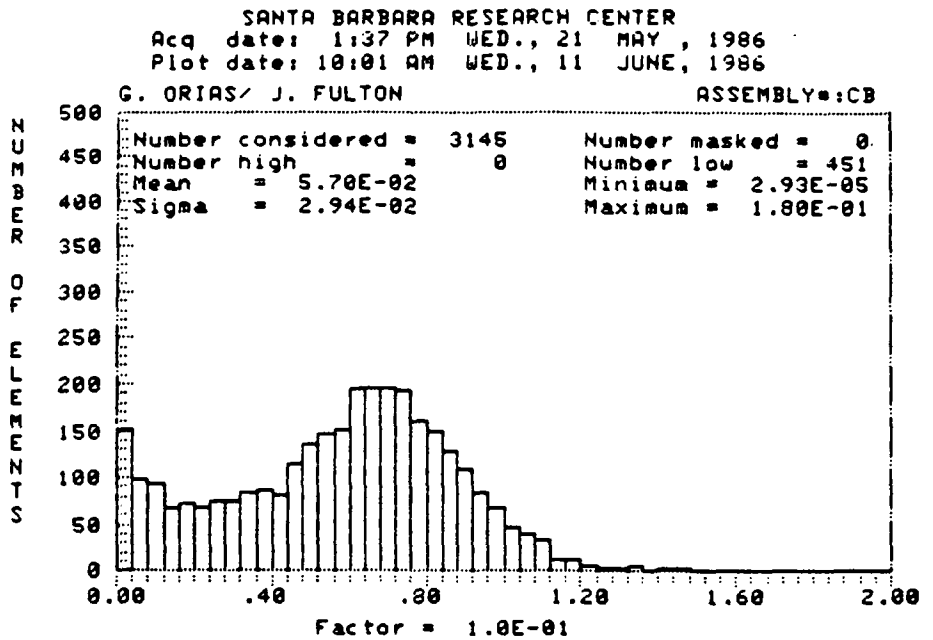
Si:Sb CB Signal in Volts



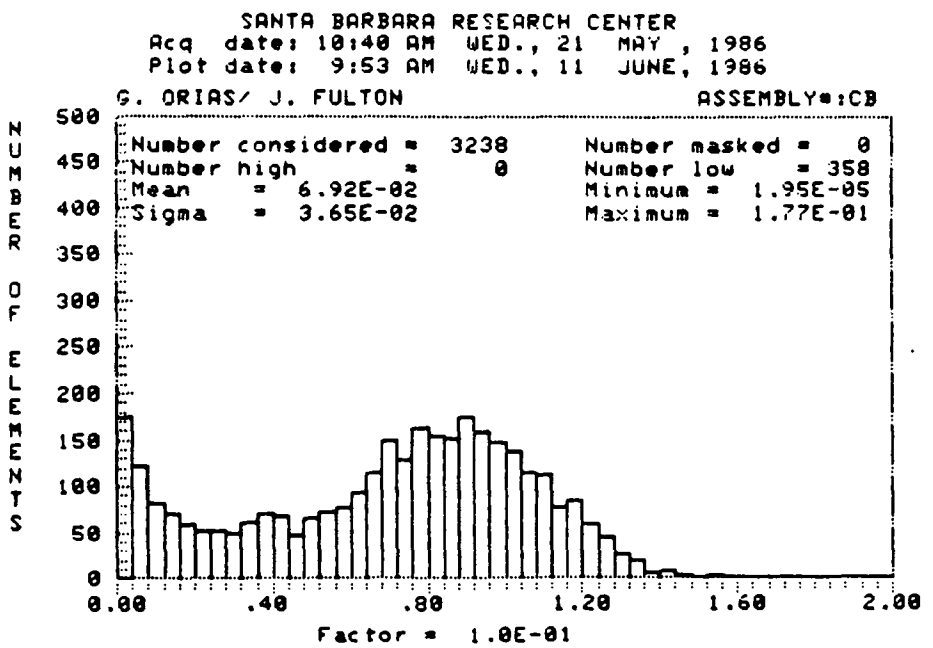


Figure 18

Si:Sb CB

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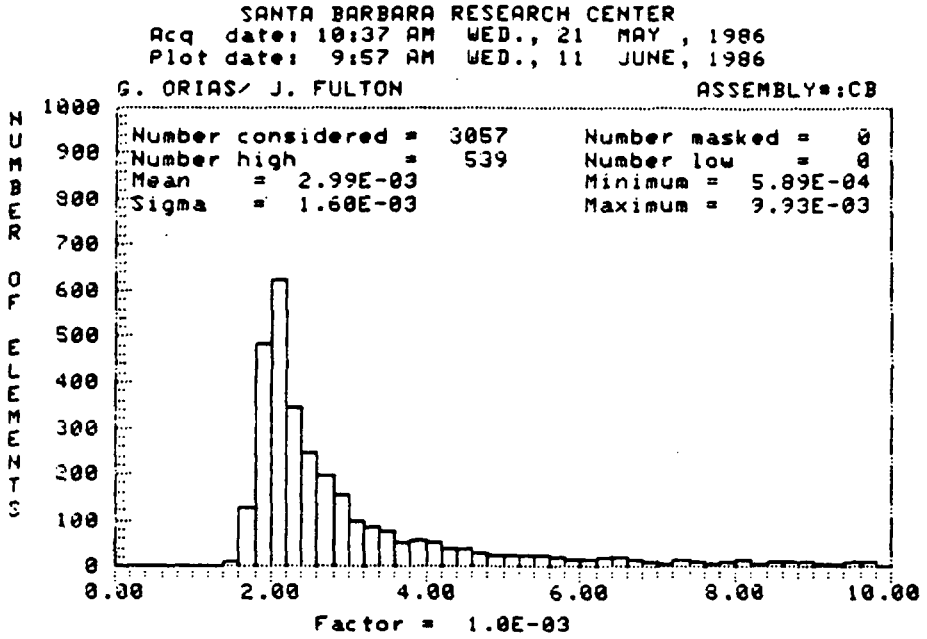

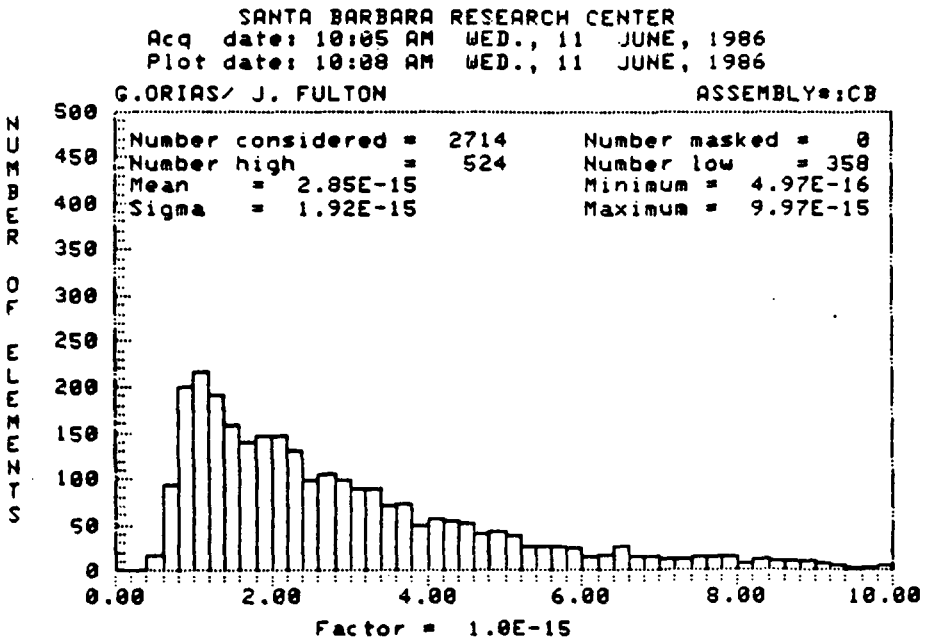

Figure 19

FPA BIAS AND CLOCK VOLTAGE SETTINGS FOR S/N 001

DC VOLTAGES		CLOCKS	LOW	HIGH
AVRST	0.0 V	RA01	0.0 V	5.0 V
VDDUC	3.0 V	RA02	0.0 V	5.0 V
VSSUC	0.0 V	RA03	0.0 V	5.0 V
VGGUC	1.5 V	RA04	0.0 V	5.0 V
VDD	5.0 V	RA05	0.0 V	5.0 V
VSUB	0.0 V	RA06	0.0 V	5.0 V
DET SUB	4.0 V	RA07	0.0 V	5.0 V
VRSTUC	2.0 V	CA01	0.0 V	5.0 V
VGRID	2.0 V	CA02	0.0 V	5.0 V
		CA03	0.0 V	5.0 V
		CA04	0.0 V	5.0 V
		CA05	0.0 V	5.0 V
		CA06	0.0 V	5.0 V
		CA07	0.0 V	5.0 V
		CAEN	0.0 V	5.0 V
		RAEN1	0.0 V	5.0 V
		RAEN2	0.0 V	5.0 V
		AØRST	0.0 V	6.0 V
		CØRSTUC	0.0 V	5.0 V

FPA BIAS AND CLOCK VOLTAGE SETTINGS FOR S/N 003

DC VOLTAGES		CLOCKS	LOW	HIGH
AVRST	0.0 V	RA01	0.0 V	5.0 V
VDDUC	3.0 V	RA02	0.0 V	5.0 V
VSSUC	0.0 V	RA03	0.0 V	5.0 V
VGGUC	1.5 V	RA04	0.0 V	5.0 V
VDD	5.0 V	RA05	0.0 V	5.0 V
VSUB	0.0 V	RA06	0.0 V	5.0 V
DET SUB	4.0 V	RA07	0.0 V	5.0 V
VRSTUC	2.0 V	CA01	0.0 V	5.0 V
VGRID	2.0 V	CA02	0.0 V	5.0 V
		CA03	0.0 V	5.0 V
		CA04	0.0 V	5.0 V
		CA05	0.0 V	5.0 V
		CA06	0.0 V	5.0 V
		CA07	0.0 V	5.0 V
		CAEN	0.0 V	5.0 V
		RAEN1	0.0 V	5.0 V
		RAEN2	0.0 V	5.0 V
		AØRST	0.0 V	6.0 V
		CØRSTUC	0.0 V	5.0 V

FPA BIAS AND CLOCK VOLTAGE SETTINGS FOR S/N CB

DC VOLTAGES	
AVRST	0.0 V
VDDUC	3.0 V
VSSUC	0.0 V
VGGUC	1.5 V
VDD	5.0 V
VSUB	0.0 V
DET SUB	4.0 V
VRSTUC	2.0 V
VGRID	1.8 V

CLOCKS	LOW	HIGH
RA01	0.0 V	5.0 V
RA02	0.0 V	5.0 V
RA03	0.0 V	5.0 V
RA04	0.0 V	5.0 V
RA05	0.0 V	5.0 V
RA06	0.0 V	5.0 V
RA07	0.0 V	5.0 V
CA01	0.0 V	5.0 V
CA02	0.0 V	5.0 V
CA03	0.0 V	5.0 V
CA04	0.0 V	5.0 V
CA05	0.0 V	5.0 V
CA06	0.0 V	5.0 V
CA07	0.0 V	5.0 V
CAEN	0.0 V	5.0 V
RAEN1	0.0 V	5.0 V
RAEN2	0.0 V	5.0 V
AØRST	0.0 V	6.0 V
CØRSTUC	0.0 V	5.0 V

NASA National Aeronautics and Space Administration

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16. Abstract

Two hybrid infrared (IR) detector arrays of antimony-doped silicon (Si:Sb) were produced and tested to evaluate their potential for use in low-background IR astronomy applications. The format of the arrays is 58 x 62 elements, with 76 μm-square pixels. A random-access, switched metal-oxide semiconductor field effect transistor (MOSFET) silicon multiplexer is used to read out the array elements. Reduced-background tests of signal, noise, and noise equivalent power were conducted over the temperature range 3.2 to 12 K. The arrays were found to have good sensitivity and good uniformity.

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