COMPUTERIZED MONITORING AND CONTROL OF EXPERIMENTS IN SPACE

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ABSTRACT

The Villanova University GAS experiment apparatus is divided into three major subsystems: the boiling experiment apparatus, the polymer experiment apparatus and the computer subsystem. This paper will be limited to a discussion of the computer subsystem.

The function of the computer subsystem is to provide data acquisition and control system support to the experiments. The computer subsystem will provide high availability, low power consumption, and highly reliable data retention. The general layout of the subsystem provides for redundant processing units, control modules, and multiple data acquisition modules.

The two redundant processing units are identical. Each processing unit will be self checking and will contain the same program code. Each processing unit will be composed of a microprocessor, control logic, PROM, RAM, non-volatile memory, timers, self check logic, and data ports to the data acquisition and control modules. One unit will control the experiment while the other shadows the primary unit operation. The data ports are generic, this yields increased flexibility in use with the current experiments, as well as with future experiments.

The data acquisition module gathers data from the experiment. The data is transferred to the redundant processing unit in digital form. The control module will receive command data from the redundant processing unit. The control module validates the data, decodes it and executes the command.

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The Computer Subsystem

The computer subsystem is designed so that it can be used for any GAS experiment to control and monitor a wide range of devices and sensors. It is also designed to operate in the harsh environment of space. The concerns for the GAS canister environment include radiation, large temperature swings, and battery power. In the boiling experiment, the computer will control devices such as a simple heating element, a stepper motor, 35mm cameras, subsystem coolant pumps, and will monitor time, temperature and pressure. In the polymer experiment, the computer will control the chemical release mechanism and monitor time and temperature. The two experiments are designed to run at different times during the space shuttle's flight. The computer will also monitor temperature inside the GAS canister.

The computer subsystem will provide high availability by having redundant capability. The redundancy will be incorporated into two processing units and duplicate monitoring and data acquisition modules as seen in Figures 1 and 2. The power consumption will be minimized by using low power Complementary Metal Oxide Semiconductor (CMOS) digital components. Highly reliable data retention will be provided by storing a copy of the data in nonvolatile memory with error detection and correction on each of the processors and also by placing the data on peripheral storage via a very small printer or information display panel with a camera. In addition to the redundant element of the system, the digital component used in the system will be "Industrial" grade, which is one grade better than is found in a typical home computer.

Identical redundant processors will each be composed of the following: a microprocessor, control logic, PROM, ROM, nonvolatile memory, timers, self check logic, and data ports. The microprocessor will be a CMOS version of either an Intel 80X86 or Motorola 680X0 processor family. The choice of processor will depend on throughput required and availability of development tools. Most of the control logic will be composed of CMOS programmable array logic (PAL) and interrupt controllers. The flight version of the PALs will be non-alterable, while the development version will be an erasable version. Like the PALs, the PROM will also be CMOS and for the flight hardware be non-alterable. The RAM will have an error detection and correcting code added to the data, allowing most data errors to be automatically corrected. The nonvolatile memory will be an Electrically Erasable Programmable Read Only Memory (EEPROM) or a similar device. The data written to nonvolatile memory will also have an error correction code associated with it. The experiment timers will be backed up by the self check logic.

The self check logic will include "deadman" timers and address range check logic. The "deadman" timers will insure that the processor does not get caught in an infinite loop because of a software error or memory upset. Memory upset can occur when radiation hits a memory cell inside a semiconductor chip. Each processor unit contains two "deadman" timers. One "deadman" timer monitors the unit's execution and is connected to the processor's non-maskable interrupt. The

other "deadman" timer monitors the execution of shadow processing unit and is connected to the programmable interrupt controller. A connection to the non-maskable interrupt which can not be postponed allows any processing to be stopped. The primary processing unit can postpone dealing with processing problems with the shadow unit, if necessary. The reason for the delay in dealing with the shadow processing unit results from the need of the primary processing unit to process events associated with the experiment in a timely manner. The address range check logic will protect against software errors and processor internal memory upsets by causing a non-maskable interrupt to occur.

Communication between the processing units to and from the control modules and data acquisition modules will provide for reliable communication and failure isolation. The ports on the processor board will have bidirectional data transmission and each port will operate either as a serial or parallel data path. The electrical interface will use a standard interface such as RS-232 or Centronics. To off-load work from the main central processing unit (CPU), a microcontroller, such as an Intel 8051, will be used to control the communication interface. Each port can be configured so that it may be used either as a port to a control module or a port to a data acquisition module.

The control or data acquisition module will be redundant. The interconnection of the modules to the processors will be pairwise as shown in Figure 1. The modules are interconnected to enable the module controlled by the operational processor to override the other module in the event that a processor shuts down. Data flows in both directions between the experiment and redundant modules.

A control module, which controls a stepper motor for example, will contain all the items needed to control the motor. The module will contain communication interfaces, logic to decode data coming from the processor, and logic to control the motor. The communication interfaces will go to a processor unit or to the redundant control module. When in operation, a processor unit will send a command to the control module. The command is then decoded by the control module which causes the stepper motor to move in the manner indicated by the command.

A data acquisition module used to collect temperature readings will read and transmit the data to a processor unit. The module will contain communication interfaces, the logic to digitize the temperature data and logic to control transmission of the data to a processor unit. When in operation, a processor will request that the module read the temperature. The data acquisition module will then, via an analog to digital converter, convert the analog electrical signal coming from a temperature sensor to a digital number which will then be transmitted to the requesting processing unit.

The PROM-resident software will control the experiments. It is the software that will coordinate a heater's output with the measurement of the corresponding temperature rise. The software will also have to configure the communication ports to the control and data

acquisition modules. The software will have control over which experiment is currently running and will switch over after the first experiment is completed. The system software can not be fully designed until all of the devices and conditions that need monitoring are known.

The main improved capability of the computer subsystem over the typical home computer is that the subsystem will incorporate many redundant features, low power consuming CMOS components, as well as higher grade semiconductor components. The many redundant features of the system and higher grade components significantly lower the possibility that the subsystem will be unavailable. The extensive use of CMOS components will lower the subsystem's power requirement thereby reducing the number of batteries needed to supply power. The highly reliable data retention is insured by storage of multiple copies of the data in two sets of nonvolatile memory with an error detecting and correcting code attached; data will also be saved on peripheral storage.

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Module Connection Diagram

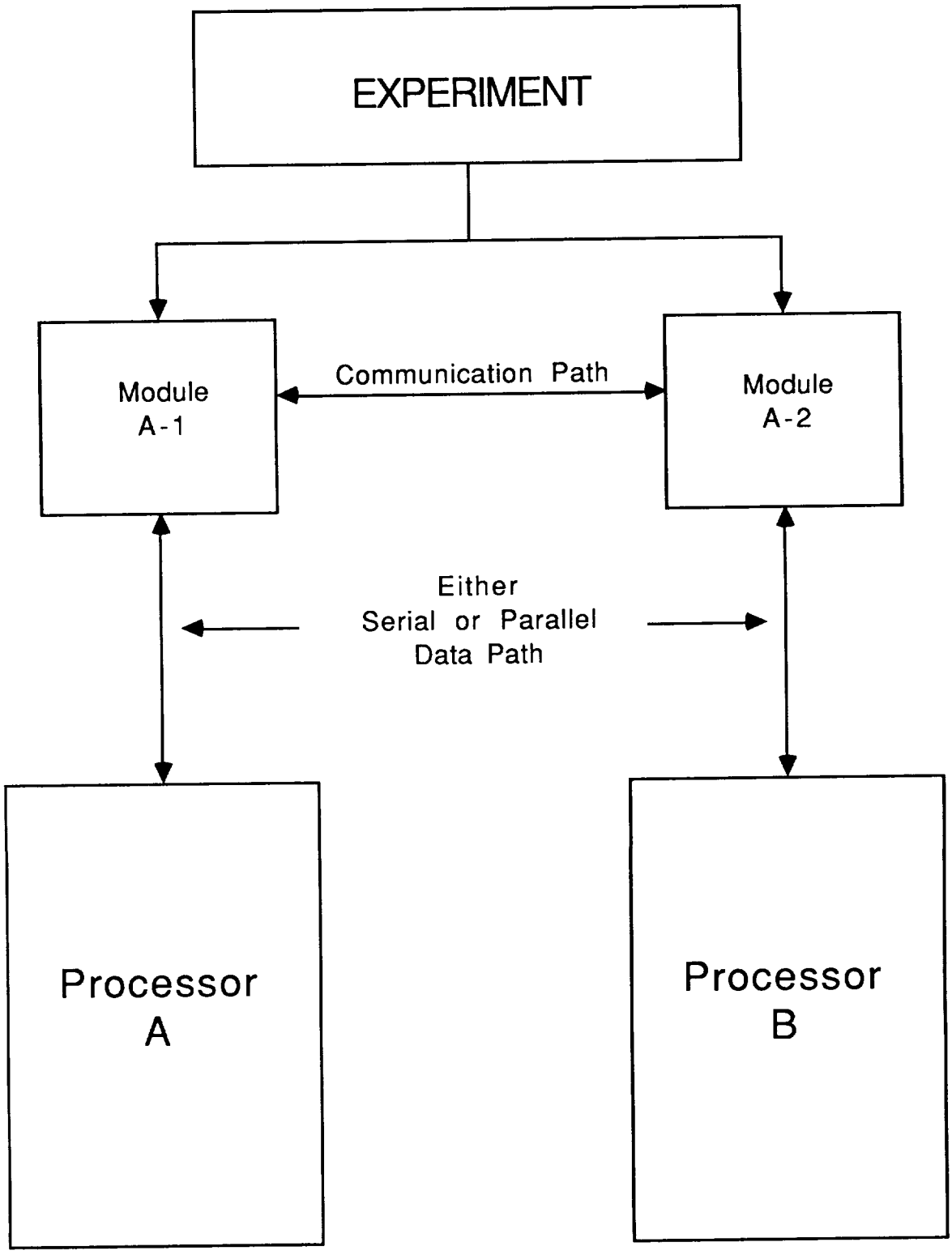
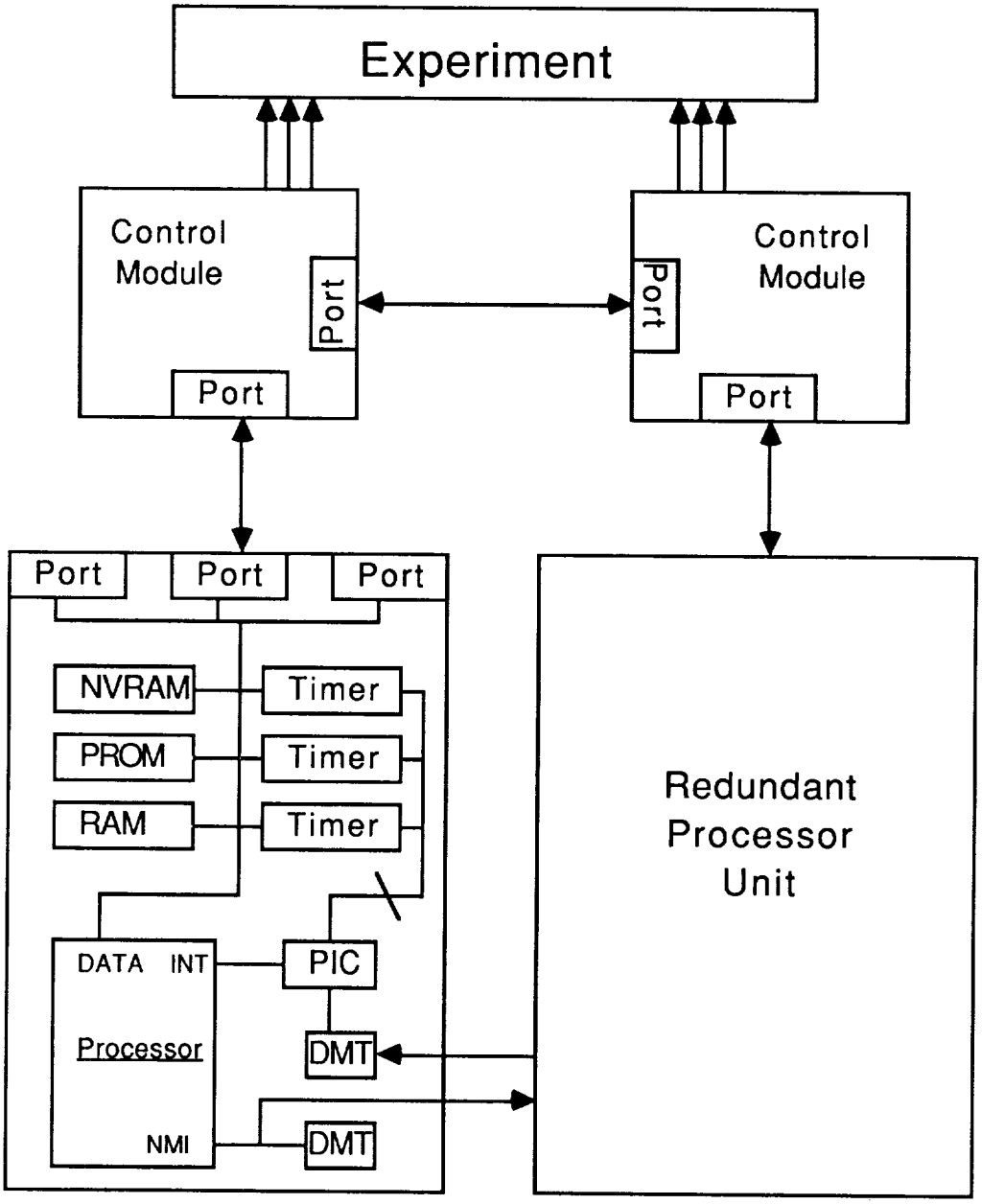


Figure 1

Computer Subsystem Block Diagram



Key:

DMT - deadman timer INT - interrupt NMI - nonmaskable interrupt NVRAM - nonvolatile RAM	PIC - programmable interrupt controller PROM - programmable read only memory RAM - random access memory

Figure 2