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POWER QUALITY LOAD MANAGEMENT FOR LARGE SPACECRAFT ELECTRICAL POWER SYSTEMS

By Louis F. Lollar

Information and Electronic Systems Laboratory

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16. ABSTRACT

In December 1986, a Center Director's Discretionary Fund (CDDF) proposal was granted to study power system control techniques in large space electrical power systems. This paper presents the accomplishments in the area of power system control by power quality load management. In addition, information concerning the distortion problems in a 20 kHz ac power system is presented.

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INTRODUCTION

In December 1986, a Center Director's Discretionary Fund (CDDF) proposal was granted to study power system control techniques in large space electrical power systems. This paper presents the accomplishments in the area of power system control by load management; specifically, load management based on a load's and a system's power quality.

AUTOMATION AND LOAD MANAGEMENT

Autonomously Managed Power System

In 1978, NASA/MSFC began studying autonomous operation techniques for large, high-power spacecraft power systems. The initial focus of this study centered around the Autonomously Managed Power System (AMPS) program. The AMPS program was a three-phase effort. The first phase identified a reference photovoltaic electrical power system for a 250 kW class low Earth orbit satellite. The second phase developed the autonomous power management approach for the reference electrical power system. Finally, the third phase produced a breadboard test facility to evaluate, characterize, and verify the concepts and hardware resulting from phases 1 and 2 [1].

This breadboard test facility consists of (1) a programmable solar array simulator which supplies 220 ± 20 Vdc directly to three power channels with a maximum power output of 75 kW; (2) an energy storage simulator which consists of a battery with 168 commercial nickel-cadmium (Ni-Cd) cells serially connected to provide a nominal dc voltage of 220 V and a capacity of 189 A-hrs; and (3) a load simulator which consists of nine resistive loads and one dynamic load that consume a total of 24 kW of power when operated at 200 Vdc. In addition, three Motorola 68000 microcomputer-based controllers provide data retrieval and low-level decision-making for the power system with a NCR Tower-based host computer providing programmability for flight power system simulations [2].

As a result of the CDDF proposal, additional funding was obtained from the Office of Aeronautics and Space Technology to install a second power channel to the AMPS test facility. This channel consists of a 17-kW solar array simulator, a flight-type Ni-Cd battery left from a Skylab project test bed, and a second microprocessor controller and battery cell scanner. Even though the second channel is lower power, the ability to manage loads between two independent power channels is attained. In addition, the lower power allows for degraded power channel simulations. The block diagram of the two-channel facility is shown in Figure 1.

Artificial Intelligence

In 1984, MSFC began the next stage of electrical power system automation with the development of expert or knowledge-based systems. The expert systems developed thus far are focused on fault diagnosis and contingency payload scheduling. Systems now under development address comprehensive fault management, automatic rescheduling, and intelligent data reduction. Future plans involve the development of expert systems for battery management, trends analysis, and component failure forecasting [3].

Several expert system prototypes that have been developed and/or are being developed include: the second generation Fault Isolation Expert System (FIES II), the Space Station Experiment Scheduler (SSES), the Hubble Space Telescope electrical power system test bed diagnoser/analyzer named NICBES (Nickel-Cadmium Battery Expert System), a second generation NICBES, three expert systems operating closed-loop for the Space Station Module/Power Management and Distribution test bed [the Loads Priority List Management System (LPLMS), the load enable scheduler (LES), the Fault Recovery and Management Expert System (FRAMES)], the Intelligent Data Reduction Expert System (I-DARE), the fault detection/diagnosis/recovery expert system for AMPS (STARR), and a second generation fault monitoring and diagnosing expert system (AMPERES) [3,4].

The 5 kW, 20-kHz Power System Testbed

In 1988, MSFC received a high-frequency (20 kHz) power system breadboard which electrically approximates a scaled-down (5 kW) version of the dual, redundant power channels of an IOC space station (Fig. 2). The breadboard includes the following major elements:

1) Nine inverter/driver modules which can be operated in single or three-phase mode with either dc or ac input power.

2) A set of source control switches [analogous to the space station Remote Power Controllers (RPCs)] to demonstrate autonomous system fault protection.

3) A dual 50-m transmission bus system.

4) A set of load control switches (RPCs) to demonstrate how the system will protect itself against load/user faults.

5) A set of five high power user modules.

6) A computer control system using a MacIntosh terminal and supervisory interface, which commands embedded processors in the power hardware, to demonstrate system control and to display system status [4].

This system is presently being analyzed and will eventually be integrated into the SSM/PMAD and AMPS breadboards for further autonomous power system operation studies.

LOAD MANAGEMENT AND POWER QUALITY

In terrestrial utility power systems power flow is typically controlled by power source management. In Low Earth Orbit, a spacecraft power system's source has limited power available and limited flexibility. Therefore, power flow management will be accomplished by load management techniques.

Load management involves determining the present state of the power system and then, if necessary, balance the system by shedding or adding loads based on certain key parameters of the loads. In order to accomplish these tasks, four load management criteria are being studied:

1) Power bus balancing on multi-channel power systems.

2) Energy balancing on multi-channel power systems.

3) Contingency load shedding/adding.

4) Power quality matching of loads to busses.

The fourth load management criteria involves relating particular loads to particular power busses. This is performed by matching the power quality of the load to the power quality of the bus. For example, a pump or a switching power regulator should not be connected to the same bus in which a critical data acquisition system is connected. Managing this criteria requires determining the power quality of the loads, sensing and storing the power quality of the buses, and then matching the correct load(s) to the correct bus(es).

Power Quality for AMPS

Initial power quality work centered on AMPS and involved evaluating various methods to define a power quality for the dc system. From terrestrial power system work, the working definition for power quality is based on the Total Harmonic Distortion (THD) of the power system busses. Thus, the attempt was made to define a THD value for a dc power system. At present, two methods are being pursued.

The first method involves using the ratio of the RMS ripple current to the average total load as the reference and then using the harmonic currents of the ripple to determine a THD. One problem with this method is that the reference is a function of load current and will therefore be constantly changing in a dynamic system.

The second method involves using the limits of Mil-Std-461 as a reference and then measuring the frequency spectrum of each load and the power bus(es) to determine a THD. One problem with this method is that each harmonic component has its own reference, therefore large percentages can result when the ratios are summed.

Further studies are continuing on both of these methods plus research into other ways of obtaining a numerical definition for power quality in a dc system. However, this research has taken a lower priority due to the power quality work being performed on a 20-kHz ac power system.

POWER QUALITY FOR A 20-kHz ac POWER SYSTEM

Soon after the CDDF was awarded, NASA/MSFC began a parallel effort to study the effects of the space station module loads on the 20-kHz ac power system. Initial studies revealed that power quality would be a critical design issue. As a result, the power quality/load management research being performed for the CDDF was applied to the space station effort with very promising results.

THD in a 20-kHz ac Power System

In most ac power system loads, the majority (>90 percent) of the load distortion is located in the first nine harmonics of the waveform. For a 60-Hz ac power system, these nine harmonics range from 60 Hz to 540 Hz and for a 400-Hz ac power system, they range from 400 Hz to 3600 Hz, but for a 20-kHz power system, they range from 20 kHz to 180 kHz. At these higher frequencies, the natural LC circuit parameters in the transmission lines begin to resonate causing distortion amplification and phase shifting. (Figures 3 and 4 are actual oscilloscope photographs of the source and load ends of the 50-m co-axial cable feeding the 28 Vdc, 1 kW load receiver in the 20-kHz testbed with no high frequency filtering.) Therefore, transmission lines, even short ones, can become critical components in the power management and distribution schemes of any 20-kHz ac power system. In fact, without careful cable consideration, even a resistive load will violate the conducted and radiated emission specifications set forth in Mil-Std-461. These facts led to a study of filter requirements needed for various loads in a 20-kHz ac power system.

A Transformer Rectifier Filter Load

The first step in studying the effects of power quality in a 20-kHz ac power system was to design a typical load for the 20-kHz testbed. In order to keep the analysis simple yet representative, a 3-kW transformer rectified dc resistive load was designed and built.

Due to the unknowns of the 20-kHz ac power system, a transformer rectified filter (TRF) circuit was modeled using SPICE (Fig. 5) before attempting any actual construction. The first model consisted of the TRF with no input filtering and the SPICE analyses predicting input current THDs in the 35 percent range. Next, a series LC input filter was added which dropped the THD to the 26 percent range on the initial attempt. Finally, by adjusting the input L and C, a THD in the 13 percent range was obtained [5].

In addition to the THD analyses of the input current, the output voltage of the TRF circuit was plotted and an output voltage change of as much as 20 percent was observed as the load current changed. Therefore, to obtain better load regulation, a saturable inductor was designed to provide variable tuning in the output filter of the circuit. After obtaining data from the SPICE analyses and the actual circuit, better regulation was obtained as a result of the saturable inductor [5].

SPICE Model Versus Actual

The actual TRF circuit is essentially the same circuit as shown in Figure 5. The input voltage source for the TRF consisted of a Mapham type series resonant inverter operating at 20 kHz. The load consisted of a bank of programmable high voltage dc resistors plus a 3 kW active load obtained from the AMPS testbed. Data was obtained using a Tektronix 7854 oscilloscope and a 7L5 spectrum analyzer [5].

Figure 6 is a plot of the first nine harmonics taken from the SPICE analysis at a load current of 10 A. The magnitude is in dB with the 20-kHz fundamental referenced at 40 dB. Figure 7 is the corresponding spectrum analyzer picture taken from the TRF circuit. The 20-kHz fundamental is referenced at one division from the top. As can be seen, the THD value for the SPICE model was 15.68 percent for a load current of 10 A and the measured and computed THD value for the actual circuit was 14.9 percent for a load current of 10 A [5].

The confidence established in the TRF SPICE model ensured its extensive utilization in the next effort to further reduce the input current THD. This next effort centered around a three-stage input filter called the Harmonic Trap/Double LC filter (HTDLC).

The HTDLC Filter

In performing research on a 20-kHz breadboard for NASA/Lewis Research Center, John Biess of TRW encountered the same distortion problems as that of MSFC's 20-kHz breadboard. As a result, he had developed a single-stage notch filter called a harmonic trap [6]. Essentially, this filter presents a resistive impedance to all frequencies except for the 20-kHz fundamental. In our effort to reduce the input current THD values to a utility industry level (<5 percent), we had to add two more filter stages to the harmonic trap to achieve the desired results, thus the HTDLC filter. This filter provided an immediate reduction in the input current THD. In fact, the 10-A TRF circuit's THD value decreased from the 15.68 percent noted earlier to an acceptable 4.32 percent.

Based on these results, we designed a "worst-case" load in order to fully test the HTDLC filter. This load consisted of a TRF circuit with a pi-filter on the output (Fig. 8). This type of load will draw large pulse currents from the source, thus causing large harmonic components. Even with this "worst-case" load, the HTDLC filter reduced the THD level from 97.8 percent to 12.14 percent for a 10-A load (Figs. 9, 10, and 11).

Despite the excellent results obtained by the HTDLC filter, problems with weight and transient response are encountered. In order to solve the problem of circulating harmonic currents, an HTDLC filter will have to be installed on practically every load and on the output of every source. Therefore, with hundreds of possible loads for space station and the power levels of these loads, adding these HTDLC filters could produce a significant weight problem for the space station. In addition to the weight problem, this many HTDLC filters will slow down the transient response of the total power system. Therefore, the next step in our research is to learn the extent of the weight and transient problems and to determine alternative solutions to the distortion problems.

Power Quality as a Load Management Tool for Space Station

Figure 12 is a simplified electrical schematic of one section of the present space station power management and distribution system (except for the HTDLCs). Each load in the system is connected to the Power Distribution Control Unit (PDCU) through a Remote Power Controller (RPC). This PDCU can control as many as 20 different loads grouped in two sets of 10. In addition, each load can be connected to either of the two power sources through one of two power transformers and the Remote Bus Isolators (RBI). Further, each PDCU is attached to the two sources through a ring bus architecture. Thus, the system is a combination of ring bus and radial power system architectures. Finally, the entire power system will be autonomously managed by a distributed processor type computer system [7].

Using this computer system and power quality load management techniques, it may be possible to reduce the number of HTDLC filters and still maintain a "quiet" power system. The first step would be to determine the THD of each load (typically required of all flight loads at present) and then assign "clean" loads to "clean" racks or "clean" PDCUs. Once these assignments are made, then the number of HTDLC filters for these "clean" loads can be reduced or even eliminated. The final step would be to incorporate this information into the load management software in order to assure a "clean" load is never attached to a "dirty" bus (or vice-versa) except in contingency modes. Thus, the number of HTDLC filters and its associated weight savings may be reduced through normal pre-flight load characterization and load management software techniques.

CONCLUSION

The CDDF proposal to study power system control techniques in large space electrical power systems has lead to numerous projects in this area, especially the topic of power quality load management techniques. Even though the CDDF is complete, the projects started as a result of the CDDF continue forward.

The projects started for AMPS include completing construction for the second power channel and expanding the AMPS capabilities through two university grants with the University of Alabama in Huntsville and the University of Tennessee Space Institute. These grants will give AMPS a new control and monitor graphics capability and a fault monitoring and diagnosis expert system. In addition, renewed testing and new power quality load management software will be developed for AMPS.

For the 20-kHz ac power system testbed, the distortion problems are still being investigated. These projects include continued computer modeling of the HTDLC filter in order to optimize the L and C values and then constructing and testing a prototype HTDLC filter. Another project involves modeling additional loads with switching semiconductors and then determining the THD values of these loads.

After the distortion problems have been fully investigated and the need for power quality load management established, then designing and writing new load management software for the SSM/PMAD breadboard can begin.

Finally, as a result of this CDDF proposal, the need for continued study in the area of space power system automation, especially in the area of load management, has been firmly established.

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6. Biess, J. J. and Inouye, L. Y.: Bidirectional Power Driver/Receiver. Final Technical Report. NASA Contractor Report 180887, May 1988.

7. Allen, W. H.: Integrated Control of the Space Station Electrical Power System. IECEC Conference Proceedings, 1988.

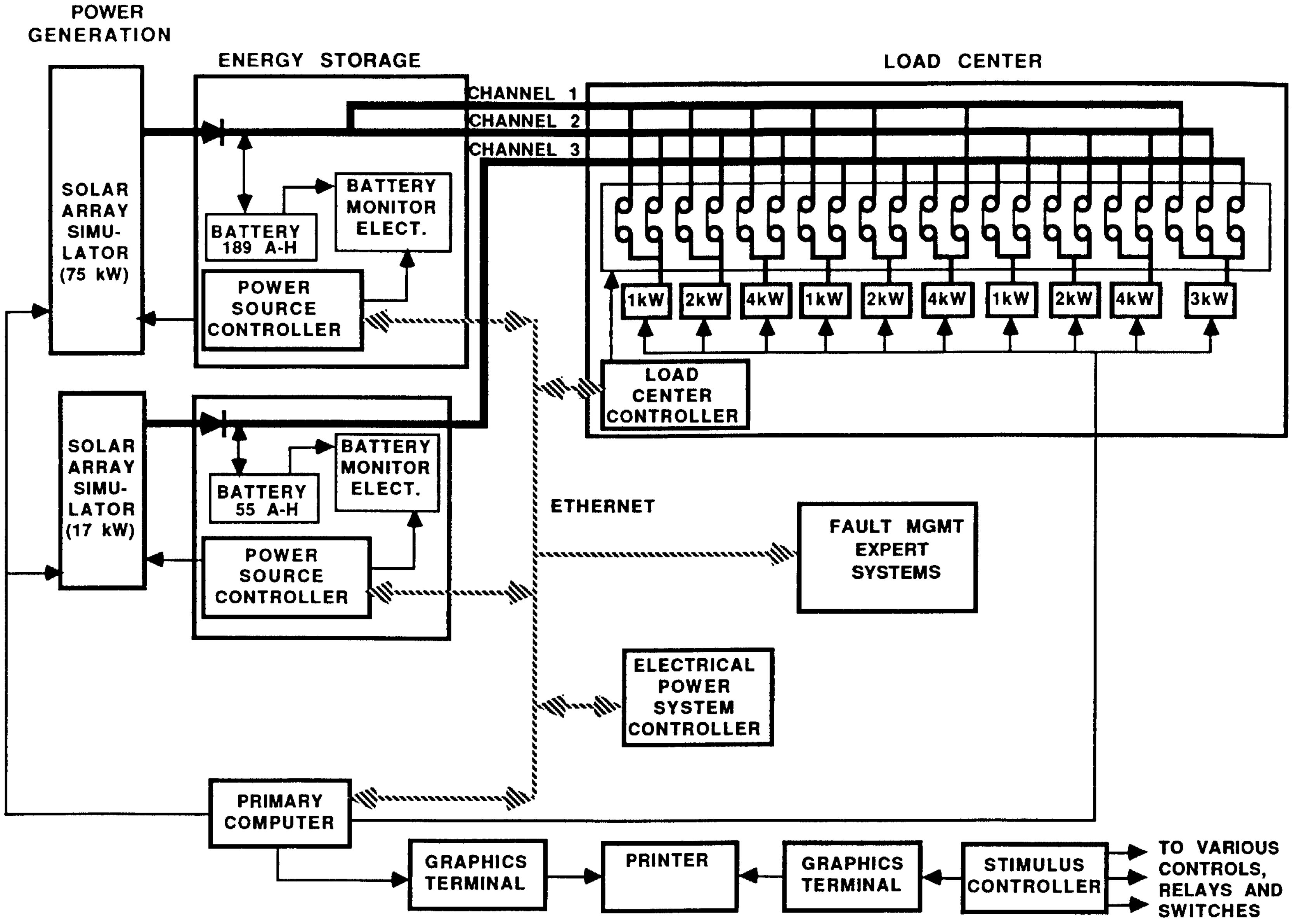

Figure 1. The Autonomously Managed Power System.

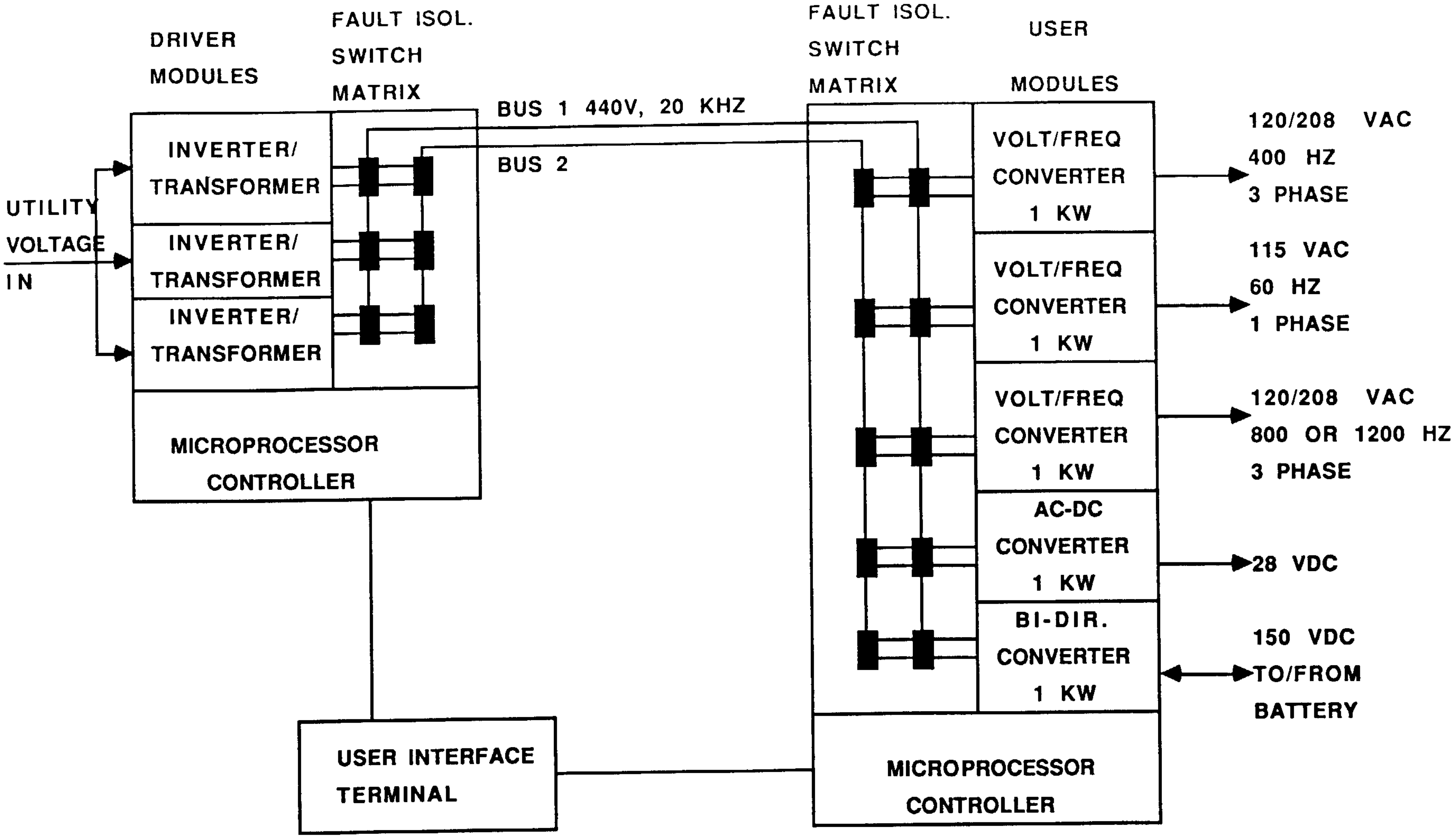

Figure 2. The 20-kHz ac power system testbed.

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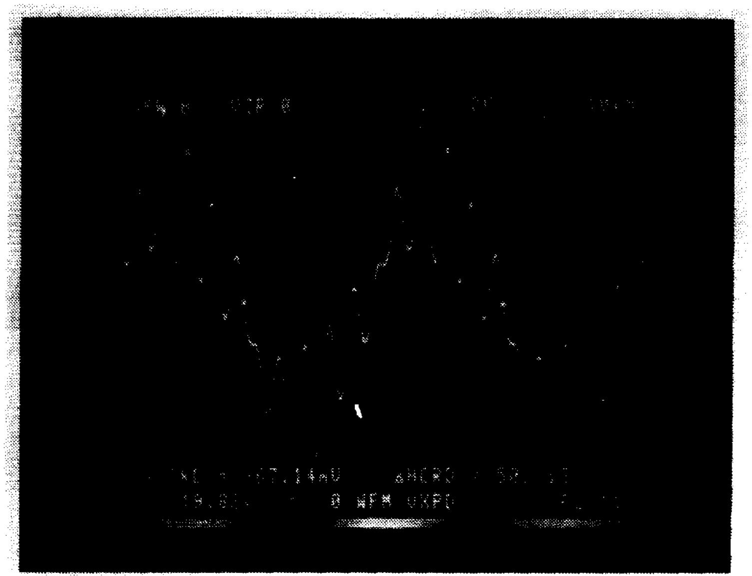


Figure 3. Source end to a 50-m cable (1 kW load).

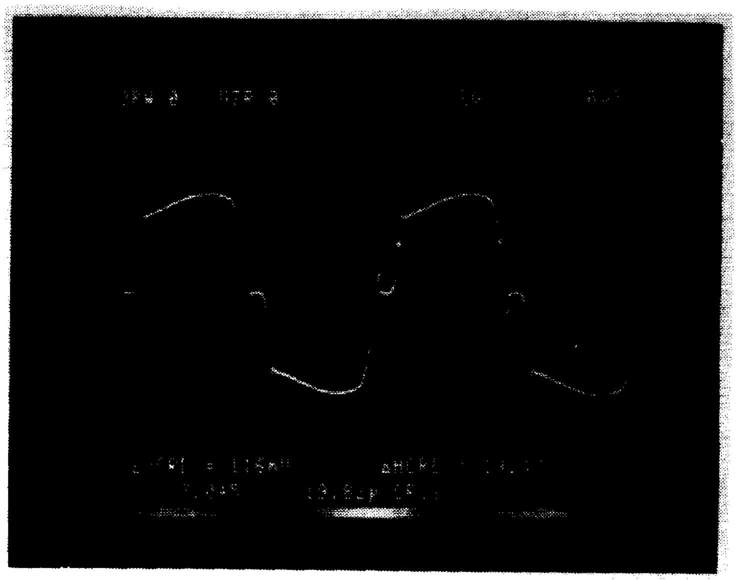
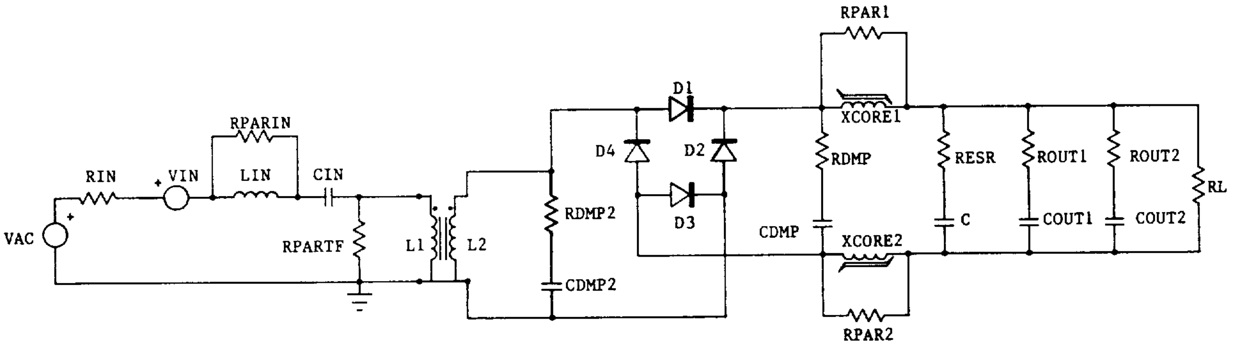
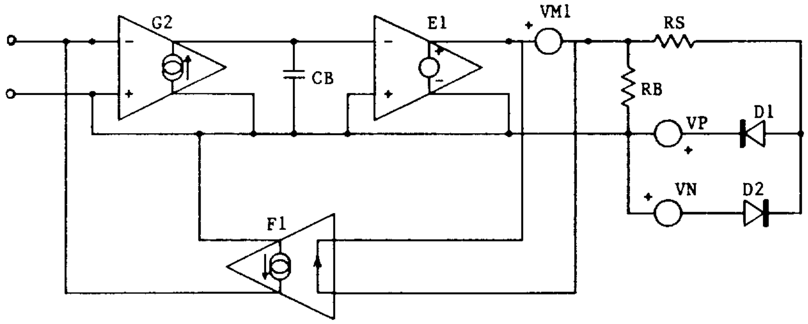


Figure 4. +28 Vdc load end of a 50-m cable (1 kW load).



TRF ELECTRICAL SCHEMATIC



XCORE SUBCIRCUIT

```
TRANS. RECT. FIL. with SAT. IND. (5 A)
VAC 1 0 SIN(0 294 20K)
VIN 4 12 DC
RIN 1 4 .09
LIN 12 13 99UH IC=100UA
RPARIN 12 13 1900
CIN 13 2 0.3943UF
L1 2 0 7.7M IC=100UA
L2 3 0 4.772M IC=100UA
RPARTF 2 0 5700
K1 L1 L2 .999643
RL 8 25 30
D1 3 7 DPWR
D2 0 7 DPWR
D3 6 0 DPWR
D4 6 3 DPWR
RPAR1 7 8 1600
XCORE1 7 8 50 CORE1
RESR 8 9 2.5
RDMP 7 10 200
COUT1 14 25 14UF IC=150V
COUT2 15 25 98UF IC=150V
ROUT1 8 14 .25
ROUT2 8 15 .25
RDMP2 3 11 200
CDMP2 11 0 2NF
CDMP 10 6 2NF IC=150V
C 9 25 600UF IC=150V
XCORE2 25 6 51 CORE2
RPAR2 25 6 2300
.MODEL DPWR D RS=.01 IBV=80UA
+TT=200NS N=1.75 CJO=5PF
.TRAN .1US 2.6MS 2.5MS UIC
.FOUR 20KHZ I(VIN)
.PRINT TRAN V(8,25) I(VIN)
.OPTIONS LIMPTS=50000 RELTOL=.001
+ITL5=500000 ITL4=10 ABSTOL=1U
```

```
*SATURABLE INDUCTOR (6T ON 4 T-31'S)
 .SUBCKT CORE1 1 2 3
 RX 3 2 1E12
 CB 3 2 3.776MF IC=0
 F1 1 2 VM1 1
 G2 2 3 1 2 1
 E1 4 2 3 2 1
 VM1 4 5
 RB 5 2 .212
 RS 5 6 42U
 VP 7 2 DC -.6548
 D1 6 7 DCLAMP
 VN 2 8 DC -.6548
 D2 8 6 DCLAMP
 .MODEL DCLAMP D
 .ENDS
*SATURABLE INDUCTOR (39T ON 55090-M4)
 .SUBCKT CORE2 1 2 3
 RX 3 2 1E12
 CB 3 2 16.69MF IC=0
 F1 1 2 VM1 1
 G2 2 3 1 2 1
 E1 4 2 3 2 1
 VM1 4 5
 RB 5 2 7.847M
 RS 5 6 131U
 VP 7 2 DC -.72
 D1 6 7 DCLAMP
 VN 2 8 DC -.72
 D2 8 6 DCLAMP
 .MODEL DCLAMP D
 .ENDS
 .END
```

Figure 5. Transformer rectifier filter electrical schematic.

TRF with SATURABLE INDUCTORS

10A OUTPUT

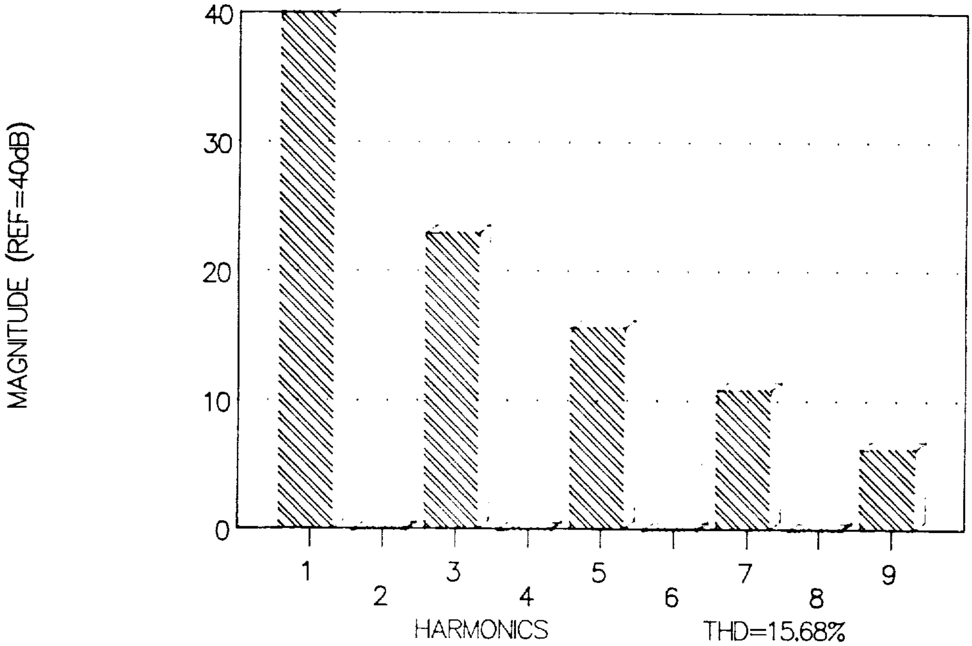


Figure 6. SPICE Fourier analysis (10-A load).

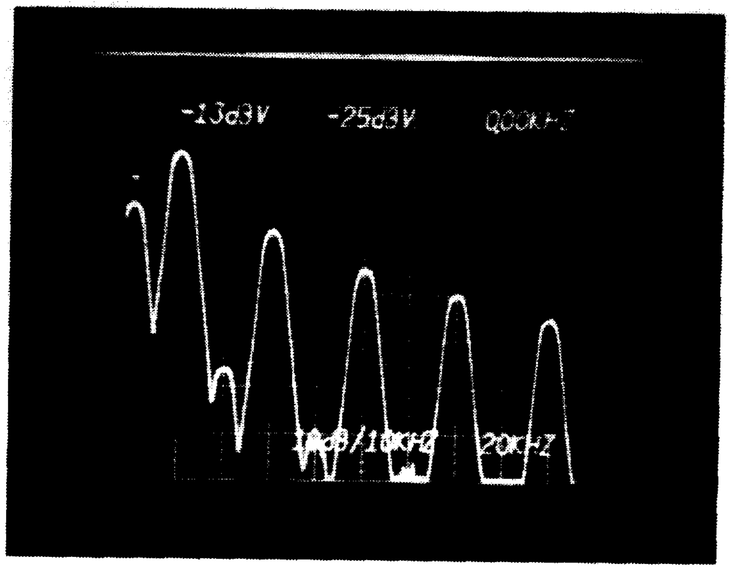
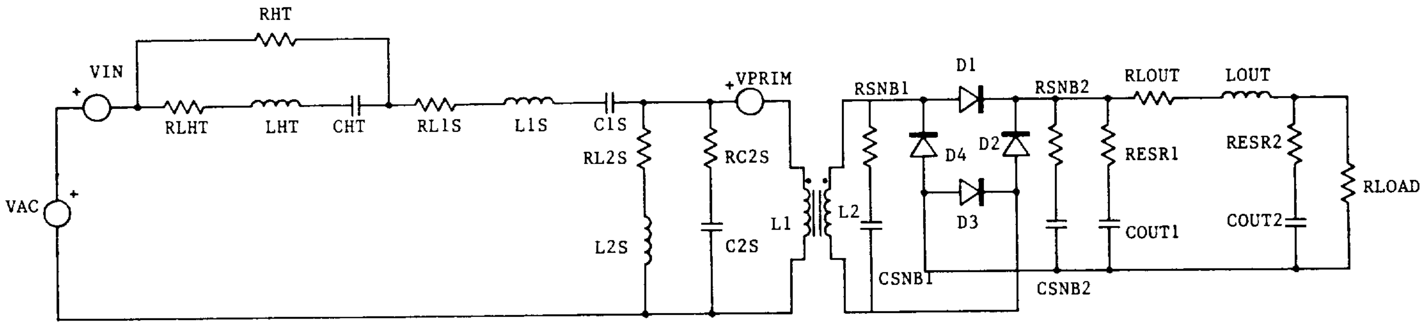


Figure 7. Actual spectrum analysis (10-A).
(20 kHz/div.), (10 dB/div.).



```
HARMONIC TRAP/DOUBLE LC with PEAK - 10A (settling time)
VAC 1 0 SIN(0 294 20K)
VIN 1 2 DC
RLHT 2 3 .01
LHT 3 4 63.3UH IC=100UA
CHT 4 5 1UF
RHT 2 5 5
RL1S 5 6 .01
L1S 6 7 63.3UH IC=100UA
C1S 7 8 1UF
RL2S 8 9 .005
L2S 9 0 63.3UH IC=100UA
RC2S 8 10 .005
C2S 10 0 1UF
VPRIM 8 15 DC
L1 15 0 7.7M IC=100UA
L2 16 0 2.115M IC=100UA
K1 L1 L2 .999643
D1 16 17 DPWR
D2 0 17 DPWR
D3 18 0 DPWR
D4 18 16 DPWR
RSNB1 16 19 200
CSNB1 19 0 2NF
RSNB2 17 20 200
CSNB2 20 18 2NF IC=140V
RESR1 17 21 .1
COUT1 21 18 200UF IC=140V
RLOUT 17 22 .005
LOUT 22 23 2UH IC=10A
RESR2 23 24 .1
COUT2 24 18 200UF IC=140V
RLOAD 23 18 14
.MODEL DPWR D RS=.01 IBV=80UA TT=200NS N=1.75 CJO=5PF
.TRAN 3US 3.0MS 0MS UIC
.FOUR 20KHZ I(VIN) I(VPRIM)
.PRINT TRAN V(23,18) I(VIN) I(VPRIM)
.OPTIONS LIMPTS=50000 RELTOL=0.001 ITL5=500000 ITL4=10 ABSTOL=1U
.END
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Figure 8. Electrical schematic for the TRF/HTDLC filter circuit.

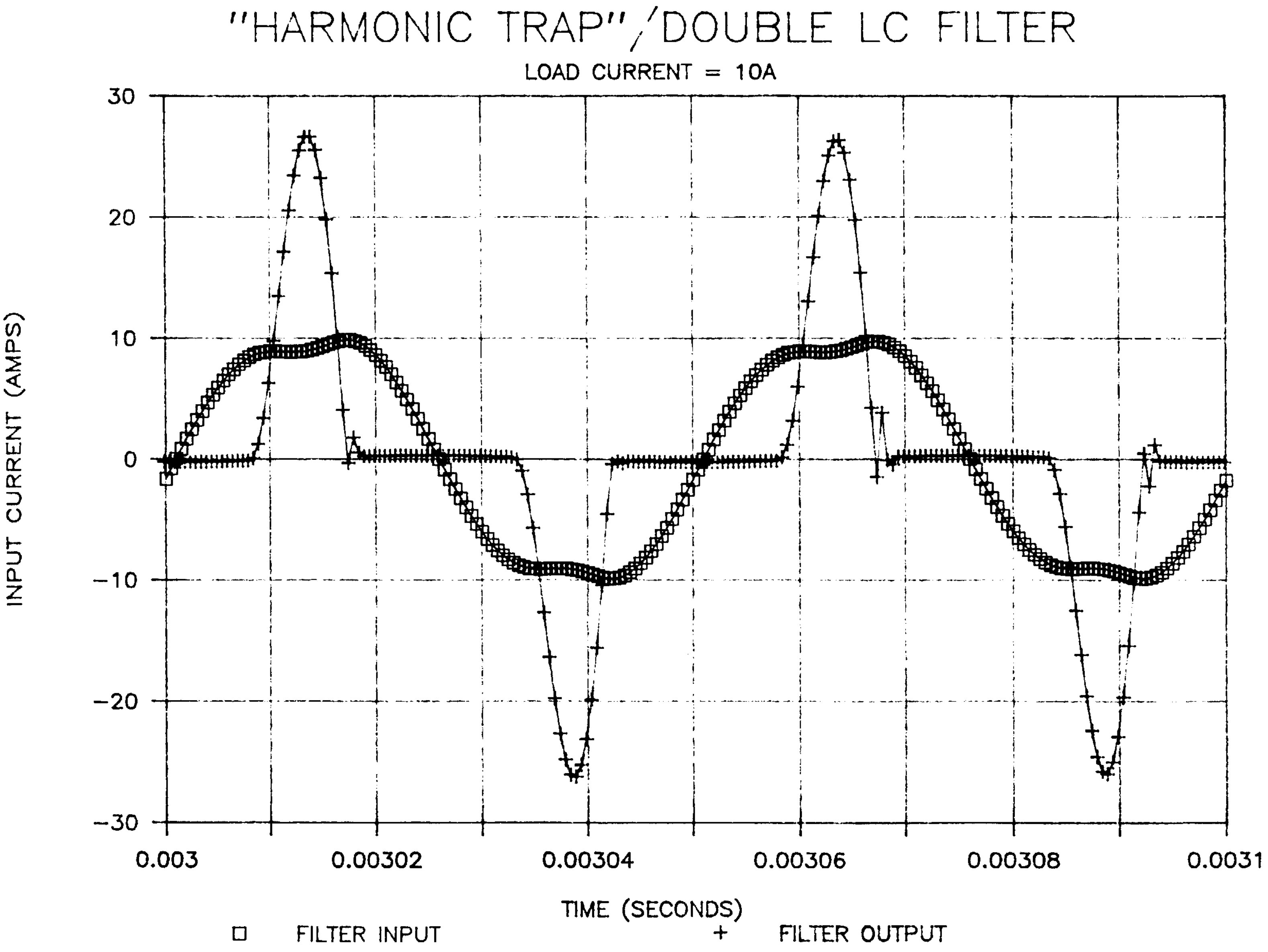

Figure 9. Input current waveforms for the HTDLC filter.

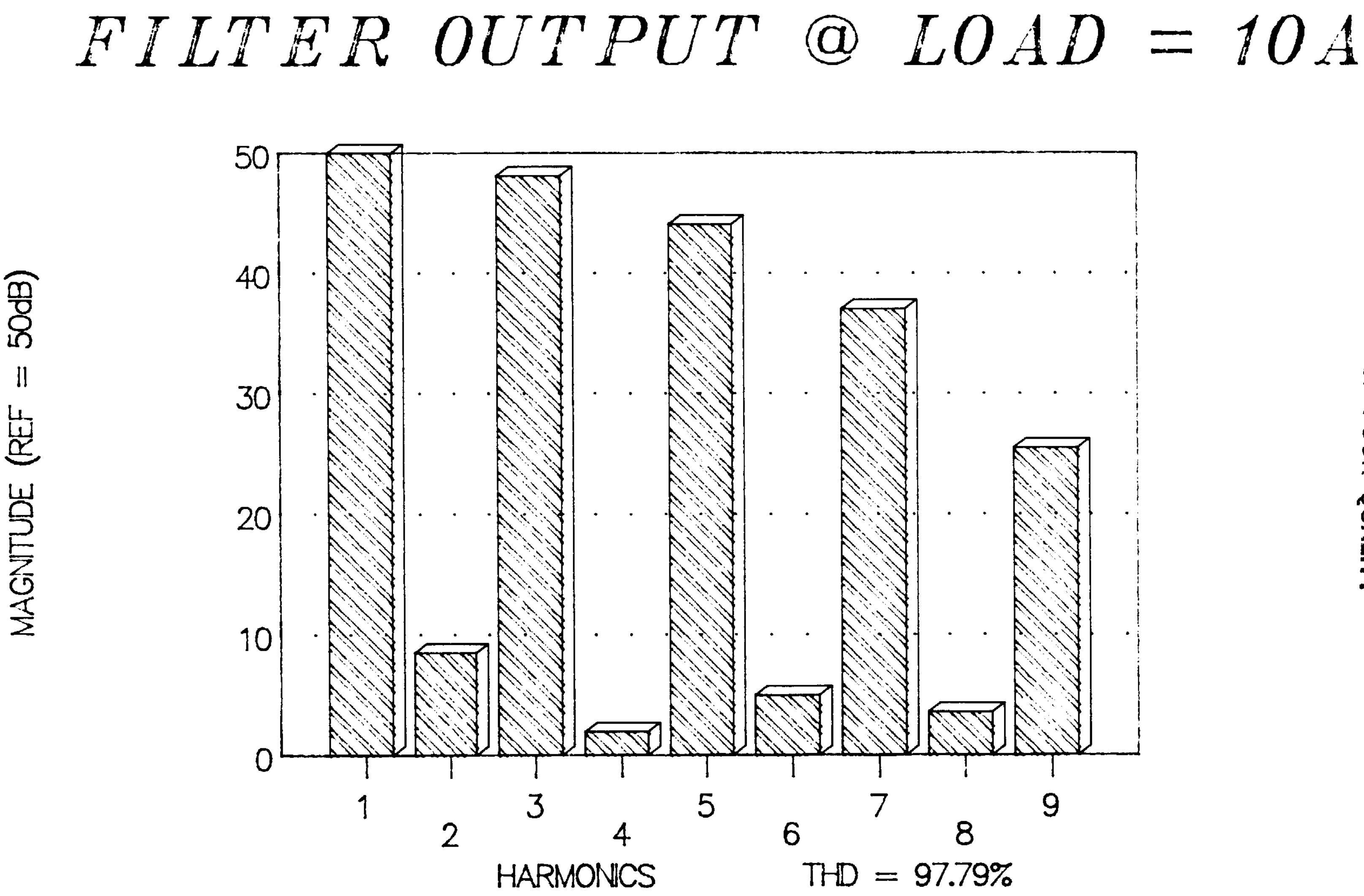

Figure 10. Input current THD (filter output) for the HTDLC filter.

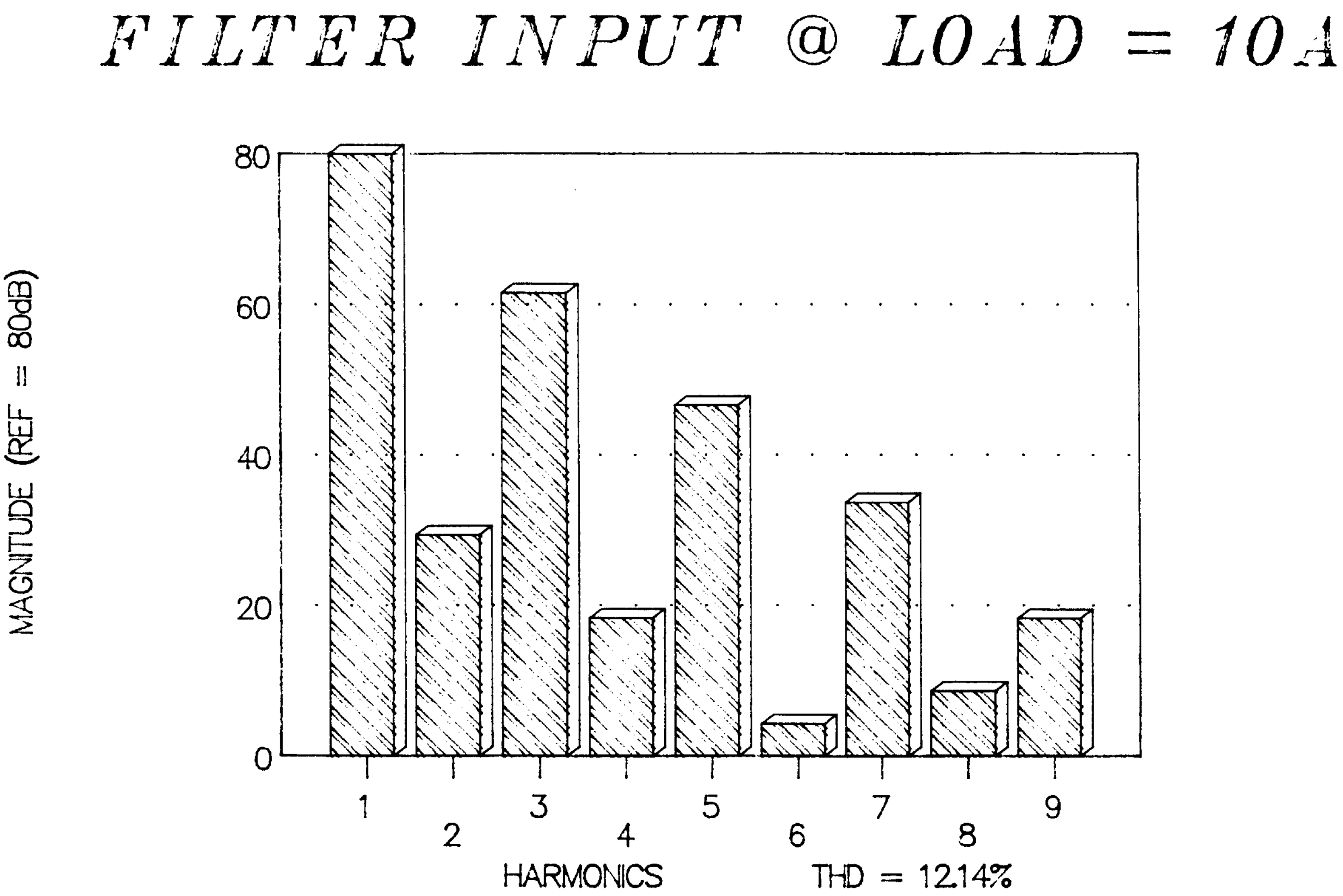

Figure 11. Input current THD (filter input) for the HTDLC filter.

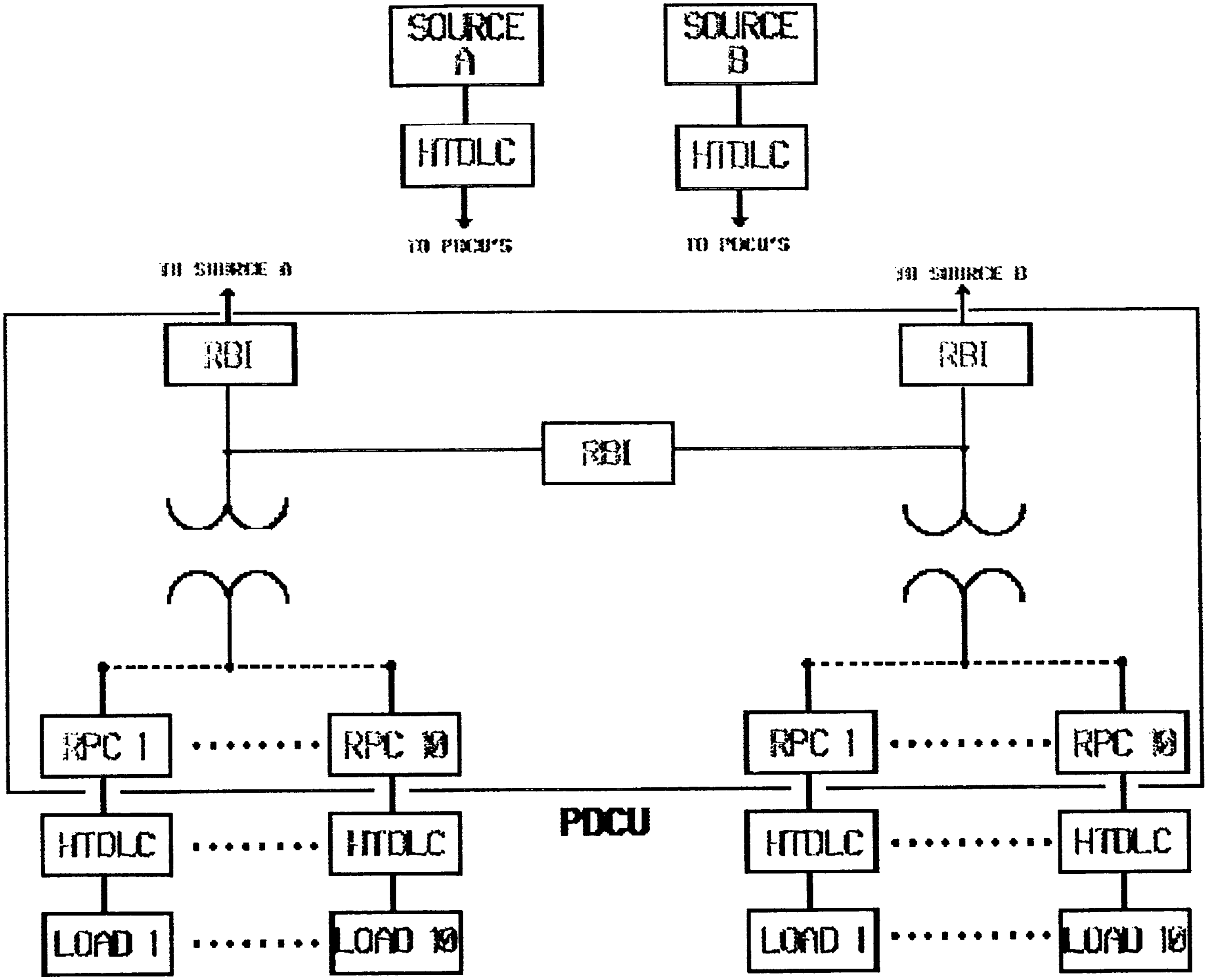

Figure 12. Simplified electrical schematic of the space station power management and distribution system.

APPROVAL

POWER QUALITY LOAD MANAGEMENT FOR LARGE SPACECRAFT ELECTRICAL POWER SYSTEMS

By Louis F. Lollar

The information in this report has been reviewed for technical content. Review of any information concerning Department of Defense or nuclear energy activities or programs has been made by the MSFC Security Classification Officer. This report, in its entirety, has been determined to be unclassified.

William B Chubb

WILLIAM B. CHUBB
Director, Information and Electronic
Systems Laboratory