NASA Contractor Report 181704

OPTICAL FIBER DATA TRANSFER SYSTEM

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Orlando, Florida

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National Aeronautics and
Space Administration

Langley Research Center
Hampton, Virginia 23665

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FINAL REPORT

1.0 INTRODUCTION

This document is the final report under contract NAS1-18331, Optical Fiber Data Transfer System (Slip Ring Replacement).

This contract was a follow up to a previous contract for basic investigation of fiber optic lateral coupling of optical energy (NAS1-17831).

This specific application of lateral coupling of optical energy is the transmission of information between relatively rotating elements of a system without physical contact. The benefits to be gained are long life, wide communication band width and low noise levels.

Under this contract a data gathering and handling system was developed along with the Optical Slip Ring itself.

The data gathering portion of the system was designed to be installed in a NASA scale-model helicopter rotor for use in wind tunnel tests.

The rotor blades of the system (built by NASA) incorporate miniature transducers. The system accepts the outputs of up to 128 transducers and converts the analog signals to 12 bit digital codes.

This is accomplished in a "beanie" mounted on the top of the rotor and rotating with it. The beanie transfers the digital data through the optical slip ring assembly to non-rotating parts of the optical slip ring. The optical slip ring assembly is located at the base of the rotor shaft. From there the "downlink" data is sent to a Local Station.

The Local Station receives the data, provides required data stream synchronization, and transmits the data to NASA recording equipment.

The data is transmitted to NASA in two ways. The first is parallel time multiplexed digital data. The second is in analog form; reconstructed transducer outputs (See Figure 1-1).

2.0 SCOPE

The primary thrust of this contract was the development of the optical slip ring. However, the data gathering to be done in the beanie presented a major challenge in terms of the number of input signals to be processed, the input signals band width, the resulting speed of 12 bit analog to digital conversion required, the serial data rate to be reliably optically transmitted through

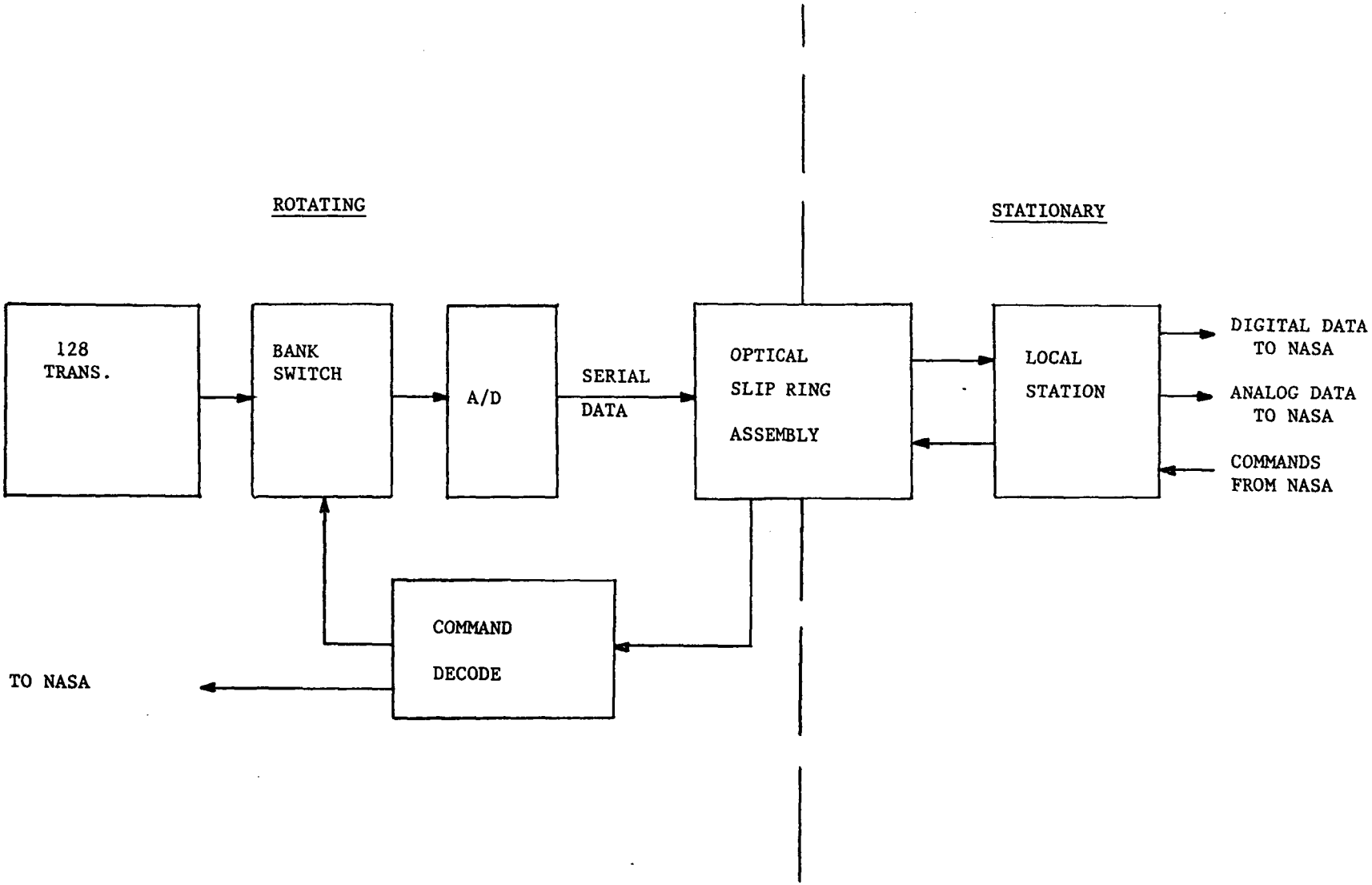

FIGURE 1-1. SYSTEM OVERVIEW

the optical slip ring, and the location and restricted volume of the beanie itself.

As a result of the above, a major portion of this report is devoted to the development of the electronics and its impact on the system configuration.

The order of presentation in this report is; first a section on the Optical Ring including a lateral optical coupling investigation carried out to extend the Phase I contract results to a practical design; second, a brief discussion of the overall system as originally conceived; third, an investigation of components to implement the original system concept; fourth, the impact of the component investigation on the system configuration; fifth, the environmental considerations and subassembly tests; sixth, final acceptance tests.

3.0 OPTICAL SLIP RING

3.1 LATERAL OPTICAL COUPLING INVESTIGATION

Under the Phase I contract the lateral optical coupling obtainable was investigated under a given set of conditions. The experimental set up used a teflon encased fiber with a 5 square millimeter detector almost in contact with the teflon. The entire internal surrounding of the fiber other than the detector was painted flat white.

The results obtained should be regarded as typical and not definitive. A summary of the measurements results is given in Table 3-1. It is to be noted that placing a reflective element at the exit end of the fiber increased the lateral coupling by about 2 dB.

For this system, the plastic fiber used is the Poly optical Standard with an outside diameter of 0.02 inches. The operating wavelength is 830 nanometers, for which laser diodes are readily available.

Based on calculations from Table 3-1 and early experimental data, the Sharp 015 MD laser diode was selected for the optical source. This is a 30 milliwatt C.W. diode that can be operated in pulse mode. Use of the C.W. diode avoids very restrictive duty cycle limitations of pulse diodes. The thirty milliwatts rating provides a generous safety margin over the anticipated 15 to 20 milliwatts peak power operation.

In the optical slip ring design the plastic fiber is coiled in a slot around the inner surface of a rotating cylinder. The inside diameter of the rotating cylinder was estimated to be 1.4 inches. The outside diameter of a suitable detector is about 0.36 inches. The detector is placed within the rotating cylinder to receive laterally coupled energy from the plastic fiber. Leaving 0.005 to 0.010 inches mechanical clearance between the

Table 3-1

SUMMARY OF FIBER PERFORMANCE DATA

WAVELENGTH = 904 nm

FIBER TYPE	ATTEN. dB/ft.	LATERAL ACCEPT. dB down from laser power	LATERAL EMISS. dB down from power in fiber
Polyoptical	*	-56.7 **	-37.2 **
PEM		-42.5	-27.25
Mitsubishi SH	*	-42.7 ∮	-23.5 ∮
Polyoptical	-2 typ.	-48.8	-39.1
"STD"	-1.83 min.obs.	-45.1	-26.3

WAVELENGTH = 852 nm

Polyoptical	-0.9	-39.3	-35.4
PEM		-33.06	-20.7
Mitsubishi SH	-1.0	-38.4 ∮	-27.1 ∮
Polyoptical	-1.27	-43.4	-39
"STD"		-37.2	-25.4

NOTES:

Where two figures are shown, the lower figure is for a point close to fiber end, and upper figure is for observed minimum remote from end.

Attenuation data are for lengths of fiber without significant faults.

Data should be considered as typical only. Acceptance and emission will vary with coupling devices used.

* Methyl Methacrylate fibers fail to guide 904 nm radiation with any reasonable efficiency.

∮ Near fiber end only. Cannot strip black plastic jacket for long distances without damage to fiber cladding.

** Short lengths. Data not reliable, but probably typical.

detector edges and the rotating cylinder places the front surface of the detector about 0.03 inches from the plastic fiber. Recessing the plastic fiber in its slot by 0.01 inches for mechanical protection increases the detector front surface to plastic fiber distance to 0.04 inches.

The detector active surface is recessed (for manufacturing reasons) about 0.09 inches below the detector front surface.

The total distance from detector active surface to plastic fiber surface (actually to the teflon tubing surface) is about 0.13 inches.

Questions to be answered in the investigation include:

What is the effect of detector active area size?

What is the effect of detector active surface to plastic fiber spacing?

What is the effect of using multiturns of plastic fiber in the slot (more than one turn of plastic fiber around the rotating cylinder inner surface)?

What is the effect of displacement of the detector along the axis of the rotating cylinder; displacement at right angles from the plane of the slot containing the plastic fibers?

What is the effect of rotating the outer cylinder (rotating the plastic fiber "ring")?

For ease of adjustment and measurement, the relationship of the plastic fiber and the detector were reversed. The plastic fiber was wound in a slot on the outside diameter of a rotatable cylinder. The detector was mounted on a stationary cylinder placed over the rotating cylinder. Figure 3-1 is a sketch of this set up.

To perform the experiments a laser diode was 100% modulated with a low frequency square wave. The optical output was directly coupled to the plastic fiber. Approximately three feet of plastic fiber was used. The exit end of the plastic fiber was monitored to determine the peak optical energy "in" the plastic fiber. All results would then be normalized to a given optical energy level "in" the plastic fiber. During measurements, the exit end of the plastic fiber was covered with a reflective material. This increased the signal output by about 2 dB.

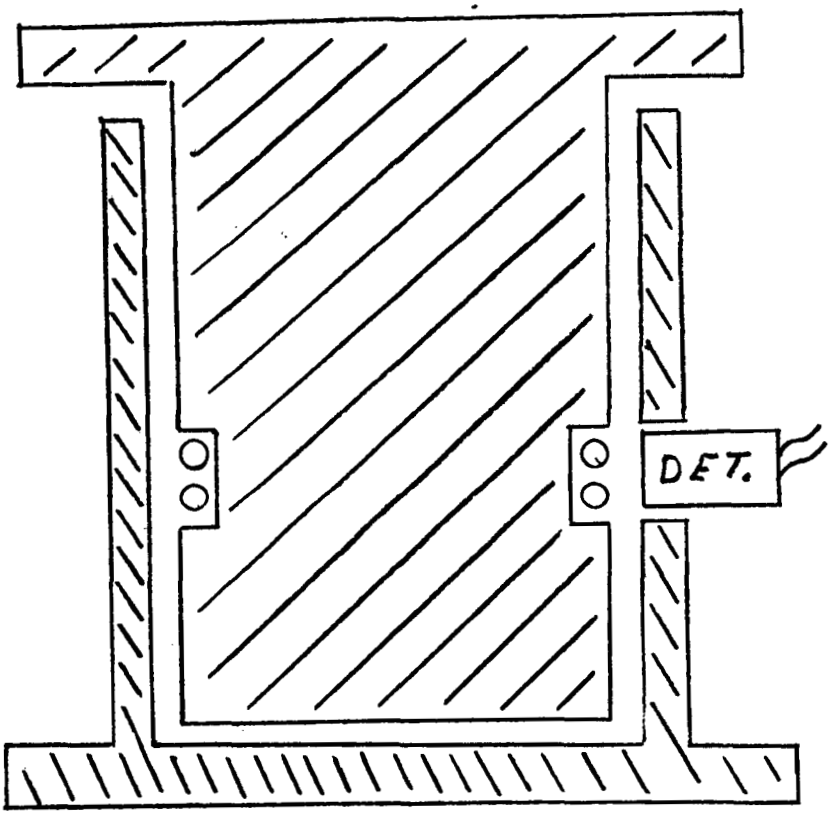

Figure 3-1. Schematic-Fiber Optic Lateral Coupling Test Fixture

The detectors used were EGG HFD 1100 and EGG HFD 1060 with 5.1 square millimeter and 1.5 square millimeter active areas respectively.

The detectors contain a transimpedance amplifier. The feed back resistor used was 100 killohm. The input signal current is the output voltage signal divided by 100,000. The optical energy on the detector active surface can then be calculated from the known response of the photodiode at 830 nanometers (approximately 0.57 amps/watt).

The effect of the transimpedance amplifier rise and fall time was eliminated by the use of low frequency (1 to 10 KHz) modulation of the laser source. The input power to the fiber was in the order of 8 milliwatts.

Extreme accuracy of measurement was not a requirement. Most of the measurements are relative in nature. Where absolute values are involved, an accuracy of $\pm$ 1 dB was considered sufficient for this preliminary work. Nevertheless, reasonable tracking of results from setup to setup was expected. This did not prove to be the case. Whenever the setup involved handling or changing the plastic fiber, the resulting measurements were very inconsistent. This will be discussed later.

As a result of the above, absolute values can not be taken too seriously. The data is still valuable on a relative basis.

In the data presented below R stands for radius and is the radius of the bottom of the slot holding the teflon encased plastic fiber. The "fiber surface" is actually the surface of the teflon tubing encasing the plastic fiber.

Figure 3-2 compares the output signal from the two detectors as a function of fiber surface to detector active area. The signal outputs are the maximum obtained as a function of rotating the fiber optic "ring" with respect to the detector. Maximums occurred for both detectors in the same fiber area. Figure 3-3 is identical to Figure 3-2 except that the minimum signal outputs as a function of rotation are plotted. The data is valid since no fiber handling was involved between the two data sets.

The increased signal output from the larger detector surface is obvious. The signal change with spacing does not follow a $1/R^2$ law. The slope of the output vs. fiber surface to detective active area spacing is about four times as great for the larger detector as for the smaller detector. Thus the larger detector is more sensitive to spacing changes than the smaller detector. It is also apparent that for both detectors the maximum signal is more sensitive (by a factor of two) to spacing changes than is the minimum signal. However, in the worst case

Figure 3-2

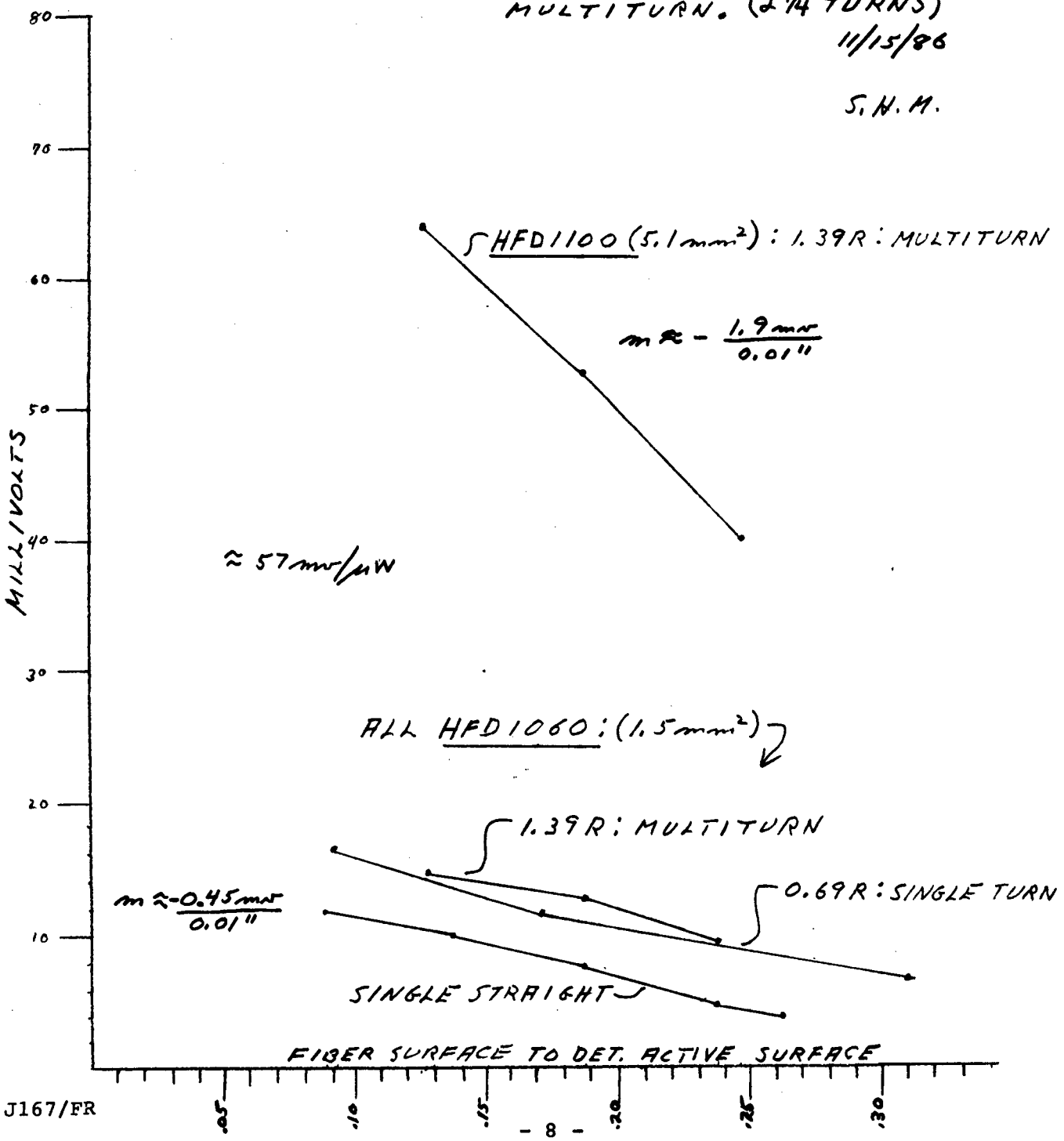

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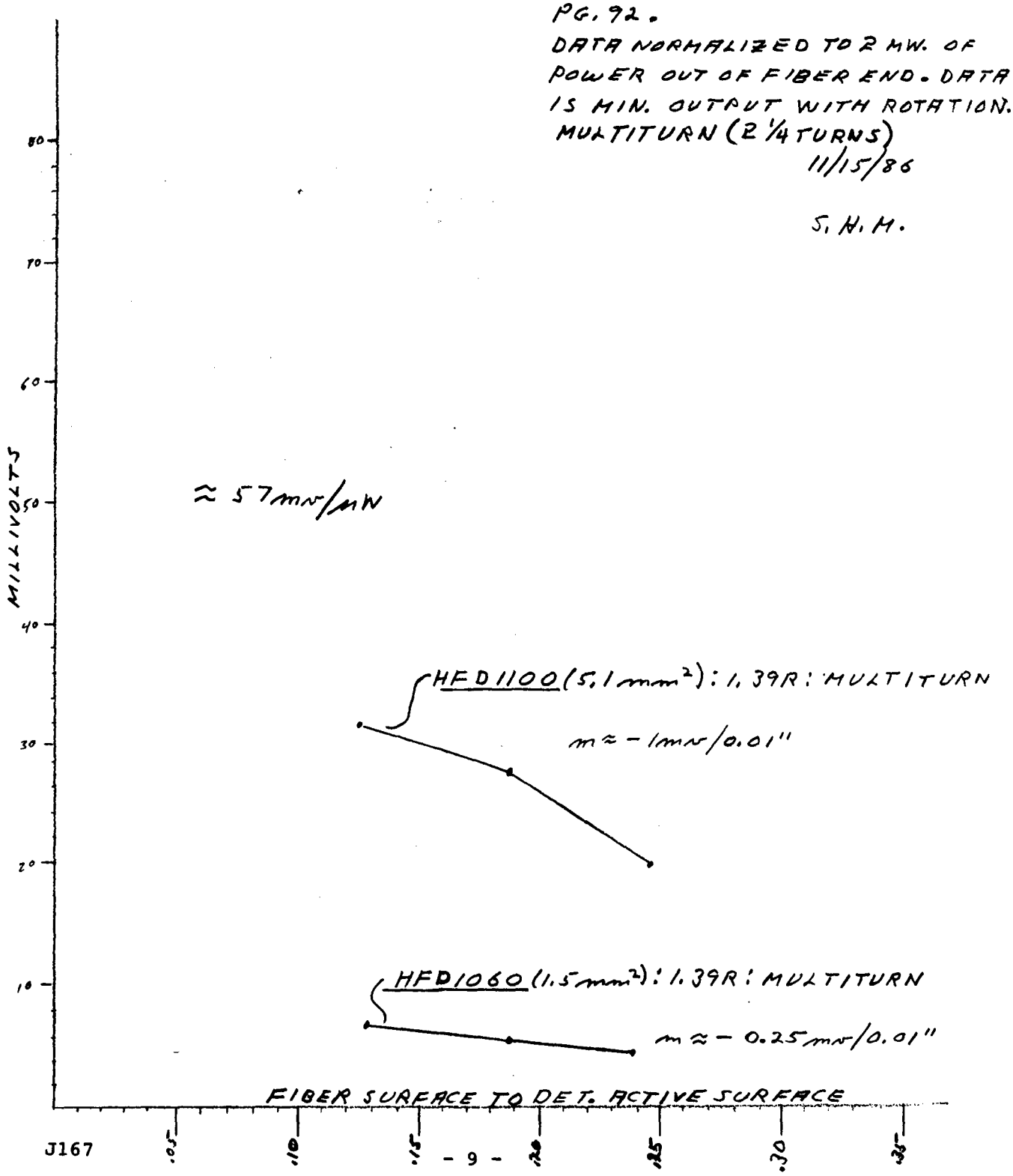
Figure 3-3



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the change in signal amplitude vs. spacing is <5% for a 0.01 inch spacing change.

The maximum to minimum signal variation as a percent of maximum is 60% for the smaller detector and 50% for the larger detector. Both represent a rather large amplitude modulation as a function of rotation.

Figures 3-4 through 3-7 indicate the effect on signal amplitude of displacement of the detector at right angles to the plane of the plastic fiber ring, at various spacings from the plastic fiber to the detector active surface.

In the worst case (Figure 3-6) the signal amplitude drops only 5% for a 0.01 inch change in detector position (up to a 0.03 inch displacemet).

The effect of displacing the detector tangentially to the plastic fiber ring was also briefly explored. For small displacements (0.01 to 0.02 inches) no significant signal amplitude change was observed. For a large displacement (in the order of 0.2 inches toward the source) the signal amplitude increased by about 50% (See Figure 3-8). This is due to the fact that optical energy escaping the plastic fiber is concentrated in a small angle essentially tangential to the fiber optic ring. The teflon tubing surrounding the fiber converts only a portion of it to right angle radiation. This phenomina was not investigated for repeatability or various mechanical tolerances. It was not used in the final optical ring design.

At this point it can be concluded that the larger detector does give a significantly larger signal than the smaller detector. Mechanical Tolerances on the detector position with respect to the fiber optic ring are not critical. The signal amplitudes are usable with further amplification prior to transmission from the optical slip ring. Signal modulation as a function of rotation would be about 50%.

It would be desirable to obtain larger signals directly from the detector and to reduce the amplitude modulation as a function of rotation.

Observation of the energy emitted from the ring showed a number of "hot spots" along the fiber. It also showed a maximum intensity where the fiber entered the slot and a low intensity where the fiber exited the slot. These locations corresponded with the maximum and minimum signals observed with rotation.

One way of moving the fiber entrance and exit points out of the detector field of view is to increase the number of turns of fiber in the ring. The slot in which the fibers are wound was therefore significantly widened to accommodate 3 turns, then four turns, and then 5 turns. The amplitude of the signals

Figure 3-4

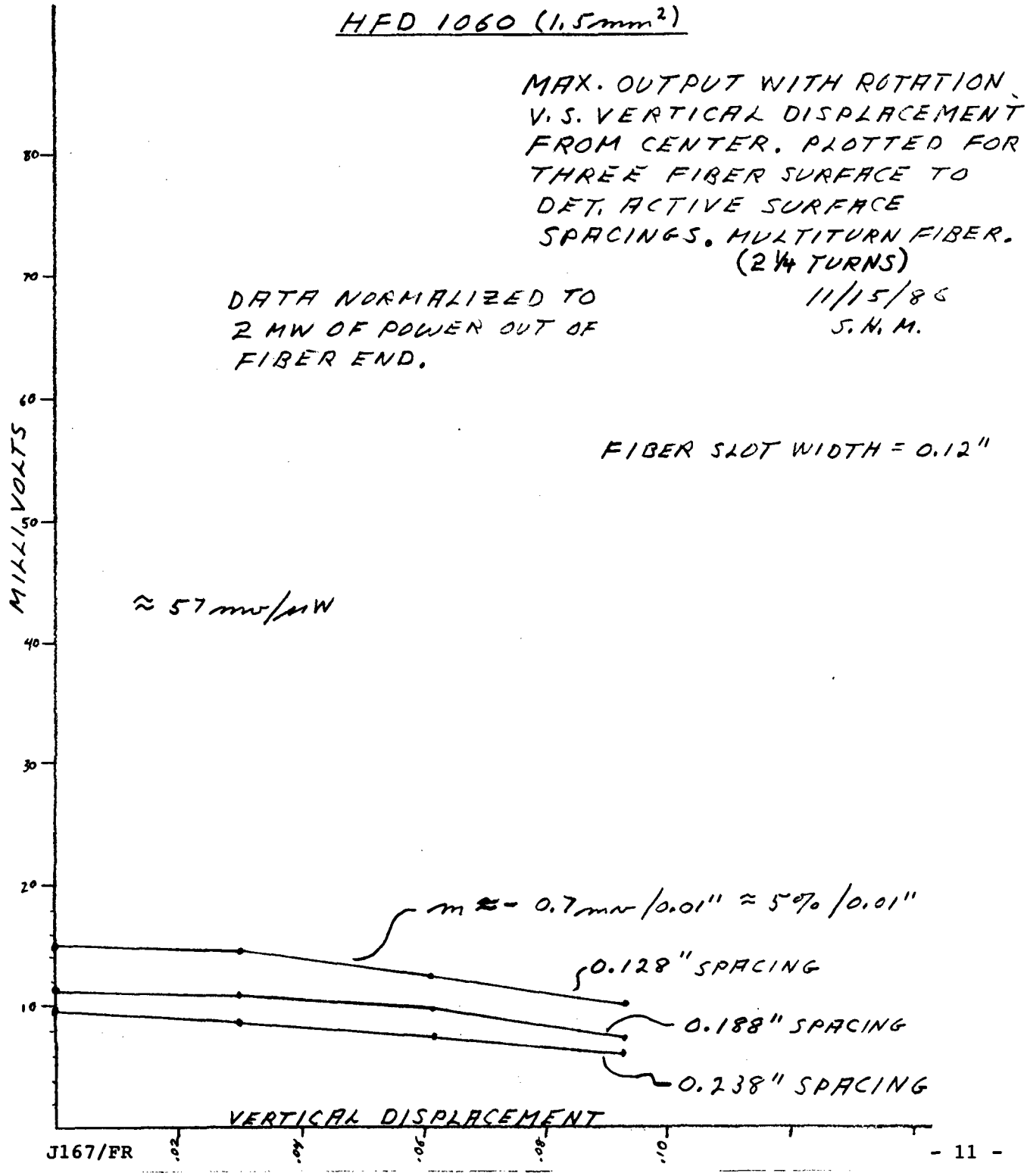
HFD 1060 (1.5mm²)
MAX. OUTPUT WITH ROTATION V.S. VERTICAL DISPLACEMENT FROM CENTER. PLOTTED FOR THREE FIBER SURFACE TO DET. ACTIVE SURFACE SPACINGS. MULTITURN FIBER. (2¼ TURNS)
DATA NORMALIZED TO 2 MW OF POWER OUT OF FIBER END.
11/15/86
S. H. M.
FIBER SLOT WIDTH = 0.12"
≈ 57 mv/μW
MILLIVOLTS
80
70
60
50
40
30
20
10
m ≈ - 0.7mv/0.01" ≈ 5%/0.01"
0.128" SPACING
0.188" SPACING
0.238" SPACING
VERTICAL DISPLACEMENT
.02
.04
.06
.08
.10

Figure 3-5

HFD 1060 (1.5 mm²)

MIN. OUTPUT WITH ROTATION V.S. VERTICAL DISPLACEMENT FROM CENTER. PLOTTED FOR THREE FIBER SURFACE TO DET. ACTIVE SURFACE SPACINGS. MULTITURN FIBER. (2¼ TURNS)

11/15/86

DATA NORMALIZED TO 2 MW OF POWER OUT OF FIBER END.

SI N. M.

FIBER SLOT WIDTH = 0.12"

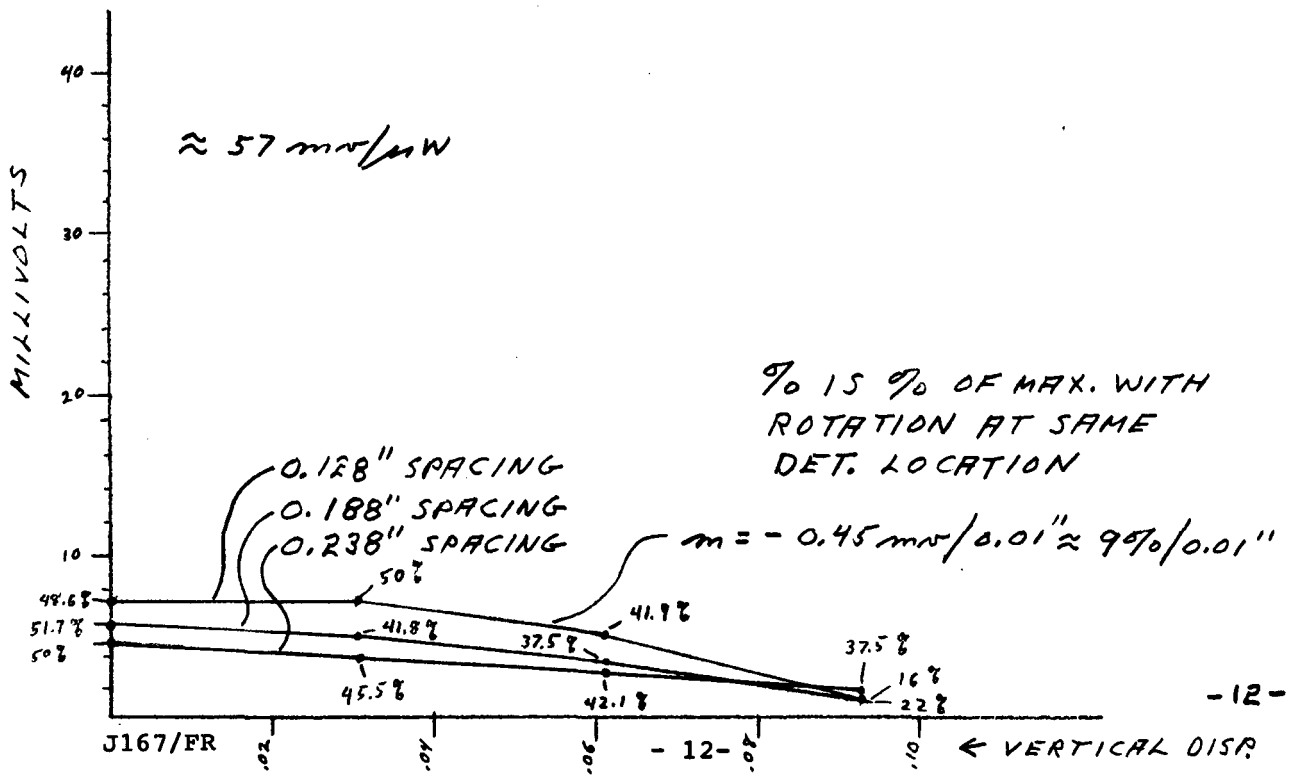

Figure 3-6

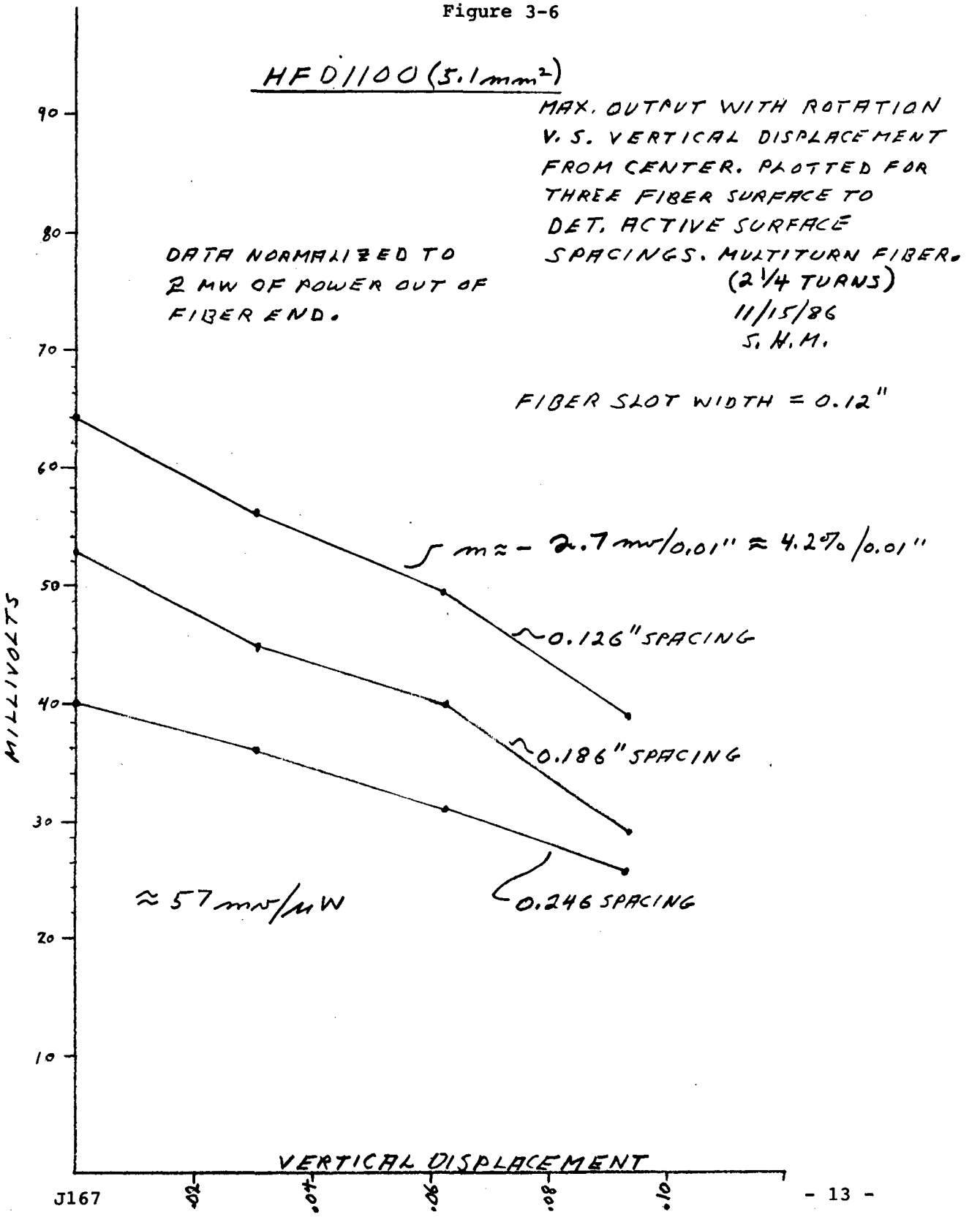

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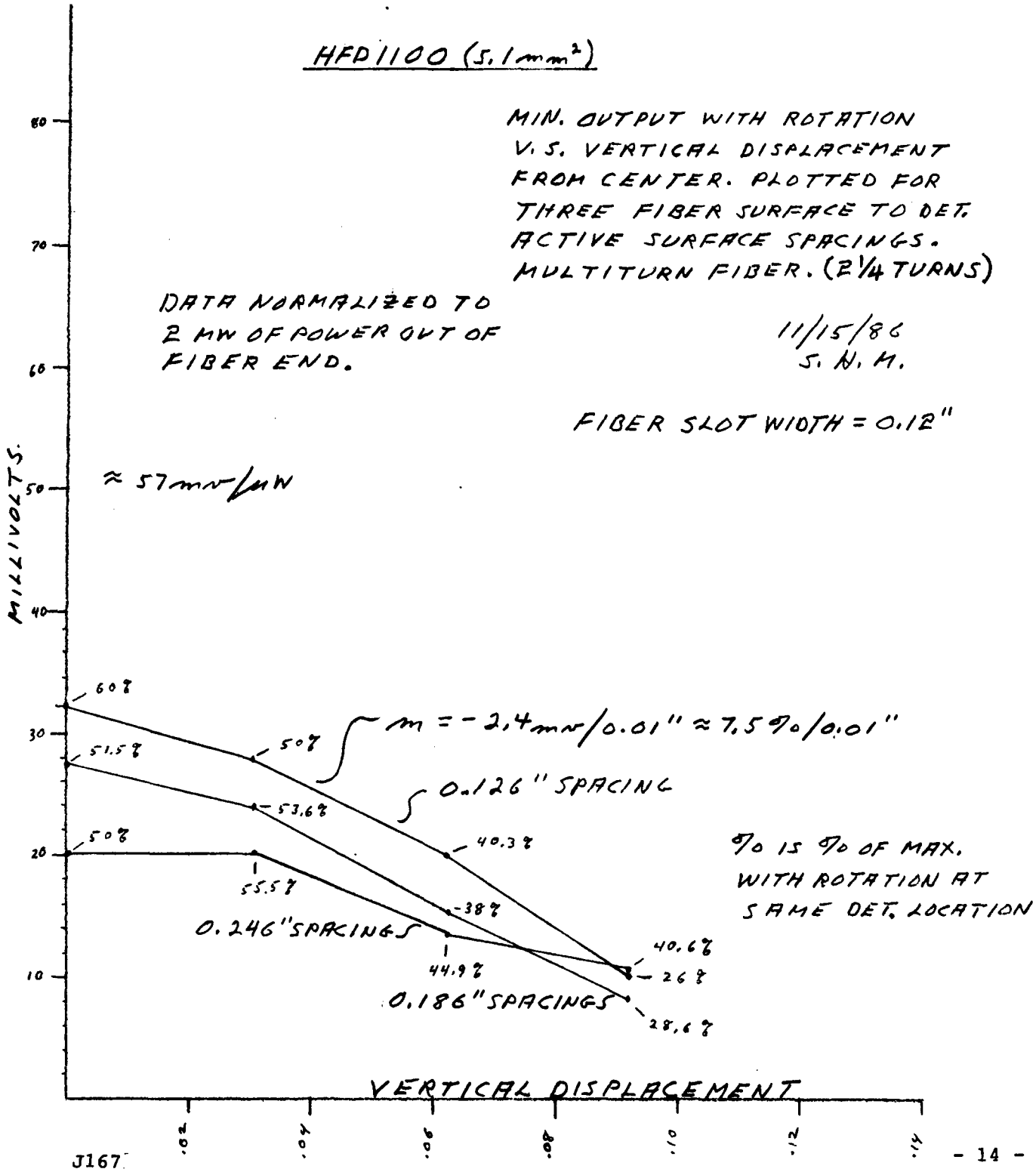
Figure 3-7



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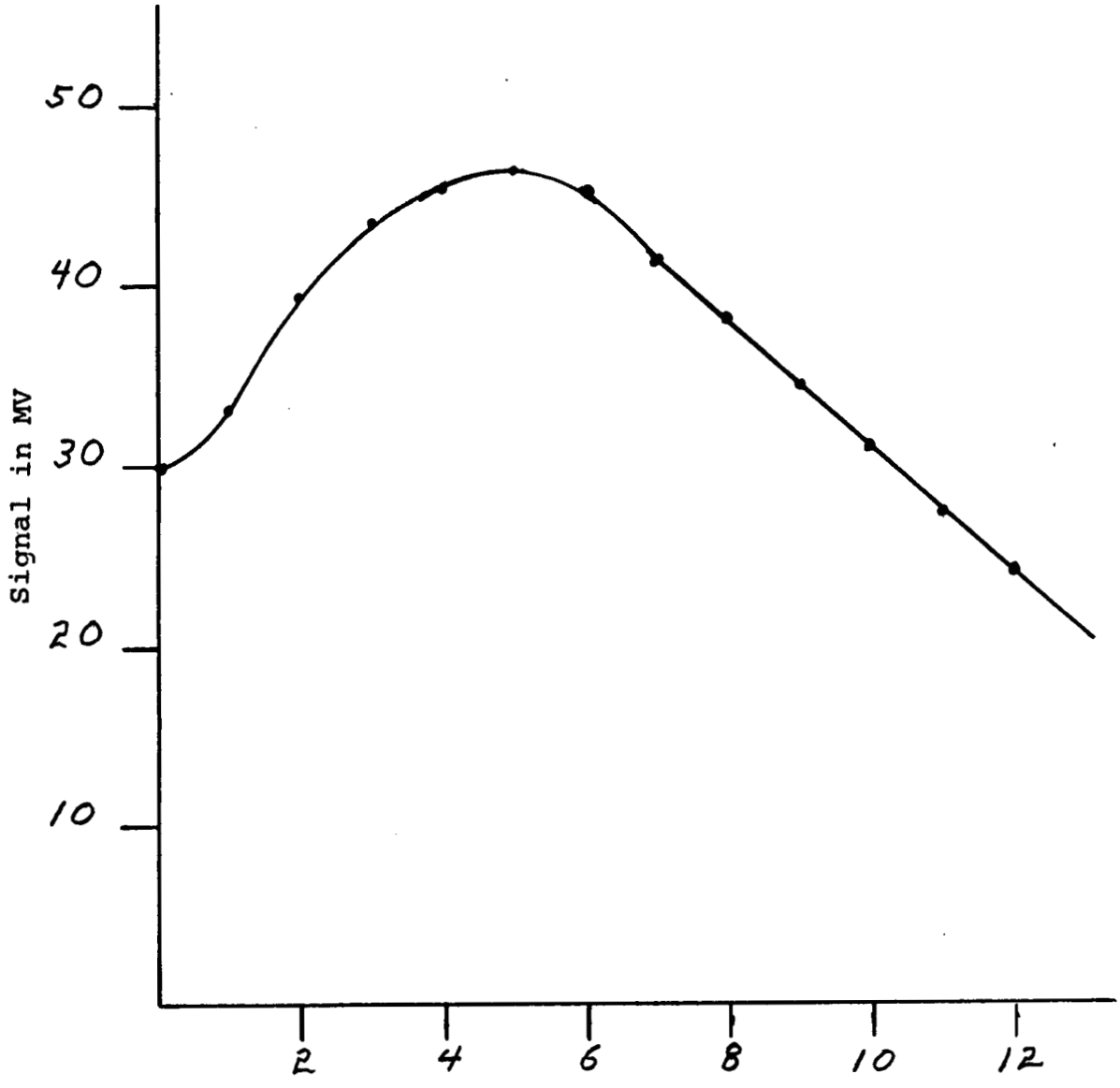

Figure 3-8. Effect of Det. Tangential Displacement

(using the larger detector) increased somewhat as the number of turns increased to four. The amplitude modulation decreased to about 30%. Five turns produced no particular improvement.

It was therefore concluded that four turns was optimum.

The question of repeatability of measurements for a given setup was then investigated. It was found that handling the plastic fiber to insert it in the teflon tubing and winding it around the ring had a large effect on the fiber attenuation. Extreme care was necessary to reduce this handling effect. Even so, the relatively sharp bends at the fiber entrance and exit points produced significant attenuation. Deliberately kinking the fiber at one point increased the attenuation by over 1 milliwatt.

This explained the large variation in lateral detected signal amplitude when the energy exiting the fiber end was used as a monitor of the power in the fiber.

The increase in fiber attenuation from handling was of course due to a change in the amount of energy escaping through the sidewalls of the fiber. The result was "hot spots" of radiation randomly occurring along the fiber length.

An increase in the amount of energy escaping the fiber is desirable if it could be controlled to provide a relatively even output signal with rotation.

Experimentation with controlled handling of the fiber produced a method of accomplishing the above. Rolling the fiber over a mandrel of approximately 1/4 inch diameter produces the desired result. Repeating the process a number of times increases the escape of energy to the point where better than 90% of the input power escapes. With reasonable care local hot spots are reduced to a minimum. Subsequent reasonable handling of the fiber has no particular effect providing sharp kinks are avoided.

With a four turn fiber optic ring constructed from the "processed" fiber, a detector signal output increase of about 10 dB was achieved with a rotation modulation of 10%.

With a detector output in the hundreds of millivolts and a small rotation modulation no further signal amplification is required for signal transmission.

In view of the handling effects on the unprocessed plastic fiber attenuation, it was clear that the plastic fiber could not be used to run up through the rotor shaft to the optical source. A transition to a glass fiber had to be incorporated in the optical ring assembly.

One further experiment was necessary before proceeding with the final mechanical design of the optical ring assembly.

With several milliwatts being emitted by the fiber rings, crosstalk between two lateral coupling channels was a potential problem.

A mechanical assembly was constructed incorporating two fiber optic rings spaced 1.75 inches apart. The two detectors were mounted facing 180 degrees from one another. The inner surface of the metal was blackened although no precautions were taken with the shiny copper clad boards mounting the detector circuitry (Figure 3-9).

No measurable crosscoupling occurred.

With all of the above information in hand the final mechanical design of the optical slip ring could proceed with confidence of success.

It is to be noted that the behavior of the "processed" plastic fiber rings was stable over several months of time, up to 58°C of temperature, and up to rotation rate of 2000 rpm.

3.2 OPTICAL SLIP RING CONFIGURATION

The number of optical channels in the optical slip ring is a function of the overall system design.

The configuration described below is the final configuration for this contract.

The optical slip ring provides two optically coupled channels from the top of the rotor shaft (the beanie) to the outside world, and one optically coupled channel from the outside world to the top of the rotor shaft. The optical coupling bridges the gap between the rotating outer cylinder and the stationary inner cylinder. Once across the gap, the optical energy is detected and passed on in the form of electrical energy.

The two optically coupled channels coming down the rotor shaft (downlink) use lateral coupling to bridge the gap. The optically coupled channel going up the shaft uses more conventional exit end coupling (noncontacting) to a detector.

No lenses are used. Figure 3-10 illustrates the general arrangement.

In addition to the optically coupled paths the ring supplies power to the beanie electronics at the top of the shaft. This is accomplished by three power slip rings in the bottom section of the ring assembly.

The optical ring assembly mounts within the bottom of the rotor shaft. The power slip ring and external connection section protruder below the bottom of the rotor shaft. In this location

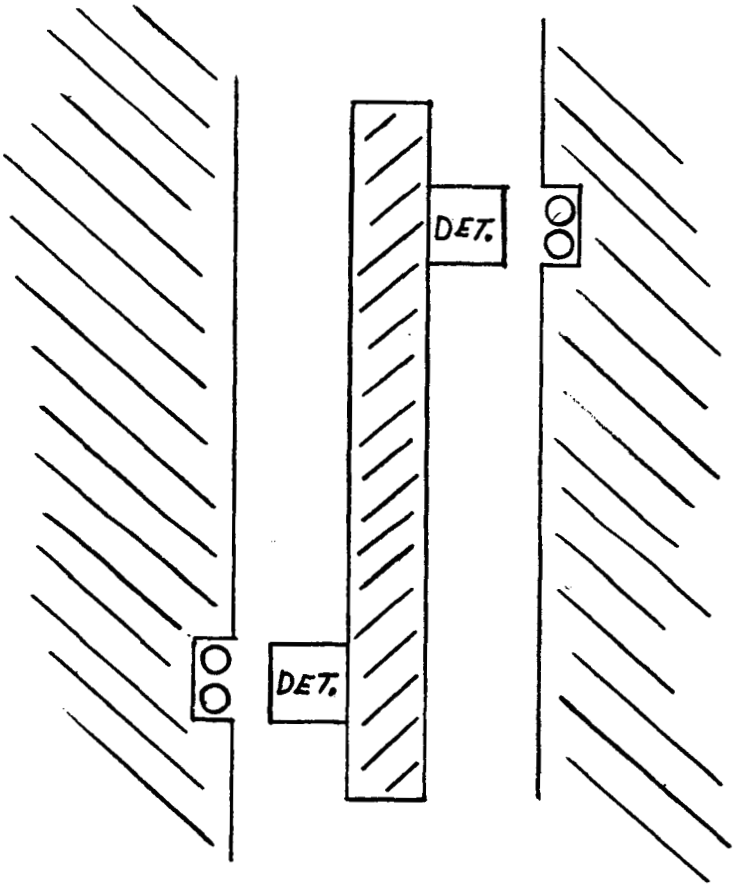

Figure 3-9. Fiber Optic Ring Cross Coupling Measurement Arrangement

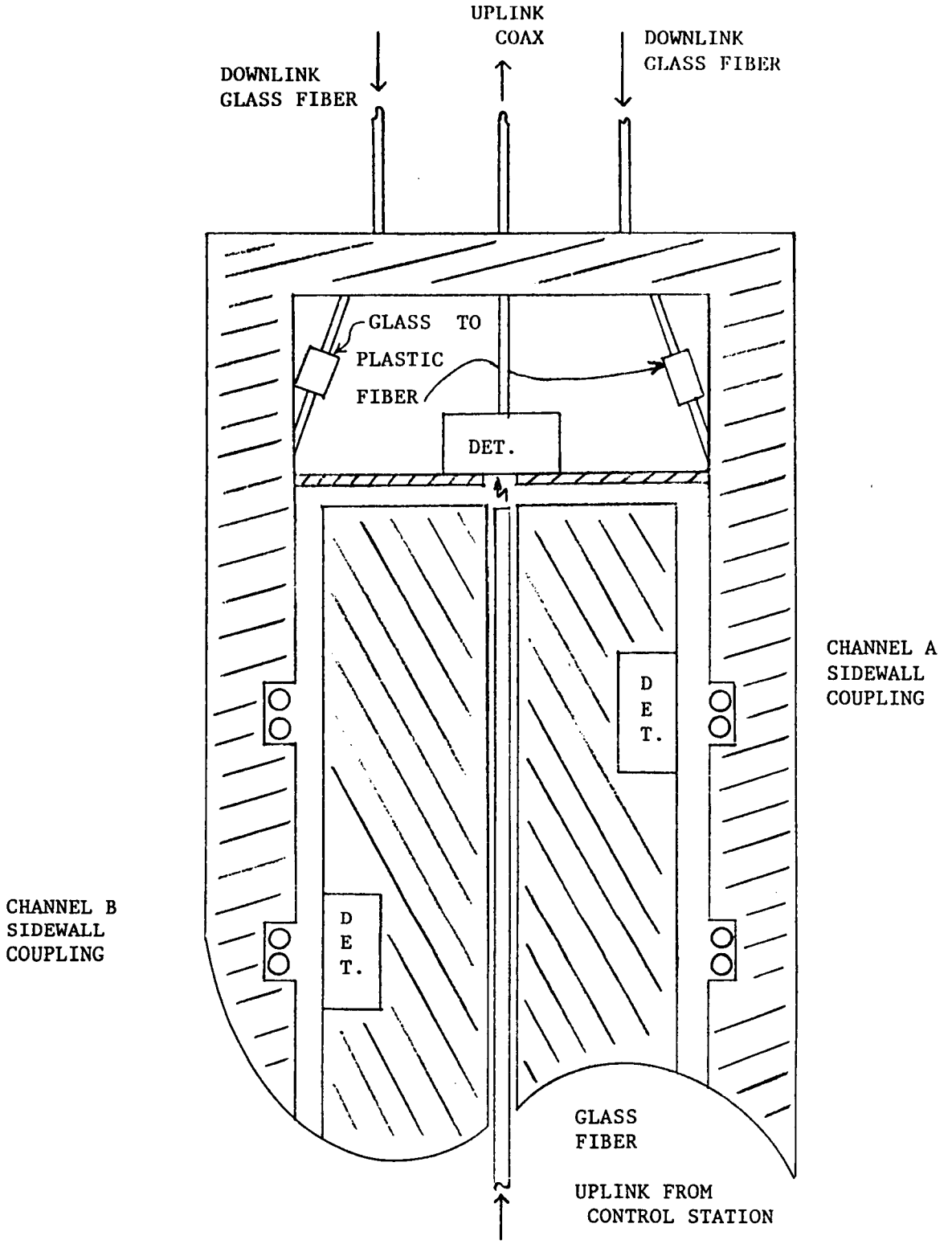

Figure 3-10. OPTICAL SLIP RING ASSEMBLY SCHEMATIC

the optical ring assembly is subjected to an environment where the ambient temperature exceeds the operating capability of the detector and of the plastic fiber (the plastic fiber softens at 71°C). Cooling of the optical ring assembly is provided for via a cooling gas entry point in the lower portion of the stationary member. The cooling gas is directed to the outside surface of the rotating member between it and the rotor shaft. The gas flows vertically over the ring assembly surface and up the rotor shaft. A shield is placed over the assembly for mechanical protection of exposed plastic fiber.

Figure 3-11 shows the optical ring assembly.

Figures 3-12, 3-13, and 3-14 show details of the detectors, plastic fiber routing, power routing, cooling ports, slip rings, etc..

As a result of the experimental work on detector positional accuracy requirements, no tight tolerances are required in the mechanical design. Standard sealed bearings are used. The assembly is constructed of stainless steel except for the power brush holder which is of plastic. The outer (rotating) shell is split into top and bottom sections. This provides access to the inner surface slots for ease of installation of the plastic fiber for lateral optical coupling.

The plastic fiber providing the lateral optical coupling mates to a glass optical fiber at the top of the assembly. This avoids installation and removal handling problems with plastic fiber.

The lateral coupling detectors are positioned to provide a 0.005 inch mechanical clearance to the rotating outer structure. The outer surface of the rotating structure is ribbed in the vertical direction. This provides space for the cooling gas flow between the shield and the assembly itself.

4.0 ORIGINAL SYSTEM CONCEPT

The purpose of the system is to collect and transfer 128 signals from the top of the rotating shaft to the stationary outside world, and to relay the information to NASA instrumentation.

The manner in which this is accomplished has a large impact on the size and power requirements of the electronic package mounted on top of the rotor shaft.

Basic system requirements include the handling of 128 signals, a signal bandwidth of 20 KHz, transmission of the data on 128 signals to NASA in 12 bit digital form, and transmission of the data on a selectable group of eight signals to NASA in reconstructed analog form.

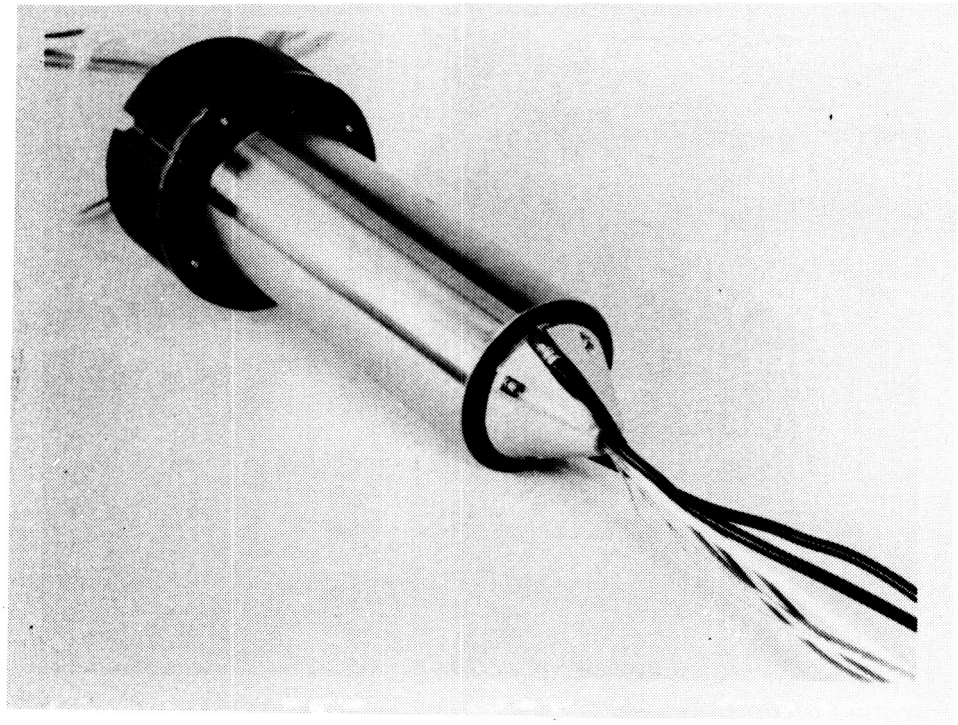

Figure 3-11. Optical Ring

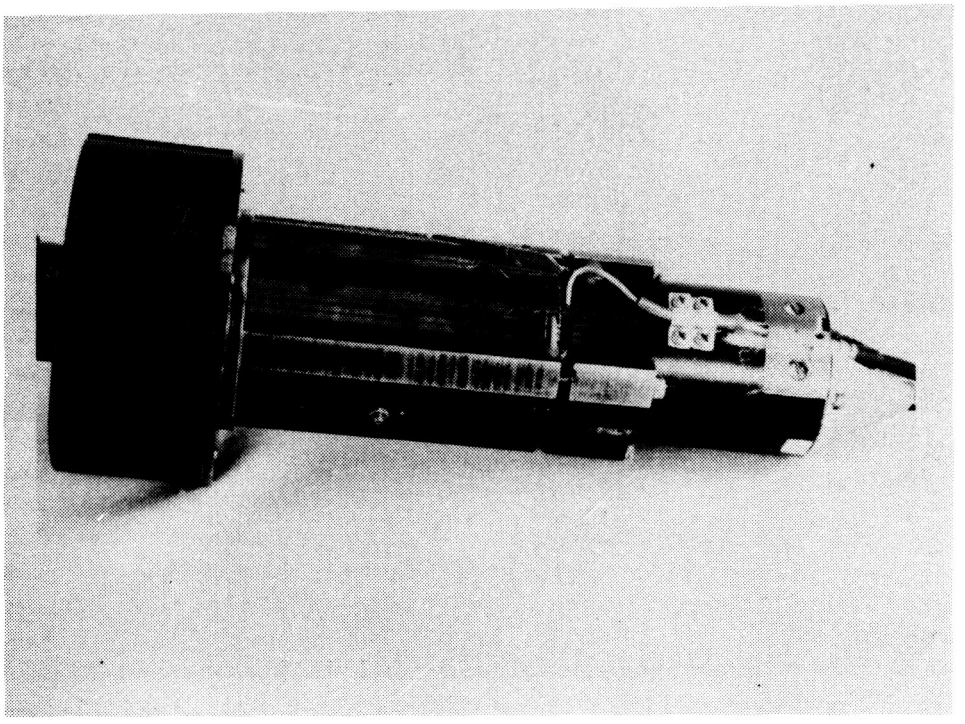

Figure 3-12. Optical Ring Side 1 Cover Off

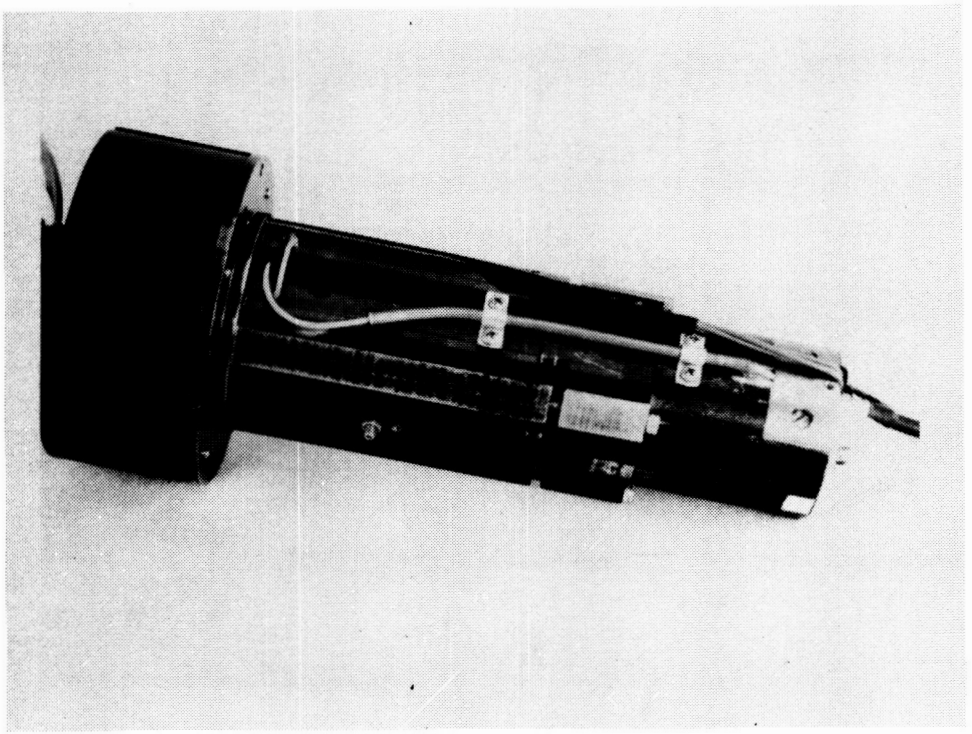

Figure 3-13. Optical Ring Side 2 Cover Off

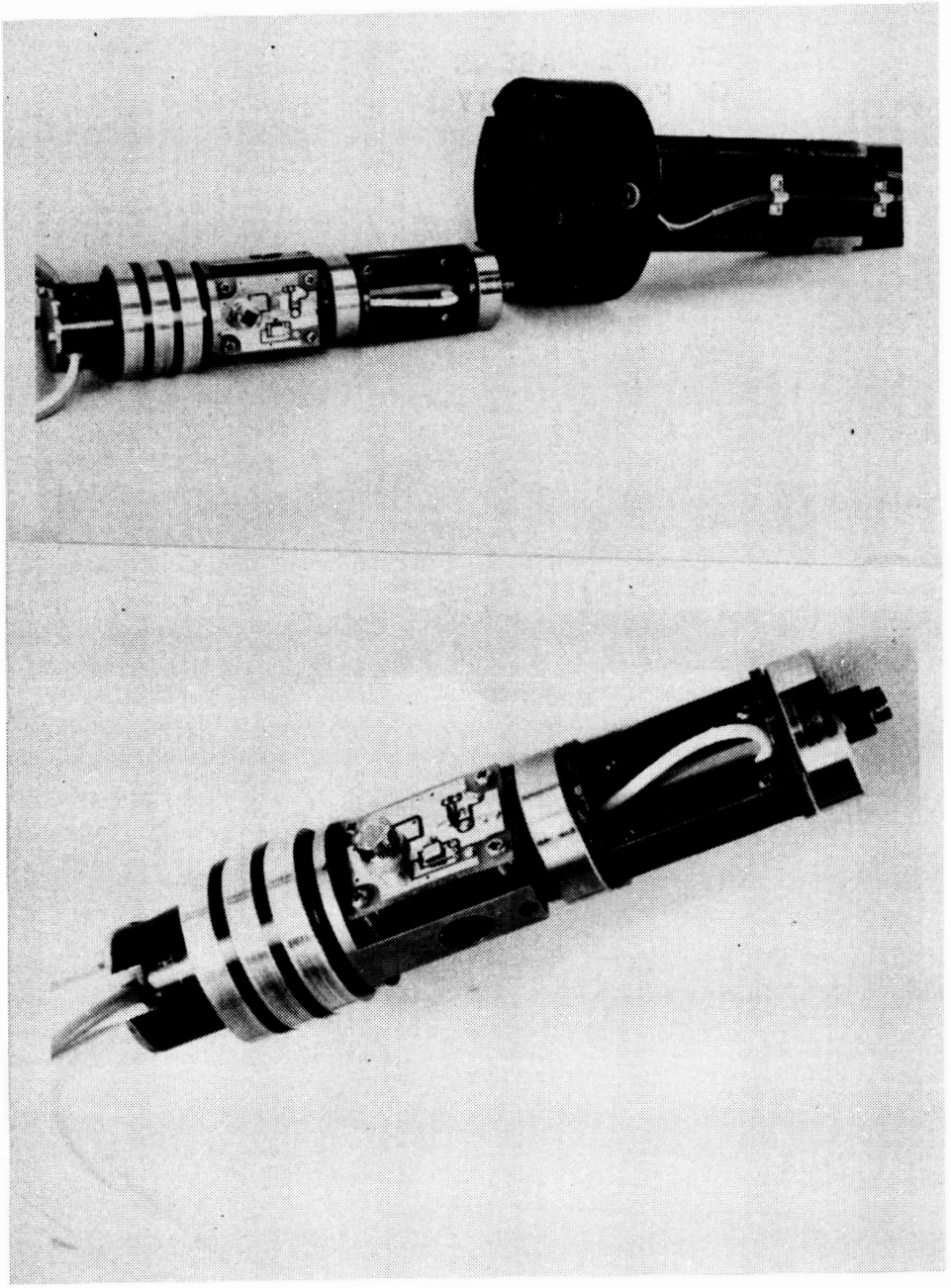

Figure 3-14. Optical Ring Exploded View

The logical approach is to digitize the input signals, transmit the data in serial form through the optical ring assembly, operate on the data as required, and transmit it to NASA instrumentation.

In practice, this approach requires sampling of the input signals. The minimum practical sampling rate for a 20 KHz bandwidth signal is about 50 KHz (to avoid aliasing of the sampled data frequency spectrum). Thus to handle 128 signals through a single channel requires a sampling rate of 128 x 50 KHz or 6.4 MHz. With a 12 bit digitizer and a seven bit identification the serial data bit rate becomes 6.4 MHz x 19 = 121.6 MHz. This sampling and serial data rate exceeds the practical state-of-the-art.

The initial system design handled the data bit rate problem by assuming four channels instead of one, thus immediately reducing the serial data bit rate to 17 (12 data + 5 I.D.) x 32 x 50 KHz = 27.2 MHz, a practical range for optical coupling.

This approach requires (for each channel) the multiplexing and 12 bit analog to digital conversion of 32 signals, a word throughput rate of 32 x 50 KHz = 1.6 MHz per channel. Thus only 625 nanoseconds is available for switching the multiplexer, performing a sample and hold function, and doing the A/D conversion.

One more step brings the system within the practical state-of-the-art. Each group of 32 signals is divided into two subgroups of 16 signals each. The word rate for each subchannel is 16 x 50 KHz = 800 KHz. This gives 1.25 microseconds from multiplexer input to digital output, within the practical state-of-the-art. Synchronizing the timing of two subgroups (16 signals each) gives 24 data bits plus four I.D. bits to be serially transmitted over an optical channel every 1.25 microseconds, a 22.4 MHz serial data rate. Transmission of one four bit I.D. with two 12 bit data sets is sufficient since time demultiplexing of the serial data stream with respect to the I.D. bits will separately identify the two 12 bit data sets.

Figure 4-1 schematically shows the primary components required in the beanie for each of the 4 downlink optical coupling channels. This represents the original system concept for the data sampling and optical coupling portion of the total system.

The total downlink system in the beanie then consists of 128 antialias filters, eight 16/1 multiplexers, eight sample and hold devices, eight 12 bit A/D converters, four 28 bit shift registers, and four optical transmitters. Plus circuitry for one uplink channel decoder, a relatively small task; plus power regulators.

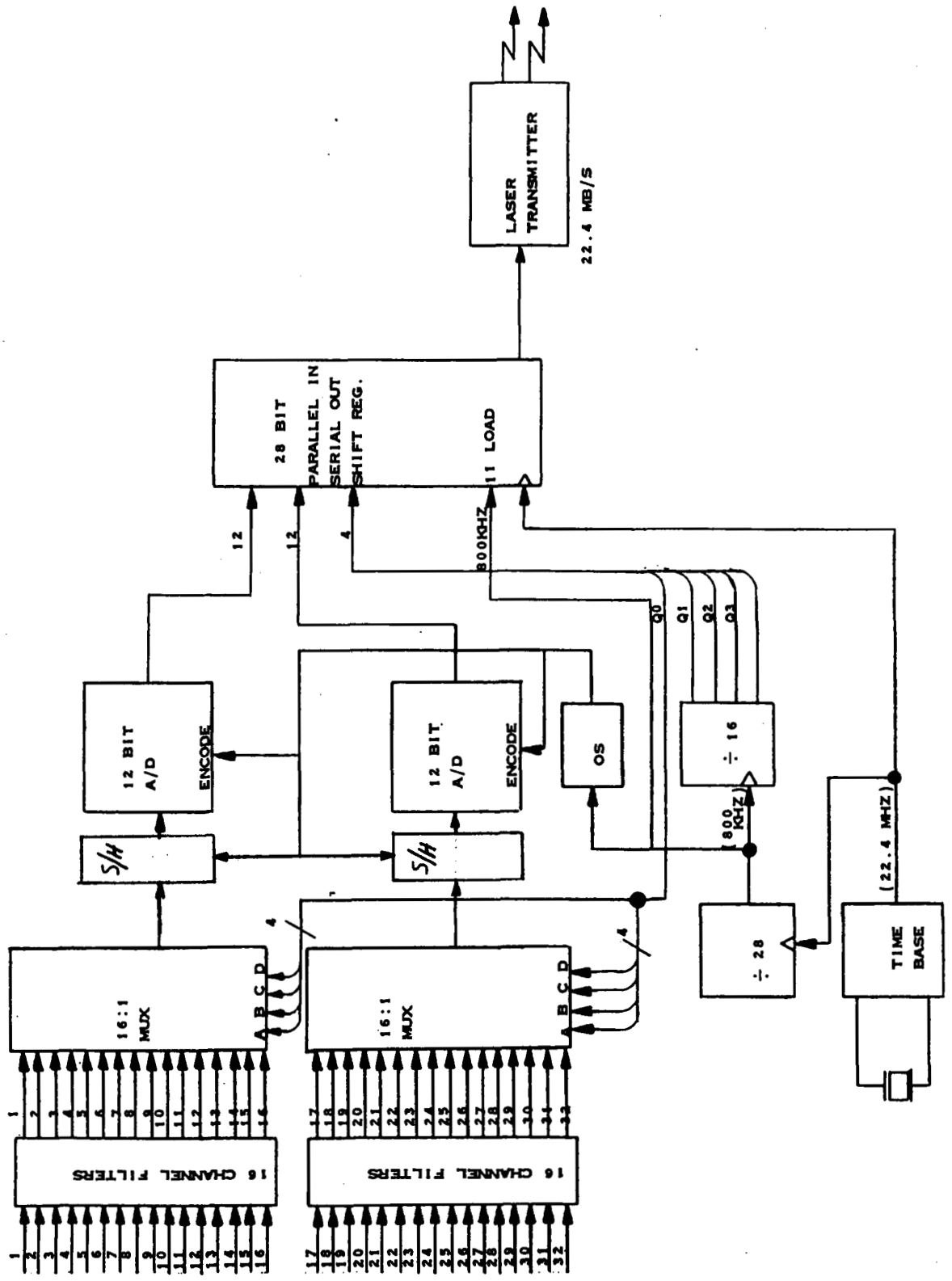

Figure 4-1. Data Encoder: One of Four

The concept was within the state-of-the-art from a circuitry viewpoint. The question of volume and power required to implement the approach was to be investigated. Clearly, the result would be contingent on the size, power requirements, and availability of the primary components.

5.0 COMPONENTS

Early in the program a search was conducted for suitable components for the beanie analog to digital converter chain. Some were already known but the search was conducted anyway in the hope of locating better, smaller, or lower power devices.

The following discussion on components assumes the original system concept described in Section 4.0 above.

5.1 ANTIALIAS FILTERS

The system requires 128 antialias filters, one for each input signal. With a signal bandwidth of 20 KHz and a sampling rate of 50 KHz the filter must have a very sharp cutoff and a floor of at least 72 dB (for a 12 bit resolution system).

The original candidate was the EGG RF5609A Elliptic Low-Pass Switched Capacitor Filter. This is a 7 pole, 6 zero elliptic filter with a 75 dB floor. The commercially available unit is in an 8 pin dip and operates at $\pm$ 8 volt with about 15 milliamps of current (0.25W).

The primary considerations in selecting the RF5609A was its very sharp cutoff frequency and small size. The primary concern was its D.C. offset specification, $\pm$0.6 volts ($\pm$491 LSB) and an unspecified temperature drift. The initial D.C. offset can be nulled by controlling a "reference" input to the I.C.

Temperature tests on six units revealed large D.C. offset drifts and D.C. gain drifts.

In the range of 25^{o}C to 55^{o} offset changes of up to 43 millivolts (0.86%, 35 LSB) were observed. D.C. gain changes of up to 0.6% (25 LSB) were observed on one unit, 0.3% (13 LSB) was the maximum gain change on the other 5 units. Room temperature D.C. offsets were indeed large (up to 0.5 volts, 410 LSB) and gain varied from 0.98 to 1.0 (82 LSB to 0 LSB). Figure 5-1 is a representative set of measurements on the D.C. characteristics.

An extensive search located three-switched capacitor filters as potential replacements for the EGG5609A. Most switched capacitor filters have a signal frequency response of 5 KHz or less.

From a specification viewpoint, the TS8512 from Thomson Semiconductor was the most attractive. Unfortunately, the unit was being phased out of production. None were available.

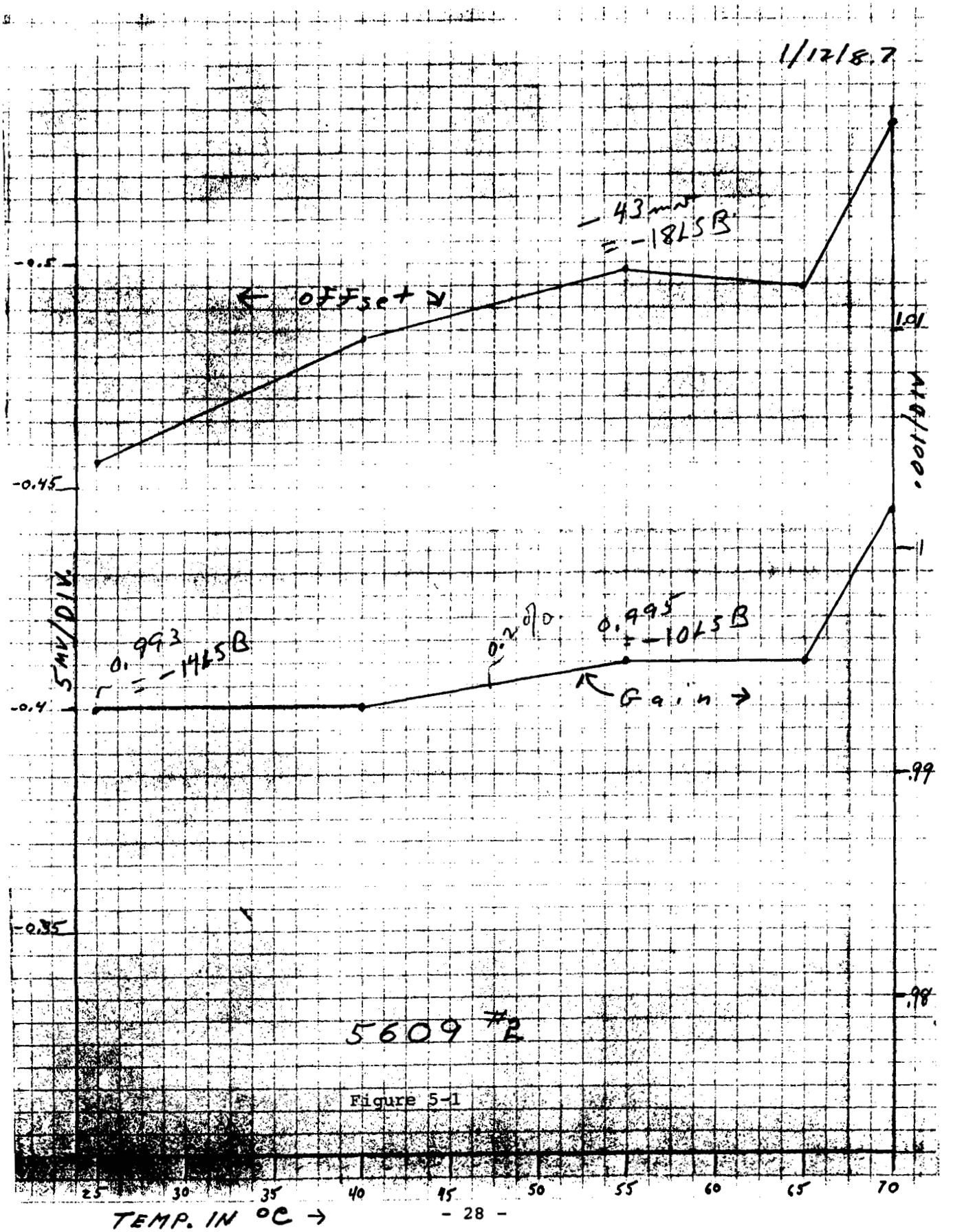

Figure 5-1

The next most attractive was the LTC1062 from Liniar Technology. This unit was designed to eliminate the D.C. drift problem. It is a fifth order maximally flat design and therefore does not have the desired very sharp cutoff characteristic required. However, two units could be cascaded to provide a sharp tenth order filter. When detailed specifications became available, it was found that although operation at 20 KHz bandwidth was possible, the filter floor raised rapidly at bandwidths above about 100 Hz. At a 10 KHz bandwidth the filter floor is only 43 dB. A floor of at least 72 dB is required.

The third candidate was the EXAR 1015. This device is an 8 pin dip with a specified initial offset (trimable) of $\pm$0.1 volt (82 LSB), six times better than the RF 5609A. It is a 7 pole, six zero, elliptic filter. The D. C. offset drift with temperature was not specified.

Six XR1015 filters were obtained and evaluated. The room temperature D.C. offset was measure at 36 mV maximum for the six units. This relatively small offset (30 LSB) can be corrected to essentially zero at room temperature.

The six units were tested for D.C. drift and D.C. gain from room temperature to 55 degrees C. The maximum rated power dissipation of the plastic unit is reached at 50 to 55 degrees C.

At 55 degrees C the worst case D.C. offset drift was 10 mV, 8 LSB. At 45 degrees C the worst case D.C. drift was 7 mV, 5.7 LSB. The average of the six units was 4 LSB of drift.

The maximum D.C. gain change observed (room temperature to 45 degrees C) was 0.15% (6 LSB).

Figure 5-2 is a representative set of D.C. measurements.

In view of this successful result, the units were tested at room temperature in a circuit incorporating a post-filter (Figure 5-3). The unfiltered XR1015 output contains 2 MHz switching noise of about 250 mV peak to peak. A third order Butterworth filter reduced this to essentially the noise floor of the XR1015, or about 2 mV peak to peak, 1 LSB (Figures 5-4 and 5-5).

The low output noise level was verified by inserting the filter circuit into an A/D breadboard. The resulting noise output from the A/D converter was no more than 1 LSB.

With these encouraging results in hand, a multifilter P.C. board was constructed for further evaluation, including P.C. board space requirements.

The circuit used for each filter is that shown in Figure 5-3.

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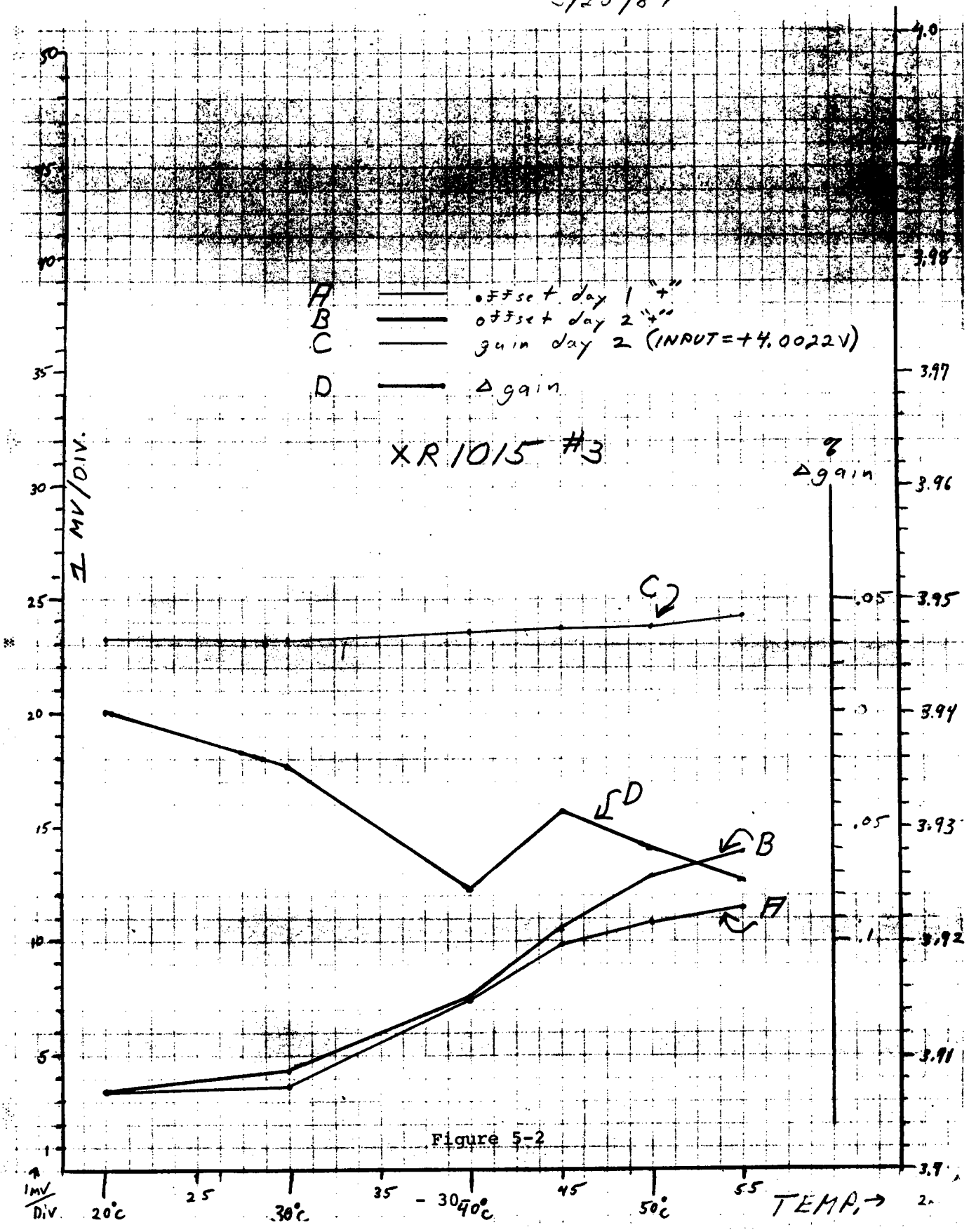


Figure 5-2

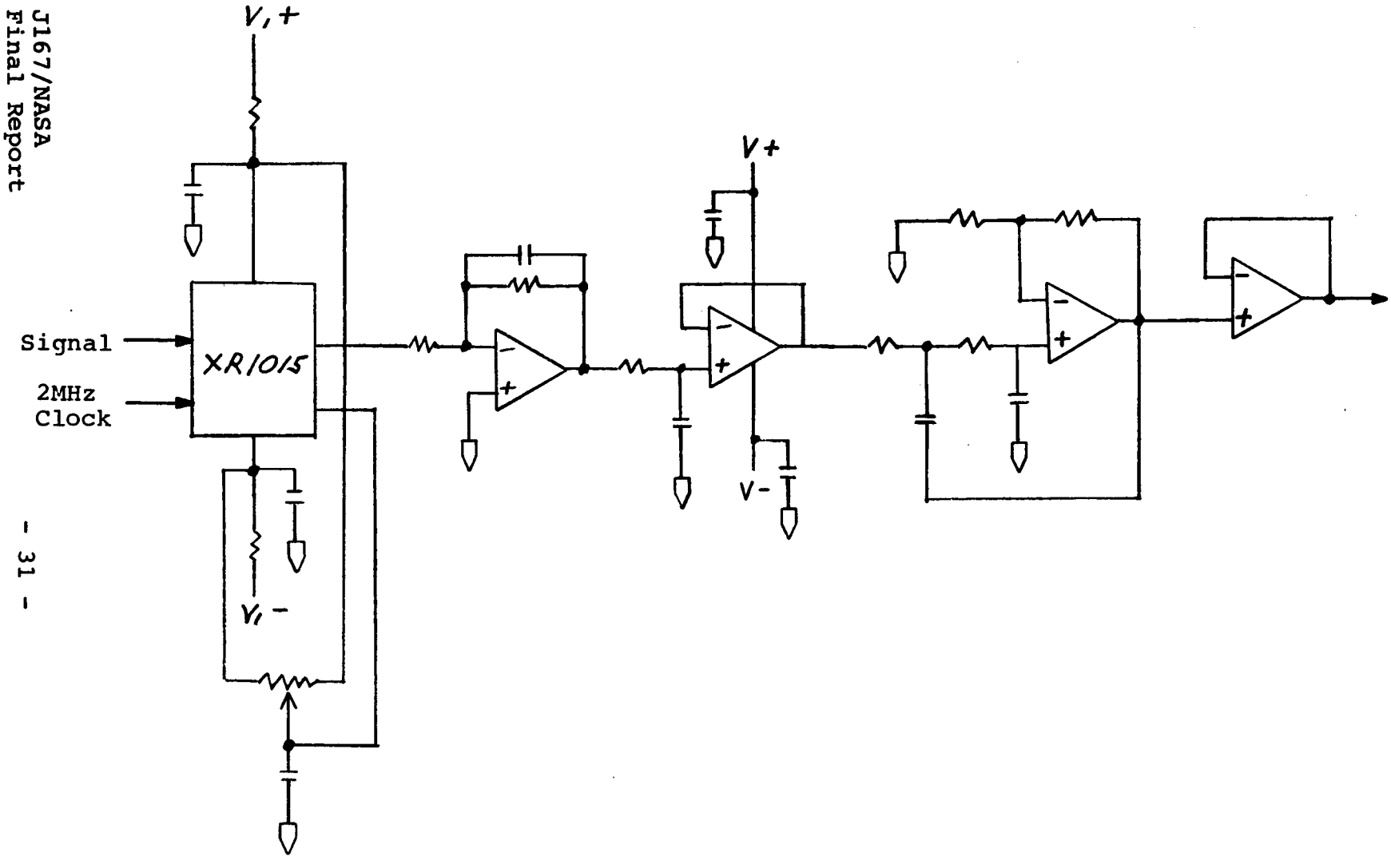


Figure 5-3. XR1015 Filter With 3rd Order Post Filter

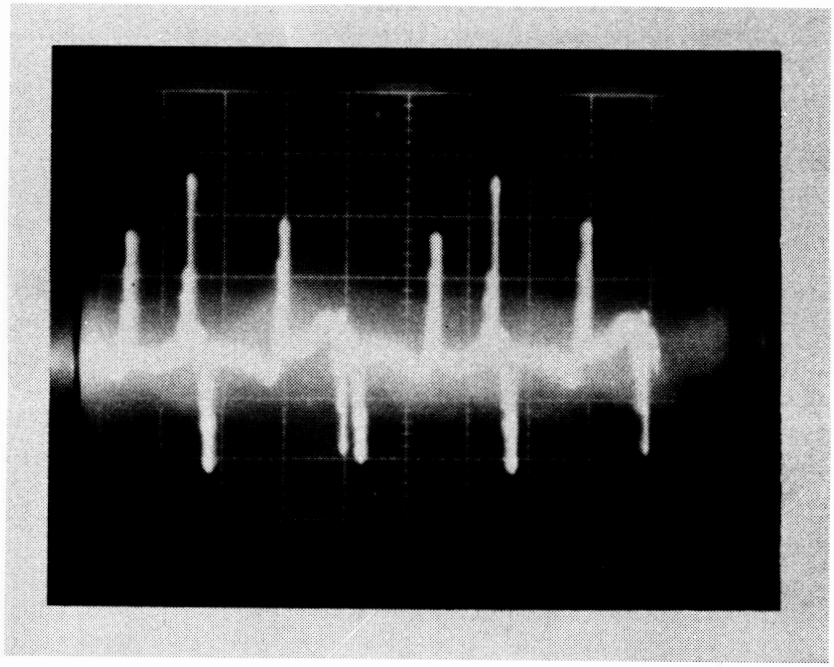


Figure 5-4. XR1015 Filter Output Noise

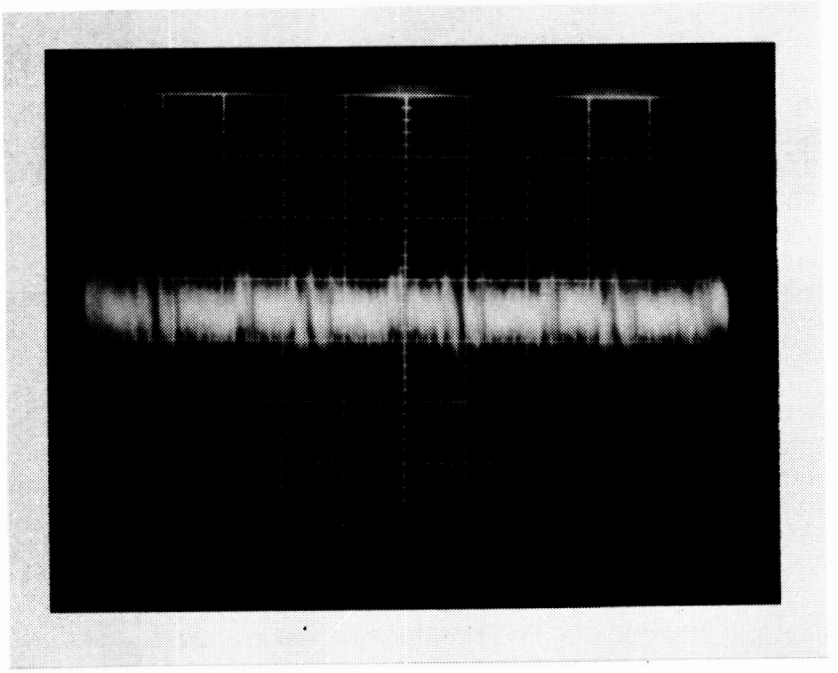


Figure 5-5. XR1015 Filter Noise Output After 3rd Order Post Filtering

With all due care in component layout satisfactory operation could not be obtained.

The internal switching of the switched capacitor filter is at a 2 MHz rate for a 20 KHz bandwidth. The 2 MHz clock is supplied externally to the filter. The high clock frequency makes it relatively easy to filter out the clock feedthru which occurs within the filter itself, but makes it difficult to keep the clock signal from coupling to the filter input. When the filter input signal contains frequency components at the filter switching frequency, the result is a D.C. output shift as a function of the amplitude of the input signal at the clock frequency. This is due to aliasing when the sampling frequency (filter switching frequency) is less than twice the maximum input frequency. This problem is compounded when more than one filter is in operation since the feedthru clock spikes (approximately 1/4 volt in amplitude, Figure 5-4) from one filter cross-couple to the input of other filters, and visa versa.

In view of the nature of the problem, and the relatively large amount of digital noise that will inevitably exist in the total system, D.C. coupling of switched capacitors filters was abandoned.

An alternative approach is shown in Figure 5-6. In this configuration the switched capacitor filter passes the A.C. part of the signal. The D.C. part of the signal bypasses the switched capacitor filter. The two signal components are recombined in an opamp, followed by a post-filter to remove the filter noise spikes.

This approach eliminated the D.C. drift problem but required precise control of the time constants in the two paths. Suitable components for operation over a reasonable temperature range could be obtained. However, component delivery times were in the order of three to four months. This was not acceptable.

In addition to the component delivery problem, a second cross-coupling effect was observable on elimination of erratic D.C. offset created by clock cross-coupling.

The switching action within the filter creates a "glitch" reflection on the filter clock input drive. Each filter has a slightly different clock threshold and therefore produces a "glitch" reflection at a slightly different point on the clock rising edge. When more than one filter is driven by a common clock line the "glitches" combine to form an unstable "glitch" pattern on the rising edge. The effect is to create a clock-to-clock time variation in the actual operation of each filter. This frequency modulation of the clock frequency can, and did, create frequency components within the 20 KHz passband of the filter. Thus, in effect, the filter output contained A.C. signals that were not present in the signal input. Presumably this could be eliminated by buffering and shielding the clock

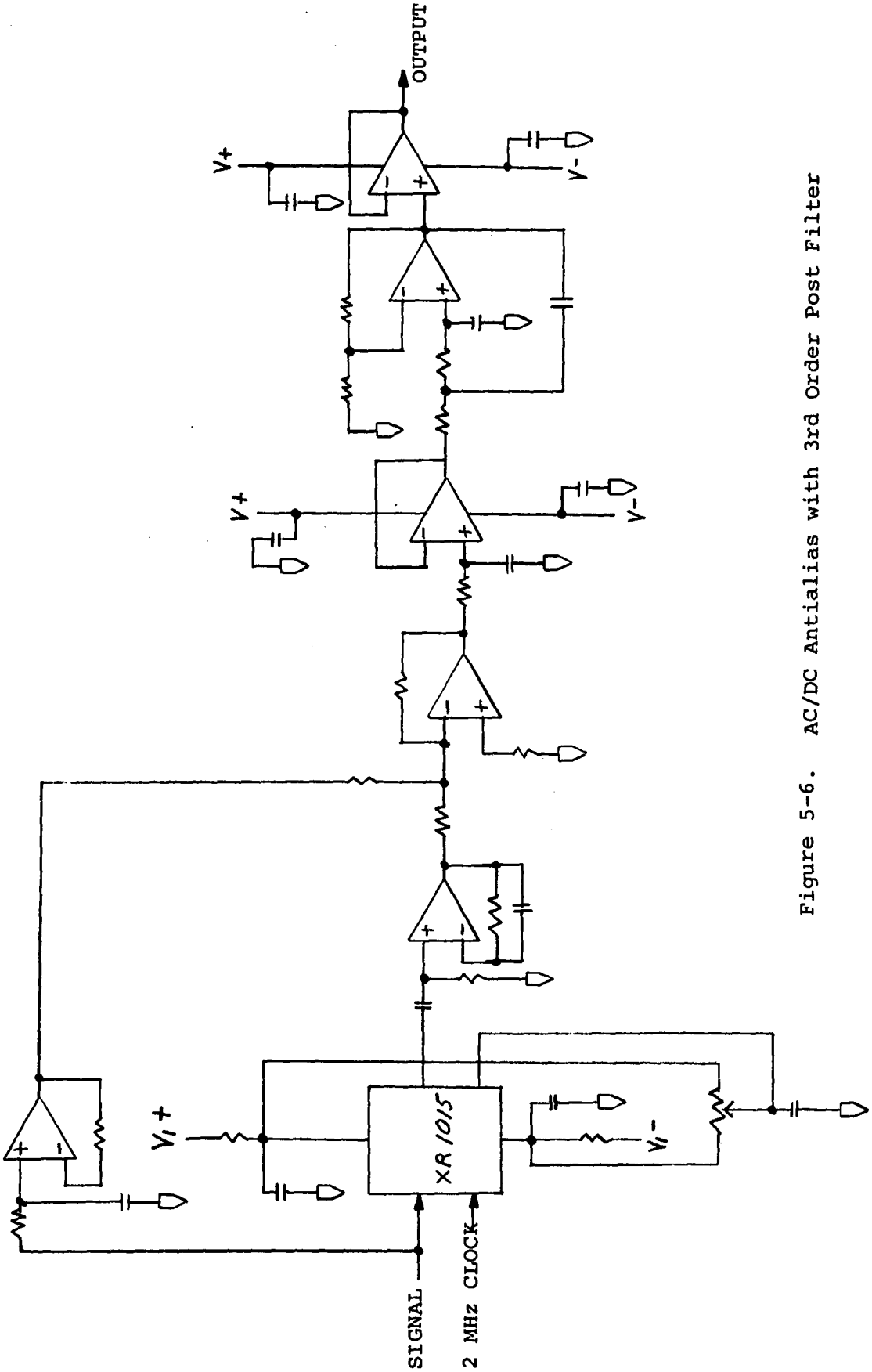


Figure 5-6. AC/DC Antialias with 3rd Order Post Filter

input to each filter. However, consideration of the P.C. area already required per filter plus the difficulties of obtaining the desired performance led to abandoning the switched capacitor filter approach.

The area required for the circuit of Figure 5-3 or 5-6 was 3.75 square inches including ground plane guard bands. For 128 filters, 480 square inches was required, without connectors. With a circular board form factor and connectors accounted for, at least 16, 9 inch diameter P.C. boards would be required to implement the filter system in the beanie. This exceeded the practical limit for the beanie electronics package. Even converting the filter circuit to a hybrid package would not reduce the P.C. board area requirement to a practical level. This result was the main factor leading to a change in the system configuration discussed later in this report.

In view of the above, passive and active antialiasing filters were considered. The smallest suitable active filter found was the Model 675 from Frequency Devices. It is a seventh order elliptic filter and requires a 4 square inch P.C. area. The smallest suitable passive filter found was from TTE, Incorporated; Model LE7-20KHz-3K-11 requiring 2.7 square inches. Both units were evaluated.

Four active filters were tested. A typical response curve is shown in Figure 5-7. Initial D.C. offsets were less than 4 millivolts (3 LSB). The maximum D.C. offset drift was 12.6 millivolts (10 LSB) over the range from 25°C to 50°C.

Four passive filters were tested. A typical response curve is shown in Figure 5-8. As a passive filter, no D.C. offset exists. The response curves (particularly the -3 dB cutoff frequency) were measured over a temperature range of 25°C to 50°C. No measurable change in response characteristics occurred.

Figure 5-9 compares the response characteristics of the active and passive filters. The frequency response curve for the active filter is shown as the solid line. The dashed line is the passive filter response. The passive filter cutoff is slightly sharper than the active filter cutoff. Both filters are 74 dB down at 50 Kilohertz (the system sampling frequency). Both filters remain below 72 dB down through ten Megahertz. Figure 5-10 shows a swept frequency response of the passive filter.

The apparent lower floor for the active filter (79 dB vs 74 dB) is due to improved low level measurement techniques.

The passive filter was selected for the final system. The reasons being its sharper cutoff, freedom from offset drift, zero power consumption (vs 1 watt per active filter), and smaller size. The passive filter 6 dB insertion loss is readily compensated for elsewhere.

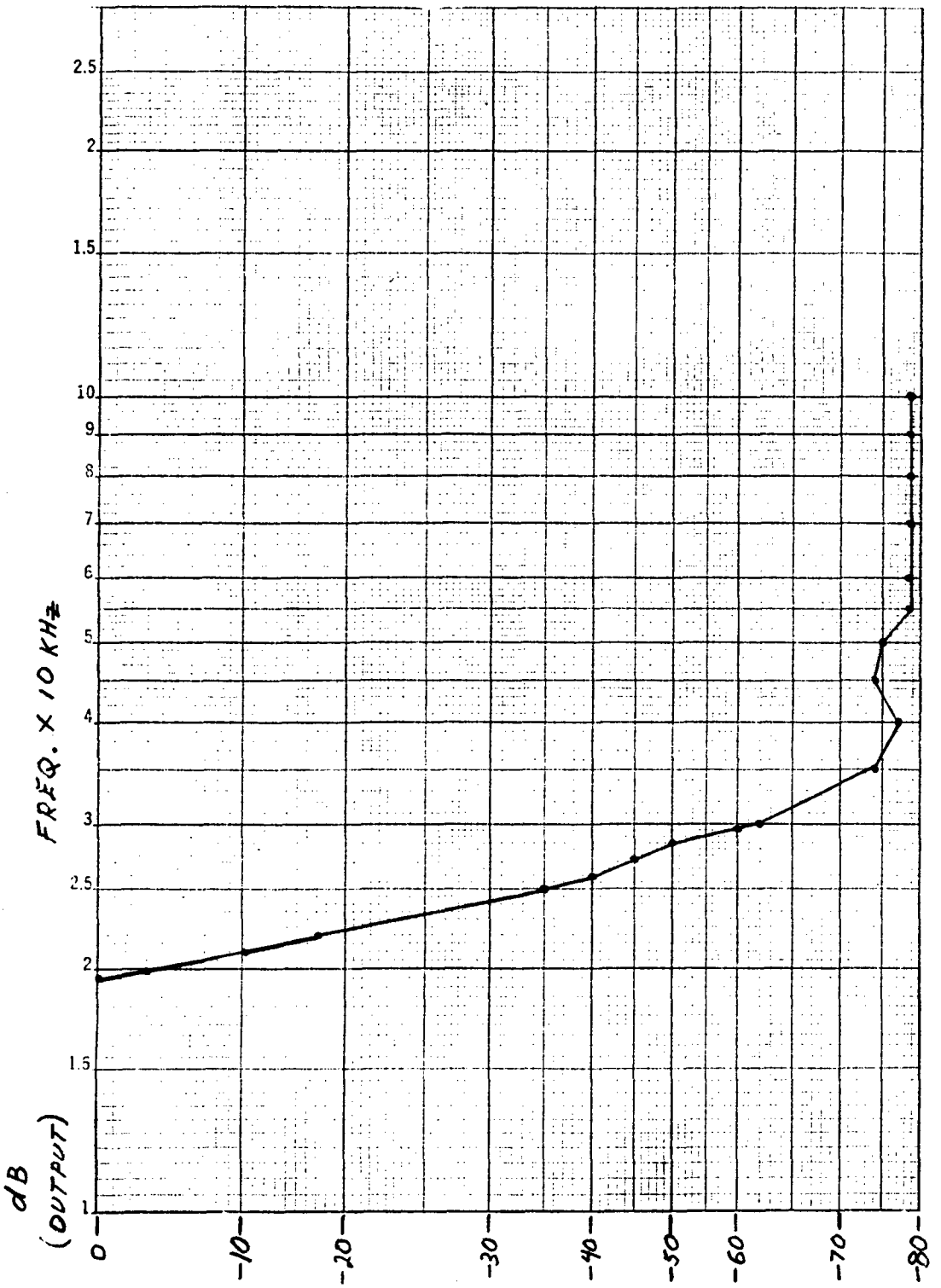


Figure 5-7. Active Filter Response

LE7-20 KHz PASSIVE FILTER

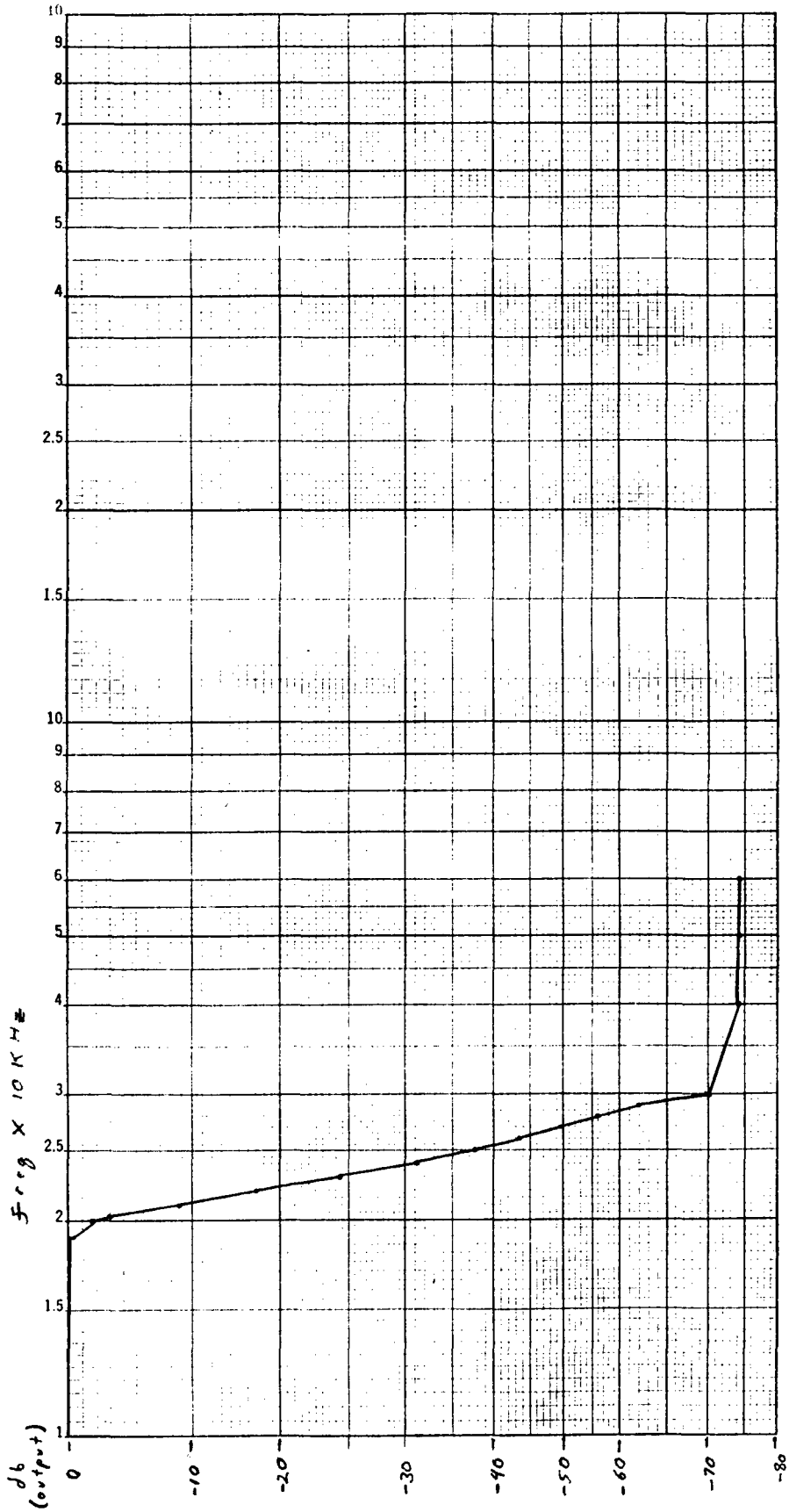


Figure 5-8

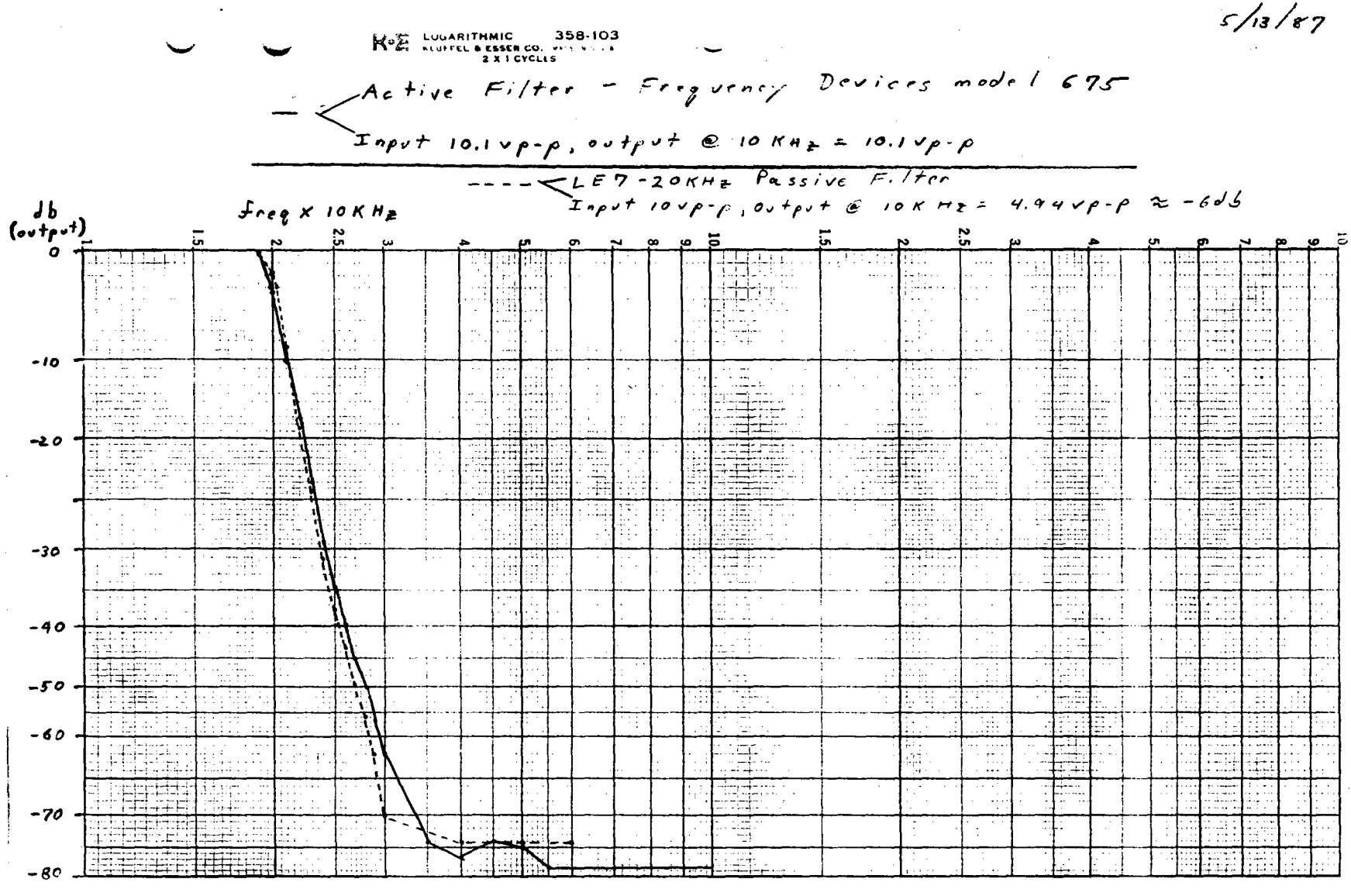


Figure 5-9. Active and Passive Filter Responses

-3dB = 20.05 KHz

≈ 3 KHz/Div.

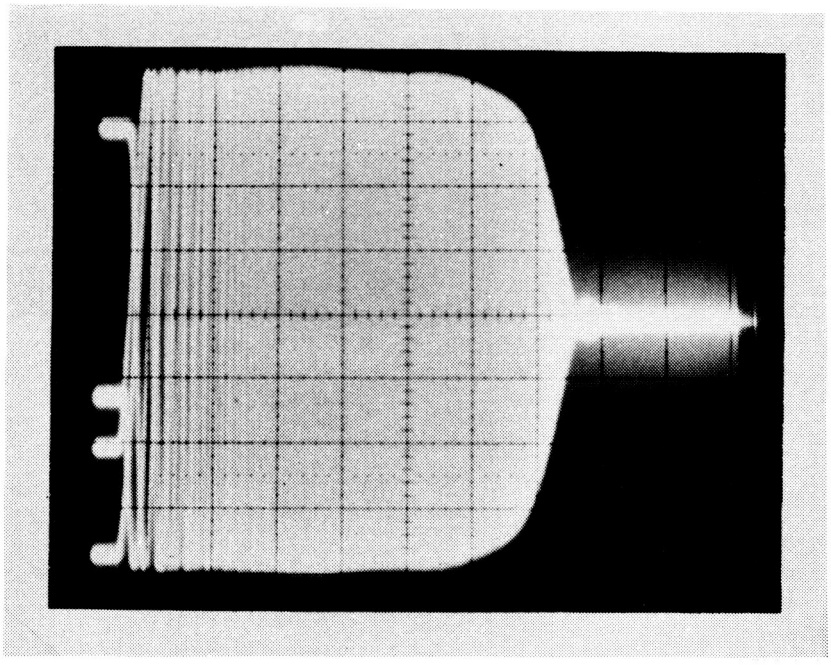


Figure 5-10. Passive Filter Swept Frequency Response

The physical size of the passive filter is about the same as that for the switched capacitor filter discussed earlier. Thus the P.C. board area requirement is about the same.

The change in the system configuration (discussed later in this report) imposed a further requirement on the filter characteristics. Namely, the filter recovery time from a full scale step input must not exceed 1 millisecond. Accordingly, the passive filters were tested for this characteristic.

In order to obtain a valid step recovery time measurement using an oscilloscope, the input to the oscilloscope must not exceed the dynamic range of the oscilloscope vertical amplifiers, otherwise the recovery time of the oscilloscope amplifiers distorts the measurement. To examine the filter step recovery to the millivolt level requires removal of the step voltage (approximately 5 volts) at the filter output. This was accomplished with the circuit of Figure 5-11. A low frequency 10 volt square wave is inverted and applied to the filter. The output of the filter is amplified by a factor of 2 to compensate for the filter attenuation. The input signal is subtracted from the filter output by the summing action at the input to the output amplifier. The output of the amplifier is further A.C. limited to $\pm$ 0.6 volts by a pair of diodes.

The 1 millisecond recovery time of the passive filter is shown in Figure 5-12 with a vertical scale of 5 millivolts per division (4 LSB) and a time base of 0.2 milliseconds per division.

5.2 ANALOG TO DIGITAL CONVERTER

The input analog signals are converted to 12 bit digital form for optical transmission through the Optical Slip Ring assembly.

In addition to good 12 bit performance the A/D must have a conversion time fast enough to perform in an A/D chain which includes multiplexer switching time, sample and hold settling time, and buffer amplifier settling time (Figure 5-13).

For a non pipelined system, the time available for A/D conversion is 1.25 microsecond minus settling time for all other components in the chain. A parallel search for fast and accurate multiplexers and sample/hold amplifiers indicated a requirement for 12 bit A/D conversion in 250 nanoseconds. This was beyond the state of the art.

Resorting to a pipelined system, in which the multiplexer is switched and settles during the actual A/D conversion, the A/D conversion time required can approach 1 microsecond.

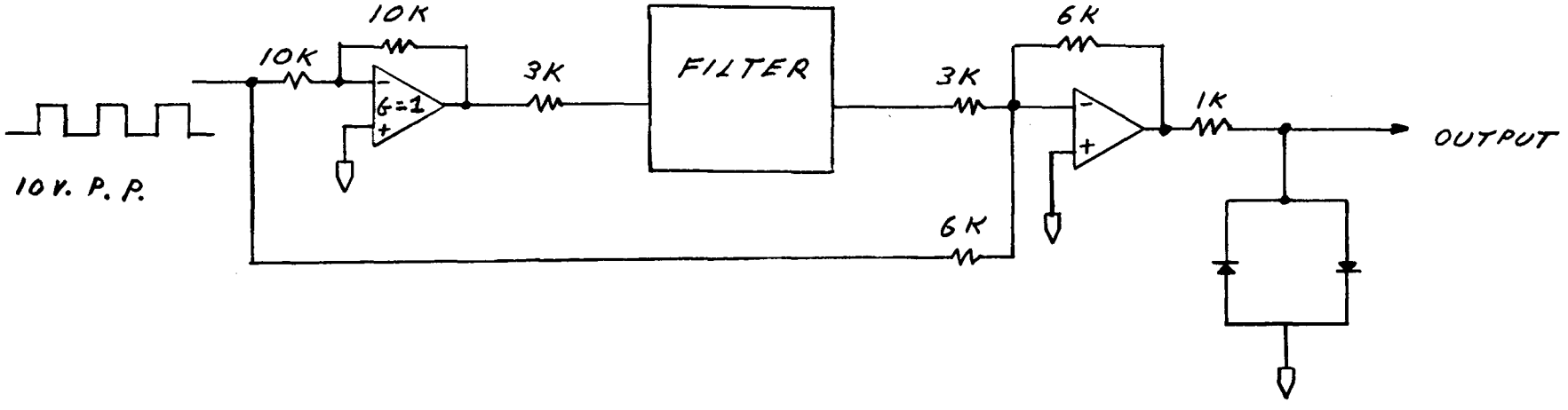


Figure 5-11. Filter Transient Test Circuit

5 MV/DIV (4 LSB)
0.2 MS/DIV

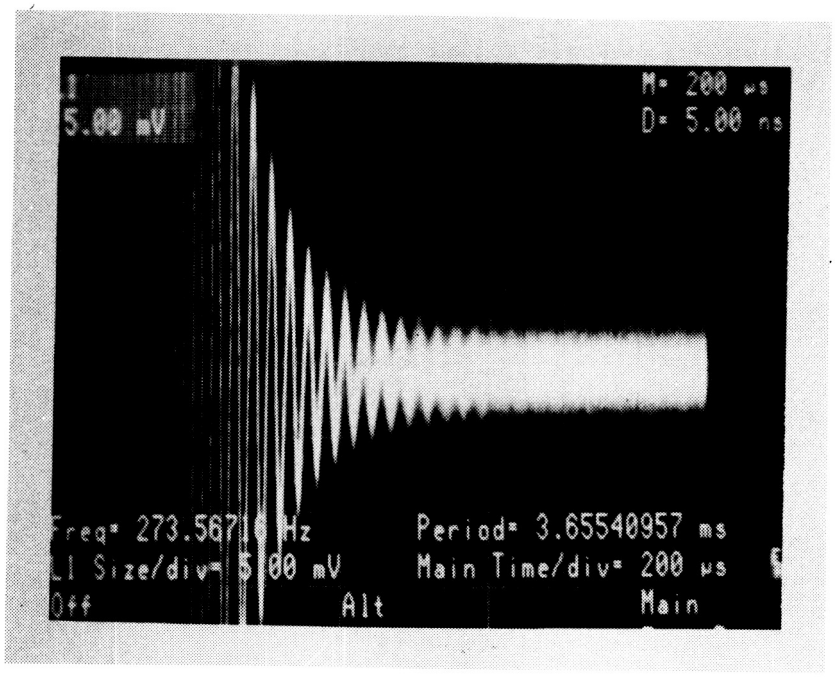


Figure 5-12. Passive Filter Step Function Response Recovery Time

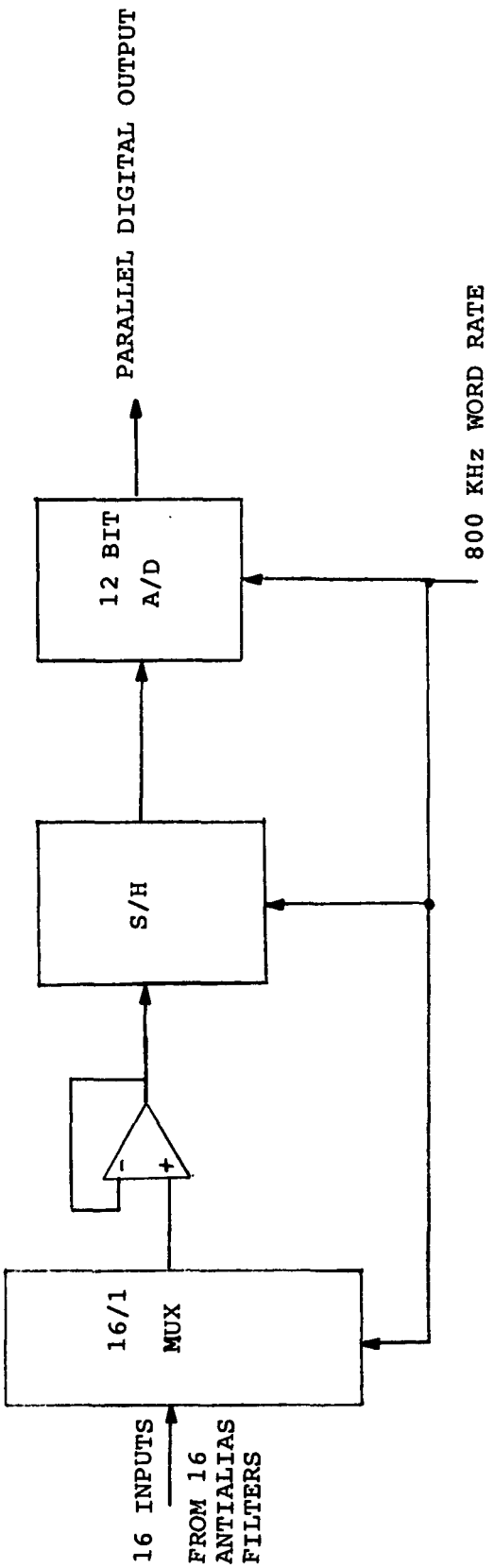


Figure 5-13. A/D Chain

The search for suitable 12 bit A/D converts was therefore conducted with a one MHz minimum word throughput criteria. Some of the companies products researched and the basic results are shown in Table 5-1. Additional A/D converters investigated did not have the needed combination of 12 bit conversion and word rate.

The Micropower 11 bit converter listed in Table 5-1 is included because of its very low power requirement. One unit was tested and performed to specification at room temperature. This was the MP7685JD 2 MHz unit. The 1 MHz version was 1 year delivery. The unit presents complication in that an external reference voltage is required, the operating voltage for a 5 volt full scale input in $\pm$ 6 volts, the digital output voltage levels are not directly compatible with standard logic levels, and several Schotsky diodes are required to protect the unit. These factors plus a strong desire for a 12 bit system removed it from further consideration.

Examination of Table 5-1 shows that most of the units are eliminated by lack of availability. The system requirement was at the limits of the practical state of the art.

The Honeywell HAD C803A was eliminated as a brand new unproven product. Normal delivery times (3 months) precluded taking a change on its viability.

The Data Devices ADC 300 was very attractive since it does not require an external sample and hold circuit. A quoted best delivery schedule of 4 months eliminated it from further consideration.

This left the Datel ADC 500 and 505 units. The ADC 500 was available with a two week delivery.

A summary of the ADC 500 specifications is contained in Table 5-2.

The unit was tested for absolute accuracy at 25° C ambient temperatue with the gain and offset adjustments grounded (zero volts). Six input voltages were used including zero and very close to full scale. The results are shown in Table 5-3.

It is clear that offset and gain trimming would increase the absolute accuracy.

Trimming and temperature testing were deferred until an entire A/D chain was in operation, from multiplexer through the A/D converter output. This subsystem temperature test is more meaningful than a single component test. The results are reported later in this document.

FAST 12 BIT A/D CONVERTERS

MFG.	MODEL	WORD RATE	INTERNAL REF.	SIZE	POWER	COMMENTS
MICRO NETWORK	MN5245	1 MHZ	Y	2.1 x 0.8	2.6W	1 Year Delivery
	MN5247	2 MHZ	Y	2.1 x 0.8	2.6W	Stopped Making It
ANALOGIC	AH8022	1 MHZ	Y	-	-	Not Released
	AH41012	2 MHZ	Y	-	-	Not Released
ANALOG DEVICES	HAS1201	1 MHZ	Y	2.4 x 1.6	3W	
	AD375	1 MHZ	Y	2.4 x 1.6	2.3W	Not Released
CRYSTAL SEMI.	CSC5212	1 MHZ	N	2.1 x 0.8	1W	Not Released
INTECH	5245	1 MHZ	Y	2.1 x 0.8	2W	
HONEYWELL	HADC803A	1 MHZ	Y	2.1 x 0.8	1.6W	New Product
DATEL	ADC868	2 MHZ	Y	4 x 6	7W	Complete Board
	ADC505	1.3 MHZ	Y	1.7 x 1.1	1.4W	
	ADC500	1.4 MHZ	Y	1.7 x 1.1	1.4W	
DATA DEVICES	ADC300	1.7 MHZ	Y	2.2 x 1.2	3.5W	Includes Sample and Hold Circuit
MICROPOWER	MP7685LD	1 MHZ	N	2 x 0.6	0.1W	11 Bit Converter
	MP7685JD	2 MHZ	N	2 x 0.6	0.13W	11 Bit Converter

TABLE 5-1

TABLE 5-2

DATEL ADC 500

Conversion Time (12 bits):	500 nanoseconds
Number Bits:	12
Missing Codes:	None
Nonlinearity:	$\pm$ 1/2 LSB
Full Scale Absolute Accuracy:	$\pm$ 3 LSB
Zero Error:	$\pm$ 1 LSB
Zero Error Temperature Coefficient:	$\pm$ 13 ppm/^{o}C = 0.05 LSB/^{o}C
Gain Temperature Coefficient:	$\pm$ 17.5 ppm/^{o}C = 0.07 LSB/^{o}C
Overflow Ouput:	Yes
Trimable Gain and Offset:	Yes

TABLE 5-3

A/D 25°C ACCURACY

INPUT	OUTPUT EQUIVALENT	ERROR	LSB ERROR
0.0000	0.0098	+0.0098	+4
0.0229	0.3427	+0.01137	+4.65
0.2018	0.21048	+0.0087	+3.55
2.5016	2.51121	+0.0096	+3.9
5.0057	5.0126	+0.0069	+2.8
7.4946	7.4994	+0.0048	+1.96
10.0008	10.00322	+0.0024	+0.98

5.3 MULTIPLEXER

The system requires the multiplexing of input signals at an 800 KHz rate. To provide time for incidental timing requirements in the A/D chain (such as sample and hold operation) a 1 MHz operating rate was used as a criteria. The operating rate includes the multiplexer switching (acquisition) time plus the time for the output to settle to within 0.024% of the final value (1 LSB).

A multiplexer inserts a series resistance between its input signal and its output (Figure 5-14). The smaller the series resistance the smaller the multiplexer output load impedance can be. The smaller the output load impedance the less susceptible the operation is to the effects of leakage currents and stray capacitance both within the unit itself and from external sources. A lower load resistance also improves the settling time.

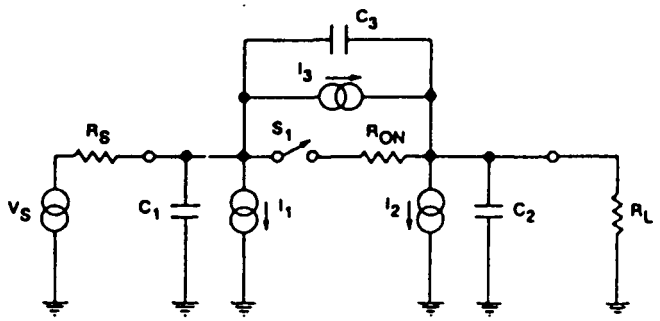
The Datel MX 1616 16/1 multiplexer was known to meet the system requirements but its series impedance and power requirements were of concern. A search for alternate multiplexers was conducted and the results are illustrated in Tables 5-4 and 5-5. Many additional multiplexer specifications were examined but those of the referenced tables represent the only ones meeting the system criteria. The table includes an illustration of parameter ranges.

For example, as the series resistance decreases the power requirement decreases, however the operating rate also decreases. In this case the operating rate decreases to the point where the system requirements are not met.

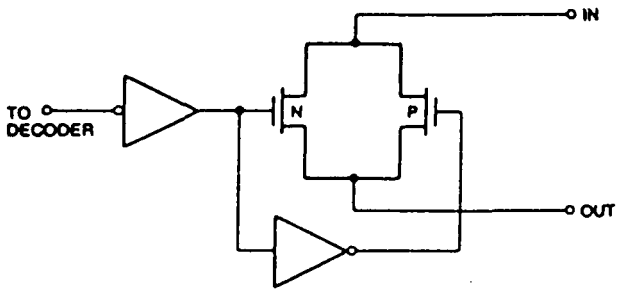
Extending the multiplexer search down to 4/1 and 2/1 multiplexers negate the above example. Fast, low series resistance low power multiplexers are available in these less complex units. However the system complexity and P.C. board area requirements increase exponentially. Thus this approach was dropped.

The Burr Brown MPC 800KG 16/1 multiplexer has a lower series resistance and a lower power requirement than the Datel MX 1616. However Table only covers the basic multiplexer requirements for performance. Several additional parameters must be taken into account; for example, crosstalk, output leakage current, off switch isolation, variation in series resistance with signal input amplitude, multiplexer output load specified for specified settling time, and the effect of ambient temperature on all parameters.

In the case of the Burr Brown multiplexer the operating rate specified is based on a one kilohm load resistor. This would result in a 38% attenuation of the signal at 25^{o}C and a 41% attentuation at elevated temperatures. Increasing the load



Equivalent Circuit of Analog Multiplexer Switch



CMOS Analog Switch Circuit

Figure 5-14

16/1 MULTIPLEXERS

MFG.	MODEL	OPERATING RATE (25°C)	% ACCURACY	ON R AT 25°C (OHMS)	DIP PINS	POWER IN MW	TYPE
BURR BROWN	MPC 800KG	1.1 MHZ	0.01	620	28	525	CMOS
DATEL	MX 1616	1.05 MHZ	0.01	750	28	900	CMOS
	MV 1606	370 KHZ	0.01	170	28	105	CMOS
HARRIS	HI 506	416 KHZ	0.025	270	28	32	CMOS
PMI	MUX 16ET	400 KHZ	0.02	290	28	380	JFET
SILICONIX	DG 506A	416 KHZ	0.01	270	28	60	CMOS

TABLE 5-4

8/1 MULTIPLEXERS

MFG.	MODEL	OPERATING RATE (25°C)	% ACCURACY	ON R AT 25°C (OHMS)	DIP PINS	POWER IN MW	TYPE
DATEL	MX818	1.08 MHZ	0.01	750	18	540	CMOS
	MV808	317 KHZ	0.01	250	16	55	CMOS
PMI.	MVX-08EP	435 KHZ	0.02	220	16	250	JFET
HARRIS	HI 508	1.18 MHZ	0.01	180	16	45	CMOS
	HI 1818A	317 KHZ	0.025	250	16	8	CMOS
SILICONIX	DG 501	167 KHZ	0.01	150	16	130	PMOS?
	DG 568	125 KHZ	0.01	50	18	?	NMOS?
	SI 3705	125 KHZ	0.01	150	16	175	PMOS

TABLE 5-5

resistor to significantly decrease the accuracy variation with temperature would decrease the operating rate below the system requirements. It would also introduce significant leakage current errors.

The Burr Brown multiplexer was therefore eliminated leaving only the Datel MX 1616 for system use. Fortunately the Datel unit is very thoroughly specified and selection of an appropriate load resistor yields a reasonable accuracy.

The MX 1616 has a specified series resistance of 750 ohm (maximum) at 25°C, and 1 kilohm (maximum) at 70°C. For 0.01% gain accuracy (0.4 LSB) through the switch a load resistor of 10 megohms is required.

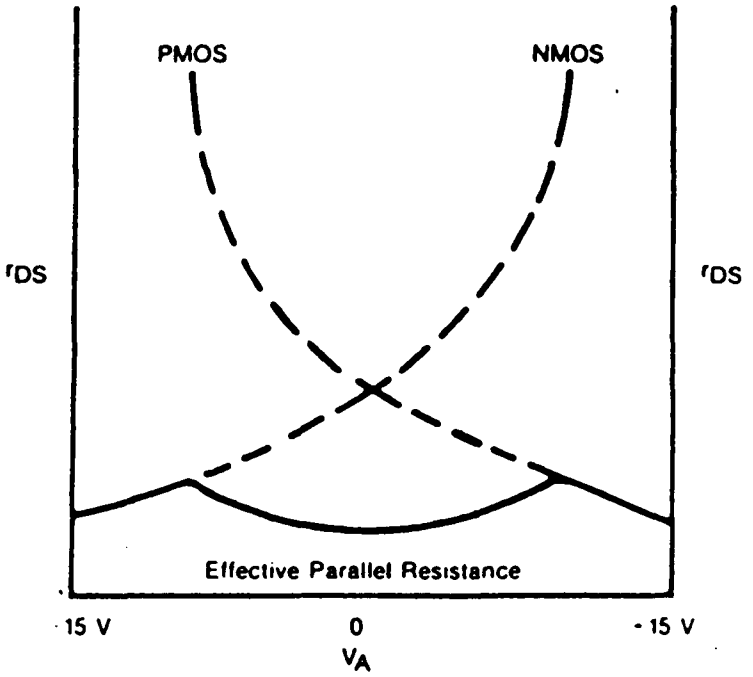
With a 10 mehohm load resistor the multiplexer current leakage output (525 picoamp) plus the input leakage of an opamp (100 picoamp) will create an error of $625 \times 10^{-12} \times 10 \times 10^{6}$ = 6.25 mv = 5.1 LSB = 0.12% at 25° C. This offset error can be corrected elsewhere but the drift with temperature would be difficult to match. At 55°C the leakage induced offset becomes 50 mv = 41 LSB = 1%. This 36 LSB offset drift with temperature was not acceptable.

Changing the load resistor to 500 kilohms drops the leakage induced offset at 25° C to 0.31 mv = 0.25 LSB. The offset at 55° would be 2.48 mv = 2 LSB. The 1.75 LSb (0.04%) offset drift with temperature was considered acceptable.

With a 500 kilohm load resistor an attenuation of the input signal takes place. At 25° C the gain error is 0.15% = 6.1 LSB at full scale input. At 55° C the switch resistance would be about 920 ohms and the gain error is 0.18% = 7.5 LSB at full scale input. The initial gain error can be corrected elsewhere. The gain error change with temperature of 1.4 LSB (at full scale input, 0.03%) was considered acceptable.

Two other factors were considered. First, switch to switch series resistance variations within the multiplexer are not specified. However a typical switch to switch variation within a given CMOS IC is typically in the 5 to 10 ohm region. This is negligible in the above calculations.

A second factor not contained in the specification is the inherent switch series resistance variation with voltage across the switch. As a CMOS switch the response can be expected to follow the general shape shown in Figure 5-15. With a 500 kilohm load resistor, a maximum switch series resistance of 1 kilohm, and a full scale input of 5 volts, the voltage across the switch is only 10 millivolts. Thus any change in switch resistance with signal amplitude should be negligible.



Graph of CMOS Switch Resistance vs. Analog Signal

Figure 5-15

5.4 SAMPLE AND HOLD AMPLIFIER

A sample and hold amplifier is required between the multiplexer output and the A/D converter input to isolate the A/D converter from the changing signal input during conversion.

With the word rate established at 800 KHz, the multiplexer selected, and the D/A converter selected, the sample and hold amplifier timing parameters required can be firmly established.

Figure 5-16 is a timing diagram of a pipelined system using the Datel MX616 multiplexer and the Datel ADC 500 A/D converter.

From Figure 5-16 the sample and hold amplifier must acquire the signal (to the desired accuracy) within 535 nanoseconds. Perturbations on the output due to switching to the hold state must settle within 134 nanoseconds. The output must remain constant to within 1/2 LSB or better for a period of 570 ns (the actual A/D convert time). The droop rate must therefore be less than 1 millivolts per microsecond.

Table 5-6 presents a list of "fast" sample and hold amplifiers. Any of the top four listed satisfy the criteria to this point. Final selection was based on additional factors such as output offset stability with input signal amplitude elevated temperature characteristics, linearity, etc. The final selection was the Datel SHM 45MC.

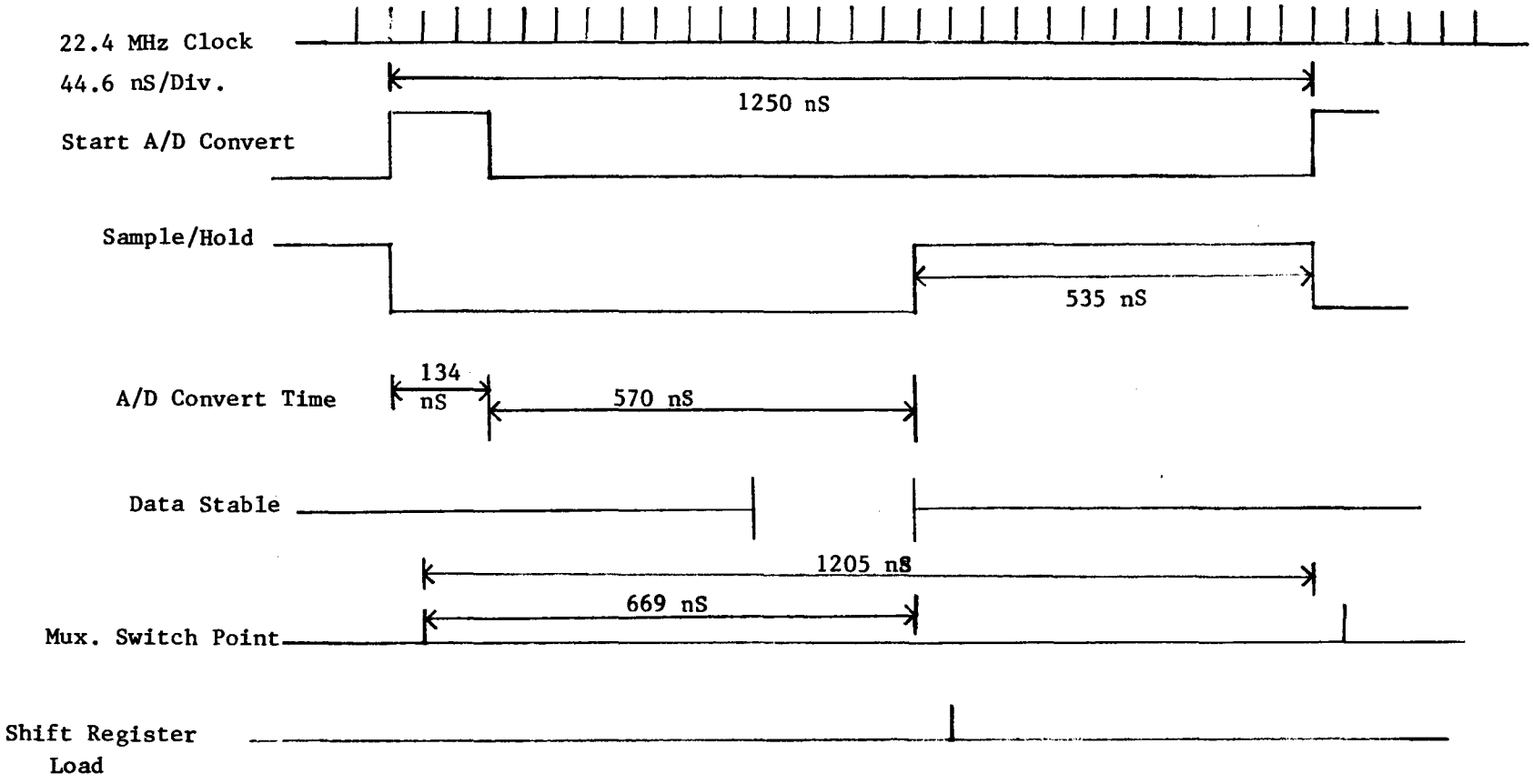
5.5 BUFFER AMPLIFIERS

A buffer amplifier is required between the multiplexer and the sample and hold amplifier. The requirements are straight forward. The input impedance should be high to avoid loading the multiplexer output. The settling time to 0.01% should be equal to or less than the multiplexer settling time of 800 nanoseconds. The input bias current and voltage offset should be low. Preferably, the amplifier should be fully compensated at unity gain and capable of inverting or non-inverting operation.

The Burr Brown 3550K nicely meets these requirements. The pertinent characteristics are listed in Table 5-7.

6.0 FINAL SYSTEM CONFIGURATION

The original system concept (Section 4 of this report) places on antialias filter in each of the 128 input signal paths. The component investigation of antialias filters (Section 5.1 of this report) made it clear that this approach required far more P.C. board area than was practical in this application. The selection of passive filters eliminated filter power requirement considerations but not the P.C. board area requirement.



A/D Chain Timing - 800 KHz Word Rate - Pipelined Timing

Figure 5-16

SAMPLE/HOLD AMPLIFIERS

MFG.	MODEL	ACQUISITION TIME: nS(.01%)	SETTLING TIME: nS(.01%)	DROOP: (70°c) V/μS	NOISE: μV RMS	FEED-THRU: -dB	SIZE	POWER: mW
DATEL	SHM 45MC	160	60	15	?	74	1.3 x 0.8	730
	SHM 4860	160	60	15	?	74	1.3 x 0.8	730
MICRO NETWORKS	MN 376	160	60	5	?	74	1.3 x 0.8	825
DATA DEVICES	THA 5210-200	150	60	15	100	74	1.3 x 0.8	700
ANALOG DEVISES	HTS 0010KD	64	20	100	20	62	1.3 x 0.8	1750
	HTC 0500AM	850	400	10	60	80	0.8 x 0.3	750
	ADSHM 5K	1000	400	12	100	70	2 x 2	2250
BURR BROWN	SHC 804CM	350	150	5	?	80	1.3 x 0.8	875
HARRIS	HA 5330-5	500	100	10	190	88	0.8 x 0.3	600

TABLE 5-6

TABLE 5-7

BURR BROWN 3550K

True Differential Input

Fully Compensated

Input Resistance = 1 x 10" OHM

Input Capacitance = 3 Picofarads

Input Bias Current = 100 Picoamps (25°C)

Input Voltage Noise = 20 Microvolt RMS

Input Offset Voltage = ± 1 Millivolt (25 °C)

Open Loop No. Load Gain = 100 dB

Settling Time = 600 nanoseconds (0.01%)

Slew Rate = 100 Volt/microsecond

A major objective of the final system configuration was to reduce the number of antialias filters required to process the 128 signals. This could be accomplished by time sharing the antialias filters among the 128 signals. The system would then operate by selecting a subgroup of the 128 signals, processing the selected subgroup for a period of time, selecting a second subgroup and processing it for a period of time, selecting a third subgroup etc until all 128 signals had been processed; and then starting over.

A convenient subgroup size is 8 signals, a convenient processing time for any selected subgroups is one full rotation of the rotor shaft.

The system operates with a rotor shaft rotation rate from 1000 to 1800 rpm. Each subgroup of 8 signals would than be processed for a period of 33 to 60 milliseconds. A complete cycle through all 128 signals would be accomplished in 0.528 to 0.960 seconds, depending on rotor shaft rotation rate.

This bank (subgroup) switching approach was acceptable to NASA. In fact, NASA had previously used this basic approach to effectively increase the signal handling capability of mechanical slip rings and was very satisfied with the results. In NASA's experience the only problem was system recovery time when bank switching occurred. NASA experienced a 20 millisecond period during which data was invalid. Thus two or more rotor shaft rotation times were required for processing of each subgroup.

In this system a "data not valid" period of 1 millisecond per bank switch was desired. The "data not valid" period is determined by the settling time of the antialias filter following a step function input. The selected antialias filters met this requirement (Section 5.1 of this report).

To maximize system flexibility, the determination of what bank of signals would be processed at any given time was placed under NASA control. This was accomplished by reserving one word of the 8 word uplink command channel for bank switch address control. Thus the total number of signals to be processed and the time duration for any selected bank is entirely determined by NASA.

The processing of 128 signals through the beanie could now be accomplished with a single A/D chain preceded by 8 antialias filters and eight 16/1 bank selection multiplexers (Figure 5-17). The timing parameters became 8 MHz bit rate for the downlink serial data (12 data bits, 7 I.D. bits, and 1 overflow bit every 2.5 microseconds); and an A/D chain word rate of 400 KHz, 1/2 the original 800 KHz word rate.

The reduction in the word rate from 800 KHz to 400 KHz doubled the time available for A/D conversion. Using the components previously selected, the A/D chain could now be

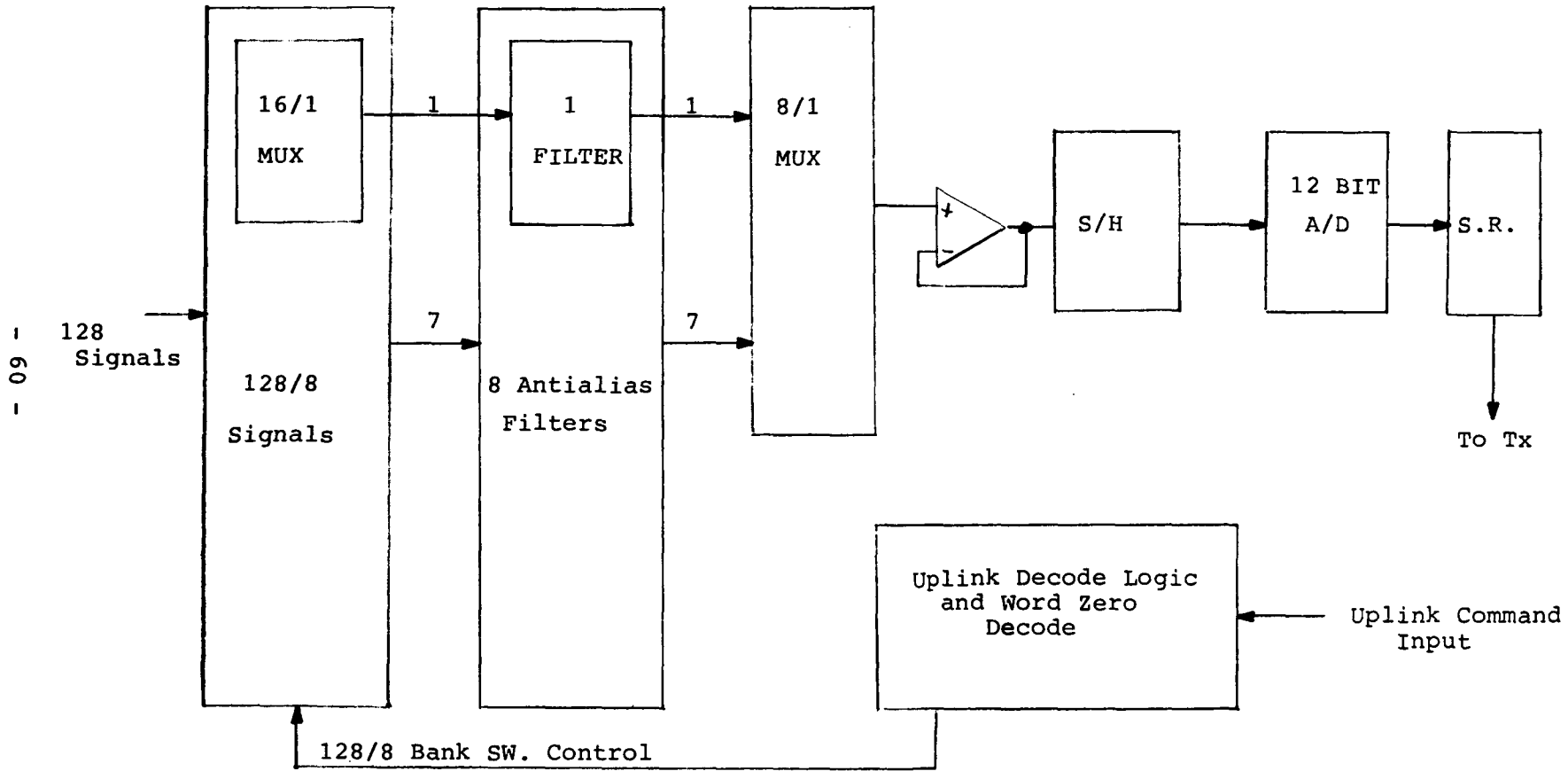


Figure 5-17. Final System Decoder Schematic For One of Two Identical Channels

operated in a non-pipelined mode: one in which no switching action takes place from the time the sample and hold amplifier is switched to "hold" until the A/D conversion process is complete. This provides significant additional noise immunity.

One additional factor remained to be considered. Realtime continuous monitoring of input signals is not possible with the time multiplexed bank switching described above. This desired feature was obtained by providing two identical signal processing channels in the beanie. The two channels are completely independent.

The bank selection for each channel is independently controlled by NASA via word zero of the uplink command channel. Thus one channel (Channel A) may be bank switched every rotor shaft revolution, while the second channel (Channel B) may remain on one selected bank for an extended period of time.

The data from each channel is independently optically coupled through the optical slip ring assembly to the stationary outside world. It is transmitted via coax cables to a Local Station.

At the Local Station Channel A data is decoded and transmitted to NASA in time multiplexed parallel digital form.

Channel B data is decoded and, via a D/A converter process, reconstructed in analog form and transmitted to NASA as 8 analog signals.

6.1 UPLINK COMMAND CHANNEL

NASA supplies command data to the Local Station. The Local Station formats the data and serially transmits it to the beanie via a fiber optic cable through the center of the optical slip ring assembly (Figure 3-10). An eight word capacity is provided. Each word provides 8 data bits and 3 I.D. bits. Word zero is reserved for bank selection control of the two downlink channels.

In the beanie, the uplink data is bit and word synchronized. The word zero is decoded for downlink bank selection control. All eight words are presented to an output port to NASA in time multiplexed parallel form.

Confidence in the data decoded is maintained by requiring the correct sequences of I.D. bits through several words before accepting the data as valid.

The serial data bit rate to the beanie is 1 MHz.

6.2 LOCAL STATION

The Local Station is the interface between NASA and the optical slip ring/beanie mounted on the rotating rotor shaft. The uplink command data is received from NASA in parallel form, formatted as described in Section 6.1 and serially transmitted to the beanie via the optical slip ring. The analog channel bank selection data can be front panel manually entered if desired.

The two downlink channels serial data streams are received at the Local Station and independently processed as required. Each channel data stream is bit and word synchronized and a confidence level established. Word synchronization is accomplished by taking advantage of the sequential nature of the three least significant bits of the word I.D. Each word received has an I.D. value one greater than the previous word I.D. The incoming data stream is shifted through a shift register and the parallel output is periodically examined. When a correct I.D. match is obtained word synchronization is assumed.

Confidence in the word synchronization is established by initially requiring a minimum of 7 successful I.D. matches before the data is acceptable as valid. Thereafter an unsuccessful I.D. match results in declaring the data invalid until subsequent I.D. matches re-establish confidence. The implementing circuitry is weighted toward lack of confidence. After establishing confidence, a single error in I.D. match requires four successful I.D. matches to restore confidence. Two successive errors require six successful I.D. matches to restore confidence. Three successive I.D. matches indicate loss of word synchronization. In the latter case, a full "start up" resynchronization is initiated. This requires approximately 50 microseconds to restore full confidence.

Channel A data is transmitted to NASA in time multiplexed parallel word form, plus a data valid strobe. A word consists of 12 data bits, seven I.D. bits, and one overflow bit (A/D converter input out of range) (See Figure 5-18).

The Channel B data is passed through a D/A converter (Figure 5-19). The D/A converter output is a time multiplexed sequence of eight analog signals. The I.D. associated with each D/A converter word input is decoded and controls the state of 8 sample and hold amplifiers to demultiplex the signals. Each sample and hold amplifier output passes through an antialias filter to a linedriver. The 8 analog signals are then transmitted to NASA in analog form. Each analog signal also has an associated overflow bit transmitted in digital form.

6.3 SERIAL DATA TRANSMISSION FORMAT

Each of the three optically coupled inputs to the optical slip ring assembly illuminate detectors whose outputs drive coaxial cables. The data at the detector outputs is in NRZ form

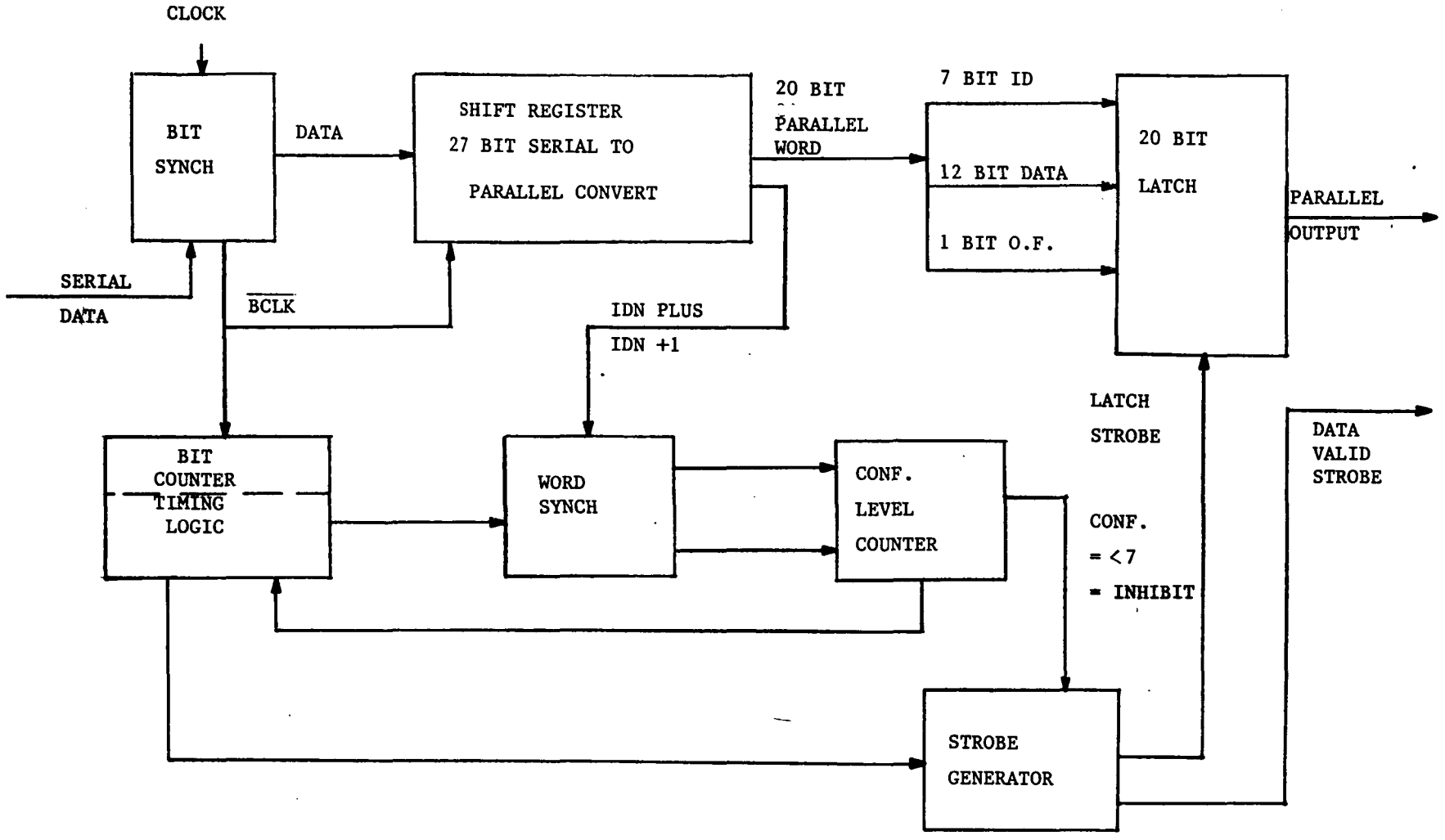
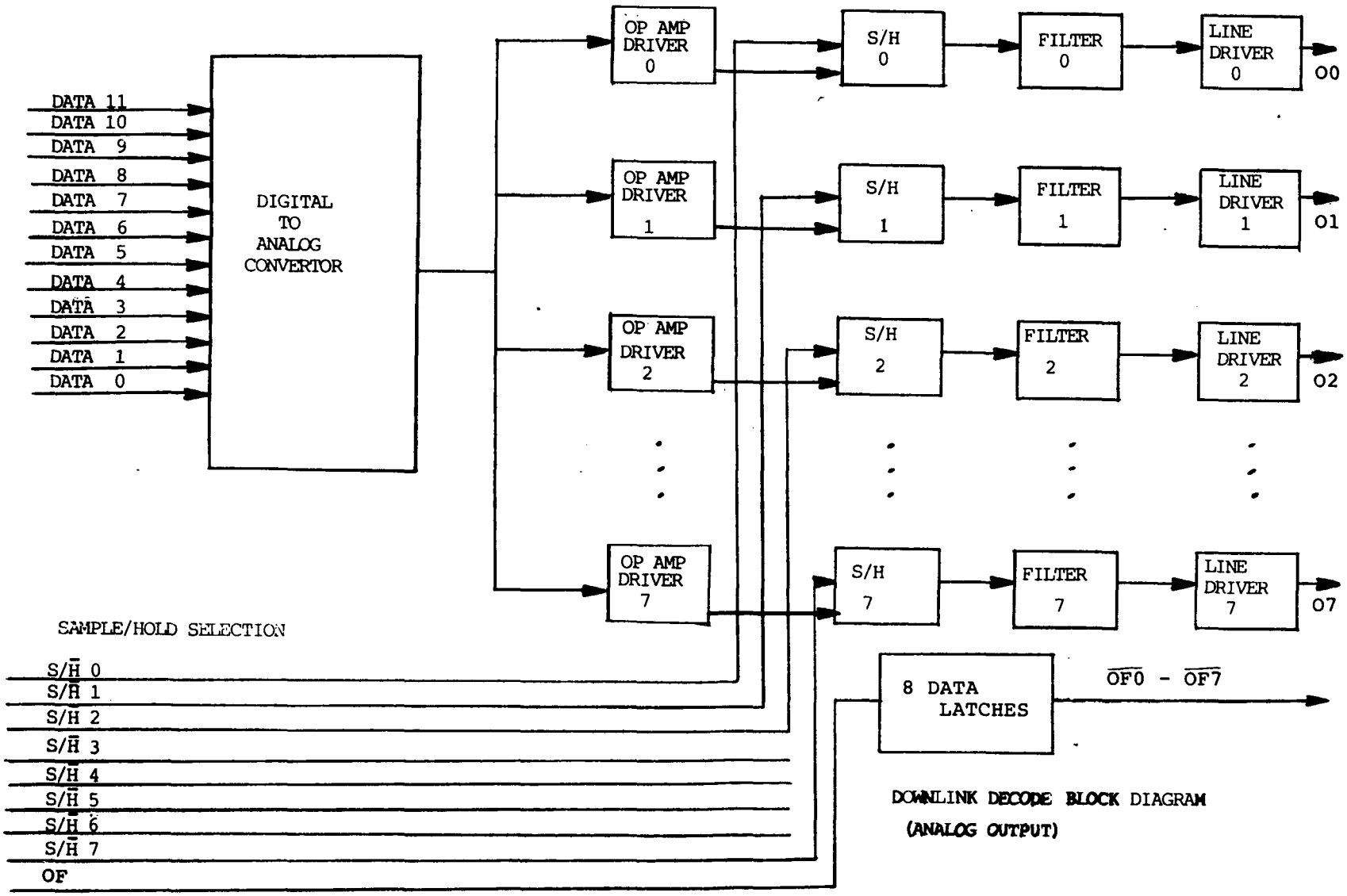


Figure 5-18. Decoder Schematic



DOWNLINK DECODE BLOCK DIAGRAM
(ANALOG OUTPUT)

Figure 5-19

plus a D.C. offset added by the detector and subject to drift with temperature variations. To reliably receive and synchronize the data streams the D.C. offset must be removed. The outputs of the detectors are therefore A.C. coupled to the coax. However, NRZ data coupled through a capacitor results in large D.C. offset variations as a function of the data content. This effect is overcome by making the coupling capacitor small enough to differentiate the NRZ waveform. This effectively removes the D.C. offset. The resulting signals (600 to 800 millivolts peak to peak in the final system) are transmitted over the coax to a receiver. A dual comparator threshold detects the positive and negative going signals. The dual comparator outputs then "set" - "reset" a flip flop to recreate the NRZ signal. The NRZ signal is supplied to bit and word synch circuitry. Figure 6-1 illustrates a typical differentiated signal in a bench setup.

The receiver bit synch circuitry has been designed to tolerate a large variation in pulse length of an NRZ bit (sequence zero, one, zero). For the 8MHz downlink data, the bit time bin is 125 nanoseconds. The bit synch circuitry will tolerate a pulse length variation from 30 to 125 nanoseconds.

The uplink channel bit time is 1 microsecond. Its bit synch circuitry will tolerate a pulse length variation from 500 to 1000 nanoseconds.

7.0 PACKAGING

7.1 BEANIE

In its final configuration, the beanie consists of seven 8 inch diameter P.C. boards. Each has a 2 inch diameter hole in the center. The beanie cover alos has a 2 inch diameter hole in its top center. When spinning, air enters through the central hole and exits through the openings in the sides of the beanie cover.

Figure 7-1 is a picture of the assembled beanie with cover in place. The package is 9 inches in diameter and 6 inches high, excluding a raised mounting structure at the bottom. It weighs approximately nine pounds and consumes about 65 watts, including 10 watts of transducer power.

The P.C. boards consist of one power regulator board which supplies the beanie and 5 volts at 2 ampere to the NASA transducers; one A/D chain board; one uplink decoder and dowlink transmitter board; and four bank switching and antialias filtering boards.

Figure 7-2 is a picture of the assembled beanie without the cover.

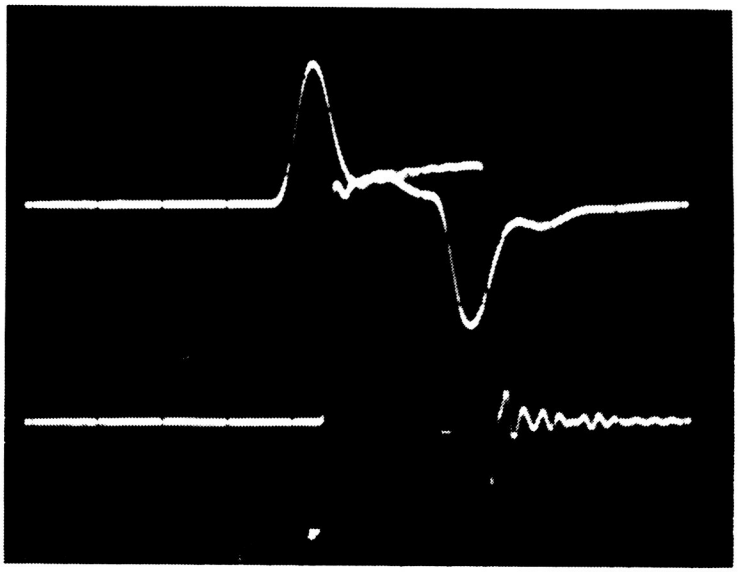


Figure 6-1. Detector Output And Reconstructed Signal

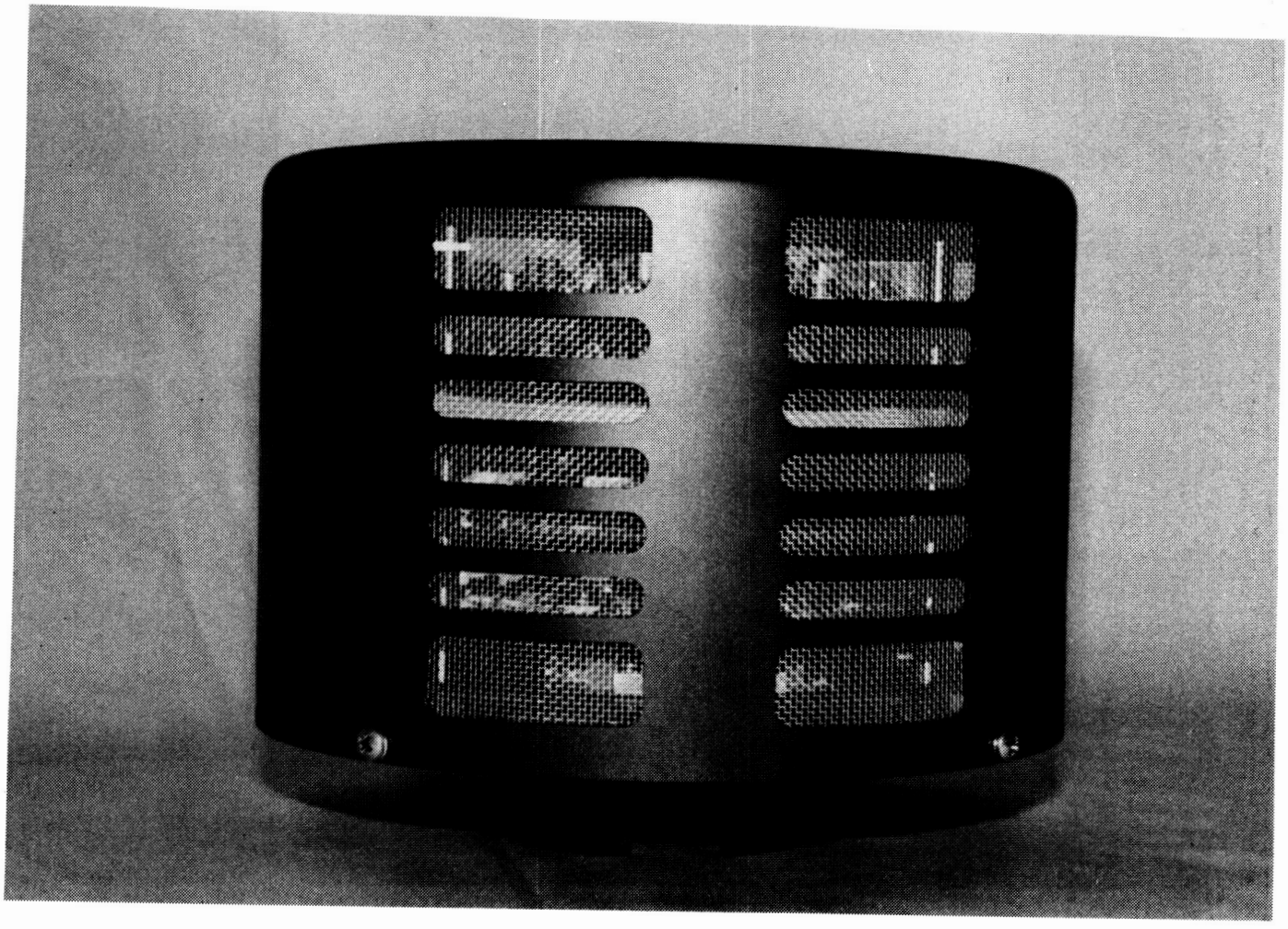


Figure 7-1. Beanie

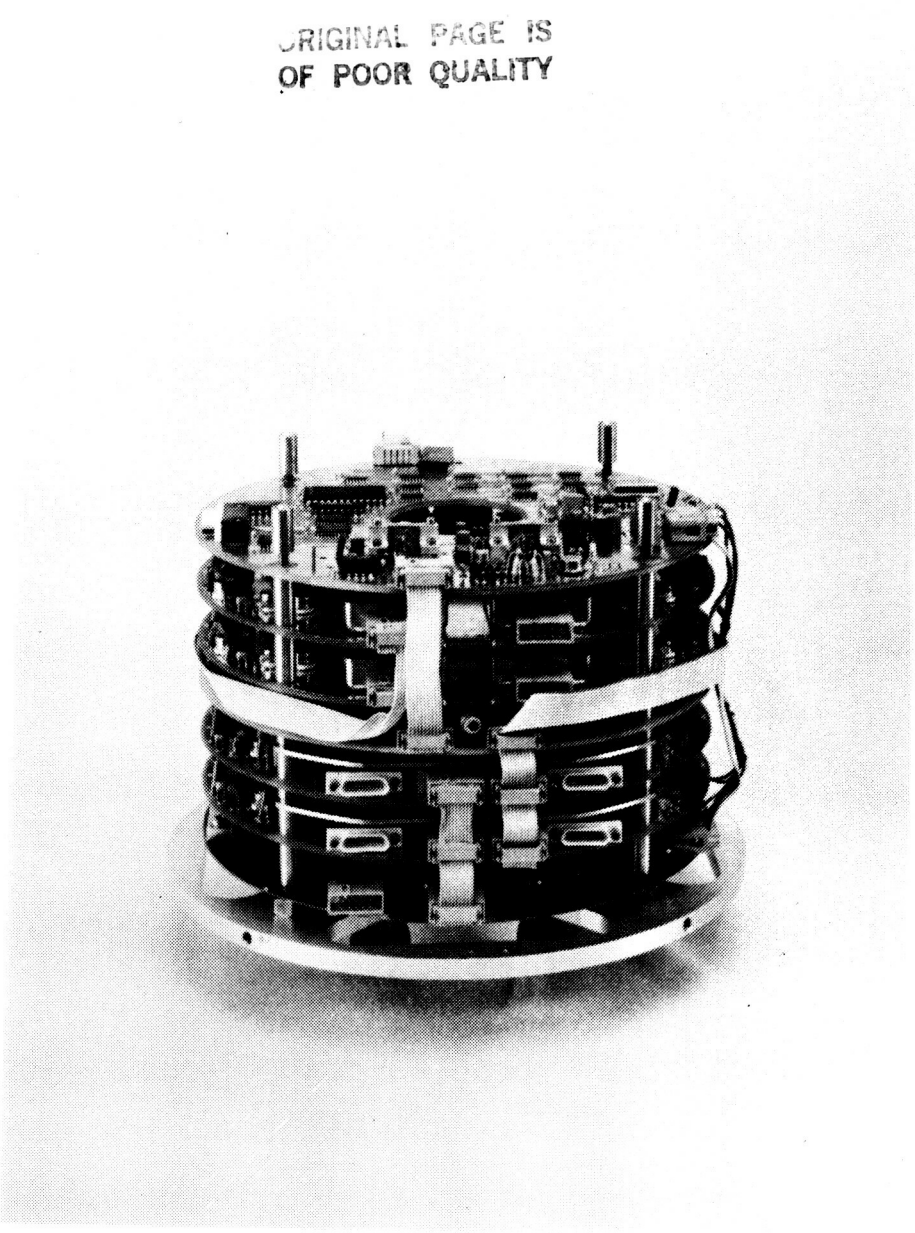


Figure 7-2. Beanie With Cover Off

The four vertical posts (Figure 7-2) are of 0.2 inch diameter stainles steel with spacers to maintain board separation. Each board is statically balanced. The filter board balance plates are attached to the vertical posts adjacent to each filter board.

Figures 7-3 through 7-6 are pictures of the individual board types in the beanie.

7.2 OPTICAL RING ASSEMBLY

Figure 7-7 is a picture of the optical slip ring assembly. It is 2 inches in diameter for the major part of its 8.5 inch length, with a 3 inch diameter poriton housing the power slip rings. It consumes approximately 1.6 watts in its three detector circuits.

The power leads, coax, and optical cables exiting the top of the unit are rated at 105°C operating temperature or higher.

The main body of the unit is constructed of stainless steel with a top cone of aluminum and a bottom brush housing of plastic.

The weight of the unit was not measured prior to delivery. However, a roughly equivalent earlier model weighs 2 pounds.

7.3 LOCAL STATION

THe Local Station is a 19 inch rack mounted unit. As such, no attempt was made to reduce size or power consumption. The unit is approximately 11 inches high by 18 inches deep. It contains all the Local Station circuity for both the downlink channels and the uplink command channel. It also houses all power supplies for the sytem.

The Local Station consumes 265 watts including 25 watts for its own P.C. boards, powerfor the beanie circuitry, power for the optical slip ring and losses for the linear power supplies.

Various test points and system operating condition indicators are contained on the front panels. An analog channel manual Bank Select provision is also front panel accessable. Figure 7-8 is a picture of the Local Station.

The Local Station is normally located 75 feet from the optical slip ring assembly and the beanie.

8.0 LABORATORY TESTING

8.1 LOCAL STATION

The Local Station is rack mounted and no severe environmental requirements exist. The power supplies limit the

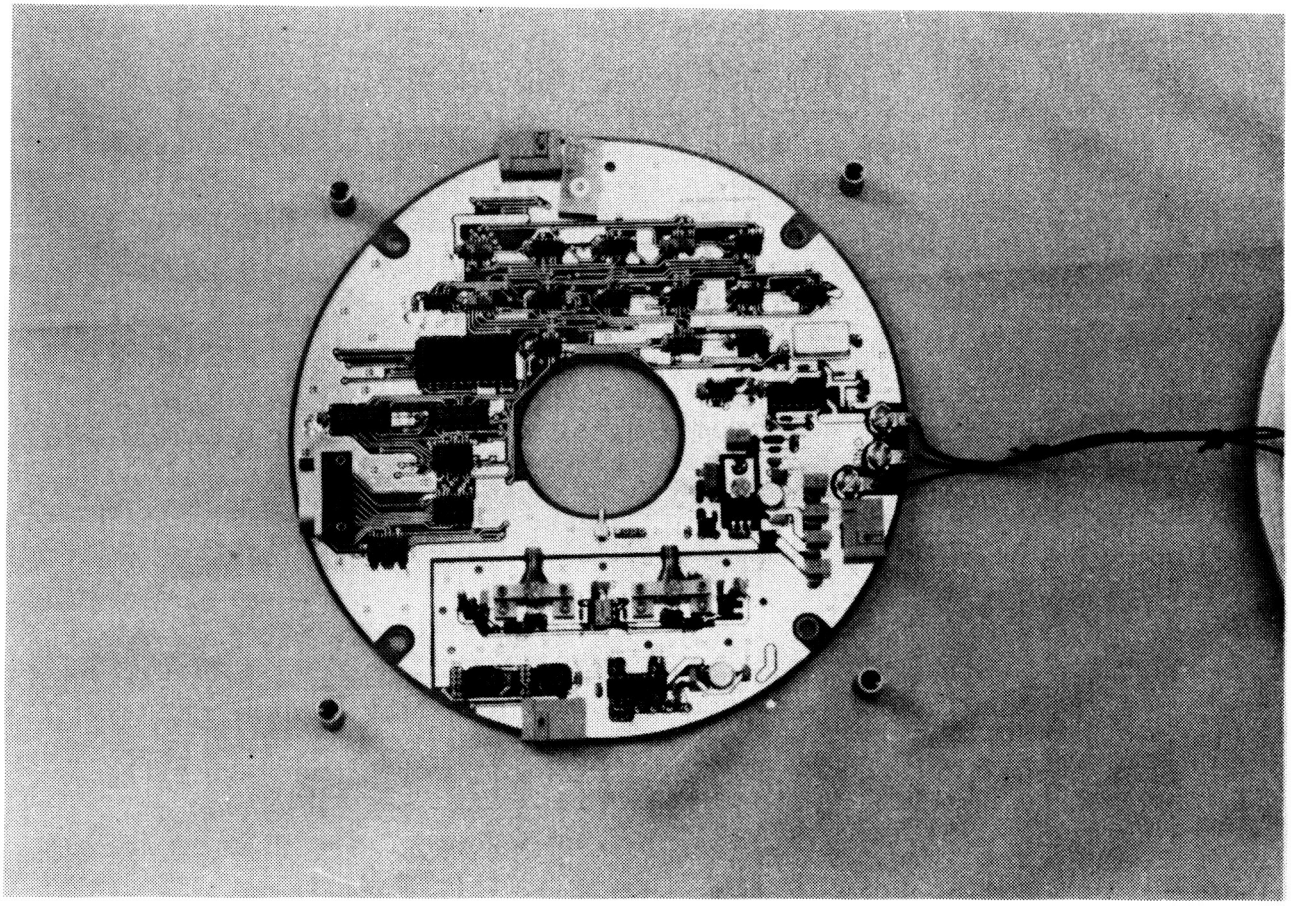


Figure 7-3. Tx, Rx Board

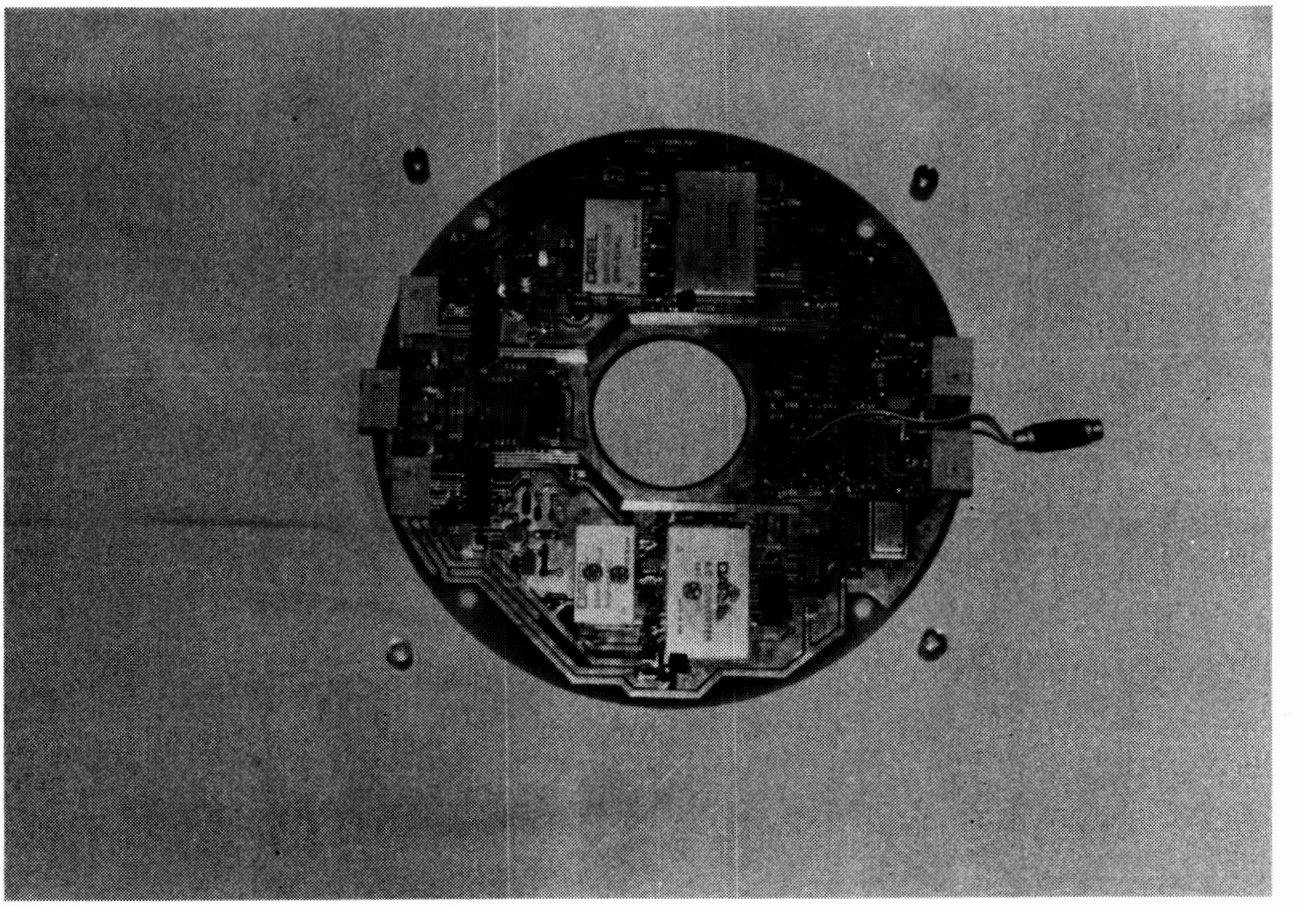


Figure 7-4. A/D Board With Bench Test Connector

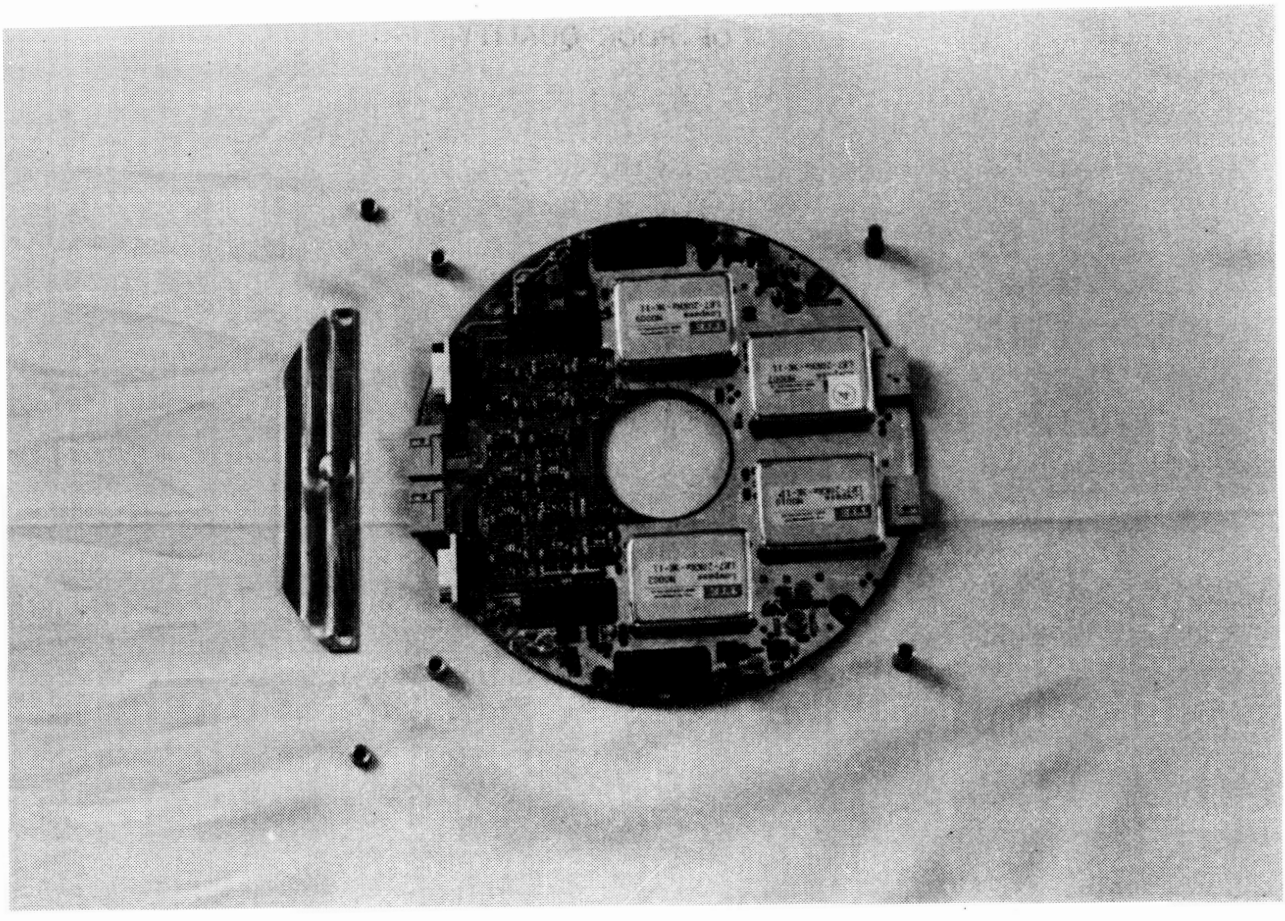


Figure 7-5. Filter Board and Balance Plate

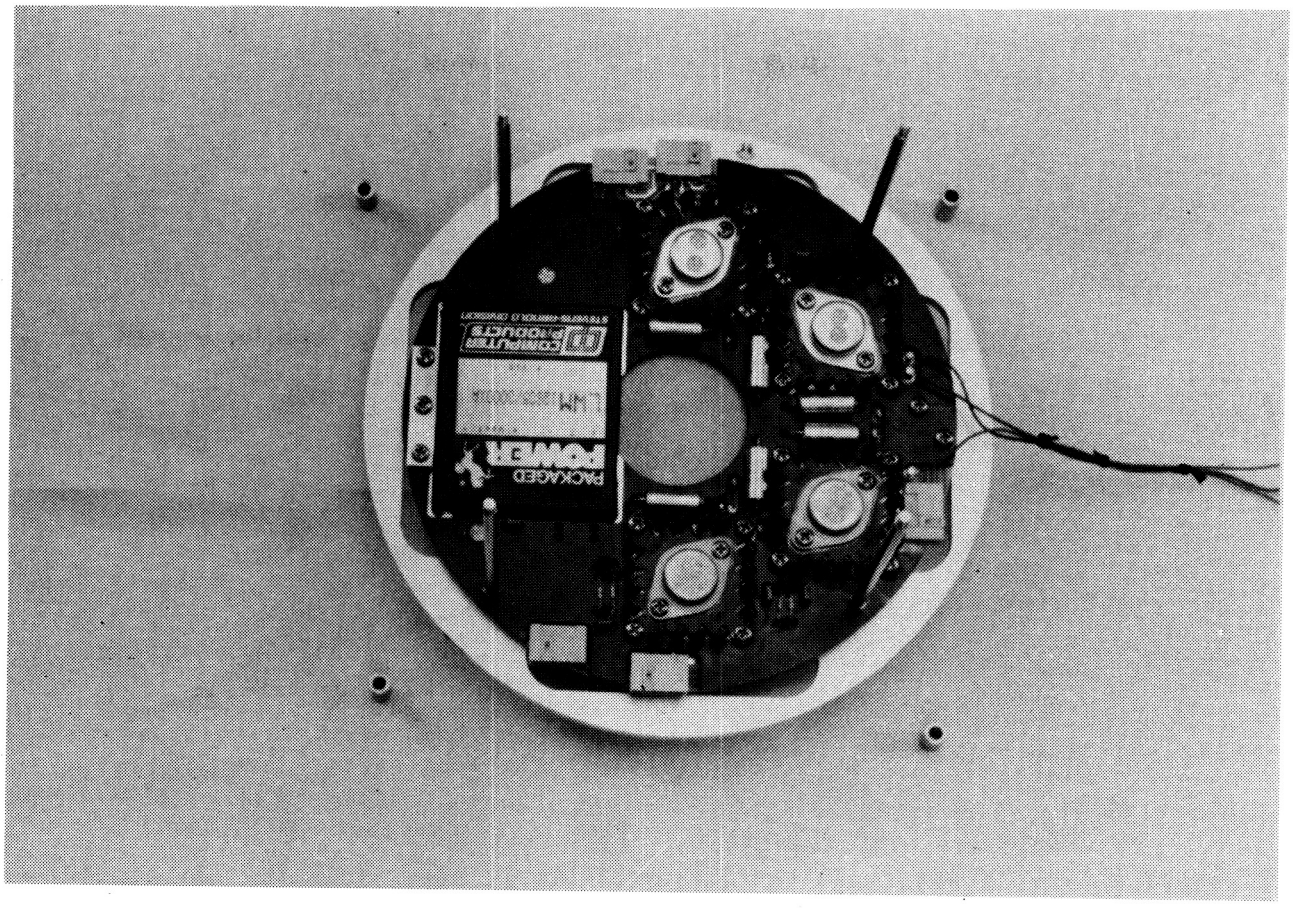


Figure 7-6. Mounted Regulator Board

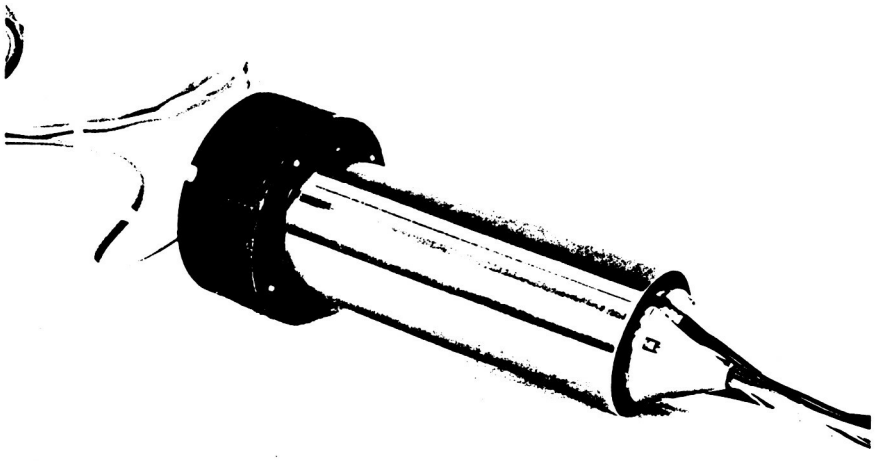


Figure 7-7. Optical Ring

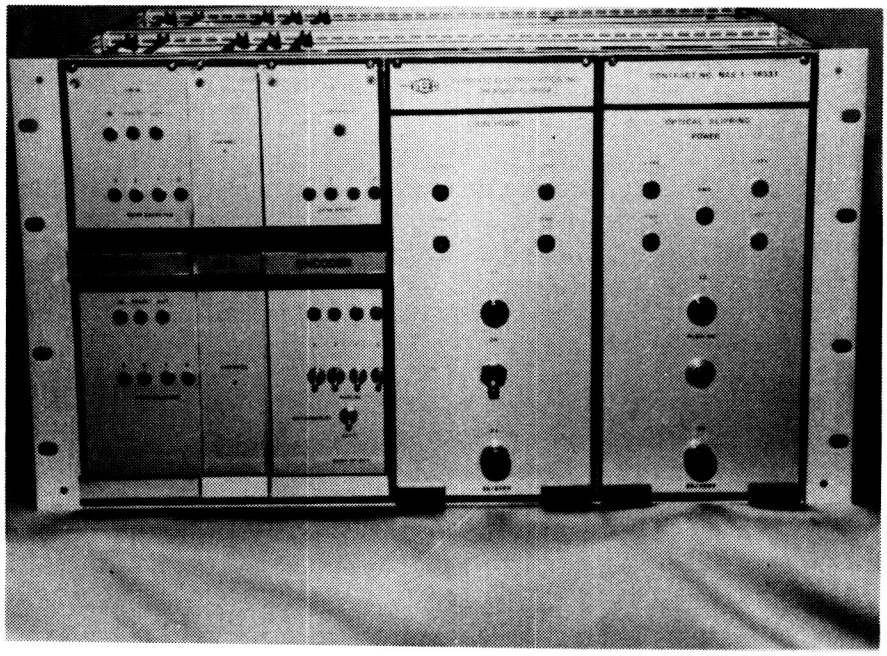


Figure 7-8. Local Station

acceptable temperature rise to 50°C ambient. Normal operation is not expected to approach this temperature.

8.2 OPTICAL SLIP RING ASSEMBLY

The optical slip ring assembly was operated at up to 58°C internal ambient temperature. This represents an upper limit.

The plastic fiber used in the optical slip ring softens at 71°C.

The temperature differential between the detector P.C. board area and the assembly outer shell (under the protective shield) is about 15°C. The maximum operating rating for P.C. mounted components is 70°C.

This sets the maximum outer shell temperature (where the plastic fiber is located) at 70°C - 15°C = 55°C.

Lower outer shell temperatures are highly desirable to obtain long term component life. An outer shell maximum temperature of about 40° or lower is desirable.

Sufficient cooling gas must be supplied to maintain the above conditions at all times.

The optical slip ring was tested under rotating conditions by mounting it in a simulated rotor shaft, mounting the beanie in it position on top of the rotor shaft, and spinning the assembly up to 2000 rpm. The uplink and downlink channels were exercised (while spinning). External test equipment was used to evaluate the equipment operation, including error rate on the downlink channels. The signals received from the optical slip ring were examined on an oscilloscope for any sign of signal deteriation. The entire functional testing was successful.

Figures 8-1 and 8-2 show the spin test setup with the beanie and optical ring mounted in place. During functional testing, a known signal source test waveforms circuit was mounted on top of the beanie cover (Figure 8-3).

8.3 BEANIE

In addition to the functional spin testing of the beanie desribed in Section 8.2 above, the beanie internal structure stability was examined from 300 rpm to 2000 rpm. A strobotac was used for the visual examination.

A previous beanie structure of considerably less stiffness was rotated up to 2700 rpm, creating forces 2-1/4 times those experienced at 1800 rpm. That structure did exhibit a swaying motion. (without the cover in place) of about 1/16 inch peak to peak from 1400 to 2700 rprm. It did, however, stay in one piece.

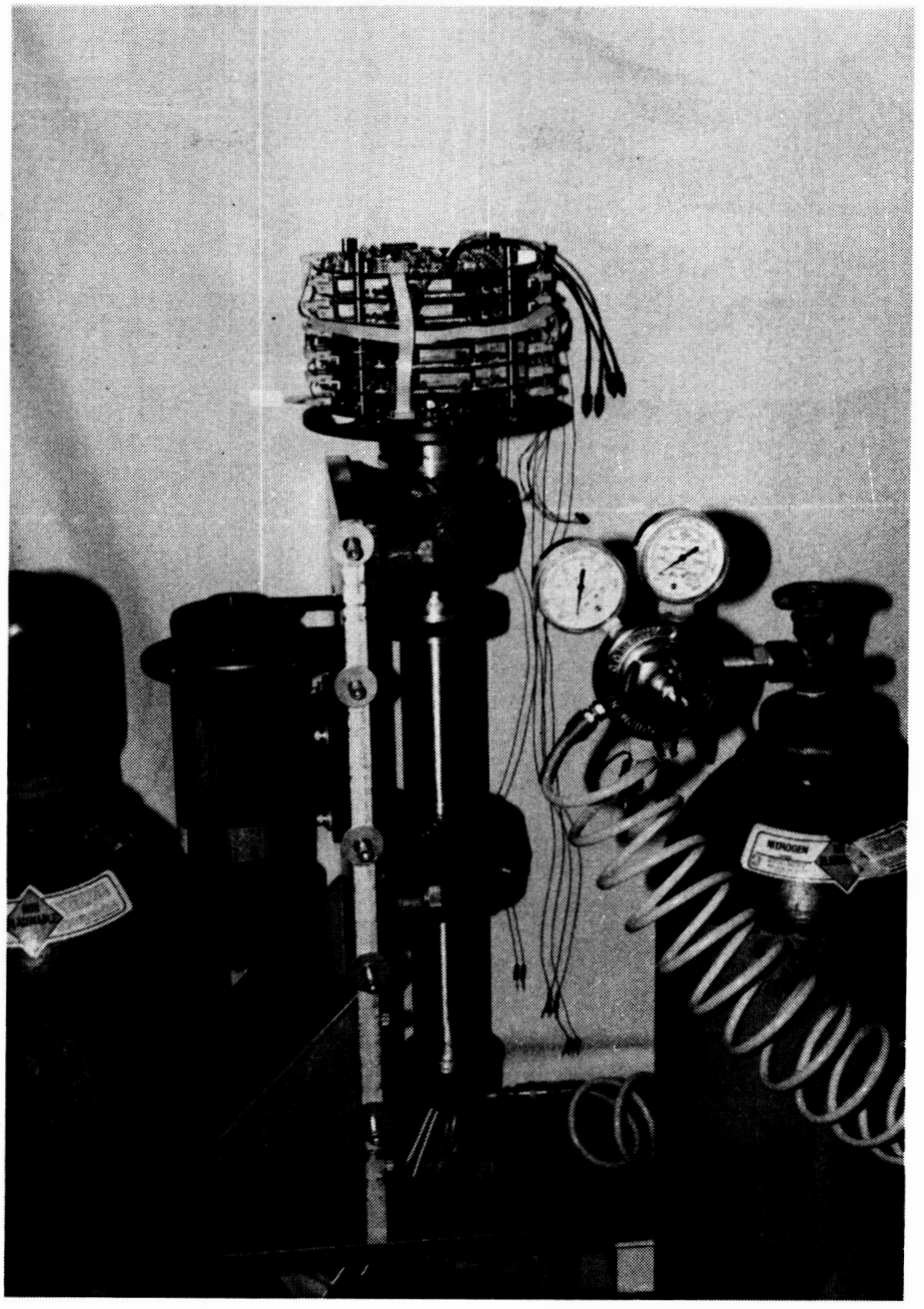


Figure 8-1. Spin Test Setup

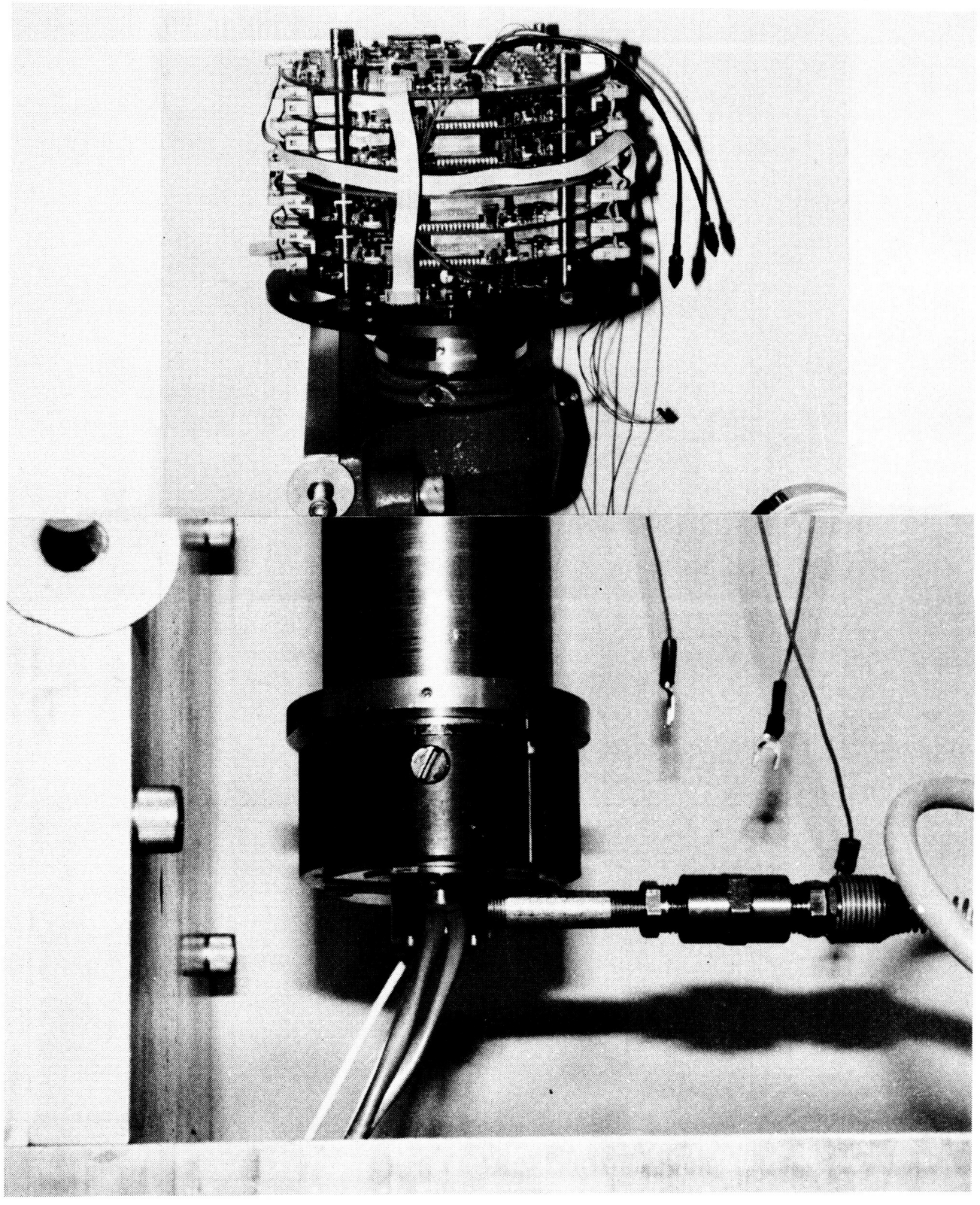


Figure 8-2. Spin Test Setup

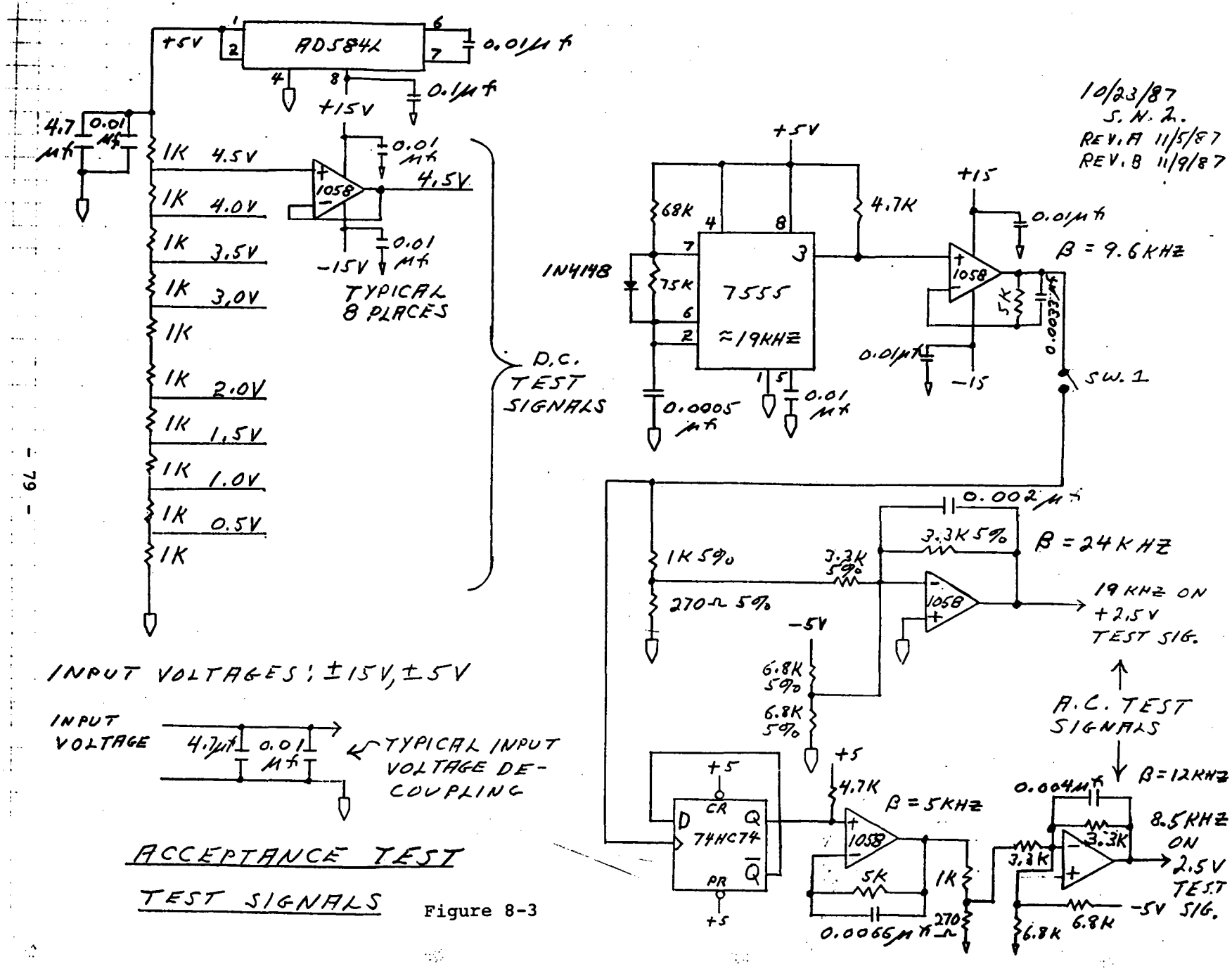


Figure 8-3

No structural damage was observed on disassembly and inspection of the component parts.

All components in the beanie are rated for operation to 70°C ambient temperature except the laser diodes which are rated at 60°C case temperature.

Operation of the beanie with its cover on and not spinning may create ambient hot spots exceeding component specifications. For this reason and for long term reliability the non-spinning beanie should not be operated without a supply of cooling air. A standard 12" fan blowing through the slots in the beanie cover provides a benign environment.

When spinning at 100 rpm or greater the beanie creates its own cooling air flow and no fan is needed.

The beanie dissipates approximately 65 watts.

8.3.1 BEANIE COMPONENTS TESTING

The antialias filter was individually temperature tested as reported in Section 5.1 of this document.

The infrared laser transmitter and its temperature compensating circuit was tested for optical power output over the range from 21°C to 50°C. The variation in powr ouptut was measured by an optical detector located outside of the temperature chamber. The total variation detected output was +4% to -6%. The tabular data is shown in Table 8-1.

The accuracy of the final A/D chain was tested at room temperature at five different input voltages from 0.2 to 4.8 volts. The A/D chain consists of the 8/1 multiplexer, buffer amplifier, sample and hold amplifier, and A/D converter. The maximum absolute error measured was minus 2.1 LSB.

A temperature drift test was conducted on the A/D chain. The multiplexer was continuously switched between two input signals at the system word rate. The two input signals were 0.2004 volts and 4.8009 volts.

Over an ambient temperature range from 20°C to 60°C the maximum drift observed was +3 LSB (0.07%). The ambient temperature was stable for 30 minutes prior to each reading. The tabular data is shown in Table 8-2.

A temperature profile was run on the assembled beanie while spinning at 1000 rpm. The points monitored were the case temperature of the power regulator, the case temperature of the A/D converter, the case temperature of the sample and hold amplifiers, the surface temperature of the laser transmitter

TABLE 8-1

DOWNLINK Tx TEMPERATURE TEST

TEMPERATURE	DUTY CYCLE	LASER PEAK DRIVE CURRENT	LASER CIRCUIT DRIVE VOLTAGE	DETECTOR PEAK VOLTAGE OUTPUT
21°C (Stabilized)	5%	80 Ma	5.05 V	108 mV
25°C (30 Min)	5%	80 Ma	5.04 V	112 mV
30°C (30 Min)	5%	82 Ma	5.1 V	112 mV
35°C (30 Min)	5%	83 Ma	5.15 V	110 mV
40°C (30 Min)	5%	84 Ma	5.2 V	110 mV
45°C (60 Min)	5%	86 Ma	5.25 V	108 mV
45°C (30 Min)	25%	86 Ma	5.255V	108 mV
45°C (30 Min)	50%	88 Ma	5.258V	106 mV
50°C (30 Min)	50%	88 Ma	5.3 V	102 mV

TABLE 8-2

A/D CHAIN TEMPERATURE TEST

INPUTS: Hi = 4.8009 Volts
Lo = 0.2004 Volts

TEMPERATURE	HI OUPUT	LO OUTPUT	HI ERROR	LO ERROR
20°C	4.797	0.1978	-3.2 LSB	-2.12 LSB
30°C	4.8006	0.2002	-0.25 LSB	-0.16 LSB
40°C	4.7994	0.1990	-1.23 LSB	-1.1 LSB
50°C	4.7994	0.1996	-1.23 LSB	-3.1 LSB
60°C	4.7994	0.1990	-1.23 LSB	-1.15 LSB

housings, the case temperature of antialias filter, and the case temperature of mulitplexers.

After 1 hour and 20 minuted of operation the system was shut down.

Inspection of tempel labels used for temperature indicators showed no temperature reaching 38^{o}C. An excellent result.

9.0 ACCEPTANCE TESTING

Acceptance tests were run for NASA at SEO. The acceptance test procedure (ATP) and the results are contained in Appendix A and B respectively.

Some additional tests were performed at NASA's request. The results are included in the ATP results.

An important deviation from the written ATP occurred in Section 14 of the ATP. The procedure calls for the beanie power to be off during the mechanical integrity spin test of Section 14.1. The power to the beanie was deliberately left on during this test.

The performane of the acceptance tests was continuously monitored by Mr. John Berry of NASA, and by Mr. Christopher Mangsen of SEO's Quality Control Department.

APPENDIX A

ACCEPTANCE TEST PROCEDURE

SCHWARTZ ELECTRO-OPTICS, INC.
3404 North Orange Blossom Trail
Orlando, Florida 32804

Telephone No.
(305) 298-1802

Fax No.
(305) 297-1794

OPTICAL FIBER DATA TRANSFER SYSTEM

ACCEPTANCE TEST PROCEDURE

CONTRACT: NAS1-18331

TABLE OF CONTENTS

TABLE OF CONTENTS (CONT'D)

1.0 INTRODUCTION

This acceptance test is designed to provide assurance that the Optical Fiber Data Transfer System meets the operational and performance requirements of the contract NAS1-18331.

The total system involves 128 signal inputs and over 256 possible signal outputs. It is not practical to exercise and examine all of these signals in the acceptance test. The acceptance test does provide typical performance results for a representative set of input signals.

2.0 TEST EQUIPMENT USED

H.P. 3468A Multimeter

IWATSU Oscilloscope (200 MHz)

H.P. 3312A Function Generator

3.0 TEST SETUP

The basic test setup is shown in Figure 3-1, Figure 3-2, and Figure 3-3. In some cases special test signals other than those of Figure 3-3 are used. Details of the special test signals and their use are described in the appropriate test section.

4.0 GENERAL SYSTEM OPERATION

This is a general purpose subjective test for basic system operation.

Set SW1 to closed.

Inject a radio output into D4. Adjust the signal to avoid audio signal peaks of greater than +5 volts and less than zero volts.

Attach a D.C. isolated speaker to the Channel B output Bank 1, D4.

Set Channel B to Bank O.

Set Channel A to Bank O, D4.

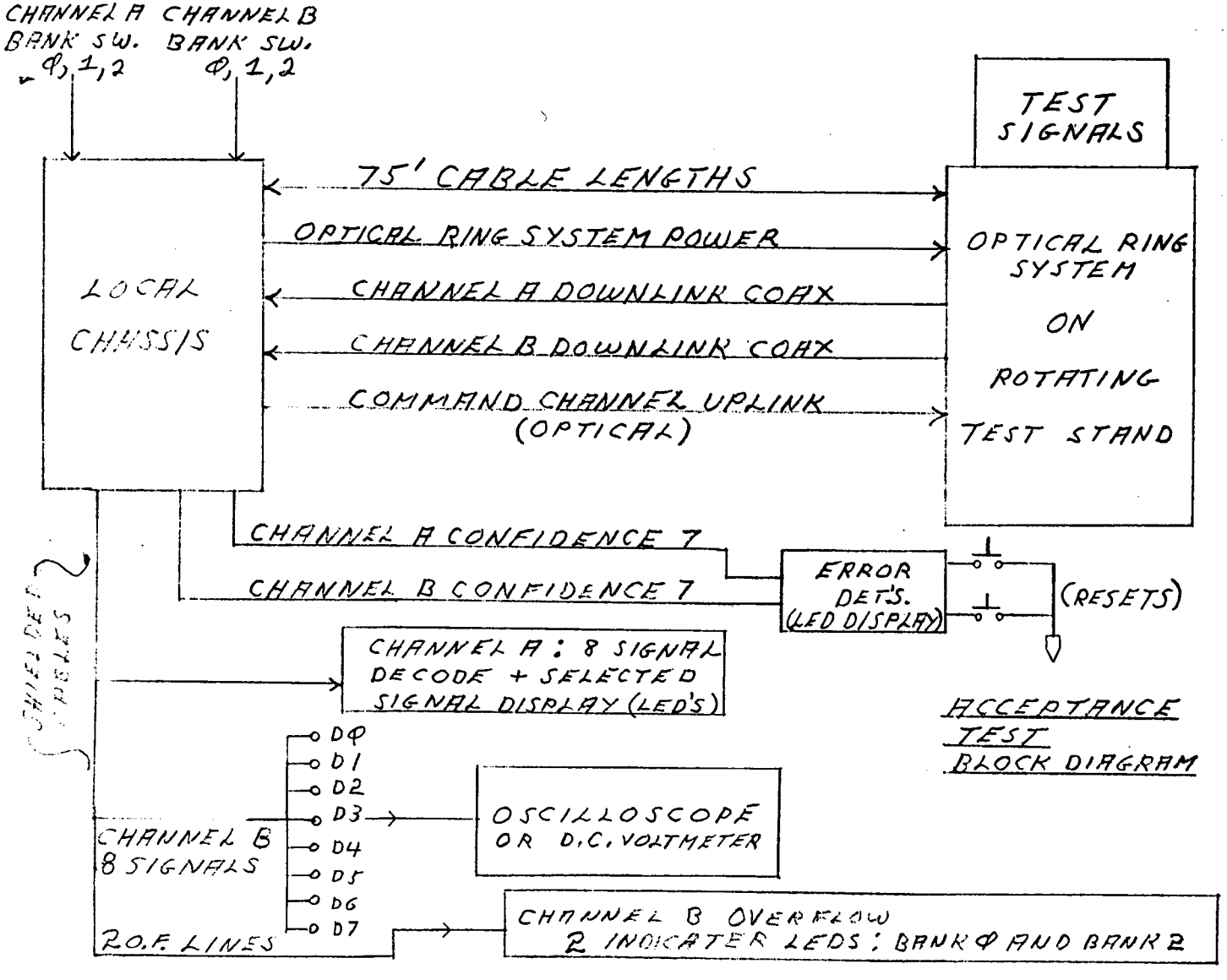
Monitor Channel B, D4 with an oscilloscope.

Turn on the radio. Hear the radio playing through the entire system without apparatus distortion or more.

Note the pseudo random portion on the Channel A led display and on the oscilloscope.

FIG. 3-1

10/22/87
S.H.m.
REV. A 11/5/8.



ACCEPTANCE TEST BLOCK DIAGRAM

TEST SIGNALS FOR ACCEPTANCE TEST

11/9/87
REV. A

CHANNEL A:

BANK SELECT Φ:

DΦ	≈	4.5V	= 1 1 1 0 0 1 1 0 0 1 1 0
D1	≈	4.0V	= 1 1 0 0 1 1 0 0 1 1 0 0
D2	≈	3.5V	= 1 0 1 1 0 0 1 1 0 0 1 1
D3	≈	3.0V	= 1 0 0 1 1 0 0 1 1 0 0 1
D4	≈	2.0V	= 0 1 1 0 0 1 1 0 0 1 1 0
D5	≈	1.5V	= 0 1 0 0 1 1 0 0 1 1 0 1
D6	≈	1.0V	= 0 0 1 1 0 0 1 1 0 0 1 1
D7	≈	0.5V	= 0 0 0 1 1 0 0 1 1 0 1 0

BANK SELECT 1: ≈2.5V + 1VPP A.C. SIGNAL

DΦ	≈	0.5V	WITH SW. 1 CLOSED: D.C. LEVEL WITH SW. 1 OPEN.
D1	≈	9.5KHZ	
D2	≈	19KHZ	
D3	≈	9.5KHZ	
D4	≈	19KHZ	
D5	≈	9.5KHZ	
D6	≈	19KHZ	
D7	≈	9.5KHZ	

CHANNEL B:

BANK SELECT Φ:

SAME AS CHANNEL A

BANK SELECT 1:

SAME AS CHANNEL A

UNUSED SIGNAL INPUTS:

FLOATING

FIG. 3-2

Reset both error indicators.

Note that they remain reset, indicating error free operation.

5.0 CROSSTALK/NOISE

The purpose of this test is to evaluate crosstalk between adjacent signals in a common bank and to determine the noise floor for this setup.

Set Channel A "Bank Select" to Bank 0.

Set Channel B "Bank Select" to Bank 1.

Remove the radio inputs to "Bank Select" 0 signal D0 and replace it with input of Figure 3-2 (≈ 4.5 V.) on D0.

Remove the speaker from the Channel B signal D0 output.

Close Sw1 and verify existence of 9.5 and 19 KHz by monitoring the Channel B output signals D3 and D4. Record the amplitudes of the 9.5 and 19 KHz signals.

Open Sw 1. This removes the A.C. signals.

Monitor the output of Channel B signal D0 with the oscilloscope with A.C. input coupling.

Measure and Record the noise floor of the analog output for this setup.

Close Sw. 1 and note any steady state change in the noise floor. This is the crosstalk from seven A.C. signals to the eighth signal in a common bank. This includes cross talk occurring externally to the equipment under test. Record the crosstalk value.

Open Sw 1

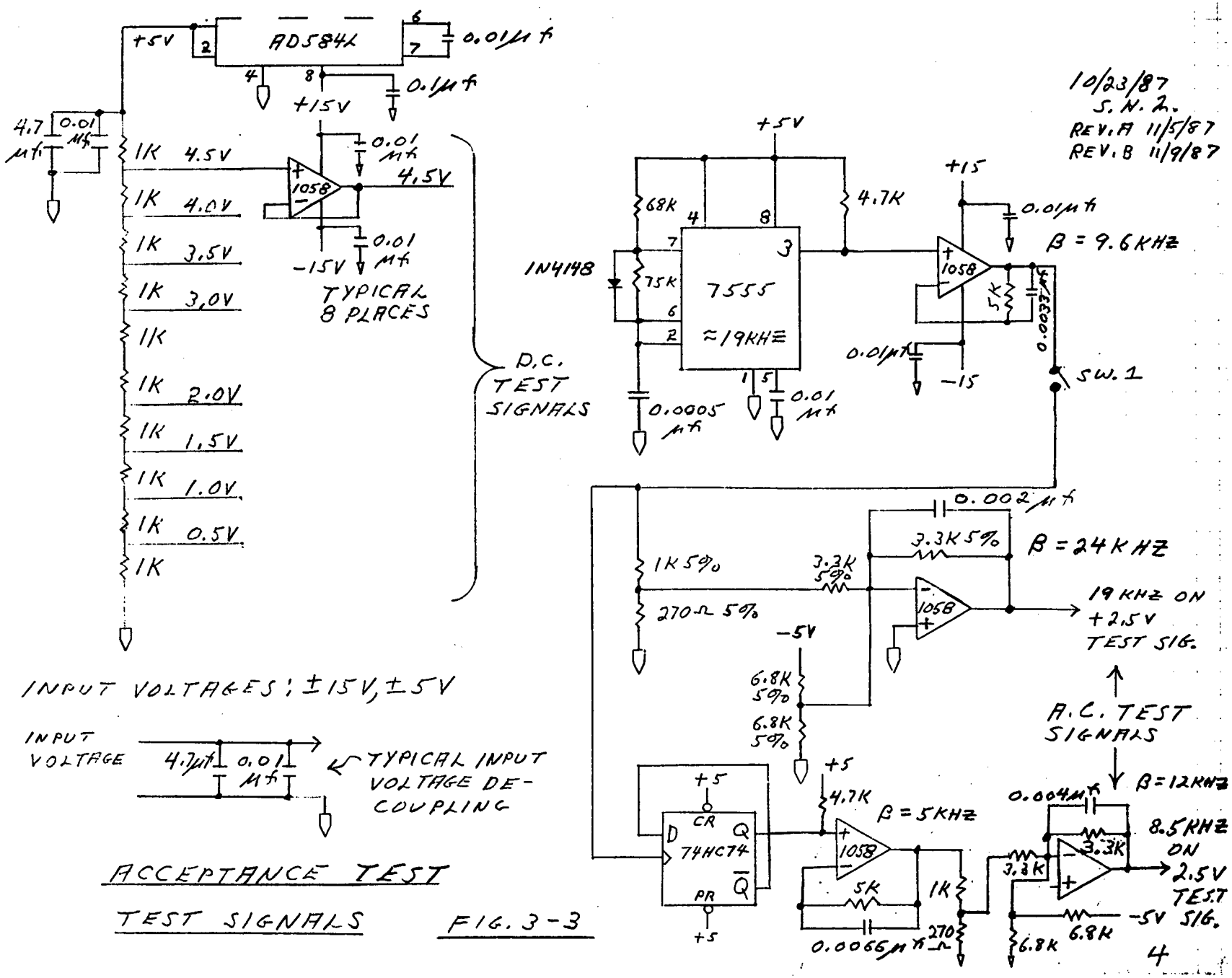
Set Channel A "Bank Select" to Bank 1.

Set Channel B "Bank Select" to Bank 0.

Set Channel A "Signal Decode" switch to signal D0.

Observe the signal D0 led display and estimate the noise level in L.S.B. Record the value. Utilize the reduced sampling led display if necessary to obtain as good a noise floor estimate as possible.

The value measured is the noise floor of Channel A.



ACCEPTANCE TEST

TEST SIGNALS FIG. 3-3

Close Sw 1 and note any steady state change in the observed noise floor. This is the crosstalk from seven A.C. signals to the eighth signal in a common bank. This includes cross talk occurring externally to the equipment under test. Record the crosstalk value.

6.0 FILTER CUTOFF

The purpose of this test is to view the filter sharp cutoff response directly from a filter, and from an analog reconstructed output.

Set Channels A and B "Bank Select" to Bank 1.

Remove the input to "Bank Select" 1 signal D0 and replace it with a ~~*~~.D.C. biased frequency modulation input.

6.1 DIRECT FILTER

Set the frequency modulation signal to sweep from a low frequency to approximately 50 KHz.

Monitor the output of the input filter corresponding to Channel B signal D0 with the oscilloscope. Set the oscilloscope to view the sharp cut off characteristic of the filter.

See Appendix A Figures 5-1 and 5-2 for filter characteristic details.

6.2 RECONSTRUCTED SIGNAL

Monitor the reconstructed waveform at the Channel B output signal D0 with the oscilloscope. Set the oscilloscope to view the sharp cutoff characteristic of the reconstructed signal.

7.0 BANK SWITCHING TRANSIENT

The purpose of this test is to measure duration of the transient created by bank switching.

Remove the frequency modulation input to "Bank Select" 1 D0. Replace with the signal of Figure 3-2. (0.5V)

Set the Channel A "Signal Decode" to signal D0.

Set the Channel A "Bank Select" to bank 1.

Set the Channel B "Bank Select" to bank 1.

Set the "switched" switch to closed. This switches Channel B "Bank Select" from bank 0 to bank 1 and back at a 195 Hz rate.

Set the oscilloscope horizontal sweep to 200 microseconds per division (2 millisecond full scale).

Set the oscilloscope vertical scale to 1 volt per division.

Set the oscilloscope input coupling to D.C. coupled.

7.1 INPUT FILTER TRANSIENT RESPONSE

With the oscilloscope monitor the output of the input filter corresponding to Channel B signal D0.

Expand the oscilloscope vertical scale as far as practical and measure the filter setting time. Record the value.

See Appendix A Figure 6-1 and Figure 6-2.

7.2 ANALOG OUTPUT TRANSIENT RESPONSE

Repeat step 7.1 but monitor the reconstructed signal output of Channel B signal D0.

Set the "switched" switch to open.

8.0 ABSOLUTE ACCURACY

The purpose of this test is to determine a representative absolute accuracy of the system, within the constraints imposed by the system noise level.

The Channel A system output is determined by the LED display. Noise will make the low order LEDs flicker. As near as practical the lowest digital number and the highest digital number viewed will be recorded. The average of the two will be taken as the output value.

The input value will be that measured by the precision voltmeter to four digit accuracy.

The Channel B output will be measured by the precision voltmeter to 4 digit accuracy. Visual averaging of fluctuating signals will be used.

The procedure for each measurement point will be to set the input at the specified value and observe the LEDS. The input may then be varied to produce a readable value. In other words, input values that produce changes in more than 3 LSB (due to noise) will be avoided; they are too difficult to interpret by viewing the LEDs.

After obtaining the "high" and "low" digital reading for an input signal, the Channel B output (for the same signal) will be measured.

Set Channel A "Bank Select" to Bank 0.

Set Channel B "Bank Select" to Bank 0.

Set the Channel A "Decode" to D0.

Remove the input to "Bank Select" bank 0 signal D0 and replace with the input from a stable variable reference.

The initial input values are:

0.2 Volts
1.25 Volts
2.5 Volts
3.75 Volts
4.8 Volts

Take and record the data as explained above.

Remove the variable input from "Bank Select" Bank 0 signal D0 and replace with the input of Figure 3.2 (4.5 V).

9.0 UPLINK AND OVERFLOW

Set "Bank Select" A to Bank 0

Set "Bank Select" B to Bank 0

Set "Signal Decode" to 0

9.1 BANK 0

Verify that Channel A "Bank Select" display is 0 and that Channel A "Bank Selected" is 0. Record results.

Verify that Channel B "Bank Select" display is 0 and that Channel B "Bank Selected" is 0. Record results.

Verify that Channel A Bank 0 has been selected by examining LEDs. They should indicate approximately 4.5 V input signal (Figure 3-2), (111001100101). Record results.

Verify that Channel B Bank 0 has been selected by a voltmeter reading on Channel B output D0. It should read approximately 4.5 V. Record results.

Note that no overflow LEDs (one for Channel A and one for Channel B) are lit. Record results.

9.2 BANK 1

Change Channel A "Bank Select" to 1.

Change Channel B "Bank Select" to 1.

Set "Signal Decode" to 0. Verify that the Channel A and Channel B "Bank Select" and "Bank Selected" displays both indicate Bank 1. Record results.

C-2

Verify that Channel A bank 1 has been selected by examining LEDs. They should indicate approximately 0.5 volt input signal (Figure 3-2). (000110011001). Record results.

Verify that Channel B bank 1 has been selected by a voltmeter reading on Channel B output D0. It should read approximately 0.5 volts (Figure 3-2). Record results.

Note that no overflow LEDs are lit. RECORD RESULTS.

9.3 OVERFLOW

Set the "Signal Decode" to D0.

Set both Channel A and Channel B Bank Selects to Bank 3.

The signal inputs of Bank 3 are >5.

Verify that Channel A and Channel B Bank 3 overflow LEDs light. Record results.

~~Verify that Channel B Bank 0 LED is not lit.~~

10.0 MANUAL "BANK SELECT" CONTROL

The system has provision for manual bank selection on Channel B.

Set the four Channel B bank selection switches to off. (down).

Set the Auto/Manual switch to manual.

Verify that Channel B "Bank Select" and "Bank Selected" indicators both indicate bank 0. Record results.

Using the switches in digital code fashion, select banks 1,3,7, 15 one after the other. For each change in the switch position, verify that the Channel B "Bank Select" indicator and the "Bank Selected" indicator correspond to the switch input. Record results.

11.0 BIT ERROR RATE

The Channel A and Channel B serial data streams are transmitted from the fiber optic ring at 8 MHz. A 20 bit group represents one complete word. A word consists of 7 I.D. bits, 12 data bits, and one overflow bit. Confidence in the bit and word synchronization at the receiver is maintained by comparing the I.D. N with I.D. N+1.

The difference should always be one count. If an error occurs an "error" LED on the test set will light. It is reset by a pushbutton.

11.1 BER TEST

Set the auto/manual switch to the auto position.

Set channel A and Channel B "Bank Select" to D0.

Reset both error indicators (LEDs not lit).

11.1.1 ERROR CIRCUITS TEST

The purpose is to verify the error detection operation.

Set Channel A "Bank Select" to Bank 1. The Channel A Error led should light. The Channel B Error led should not light. Record results.

Set Channel B "Bank Select" to D1. The Channel B "Bank Select" Error led should light. The Channel A Error led should stay lit. Record results.

11.1.2 PROCEDURE

Reset both error indicators.

Start a stop watch.

Monitor the error leds for six minutes. Record the number of errors per channel.

If no errors occur terminate the test.

If an error occurs, reset the error circuit and continue timing FOR AN ADDITIONAL 6 MINUTES.

12.0 SPIN TESTING

For the remaining sections of this procedure tests will be performed with the optical ring system rotating at various speeds up to 1800 rpm.

Under these conditions it is not practical to introduce special test signals to measure absolute signal values, frequency and transient response, etc. However, there is no reason to expect such values to change due to spinning the equipment.

This part of the procedure is therefor mostly one of performance observation rather than specific parameter values. However, signal transmission and reception capability and BER can be verified.

13.0 TEST SET UP

The test set up is shown in Figure 3-1, Figure 3-2 and Figure 3-3.

The cover of the "beanie" is mounted in place.

The test signals circuitry of Figure 3-3 is mounted on top of the "beanie" cover.

Sw. 1 is in the closed position.

No fan is used for cooling.

Dry nitrogen at a pressure of 7b to 15 psi is supplied to the optical ring throughout this test.

Remove any extra "test signal" leads from the "beanie" that were used for tests in prior sections of this procedure.

14.0 MECHANICAL INTEGRITY

All power to the optical ring system is turned off.

The nitrogen to the optical slip ring is turned on.

A strobotac is used to view the "beanie" while rotating. The inner structure supporting the P.C. boards and the P.C. boards themselves are visible through the cooling openings in the sides of the "beanie" cover.

The strobotac is also used to monitor the spin rate.

14.1 PROCEDURE

Slowly bring the spin rate up to 1000 rpm.

With the strobotac, examine the beanie structure for any signs of resonance. Record any resonance observed.

Slowly increase the spin rate to 1800 rpm.

Continue the above examination of the "beanie" structure as the spin rate is increased.

Decrease the spin rate to 1000 rpm. This spin rate will be used during the rest of this test procedure. It minimizes the cooling of the "beanie" electronics and thus maximizes the temperature stress on electronic components.

15.0 NOISE

Set the Channels A and B to bank 1.

Set the signal select to DO.

Monitor theoutput of Channel B signal DO on the oscilloscope.

Record the noise level.

Monitor the ϕoutput of Channel A on the LEDs.

Record the noise level.

Examine the outputs of Channel B signals D1 and D2 to observe the presence of A.C. signals.

Examine the outputs of Channel A signal D1 and D2 to observe the presence of A.C. signals.

16.0 UPLINK AND OVERFLOW

Repeat the procedure of Section 9.0.

17.0 MANUAL "BANK SELECT" CONTROL

Repeat the procedure of Section 10.0.

18.0 BIT ERROR RATE

Repeat the procedure of Section 11.0.

After completing the above, turn off all power to the optical ring system but leave the optical ring spinning.

After 2 minutes have elapsed stop the optical slip ring spinning.

This completes the ATP.

APPENDIX B

ACCEPTANCE TEST PROCEDURE RESULTS

1.0 NO DATA TO RECORD

2.0 NO DATA TO RECORD

3.0 NO DATA TO RECORD

4.0 NOT DATA TO RECORD

5.0 CROSSTALK AND NOISE

Approximate peak to peak amplitude of 9.5 KHz signal:

~~0.6~~ 1.0 Volts P. to P.

Approximate peak to peak amplitude of 19 KHz signal:

0.8 Volts P. to P.

Channel B Noise: 1.0 Millivolts P. to P.

Channel B Crosstalk (Measured minus Channel B noise):

- 0 - Millivolts to P. to P.

Channel A Noise: ± 1 L.S.B.

Channel A Crosstalk (=L.S.B. Measured minus Channel A noise):

0 L.S.B.

Note; Ch B DY questionable

6.0 FILTER CUTOFF

No Data to record.

7.0 BANK SWITCHING TRANSIENT

7.1 INPUT FILTER SETTING TIME:

1000 Microseconds

7.2 ANALOG OUTPUT SETTING TIME:

1000 Microseconds

8.0 ABSOLUTE ACCURACY

All digital readings are to be recorded as 12 digital bits (ex. 111010101110).

A full scale digital reading is 4,095 LSB. This represents an input signal of 5.000 volts.

For a given input signal the highest and lowest digital output will be recorded. The difference between the two expressed in number of LSBs, is divided by two. The result is added to the lowest digital output recorded. The result is the average digital output assumed for the given input signal.

The digital equivalent of the given input signal is then calculated.

The absolute accuracy is then calculated as the digital equivalent minus the average digital output, expressed in L.S.B.s.

For a given analog input signal, the visually averaged output is recorded.

The absolute accuracy is the input signal minus the output signal. The result is divided by 1.221×10^{-3} (5 volt ÷ 4095) to express the error in L.S.B.

8.0 (CONTINUED)

DIGITAL OUTPUT .2007

Input Signal (4 Digits): ~~2.005~~ Volts

Input Signal Digital Equivalent = 0000/0100/100

Digital High: 0000/0100/110

Digital Low: 0000/0100/100

Difference: ~~0000/0100101~~ = 2 L.S.B.

Average = $\frac{\text{LSB}}{2}$ + Digital Low = 0000/0100/01

Absolute Accuracy = Average - Digital Equivalent

= .201 = 1 LSB

ANALOG OUTPUT

Input Signal (4 Digits): .2007 Volts

Output Signal (4 Digits): .2013 Volts

Difference: .6 mV Volts

Difference ÷ 1.221×10^{-3} = 0.5 LSB

B Digital Input = .2006

High 0000/0100/110

Low 0000/0100/101

Av 0000/0100/110 = .2024 V

8.0 (CONTINUED)

DIGITAL OUTPUT

Input Signal (4 Digits): 1.251 Volts

Input Signal Digital Equivalent = 0100000000000

Digital High: 0100000000100 ~~011~~ 4 ✗

Digital Low: 0100000000010

Difference: _____ = +2 L.S.B.

Average = $\frac{\text{LSB}}{2}$ + Digital Low = 0100000000011

Absolute Accuracy = Average - Digital Equivalent

= 1.2524 = 2 LSB

ANALOG OUTPUT

Input Signal (4 Digits): 1.2504 Volts

Output Signal (4 Digits): 1.2514 Volts

Difference: 1mv Volts

Difference ÷ 1.221×10^{-3} = 1 LSB

Digital Input = 1.2504

High 0100000000010

Low 0100000000000

Av 0100000000001 = 1.2512 ✓

8.0 (CONTINUED)

DIGITAL OUTPUT

Input Signal (4 Digits): 2.4997 Volts

Input Signal Digital Equivalent = 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Digital High: 1 0 0 0 0 0 0 0 0 0 1 1

Digital Low: 1 0 0 0 0 0 0 0 0 0 0 1

Difference: _____ = 2 L.S.B.

Average = $\frac{\text{LSB}}{2}$ + Digital Low = 1 0 0 0 0 0 0 0 0 0 1 0

Absolute Accuracy = Average - Digital Equivalent

= 2.5024 = 2 LSB

ANALOG OUTPUT

Input Signal (4 Digits): 2.5046 Volts

Output Signal (4 Digits): 2.5052 Volts

Difference: 1.4 mV Volts

Difference ÷ 1.221×10^{-3} = 1 LSB

B Digital -

Low 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

High 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Av 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 = 2.5 V

8.0 (CONTINUED)

DIGITAL OUTPUT

Input Signal (4 Digits): 3.744 Volts

Input Signal Digital Equivalent = 1011111110 10

Digital High: 1011111111 10

Digital Low: 1011111111 01

Difference: _____ = 1 L.S.B.

Average = $\frac{LSB}{2}$ + Digital Low = 1

Absolute Accuracy = Average - Digital Equivalent

= 3.7484 = 3.5 LSB

ANALOG OUTPUT

Input Signal (4 Digits): 3.7476 Volts

Output Signal (4 Digits): 3.7488 Volts

Difference: 1.2 mv Volts

Difference ÷ 1.221×10^{-3} = 1 LSB

B digital High 1011111111 10

Low 1011111111 10

Av 1011111111 01 = 3.7454

8.0 (CONTINUED)

DIGITAL OUTPUT

Input Signal (4 Digits): 4.8004 Volts

Input Signal Digital Equivalent = 1111 0101 1100 1111

Digital High: 1111 0111 0000 0000

Digital Low: 1111 0101 1111 1110

Difference: _____ = 2 L.S.B.

Average = $\frac{\text{LSB}}{2}$ + Digital Low = 1111 0101 1111 1111

Absolute Accuracy = Average - Digital Equivalent

= 4.8048 = 4 LSB

ANALOG OUTPUT

Input Signal (4 Digits): 4.8012 Volts

Output Signal (4 Digits): 4.8012 Volts

Difference: 0 Volts

Difference ÷ 1.221×10^{-3} = 0 LSB

B Digital

High 1111 0101 1100 0000

Low 1111 0101 1011 1111

Av 1111 0101 1100 0000 = 4.8012

9.0 UPLINK AND OVERFLOW

9.1 BANK 0

Channel A Bank Select: yes Both 0: Yes No

Channel A Bank Selected: yes }

Channel B Bank Select: yes Both 0: Yes No
Channel B Bank Selected: yes }

Channel A Digital Output ≈ 4.5 Volts: Yes No
Channel B Analog Output ≈ 4.5 Volts: Yes No

Overflow Leds:
Channel A: LIT NOT LIT
Channel B: LIT NOT LIT

9.2 BANK 1

Channel A Bank Select: yes Both 1: Yes No
Channel A Bank Selected: yes }

Channel B Bank Select: yes Both 1: Yes No
Channel B Bank Selected: yes }

Channel A Digital Output ≈ 0.5 Volts: Yes No
Channel B Analog Output ≈ 0.5 Volts: Yes No

Overflow Leds:
Channel A: LIT NOT LIT
Channel B: LIT NOT LIT

9.3 OVERFLOW

Overflow Leds:
Channel A: LIT NOT LIT
Channel B: LIT NOT LIT

10.0 MANUAL "BANK SELECT" CONTROL

	Bank Select	Bank Selected
Bank 0	0000	0000
Bank 1	0001	0001
Bank 3	0011	0011
Bank 7	0111	0111
Bank 15	1111	1111

11.0 BIT ERROR RATE

11.1.1 ERROR CIRCUIT TEST

	ERROR LEDS	
Channel A Bank Select to bank 1:	LIT	NOT LIT
Channel B Bank Select to bank 1:	LIT	NOT LIT

11.1.2 PROCEDURE

TIME START TEST: 11:46

Errors

Channel A: Prior observation indicates proper operation

Channel B:

TIME STOP TEST:

12.0 NO DATA TO RECORD

13.0 NO DATA TO RECORD

14.0 MECHANICAL INTEGRITY

Time of Start (at 1000 rpm): _____

Resonance Observed (1000 To 2000 rpm): Yes (No)

TIME	RPM	ESTIMATED AMPLITUDE

15.0 NOISE

Channel B Noise: 10 Millivolts P. to P.

Channel A Noise: 3 L.S.B.

16.0 UPLINK AND OVERFLOW

16.1 BANK 0

Channel A Bank Select: yes Both 0: Yes No
Channel A Bank Selected: yes }

Channel B Bank Select: yes Both 0: Yes No
Channel B Bank Selected: yes }

Channel A Digital Output ≈ 4.5 Volts: Yes No
Channel B Analog Output ≈ 4.5 Volts: Yes No

Overflow Leds:
Channel A: LIT NOT LIT
Channel B: LIT NOT LIT

16.2 BANK 1

Channel A Bank Select: Yes Both 1: Yes No
Channel A Bank Selected: yes }

Channel B Bank Select: yes Both 1: Yes No
Channel B Bank Selected: yes }

Channel A Digital Output ≈ 0.5 Volts: Yes No
Channel B Analog Output ≈ 0.5 Volts: Yes No

Overflow Leds:
Channel A: LIT NOT LIT
Channel B: LIT NOT LIT

16.3 OVERFLOW

Overflow Leds:
Channel A: LIT NOT LIT
Channel B: LIT NOT LIT

17.0 MANUAL "BANK SELECT" CONTROL

	Bank Select	Bank Selected
Bank 0	0000	0000
Bank 1	0001	0001
Bank 3	0010	0010
Bank 7	0100	0100
Bank 15	1000	1000

18.0 BIT ERROR RATE

18.1 ERROR CIRCUIT TEST

	ERROR LEDS	
Channel A Bank Select to bank 1:	LIT	NOT LIT
Channel B Bank Select to bank 1:	LIT	NOT LIT

18.2 PROCEDURE

TIME START TEST: _____

Errors

Channel A: 1

Channel B: 2

} 5 minutes

TIME STOP TEST

Dϕ	4.8		4.8	0
D1	4.0003			-13mv
D2	In 3.5001	out	3.5104	
D3	In 2.9947	out	3.0036	
D4	1.99923		2.0025	
D5	1.50004		1.5072	
D6	.99994		1.00385	
D7	.49949		.5037	

Offset

Dϕ = 1.2 mv

D1 = 4.0 mv

D2 = 8.6 mv

D3 = 1.8 mv

D4 = 1.95 mv

D5 = 6.5 mv

D6 = 1.8 mv

D7 = 5.0 mv

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SBIR Phase II Final Report

16. Abstract

This Phase II effort applies the results of Phase I to design and fabricate an optical "slip ring" system for a helicopter rotor blade/wind tunnel application. In this application, there are two assemblies: one on the rotating portion of the mechanical system, one on the stationary portion. The assembly on the rotating portion digitizes and encodes 128 transducer signals (20 KHz band width each) from various parts of the blade, and optically transfers data across the noncontacting coupling. Two complete identical independent channels are provided. On the stationary side, the signals are decoded and one channel is transmitted in digital form to a computer for recording and analysis. The second channel reconstructs the analog transduer signals for real time observation. In the opposite direction, eight signal channels enable control signals to be passed from the stationary to the rotating part of the system. Power to the rotor mounted electronics is supplied via power slip rings. The advantages of the optical over the traditional electro-mechanical slip ring method of data transfer across a rotating joint are long life, low-maintenance, immunity to noise crosstalk, and wider bandwidth. Sucessful completion of this effort demonstrated that this method is practical and reliable, and can be implemented under difficult conditions of available space, power, environment, and stringent performance and equipment life requirements.

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