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Heavy Ion Induced Single Event Phenomena (SEP) Data for Semiconductor Devices from Engineering Testing

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ABSTRACT

This document is the first presenting the accumulation of JPL data on single event phenomena (SEP), from 1979 to August 1986, in full report format. It is expected that every two years a supplement report will be issued for the follow-on period. This data for 135 devices expands on the abbreviated test data presented as part of Refs. (1) and (3) by including figures of single event upset (SEU) cross sections as a function of beam linear energy transfer (LET) when available. It also includes some of the data compiled in the JPL computer in RADATA* and the SPACERAD data bank.**

This volume encompasses bipolar and MOS (CMOS and MNOS) device data as two broad categories for both upsets (bit-flips) and latchup. It also includes comments on less well known phenomena, such as transient upsets and permanent damage modes.

*RADATA is a continually updated record of all recent JPL data except for CRRES data. The reader can obtain more recent data there that is not included in this report.

**The SPACERAD data bank contains JPL's completed data set for the CRRES satellite program. All of that data is given herein except for data on GaAs devices, which are deemed proprietary.

ACKNOWLEDGMENTS

The authors would like to thank the JPL test crew--Carl Malone, George Soli, Peter Wang, Harvey Schwartz, Kevin Watson, and Mike Havener--for their diligent efforts, so vital to the successful completion of the many tests summarized herein.

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INDEX OF DEVICE TYPES

The device types described in this report are all listed in Table 1 or Table 2, as either MOS or bipolar technology, respectively. Much of the data consists of only one cross section value and an estimate or measurement of the threshold LET (minimum value of LET for which the cross section, or upset rate, approaches zero).* Such limited data is also included in Tables 1 and 2. Devices with more extensive cross section data are presented in the tables and also as individual figures (cross section vs. LET) on the pages shown in the Table of Contents and in Tables 1 and 2. A description of vendor identification codes is provided in Appendix A. A sample upset rate calculation is discussed in Appendix B. A tabulation of ion energy and incident beam angle associated with the effective LET plotted in Figures 4 through 28 is given in Appendix C. A glossary of terms is given in Appendix D.

*This definition of threshold LET depends somewhat on how large a fluence was delivered to the part when the zero-upset condition is found. JPL usually tests to 10^6 ions/cm^2 or more when establishing this value.

SECTION I

INTRODUCTION

The data presented in this report describe the results of testing for single event phenomena (SEP) induced by irradiation with heavy ions having an atomic number $Z \geq 2$. This report specifically excludes the effects of protons that may induce upsets via another mechanism reported elsewhere (Ref. 1). SEP includes both single event upset (SEU) (reversible bit flips or soft errors) and latchup (a high conductivity state that can lead to catastrophic failure). Other manifestations of heavy-ion induced SEP, not observed by JPL, are mentioned briefly in Section III for completeness.

SEU data required for a complete device characterization consists of an SEU device cross section (measured upsets per unit fluence) as a function of beam linear energy transfer (LET) or dE/dx, the amount of energy deposited along the path by an ion of known energy. Less complete characterizations obtained to satisfy more limited objectives may include only the threshold LET or a single cross-section point for a single ion. A full characterization is presented as a graph; a partial characterization is included as a line in one of two tabulations for CMOS (MNOS) and bipolar devices.

All data reported here were taken at tests which were directed by JPL or in which JPL had a substantial participation through August 1986. Data taken by others on a piggyback basis at tests where JPL had test direction are regarded as proprietary and are not reported here. Special runs in support of modeling studies are reported separately (Ref. 2). Hence, this report has less breadth (scope) than that given in Ref. (3), in which data from the Aerospace Corporation is also included. It does, however, have more depth (with tables and cross section plots).*

The primary heavy ion sources used were the U.C. Berkeley 88-inch cyclotron, and the Brookhaven and Caltech Van de Graaff accelerators. Other types of sources (Californium-252 fission source, alpha sources, and the high energy [1 to 2 GeV/amu] Berkeley Bevalac synchrotron) have not been used for obtaining these data.

With very few exceptions, all data were obtained from sample sizes of one to three parts. However, data taken at a given time for two or more parts of a single device type are remarkably similar (<20% difference), in accord with analytical expectations. Data taken of the same device type in subsequent tests may occasionally show larger variations. JPL believes that this can be attributed to:

(1) Effects of total dose (in some instances).

(2) Change in fabrication parameters by the manufacturer without a change in device number.

*This report also includes the JPL data set for commercial CRRES satellite parts, completed in June 1987.

All tests performed by JPL conform with the new ASTM "Guide" (Ref. 4) which will be released shortly. This guide is the first document defining and describing good practices for SEP testing, and represents a joint effort by all major SEP testers as of 1987.

The cost of doing off-site testing includes accelerator rental and travel costs for a test crew of 6-10 persons to operate around the clock. Test complexity permits only 3-4 device types to be tested in one 24-hour period.

A full characterization, requiring several different ions, greatly adds to the test time and expense. As a result, test data is limited to specific project objectives. Hence, many devices receive a less than complete characterization (for example, a "go," "no-go" test with krypton only). These considerations are reflected in the data organization described in Section VII.

SECTION II

DOCUMENT USES AND LIMITATIONS

The purpose of this report is to provide test data for semiconductor devices (usually those having one or more bistable elements) exposed to heavy ions. These tests simulate the trace components of heavy ions in intergalactic cosmic rays, radiation belts around some planets, and solar flares. The data offer a useful radiation response comparison of different devices that might be considered in the development (circuit design) of a SEP-hard system. The data also offer a quick method for assisting an engineer to determine potential weak spots in an existing system.

The data presented here cannot, in any way, be used as a substitute for a comprehensive testing program of the key devices actually used in a given system, but is intended as a useful guideline for device selection. In general, SEP device response does not show large lot-to-lot variation, nor is there a significant difference among manufacturers, using the same technology. However, as noted earlier, the user must use extreme care in judging whether existing SEP data for a part is in fact representative of nominally identical devices proposed for a system, because small changes in design or processing can result in major SEP effects.

Anomalous or "maverick" device response is not seen with respect to soft errors. However, the variability in device response to latchup can be fairly large. Latchup susceptible parts are specifically not recommended for use in high LET space environments (polar and/or geosynchronous orbit).

It is often useful to have a coarse estimate of how the measured cross-section data corresponds to predicted upset rates for a known space heavy-ion environment. This subject is discussed briefly in Appendix B. It is important to realize that an accurate prediction requires a computer calculation that accounts for the LET dependence of the cross section, a realistic estimate of the heavy ion environment vs. LET, and the effects of ions impinging at an angle to the chip face.*

*For fairly hard parts (those having an LET threshold of ~40 MeV/[mg/cm^2]), the angle factor affecting the cross section may be as high as 1,000 and will depend strongly on the shape of the sensitive volume (e.g., its area/depth ratio). For softer parts, the angle factor has been taken to be 3.

SECTION III

GENERIC DEVICE TYPE INFORMATION

Some generalized comments or trends appropriate to each generic device type are provided in the following subsections.

A. MOS DEVICES

PMOS and NMOS devices are always very susceptible to SEP, because of their low threshold LET (< 10 MeV/[mg/cm^2]) and large per-bit cross sections (>1000 square microns per bit). DRAMs (NMOS technology) are very susceptible to SEP.

CMOS RAMs show a wide variation in SEU and latchup responses. Bulk devices generally exhibit latchup with argon (LET = 18 MeV/[mg/cm^2]) or krypton (LET = 37 MeV/[mg/cm^2]) unless special fabrication steps have been employed (e.g., guard rings [see Ref. 5]). Epi-CMOS and CMOS/SOS devices are very resistant to latchup, although the epi process must use thin layers to assure latchup immunity. CMOS microprocessors can be very susceptible or very resistant to SEP. Logic devices are usually resistant.

B. MNOS DEVICES

MNOS (metal nitride oxide semiconductor) devices have not been tested by JPL. Jim Pickel (Ref. 6) reports that EAROMs (electrically alterable read-only memories) and gate insulators, which are not subject to soft errors, can experience hard failures (permanent upsets) when operated in the high field (write or erase) mode. Pickel postulates that all MNOS structures may be susceptible to permanent rupture of the dielectric when the device is operated under high field conditions.

C. BIPOLAR DEVICES

As a general rule, bipolar devices tend to be more susceptible to SEP than CMOS devices, but have never exhibited heavy-ion induced latchup. Microprocessors range from very susceptible (LET ~3) to fairly resistant (LET ~18). A special case intensively studied by JPL was the bipolar AM2901B 4-bit slice (a component of a microprocessor for JPL's Project Galileo). When it was found necessary to harden this device, a CMOS part was designed and fabricated to replace it. Logic device susceptibility depends on the technology; standard parts are very resistant but other variations (low power Schottky, etc.) are less so (see Section III.F). All bipolar RAMs are very susceptible. Two tested digital-to-analog converters were fairly resistant (LET = 15).

D. POWER FETS

It is now well-established by experiments of Rockwell (Ref. 7), Aerospace, Boeing, NASA-Goddard, and others that the class of n-channel power hex-FETs (power transistors) operated in the "off" mode is susceptible to a high-current catastrophic burn-out when irradiated with heavy ions. The burn-out data is given in terms of the maximum percentage of rated voltage that a part can withstand for a given test ion (krypton, argon, etc.). Some worst-case data (using highly ionizing krypton) for a few part types show that they cannot be run at more than 25% of rated voltage, but other parts can be operated at higher voltages whose value depends on the space environment.

It is established that heavy ions will not affect p-channel devices nor any device operated in the "on" mode. It is also clear that burn-out susceptibility depends strongly on the manufacturer.

The subject of power-transistor burn-out is new. More experimental data is sure to be forthcoming and candidate theories to explain the effect are just now making their way into print (Ref. 8).

E. ROMS AND PROMS

Fusible link ROMs and PROMs (which have no bistable state circuit elements) exhibit transients when exposed to highly ionizing ions (argon and krypton). JPL believes that these transients may propagate as an error in adjacent circuitry. CMOS PROMs can exhibit latchup, but were generally more resistant to transient upsets than the bipolar PROMs that were tested.

F. LOGIC DEVICES

Logic devices exhibit a wide range of response to SEP and are listed separately here in order to show a ranking. The ranking is as follows, with the most resistant parts listed first:

1) CD4XXX Series CMOS (RCA)
2) Other CMOS logic (LS, HC, HCT, SC)
3) Standard Power Bipolar (54XXX)
4) Other bipolar logic (low power, FAST, Schottky)
5) Low power Schottky bipolar (54LSXXX)
6) Advanced LS bipolar (54ALSXXX)

However, the test data used to establish the above generalizations is limited, so specific device response data may be required to satisfy systems SEP evaluations.

G. COMBINATORIAL LOGIC

A. L. Friedman (Ref. 9) reports device disturbances for both combinatorial and sequential current mode logic, following tests with heavy ion sources. His data confirms that terminal latch upset is primarily due to flip-flop toggling rather than by data path combinatorial logic disturbances.

SECTION IV

RADIATION SOURCES

JPL has used two different types of heavy ion accelerator to obtain the test data presented here: the U.C. Berkeley 88-inch cyclotron and Van de Graaff accelerators. The latter include an old facility at the California Institute of Technology (CIT)* and the Tandem machine at Brookhaven National Laboratory (BNL).

A. U. C. BERKELEY 88-INCH CYCLOTRON

This machine has been used to generate the majority of data reported here. It provides the greatest flexibility of test options because it can supply a number of different heavy ions at a finite number of different energies. The maximum available ion energy is greater than that energy corresponding to the maximum LET (~2 MeV/nucleon)**, and ions can be selected to have adequate penetration (range) through the overlayers of the delidded devices.

B. VAN DE GRAAFF ACCELERATORS

Early tests were performed at CIT, using a low-energy machine. At present, all Van de Graaff data are obtained at BNL. These machines have the advantages of being able to pinpoint low LET thresholds of sensitive devices where lower energy, lower Z ions of continuously variable energies are desirable. However, a Van de Graaff has an upper energy limit which may prevent obtaining higher Z ions of adequate range.

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* A new Van de Graaff facility is now available at CIT. JPL expects to use it for some limited low LET characterizations in the future.

** The beam LET has a maximum value at an energy around 2 MeV per nucleon for most ions. The maximum (called the Bragg peak) arises because (1) higher energy particles of higher velocity deposit less energy during their shorter interaction time with the nuclei of the parent material and (2) the ions with energy less than the Bragg peak are starting to attach electrons (become neutralized), thereby reducing their interaction with the nucleus.

SECTION V

BEAM DEVELOPMENT AND DOSIMETRY

The beams used for SEP testing are several orders of magnitude less intense than those commonly used at accelerator facilities. Hence, special dosimetry procedures had to be developed, involving the count of individual ions.

A. DOSIMETRY

The flux of the beam (10^3 to 10^6 ions/cm^2/s) is measured by passing it through a scintillator. In early tests the ions were passed through a very thin (microns-thick) foil, but in later tests a part of the beam was passed unimpeded to the device through an annular scintillator. In both cases light generated by the scintillator was conducted to a photomultiplier tube (PMT) and counted. Care was taken to adjust the PMT bias to eliminate all noise pulses while counting all ion pulses. To avoid pulse pile-up in the dosimetry electronics, the flux never exceeded 3×10^6 ions/cm^2/s.

B. UNIFORMITY

Beam uniformity is established initially with a high intensity visual display on a quartz plate inside the beam tube. After the intensity is reduced, the uniformity is checked by comparing the beam counts in two concentric areas. One area is the annular scintillator, and the other is the area of a surface barrier detector (SBD) located in back of the device position and operated in the beam counting mode. In some tests additional checks on the translational uniformity were obtained by sweeping a position-sensitive detector along one diameter of the beam. A 10% variation in uniformity is deemed acceptable, but certain test objectives (e.g., "go" or "no-go") permit this criterion to be relaxed.

C. ENERGY MEASUREMENT

The ion energy spectrum measured by the pre-calibrated SBD is displayed on a multi-channel analyzer screen. Typical full width at half maximum (FWHM) of the energy peak is a few MeV, corresponding to negligible variation in the nominal LET. This spectrum measurement is important to insure that the desired ion is present.

SECTION VI

TEST SETUP AND PROCEDURES

A schematic overview of the SEP test setup is provided in Figure 1. The essential feature is a vacuum chamber aligned with a collimated, spatially uniform beam of particles from the source. Beam measurement equipment and test electronics are provided inside and outside the chamber.

The JPL vacuum chamber interior is shown in Figure 2. Inside are the beam collimators/shutters and diagnostic sensors, the PMT/scintillator assembly and a motorized rotatable and translatable board for positioning the selected device under test (DUT) at desired angles in the beam.

The test board with sockets for several DUTs is shown in Figure 3, together with the associated driver logic. Sometimes a device located outside the beam (a "gold" reference device) is used for signal comparison, sometimes one half of a test device is used to compare with its symmetrical other half*, and sometimes an established output is compared with the test output signal to detect the presence of errors.

Various tester approaches with different capabilities have been used during the course of the test program. All test capabilities have fast ($<<$1 millisec) automatic error reset capability, many have a capability of distinguishing between long-term upsets and transients (of various time durations), and all permit a continuous adjustment of the applied parts voltage. Most tests allow selection of an "all ones," "all zeroes," "checkerboard," or "inverse checkerboard" configuration.

Latchup tests are routinely used for all CMOS devices. When latchup occurs, one measures the fluence (time-integrated flux) before the onset of latchup and may repeat measurements several times after manual interrupt and device cooling. Current-limited power supplies are used to forestall device burn-out, while allowing the inception of latching current.

A test report is prepared for each facility experiment, in which the test objectives, background, tester type, test conditions and a descriptive interpretation of the data are provided. A copy of the raw data is usually available upon request.

JPL also has an in-house capability for calculating a device upset rate for a specified radiation environment, using a JPL computer code (contact Dr. Paul Robinson, Section 513).

*Testing two halves of a DUT in the same beam relies on the fact that two "simultaneous" upsets will almost never occur.

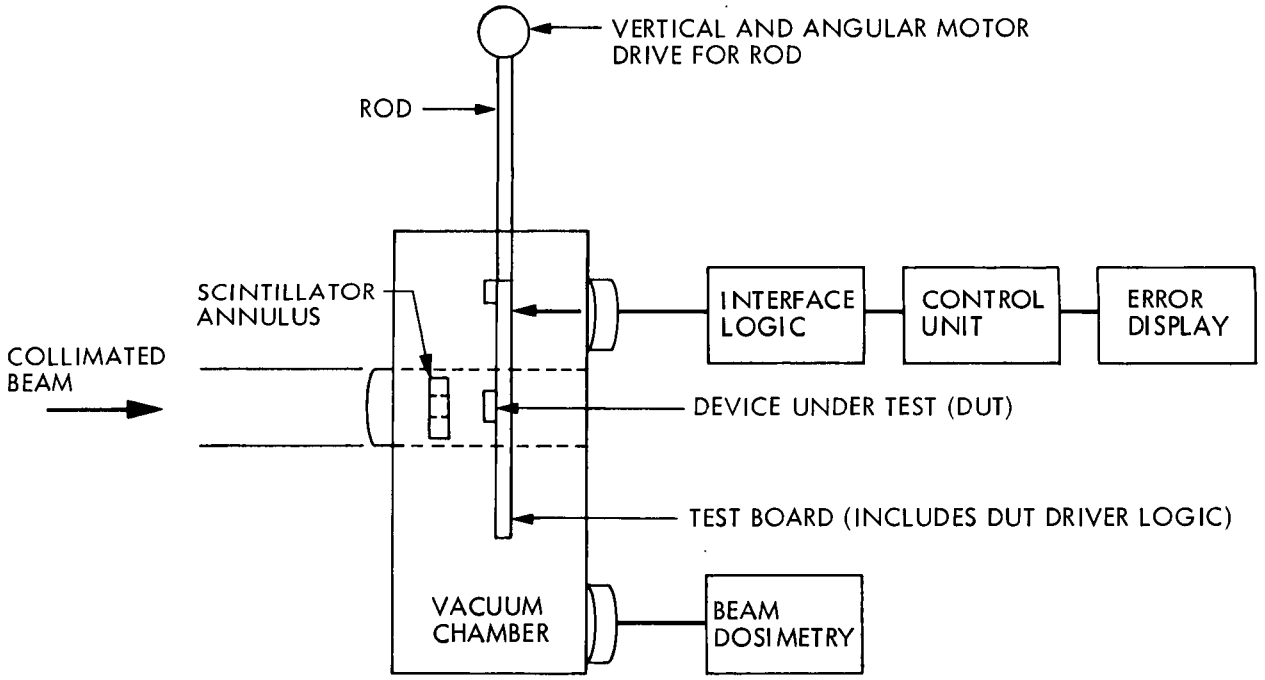

Figure 1. Schematic Overview of SEU Test

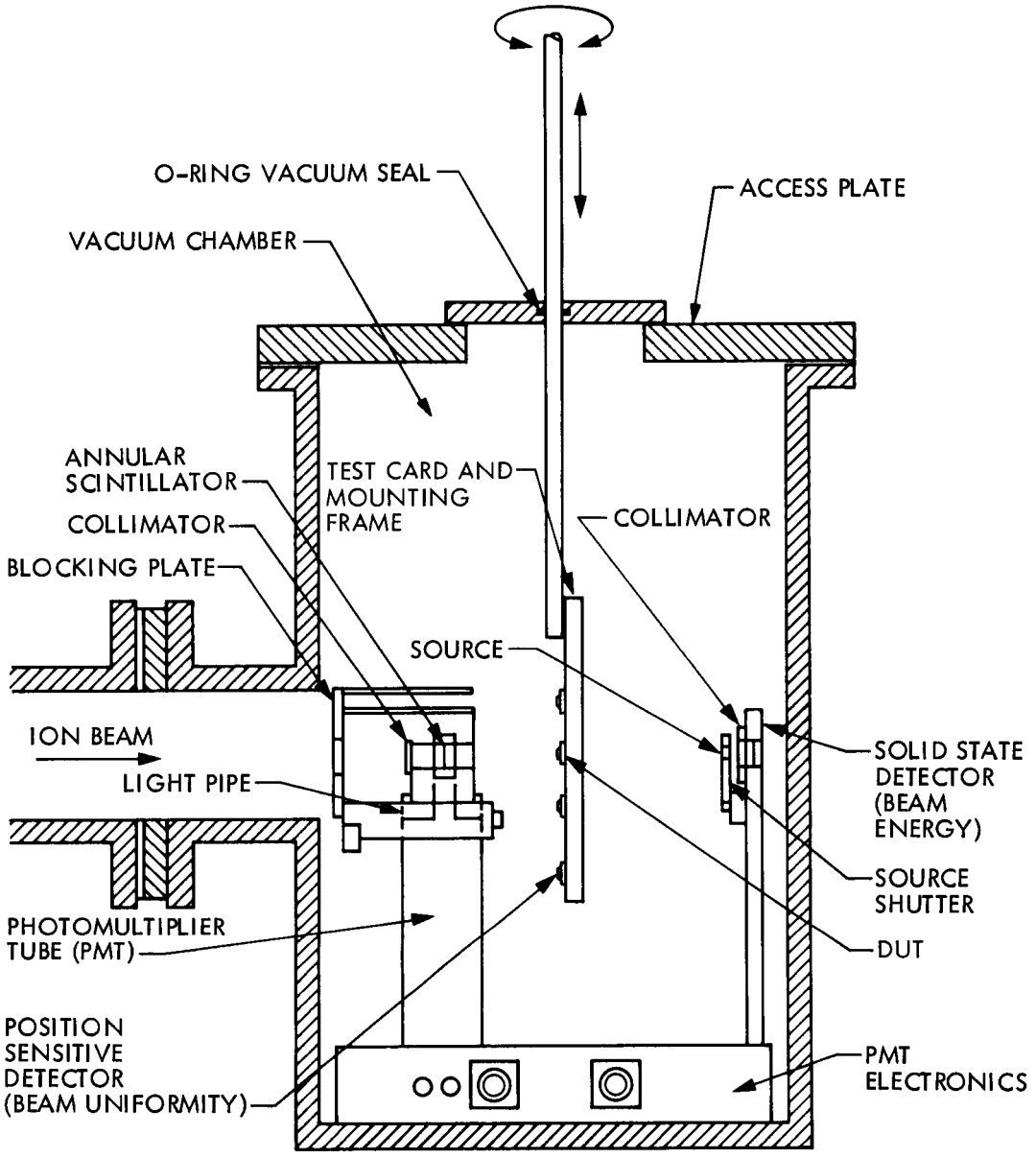

Figure 2. JPL Vacuum Chamber

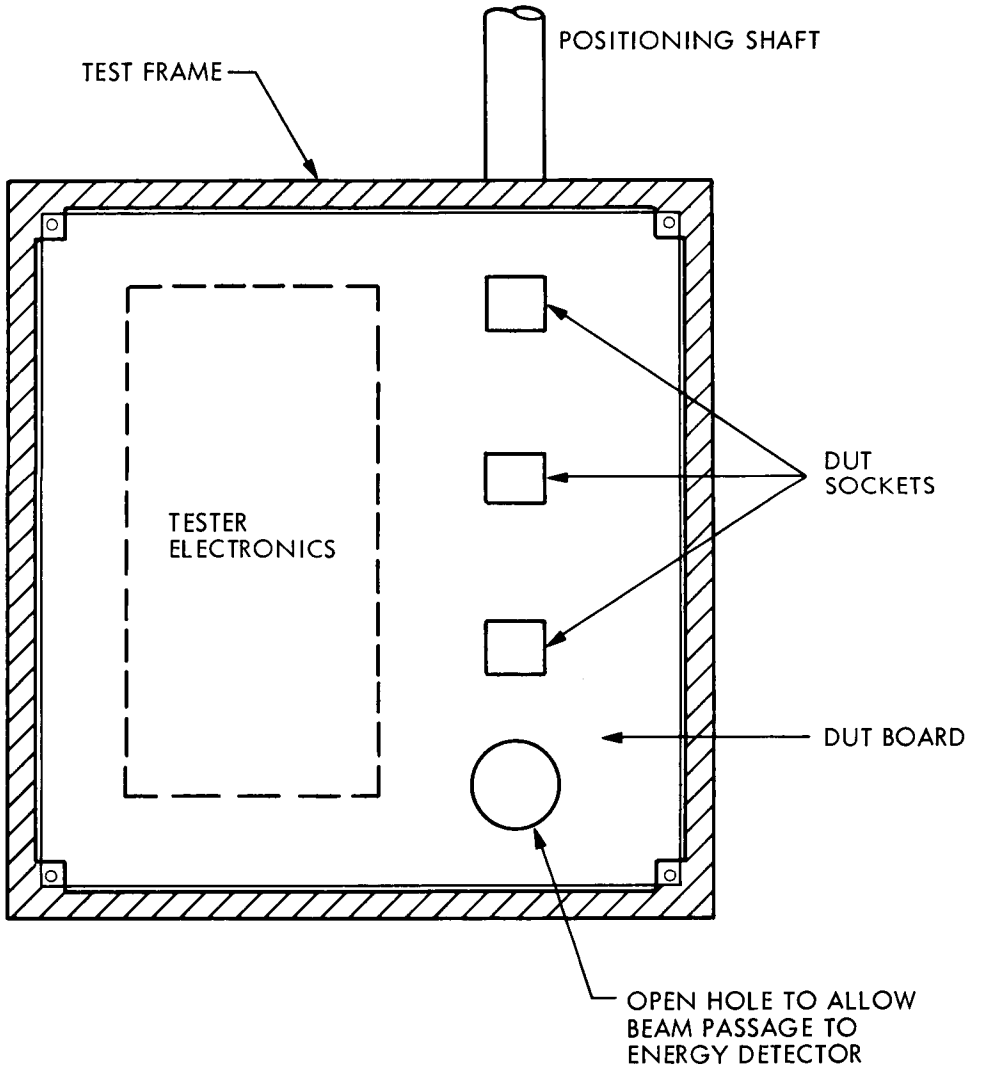

Figure 3. Typical DUT Board (Front Face) Located in Vacuum Chamber. Connector cables lead off from rear of board.

SECTION VII

DATA PRESENTATION

All of the JPL experimental data presented in this report is included in one of two tables. Table 1 includes a list of devices having MOS (CMOS, NMOS, etc.) technologies, and Table 2 lists bipolar devices. Each table includes a device description; device number, function (e.g., RAM), technology (e.g., CMOS/SOS), manufacturer, number of bits, effective soft-error threshold* LET, test facility (e.g., U. C. Berkeley) and comments on anomalous events (including non-nominal test conditions, and extrapolations). The tables list a cross section (upsets/fluence) for soft errors (defined as those errors erased upon subsequent rewrite) obtained with one maximum ionizing beam (Kr or Br) of normal incidence when known. They also list cross sections on a per bit basis (in square microns) when known. If more extensive soft-error cross-section data vs. LET is available, a reference to a figure giving a plot is noted in the column entitled "Remarks." These cross sectional plots are provided in Figures 4 through 28.

Latchup is indicated when it occurs. No latchup cross sections are reported because our present test approach does not permit enough measurements to establish a statistically valid cross section. Standing JPL policy is to recommend exclusion from JPL systems of all devices that run the risk of latchup.

LET values include effective LET measurements defined by the relation:

$$LET_{eff} = (\text{Beam Particle LET}) \times \sec\theta \qquad \theta \leq 60^\circ$$

where θ is the angle of the beam with respect to the chip's normal. The validity of this relation depends on a constant LET along the length of the particle path, and the assumption that the device sensitive volume is thin compared to the lateral dimensions. The relation also neglects the effect of funneling which introduces charge collection from regions along the ion track outside of the device depletion region, as well as several other postulated conditions.

Several instances have been noted where soft error measurements do not confirm this relation (e.g., by comparing argon [having an LET of 18] at a 60° beam angle with krypton [having an LET of 36] at $0°$). For the case of latchup, the concept of an effective LET is often less useful.

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*JPL defines the threshold LET as that value of the LET where soft errors (upsets) first appear for fluences exceeding 10^6 ions/cm^2. Other experimentalists define it differently; e.g., as that value of LET where the cross section is 10% of the maximum measured cross section. These differences in definition can lead to widely different reported threshold LET values.

The statistics for SEP testing are very meager because of:

(1) The high cost of testing individual parts.

(2) The similarity of test data for devices from a given lot.**

However, devices of a different vintage may have a very different SEP response. Also, latchup data is more likely to exhibit a wide variation in behavior than data on soft errors.

The figures presenting data indicate a statistical spread in response as follows:

(1) Two devices (error bars show minimum and maximum values).

(2) Three or more devices (error bars are one standard deviation).

The precision in repeated measurements of the same part (e.g., same serial number) always agree within a few percent.

**A "lot" is defined here as a group of contemporary parts from a manufacturer's single shipment. No wafer-to-wafer type testing, common to ionizing total dose studies, has been performed by JPL for SEP studies.

Table 1. SEU Data for MOS and MNOS Devices

	Device	Function	Technology	Mfr.	Bits	Effective LET* Threshold	Device Cross Section (cm^2)**	Cross Section Per Bit (10^{-8} cm^2)	Facility***	Remarks
1)	8085	Microprocessor	NMOS	INTEL	>125	<2.8	4×10^{-3}	--	88 in.	Extrapolated cross section. Plotted in Fig. 4.
2)	8085	"	"	AMD	>125	<6	3×10^{-3}	$\geq$1200	88 in.	Plotted in Fig. 5
3)	NS 32016	16-Bit uP	"	NSC	>436	<3	2×10^{-2}	--	88 in.	Plotted in Fig. 6. Extrapolated.
4)	NS 32081	Float Pt. Unit	"	"	>288	<3	6×10^{-3}	--	88 in.	Plotted in Fig. 7 (8 32-bit reg. only)
5)	NS 32201	Timing Control	Schottky Bipolar†	"	>10	6	$\geq 3 \times 10^{-4}$	--	88 in.	Plotted in Fig. 8 (DIV2 & Reset F/F only)
6)	1802 RH	Microprocessor	CMOS	RCA	343	>120	No Upset	--	88 in.	Only 256-bit memory is tested.
7)	1802	"	"	Sandia	343	>120	No Upset	--	88 in.	"
8)	SA 3000	"	"	"	>125	>120, 50	No Upset	--	88 in., Orsay	Thresholds at 10 V and 5V, respectively
9)	80C85	"	"	Harris	>125	>75	No Upset	--	BNL	Equivalent to SA 3000
10)	GP 001 (old & new)	"	CMOS/SOS	RCA	113/226	>75	No Upset	--	88 in.	
11)	80C86	"	CMOS-epi	Harris	635	<5	$>2.4 \times 10^{-2}$	>4000	88 in.	Plotted in Fig. 9
12)	80C86	"	CMOS-bulk	"	"	<5	--	--	88 in.	Latchup threshold located between LET of 11 to 18 MeV/mg/cm^2
13)	2901	4-Bit Slice	CMOS with 80 KΩ Resistor	Sandia	68	>100	No Upset	--	88 in.	Only 64-bit register is included here.
14)	2901	"	CMOS (0 KΩ)	"	68	~100	No Upset	--	88 in.	"

*LET is Linear Energy Transfer in MeV/mg/cm^2.
**Unless otherwise noted, the cross section (upsets/fluence) is given for 120-300 MeV krypton ions at normal incidence, with an LET = 37 MeV/mg/cm^2.
***CIT is Caltech Van de Graaff; ORNL is Oak Ridge 25 MeV Tandem Van de Graaff; Cf is IRT Calif-252 Facility; Orsay is cyclotron at Institut de Physique Nucleaire, Orsay, France; other facilities are U.C. Berkeley cyclotrons.
†Bipolar device is included here because it is an NS32016 peripheral.

Table 1. SEU Data for MOS and MNOS Devices (continued)

	Device	Function	Technology	Mfr.	Bits	Effective LET* Threshold	Device Cross Section (cm^2)**	Cross Section Per Bit (10^{-8} cm^2)	Facility***	Remarks
15)	2909 (SA 3327)	4-Bit µP Sequencer	CMOS (80 KΩ)	Sandia	26	>100	No Upset	--	88 in.	
16)	2909 (SA 3227)	"	CMOS (0 KΩ)	"	26	50	No Upset	--	88 in.	
17)	ADSP 1016A	Multiplier	CMOS	ADI	--	<37	4×10^{-4}	--	88 in.	Latchup
18)	54LS73 (SA 3318)	J/K Flip-Flop	CMOS	Sandia	4	>75	No Upset	--	88 in.	
19)	54HC73	"	"	NSC	4	>75	No Upset	--	88 in.	
20)	54HC373	Latch	"	"	8	>75	No Upset	--	88 in.	
21)	54HC373	"	"	SPI	8	>75	No Upset	--	88 in.	
22)	54HC373	"	"	RCA	8	>75	No Upset	--	88 in.	
23)	54HCT373	"	"	"	8	>75	No Upset	--	BNL	
24)	54HCT373	"	"	Supertex	8	>75	No Upset	--	88 in., Orsay	
25)	54SC373	"	"	Mitel	8	35	10^{-6}	~10 (See remarks)	88 in.	Near threshold
26)	54LS373	"	"	Sandia	8	>75	No Upset	--	88 in.	
27)	54LS374	D Flip-Flop	"	"	8	~55	No Upset	--	88 in.	
28)	54LS74	"	"	"	6	>75	No Upset	--	88 in.	
29)	9407 (SA 3268)	4-Bit Data Register	CMOS (80 KΩ)	"	32	>55	No Upset	--	88 in.	
30)	9407 (SA 3268)	"	CMOS (0 KΩ)	"	32	No Data	No Data	--	88 in.	Included to give parts overview for JPL program
31)	54169 (SA 3269)	4-Bit Counter	CMOS (80 KΩ)	"	8	>55	No Upset	--	88 in.	
32)	54169 (SA 3269)	"	CMOS (0 KΩ)	"	8	No Data	No Data	--	88 in.	Included to give parts overview for JPL program
33)	54395 (SA 3270)	4-Bit Shift Register	CMOS (80 KΩ)	"	8	>55	No Upset	--	88 in.	

Table 1. SEU Data for MOS and MNOS Devices (continued)

	Device	Function	Technology	Mfr.	Bits	Effective LET* Threshold	Device Cross Section (cm^2)**	Cross Section Per Bit (10^{-8} cm^2)	Facility***	Remarks
34)	54395 (SA 3270)	4-Bit Shift Register	CMOS (0 KΩ)	Sandia	8	No Data	No Data	--	88 in.	Included to give parts overview for JPL program
35)	CD 40160	4-Bit Counter	CMOS	Fairchild	8	>75	No Upset	--	88 in.	
36)	CD 40161	"	"	RCA	8	>75	No Upset	--	88 in.	
37)	CD 4013b	D Flip-Flop	"	"	4	>75	No Upset	--	88 in.	
38)	CD 4027b	J/K Flip-Flop	"	"	4	>75	No Upset	--	88 in.	
39)	CD 4031	"	"	"	128	>75	No Upset	--	88 in.	
40)	CD 4061	RAM	CMOS	RCA	256 x 1	~80	No Upset	--	88 in.	
41)	CDP 1822	"	CMOS/SOS	"	256 x 4	>216	No Upset	--	88 in.	
42)	CDP 1821	"	"	"	1K x 1	145	No Upset	--	88 in.	
43)	TCS 130S (Commercial)	"	"	"	16K	~48	No Upset	--	88 in.	
44)	NBRC 4042	"	"	Hughes	16K	20	2×10^{-3}	12.5	88 in.	
45)	SA 3001	"	CMOS/epi	Sandia	256 x 8	>75	No Upset	--	88 in.	
46)	MM54C929	"	CMOS	NSC	1K x 1	15	10^{-2}	1000	88 in.	Latchup
47)	MM54C200D	"	"	"	256 x 1	>120	No Upset	--	88 in.	
48)	4736B	"	LOC/MOS Si Gate-epi	Phillips	1K	~100	No Upset	--	88 in.	
49)	IM 6518	"	CMOS	INTEL	1K x 1	<37	3×10^{-3}	300	88 in.	
50)	MB 8404K	"	CMOS (fast) epi-Si Gate	Fujitsu	4K	~100	No Upset	--	88 in.	
51)	TCC 244	"	CMOS C^2L-Si Gate	Sandia	256 x 4	>75	No Upset	--	88 in.	
52)	TCC 244 (rad hard)	"	CMOS	RCA	1K	>100	No Upset	--	88 in.	
53)	HM 6504	"	"	Harris	4K x 1	10	5×10^{-3}	125	88 in.	Latchup
54)	HS 6504 RH	"	CMOS-epi rad-hard Si gate	"	4K x 1	36	1.2×10^{-3}	50 (See remarks)	88 in.	Near threshold

Table 1. SEU Data for MOS and MNOS Devices (continued)

	Device	Function	Technology	Mfr.	Bits	Effective LET* Threshold	Device Cross Section (cm^2)**	Cross Section Per Bit (10^{-8} cm^2)	Facility***	Remarks
55)	HM 6508	RAM	CMOS	Harris	1K x 1	15	10^{-2}	1000	88 in.	Latchup
56)	HM 6508 RH	"	CMOS-epi	"	1K x 1	>37	4×10^{-3}	400	88 in.	
57)	HM 6516	"	CMOS/bulk	"	2K x 8	<17	$<5 \times 10^{-4}$	<1	88 in.	Latchup Ar, Kr
58)	HM 6516	"	CMOS/epi	"	2K x 8	<29	5×10^{-2}	300	88 in. BNL	Latchup LET = 55
59)	HM 6551 (Commercial)	"	"	"	256 x 4		--	--	88 in.	Latchup (75° only)
60)	HM 6551 RH	"	"	"	256 x 4	~75	No Upset	--	88 in.	
61)	HM 65262 RH	"	"	"	16K x 1	20	10^{-2}	60	88 in.	Plotted in Fig. 10
62)	HMI-6562B-8	"	CMOS	"	1K	~100	No Upset	--	88 in.	
63)	8155	"	NMOS	AMD	256 x 8	<37	4×10^{-2}	2000	88 in.	Plotted in Fig. 11
64)	8155	"	"	INTEL	256 x 8	<37	6×10^{-2}	3000	88 in.	Plotted in Fig. 12
65)	AM 92L44	"	"	AMD	4K x 1	1.6	0.41	10,000	Orsay, UCB	Plotted in Fig. 13
66)	AM 21L47	"	"	"	4K x 1	<1.6	0.41	10,000	Orsay, UCB	Plotted in Fig. 13
67)	MB 81256	DRAM	NMOS	Fujitsu	256K x 1	~3.5	0.1	40	BNL	Plotted in Fig. 14
68)	2764A	PROM	"	INTEL	8K x 8	<17	1.5×10^{-3}	--	BNL	
69)	2864	EAPROM	"	"	8K x 8	<37	10^{-4}	--	88 in.	
70)	27C64	PROM	CMOS	"	8K x 8	--	--	--	BNL	Latchup threshold = 14
71)	HM 6611	PROM	"	Harris	512 x 8	~45	No Upset	--	88 in.	Latchup
72)	HM 6641	PROM	"	"	512 x 8	~40	No Upset	--	88 in.	Latchup
73)	HM 6616	PROM	"	"	2K x 8	<37	10^{-2} (transients)	--	88 in.	No latchup at 45° (KR)
74)	AM 2813	FIFO Reg.	PMOS	AMD	288	10	6×10^{-3}	2000	88 in.	
75)	CDI6007	Gate Array	CMOS	Lockheed	--	>75	No Upset	--	Orsay	
76)	MN5253	A/D (12-bit)	CMOS	MNC	--	<<5	--	--	88 in.	Parts bigger than beam

Table 2. SEU Data for Bipolar Devices

	Device	Function	Technology	Mfr.	Bits	Effective LET* Threshold	Device Cross Section (cm^2)**	Cross Section Per Bit (10^{-8} cm^2)	Facility***	Remarks
1)	SBP 9989	Microprocessor	I^2L	TIX	336	~3	$\sim 10^{-4}$	~30	88 in.	
2)	SBP 9900A	"	"	"	346	18<LET<37	10^{-5}	3	"	
3)	2901A	4-Bit Slice	LS/TTL	AMD	68	~7	5×10^{-3}	8000	88 in. CIT	Only 64-bit RAM data is reported here.
4)	2901-A1	"	--	NSC	"	<3.3	1.2×10^{-3} 27 MeV Carbon	2000	CIT	Only 64-bit RAM data is reported here.
5)	2901-A2	"	--	NSC	"	<3.3	9×10^{-4} 27 MeV Carbon	1500	CIT	Only 64-bit RAM data is reported here.
6)	2901-AX	"	--	NSC	"	<3.3	9×10^{-4} 27 MeV Carbon	1500	CIT	Only 64-bit RAM data is reported here.
7)	2901B	"	LS/TTL	AMD	"	~4	3×10^{-3}	5,000	88 in. CIT	Plotted in Fig. 15. Only 64-bit RAM data is reported here.
8)	2901C	"	ECL/TTL	"	"	<<3.3	3×10^{-3}	5,000	88 in. CIT	Plotted in Fig. 16. Only 64-bit RAM data is reported here.
9)	29F01	"	FAST	Fairchild	"	<6	2.7×10^{-4} 26 MeV Oxygen	400	CIT	Only 64-bit RAM data is reported here.
10)	2909A	4-Bit µP Sequencer	TTL	AMD	26	<2.9	$>3 \times 10^{-4}$	1500	88 in.	Stack plus pointer. (18 bits.) Plotted in Fig. 17.
11)	2909	4-Bit µP Sequencer	"	"	26	3.0	2.3×10^{-4}	500	88 in.	Stack plus pointer. (18 bits.) Plotted in Fig. 18.
12)	9407	4-Bit Data Register	"	Fairchild	32	<2.9	7×10^{-4}	2200	"	4-registers. Plotted in Fig. 19.
13)	9407	"	I^2L	"	32	15	1.4×10^{-4}	400	"	4-registers
14)	54161	4-Bit Counter	I^2L	Raytheon	4	>75	No Upset	--	"	
15)	74162	"	"	Fairchild	4	>75	"	--	"	

*LET is Linear Energy Transfer in MeV/mg/cm^2
**Unless otherwise noted, the cross section (upsets/fluence) is given for 120-300 MeV krypton ions or for Calif-252 fission products at normal incidence, with an LET ≈ 37 MeV/mg/cm^2.
***CIT is Caltech Van de Graaff; ORNL is Oak Ridge 25 MeV Tandem Van de Graaff; Cf is IRT Calif-252 Facility; other facilities are U.C. Berkeley cyclotrons.

Table 2. SEU Data for Bipolar Devices (continued)

	Device	Function	Technology	Mfr.	Bits	Effective LET* Threshold	Device Cross Section (cm^2)**	Cross Section Per Bit (10^{-8} cm^2)	Facility***	Remarks
16)	54109	J/K Flip-Flop	I^2L	Signetics	4	>75	No Upset	--	88 in.	
17)	5473	J/K Flip-Flop	TTL	Signetics	4	>75	"	--	"	
18)	5495	Shift Register	"	"	4	>75	"	--	"	
19)	5497(7495)	"	"	TIX	4	~75	"	--	"	
20)	76L70	"	L TTL	NSC	8	<37	3×10^{-3}	40,000	"	
21)	54L95	"	"	"	4	<37	2×10^{-4}	5,000	"	
22)	54L95	"	"	TIX	4	<37	2×10^{-4}	5,000	"	
23)	54L73	J/K Flip Flop	"	"	4	~30	10^{-5}	250	"	
24)	54L73	"	"	RCA	4	50	No Upset	--	"	
25)	54L73	"	"	NSC	4	>37	2×10^{-4}	5,000	"	
26)	54L78	" "	"	"	4	>37	No Upset	--	Bevalac	No beam angle test
27)	54L75	4-Bit Counter	"	"	4	<37	10^{-5}	250	88 in.	
28)	54L93	"	"	TIX	4	30	--	--	BNL	1982 date code
29)	54L93	"	"	"	4	12	4.5×10^{-4}	10,000	BNL	1974 date code
30)	54S169	4-Bit Counter	Schottky	AMD	4	>28	--	--	88 in.	
31)	93S10	"	"	Fairchild	4	<37	5×10^{-6}	125	88 in.	
32)	54S374	D Flip-Flop	"	TIX	8	15	--	--	88 in.	
33)	54LS00	NAND Gate	LS TTL	Signetics	4	<37	Transients (Kr)	--	88 in.	>200 mV; PW 20-25 nsec
34)	54LS109	J/K Flip-Flop	"	Fairchild	4	10 ± 3	9×10^{-5}	2250	88 in.	Plotted in Fig. 20
35)	54LS73	"	"	Signetics	4	~4	8×10^{-5}	2000	88 in.	Plotted in Fig. 21
36)	25LS169	4-Bit Counter	"	AMD	4	<37	Yes (Krypton)	--	88 in.	
37)	74LS162	"	"	TIX	4	<37	2×10^{-4}	5000	88 in.	
38)	54LS163	"	"	NSC	4	13	2×10^{-4}	4000	88 in.	Plotted in Fig. 22
39)	54LS74A	D Flip-Flop	"	AMD	4	13	3×10^{-6} 38 MeV Oxygen	75	88 in.	At threshold

Table 2. SEU Data for Bipolar Devices (continued)

	Device	Function	Technology	Mfr.	Bits	Effective LET* Threshold	Device Cross Section (cm^2)**	Cross Section Per Bit (10^{-8} cm^2)	Facility***	Remarks
40)	25LS374	D Flip-Flop	LS TTL	AMD	8	8 ± 3	5×10^{-5}	600	88 in.	
41)	54LS395	Shift Register	"	Signetics	4	8	--	--	88 in.	
42)	54LS398	"	"	"	6	<37	3×10^{-4}	5000	88 in.	
43)	54LS95	"	"	"	4	11 ± 2	6×10^{-4}	5000	88 in.	Plotted in Fig. 23
44)	74LS95	"	"	TIX	4	<37	10^{-4}	2500	88 in.	
45)	54LS194A	"	"	"	4	5	8×10^{-5}	2000	88 in.	
46)	54ALS373	Latch	ALSTTL	TIX	8	8	4.5×10^{-4}	5000	BNL	Plotted in Fig. 24
47)	54F373	Fairchild	FTTL	Fairchild	8	25	2×10^{-5}	--	BNL	Plotted in Fig. 25
48)	31L01	RAM	LTTL	AMD	16 x 4	6	1×10^{-3}	1500	88 in.	
49)	93L422	"	"	"	256 x 4	<1	4×10^{-2}	4000	88 in.	Plotted in Fig. 26
50)	93L422	"	"	Fairchild	1K	~1.8	2×10^{-2}	2000	88 in.	
51)	93L425	"	"	"	1K x 1	<37	1.5×10^{-2}	1500	88 in.	
52)	82S212	"	STTL	Signetics	256 x 9	1	2×10^{-2} 29 MeV Oxy	1000	BNL	Plotted in Fig. 27
53)	82S19	"	"	"	64 x 9	<5	$\geq 10^{-2}$ 29 MeV Oxy	$\geq$2000	CIT	
54)	93419	"	TTL	Fairchild	1K	<5	$\geq 7 \times 10^{-3}$ 47 MeV Oxy	$\geq$700	88 in.	
55)	93422	"	"	AMD	256 x 4	<1	4×10^{-2}	4000	88 in.	Plotted in Fig. 26
56)	93451	PROM	Schottky TTL Tri-State	Fairchild	1K x 8	<37	~2×10^{-6}	--	88 in., BNL	
57)	AM 6012	DAC	Bipolar	AMD	--	15	10^{-6}	--	88 in.	Plotted in Fig. 28
58)	AD 562	"	"	ADI	--	15	10^{-6}	--	88 in.	Plotted in Fig. 28
59)	AD 573	A/D (10-bit)	"	"	--	5	--	--	88 in.	Parts bigger than beam

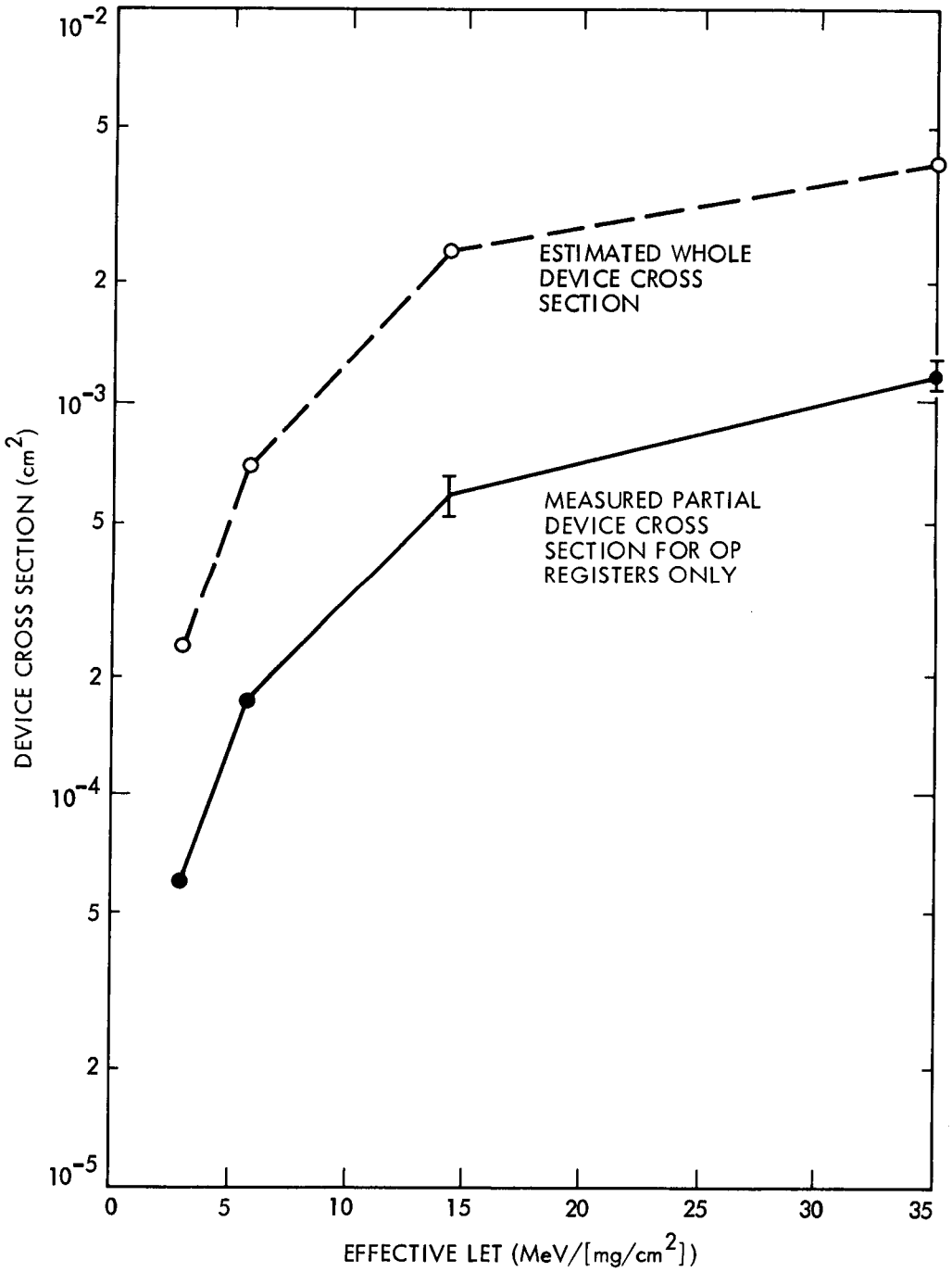

Figure 4. 8085 INTEL NMOS 8-Bit Microprocessor

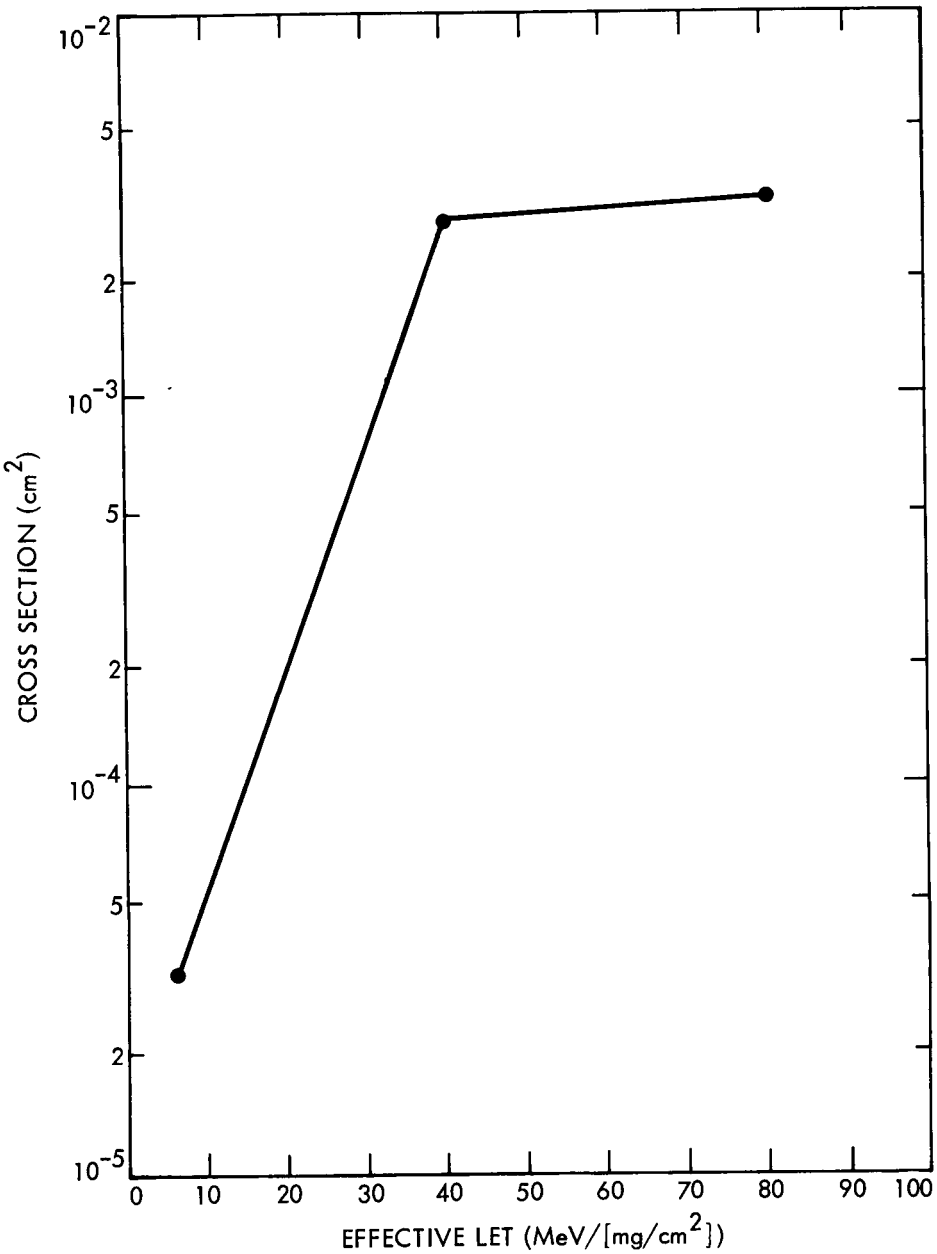

Figure 5. 8085 AMD NMOS 8-Bit Microprocessor

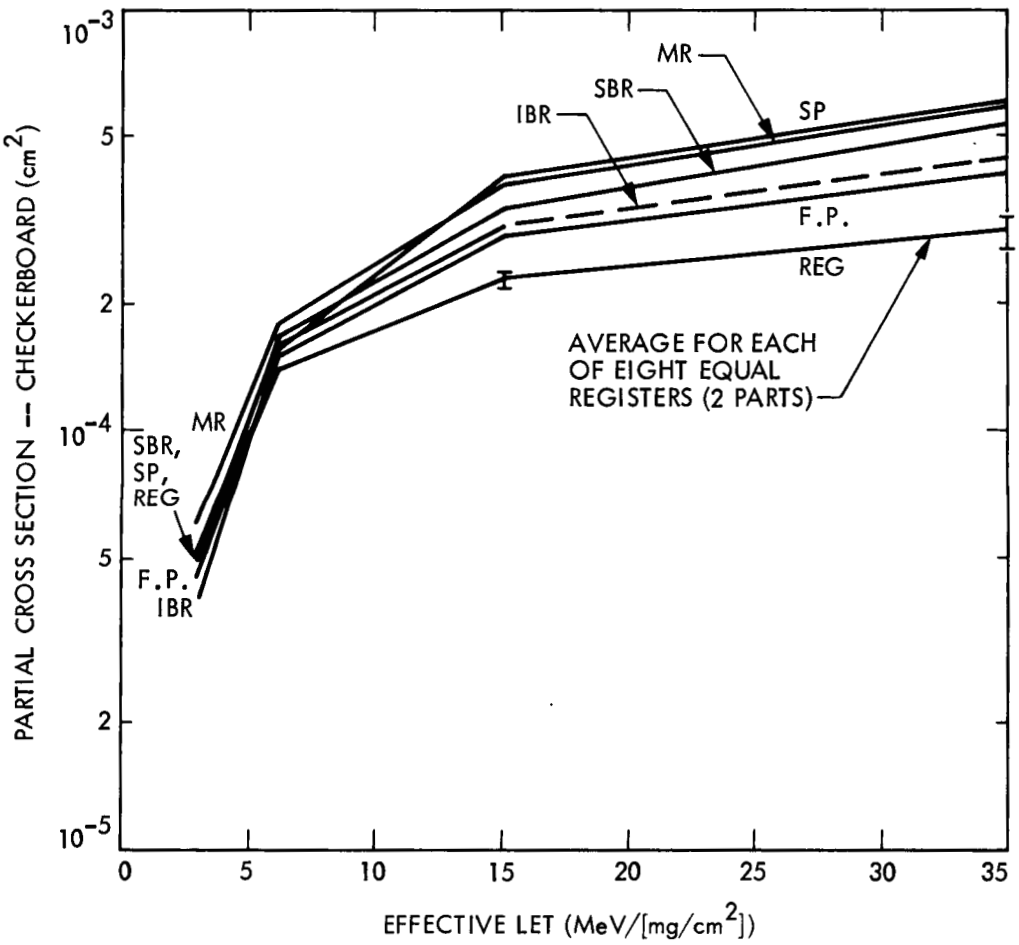

Figure 6. Partial Cross Section Data for Each Test Element of the 32016 NSC NMOS 16-Bit Microprocessor. The letters identify the elements as follows: FP = Frame Pointer, SP = Stack Pointer, SBR = Static Base Register, IBR = Interrupt Base Register, and MR = Module Register. The total cross section is given in Table 1.

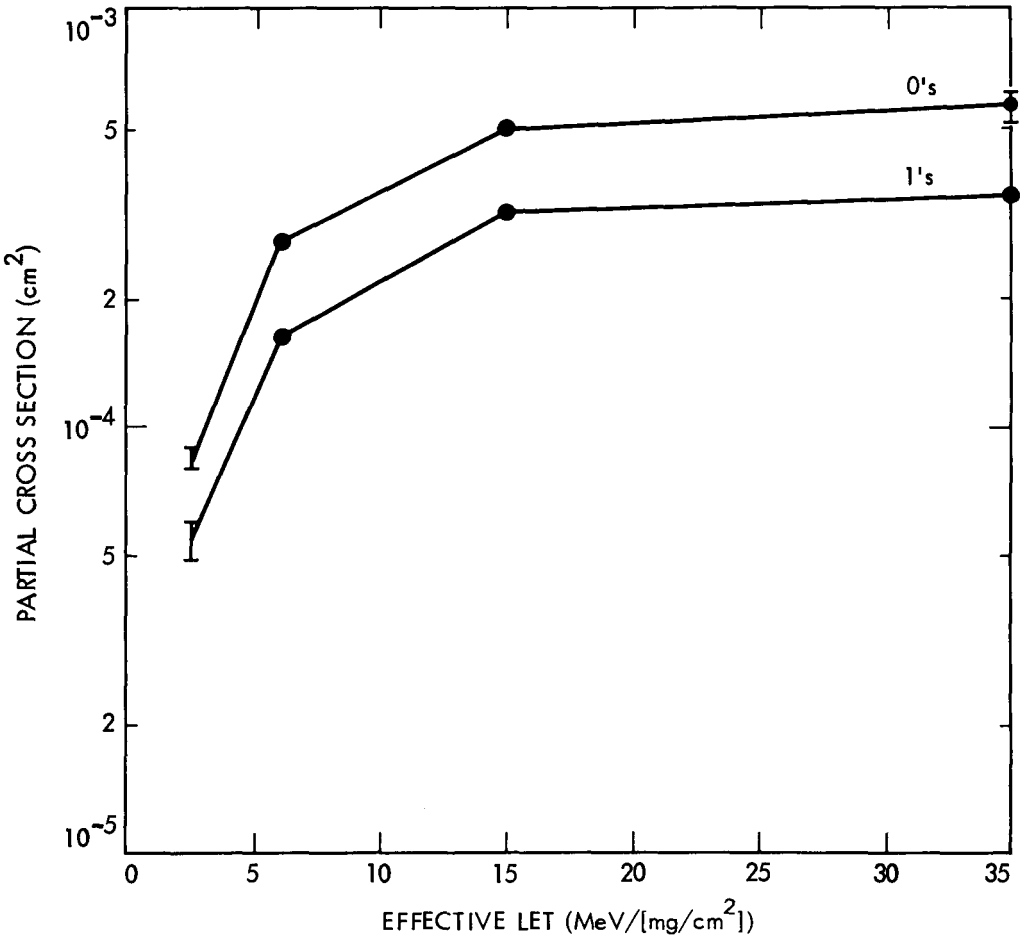

Figure 7. Partial Cross Section Data for a Single 32-Bit Register of the 32081 National NMOS Floating Point Unit. The total cross section is estimated to be 12 times the individual register cross section. The error bars show the spread of the average value calculated for each part. Input patterns are denoted by "0's" and "1's."

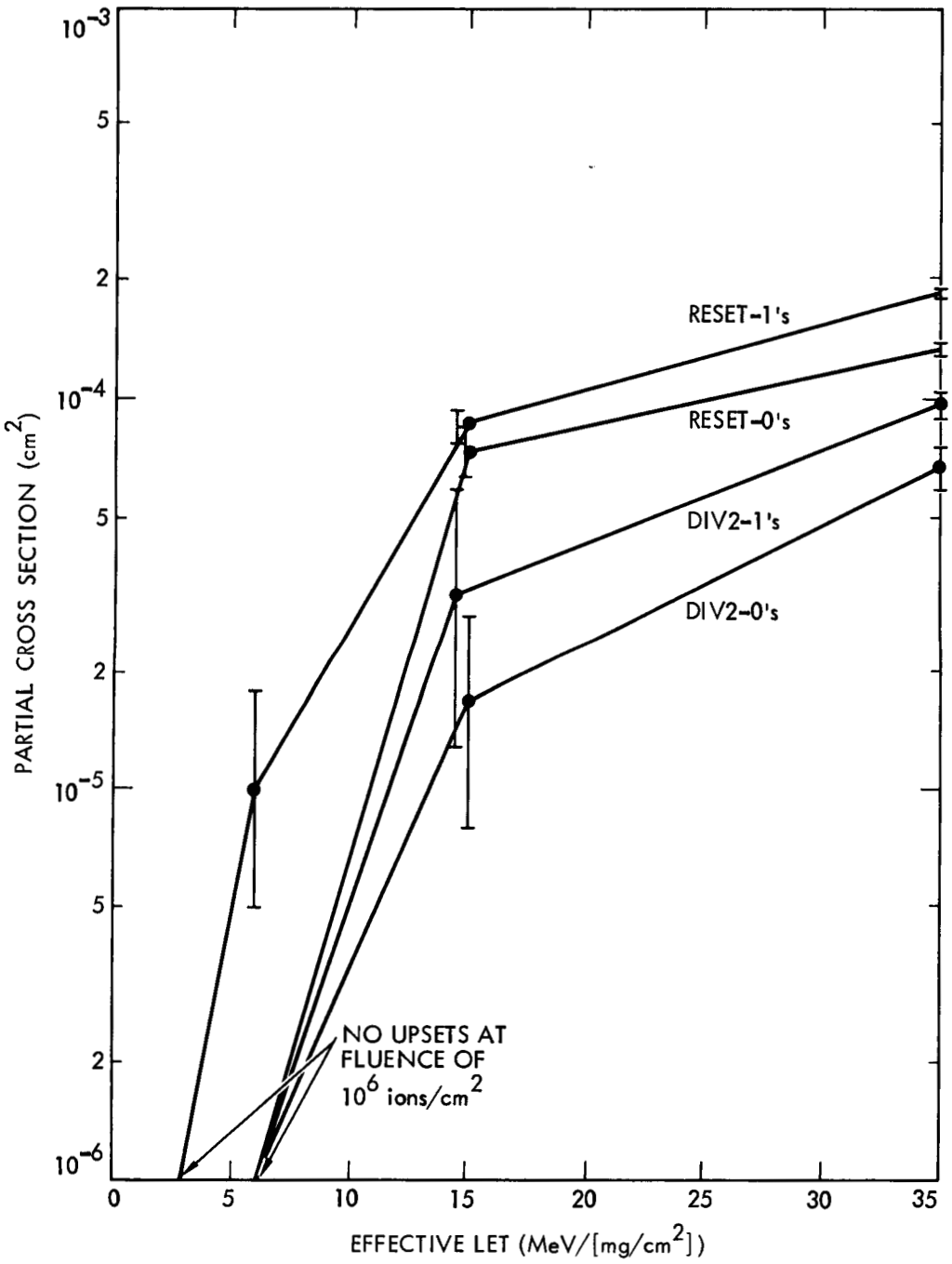

Figure 8. Partial Cross Section Data for 32201 NSC Bipolar Timing Control Unit (Peripheral to NSC 32016 Microprocessor). The tester measures a single "divide-by-two" flip-flop and a "reset" flip-flop in either a "1" or "0" configuration, as shown. The total cross section is taken to be equal to or greater than the sum of each flip-flop in the worst-case 1's configuration.

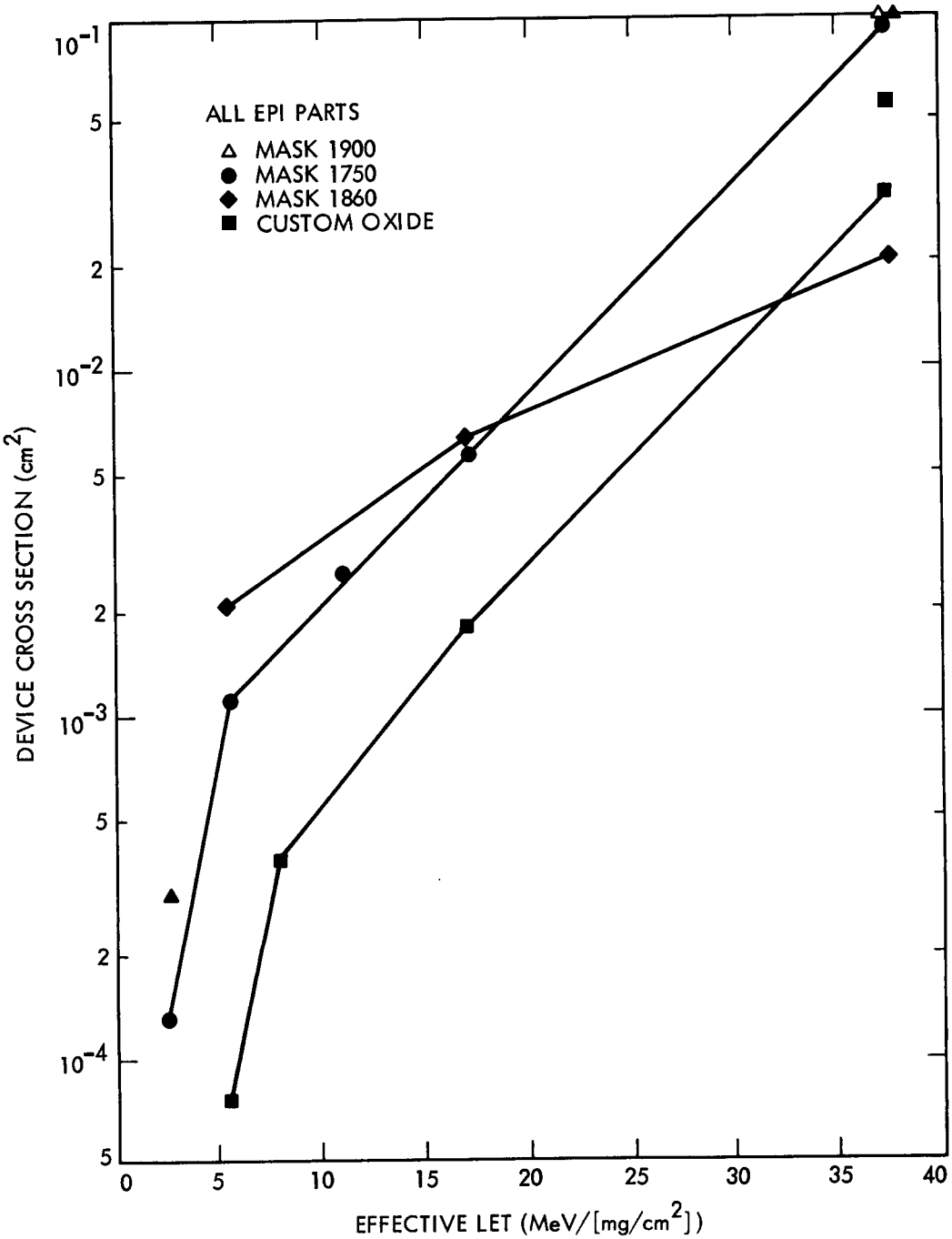

Figure 9. 80C86 Harris CMOS/epi 16-Bit Microprocessor

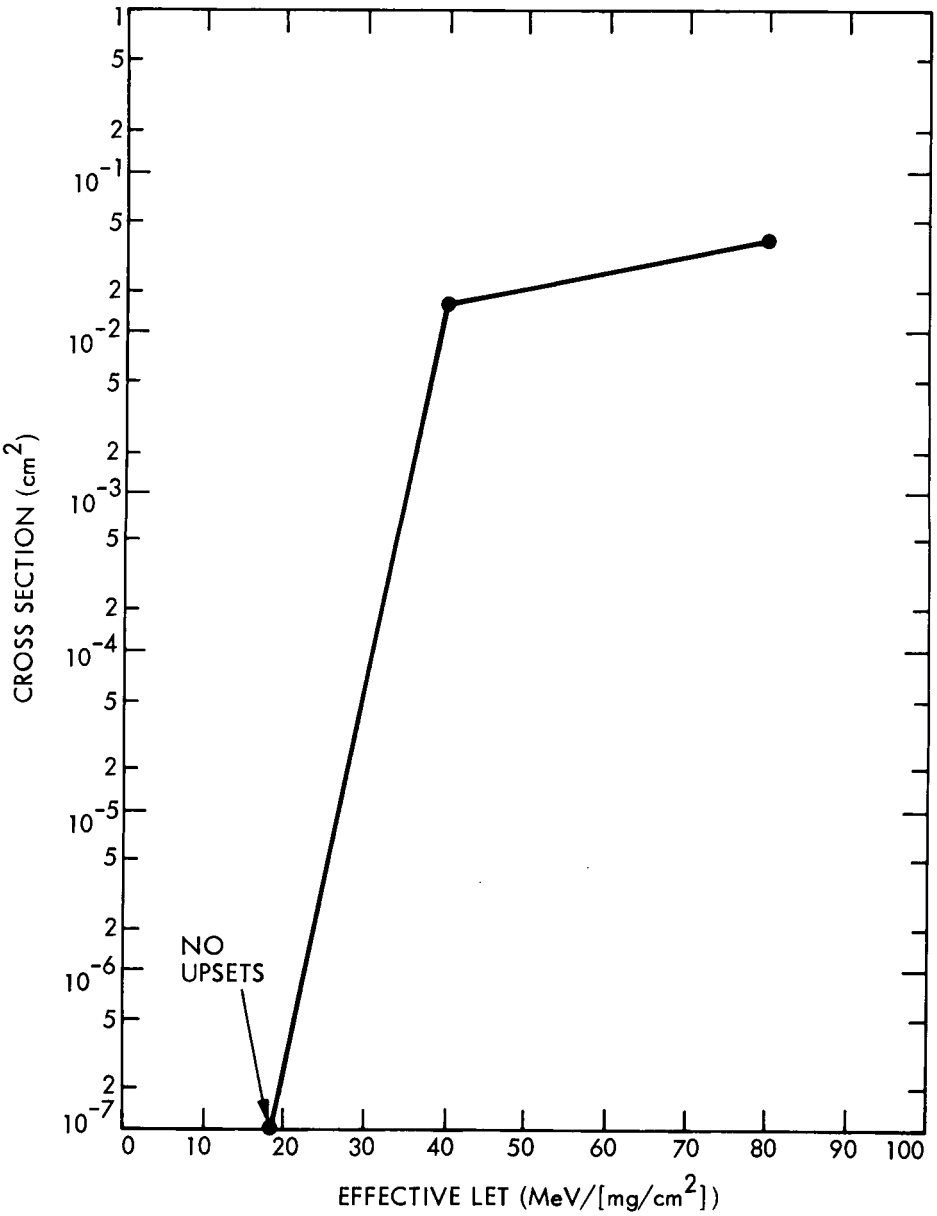

Figure 10. HS65262RH Harris CMOS 16K x 1 SRAM

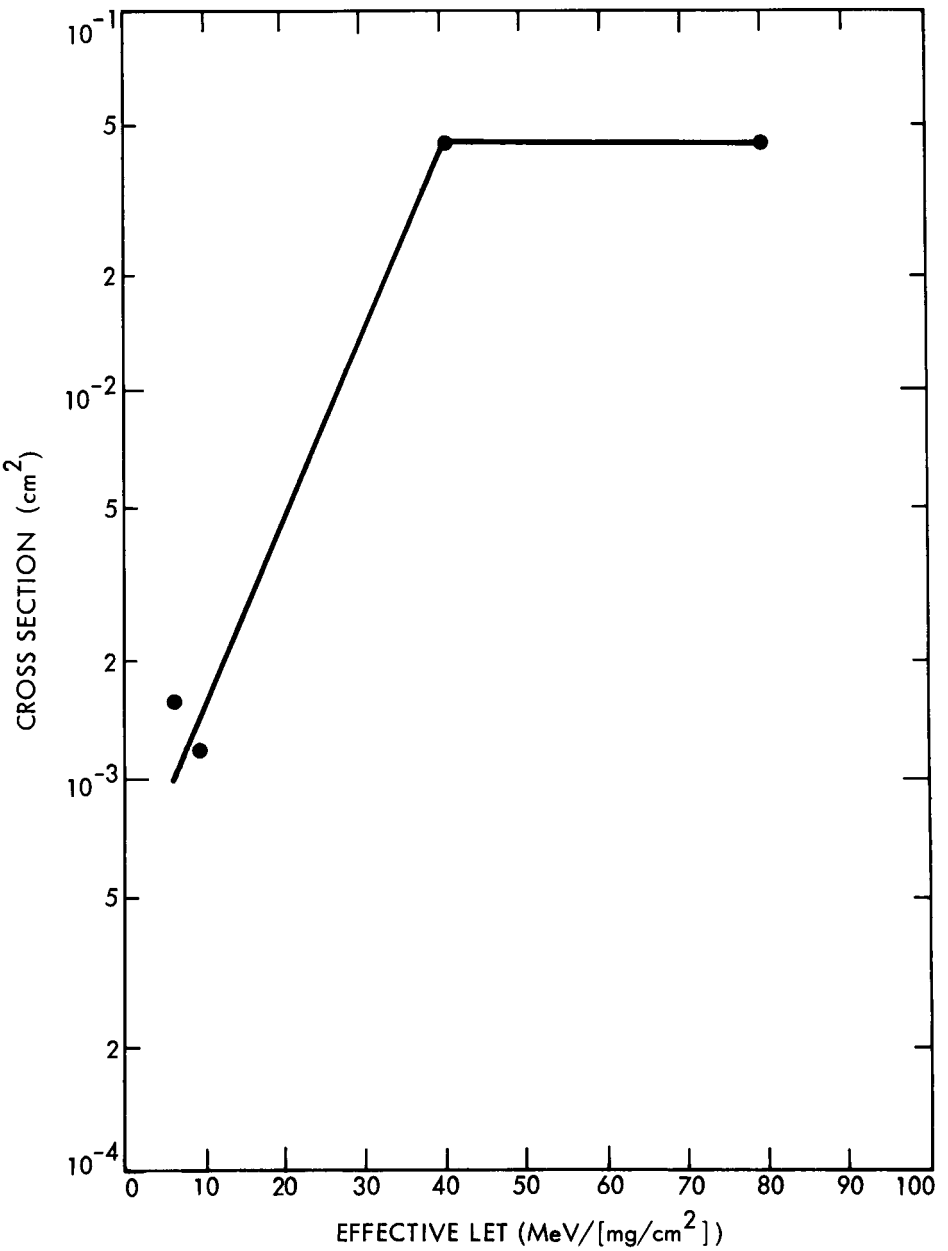

Figure 11. 8155 AMD NMOS 256 x 8 SRAM

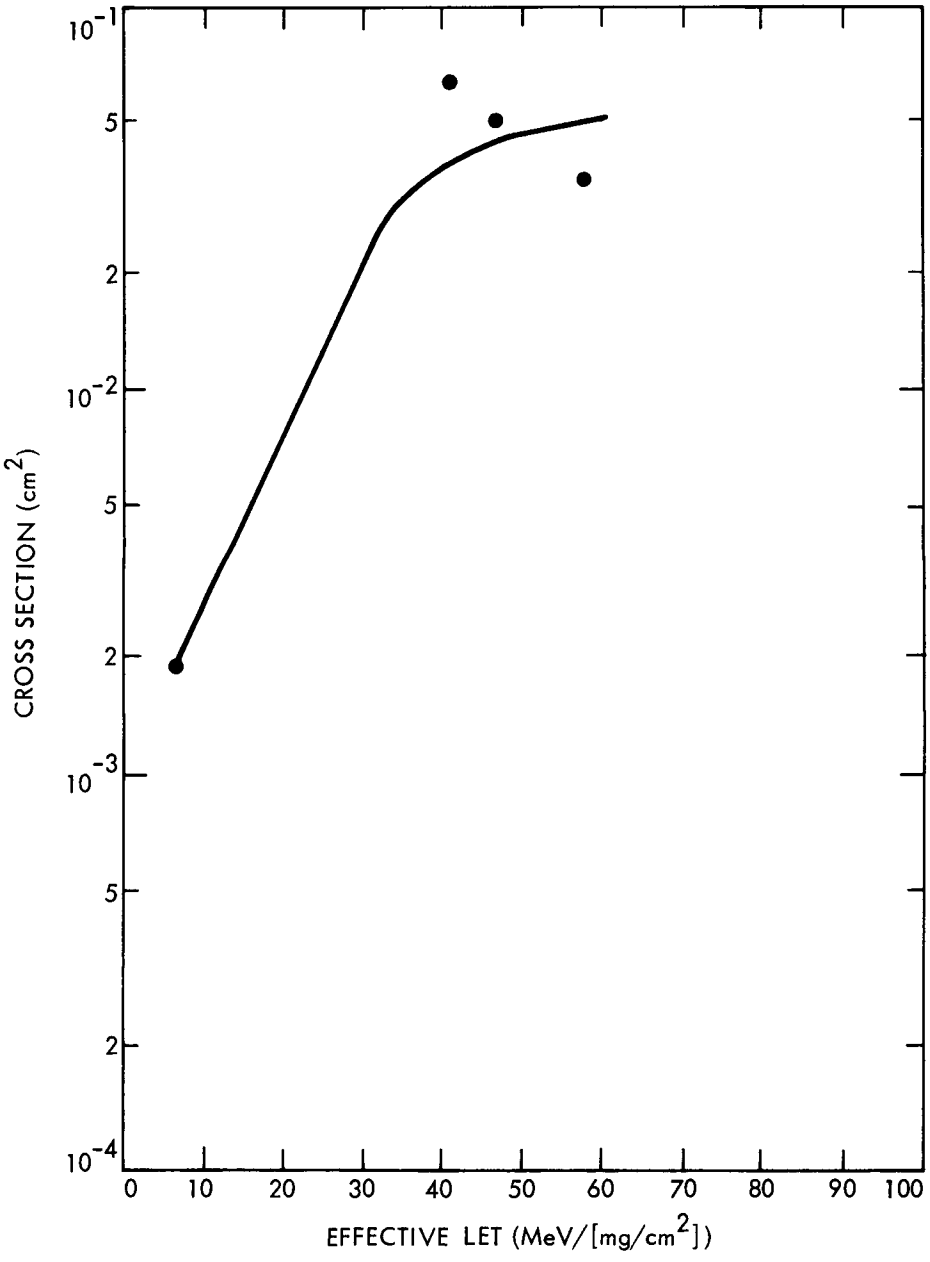

Figure 12. 8155 INTEL NMOS 256 x 8 SRAM

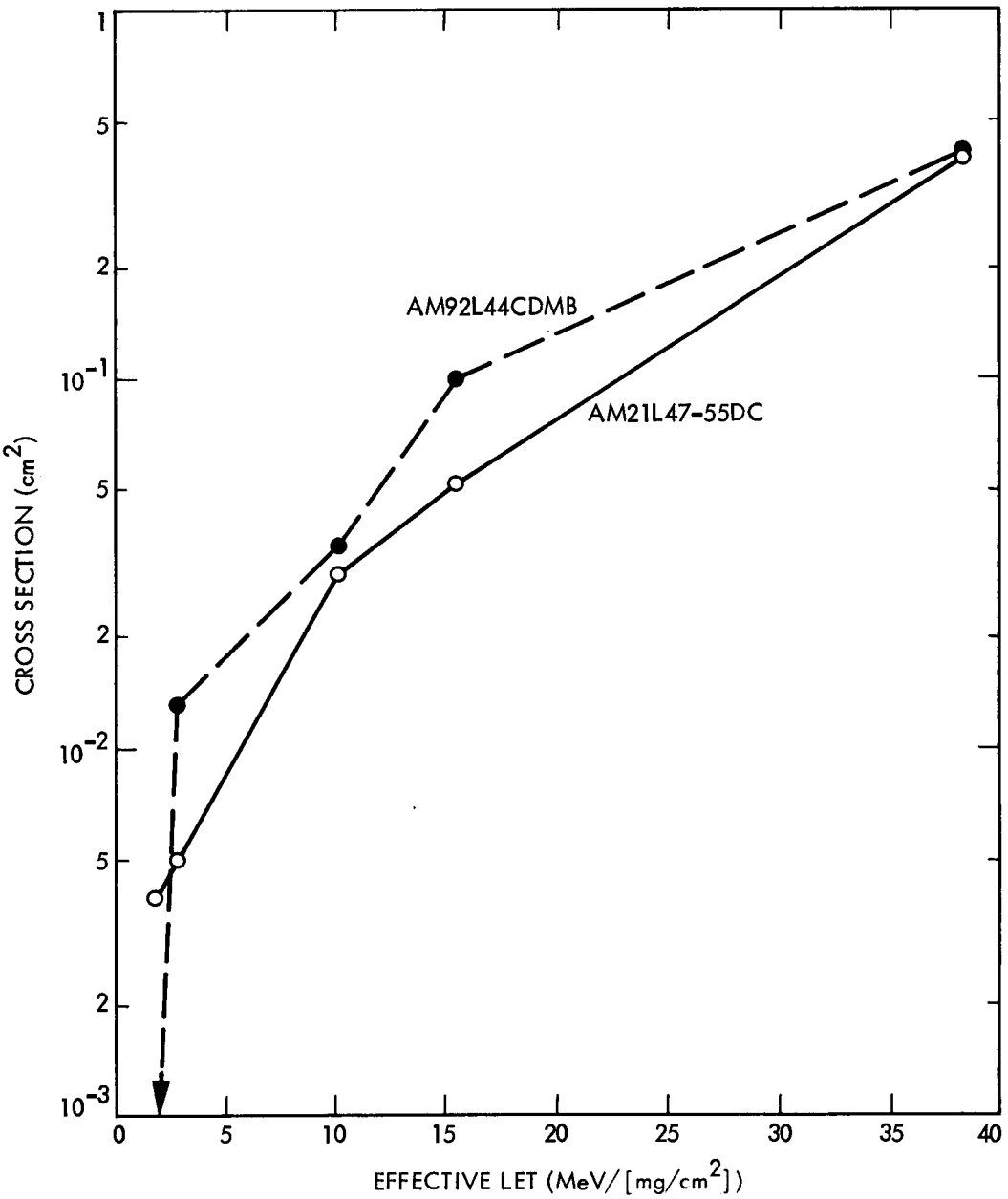

Figure 13. AM92L44 AMD NMOS 4K x 1 SRAM and AM21L47 AMD NMOS 4K x 1 SRAM

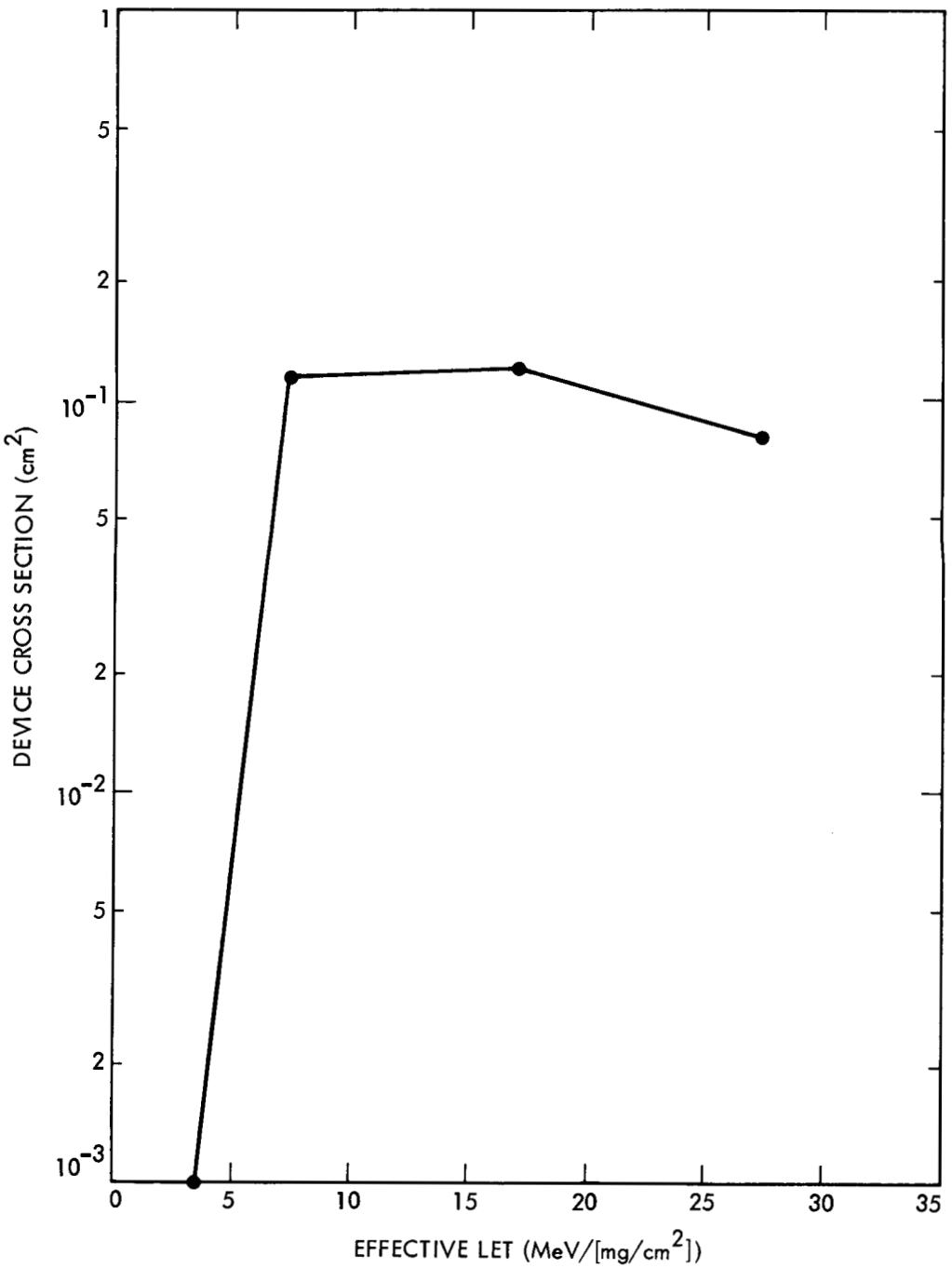

Figure 14. 81256 Fujitsu NMOS 256K x 1 DRAM

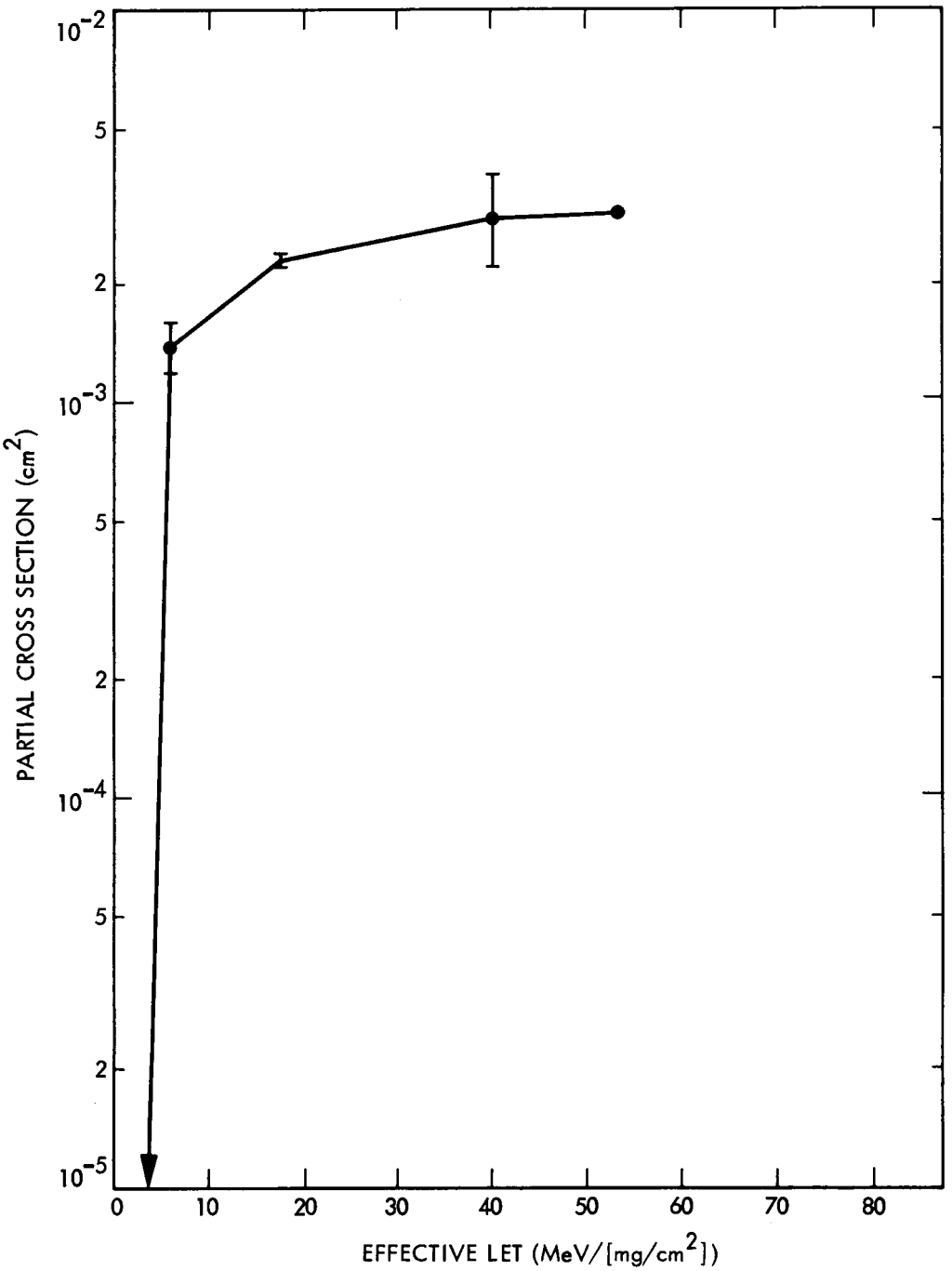

Figure 15. 2901B AMD LS TTL 4-Bit Slice. This data for the 64-bit unaddressed RAM equals ~2/3 of the total cross section.

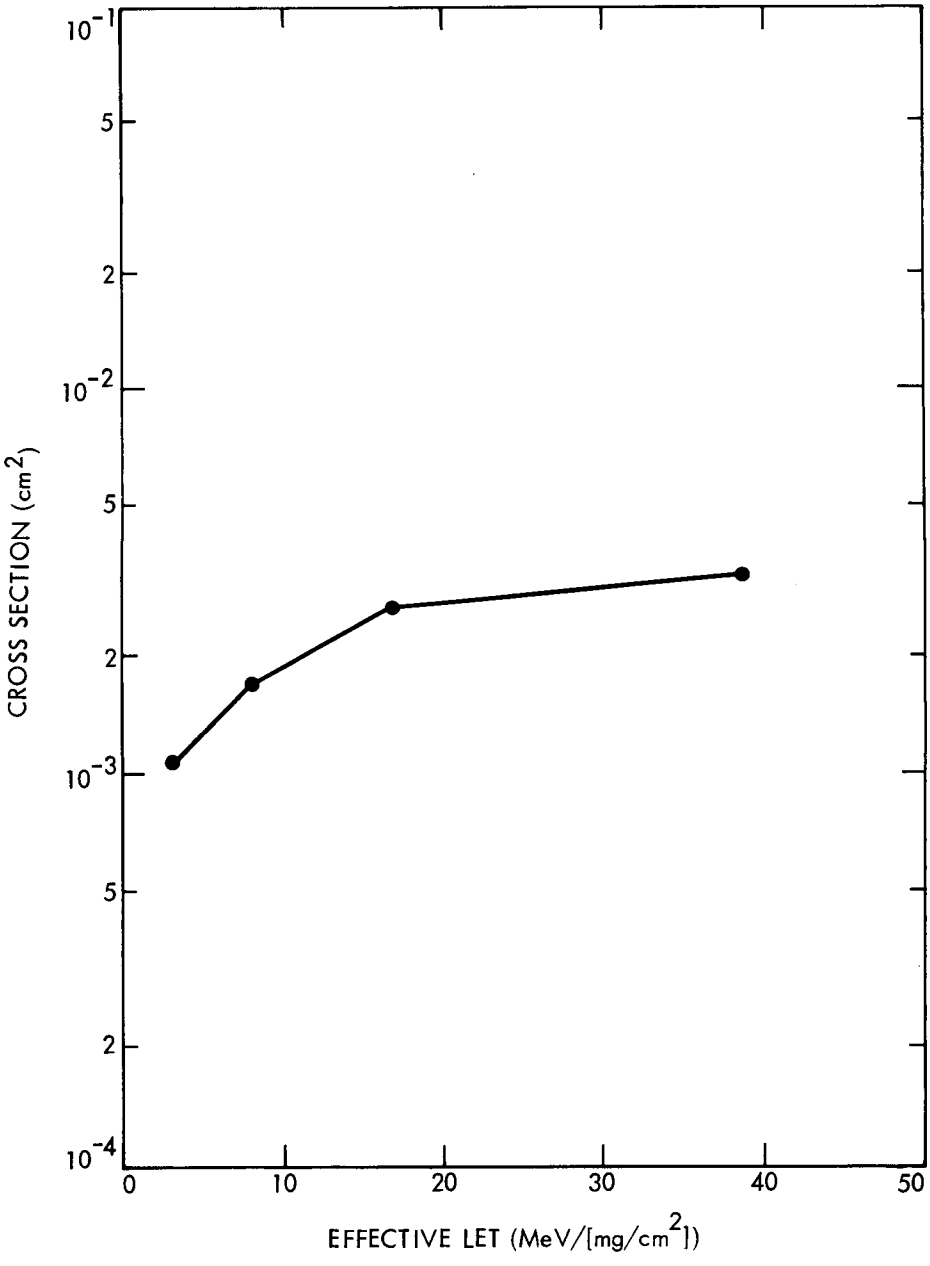

Figure 16. 2901C AMD ECL/TTL 4-Bit Slice

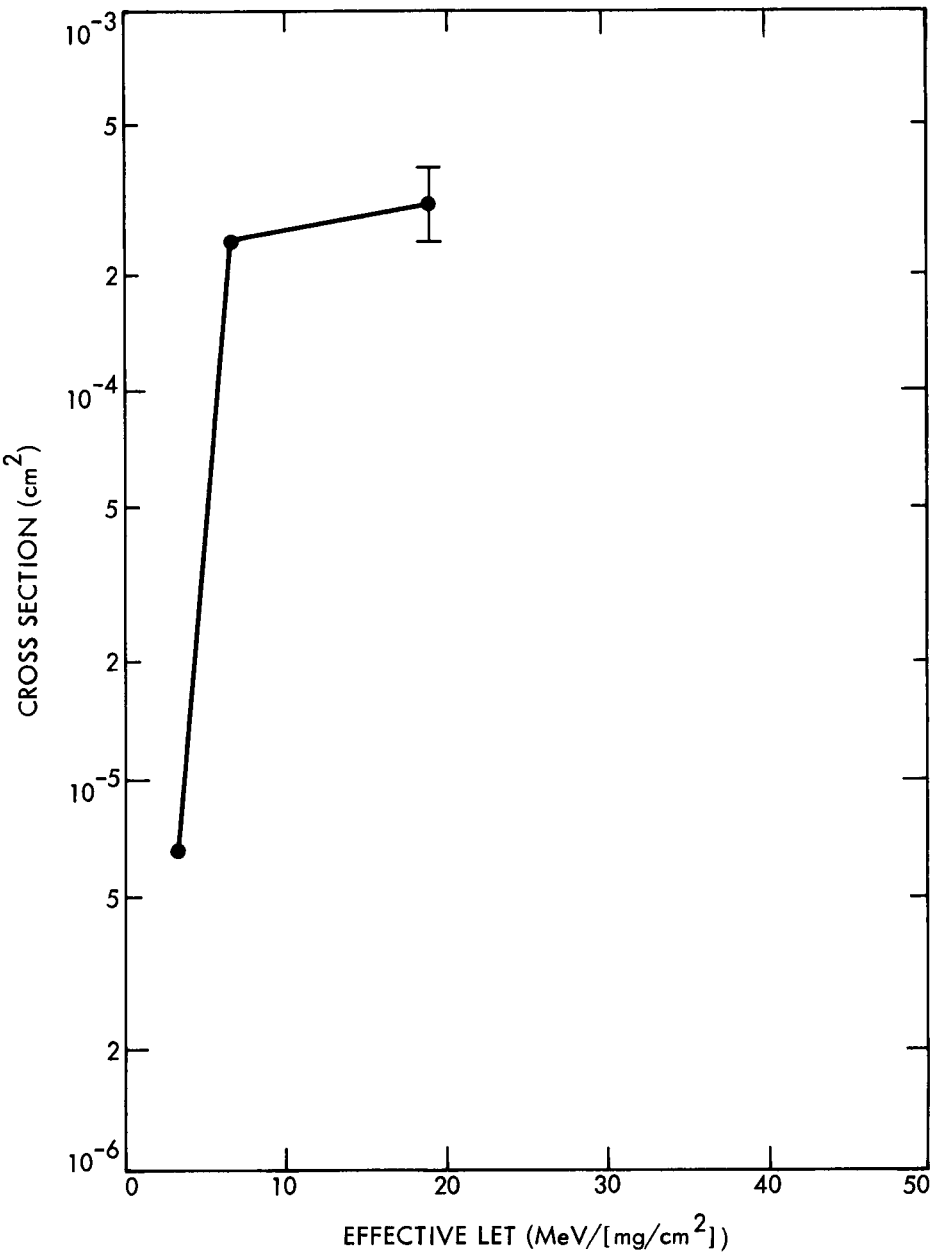

Figure 17. 2909A AMD LS TTL Microprogram Sequencer (Stack Plus Pointer)

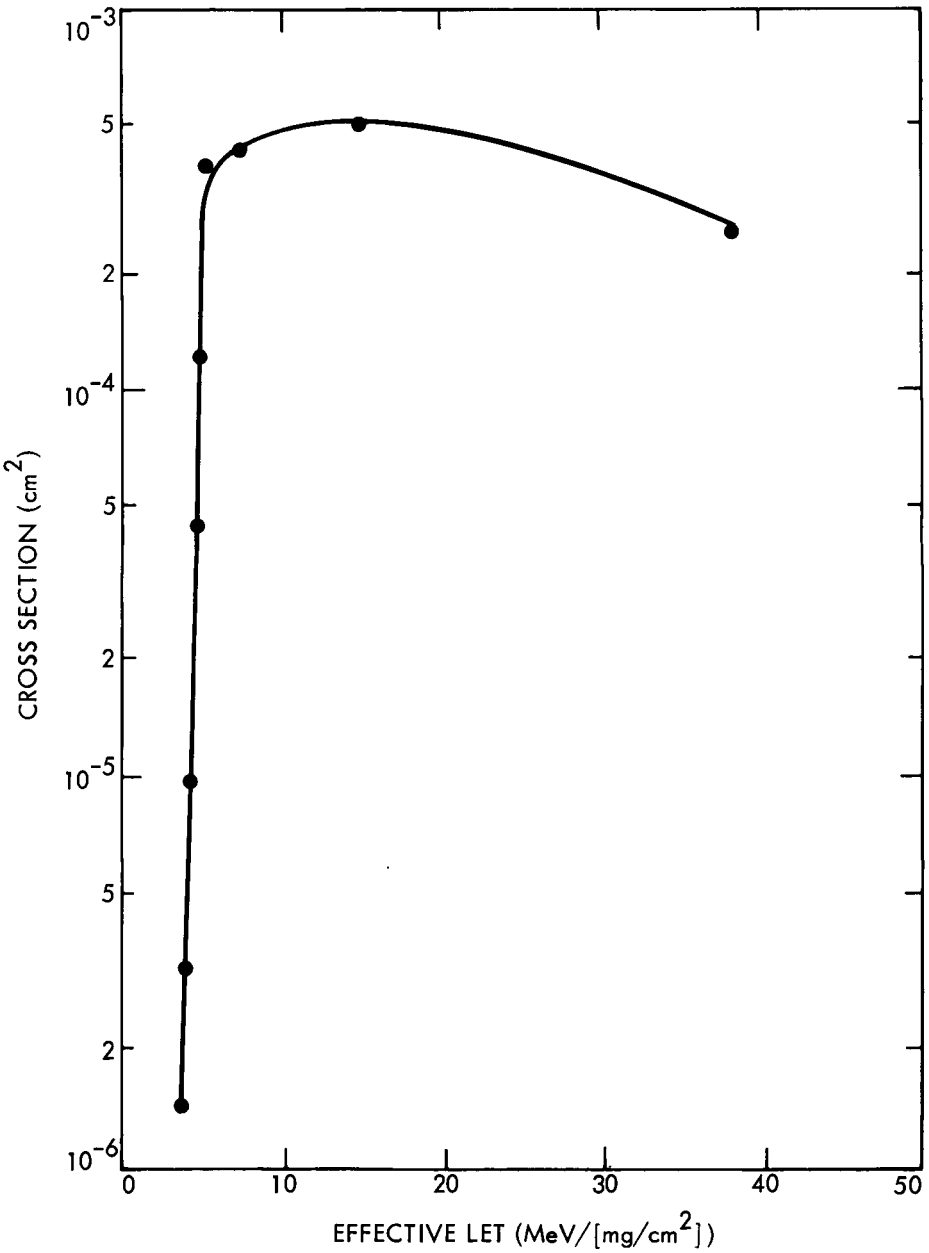

Figure 18. 2909 AMD LS TTL Microprogram Sequencer (Stack Plus Pointer)

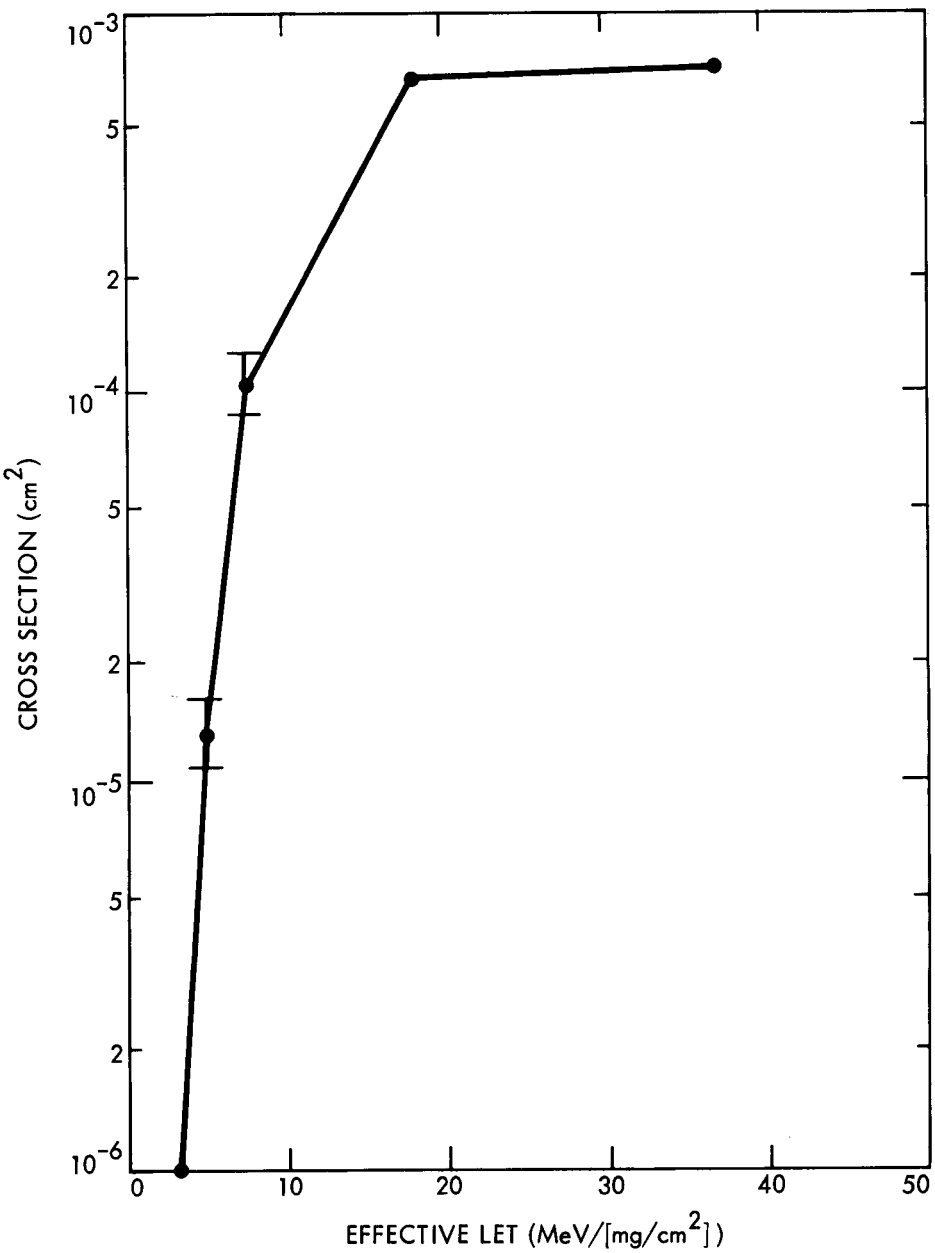

Figure 19. 9407 FSC TTL 9-Bit Data Register

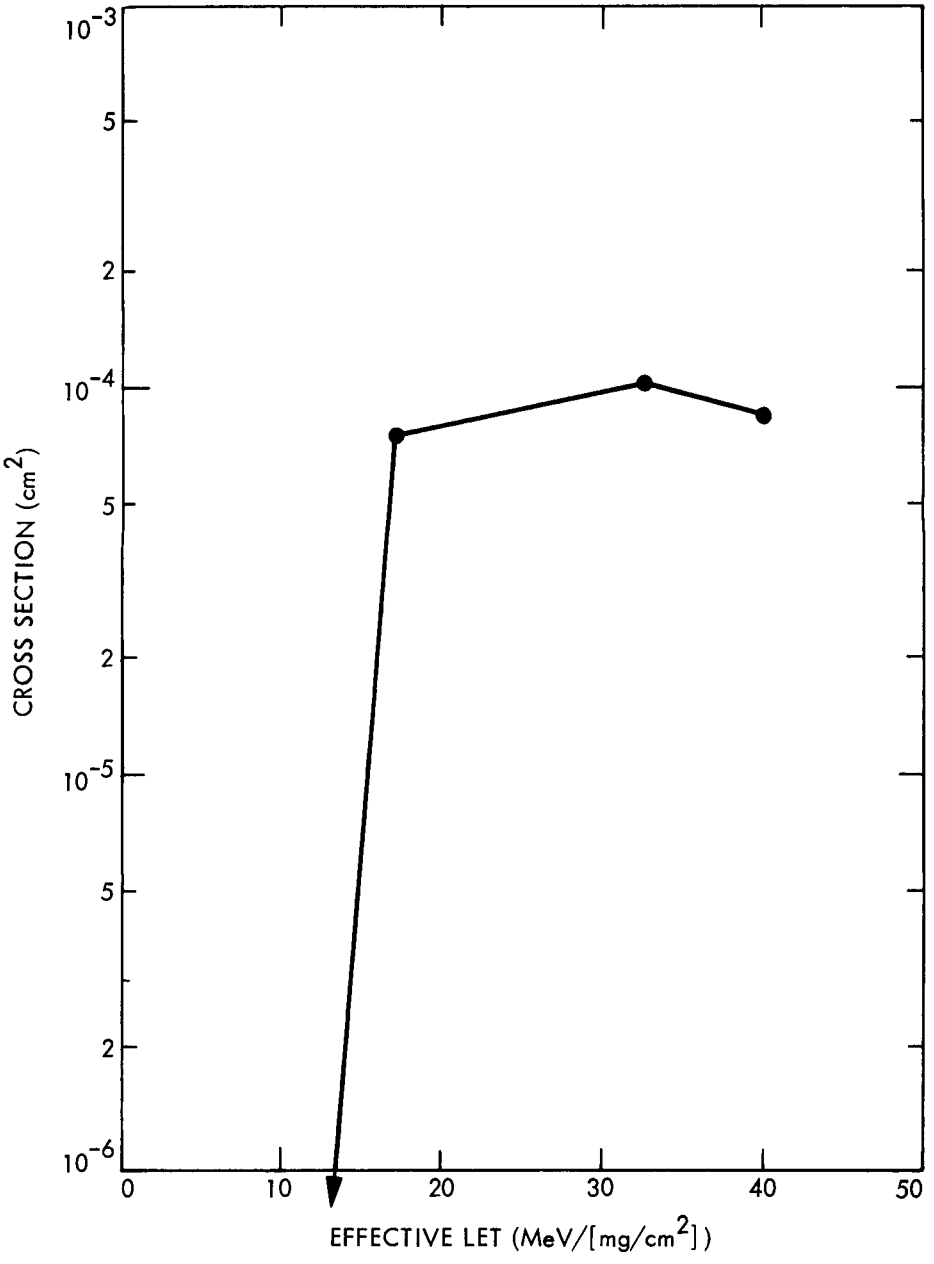

Figure 20. 54LS109 Fairchild LS TTL Dual J/K Flip-Flop

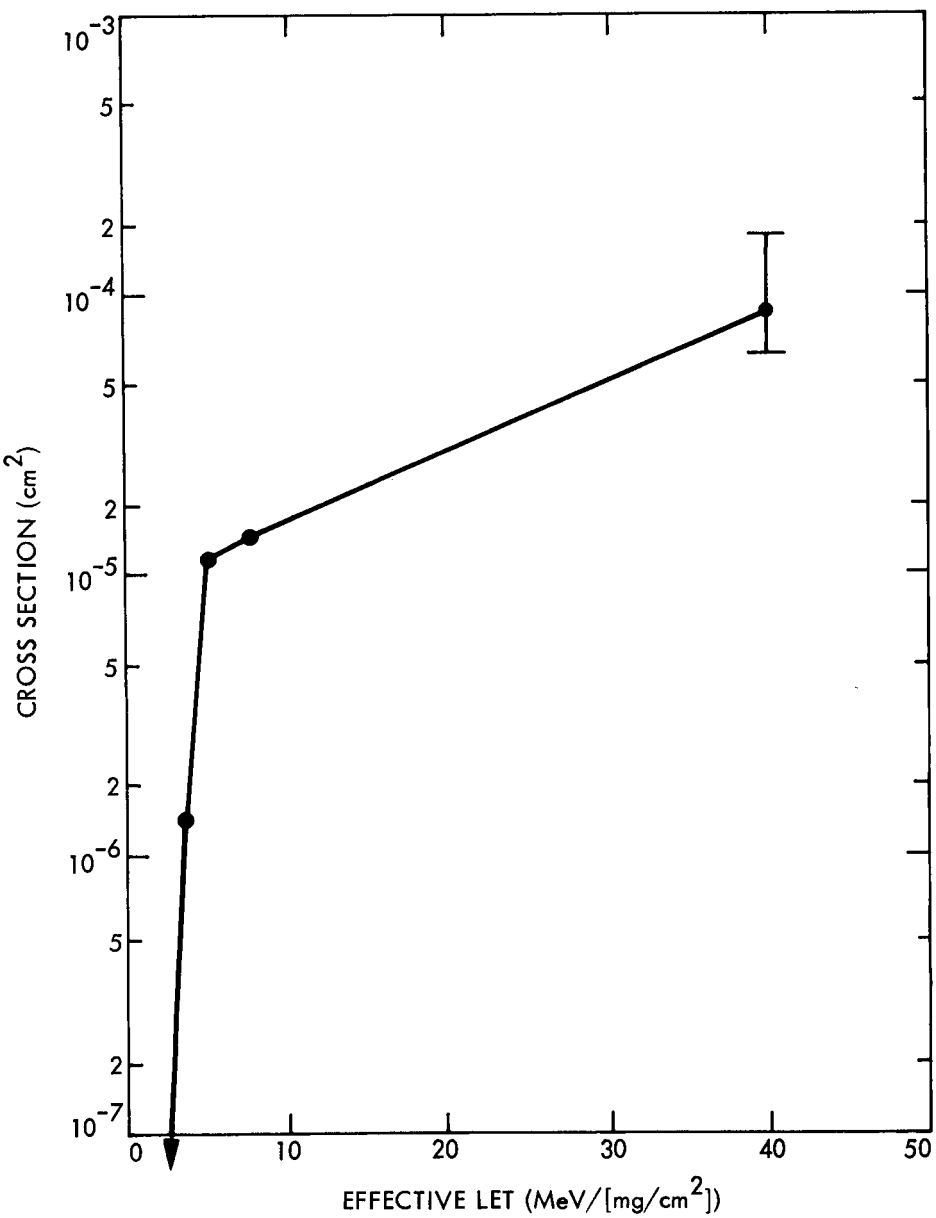

Figure 21. 54LS73 SGN LS TTL Dual J/K Flip-Flop

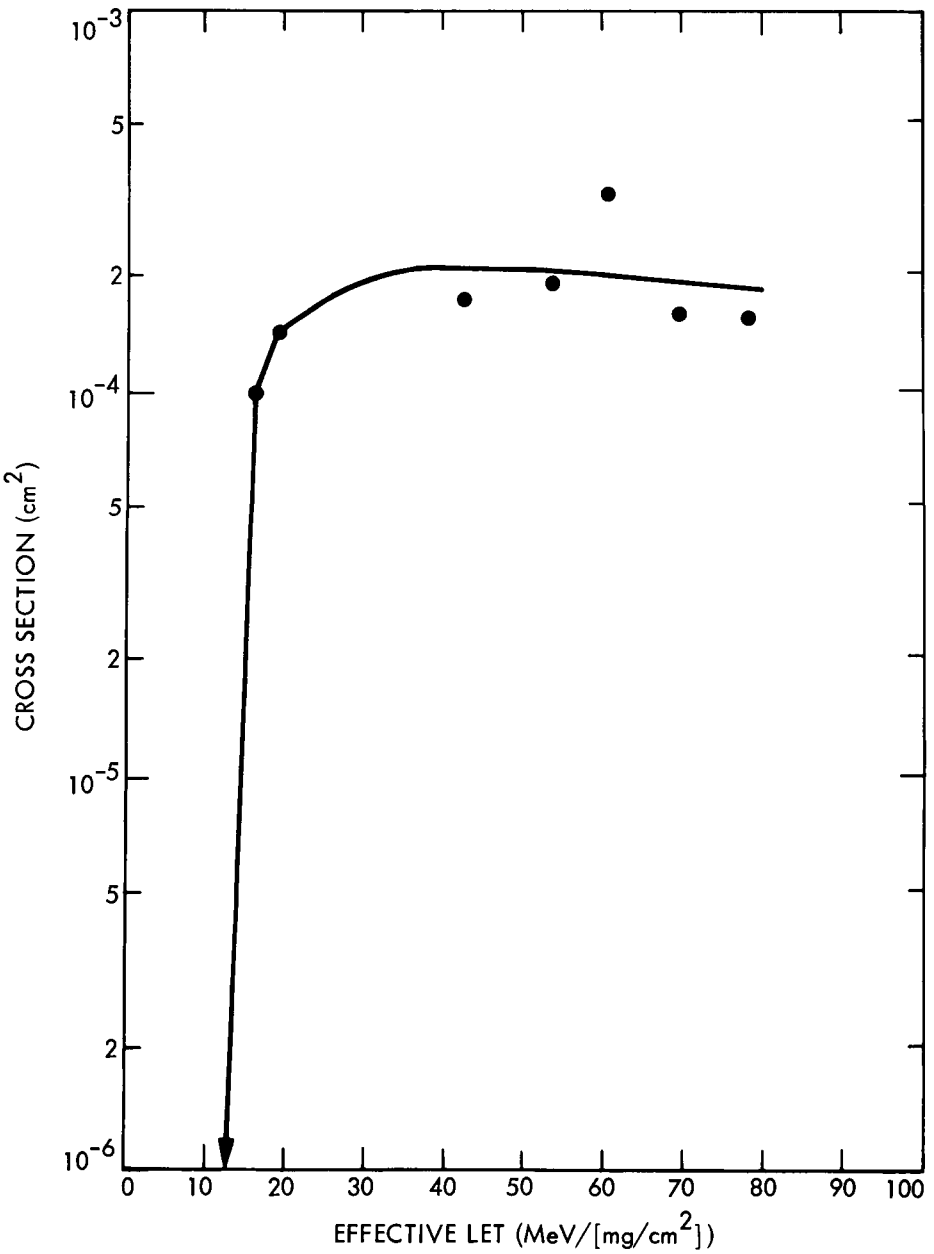

Figure 22. 54LS163 NSC LS TTL Synchronous 4-Bit Counter

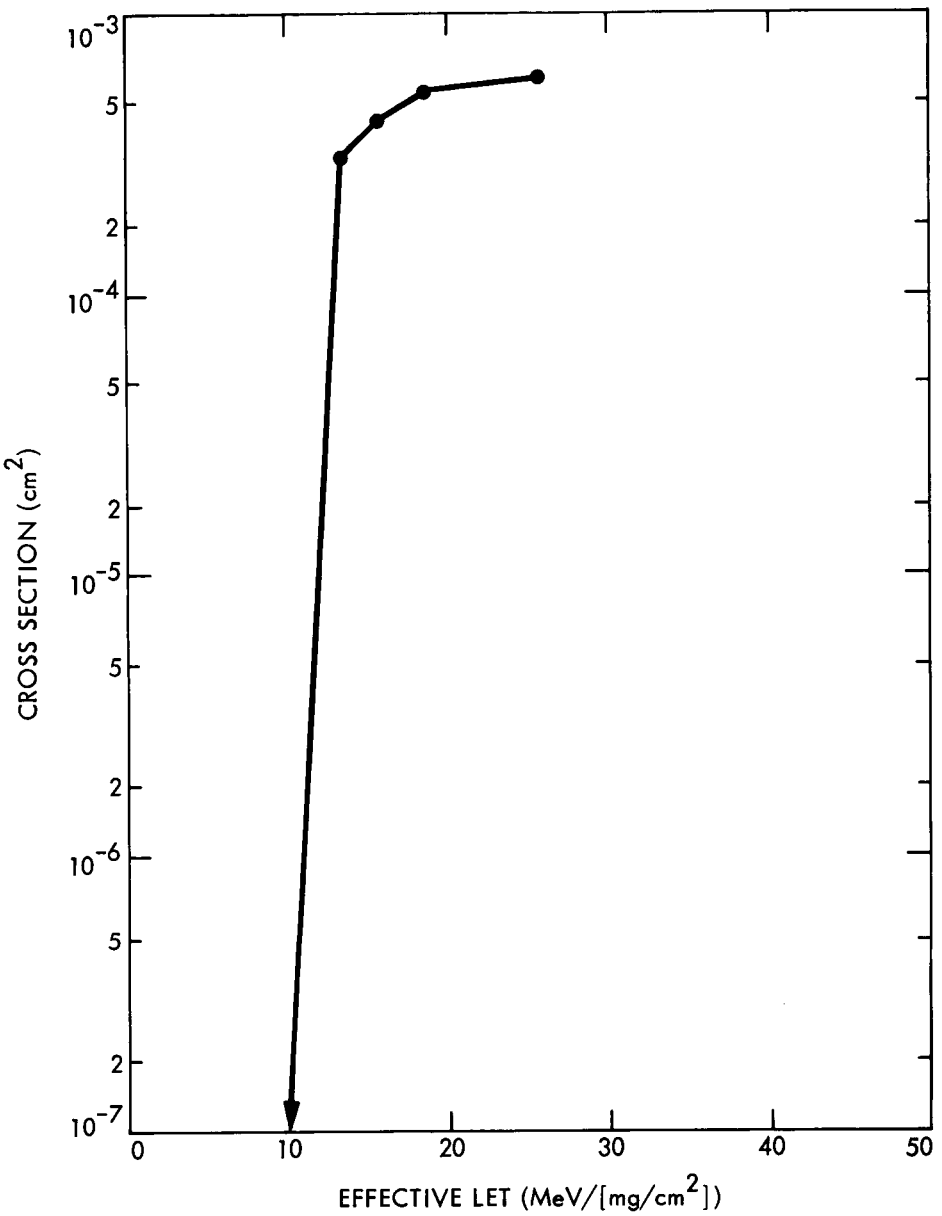

Figure 23. 54LS95 SGN LS TTL 4-Bit Shift Register

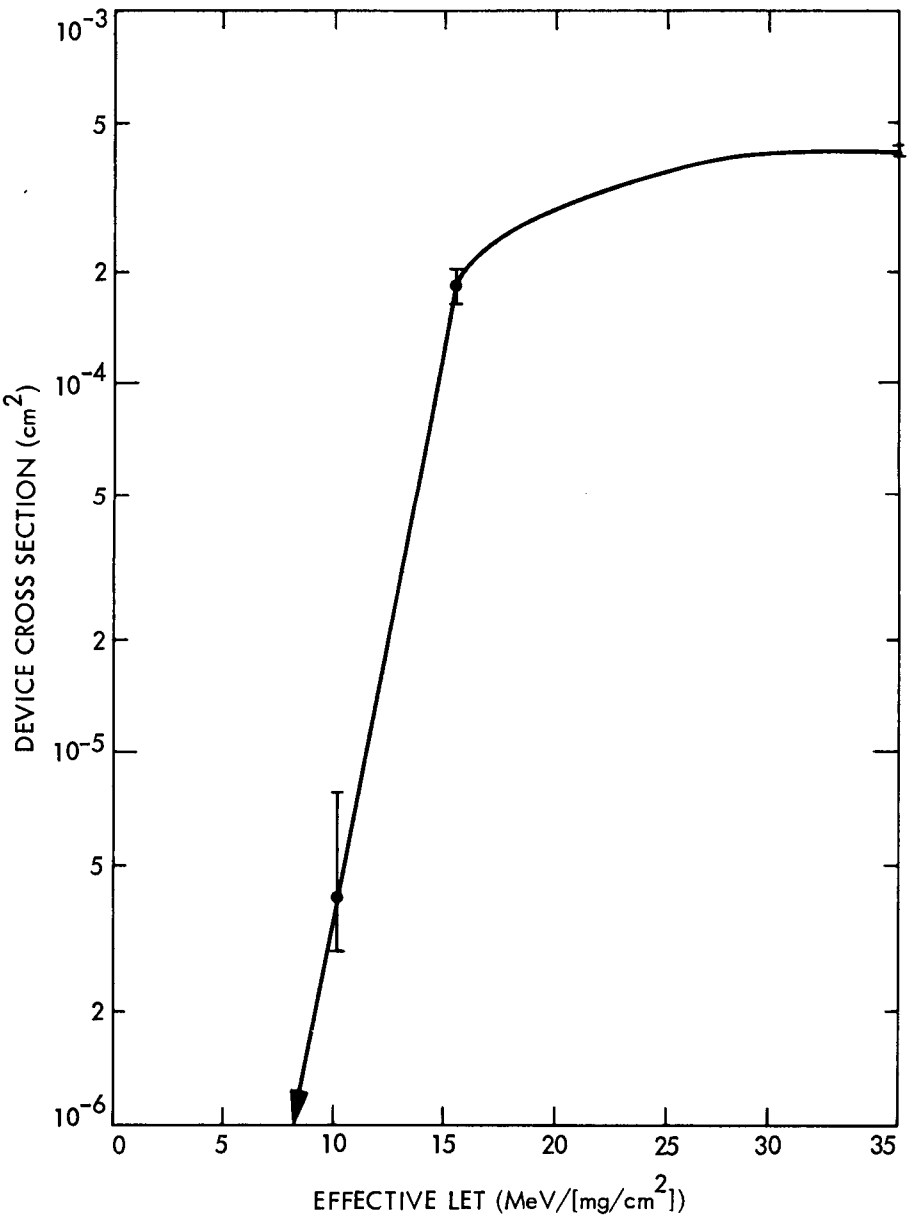

Figure 24. 54ALS373 TIX ALS TTL Octal Latch

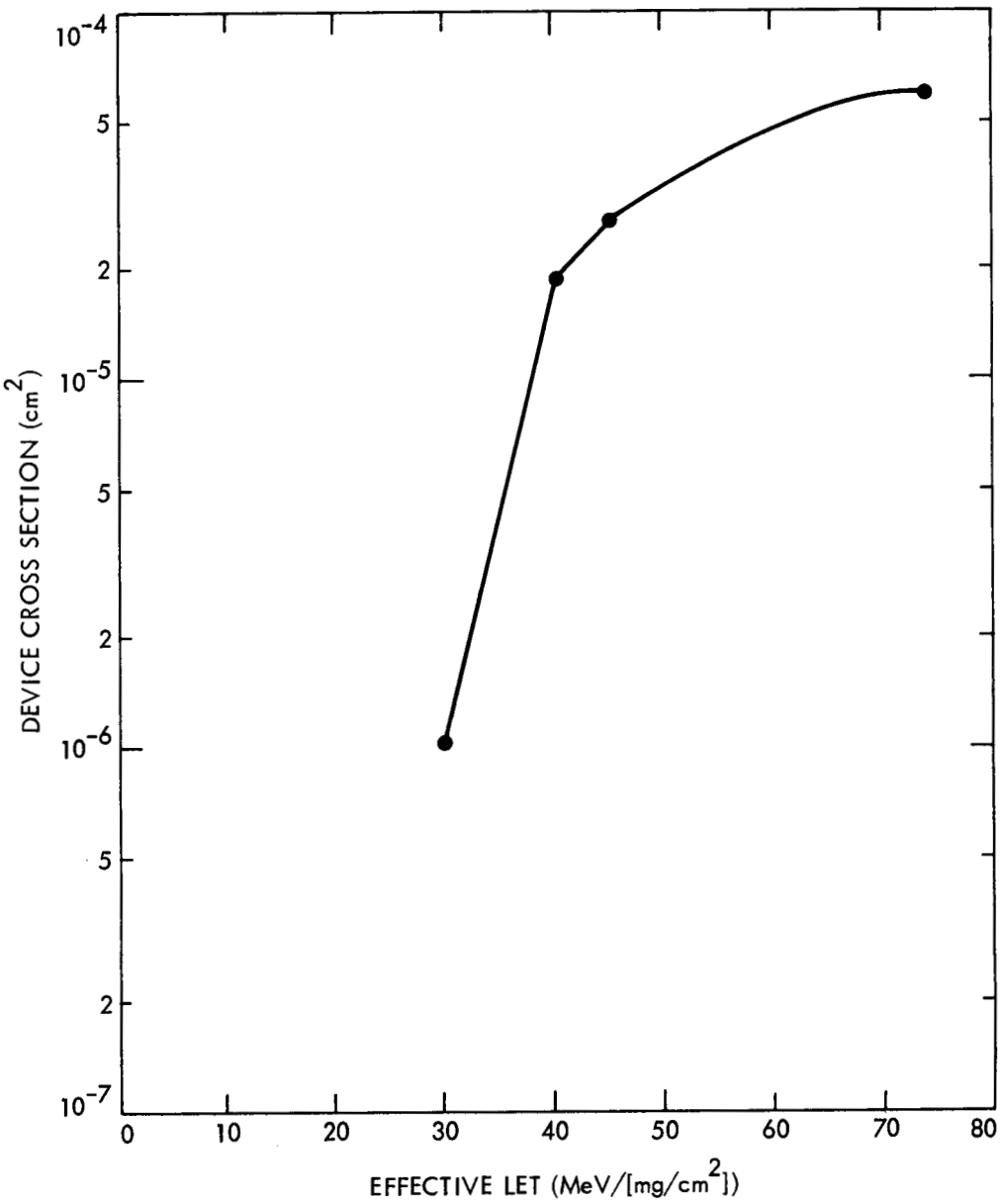

Figure 25. 54F373 Fairchild (FAST Technology) TTL Octal Latch

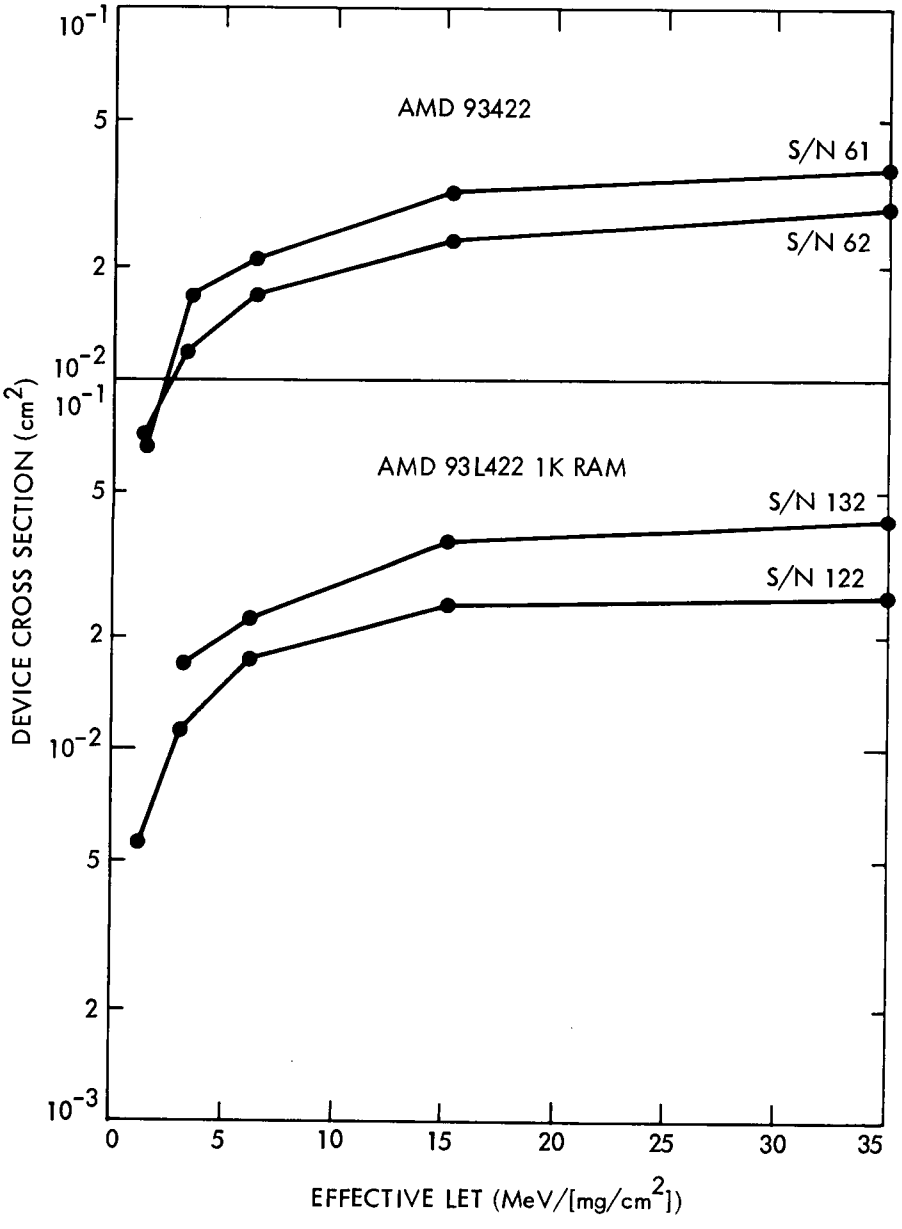

Figure 26. 93422 AMD TTL and 93L422 AMD LTTL 1K x 1 SRAMs. Devices are operated at 250 kHz.

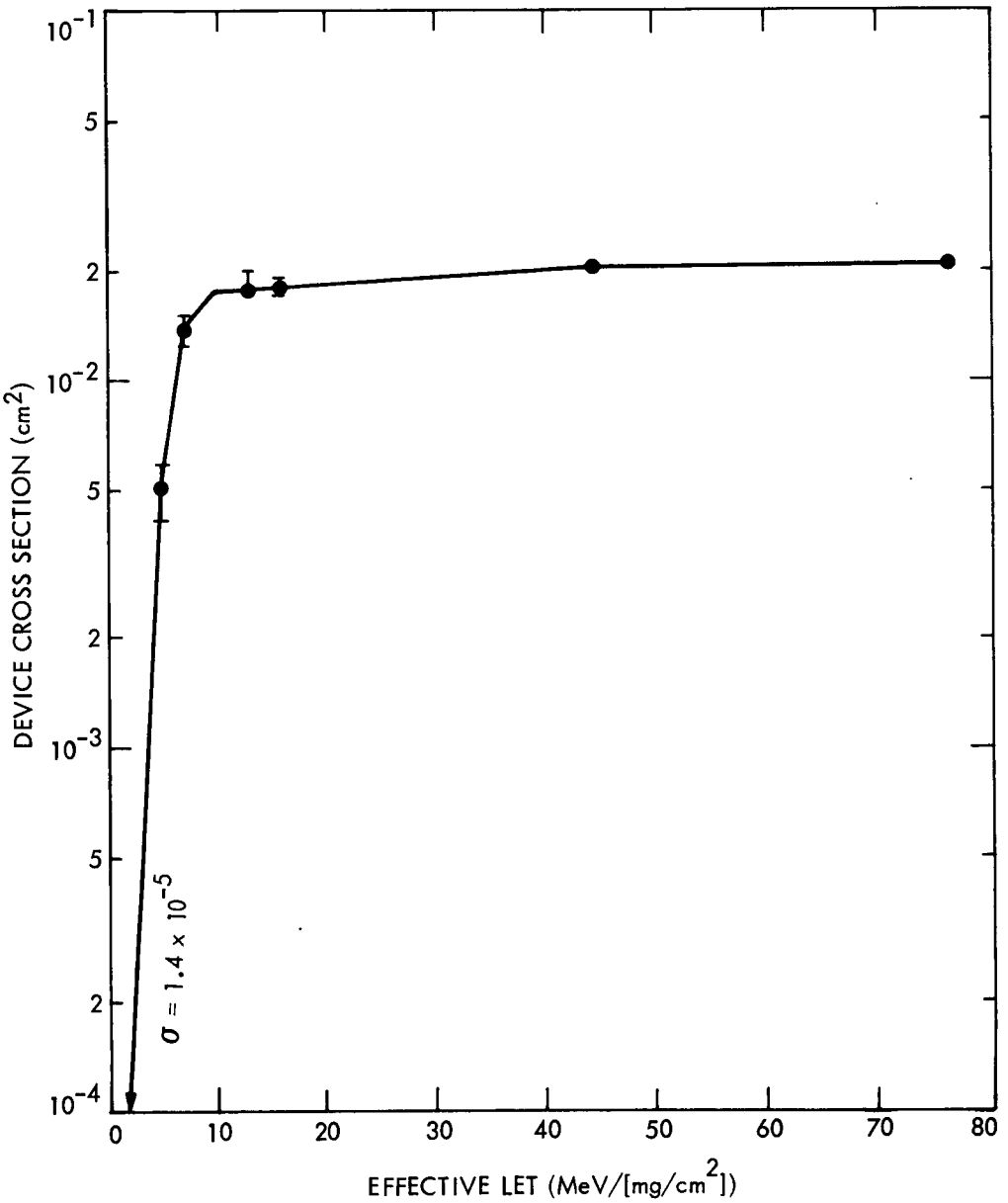

Figure 27. 82S212 Signetics TTL 256 x 9 SRAM

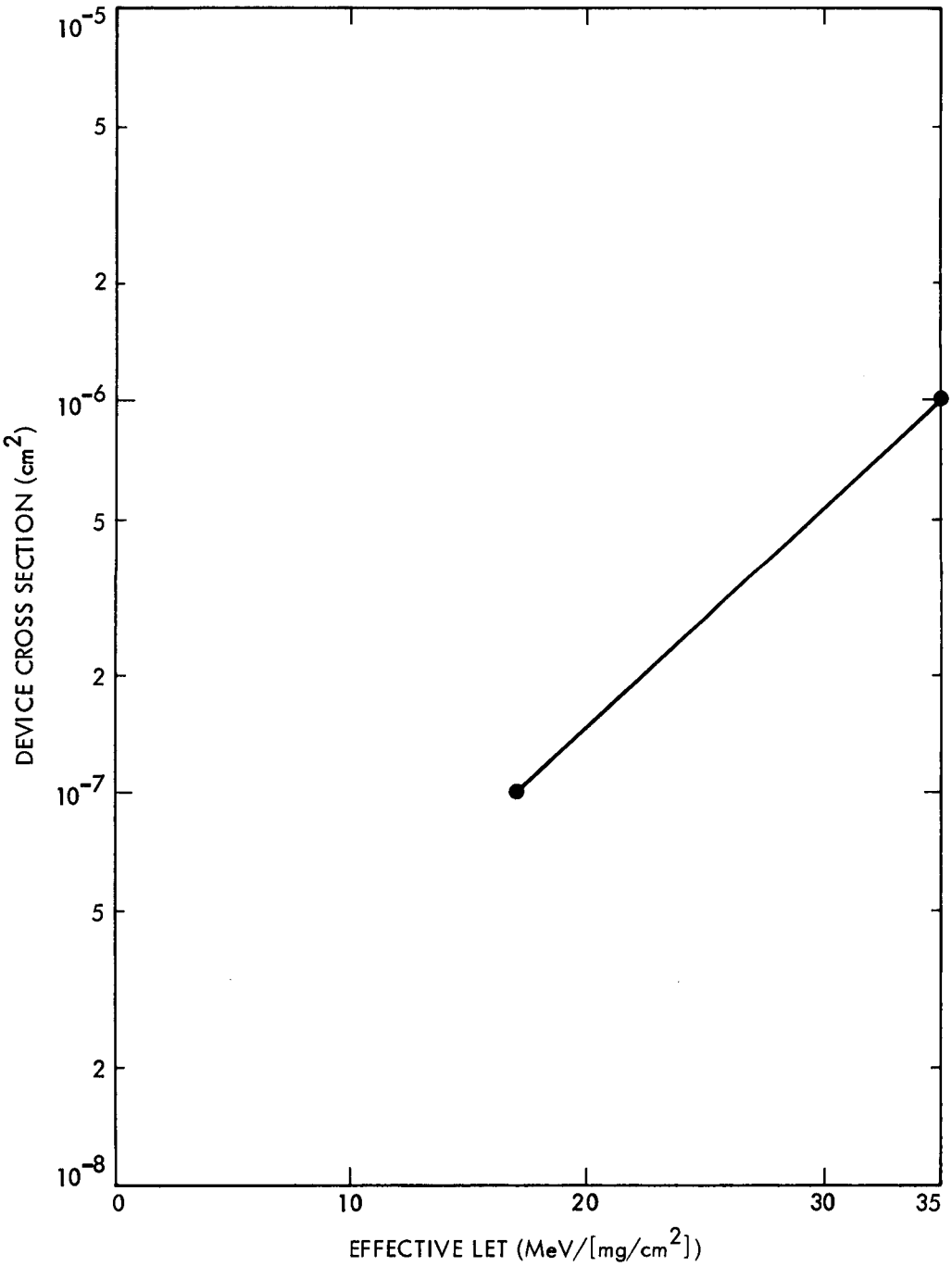

Figure 28. AM6012 AMD Bipolar Digital-to-Analog Converter (DAC) and AD562 ADI Bipolar DAC. The curves for each device are identical.

SECTION VIII

REFERENCES

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(8) T. A. Fischer, "Heavy-Ion-Induced Gate-Rupture in Power MOSFETs," IEEE Trans. on Nuclear Science, NS-34, No. 6, 1786 (Dec. 1987).

(9) A. L. Friedman, "SEU in Combinatorial and Sequential Current Mode Logic," IEEE Trans. on Nuclear Science, NS-32, No. 6, 4216 (Dec. 1985).

(10) J. Adams, Jr., IEEE Trans. on Nuclear Science, NS-31, No. 6, 1212 (Dec. 1984).

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APPENDIX A

VENDOR IDENTIFICATION CODE LIST

VENDOR IDENTIFICATION CODE LIST

ADI	Analog Devices
AMD	Advanced Micro Devices
ATT	American Telephone and Telegraph
FSC	Fairchild Semiconductor
FUJ	Fujitsu Electronics
GEC	General Electric Corporation
GIC	General Instruments Corporation
HAR	Harris Semiconductor Corporation
HPA	Hewlett-Packard Corporation
HON	Honeywell
HUG	Hughes Microelectronics
IDT	Integrated Devices Technology, Inc.
INL	Intersil Electronics
INT	INTEL Corporation
MDD	McDonnell Douglas
MOS	MOSTEK
MOT	Motorola, Inc., Semiconductor Products Division
MIC	Micron Technologies
MNC	Micro Networks
MTL	Mitel
NCR	National Cash Register
NSC	National Semiconductor Corporation
PHL	Phillips of North America Corporation
RAY	Raytheon Company
RCA	RCA Corporation, Solid State Division
ROC	Rockwell International, Semiconductor Division
SGN	Signetics Corporation
SIL	Siliconix Devices, Inc.
SNL	Sandia National Laboratories
SPI	Semi Processes, Inc.
STX	Supertex, Inc.
TIX	Texas Instruments, Inc.
TRW	TRW, Inc., Semiconductor Division
WEC	Westinghouse
XIC	XICOR
ZIL	Zilog

APPENDIX B

UPSET RATE CALCULATIONS

Accurate upset rate calculations require a computer code to integrate the measured device cross section over the heavy ion flux (each a function of LET) in such a manner that additional charge deposited by ions impinging obliquely on the device is properly accounted. This latter effect requires, in turn, a knowledge of the three-dimensional geometry of the device sensitive volume. Determination of the heavy ion flux is another separate problem that may require consideration of spacecraft shielding, altitude (trajectory), orbital inclination with respect to the equator, flare distributions, time period in the solar cycle, earth shielding, etc. Hence, it should not be assumed that an accurate evaluation can be made without contacting an organization possessing such a computer code. Some of these organizations are:

JPL - Paul Robinson or Don Nichols (Pasadena, CA)
Naval Research Labs - James Adams, Jr. (Washington, D.C.)
IRT - Jim Pickel (Placentia, CA)

Nevertheless, it is useful to try to arrive at an order-of-magnitude estimate. To zeroth order, one can estimate:

$$\text{Upset Rate} = A\,\bar{\sigma} \times \text{Flux}$$

where A is a factor allowing for the additional effect of ions that impinge omnidirectionally on the device, $\bar{\sigma}$ is an average cross section weighted toward a value representative of the more numerous lower LET ions, and Flux is the number of ions/cm^2/day having an LET greater than the measured threshold LET of the device.

The factor A is itself a complex entity, which may be equal to 2 or 1,000. Note also that if there are no ions in a specified environment with an LET greater than the measured device threshold LET, there may still be upsets from ions impinging obliquely. In this case, the above approximation fails completely and even a computer program is severely tested.

The environmental flux can be approximated in many cases by one of the three broad categories given in Table B-1. "Near Earth (30°)*" is a benign environment, shielded by the earth's magnetic field. Only very energetic ions (with a correspondingly low LET) are capable of penetrating the geomagnetic field, so there are very few ions with an LET > 2 MeV/mg/cm^2. Note, however, that shielding will only slow these ions and thereby increase the fraction having a higher LET.

The "Near Earth (90°)*" environment is dominated by the galactic cosmic ray environment, because these ions are capable of penetrating to low altitudes near the earth's poles. This environment is seen to be about 1/6 that of geo-synchronous orbit. The reduction factor arises from the earth's shielding at low altitudes (1/2) and geomagnetic shielding over two-thirds of the orbital path. Exact calculations available from GSFC (Goddard) by E. Stassinopoulos are given in Table B-1.

*The angles refer to the inclination of the orbit with respect to the equator.

The geosynchronous environment is equivalent to that present throughout the solar system, and has been derived from a series of detailed computations by J. Adams (Ref. 10). The tabulated environment presents a maximum galactic flux (occurring at solar minimum) and accounts for solar flares by representing the condition when the flux in space is less than the tabulated value 90% of the time. These values assume 100 mil of aluminum shielding, but minor thickness variations have little effect on galactic cosmic ray distributions. The shielding is important, however, in reducing or stopping the relatively low energy heavy ions present in flares. During the 11-year solar cycle, the galactic flux is modulated by a factor of three or five with smaller fluxes reaching earth during the peak period of solar activity. This advantage may be offset by increased flare activity which actually dominates the total unshielded fluence of heavy ions over the long run (one-year time span).

An example calculation of upset rates is given for a representative microprocessor cross section presented in Fig. B-1 as follows. Consider the question: What is the upset of this part in transit to Jupiter?

Answer: Take A = 3.
Perform a coarse manual integration of cross section times flux.
Select values of an average cross-section ($\bar{\sigma}$) from Figure B-1 versus LET.

For LET ranging from:
3 to 6, take $\bar{\sigma} = 10^{-4}$ cm^2
6 to 15, take $\bar{\sigma} = 3 \times 10^{-4}$ cm^2
15 to 35, take $\bar{\sigma} = 7 \times 10^{-4}$ cm^2

The corresponding flux interpolated from the "geosynchronous" column of Table B-1 is taken as:

LET:
3 to 6, Flux = 35 - 5 = 30 ions/cm^2/day
6 to 15, Flux = 5 - 0.5 = 4.5 ions/cm^2/day
15 to 35, Flux = 0.5 ions/cm^2/day

$$\text{Upsets} = A\,(\Sigma\,\bar{\sigma} \bullet \text{Flux}) = 3(30 \times 10^{-4} + 13.5 \times 10^{-4} + 3.5 \times 10^{-4})$$
$$= 3(4.7 \times 10^{-3})/\text{day}$$
$$= 1.4 \times 10^{-2} \text{ upsets/day}$$

The above result is a crude estimate for one part, assuming a 100% duty factor. For a system calculation, one must multiply by the number of such parts, as well as by a meaningful value for the duty factor (DF). The DF will depend on system usage as well as the internal workings of the microprocessor (a subject beyond the scope of this report).

Table B-1. Heavy Ion Flux Environments*

NEAR EARTH (30°)**		NEAR EARTH (90°)†	GEOSYNCHRONOUS††
LET (MeV/mg/cm^2)	Flux (ions/cm^2/day)	Flux (ions/cm^2/day)	Flux (ions/cm^2/day)
0.5	15	180	600
1	10	90	270
2	~10^{-2}***	10	50
5	10^{-3}***	1.2	6
10	10^{-4}***	0.2	1
20	$<<10^{-6}$***	3.0×10^{-2}	0.15
26 (Fe)	--	1.1×10^{-2}	4×10^{-2}
40 (Kr)	--	$<10^{-5}$	4×10^{-5}

*90% worst-case flares and 0.68 g/cm^2 Al (100 mils) shielding. See pp. B-3 and B-4.

**The angle of orbital inclination is $\leq$30° with respect to the equator. These calculations assume 2π steradians of space and are taken from Ref. 10, Figure 5. These numbers are independent of altitude between 200 and 1200 km. See also Ref. 11.

***These fluxes increase if thick shielding is included (as in the space station), because the shield generates lower energy, higher LET ions.

†Polar orbit is 90° $\pm$25° with respect to the equator. These calculations are taken from a printout provided by E.G. Stassinopoulos of GSFC (Goddard). These numbers are independent of altitude between 200 and 1200 km.

††These calculations are taken from Ref. 10, Table I, and assume that there are 4π steradians of flux. This environment applies to all regions beyond geosynchronous orbit as well.

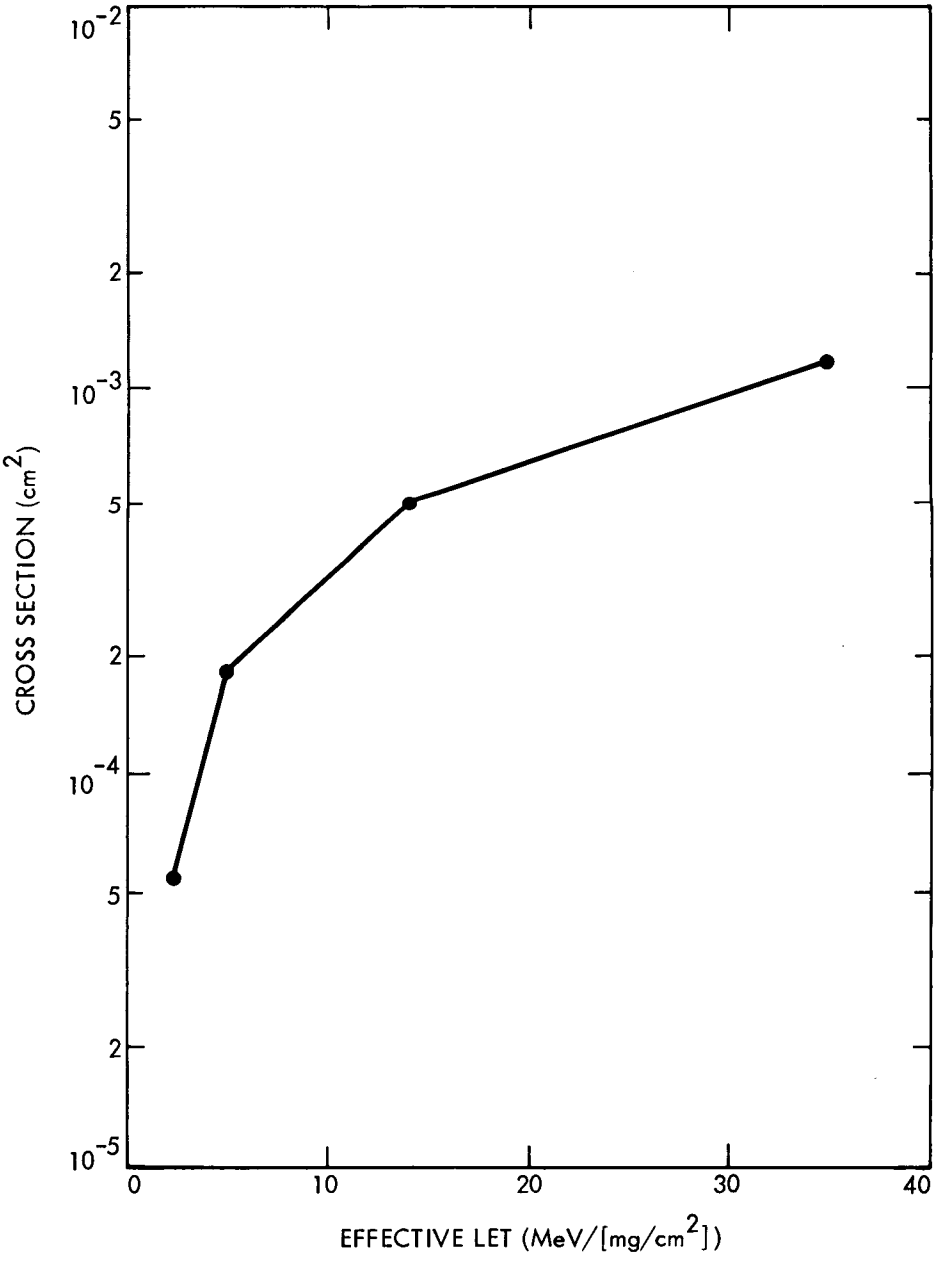

Figure B-1. Sample Cross Section

APPENDIX C

BEAM PARAMETERS FOR FIGURES 4 THROUGH 28

The beam parameters for each "effective LET" point of the plotted data curves in Figures 4 through Figure 28 are given in Table C-1. Also included are points that fall below the lowest value of the logarithmic y-axis, corresponding to the lowest LET point (indicated by an arrow in the figures). The accuracy of energy values is ±5%. The accuracy of LET values may be wider, because LET is a value not yet precisely established by outside researchers, especially for higher Z ions.

Some people (including those at JPL) have noted that the cosine rule for calculation of the effective LET may not always apply very accurately, especially at higher incident beam angles. It is expected that the data of Appendix C will accommodate those objections. It is worth noting that in constructing Figures 4 through 28, some ion/energy/angle points have occasionally been omitted for various reasons. Some of these omitted points did in fact represent inconsistencies that may have come about from a violation of the cosine rule.

Table C-1. Beam Parameters for Figures 4 through 28*

Figure	LET (MeV/mg/cm^2)	(Energy) Ion	Angle	Test Date
4	2.8	67 MeV N	0	June 1986
	5.4	82 MeV Ne	0	June 1986
	14	160 MeV Ar	0	June 1986
	37	241 MeV Kr	0	June 1986
5	6	24 MeV O	0	June 1983
	37	165 MeV Kr	0	June 1983
	74	165 MeV Kr	60	June 1983
6,7,8	3.1	58 MeV N	0	Aug. 1986
	5.7	85 MeV Ne	0	Aug. 1986
	14	174 MeV Ar	0	Aug. 1986
	37	245 MeV Kr	0	Aug. 1986
9	2.6	118 MeV O	0	Aug. 1985
	5.2	118 MeV O	60	Aug. 1985
	5.5	36 MeV O	0	May and Oct. 1985
	7.8	118 MeV O	70	Aug. 1985
	11	36 MeV O	60	May 1985
	18	88 MeV Ar	0	May and Oct. 1985
	37	~300 MeV Kr	0	Aug. and Oct. 1985

*Figures 24 through 27 are data for the CRRES satellite program, only recently approved for publication from the JPL SPACERAD data bank. For this special part category, we have drawn from all data available even though it was obtained after the August 1986 cutoff date established for all other parts data.

Table C-1. Beam Parameters for Figures 4 through 28 (continued)

Figure	LET (MeV/mg/cm^2)	(Energy) Ion	Angle	Test Date
10	18	88 MeV Ar	0	Oct. 1985
	37	~300 MeV Kr	0	Oct. 1985
	74	~300 MeV Kr	60	Oct. 1985
11	6.0	24 MeV O	0	June 1983
	8.5	24 MeV O	0	June 1983
	37	165 MeV Kr	0	June 1983
	74	165 MeV Kr	60	June 1983
12	6.0	24 MeV O	0	June 1983
	37	165 MeV Kr	0	June 1983
	43	165 MeV Kr	30	June 1983
	53	165 MeV Kr	45	June 1983
13	2.6	130 MeV O	0	June 1985
	4.9	110 MeV Ne	0	June 1985
	10.2	400 MeV Ar	0	June 1985
	15.7	160 MeV Ar	0	June 1985
	37	330 MeV Kr	0	June 1985
14	3.8	20 MeV C	0	April 1986
	7.6	20 MeV C	60	April 1986
	16.5	75 MeV Cl	0	April 1986
	28	100 MeV Fe	0	April 1986
15	3.3	27 MeV C	0	Oct. 1982
	7.2	49 MeV Ne	0	March 1983
	16.5	93 MeV Ar	0	March 1983
	37	165 MeV Kr	0	June 1983
	52	130 MeV Kr	45	Sept. 1981
16	3.3	27 MeV C	0	Oct. 1982
	7.2	49 MeV Ne	0	March 1983
	16.5	93 MeV Ar	0	March 1983
	33	93 MeV Ar	60	March 1983
17	2.9	108 MeV O	0	March 1983
	7.2	49 MeV Ne	0	March 1983
	16.5	93 MeV Ar	0	March 1983

Table C-1. Beam Parameters for Figures 4 through 28 (continued)

Figure	LET (MeV/mg/cm^2)	(Energy) Ion	Angle	Test Date
18	3.0	108 MeV O	15	March 1983
	3.1	108 MeV O	20	March 1983
	3.2	108 MeV O	25	March 1983
	3.4	108 MeV O	30	March 1983
	4.1	108 MeV O	45	March 1983
	5.8	108 MeV O	60	March 1983
	7.2	49 MeV Ne	0	March 1983
	14	49 MeV Ne	60	March 1983
	37	171 MeV Kr	0	May 1984
19	2.9	108 MeV O	0	March 1983
	7.2	49 MeV Ne	0	March 1983
	9.4	49 MeV Ne	40	March 1983
	16.5	93 MeV Ar	0	March 1983
	37	167 MeV Kr	0	Nov. 1984
20	12	28 MeV O	60	Jan. 1984
	15	162 MeV Ar	0	Jan. 1984
	30	162 MeV Ar	60	Jan. 1984
	37	132 MeV Kr	0	Jan. 1984
21	5.1	38 MeV O	0	Mar. 1982
	5.5	109 MeV O	60	April 1982
	6.2	38 MeV O	35	Mar. 1982
	7.2	38 MeV O	45	Mar. 1982
	37	130 MeV Kr	0	April 1982
22	11.6	28 MeV O	60	Jan. 1984
	15	162 MeV Ar	0	Jan. 1984
	17	162 MeV Ar	30	Jan. 1984
	37	132 MeV Kr	0	Jan. 1984
	49	132 MeV Kr	40	Jan. 1984
	58	132 MeV Kr	50	Jan. 1984
	65	132 MeV Kr	55	Jan. 1984
	74	132 MeV Kr	60	Jan. 1984
23	10	38 MeV O	60	March 1982
	12	212 MeV Ar	0	April 1982
	14	212 MeV Ar	30	April 1982
	17	212 MeV Kr	45	April 1982
	24	212 MeV Kr	60	April 1982
24	6.5	40 MeV O	40	Dec. 1986
	7.8	40 MeV O	50	Dec. 1986
	15	82 MeV Cl	0	Dec. 1986
	39	170 MeV Br	0	Dec. 1986

Table C-1. Beam Parameters for Figures 4 through 28 (continued)

Figure	LET (MeV/mg/cm^2)	(Energy) Ion	Angle	Test Date
25	30	82 MeV Cl	60	Dec. 1986
	39	170 MeV Br	0	Dec. 1986
	45	82 MeV Cl	70	Dec. 1986
	78	170 MeV Br	60	Dec. 1986
26	1.1	76 MeV B	0	June 1987
	3	58 MeV N	0	Aug. 1986
	6	85 MeV Ne	0	Aug. 1986
	13	174 MeV Ar	0	Aug. 1986
	37	245 MeV Kr	0	Aug. 1986
27	1.1	76 MeV B	0	June 1987
	2.2	76 MeV B	60	June 1987
	6	49 MeV F	0	June 1987
	8.5	49 MeV F	45	June 1987
	12	49 MeV F	60	June 1987
	15	105 MeV Cl	0	June 1987
	39	160 MeV Br	0	June 1987
	78	160 MeV Br	60	June 1987
28	17	87 MeV Ar	0	March 1986
	35	297 MeV Kr	0	March 1986

APPENDIX D

GLOSSARY OF TERMS

ALS--Advanced LS technology.

BNL--Brookhaven National Laboratory.

CIT--California Institute of Technology.

CMOS--Complementary MOS.

Cross-Section--(Number of upsets)/(projected fluence).

CRRES--Combined Release and Radiation Effects Satellite. This is a scheduled satellite designed to measure the effects of heavy ion radiation and other radiation on semiconductor devices. Flight data will be compared with the ground test data referred to in this report.

DRAM--Dynamic RAM.

DUT--Device under test.

EAROM--Electrically alterable ROM.

FET--Field effect transistor.

Fluence--Ions/cm^2 or integrated flux.

Flux--Flux is the number of ions passing through a one-cm^2 area perpendicular to the beam per second, measured as ions/cm^2/sec.

Geosynchronous Orbit--A satellite orbit located at the height of 22,000 miles, where the full spectrum of cosmic ray heavy ions is present.

Hard Device--An SEP-immune device.

Latchup--Latchup is an abnormal low-impedance, high-current-density state induced in an integrated circuit that embodies a parasitic p-n-p-n structure operating as a silicon controlled rectifier.

LET--Linear energy transfer. This is the density of ionization deposited along an ion track, usually measured in units of energy/density-length or MeV/(mg/cm^2). "Effective LET" refers to a calculated value of LET when the ion impinges on the device at an angle ϕ measured from the normal. LET (eff.) = LET (ion)/cosϕ. See the definition of "threshold LET" on page x.

LS--Low-power Schottky technology.

LTTL--Low-power TTL technology.

Maverick--A maverick device is one that displays a radiation response far different from that of its peers.

MNOS--A metal-nitride-oxide-semiconductor device.

MOS--A metal-oxide-semiconductor device.

NMOS--An N-channel MOS device.

PMOS--A P-channel MOS device.

PMT--A photomultiplier tube.

PROM--Programmable ROM.

RAM--Random access memory.

ROM--Read-only memory.

SBD--Silicon barrier detector.

SEP--Single event phenomena. This is the class of all radiation effects induced by the passage of a single ion through a device.

SEU--Single event upset. This subset of SEP refers to an ion-induced change of state of a bistable element. This state is "soft" if it operates correctly upon being rewritten; it is "hard" if the fault or upset is permanent.

Soft Device--An SEP-susceptible device.

SOS--Silicon-on-sapphire technology.

SRAM--Static RAM.

TTL--Transistor-transistor logic.

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15. Supplementary Notes

16. Abstract

This document is the first presenting the accumulation of JPL data on single event phenomena (SEP), from 1979 to August 1986, in full report format. It is expected that every two years a supplement report will be issued for the follow-on period. This data for 135 devices expands on the abbreviated test data presented as part of Refs. (1) and (3) by including figures of single event upset (SEU) cross sections as a function of beam linear energy transfer (LET) when available. It also includes some of the data complied in the JPL computer in RADATA* and the SPACERAD data bank.**

This volume encompasses bipolar and MOS (CMOS and MNOS) device data as two broad categories for both upsets (bit-flips) and latchup. It also includes comments on less well known phenomena, such as transient upsets and permanent damage modes.

*RADATA is a continually updated record of all recent JPL data except for CRRES data. The reader can obtain more recent data there that is not included in this report.

**The SPACERAD data bank contains JPL's completed data set for the CRRES satellite program. All of that data is given herein except for data on GaAs devices, which are deemed proprietary.

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