STATUS REPORT FOR NAG-5-929
EFFECTS OF COSMIC RAYS ON SINGLE EVENT UPSETS

SUBMITTED TO

National Aeronautics and Space Administration, Goddard Space Flight Center
Greenbelt, MD 20771

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February 1989

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I. Introduction

Hampton University is currently in its second annual contract studying "The Effect of Cosmic Rays and Single Event Upsets" (NAG-5-929). At this point in time (half way through the second annual contract - January 1989) it is fitting to state the major goals of this work:

First is the assistance of Drs. Stassinopoulos and Van Gunten in the Brookhaven SEU Test Facility. Our research assistant professor, Vladimir Zajic and research technician, Christopher Humphry, have spent many long days and nights at the Brookhaven Facility. We are proud of their accomplishments. Recently, Chris Humphry has resigned to become Head of the Keystron Maintenance section at CEBAF. While we will miss Chris' work both at Brookhaven and at Hampton, we are happy for his professional development. Considering the level of the work at Brookhaven, we hope to replace Chris with a M.S. level research assistant.

Our second goal is the development of our own SEU Test program at Brookhaven. We chose for our initial test the SEU evaluation of a 16 K 2 micrometer Design Rule Static RAM process by the RAD Modified CMOS 1 micrometer AT&T Bell Laboratory process. An abstract and summary of this work has been submitted to the IEEE Nuclear Society for their July 1989 Conference. (See Appendix I).

The third area of our work concerns the fundamental study of interface states and Oxides Traps as they affect Parametric Degradation under Total Dose Irradiation. It is reasonable to believe that such Total Dose and Dose Rate effects

may adversely affect the SEU rate. Our initial capability consisted of that of making CV curves and Bias Temperature Aging. Since then, we have developed a computer controlled Charge Pumping facility for the evaluation of the density of Interface States as a function of energy. We have also studied the Sub-threshold method and have found errors in the transportation of earlier work formulas to later work. Currently we are adding Computer controlled Terman Analysis to our CV capability. Finally, we are investigating IV methods utilizing the HP-4192A LF Impedance Analyzer used in our CV work and the DLTS method. We also have on hand an HP-4145B Semiconductor Parametric Analyzer which we have used in Threshold Voltage and Transconductance measurements of MOS devices in fill factor measurements of Photovoltaic devices. We have ordered a RAPID System as a PC Controlled Data Generator-Data Analyzer. Bell Labs has given us through the College Gift Program, a Scanning Electron Microscope (SEM) with Energy Dispersive Analysis.

Fourth, we are developing our computer-aided design and modeling by adding to our existing PSPICE capability (circuit analysis), ICED, a mask-level Layout Generator compatible with Reading, PA Bell Labs Mask Facilities and PREDICT (a process simulator). Bell Labs has loaned us a VAX 11-785 for this purpose. Finally we are developing Vacuum Deposition, Diffusion Furnaces, Oxidation and Annealing Furnaces and Plasma Etching equipment so that we are capable of duplicating wafer fabrication processes in-house at the 3 micrometer or greater Design Rule. We have no intention of becoming a Silicon foundry but would like the flexibility of controlling experimentally critical process steps in-house. Most of our Wafer Fab work would be accomplished using the Bell Labs shuttle (a method of running a few wafers of our specific design through a normal

Bell Labs process with perhaps one or two experimental steps in our facility).

Our most important goal is in fulfilling the need for human resource development. As stated in our 1988-89 contract, there should be a long term plan to establish an institute for the training of Minority Scientists and Engineers at Hampton University in the area of Space Radiation Effects on Materials, Devices and Systems.

In the course of this work, four graduate students and seven undergraduate students have worked on the Project. Under a separate contract, NAG-9-333, Hampton university, through its subcontractor MD SSC-ESD with T. N. Fogarty as common advisor, we will serve as an integrator of a Consortium including North Carolina A&T, Prairie View A&M, and Texas A&I for Space Radiation Effect Studies.

Each of the five goals are addressed individually in following sections. The format of the individual reports is such that first, the work accomplished to date in the first two years of NAG-5-929 is reviewed. Then projections of work for the third year is summarized. For example, our work to date centered on MOS devices and CMOS Static RAMs. We intend to expand this work to include CCD devices, Higher Density Static RAMs, Gallium Arsenide Static RAMs and Solar Cells.

II. Support SEFG at Brookhaven SEUTF

Under the NASA contract "Effects of Cosmic Rays on Single Event Upsets" (NAG-5-929) we have provided continuous technical assistance to the Single Event Facility Group (SEFG) at the Single Event Upset Test FAcility (SEUTF) at the Brookhaven National Laboratory. The Hampton University maintenance crew, Dr. V. Zajic and C. Humphry, was dispatched to the BNL 10 times in the past half year (since July 1988). This arrangement proved to be very useful in assisting the users of the facility, performing necessary repairs of the end station, and even upgrading the facility. The accomplishments include the beam energy monitoring, LET calculation, and experimental set-up for LET measurement. These are described below in more details.

A fully automated system was developed to monitor the energy of heavy ion beams from the Twin Tandem Van de Graaff Accelerator. The beam energy is measured by Si surface-barrier detectors with 60 or 300 μm nominal depletion depths. Data collection and processing are controlled by a computer, including detector shutters, main amplifiers, and a multichannel analyzer. However, for highly ionizing particles the detector response is not proportional to the beam energy because of the pulse-height defect caused by the nuclear stopping and electron-hole recombination in the detector[1]:

$$\text{Peak Channel} = G/G_0 * C * (\text{Energy-P.H.D.}) \qquad (1)$$

where G is the main amplifier gain and C [channel/MeV] the system calibration constant at a fixed reference gain G_0. Based on the heavy ion and energy information from the accelerator, the pulse-height defect is estimated using a

semiempirical formula suggested by Ogihara et al.[2]:

$$P.H.D. = \Delta_1 + \Delta_2$$

$$\Delta_1 = 2.33X10^{-4} \ (ZA)6/5 \ (E/A)^{1/2} \qquad (2)$$

$$\Delta_2 = \Delta_1 \ * \ 1.32X10^3 \ Z \ (LET/E^2)^{1/3}/(\rho^{1/4} \ F)$$

where Z and A are the incident ion atomic and mass numbers, respectively, E [MeV] is the beam energy, LET [MeV cm^2/mg] the stopping power in Si, ρ [Ω cm] the detector resistivity, and F [V/cm] the average electric field intensity along the incident ion track in the detector depletion layer. Knowing the system calibration constant from previous measurements, the main amplifier gain is adjusted so that the peak is expected at the center of the multichannel analyzer screen. Following the data collection and automatic peak search, the peak channel is normalized to the reference gain and the beam energy is calculated from Eq. (1) by an iteration method. A calibration curve for the Si surface-barrier detector with 60 μm depletion depth is shown in Fig. 1. The data were obtained using the heavy ion beams ranging from ^{12}C, 40 MeV to ^{197} Au, 330 MeV. Since the channel offset is statistically insignificant, a direct proportionally was assumed:

$$\text{Peak Channel} = 2.178(5) \ x \ (\text{Energy} - \text{P.H.D.}). \qquad (3)$$

The above fit makes it possible to determine the beam energy with an uncertainty of 1.2% at the 95% confidence level. In order to remove the remaining dependence on the energy information from the accelerator, the Si surface-barrier detectors have been calibrated by a ^{241}Au source emitting alpha particles with energy 5.48 MeV. A broad peak is measured due to the self-absorption in the sealed radioactive source. The calibration constant is obtained

by fitting a gaussian to the high energy edge of the peak. (See Fig. 2.) By making a correction for main amplifier non-linearity, it is possible to determine the beam energy with an uncertainty of 0.6% at the same confidence level.

The SEU Test Facility operating software was upgraded by the calculation of LET and range for heavy ions in Si and GaAs, which can be overridden by user defined values. The calculation of LET as a sum of the electronic and nuclear stopping S_e and S_n, respectively, is based on the tables of Ziegler[3]:

$$LET = S_e + S_n. \qquad (4)$$

The electron stopping for the heavy ions is obtained from that for protons by scaling the heavy ion energy to E/A and multiplying by the square of the effective charge ratio:

$$S_{eHI}(E) = S_{eP}(E/A)\left(\frac{Z^*_{HI}}{Z^*_P}\right)^2 \qquad (5)$$

Results of the calculations are compared to the tables of Ziegler[3] and Stassinopoulos[4] in Table 1. The range is approximated by the total path length:

$$R = \int_0^E \frac{dE}{LET} \qquad (6)$$

The integral is computed by fitting LET^{-1} by the 3rd order natural spline. Since the total path length is longer than the range, this calculation calls for an improvement.

The possibility of LET measurement was also investigated. A preliminary experiment was done using the Si surface-barrier detector with two apertures, one covered by a thin 0.67 mg/cm^2 Al foil, and measuring the difference of two peaks. The measured LET for ^{58}Ni, ^{81}Br, ^{127}I, and ^{197}Au was in reasonable agreement with Ziegler's tables and will be published when a representative set of data is collected. The uncertainty of the method was estimated to less than 5% as long as the energy loss in the foil is kept within 10-20% of the beam energy. Four detectors each with a different foil thickness are available to cover the LET range for heavy ion beams employed in SEU experiments. Since the detectors are used one at a time, an additional relay controller operating the four detector shutters independently was constructed to avoid unnecessary radiation damage of the detectors. (See Fig. 3.) It is hoped that this method will provide inexpensive LET data for heavy ions in an energy region where no experimental data exists at all.

III. SSRL SEU TEST of SRAM

We have a project to test SEU susceptibility of CMOS SRAMs degraded by various total dose exposures and dose rates of X-rays and proton radiation, and compare these to the virgin SRAMs. It is expected that the parametric degradation, including threshold voltage shifts, mobility degradation, and rebound phenomena may significantly increase the SEU rate[5,6]. The parametric degradation can be measured using simple test chips with few PMOS and NMOS transistors, capacitors, and polysilicon resistors. As long as the SRAMs and test chips are fabricated by the same technology and irradiated under the same conditions, the parametric degradation is expected to be identical. We assume the principal causes of parametric degradation are filling of the charge traps in the SiO_2 layer, and increase in the density of energy levels in the forbidden band gap at the Si-SiO_2 interface. So far we have completed two steps of this project:

1. Measurement of the SEU cross-section for virgin SRAMs, and
2. Measurement of the threshold voltages and interface state densities on the test chips prior to the irradiation.

A memory cell of the CMOS SRAM (see Fig. 30) is capable of storing logical 0 or 1. When a heavy ion cosmic ray hits the drain of the OFF transistor, the collected charge will change the gate voltage on the other invertor. As a result, the ON transistor is turned OFF. The memory cell assumes a stable state opposite to the original causing a Single Event Upset (SEU).

The collected charge can be calculated by evaluating the following integral[7,8]

$$Q_{COLL} = q \int_0^{L_{COLL}} \rho \frac{LET}{\varepsilon_i} dx \qquad (7)$$

where $q = 1.6X10^{-19}$ C is the electron charge,

$\rho = 2.32$ g/cm^3 is the density of Si,

LET [MeV cm^2/g] is a linear energy transfer for the incident ion in Si,

$\varepsilon_i = 3.6$ eV is the average electron-hole pair formation energy in Si, and

L_{COLL} is a collection length given by $L_{COLL} = K W_D/\cos\theta$, where W_D is the depletion depth, θ the particle angle of arrival, and K is a constant (3.7 and 2.0 for NMOS and PMOS respectively) accounting for funneling effects. For the twin-tub technology the expression can be replaced by $L_{COLL} = (W_D + W_{EPI})/\cos\theta$ where W_{EPI} is the epitaxial thickness.

If the energy loss in the collection length is small compared to the incident ion energy, the LET is approximately constant and the collected charge becomes proportional to the effective LET, which is related to the normal LET through the particle angle of arrival

$$LET_{eff} = LET/\cos\theta \qquad (8)$$

The presented experimental data for SEU cross-sections were measured on TA670 CMOS 16 K SRAMs fabricated by the AT&T Bell Labs CMOS 1 μm Twin-Tub IV technology using 2 μm design rules[9]. Important processing and design variables are listed later in this report (see Chapter V, page 27). Polysilicon decoupling resistors were inserted in the invertor pair cross coupling lines of an existing memory cell designed to improve the SEU immunity by reducing the gate

voltage charge on the now-struck invertor (see Fig. 33). Four memory chips with the decoupling resistor values 82, 109, 151, and 240 kΩ, respectively, were available for the experiment.

The experimental setup for the measurement of SEU cross section is pictured in Fig. 5. HP-8180A/8181A 32 channel Data Generator/Extender offer programmable digital patterns for the simulation of digital circuits and HP-8182A 16 channel Data Analyzer provides capabilities for data capture and comparison and for level timing measurement for the analysis of digital circuits response. An HP-15425A Test Head allows connection and switching with relays up to 84 DUT pins. The SRAM under test was loaded with one of the three memory patterns (all zeros, checkerboard, or all units) and submitted to a heavy ion beam until the desired fluence was accumulated. The number of SEUs was obtained by comparison of the initial and final memory patterns. The SEU cross-section simply equals

$$\sigma_{SEU}[cm^2] = (\text{Number of SEU})/(\text{Incident Ion Fluence } [cm^{-2}]).$$

However, the observed number of SEU is smaller than the actual number of SEUs due to the possibility of multiple upsets of the same memory cell. Depending on the parity, the multiple upsets either escape observation or are recorded as one SEU. The following correction was applied to the experimental data to account for multiple upsets:

$$N_{SEU}\ \text{observed} = N_{SEU}\left[1 - \frac{N_{SEU}}{16\ K} + \left(\frac{N_{SEU}}{16\ K}\right)^2 + \ldots\right]$$
$$= \frac{N_{SEU}}{\left(1 + \frac{N_{SEU}}{16\ K}\right)} \qquad (9)$$

To keep both this correction and statistical uncertainty small, it is a good practice to choose a fluence resulting in approximately 10% of upsets. Since we observed a few memory errors even with no radiation present at all, the power supply voltage of the SRAM was increased from 5 to 5.25 V, which was still less than the maximum 5.5 V for the technology. Unfortunately the voltage drop in our test fixture, if any, was not recorded.

The measurement was made at the Brookhaven SEUTF using the Twin Tandem Van de Graaff Heavy Ion Accelerator. Two heavy ion beams were employed in the experiment.

Ion	Energy [MeV]	LET [MeV cm^2/mg]
^{81}Br	260	37.85
^{197}Au	325	80.95

The effective LET was varied by changing the particle angle of arrival from 0° to a maximum of 73°. The 16 K SRAMs were addressed 1K element at a time. Data from half of the elements were eliminated for angles greater than 60° because of the package well shadowing. The accumulated fluence was 9 X 10^6 and 9 X 10^5 ions/cm^2 for the bromine and gold ion beams, respectively.

Experimental data indicate that no upsets were observed at the room temperature (T = 27° C) for any of the tested SRAMs, e. g. for any value of the decoupling resistors up to the highest effective LET of 162 MeV cm^2/mg using 325 MeV ^{197} Au ions. This result is contrary to the data reported in Refs. 9 and 10. These authors found threshold effective LET of 80 and 60 MeV cm^2/mg for the power supply voltages of 5 and 4.5 V, respectively for SEU cross sections at room temperature for TA670 CMOS SRAMs with 100 KΩ decoupling resistors. Their data were probably obtained at the Lawrence Berkeley Laboratory cyclotron using 370 MeV Kr ions. The only factor which could account for such a difference is the higher power supply voltage 5.25 V used in our experiment.

The polysilicon decoupling resistor values are temperature dependent and will decrease with increasing temperature. A higher SEU susceptibility of the SRAMs is therefore expected at elevated temperatures.[11] The memory chips were heated to 90, 110, and 125° C by 50 Ω resistors attached to the bottom side and the temperature was monitored by measuring the resistance of YSI 44006 Thermistors attached to the top side of the chip package. Using a manual control, the temperature was maintained with the stability of ±5° C. A better stability should be achieved with an automatic control using the Metrobyte Relay Output Board model ERB-24.

Experimental SEU cross-sections measured at elevated temperatures using 260 MeV ^{81}Br ions for the SRAMs with 82, 109, and 151 kΩ decoupling resistors are shown in Figs. 6, 7, and 8, respectively. No upsets were observed even at elevated temperature for the SRAM with 240 kΩ decoupling resistors using the bromine ion beam. Results obtained at elevated temperatures using

325 MeV ^{197}Au ions for the SRAMs with 82 and 240 kΩ resistors are shown in Figs. 9 and 10, respectively. In all cases it was confirmed that the threshold effective LET, which is proportional to the critical collected charge causing upsets, decreases with increasing temperature.

Fig. 11 compares the SEU cross-section measured at elevated temperatures using 260 MeV ^{81}Br and 325 MeV ^{197}Au ions for the SRAM with 82 kΩ decoupling resistors. Probable explanation for the shift in the threshold effective LET obtained with these two ion beams is an energy loss in a passivation layer. As a result, the effective LET in the sensitive region may be substantially lower for the ^{197}Au ion while it would not change much for the ^{81}Br ion (see Fig. 12). On the other hand, the difference in the saturated SEU cross section is probably due to the fact that the accumulated fluence for ^{81}Br ions was too high and the number of upsets (up to 38%) substantially exceeded the recommended 10%. A correction described earlier in this report (Eq. (9), page 11) was applied, but was it evidently insufficient. Thus we conclude that the threshold effective LET obtained with the bromine and the saturated SEU cross sections obtained with the gold ion beam are well founded.

Fig. 13 compares the SEU cross sections measured at a temperature of 110° C using 260 MeV ^{81}Br ions for the SRAMS with various decoupling resistors. No statistically significant differences were observed for the decoupling resistors of 82 and 109 kΩ. However the SEU immunity dramatically improves for higher values, 151 and 240 kΩ. In fact, no upsets were observed under the above conditions for the decoupling resistors of 240 kΩ.

Although no dependence of the SEU cross section on the initial memory

pattern is expected for virgin SRAMs, the opposite is true for SRAMs degraded by a total dose exposure of X- or gamma- rays. The degraded SRAMs were reported to prefer the state in which they were irradiated[6]. Fig. 13 shows that no statistical difference for various initial memory patterns (all zeros, checkerboard, or all units) was observed for any of the tested SRAMs prior to the irradiation.

IV. Fundamental of Device & Material Defects Total Dose & Dose Rate Effect on Parameters

In order to judge parametric degradation of the test chips fabricated by the same technology as the SRAMs, we have been working on three independent methods for the measurement of the interface state density: (1) charge-pumping and (2) subthreshold slope techniques for MOS transistors, and (3) CV-methods for MOS capacitors. Menu driven programs in GW-BASIC were completed for the three methods to convert them into routine procedures. The experimental equipment (HP-8112A 50 MHz Pulse Generator and KEITHLEY 617 Programable Electrometer for the charge-pumping, HP-4145B Semiconductor Parametric Analyzer for the threshold voltage and subthreshold slope, and HP 4192A LF Impedance Analyzer for the CV-measurements) is computer controlled over the IEEE-488 Metrabyte Interface Board. The individual methods and results obtained for the test chips prior to the irradiation by x-ray or protons are briefly described below.

A reliable approach to the charge-pumping technique was developed in Ref. 13 and 14. The basic experimental setup is pictured in Fig. 14. The source and drain of a MOS transistor are connected and grounded (or reverse biased). The substrate is also grounded and the transistor is pulsed from inversion to accumulation and back by a gate voltage waveform. For further explanation we suppose an N-channel MOS transistor (NMOS). When the transistor is pulsed into inversion, electrons flow from the source and drain into the channel and some are captured by interface traps in the upper half of the band gap. When the transistor is pulsed back to accumulation, the mobile electrons drift back to the source and drain, but the trapped electrons recombine with majority holes

coming back from the substrate. The result is a net current into the substrate. A similar argument holds for holes captured in accumulation by interface traps in the lower half of the band gap and recombining with channel electrons when the transistor is pulsed into inversion. They also contribute to the charge-pumping current into the substrate. The charge recombining per cycle equals

$$Q_{it} = \frac{I_{cp}}{f} = q\, A_G \int_{E_L}^{E_U} D_{it}(E)dE \qquad (10)$$

where I_{cp} is the charge pumping current,

f is the waveform frequency,

g is the electron charge

A_G is the gate area

D_{it} [#/cm^2/eV] is the interface state density, and

E_L, E_U are energy levels in the lower and upper halves of the band gap, respectively.

Suppose a very short fall-time when pulsing the transistor from inversion to accumulation. Then no electrons have time to be released from the traps, all recombine and contribute to the charge-pumping current. On the other hand, if the fall-time is long, only the electrons in deep traps close to the center of the band gap do not escape. Clearly, there is a relationship between the fall-time and energy level of the electron traps in the upper half of the band gap and similarly, a relationship between the rise-time and energy level of the hole traps in the

lower half of the band gap:

$$E_L - E_i = kT \ln\left(v_{th}\,\sigma_h\,n_i\left|\frac{V_{TH} - V_{FB}}{\Delta V_G}\right|t_R\right)$$

$$E_U - E_i = -kT \ln\left(v_{th}\,\sigma_e\,n_i\left|\frac{V_{TH} - V_{FB}}{\Delta V_G}\right|t_F\right) \qquad (11)$$

where E_i is the middle-gap energy level,

k is the Boltzman constant,

T is the absolute temperature,

v_{th} is the thermal carrier velocity

σ_n, σ_e are the hole and electron capture cross-section, respectively,

n_i is the intrinsic carrier density,

V_{TH} is the threshold voltage,

V_{FB} is the flatband voltage,

ΔV_G is the gate-voltage sweep, and

t_R, t_F are the rise- and fall-times, respectively.

If we use a square waveform, e.g. if we keep both the rise- and fall-times constant, the charge-pumping current is proportional to the frequency (see Figs. 15, 16). This may serve as a proof of measuring the charge-pumping current and not a leakage current. If a sawtooth waveform is applied, e. g. if both the rise- and fall-times are equal to 50% of the waveform period, the energy sweep in the band gap can be calculated as a linear function of the logarithm of frequency.

Replacing the integral by the average interface state density we have

$$Q_{it} = \frac{I_{cp}}{f} = q\, A_G\, \overline{D}_{it}\, \Delta E \qquad (12)$$

Consequently (see Figs. 17, 18), the slope of Q_{it} as a function of the logarithm of frequency is proportional to the average $\overline{D}_{it}$:

$$\frac{dQ_{it}}{d(\ln f)} = 2kT\, q\, A_G\, \overline{D}_{it} \qquad (13)$$

and the extrapolated frequency to the zero interface state charge $Q_{it} = 0$ is proportional to the geometrical mean of the electron and hole capture cross-sections:

$$f_o = 2v_{th}\, \sqrt{\sigma_e \sigma_h}\, n_i \left| \frac{V_{TH}-V_{FB}}{\Delta V_G} \right| \qquad (14)$$

It is reasonable to suppose that the electron and hole capture cross-sections are approximately equal, at least around the middle-gap energy. If we keep the rise-time constant and vary the fall-time, we can monitor the energy distribution of the electron traps over the upper half of the band gap. Inversely, if we keep the fall-time constant and vary the rise-time, we can monitor the energy distribution of the hole traps over the lower half of the band gap (see Figs. 19, 20). The measurements of the interface state densities by the charge-pumping technique provided reasonable results which are summarized in the table below.

			D_{it} [#/cm^2/eV]	
transistor	W(μm)	L(μm)	lower half	upper half
PMOS	50	2	3.3 x 10^{10}	2.1 x 10^{10}
NMOS	50	2	3.1 x 10^{10}	5.3 x 10^{10}

W,L are the channel width and length, respectively.

The subthreshold slope technique was proposed almost 20 years ago in Ref. 14. It is based on the change in the drain current versus gate voltage characteristics of a MOS transistor operating in weak inversion e. g. below the threshold voltage. The weak inversion drain current for a long channel transistor (L > 20 nm) is given by

$$I_D = \text{const} \times \exp\left(\frac{q}{nkT}\left|V_G - V_G^*\right|\right)\left[1-\exp\left(\frac{mq}{nkT}\left|V_D\right|\right)\right] \qquad (15)$$

where V_G, V_D are the gate and drain voltages, respectively,

V_G^* is a gate voltage in the middle of weak inversion,

$$n = \frac{C_{ox} + C_D + q\,\overline{D}_{it}}{C_{ox}}, \quad m = \frac{C_{ox} + C_D}{C_{ox}}$$

C_{ox}, C_D are the oxide and depletion capacitances per unit area which can be calculated from the oxide thickness and surface doping density, respectively.

The weak inversion gate voltage V_G^* can be calculated using these capacitances and knowing either the threshold or flatband voltage. The subthreshold slope

$$\frac{d(\ln I_D)}{d V_G} = \frac{q}{nkT} \qquad (16)$$

is constant which makes it possible to calculate the parameter n and the interface state density. Unlike the charge-pumping technique, the subthreshold slope methods provides the average density of interface states only around the weak inversion surface potential

$$\phi_s = \frac{3}{2}\phi_F = \pm kT \ln \frac{N_D}{n_i} \qquad (17)$$

where ϕ_F is the Fermi potential and N_D is the doping density, e.g., in the upper half of the band gap for an NMOS transistor and in the lower half of the band gap for a PMOS one. The subthreshold slope technique was criticized in Refs. 15, 16 and 17 as unreliable because of fluctuations in the fixed oxide charge which results in overestimating the interface state density. Recently, the method has been revived in Refs. 18 and 19 and a good agreement was reported between the charge-pumping, subthreshold slope, and CV measurements. (See also Refs. 20 and 21.) However, the authors made their measurements on transistors with a channel length substantially shorter then 20 μm, used incorrect equations for the subthreshold slope method and did not report uncertainties, which makes their results doubtful. Our experience with the subthreshold method is in

agreement with the older works (Refs. 15, 16, and 17). The measured interface state density was approximately 1.3 x 10^{11} #/cm^2/eV for an NMOS transistor which is too high to be true. (See Fig. 21 for the threshold voltage measurement and Figs. 22,23 for the subthreshold slope measurement.) Moreover, from the basic formula

$$q\,\overline{D}_{it} = \left(\frac{q/kT}{d(\ln I_D)/dV_G} - \frac{C_D}{C_{ox}} - 1 \right) C_{ox} \qquad (18)$$

it follows that the sensitivity of the method is proportional to the oxide capacitance and thus inversely proportional to the oxide thickness. Since an uncertainty of 1 x 10^{10} #/cm^2/eV was reported in Ref. 17 for the oxide thickness 2000 Å, an order of magnitude higher uncertainty is expected for our test chips with the oxide thickness 215 Å.

The capacitive - voltage measurement can be used to determine the density of interface states in an M.O.S. device. This method was first investigated by Terman[22]. This method is historically the classical approach as opposed to more current trends such as charge-pumping and the sub-threshold[12, 14] methods of measuring D_{it}, interface state density, although the sub-threshold method theory emanates from capacitive and conductance measurements and theory.

In the high frequency C-V measurement, the device capacitance is measured as a function of gate bias voltage (Fig. 24). The presence of interface trap capacitance alters the shape of this curve. If the capacitance between the gate and the silicon surface is related as such[24]

$$C_{ox}(V_G - \psi_s) = -Q_{it}(\psi_s) - Q_s(\psi_s) \qquad (19)$$

where . . .

Q_{it} = interface state charges per area

Q_s = silicon surface charge per area

V_G = gate bias

ψ_s = surface potential

C_{ox} = oxide capacitance per area

then

for small infinitesimal changes in gate bias dV_G

$$C_{ox}\frac{dV_G}{d\psi_s} = C_{ox} - \frac{dQ_{it}}{d\psi_s} - \frac{dQ_s}{d\psi_s}$$

$$C_{ox}\,dV_G = [C_{ox} - C_{it}(\psi_s) - C_s(\psi_2)]\,d\psi_s$$

rearranging . . .

$$C_{it}(\psi_s) = C_{ox}\left[\frac{dV_G}{d\psi_s} - 1\right] - C_s(\psi_s) \qquad (20)$$

This is the capacitive relation which will be used to determine the interface state trap density.

The value of $C_s(\psi_s)$ shall be obtained theoretically[23] from

$$C_s(\psi_s) = \sqrt{\frac{q\epsilon_s N_D \beta}{2}} \frac{\exp(\beta\psi_s) - 1}{\left[\exp(\beta\psi_s) - \beta\psi_s - 1\right]^{1/2}} \qquad (21)$$

where . . .

β = q/kt,

ε_s = dielectric constant of Si

N_D = doping density

The value of $dV_G/d\psi_s$ shall be obtained from the mergence of experimental and theoretical data to produce a ψ_s vs V_G curve. This curve is then graphically differentiated and the density of interface states is calculated. The following steps outline this procedure:

1. C-V data is obtained experimentally at a frequency f > 100 kHz (Fig 24),
2. From the experimental data the following properties are determined[24]
   - A. OXIDE THICKNESS Å
   - B. DOPING DENSITY N/cm^3
   - C. FLATBAND VOLTAGE V_{FB}
3. A theoretical C-V curve is calculated without the interface states using equation (21) and

$$C_{HF} = \frac{C_s C_{ox}}{C_s + C_{ox}} \qquad (22)$$

4. From this calculation a determination of C_{HF} a function of ψ_s is found
5. The plot of C_{HF} vs ψ_s and the experimental data C_{HF} vs V_G are used to

prepare a curve ψ_s vs V_G where ψ_s and V_G are found at equivalent points of C_{HF} (Fig 25, 26)

6. $dV_G/d\psi_s$ is determined graphically for each $C_s(\psi_s)$ (Fig 27)

7. Equation 4 is then used to extract the interface-trap capacitance and the relation

$$C_{it}(\psi_s) = q\, D_{it}(\psi_s) \qquad (23)$$

gives the interface-trap densities. (Fig 28)

V. Modeling, CAD, Wafer Processing & Diagnostics

Modeling & CAD

As a part of the Solid State Radiation Lab research team P. M. Kibuule, Duc Ngo, and Alfreda Branch, in consultation with T. N. Fogarty, devoted most of their time on modeling and studying the behavior of SRAM cells once hit by charged particles. At the beginning they were charged with the responsibility of testing the software that was available on the market and select one that would best fit our needs in terms of cost, user friendliness, and adaptability without compromising performance. So far types of software tested and results analyzed are:

a) MICROCAP II: this is graphics oriented software, which makes it easier for the user to visualize what is going on within the SRAM-cell. Nevertheless, its lack of some parameters that are essential to our work, e. g. lateral diffusion and overlap capacitance, prevented us from selecting it as our tool.

b) ALLSPICE: this software met most of our needs. However the program could not simulate at temperatures above 90° C. In addition, we needed software which could, eventually, be used by students. Because we did not have a student version, we decided no to adopt it.

c) PSPICE: at the moment, we have decided to use PSPICE for modeling purposes. It has all the parameters needed in our work. Also, our students can use it because the PSPICE students' version is already

installed on most of our personal computers.

d) Mask software: for laying out the Masks, we hope to use ICED and PREDICT. We feel, both software will adequately address our needs in this area.

In order to harden the SRAM cell against SEU we hope to find a way either to: (a) minimize the amount of charge that can be collected by a sensitive node per event (Q_{COLL}) and/or (b) maximize the critical charge necessary to produce an upset Q_{crit}). So far, effort has been made to identify areas of the SRAM cell most likely to cause upset, once struck by charged particles. Like other investigators[25], it has been found that the depletion region under the drain of the OFF MOS is the most sensitive. Basically a CMOS static RAM is a flip-flop formed from two cross coupled CMOS inverted as shown in Fig. 30. A single, high energy particle can strike the drain diffusion of either the OFF p-channel or n-channel device. Logic upset will occur if enough charge is deposited and collected on the proper nodes in the cell (see Fig. 31).

In this research , PSPICE was used to simulate the TA670 CMOS integrated circuit. The TA670 is a 16 K static RAM organized as 16 by 1 bit, and the memory is fabricated by using 2 μm design rule with a 1 μm twin-tub CMOS process. The list of the important doping profile is:

Channel width/length	
PMOS transistor	4.25/2.0 μm
NMOS transistor	5.0 /2.0 μm
Drain Area	
P-drain	25.5 μm^2
N-drain	50.3 μm^2
Gate Oxide thickness	215 A
N-substrate doping	4×10^{16} cm^{-3}
P-well doping	1.5×10^{17} cm^{-3}
Epitaxial thickness	1.7 μm

The collected charge Q_{COLL} is calculated by evaluating the integral (7) in Chapter III, page 9.

The cosmic ray interaction was simulated by applying a current pulse placed in parallel with the sensitive device junctions. (see Fig. 32) The current pulse amplitude was varied to find the threshold for memory changes. To determine the critical charge, one calculates the time integral of that minimum current that causes the upset,

$$Q_{crit} = \int_0^{\infty} i(t)\, dt \quad . \tag{24}$$

When a charge particle strikes a drain depletion region, it creates

electron-hole pairs which are collected as photon-current that changes the gate voltage of the opposite invertor and tend to destabilize the memory state. The amount of gate voltage change depends on the charge collected (Q_{coll}) at the sensitive node. By inserting a pair of decoupling resistors, one expects to reduce the maximum gate voltage change produced by the charge collected (see Fig. 33). This will increase the minimum critical charge (Q_{crit}) a charged particle must deposit in order to cause an upset. Simulation of the SRAM cell with decoupling resistors has indicated that the effective resistance value decreases with an increase in temperature. This is because polysilicon from which these resistors are made, has a negative temperature gradient. So as to select the right decoupling resistors to harden the SRAM cell without compromising it writing speed, we need to do more investigation on the resistors' dependence on temperature.

The use of D. C. transfer curves to improve design of SRAM cells has been investigated. As a result in Fig. 34 curve 2 gives the most symmetrical digital logic swing and best immunity noise level. Curve 2 is obtained by adjusting the β ratio of the NMOS/PMOS of the invertor.

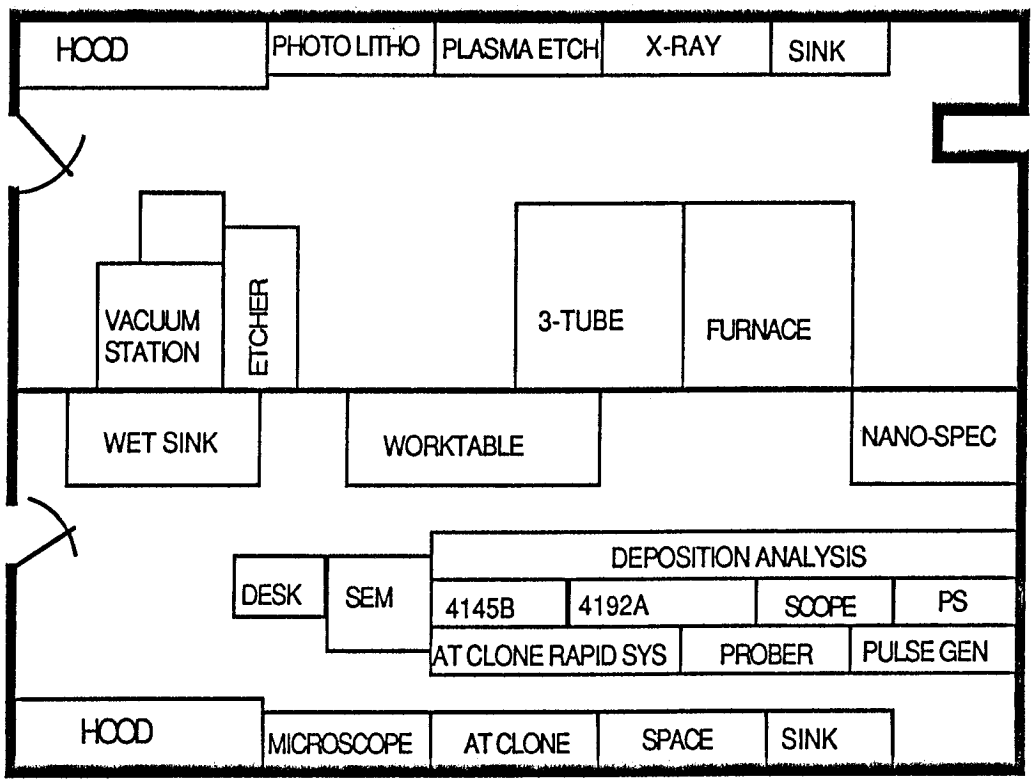
After establishing a way of predicting the minimum amount of charge needed to cause SEU, we plan to embark on searching the effective way of hardening the SRAM.

Wafer Processing and Diagnostics Equipment

As part of the study of single event upset induced by cosmic radiation, a one-step wafer fabrication laboratory is being planned. It is one-step because only the steps needed to test the general theory of the research shall be conducted at this facility. Complete wafers will be supplied to our design specifications by AT&T Bell Laboratory shuttle.

The laboratory shall consist of two rooms; one acting as a "dirty" room while the other serves as the "clean" room. The dirty room will house furnaces,

SOLID STATE RADIATION LAB



plasma etcher, vacuum station, photo lithographer and an x-ray machine. The

clean room will house a nano-spectrometer, scanning electron microscope, prober, pulse generator, parametric analyzer and the various computer instrumentation equipments. Also planned for the laboratory is a plasma assisted liquid phase chemical vapor deposition (LPCVD) unit which is currently under construction. This reactor will form a part of the multi-chamber in-situ deposition and analysis of amorphous silicon system that is also being planned. Other units of the chamber are:

*Quadrupole Mass Spectrometer for residual gas analysis

*Chamber for demoisturization, dry oxide and metalization.

*Surface Analysis Chamber to contain:

..ion sputter gun

..x-ray photoelectron spectroscopy and

..HEED for structure determination

Some of the necessary equipment have been purchased or secured as college gifts and others are yet to be bought. A listing is given below. We desire a HIMEV ion implanter but may obtain as a gift from University of California Santa Barbara, a high voltage incorporated 200 keV single wafer ion implanter. The only cost to us will be for shipping and handling.

PREDICT 1.3 OVERVIEW

PREDICT™ (PRocess Estimator for Design of IC Technologies) is an accurate multilayer process simulator for advanced silicon technologies. The goal in developing the program was to couple physical models together, verify the models and the coupling with a large measured data base, and imbed the calculations in a fast numerical integration scheme. PREDICT 1.3 represents the achievement of this goal. The program is intended for use by silicon process engineers as well as researchers needing to simulate experimental data. The over 500 models in PREDICT 1.3 include verified models similar to those commonly used in other simulators as well as many new models based on extensive, detailed data generated as part of MCNC's submicron CMOS program.

PREDICT 1.3 Features:

- One-dimensional multi-layer simulator
- Fast computation (average cpu time between 5 and 30 seconds with a worst case average of 5 minutes)
- New models, fully verified:
  - RTA and low temperature annealing (550 - 1250° C) - a full set of models
  - RTO, standard oxidation, doping effects (700 - 1250° C)
  - implantation through oxides, nitrides, polysilicon (1 KeV - 2 MeV)
  - Si^+ and Ge^+ pre/post-amorphization effects and epitaxial regrowth
  - activated implant damage removal with spatially dependent diffusion effects includes five specific types of damage
  - nitridation, oxynitridation and associated dopant diffusion effects.
  - TiSi$_2$ and CoSi$_2$ silicide models and dopant redistribution calculations
  - accurate sheet resistance and layer thickness calculations
  - codiffusion models (P/AS, As/B, P/B, etc.) with account for implantation damage effects.
- Full documentation and user's guide
- SUPREM III command file parser - runs SUPREM files
- Masking preprocessor that allows parallel calculations of multiple wafer regions.
- Variable model parameter file
- Interfaces to device simulators
- Line printer or HP plotter output

PREDICT is a trademark of the Microelectronics Center of North Carolina.

SOLID STATE RADIATION LAB DIAGNOSTIC EQUIPMENT

EQUIPMENT	SOURCE	K$ MARKET	K$ REPLACEMENT
HP-4192A Impedance Anal.	Hampton	13	17
HP-4145B Parameter Anal.	NAG5-929	22	23
HP-81124 Pulse Gen. Anal.	NAG5-929	8	8
Keithley 617 Electrometer	NAG5-929	8	8
AT clone PC	NAG5-929	3	3
Assorted Tools	NAG5-929	1	1
X-ray & Detectors	NAG5-929	25	25
Metrabyte GPIB (2)	NAG5-929	2	2
HP-7570A Plotter	NAG5-929-89	3	3
AT clone PC	NAG5-929-89	3	3
RAPID 3030 Gen./Anal.	NAG5-929-89	5	5
	NASA sub-total	98,000.00	
HP-1600A Logic Anal.	Bell Labs College gift	2	3
Laminar Flow Hood	BL College G.	1	2
Lam. Flow Wet Bench	BL 52100 gift	2	4
RF Plasma Etch	BL52100 gift	15	35
Plasma Stripper	BL52100 gift	3	10
Hipox Steam Oxide	BL52100 gift	85	200
SEM+ E Dispersive Anal.	BL52100 gift	99	200
VAX 11-785	BL52100 gift	200	500+
Graphics Stations (4)	BL52100 gift	20	60
Vacuum Dep. EB Sputter	BL52100 loan	15	90
Electro-glas Probe	BL52100 loan	10	25
CV Test fixture	BL52100 loan	1	1
HP-1000	BL52100 loan	2	10

Equipment Desired

Sun Work Station	NAG-5-929-89	20
High E Ion Implant	Major Grant	1000
Oriel Mask Al&Exp.	Consortium	89
In Situ Dep. & Anal.	Consortium 5 year plan	
Laminar Flow (5)	BL	

Upgrade To SEMICLEAN ROOM CLASS 10K or BETTER

VI. Human Resource Development

Space radiation effects on materials, devices and systems is an attractive topic to students of diverse disciplines in Natural Sciences and Engineering. Therefore, the long term goal of establishing an institute at Hampton for the graduate training of minorities is fitting. As a Consortium of Minority Schools has now been established by NASA with Hampton in an integrating role, we expect by an interchange of technical talks to attract more students to graduate work in this area. For example, we expect undergraduate students in consortia school to enroll in Hampton's graduate program to pursue advanced studies in radiation effects in materials.

We are beginning the planning of a NASA-Hampton International Conference on Space Radiation Effects on Materials, Devices and Systems. This conference is now planned for spring 1990. A similar conference was sponsored by NASA at Prairie View, a member of the consortium.

The training of students in the area of radiation effects in materials has continued to be the principal focus of this project. To date four graduate students have had involvement with the project. Cecily Smith worked for one semester under the project and is currently developing a thesis with Dr. Calvin Lowe under another NASA grant on optical properties of Laser materials. Mr. Kurt Kloesel has worked on the grant for four semesters and is now writing a thesis on total dose radiation effects. Daniel Owasu worked on the project for one semester and is currently pursuing a thesis topic in polymer chemistry in the Department of Chemistry. Duc Ngo worked on the project for one year and used his research to serve as a basis for a NASA Graduate Student Training Fellowship proposal on Nuclear Fragmentation and SEU Modeling. This project has been funded through NASA.

Several undergraduate students have also been involved in the project. Faith

Welch performed some of our early SPICE modeling. Alfreda Branch has been involved with our modeling effort. She will present some of our work at the NASA-HBCU Huntsville Conference in March 1989. Eric Edwards has worked with our evaluation of ICED software, and assisted in the development of our vacuum and x-ray systems. Christopher Washington has assisted with the development of wafer fabrication capabilities.

Several other undergraduate students have been involved with the project to a lesser degree in that they have recently joined the team and have not yet completed a principal assignment. These are, M. Masilela, W. Harding, S. Shanck, S. Ridley, and G. Coleman.

It is important to note that 75% of the graduate students and 90% of the undergraduate students involved with the project are American citizens.

VII. Conclusion

The first two years of work under the project have involved the items indicated in the table given below.

SEU Phase I - NAG 5-929

1) Provide assistance to Drs. Stassinopoulos and Van Gunten at the Brookhaven SEU Test Facility. Zajic and Humphry.

2) Develop computer codes for fragmentation and secondary radiation affecting VLSI in space. Zajic, Buck, Wilson, Ngo.

3) Develop computer controlled CV (HP4192) test for Terman analysis. Kloesel and Fogarty.

4) Develop high speed parametric tests which are independent of operator judgement (HP4145). Ngo and Fogarty.

5) Develop charge pumping technique for measurement of $D_{it}(E)$. Kloesel, Zajic, and Fogarty.

6) X-ray simulation secondary effects on D_{it} and D_{ot} and parametric degradation as a function of dose rate. Edwards, Oladipupo, and Lowe.

7) SPICE simulation of static RAMs with various resistor filters. Test at Brookhaven for SEU. Ngo, Welch, Branch, and Mawanda-Kibuule.

Note: Students are underlined

We are proud of our achievements over the past year and a half both at the Brookhaven SEU Facility and at Hampton where we have emphasized the characterization of fundamental device phenomena. We have trained four graduate students, two of whom will complete masters thesis in the area by December 1989 and several undergraduate students, whom we hope will continue on to graduate school. Therefore, we believe we are meeting both the scientific research requirement and the human resource development aspect of the contract NAG-5-929.

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Figures

Ion	Energy [MeV]	LET in Si [MeV cm^2/mg]		
		calculation	Ziegler	Stassinopulos
^{12}C	102	1.4	1.4	1.4
^{19}F	140	3.4	3.4	3.4
^{28}Si	186	7.9	7.9	7.9
^{35}Cl	208	11.5	11.6	11.6
^{59}Ni	265	26.7	26.7	26.8
^{80}Br	285	37.3	37.4	37.5
^{127}I	320	59.7	59.7	60.5
^{197}Au	345	81.9	82	83.0

Tab. 1: Results of the LET calculation for heavy ions in Si compared to the tables of Ziegler and Stassinopulos.

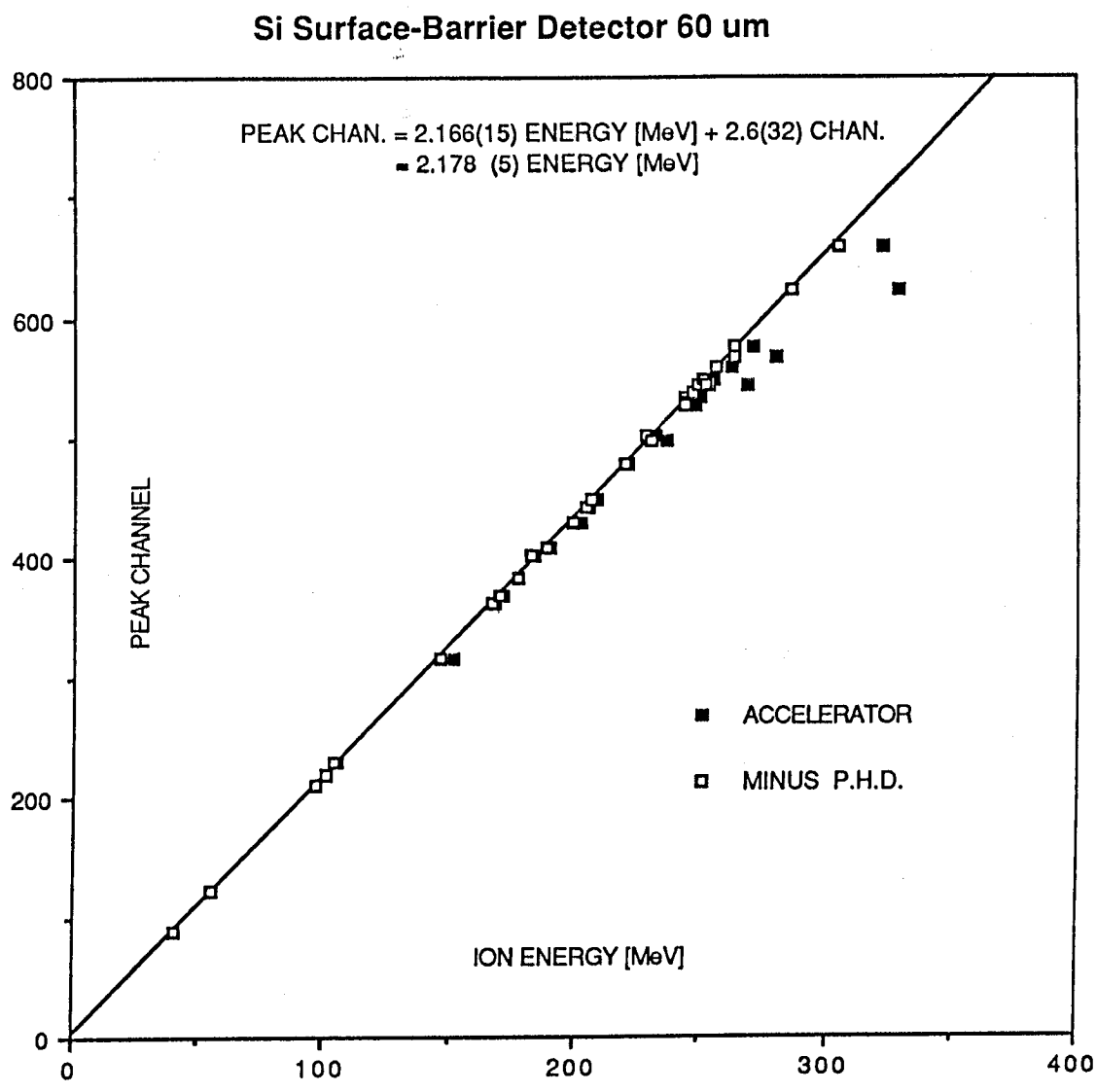


Fig. 1: Calibration curve of Si surface-barrier detector with 60 um depletion depth. The data was obtained using heavy ion beams ranging from ^{12}C, 40 MeV, to ^{197}Au, 330 MeV. The pulse height defect was subtracted from the beam energy before data fitting.

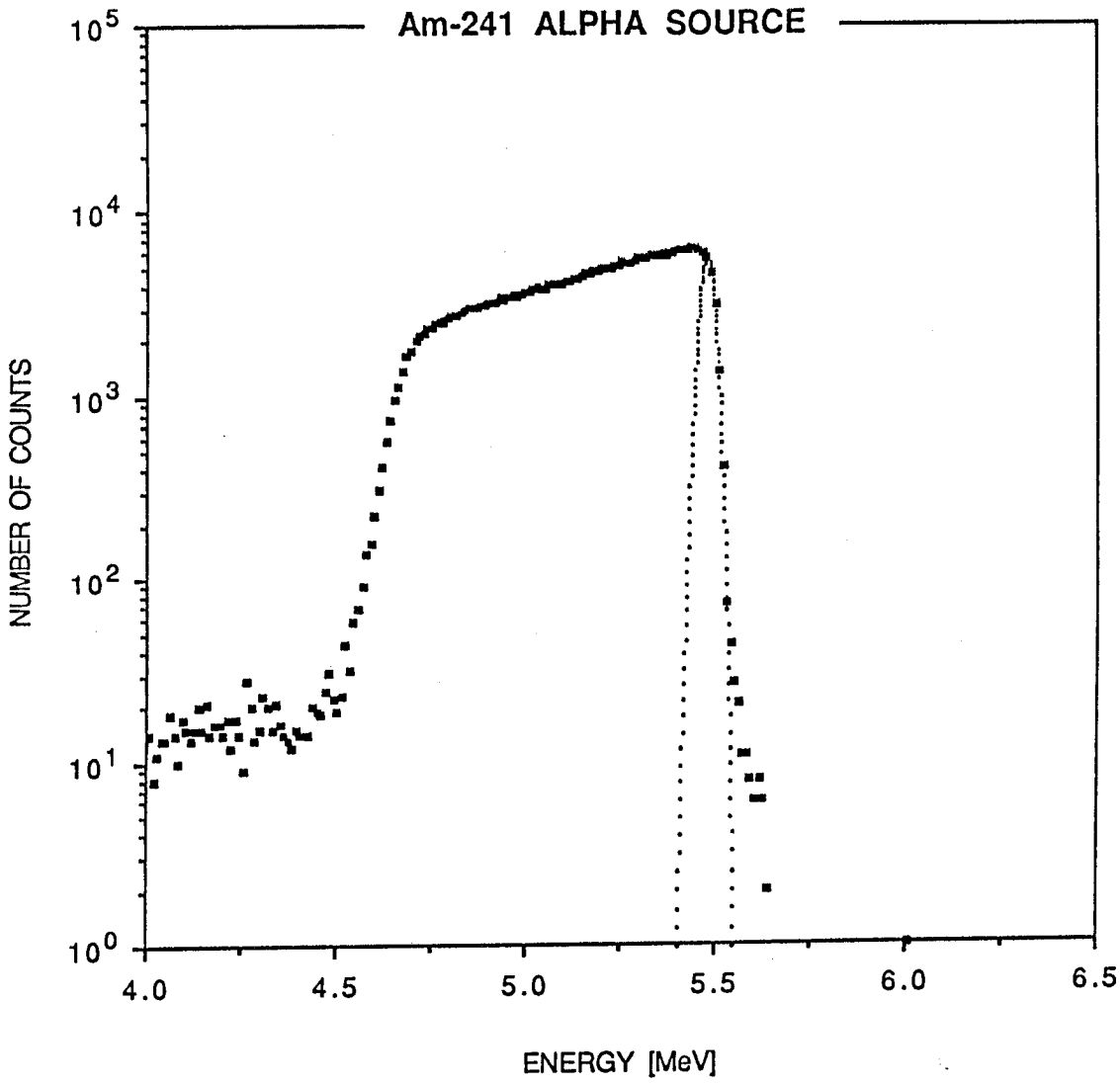


Fig. 2: Calibration of the Si surface-barrier detector with 300 um depletion depth using ^{241}Am alpha source (5.48 MeV). Due to self-absorption in the source the calibration constant is determined by fitting a Gaussian into the high-energy edge of the peak.

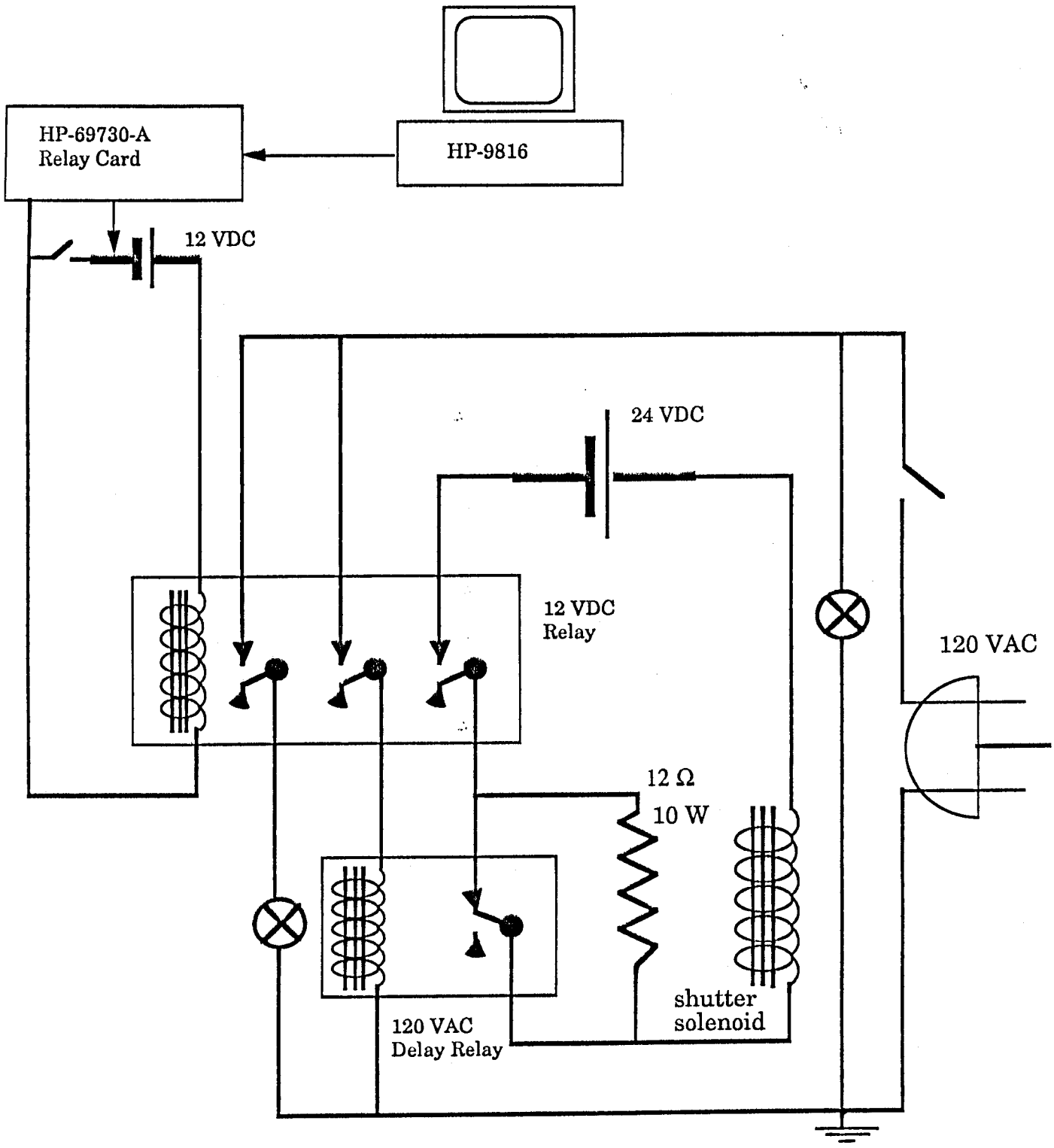


Fig. 3: Circuit operating the detector shutter. The 12 VDC relay opens both the shutter and after a delay time, the 120 VAC relay which reduces the stand-by current keeping the shutter open.

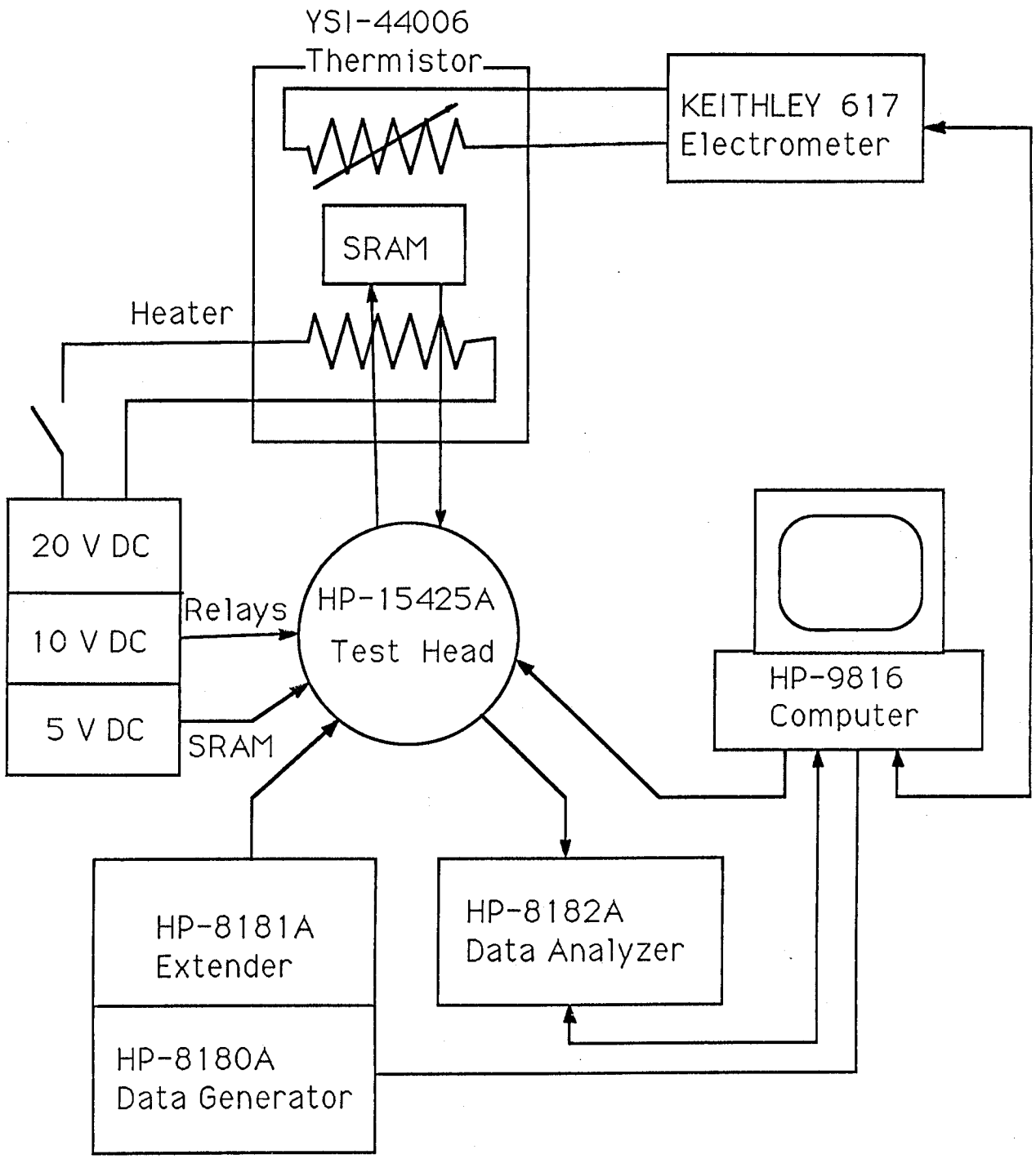


Fig. 4: Experimental set-up for the measurement of the SEU cross-sections.

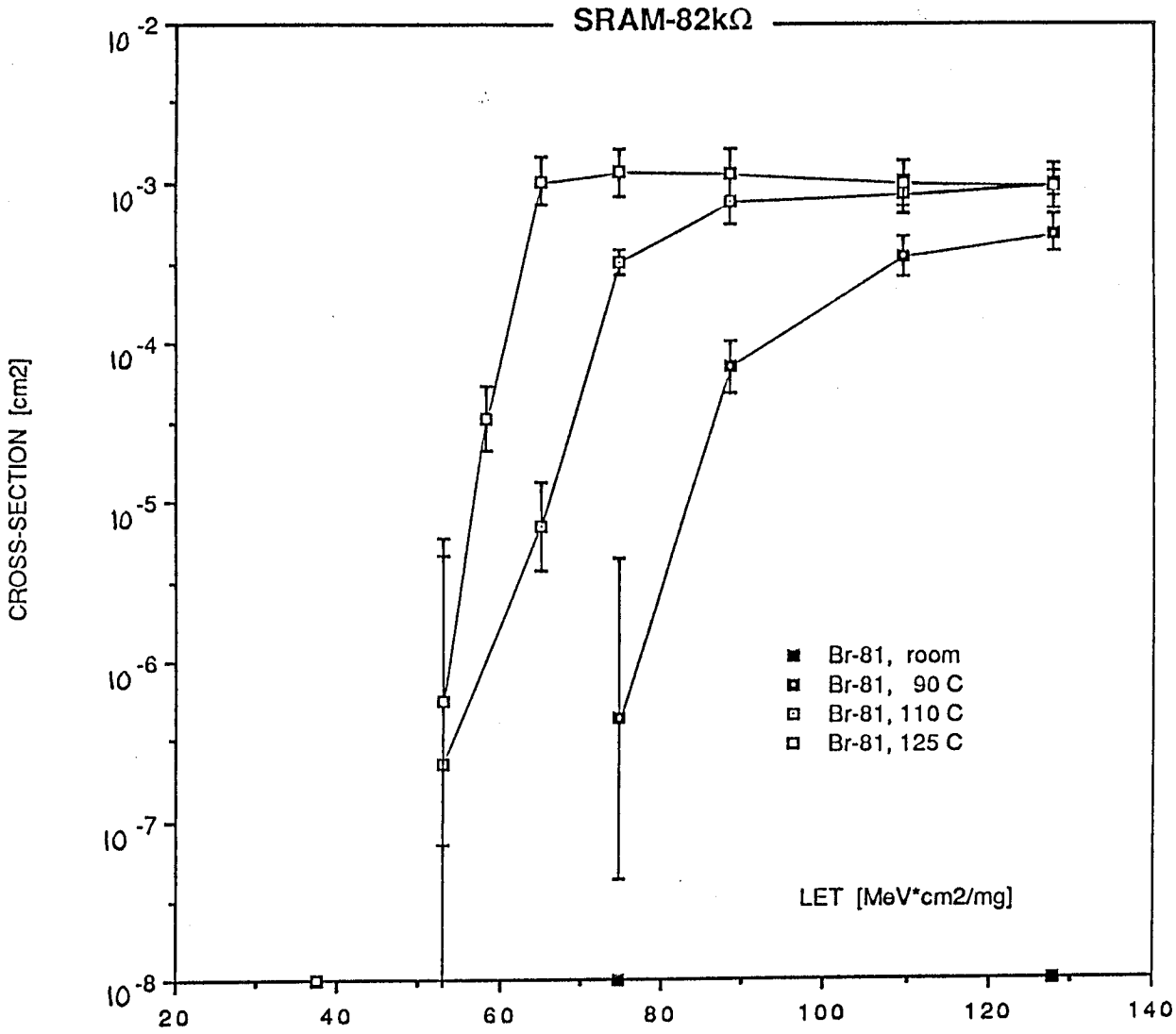


Fig. 5: SEU cross-sections vs. effective LET for 16K SRAM TA670 (1 um technology) with 82k feedback resistors irradiated by 260 MeV ^{81}Br ions at various temperatures. V_{DD} was 5.25 V.

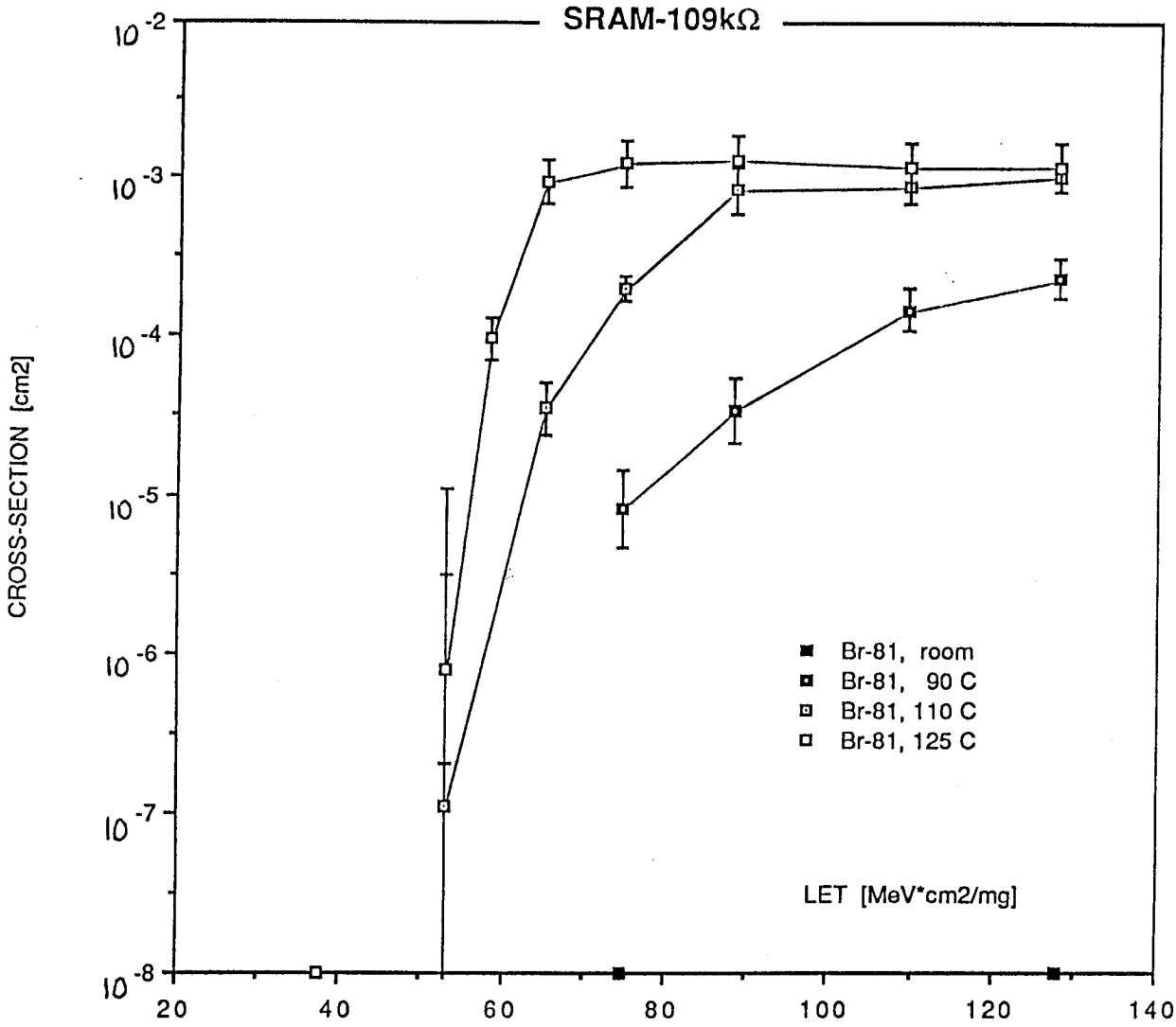


Fig. 6: SEU cross-sections vs. effective LET for 16K SRAM TA670 (1 um technology) with 109k feedback resistors irradiated by 260 MeV ^{81}Br ions at various temperatures. V_{DD} was 5.25 V.

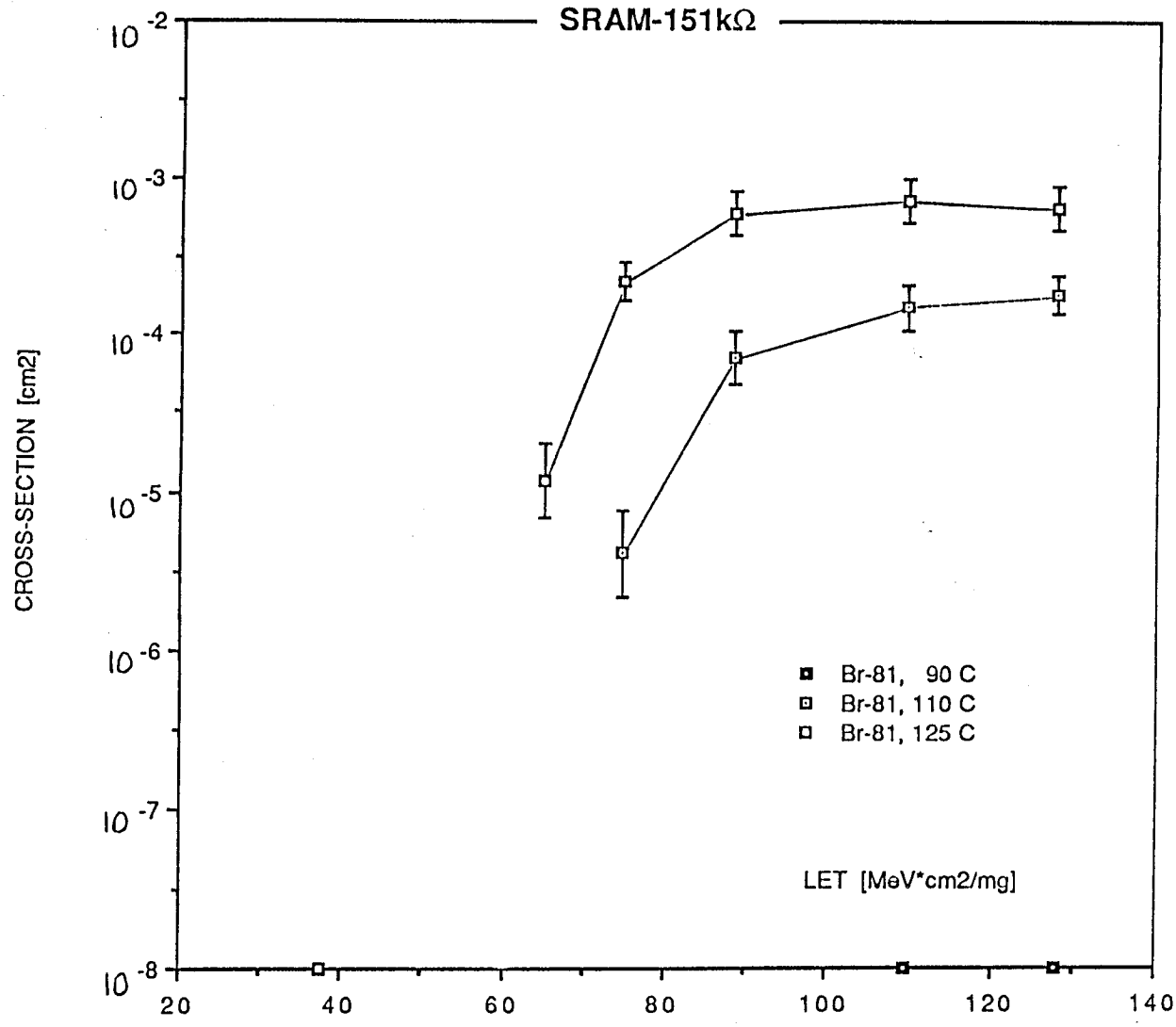


Fig. 7: SEU cross-sections vs. effective LET for 16K SRAM TA670 (1 um technology) with 151k feedback resistors irradiated by 260 MeV ^{81}Br ions at various temperatures. V_{DD} was 5.25 V.

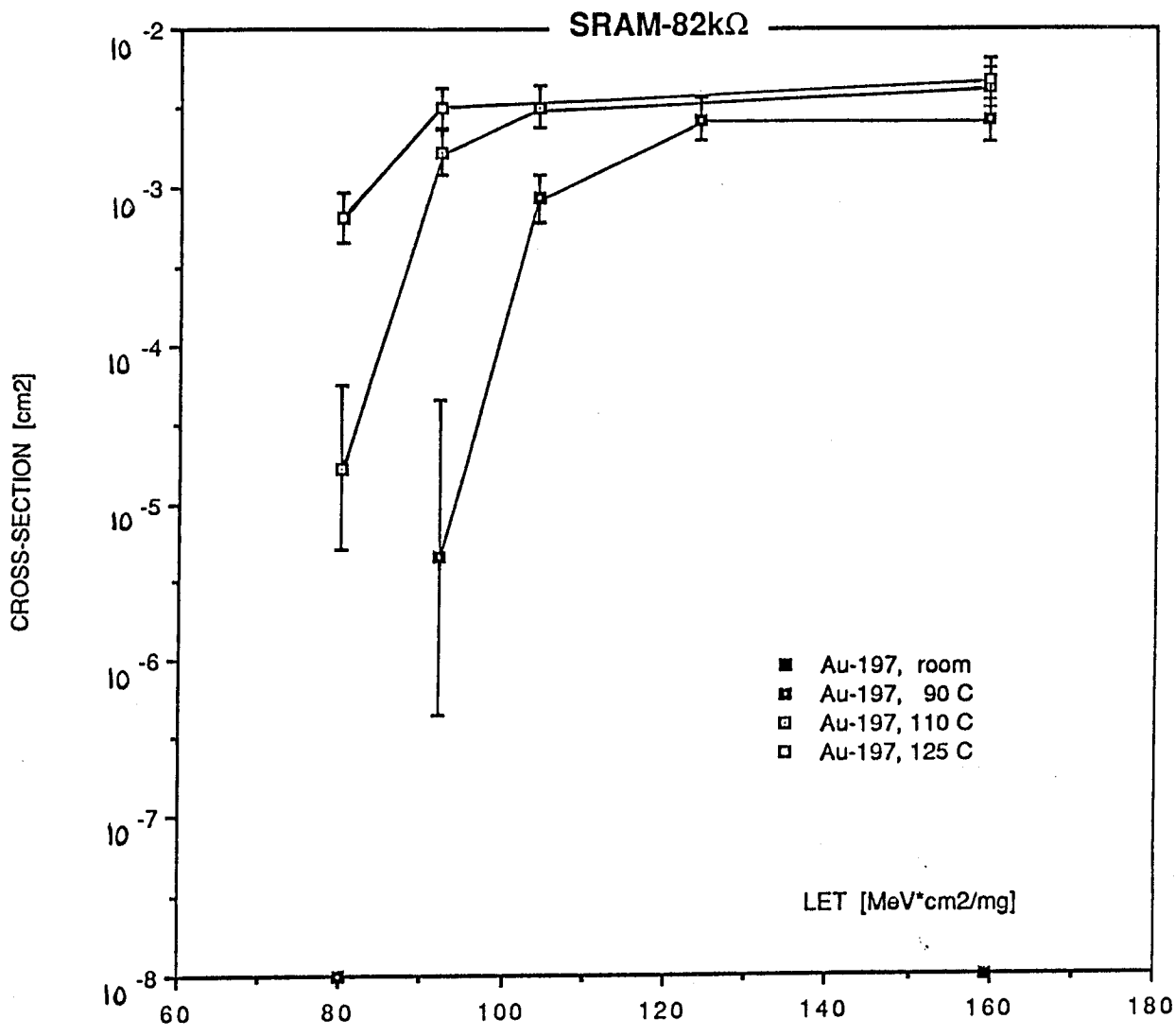


Fig. 8: SEU cross-sections vs. effective LET for 16K SRAM TA670 (1 um technology) with 82k feedback resistors irradiated by 325 MeV ^{197}Au ions at various temperatures. V_{DD} was 5.25 V.

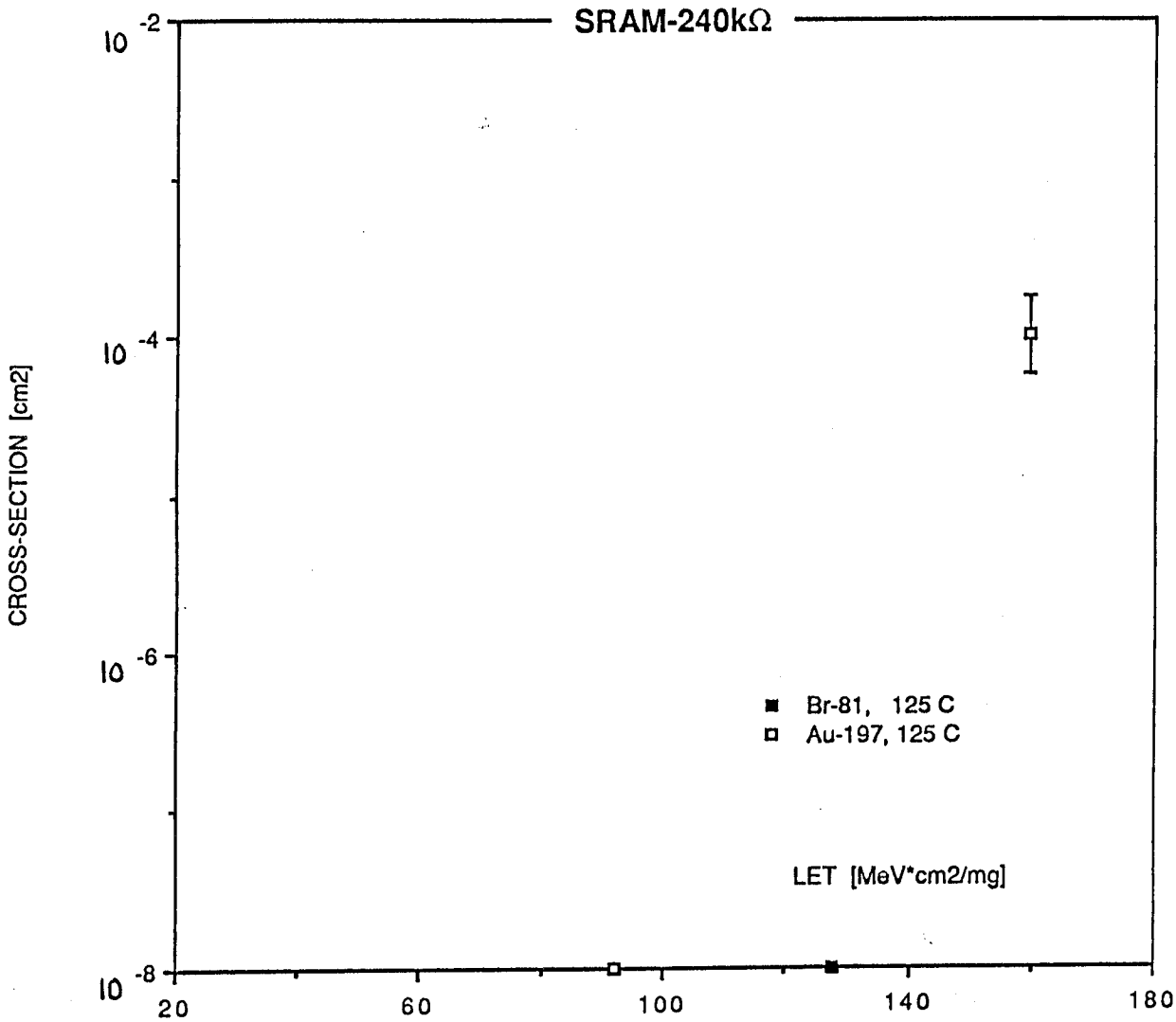


Fig. 9: SEU cross-sections vs. effective LET for 16K SRAM TA670 (1 um technology) with 240k feedback resistors irradiated by 260 MeV ^{81}Br and 325 MeV ^{197}Au ions at 125°C. V_{DD} was 5.25 V.

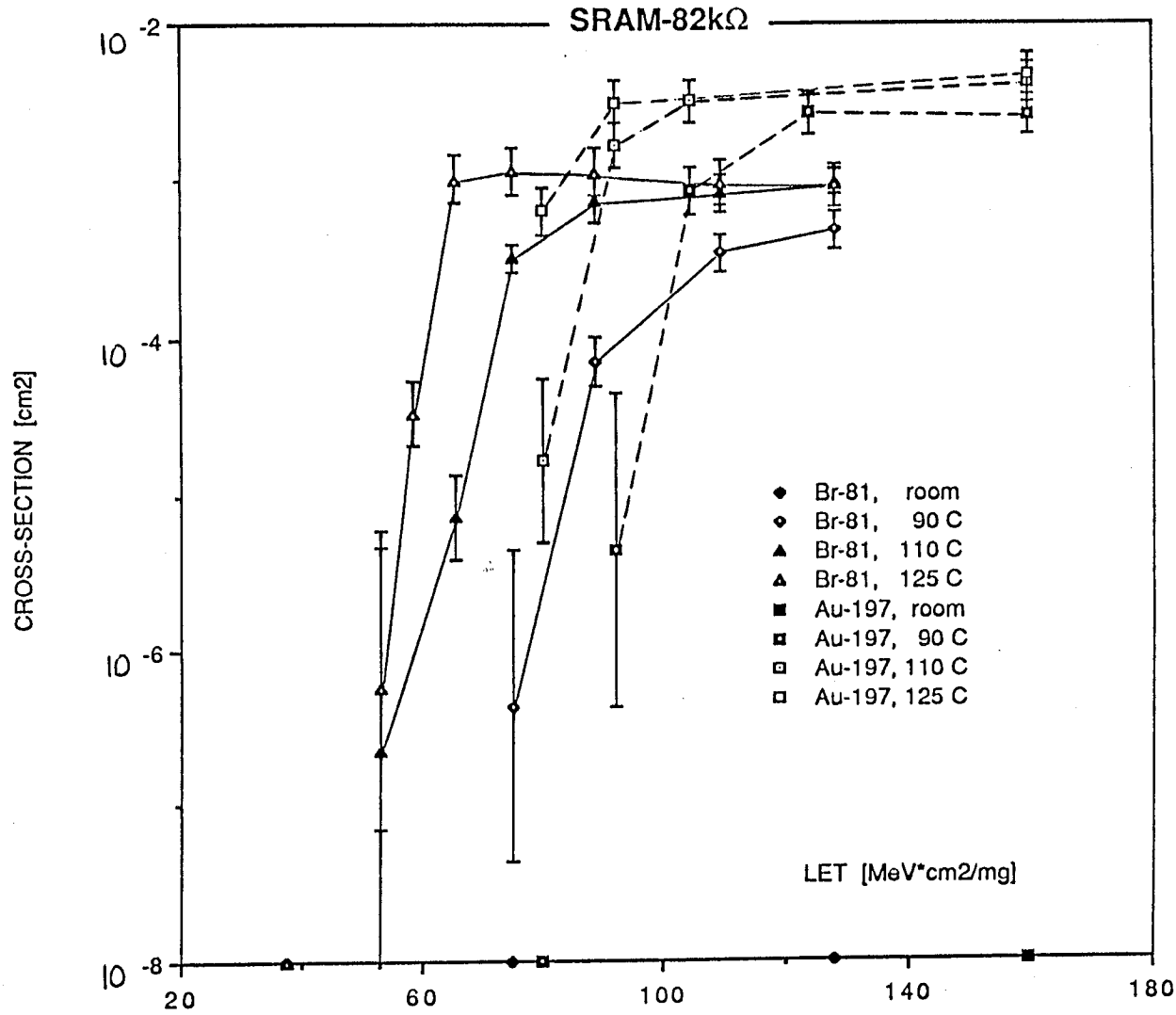


Fig.10: SEU cross-sections vs. effective LET for 16K SRAM TA670 with 82k feedback resistors. Results for 260 MeV ^{81}Br are compared to those for 325 MeV ^{197}Au. The difference in thresholds is due to the energy loss in a passivation layer, which does not change LET of 260 MeV ^{81}Br but reduces that of 325 MeV ^{197}Au.

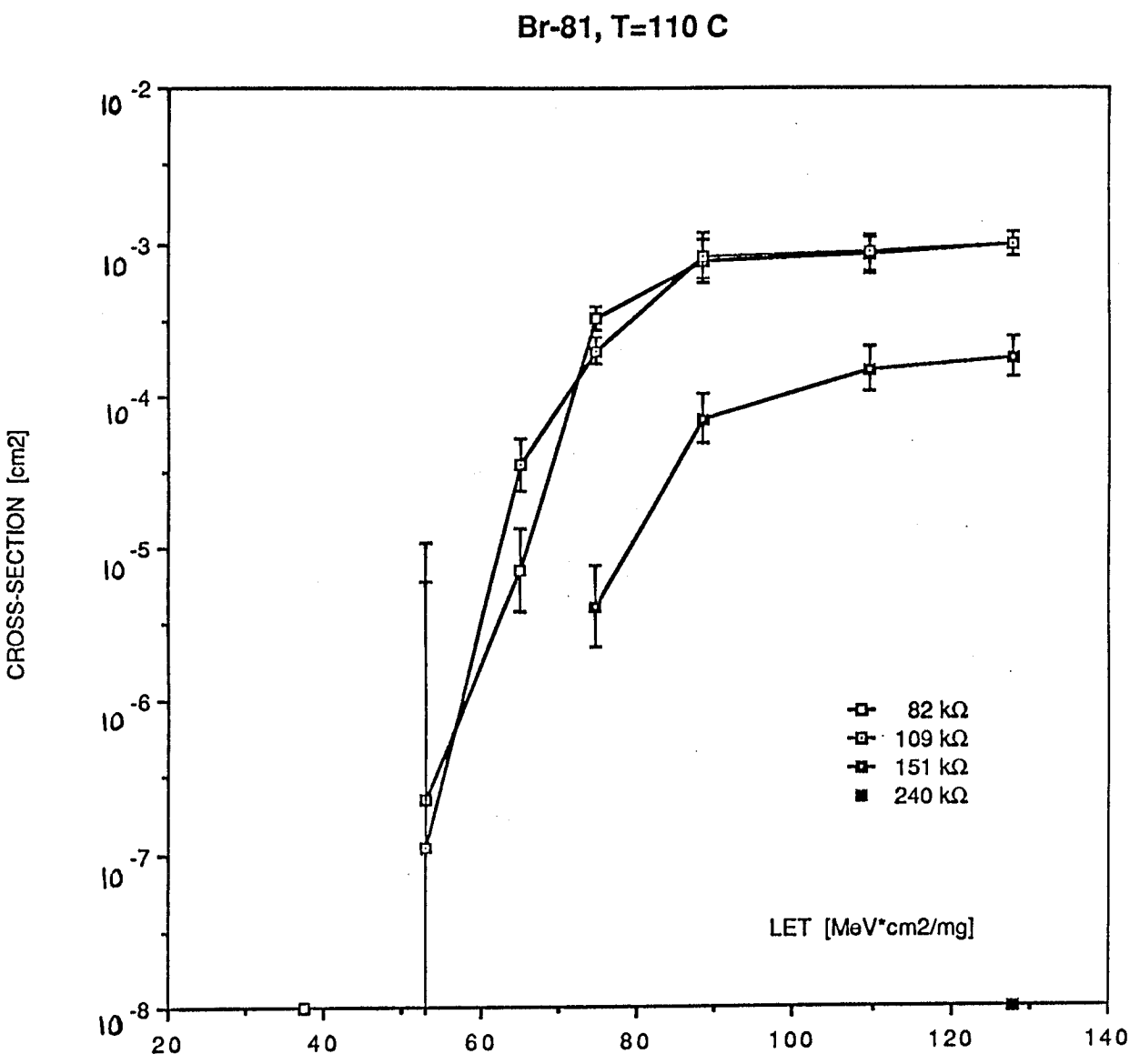
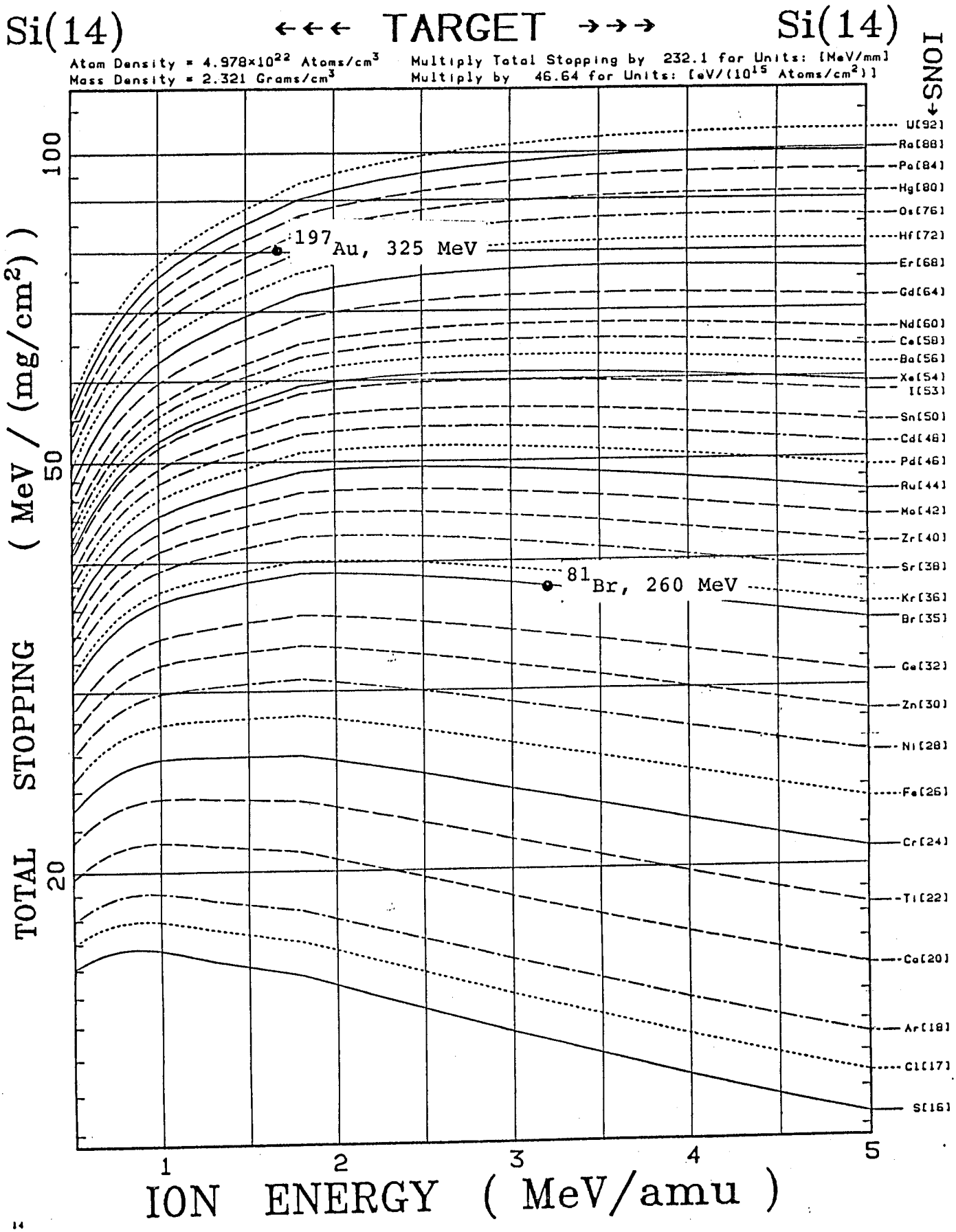


Fig.11: SEU cross-sections vs. effective LET for 16K SRAMs TA670 with various feedback resistors irradiated by 260 MeV ^{81}Br ions at 110°C.

Fig.12: LET for heavy ions in Si (from Ziegler's tables).



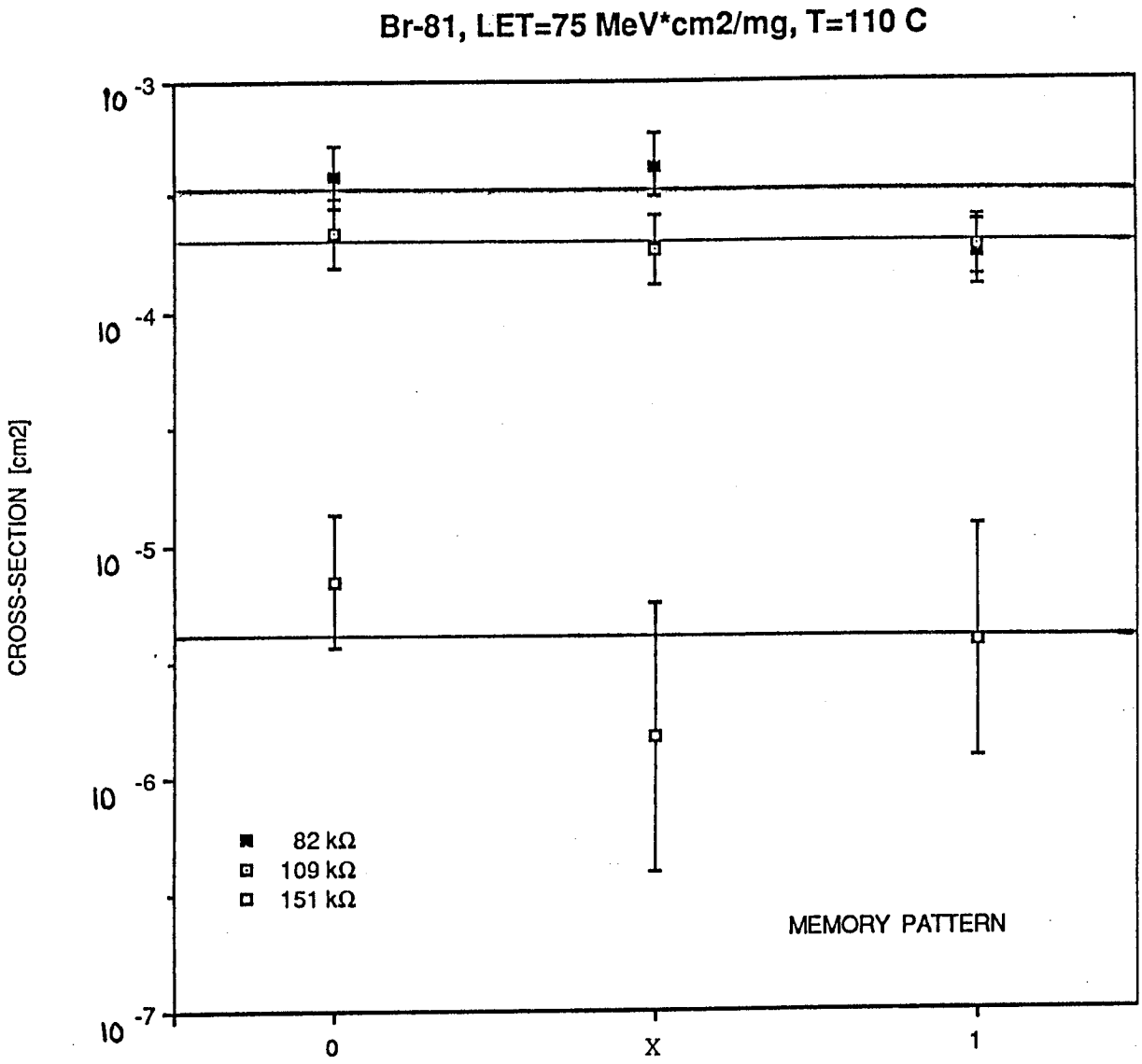


Fig.13: Comparison of SEU cross-sections for 16K SRAMs TA670 with various feedback resistors irradiated by 260 MeV ^{81}Br ions at 110°C for different original memory patterns: (0) all zeros, (X) checkerboard, and (1) all units. The tilt angle was 60°.

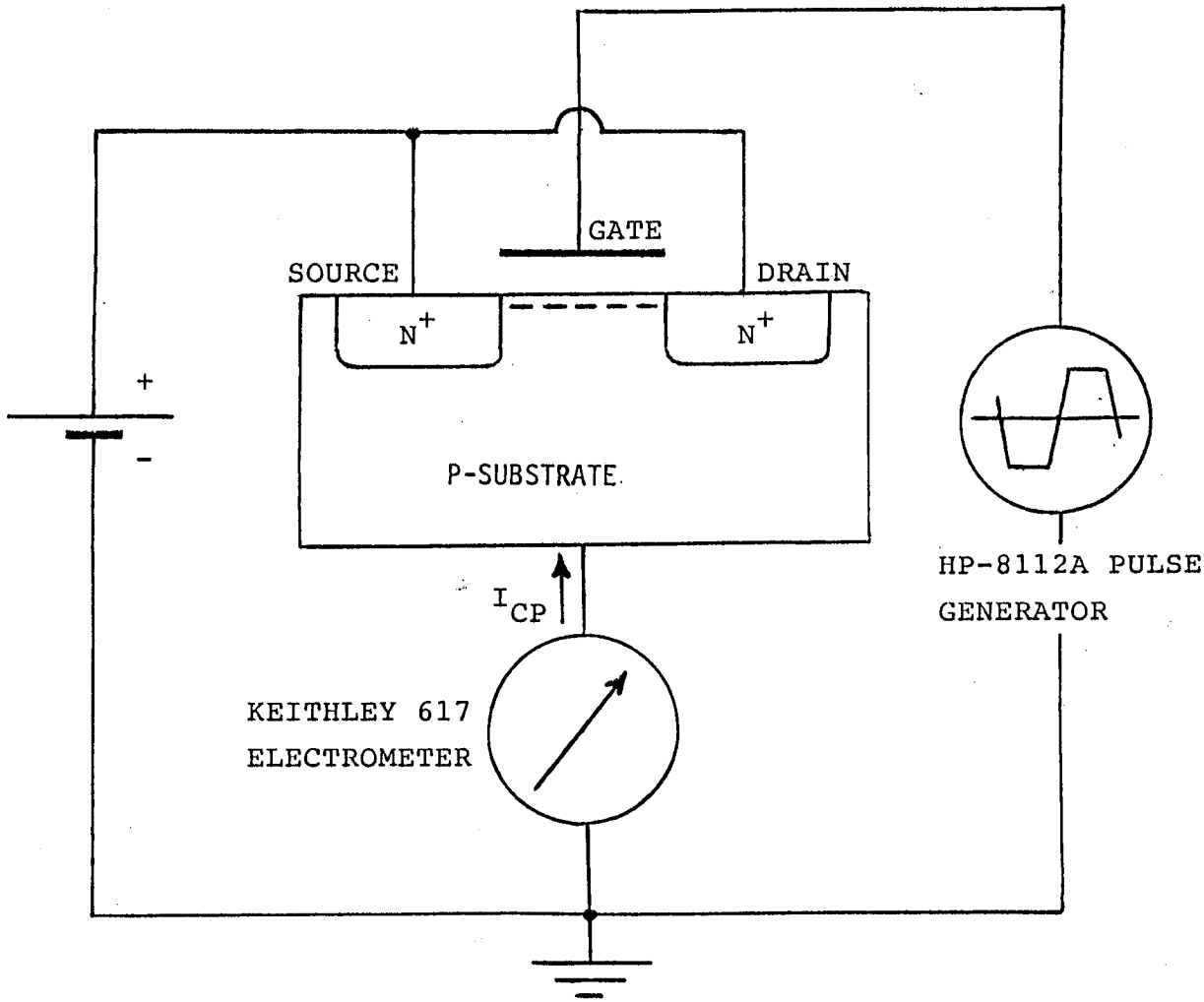


Fig.14: Basic Charge Pumping experimental set-up with NMOS transistor.

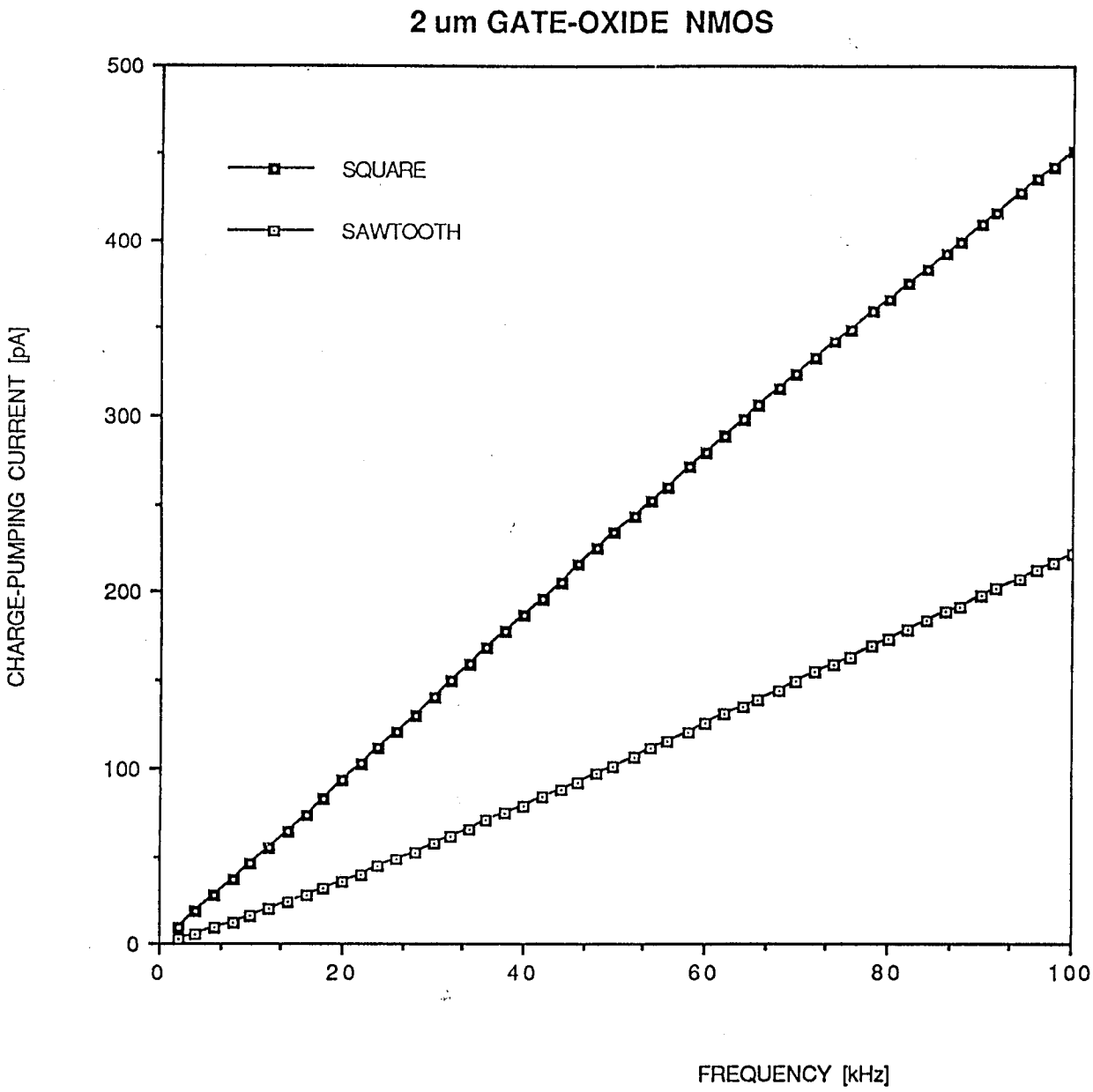


Fig.15: Charge pumping current vs. frequency for square and sawtooth waveforms. For the square waveform, the dependency is linear.

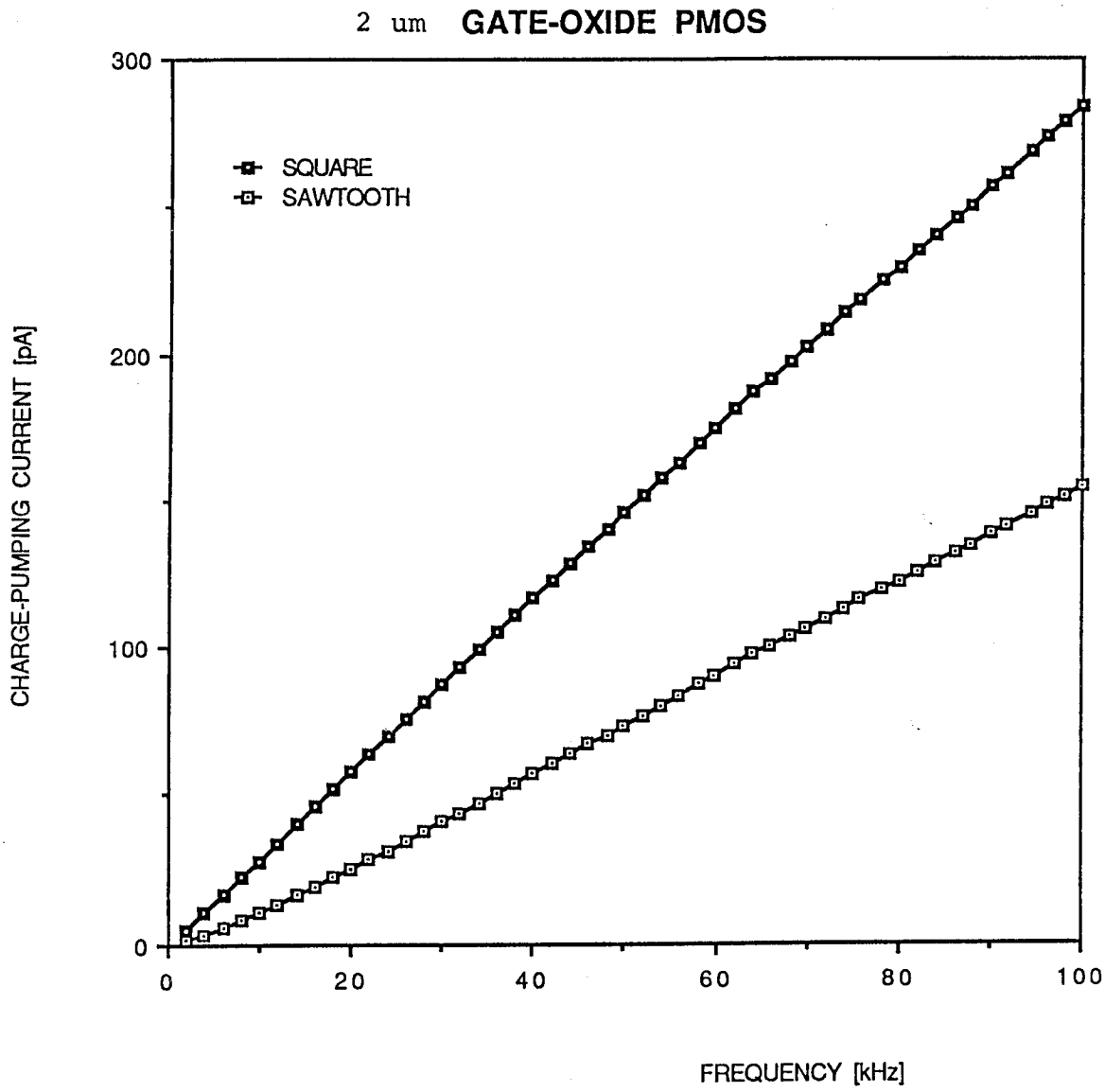


Fig.16: Charge-pumping current vs. frequency for square and sawtooth waveforms. For the square waveform, the dependency is linear.

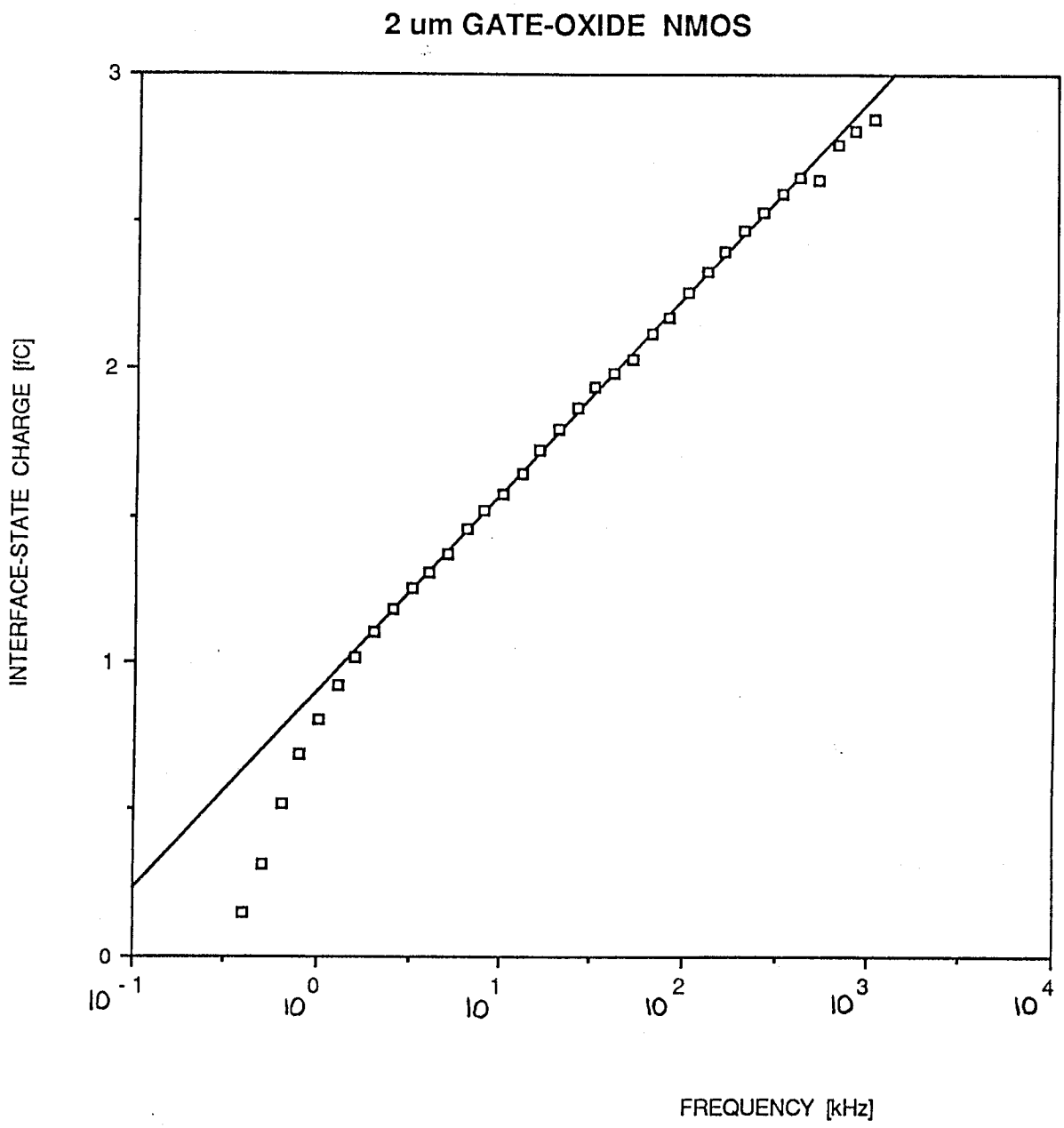


Fig.17: Interface state charge vs. frequency for the sawtooth waveform. The slope is proportional to the average interface trap density and the extrapolated frequency to the geometrical mean ofelectron and hole capture cross-sections.

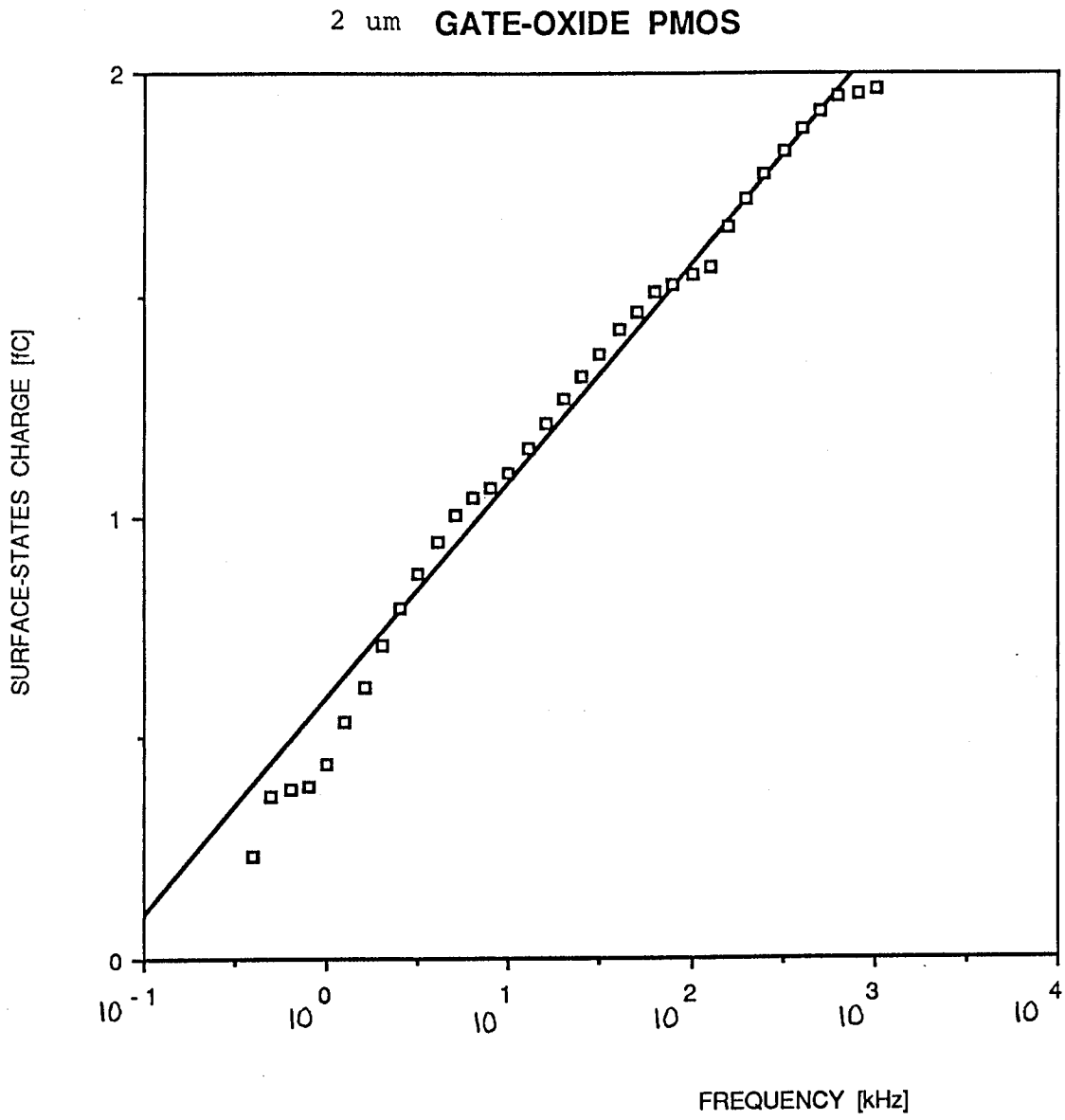


Fig.18: Interface state charge vs. frequency for the sawtooth waveform. The slope is proportional to the average interface trap density and the extrapolated frequency to the geometrical mean of electron and hole capture cross-sections.

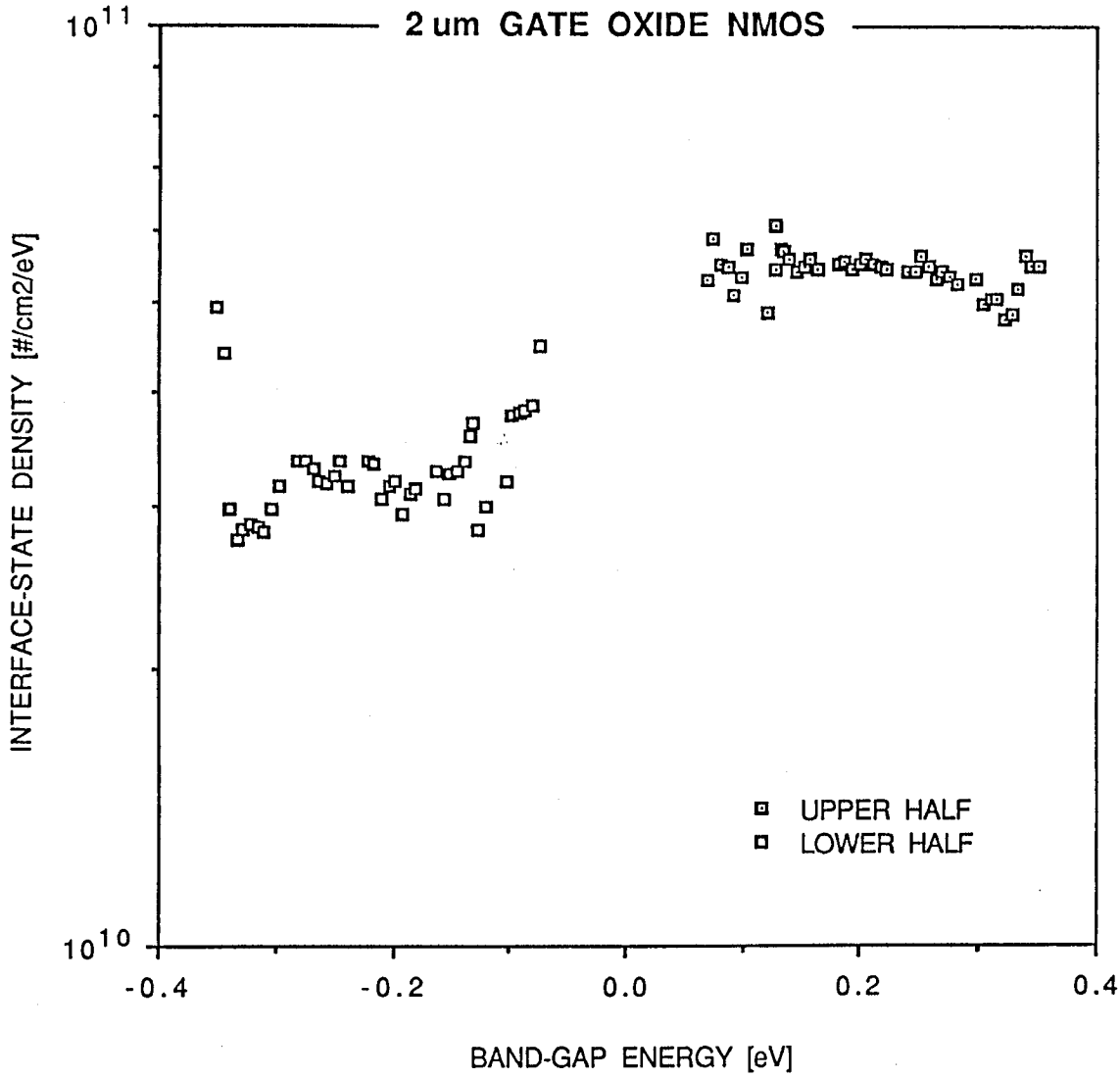


Fig.19: Energy distribution of the interface states over the band gap.

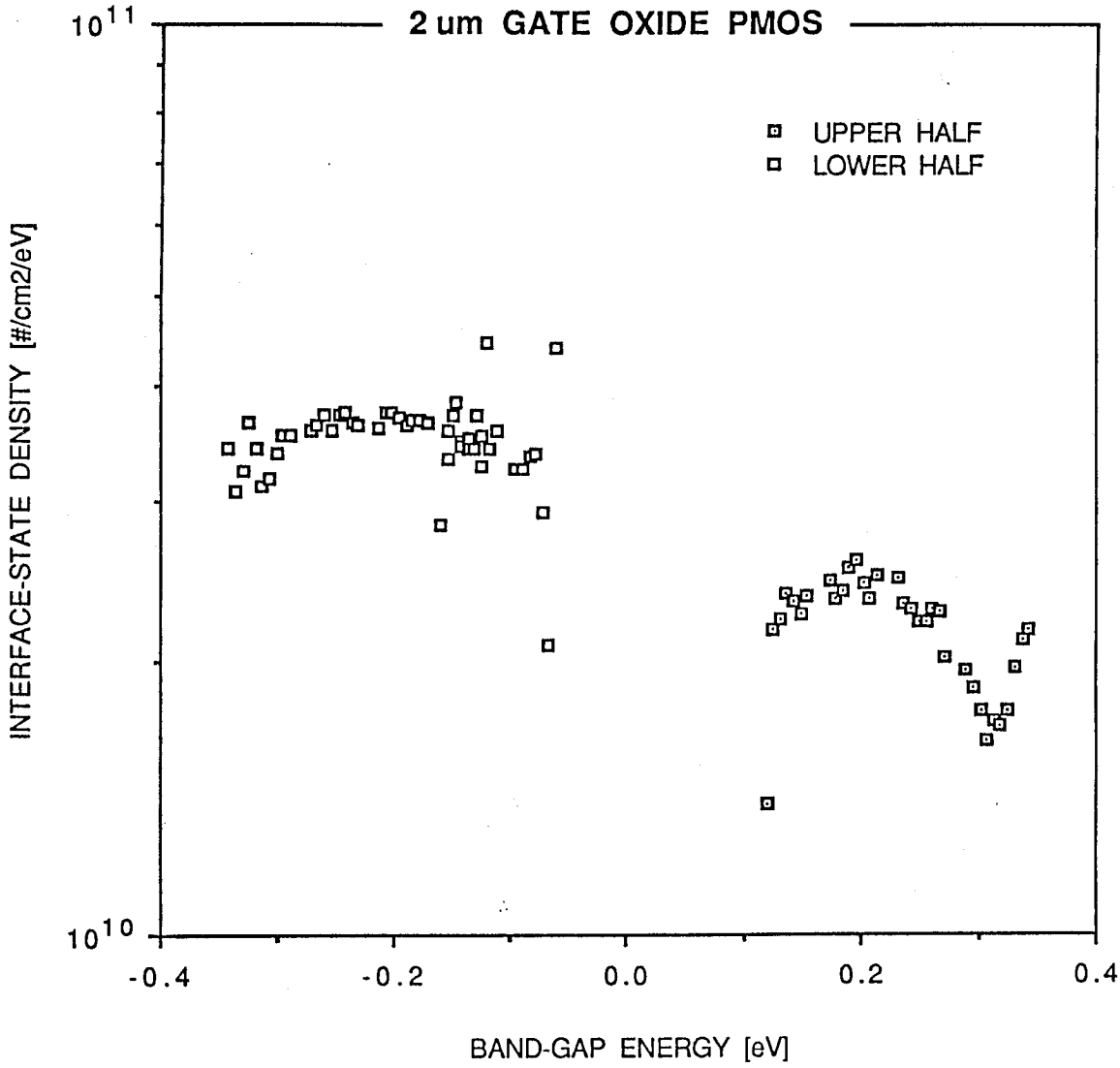


Fig.20: Energy distribution of the interface states over the band gap.

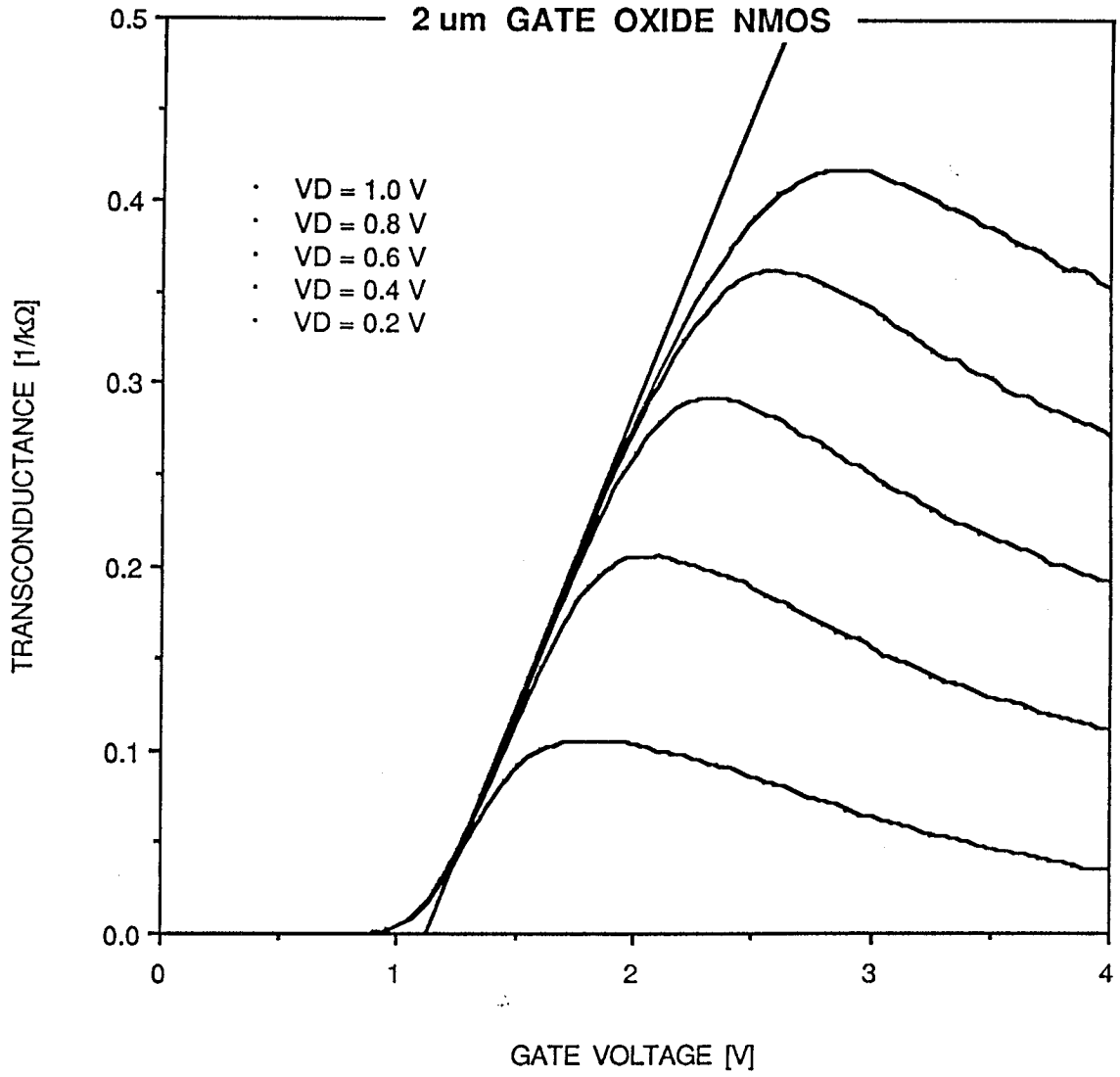


Fig.21: A family of transconductance curves $g_m = dI_d/dV_g$. The threshold voltage is determined by putting a line through the inflexion point.

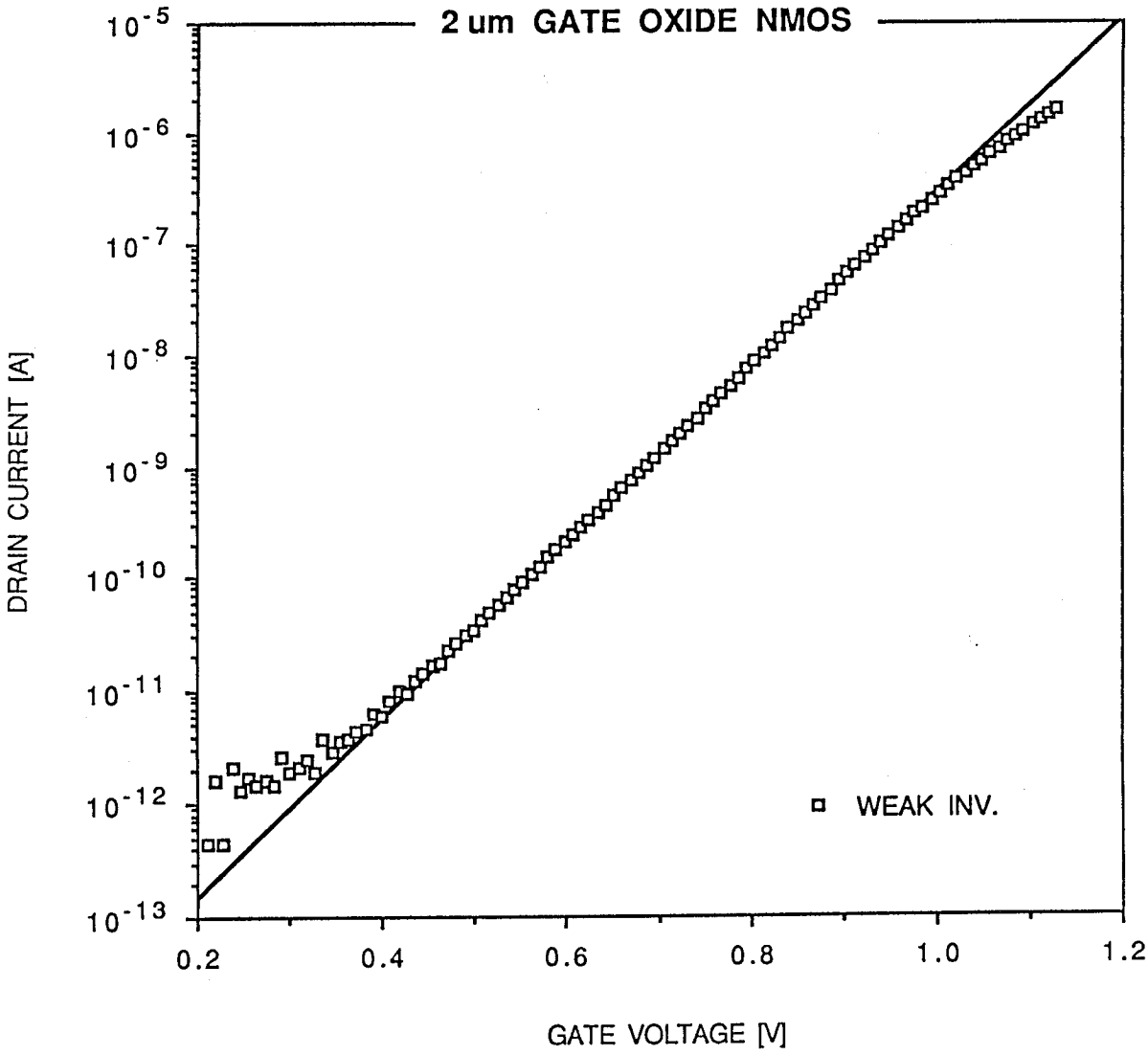


Fig.22: The sub-threshold slope $d(\ln I_d)/dV_g$.

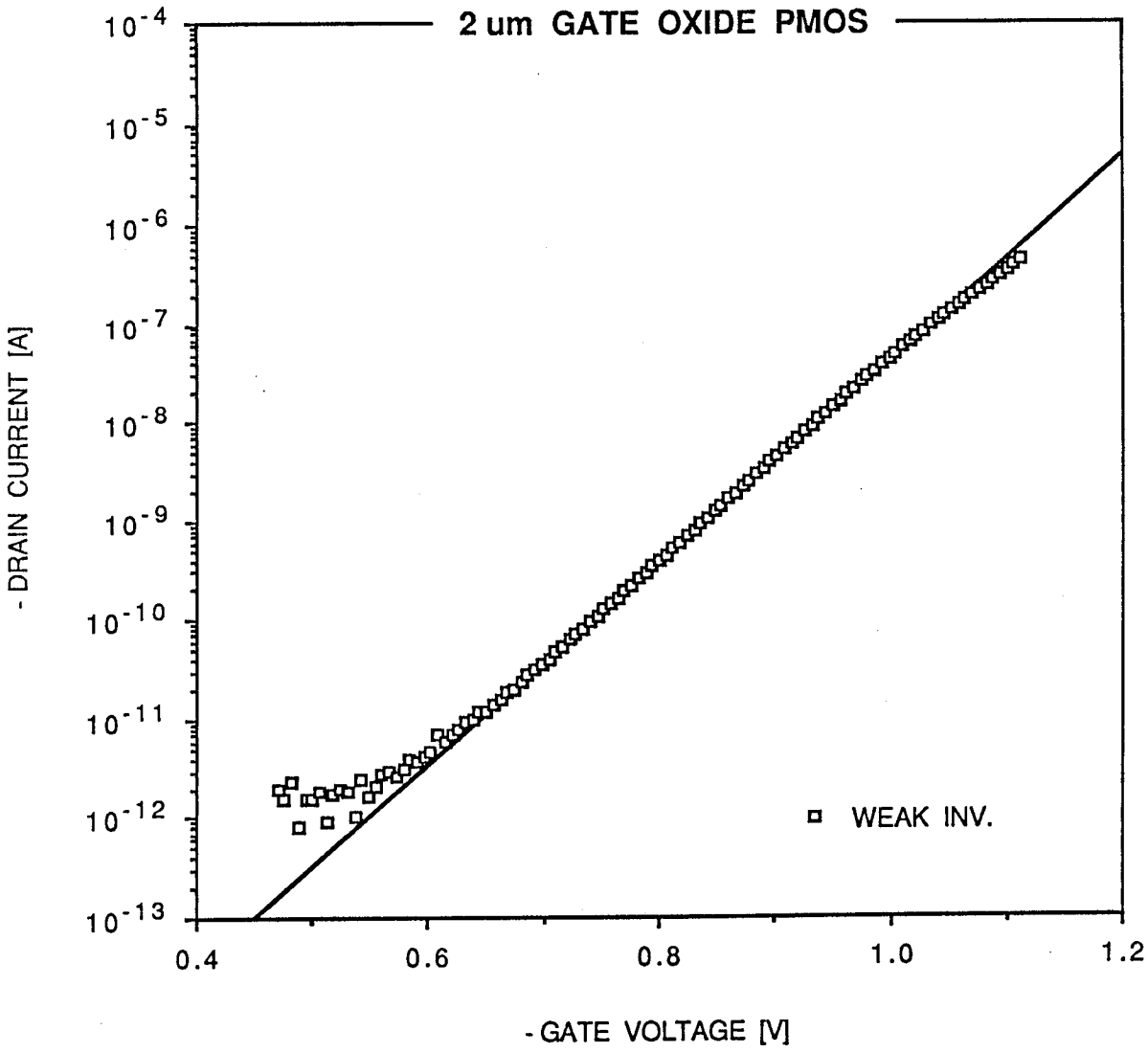


Fig.23: The sub-threshold slope $d(\ln I_d)/dV_g$.

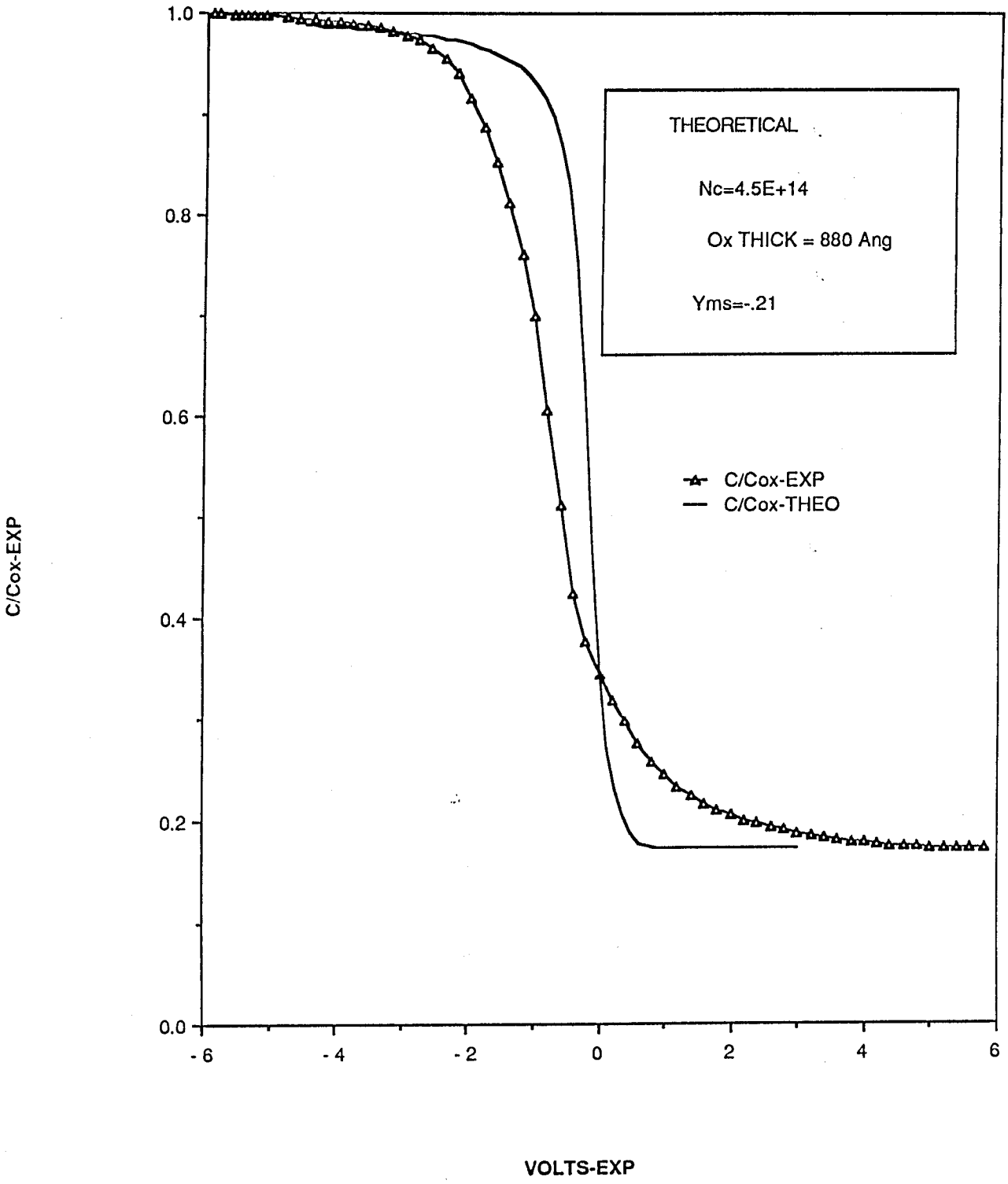

Na-FREE-CV
THEORETICAL
Nc=4.5E+14
Ox THICK = 880 Ang
Yms=-.21
C/Cox-EXP
C/Cox-THEO
C/Cox-EXP
1.0
0.8
0.6
0.4
0.2
0.0
-6
-4
-2
0
2
4
6
VOLTS-EXP

Fig. 24

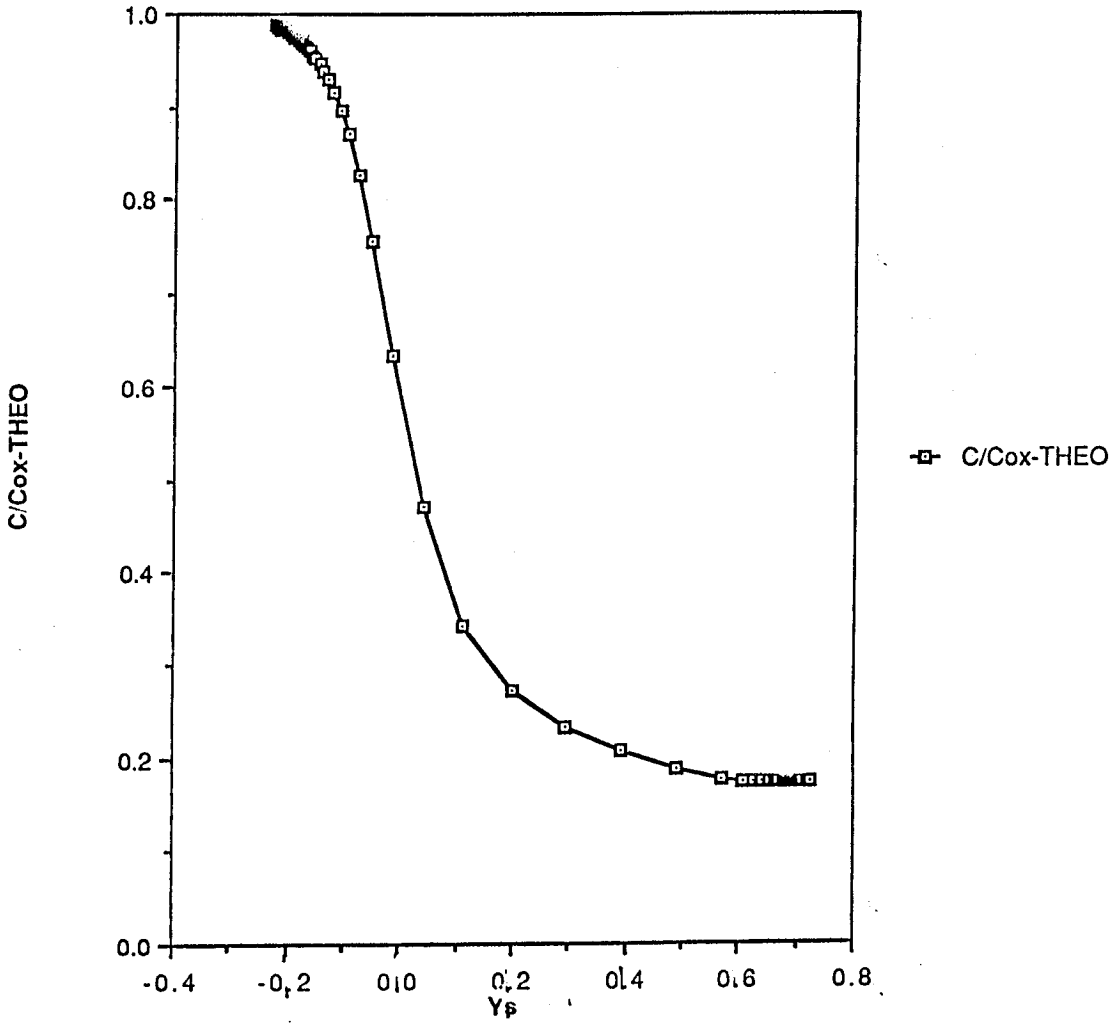

sig volts vs capacitance
C/Cox-THEO
1.0
0.8
0.6
0.4
0.2
0.0
-0.4
-0.2
0.0
0.2
0.4
0.6
0.8
Ys
C/Cox-THEO

Fig. 25

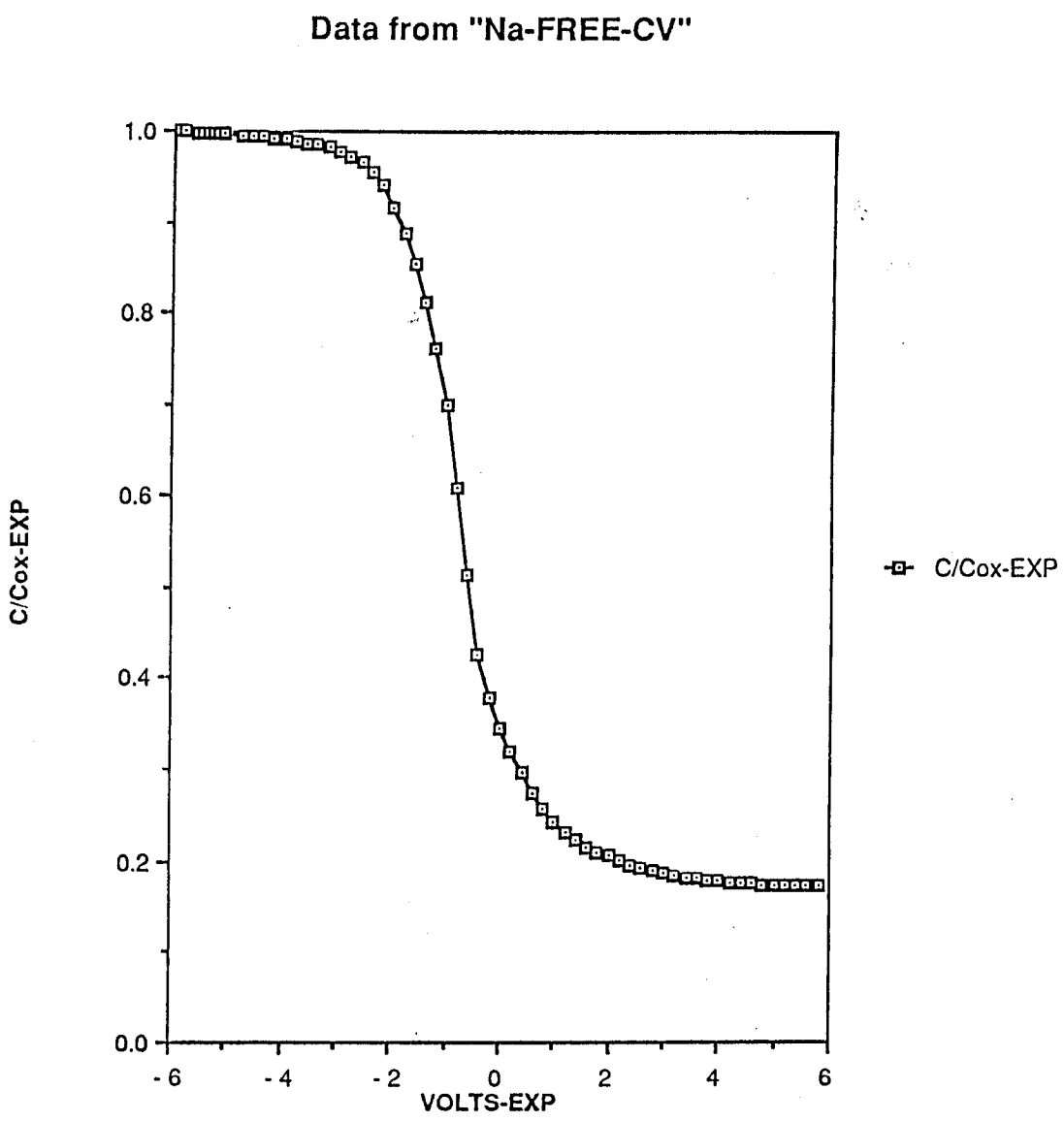

Data from "Na-FREE-CV"
C/Cox-EXP
1.0
0.8
0.6
0.4
0.2
0.0
-6
-4
-2
0
2
4
6
VOLTS-EXP
C/Cox-EXP

Fig. 26

TERMAN ANALYSIS
GATE VOLTS
-4
-2
0
2
4
6
SURFACE VOLTS
-10
0
10
20
30
THEORETICAL Dit=0
STRETCHOUT Dit>0

Fig. 27

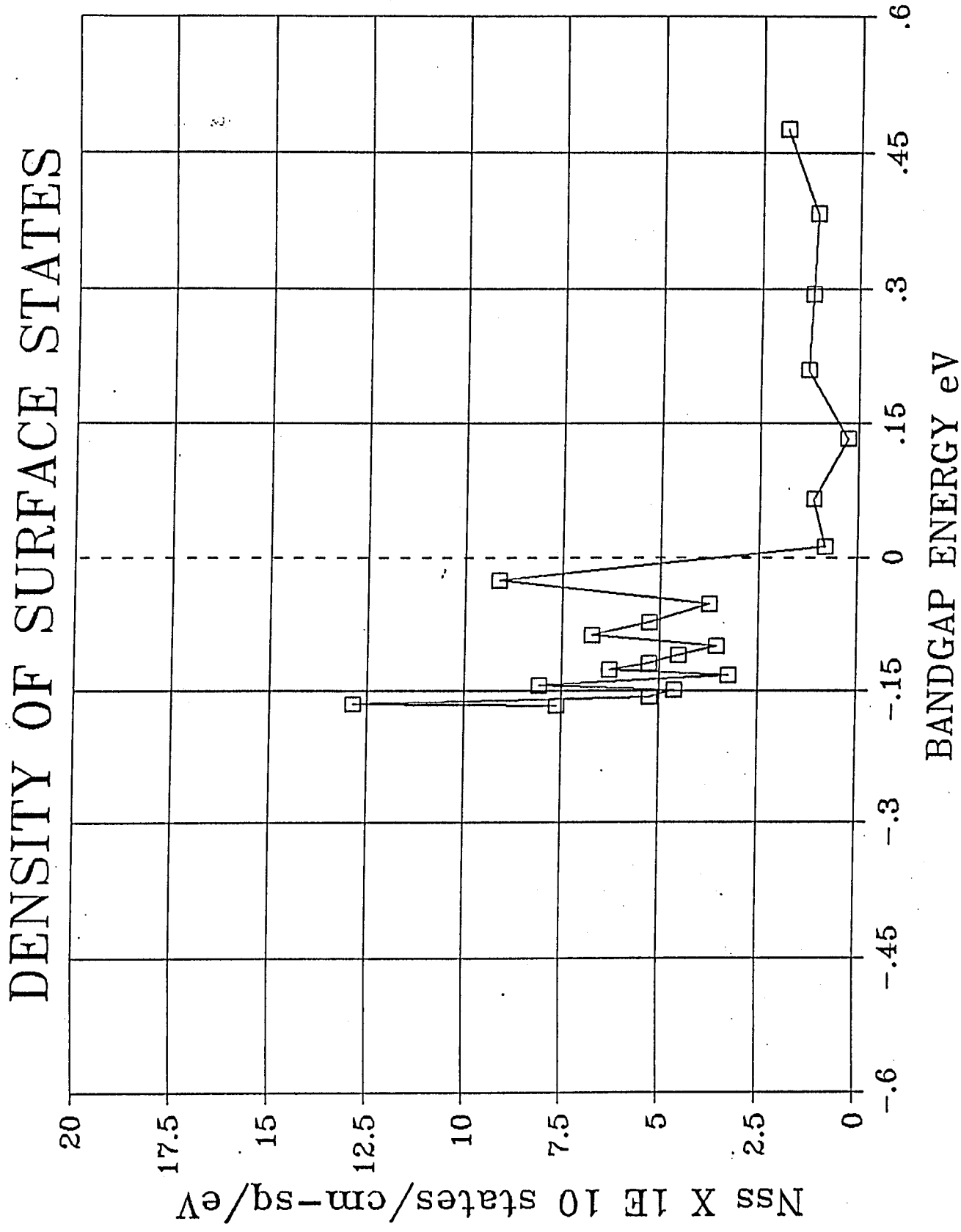
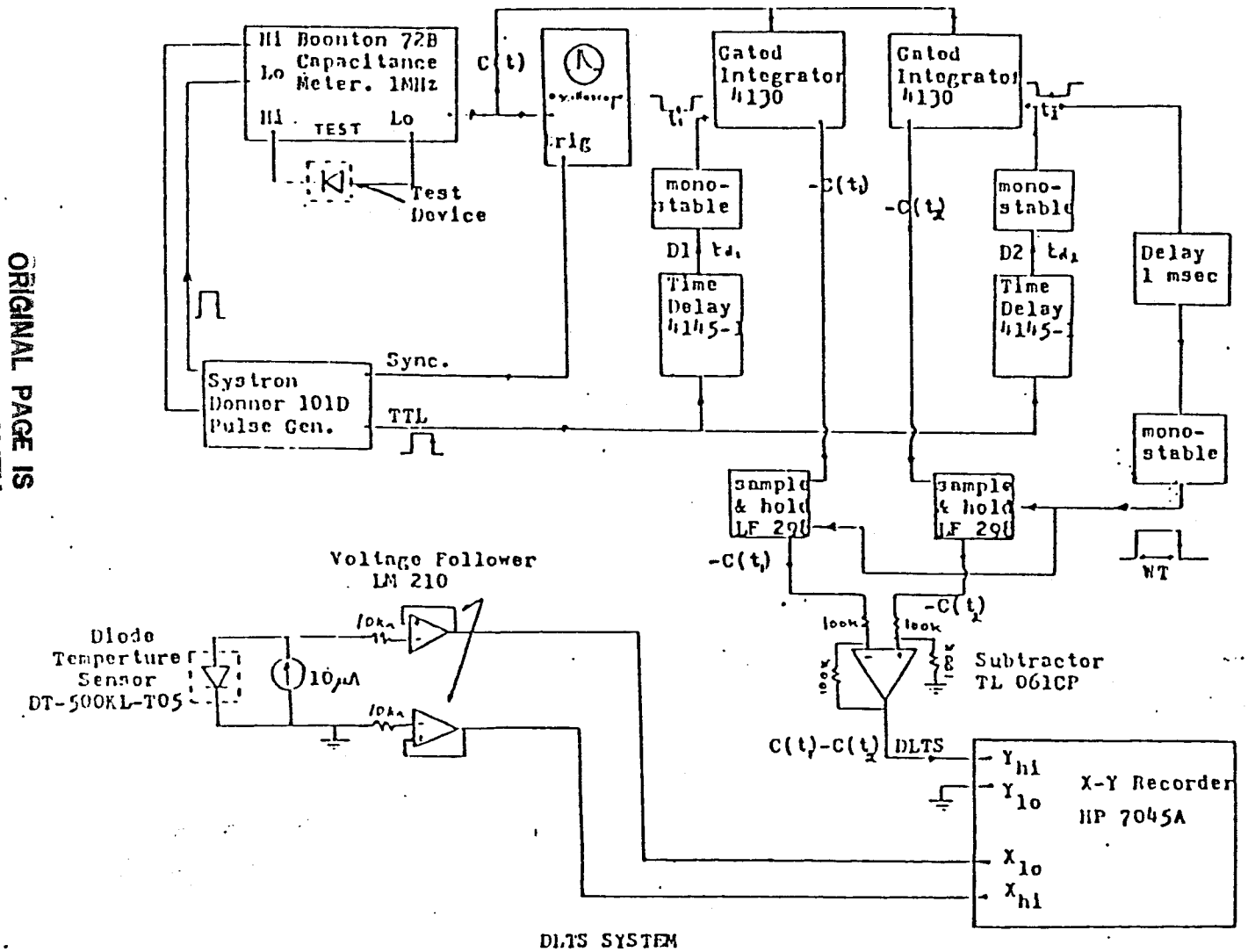

DENSITY OF SURFACE STATES
Nss X 1E 10 states/cm-sq/eV
20
17.5
15
12.5
10
7.5
5
2.5
0
-.6
-.45
-.3
-.15
0
.15
.3
.45
.6
BANDGAP ENERGY eV

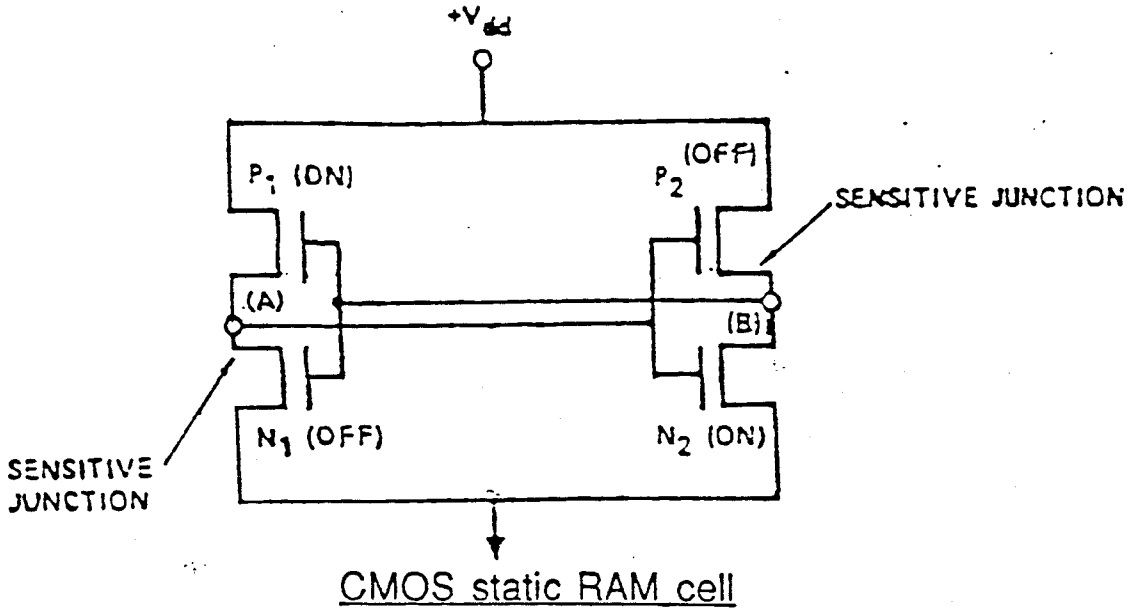
Fig. 28



DLTS SYSTEM

Figure 29. Second DLTS System.

Fig. 30: CMOS STATIC RAM SEU-ERROR MECHANISM



_ When a cosmic ray strikes a Drain of the "OFF" transistor, the Gate-voltage change occurs on the other Inverter .

_ "ON" transistors forced "OFF"; "OFF" transistors forced "ON"

_ CMOS Static RAM cell assumes stable state opposite to original, resulting in SEU error.

Fig. 31: **RADIATION INDUCED SINGLE EVENT UPSET MECHANISM**

- p_type silicon in "deep depletion"
- Potential well empty

- 5 MeV Alpha-particle created 1.4 million electron-hole pairs.

- Electrons reaching a depletion region are swept into the potential well by the region's electric field.
- Holes are repelled.

- Potential well completely filled.
- If the amount of collected charge greater than the amount of critical charge, a SEU error or data change occurs.
- No permanent damage results

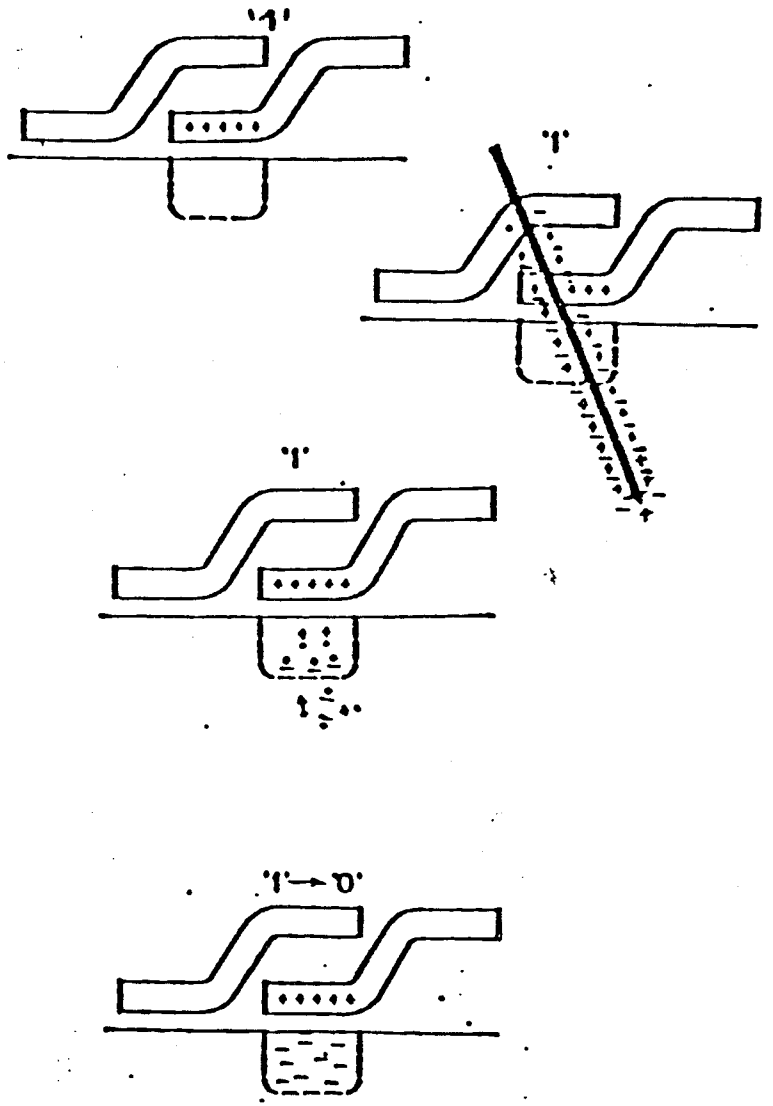
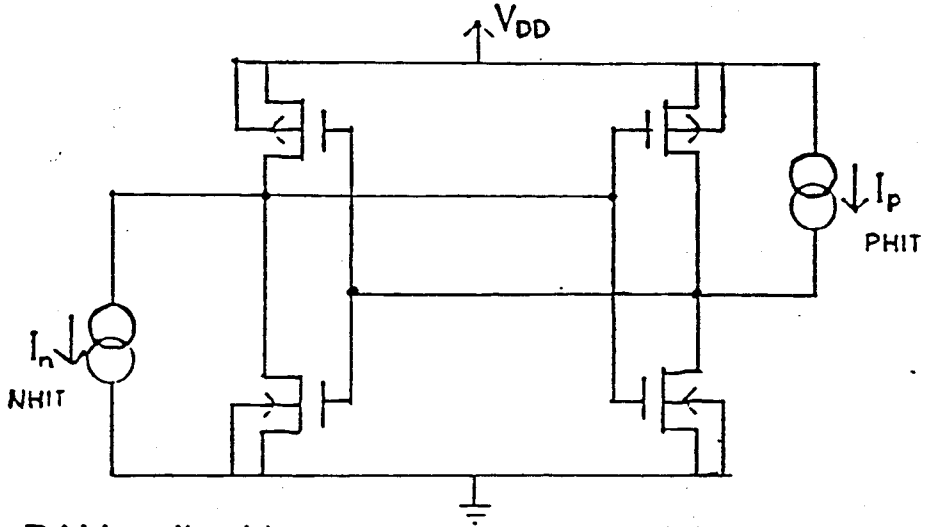


Fig. 32: **RAM CELL CRITICAL CHARGE ESTIMATE**

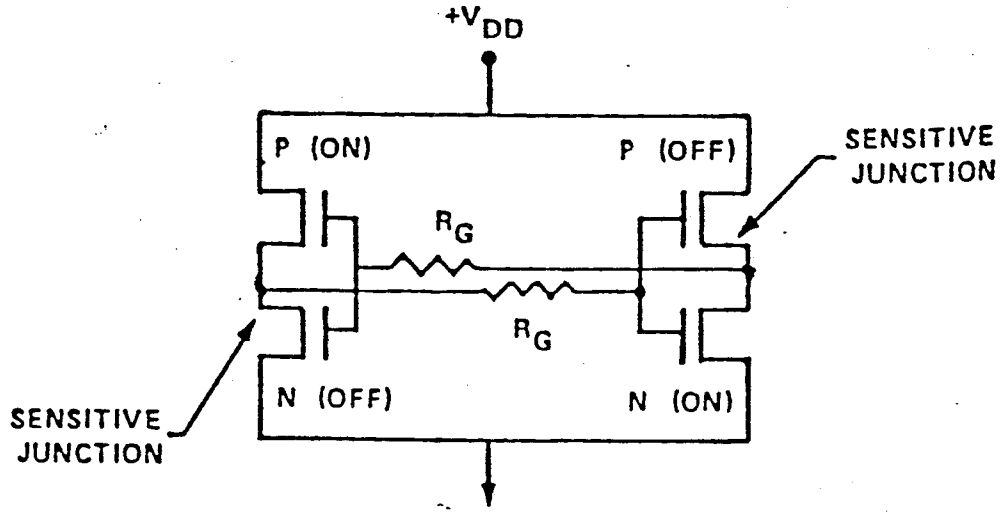


CMOS static RAM cell with current source model for critical charge estimate

- RAM cell simulated using the SPICE computer program by placed the current pulse in parallel with sensitive junctions and varied the current to find the threshold for memory changes.

- Critical charge(Q_C) determined by calculating the time integral of the minimum current pulse that caused upset.

Fig. 33: CMOS STATIC RAM CELL WITH FEEDBACK RESISTORS

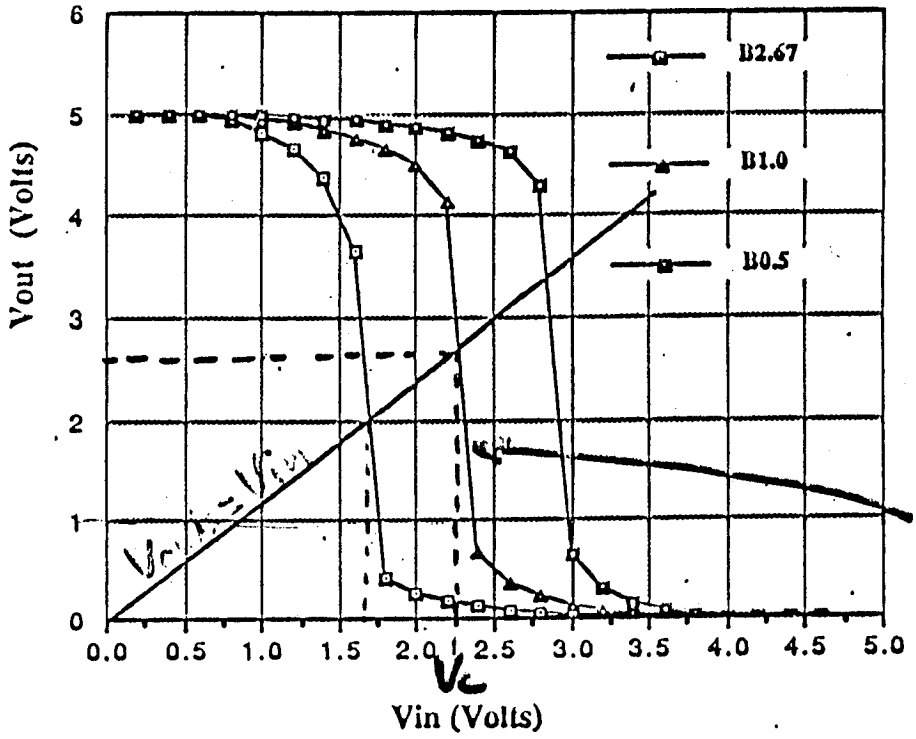


CMOS RAM cell Modified with R_G Resistors

- Resistors R_G will reduce the maximum amount of change in Gate-voltage produced by deposited charges(Q_D).

- Resulting increases the minimum of critical charge(Q_C) which a cosmic ray must deposits in order to produce an SEU error.

Fig. 34a: D.C. Voltage Transfer Curves

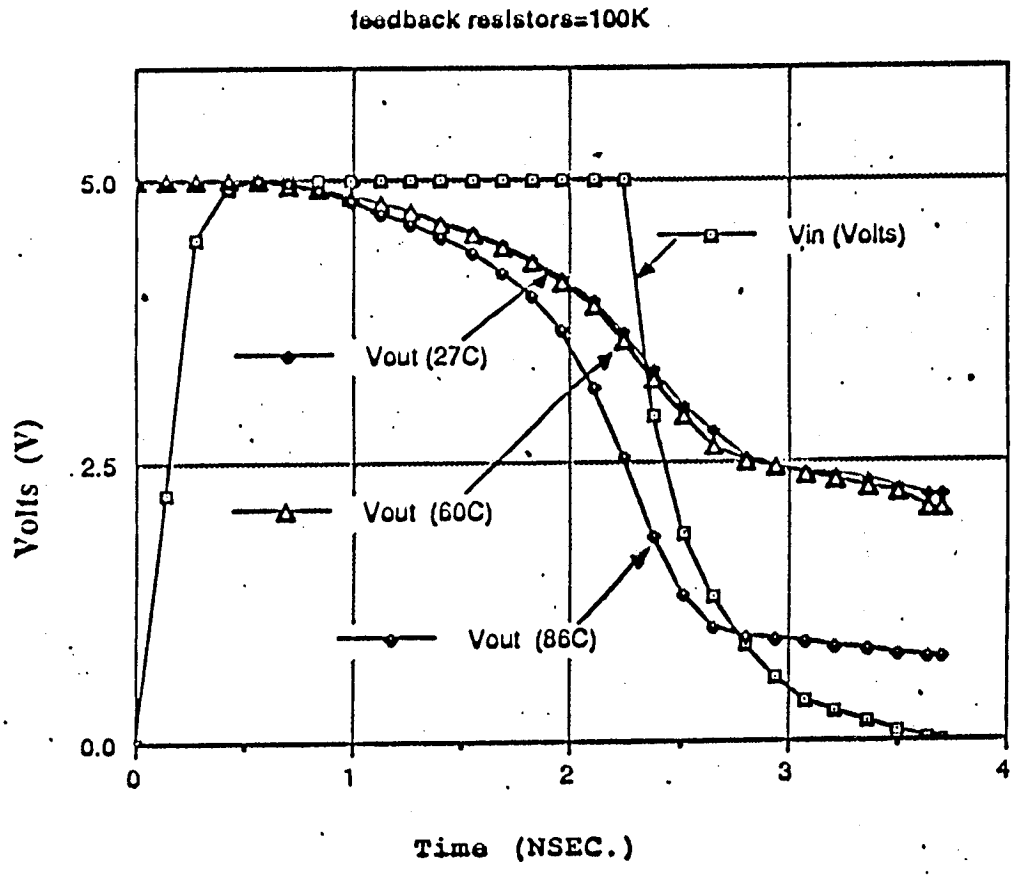


where

$B = \frac{\mu_n C_{ox}}{\mu_p C_{ox}} = \frac{\mu_n}{\mu_p}$.

Curve for TA670

Fig. 34b: Effect of Temp. on SEU



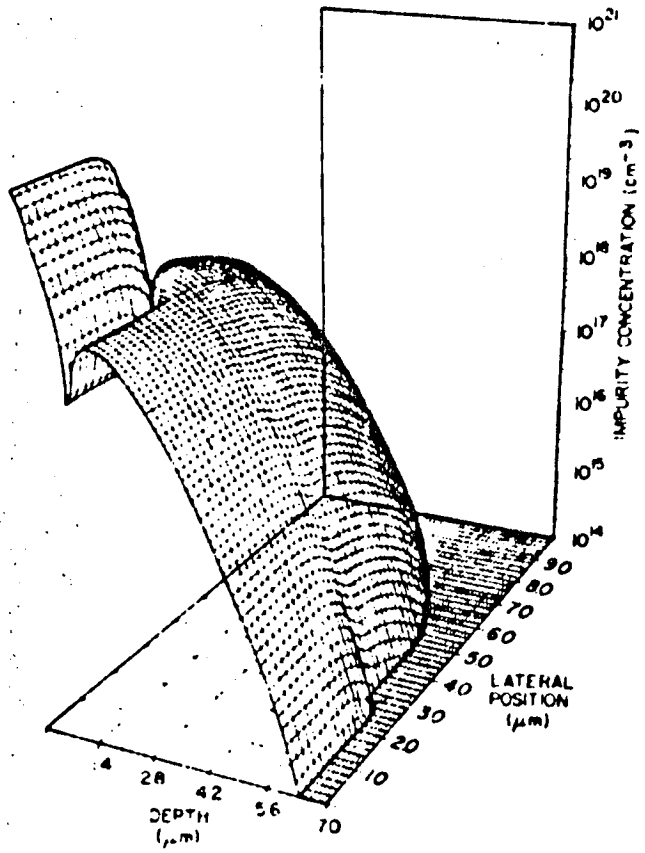


Fig.35: Final phosphorus and boron doping profiles.
Surface plot of the phosphorus boron impurity.

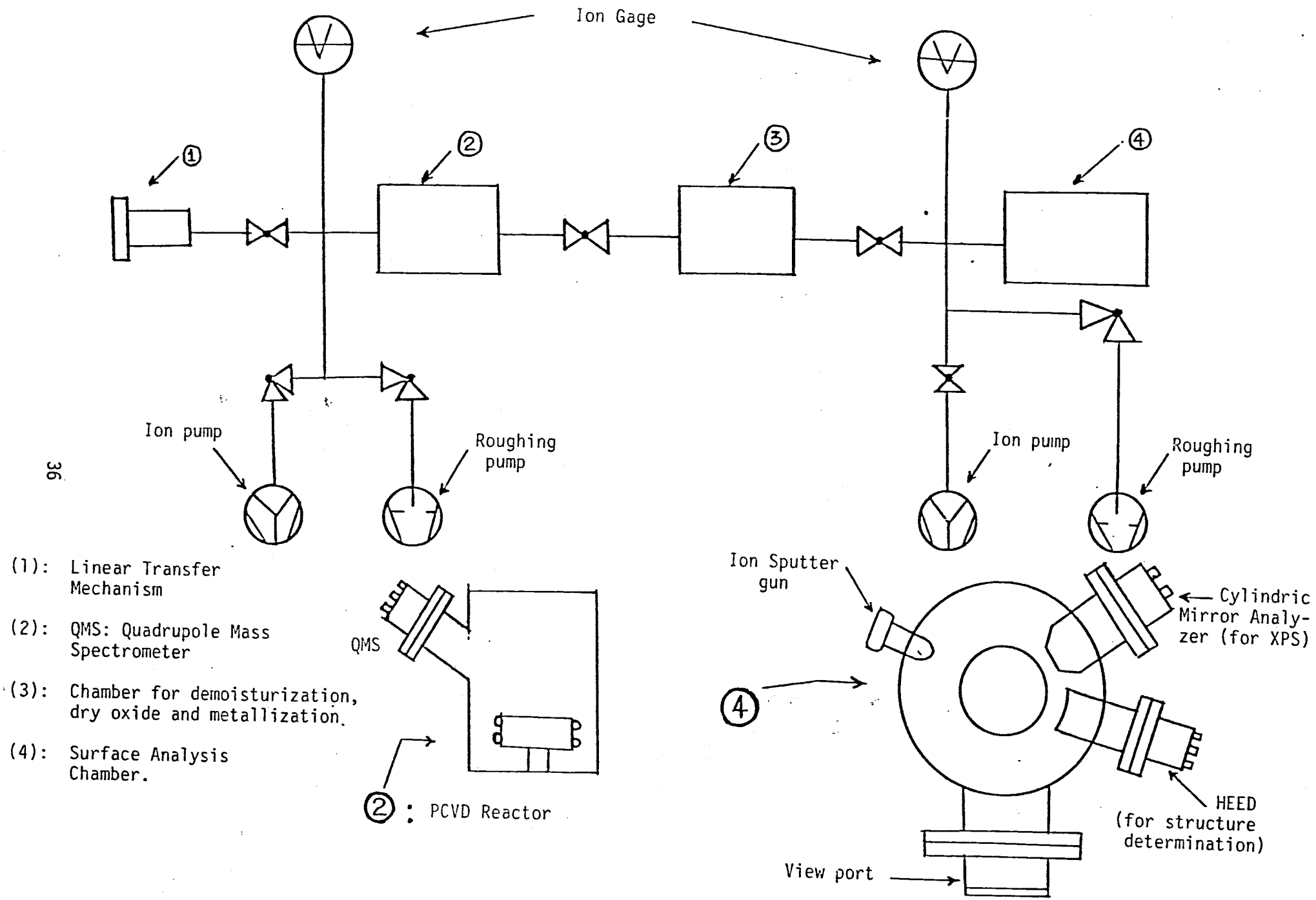


Fig. 36: Proposed experimental set-up for growth and analysis of amorphous Si.

Appendicies

APPENDIX i ABSTRACT SUMMARY NS_IEEE SUMMER '89

Single Event Upset & Total Dose Radiation Effects on Rad-Hard SRAMs

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E.G.Stassinopoulos****

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Radiation-hardened micro-geometry SRAMs were tested at the Brookhaven SEU Test Facility using the Twin Tandem Van de Graaff Heavy Ion Accelerator. These devices were fabricated by AT&T Bell Laboratories CMOS Twin-Tub IV--1 um--technology. Feedback polysilicon resistors were used to reduce SEU rate. A unique feature of this facility is laser optics for accurate device positioning into the beam. The devices were irradiated by 260 Mev Br-81 and 325 Mev Au-197 heavy ion beams. The effective LET equal to LET/cos θ was varied by variable angle of particle arrival θ. No failures were observed at room temperature up to the effective LET = 160 Mev*cm^2/mg with any value of the feedback resistors. The SEU cross-sections at elevated temperatures and with variable feedback resistors are pictured in Figs.1 and 2. The difference in threshold LET for 260 Mev Br-81 and 325 Mev Au-197 ions was probably caused by energy loss in the passivation layer. Considering LET vs Energy Curve for Si (14), a small decrease in E shows Br-81 gradually approaching a maximum. Therefore the LET of Br-81 remains relatively constant. But a similar Energy loss in Au-197 has already passed the maximum and is in region of steep decay, thus the expected LET reduction is significant. The LET threshold may be also affected by the bias voltage, 5.25 V in our experiment.

Density of interface states on PMOS and NMOS transistors fabricated by the same radiation-hardened process as the SRAMs were measured by the charge pumping, CV, and subthreshold methods. Results of the charge pumping measurement prior to irradiation are shown in Figs.3 and 4. Parametric shift due to the total dose of radiation is dependent on the dose rate, device bias, and post-radiation anneal. Total dose 1 Mrad(Si) of both 1-2 Mev protons and Cu K X-rays are examined. The parametric shift is expected to increase the SEU rate. Results of the device modeling including the variation of β-ratio, and SEU cross-section as a function of the feedback resistor value are compared to the experimental data.

APPENDIX ii ABSTRACT VA ACADEMY OF SCIENCE PRESENTATION

NATURAL SPACE RADIATION EFFECTS ON MATERIALS, DEVICES, AND SYSTEMS.T.N.Fogarty, V.Zajic, P.M.Kibuule, and C.Lowe, HAMPTON UNIVERSITY, HAMPTON, VA. 23668. Scaling down devices and systems has increased concern for SEU (soft errors) in VLSI. Spice and Crum simulation, and experimental results seem to confirm this. In this paper, the effect of total dose, rate, rebound phenomenon, and secondary radiation effects on materials, devices, and systems will be discussed. The effect of parametric degradation, due to prior total dose radiation, on SEU will be investigated at the new SEFG-SEU facility at BROOKHAVEN. (Supported by the Grants from NASA NAG 5-929)

APPENDIX iii ABSTRACT HUNTSVILLE NASA PRESENTATION

NASA-HBCU

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Principal Investigator(s) Demetrius D. Venable

Technical Monitor(s) E. G. Stassinopulos

Research Topic Effects of Ionizing Radiation on VLSI Electronic Devices

ABSTRACT

Abstracts including references should not exceed 300 words each. Use a separate form for each abstract submitted.

Earlier studies have revealed that scaled down SRAMS once exposed to charged particles are more susceptible to single event upset (SEU) because the critical charge decreases as the square of the feature size. The device parameters are affected by total dose radiation and dose rate. The density of interface states and oxide trapping play an important role in degradation and rebound Phenomena. This degradation will affect the SEU rate.

The efforts of our study is to explore ways of hardening data storage systems against SEU or soft errors. Charge pumping and Terman analysis of CV-IV data are compared for the evaluation of DIT as a function of energy. The test chips evaluated in DIT studies are from the same process lot as the SRAMS. Also, the role of decoupling resistors, and Beta Ratio are investigated. Final SEU tests are performed at the Brookhaven facility.

APPENDIX iv ABSTRACT SPACE STATION PARTICLE & WAVE WORKING GROUP NASA/JSC

Abstract No. 624

SIMULATION OF NATURAL SPACE RADIATION EFFECTS ON VLSI TECHNOLOGY

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**Prairie View A&M Univ.,Prairie View,Tx.

As space station was added to the NASA program, concern for the effect of low dose rate, relatively low energy particles and their secondary radiation over long exposure time has grown. With the increased compaction of design in VLSI systems concern for size effects has also increased. (1,2,3)

In this study(4) NMOS structures and equivalent CV test structures were submitted to one Mev. Proton and Electron radiation. Conventional parametric analysis using a HP-4145b as well as CV testing were applied before and after radiation. Considerable annealing immediately following removal from radiation.(within 3000 sec.) This is due to rapid hole transport. Even when the device is completely shielded from Protons by the(Kovar) encapsulation, secondary radiation including Fe,Ni,&Co Kα characteristic emmission causes considerable damage.(See fig 1&2) Normally after radiation the flatband voltage shifts in a negative direction. All components of Qss, Qot+Qf+Qit have positive charge.However if the device is biased to inversion negative charge is observed at the interface causing "REBOUND" of the Vfb. This confirms earlier work by Winokur et al(5) with Co 60 radiation.(fig.3)The Charge Pumping Technique allows determination of Dit, the density of interface states,in relation to the location in energy space. Thus it can be ascertained that one possible cause of negative charge is the filling of states in the upper half of the bandgap.(4a,b) Winokur (fig,5) also points out a dose rate dependence with timing failure more prevalent at lower dose rate.

Another aspect of the problem is the SEU, Single Event Upset, a non permanent bit flip caused by a charged particle passing through a critical region of a Mos SRAM changing from 0 to 1 or 1to 0 when Qcrit is reached. Diehl et al(8)have demonstrated that novel circuit design can eliminate SEU in SRAM, & Okyere has analized size effects in(fig.6) relation to SEU.(9) Because holding time, alpha particle & SEU are related in RAM the authors propose that those process variables such as the use of epi efficient gettering treatments will reduce stacking faults and also increase Alpha particle resistance.

While MOS-VLSI will account for large portion of Silicon device area used in space, amorphous aSI:H utilized in photovoltaic & display device may rival the area of single silicon used. Good photovoltaic aSi:H was deposited by Plasma Assisted LPCVD and submitted to 2 Mev Electron and Protons.Film is ascertained by ESR & IR before and after exposure to radiaton. (10,11) The ESR spin density has been related to dangling bonds in Amorphous Silicon. The IR adsorption in the region of wavenumber 2000 cm-1 is indicative of intrinsic aSi:H while the peak at 2070 is believed to be caused by microvoids. IR may be more sensitive to electron damage than spin density.

This work was partially supported by NASA NAS9-17136 and by SERI.

References:
1.Messinger,G.C.& ASH,M.S. The Effect of Radiation on Electronic Systems" Van Nostran Reinhold,published 1987.
2.Fogarty et al;Proceedings of NASA/Prairie View A&M Conference on Natural Space Rad. & VLSI Technology.To be published July 1987.
3.Sanderson,T.K;et al;"The Application of Californium 252 Fission Particles to SEU and Latch-up Testing in VLSI Device op.cit.2.
4.Diogu,K.K;et al;"Charge Anomoly at MOS Interfaces Submitted to 1Mev Proton Radiation"op.cit2.
5.Winokur,P.S;et al "CMOS Device Response and Failure Mechanisms in Space Satellite Environments"op.cit.
6.Cilingiroglu,U;"A General Model for Interface-Trap Charge Pumping Effects in MOS Devices"Solid State Electronics 28,1127,1985.
7.Groeseneken,G;et al;"A Reliable Approach to Charge-Pumping Measurements in MOS Transistors" IEEE Transactions on Electron Devices.ED-31,42, 1984.
8.Diehl,S.E;et al;"Error Analysis and Prevention of Cosmic Ion-Induced Soft-Errors in Static CMOS RAMS"IEEE Transactions on Nuclear Science,NS-29, 2032,1982.
9.Okyere,J.C;"Effect of Transistor Sizing on Circuits for Hardening CMOS SRAM Against Single Event Upsets"op.cit.2.
10.Roopwah,K;et al;"Properties of Glow-Discharge Intrim a-Si:H Submitted to 2Mev Proton and Electron Radiation"SERI Advanced Photovoltaic Conference.To be published Fall 1987.
11.Mahan,A.H;et al;"Evidence for Microstructure in Glow Discharge a-SiC:H Alloys" Proceedings of SERI PV.AR&D Conference,Denver,May 1986.

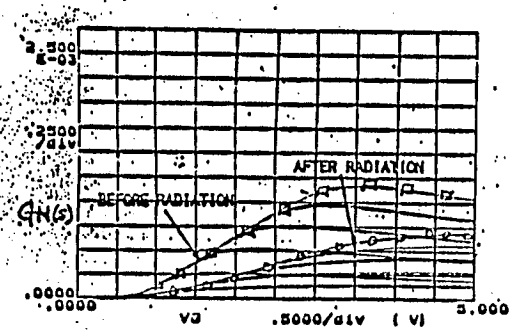

Figure 4: Transconductance versus gate voltage (Encapsulation off —Proton damage)

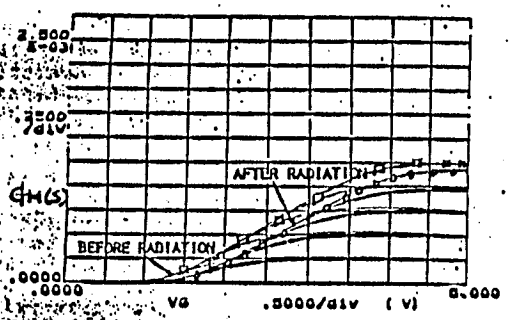

Figure 3. Transconductance versus gate voltage (Encapsulation on —Secondary radiation)

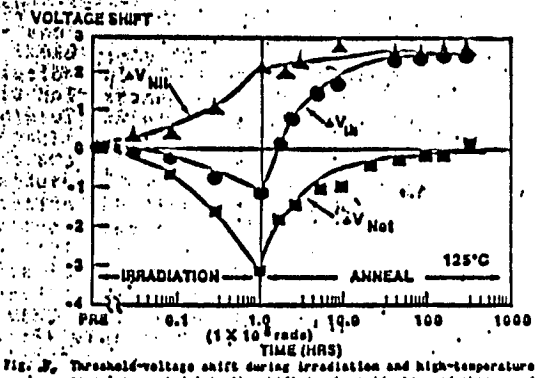

Fig. 5. Threshold-voltage shift during irradiation and high-temperature anneal separated into the shift due to oxide-trapped charge and interface traps. A 10-V bias was applied between gate and substrate during irradiation and anneal.

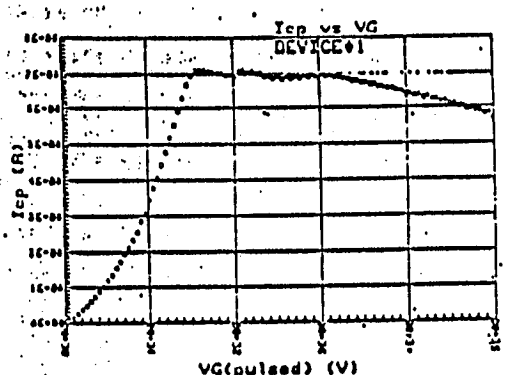

Figure 4:(a) Charge pumping current versus pulsed V_G before radiation

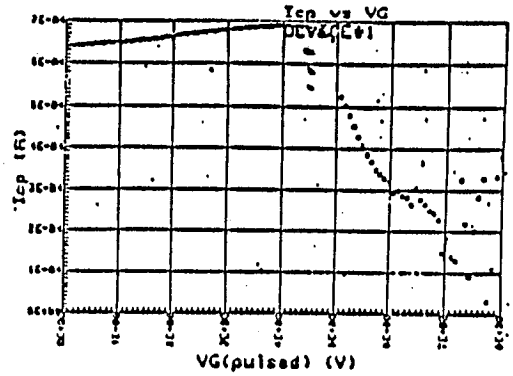

Figure 4: (b) Charge pumping current versus pulsed V_G after radiation

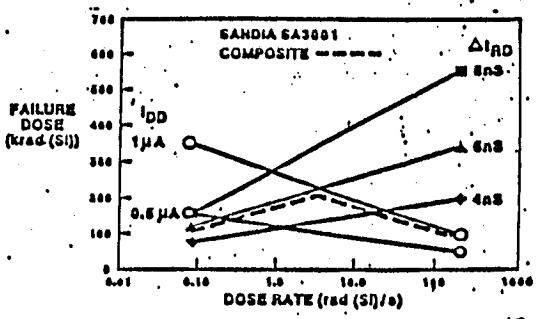

Fig. 4: Failure dose versus dose rate for Sandia SA3081 2K SRAMs.

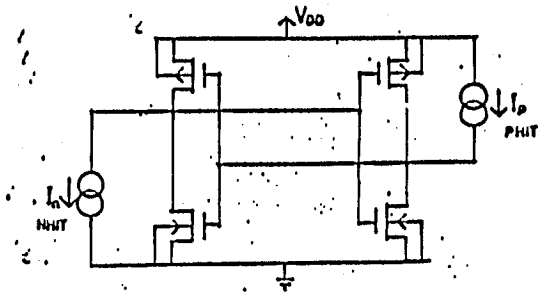

Fig.6 CURRENT SOURCE MODEL FOR PARTICLE HIT

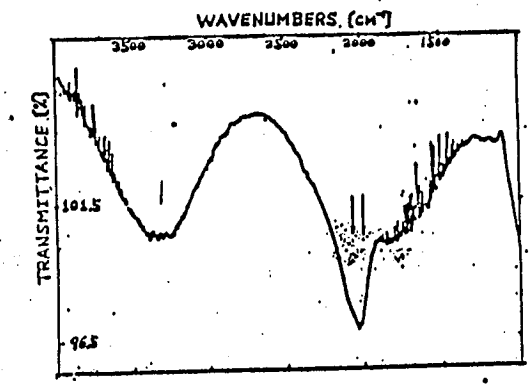

Fig.7 IR-Transmittance for a Good a-Si:H