Programmable Rate Modem Utilizing Digital Signal Processing Techniques

George K. Bunya and Robert L. Wallace

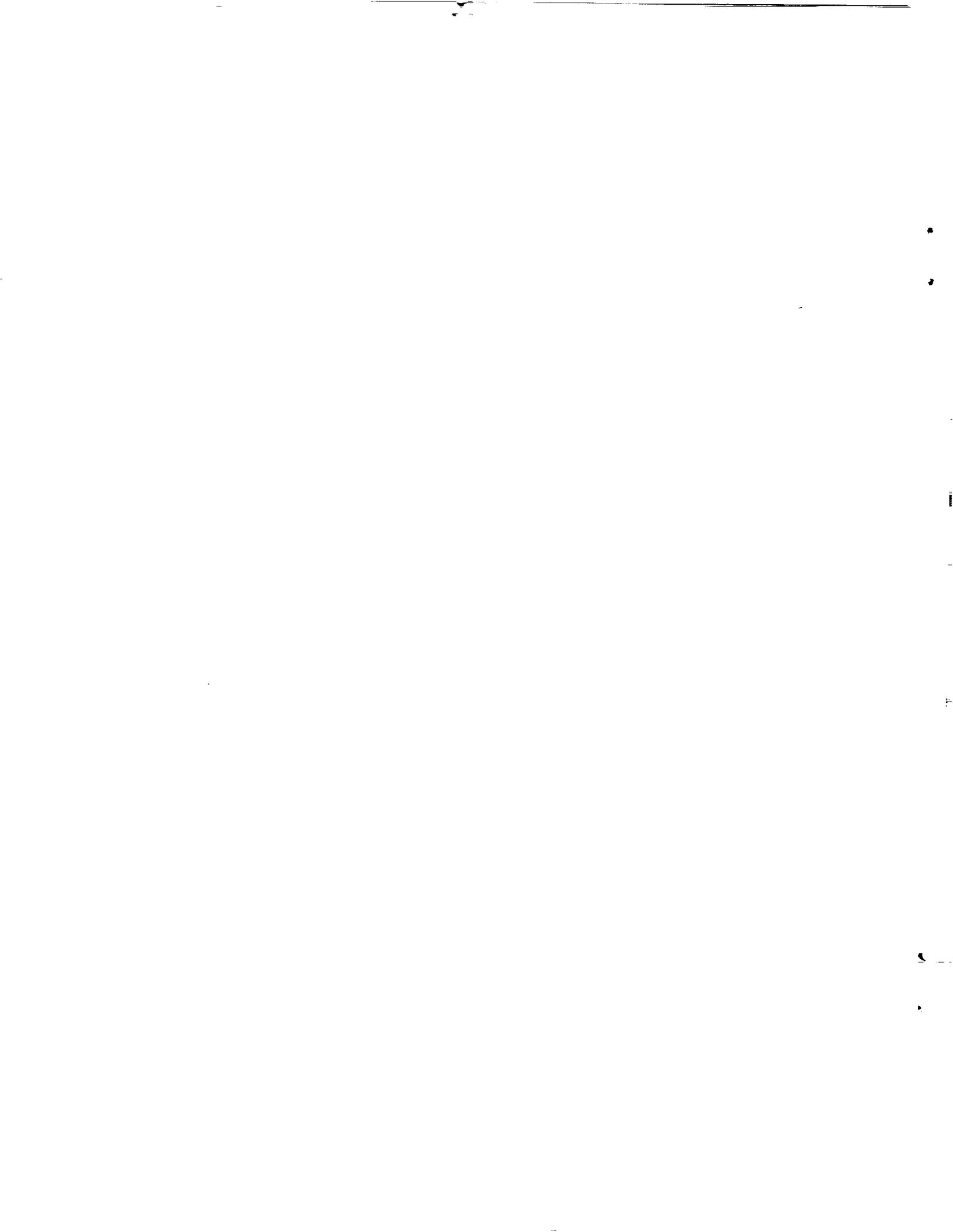*Multipoint Communications Corporation*
Sunnyvale, California

July 1989

NASA

National Aeronautics and
Space Administration

SUBJECT: PROGRAMMABLE RATE MODEM UTILIZING
DIGITAL SIGNAL PROCESSING TECHNIQUES
(SBIR-PHASE 1 Contract #NAS3-25336)

PROJECT SUMMARY

The engineering development study to follow was written to
address the need for a Programmable Rate Digital Satellite
Modem capable of supporting both burst and continuous
transmission modes with either BPSK or QPSK modulation. The
preferred implementation technique is an all digital one which
utilizes as much digital signal processing (DSP) as possible.
The majority of this report consists of outlining design
trade-off's in each portion of the modulator and demodulator
subsystem and of identifying viable circuit approaches which
are easily repeatable, have low implementation losses and have
low production costs.

The research involved for this study was divided into nine
technical papers, each addressing a significant region of
concern in a variable rate modem design. Trivial portions and
basic support logic designs surrounding the nine major modem
blocks were omitted. In brief, the nine topic areas were:
1) Transmit Data Filtering; 2) Transmit Clock Generation;
3) Carrier Synthesizer; 4) Receive AGC; 5) Receive Data
Filtering; 6) RF Oscillator Phase Noise; 7) Receive Carrier
Selectivity; 8) Carrier Recovery and 9) Timing Recovery. It
was the intent of each paper to address a specific modem issue
and to discuss and to examine techniques which effected the
choice of a viable circuit implementation approach. All of
these papers achieved this goal and have specific
recommendations on realizable circuit designs.

A programmable rate digital modem design operating in the burst
and the continuous mode has several potential applications in
the future of satellite communications. This modem or one
similar will be a vital part of the Next Generation VSAT-based
DAMA systems. Current and future international networks could
benefit from the design concepts here within. The proposed
modem would allow networks to utilize new and power advanced
satellite features such as those of the ACTS spacecraft.

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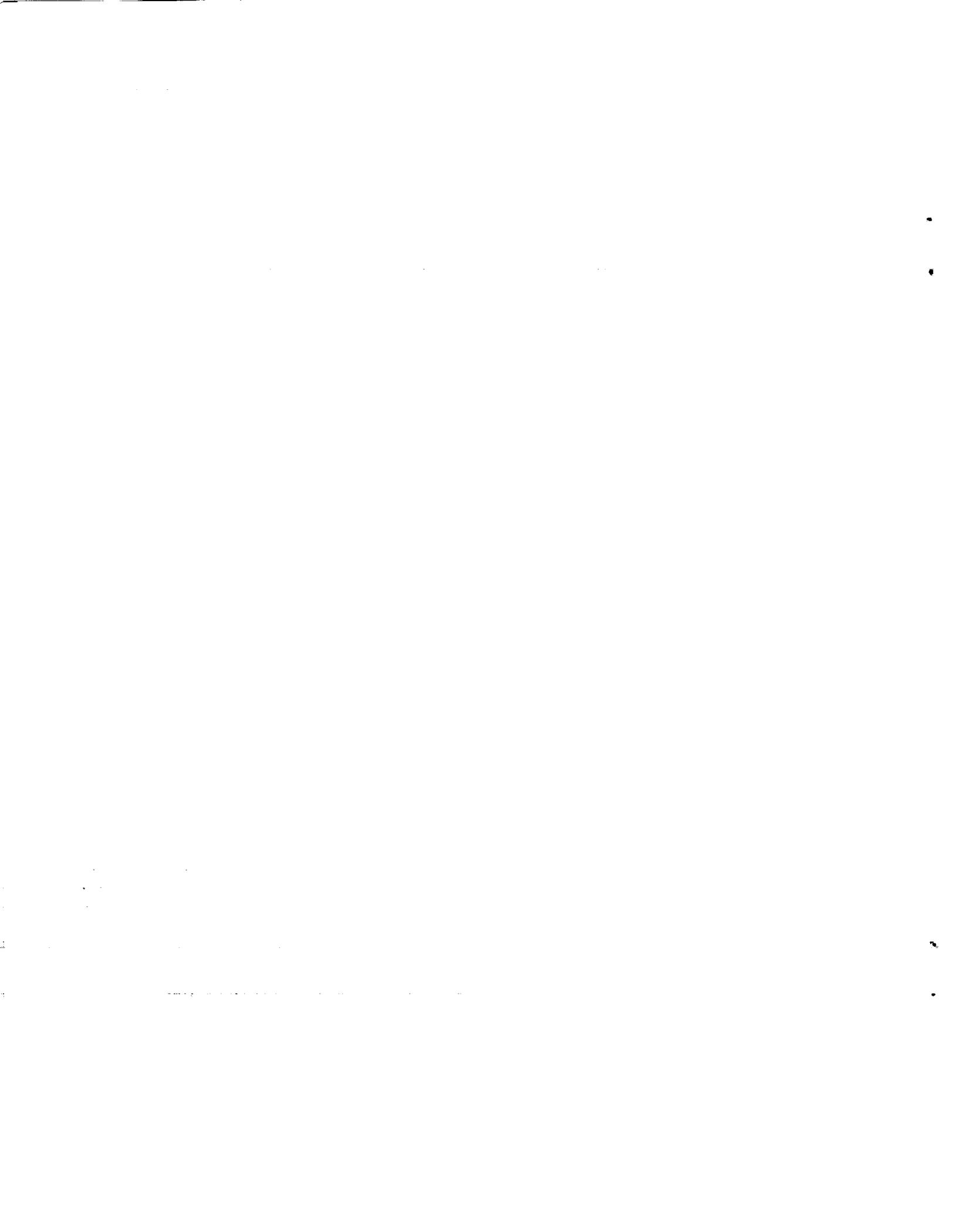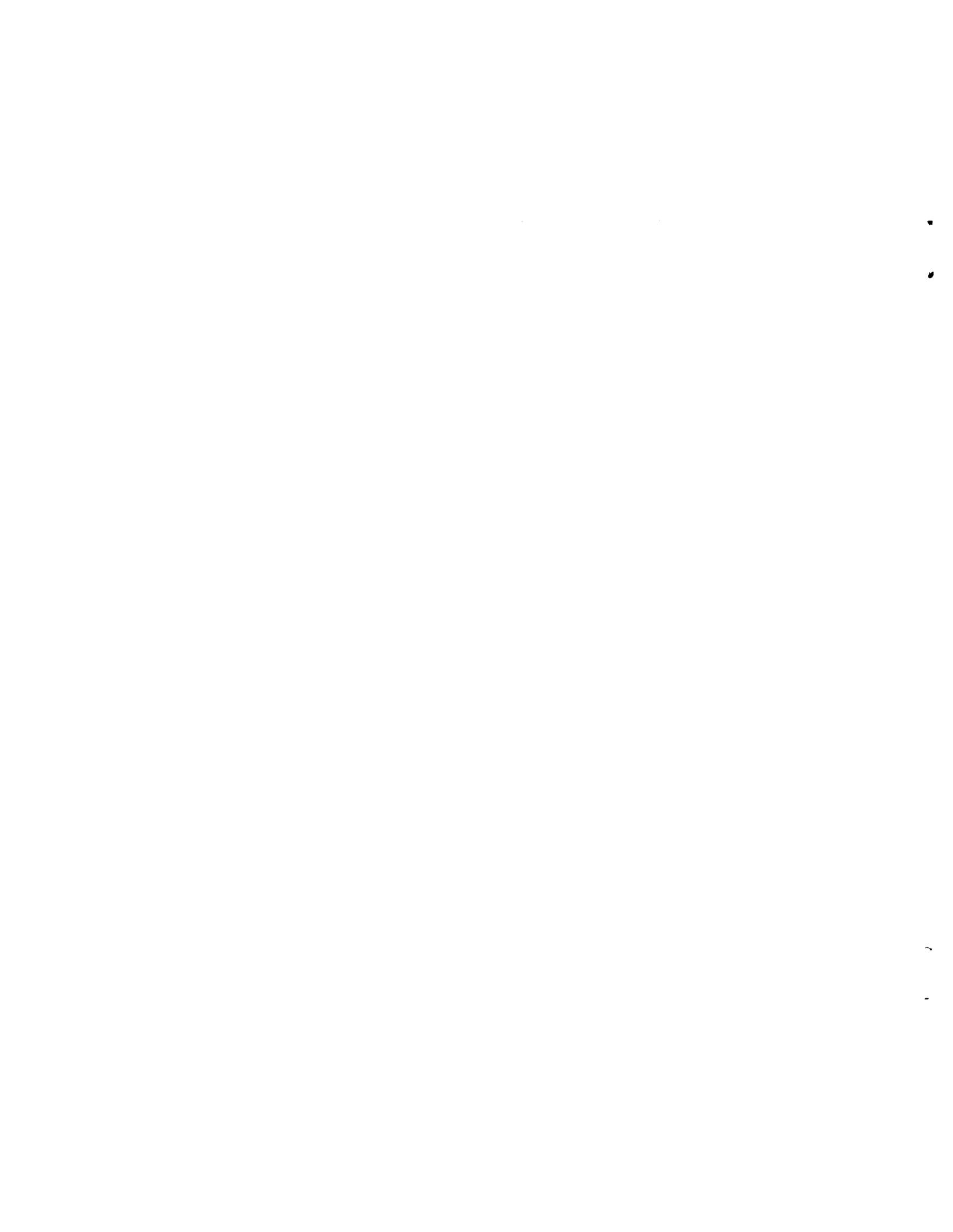Telex: 346352
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INTRODUCTION

The use of satellites has been and will continue to be a viable means of providing reliable communications needs between distant and remote sites. Today's satellites are more powerful and more sophisticated and those being developed are even more advanced than those of just a few years ago. To compliment this activity, the industry needs to design and to develop new highly integrated, reliable and cost effective digital satellite modems for earth station applications. New designs of modems should consider offering variable data rates (under software control), and multiple modulation schemes to support flexible networking alternatives which support integrated communications of data voice and facsimile. The goal of the following papers was to present currently available techniques and viable approaches towards the development of a truly Variable Rate Digital Satellite Modem capitalizing on digital signal processing implementation techniques.

The effort to follow is a collection of almost a dozen different papers or chapters. Each of these sections addresses a particular subject area by identifying salient requirements and critical considerations towards the implementation of a variable rate modem. The overall objectives of the study were the following:

- a) Determine the upper bound modem rate limitation using DSP techniques given current, cost-effective technology.

- b) Assess current new generation digital modem implementations and develop a robust programmable rate digital modem design which supports both burst and continuous modes of operation utilizing QPSK/BPSK modulation.

- c) Trade off practical, programmable digital filter and equalizer implementations for both the modulator and demodulator functions.

- d) Assess the minimum number and center frequency of intermediate carrier frequencies which support an agile, yet bit rate selective digital modem design in a shared transponder environment.

- e) Development of carrier and timing recovery networks which support fast acquisition and settling properties as well as low cycle skipping and precise phase alignment at low Eb/No's.

- f) Determine the spectral efficiency, bit error rate performance degradations, acquisition settling times of the proposed digital modem design in a multicarrier transponder environment.

v

g)   Assess the material cost, physical size and factory test alignment cost of the proposed digital modem design.

This Phase 1 study addresses the first five (a through e) objectives and left the remaining two objectives (f and g) for the Phase 2 portion of this study.

An important objective of this study was to assess the uppermost bit rate which the variable rate design could support. The initial thoughts were that the DSP baseband signal filters would be the determining issue. In fact, the first paper was written in this area to possibly identify an ultimate bit rate speed for the design. The result was one paper on Transmit DSP filtering but no evidence suggesting that this would be a limiting bit rate factor. In this paper, it was apparent that the greater the amount of filter selectivity the higher the clock rate of the design. However, when less spectral filtering is required, for the same data rate, the entire filter design can operate at a lower speed. This conflict between uppermost bit rate and the speed of the digital signal processing can be observed throughout all of the studies' papers.

In the Transmit and in the Receive digital filtering it was interesting to note that a continuum of data rates could be filtered. This is to say that once coefficients have been selected then these filters would operate at any frequency from dc to their maximum toggle rate. The restriction of "N" time 64KBPS is a result of the difficulties of transmit clock synthesis and of receive clock recovery.

The transmit clock synthesis paper describes the frequency limitations of producing clocks for the FIR filter which are "N" times faster than the incoming data rate. Beside creating the FIR clock, the clock synthesizer also considered the needs of supporting Forward Error Correction (FEC). The FEC clock is a fractional multiple of the input data clock. In the body of the paper several approaches are outlined but only one approach is capable of synthesizing both the FEC and the FIR clock and has the ability to instantaneously change clock rates. The reason for this importance is readily apparent in a burst modem scenario, which requires burst-to-burst data rate and FEC rate agility.

Besides burst-to-burst data rate agility, burst-to-burst carrier frequency agility should also be supported to allow networks to grow in capacity by using multiple carriers. Today, most commercially viable digital satellite modems are equipped with transmit and receive carrier synthesizers. In older satellites, the synthesizers needed to produce carriers across a 36 MHz wide range of frequencies which was centered at 70 MHz. Today's newer satellites support wider frequency transponders and thus have dictated higher IF frequencies.

Viable approaches must consider the ability to assist in synthesizing carrier frequencies from 104 to 176 MHz. Additionally, these synthesizers must be able to produce carrier spacing of 25 or 50 kilohertz with minimum phase noise degradation.
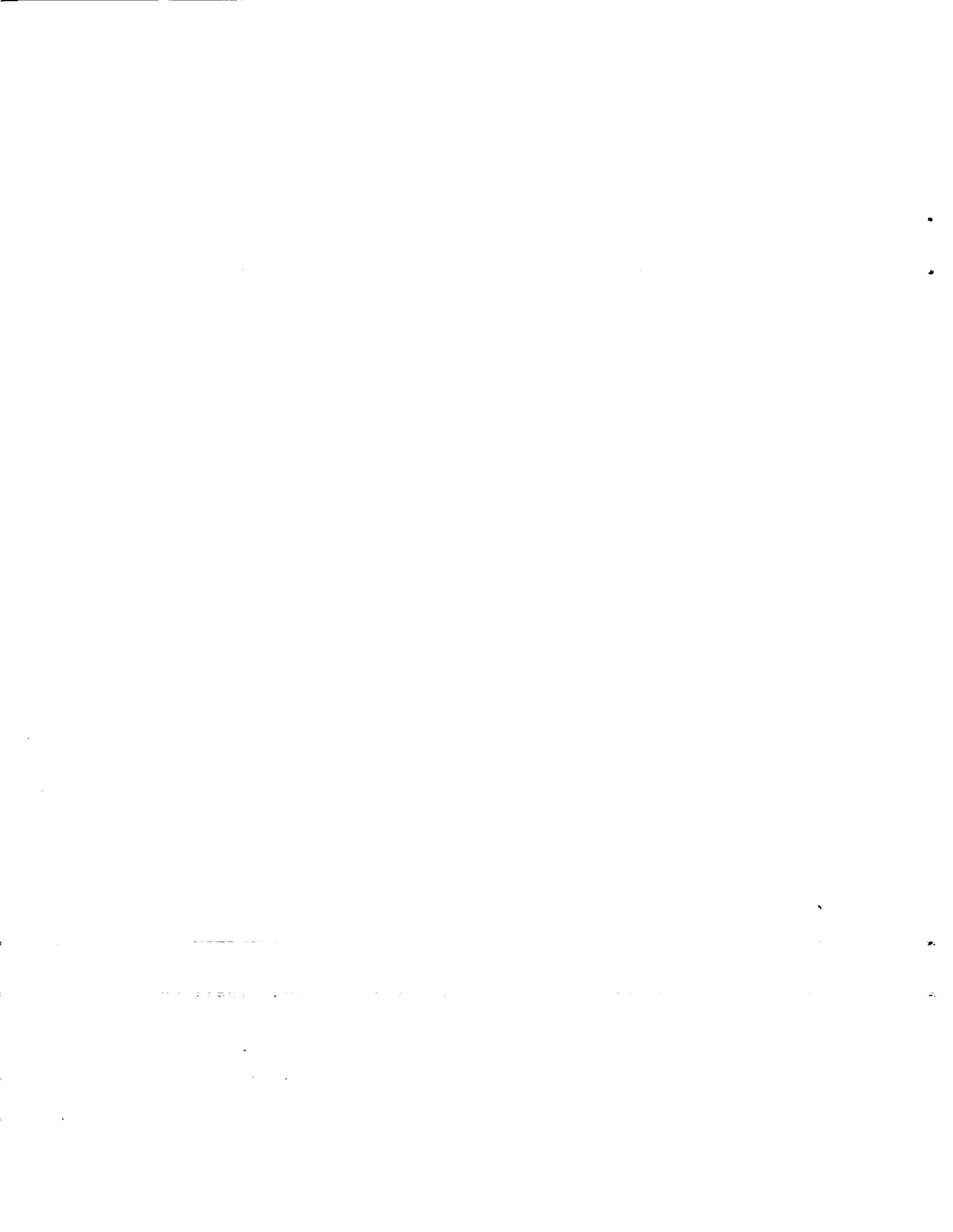
After the digital data has been modulated onto the synthesized carrier, it is uplinked to the satellite. The downlink signal received at the earth station will have time variant level variations. The study paper entitled, "Demodulator's Automatic Gain Control" discussed AGC issues as they apply to Burst and Continuous modes of operation. The AGC circuit is responsible for removing all signal level variations. Constant signal levels are critical for optimum demodulation performance especially in the carrier and bit timing recovery circuits and data detection areas.

Following the paper on AGC there are three papers which address and discuss the important topics related to carrier recovery and optimum demodulation. Without a doubt, the carrier recovery approach and its performance has the greatest overall effect on the modem's architecture and response in a noisy environment. One critical issue that the study addressed is that of the effects of carrier phase noise on digital transmission methods. This effort relates to the determination of a lower data rate transmission limit. Another topic researched was the methodology of carrier selective filtering and its impact on the number of receive side carrier frequency conversions. Here the ramifications of mixer intermodulation products and pass band filter selectivity issues were analyzed. Also addressed are the constraints governing the choice of common intermediate frequencies which support variable data rates in both I.F. bands.

The last paper associated with carrier recovery characterized and described the pro's and con's of several common carrier recovery schemes. The approaches examined were pilot tone, inverse modulator, X "N" multiplier, costas loop and many form of data directed loops.

To finish up the study, timing recovery techniques and their performance attributes is examined. The discussion identifies the various types of timing recovery techniques and their operational characteristics. Based upon this comparison process, a candidate scheme is selected. Implementation suggestions for this technique are also shown.

We conclude this Phase 1 SBIR Study with proposed finalized block diagrams of the Variable Data Rate Modulator and Variable Data Rate Demodulator.

MEMORANDUM

TO: NASA Modem Study File   DATE: May 25, 1988

FROM: George K. Bunya   MCC FILE MCC-93

SUBJECT: TRANSMIT DSP DATA FILTERS - FILE NUMBER (NASA TX1.DSP)

- -

The primary objective of the NASA study contract is to assess
currently available techniques and viable approaches towards the
development of a truly variable rate digital satellite modem. After a
quick survey of current modem vendors, it is apparent that no one has
a variable rate modem. Although one vendor does currently offer a
satellite modem with three independent data rates. But these data
rates must be specified at the time of product procurement. It is
obvious that two parameters which elude designers of variable rate
modem are the transmit and receive data filters.

Currently available digital modems sidestep the issues associated with
variable rate filter by offering factory tuned plug-in filters. It is
the intent of the author to surface and to discuss a viable approach
to a continuously variable transmit date rate filter.

FREQUENCY DOMAIN FILTERING

In general there are two basic signal filtering approaches. The first
approach is classical signal filtering in the frequency domain. This
approach uses frequency differentiation to attenuate undesired
frequency components. This approach encompasses the following types
of filters.

        Frequency Domain Signal Filter types:

            1)   Active Op-Amp Filters
            2)   L & C Classical Filters
            3)   Ceramic Filters
            4)   Crystal Filters
            5)   SAW (Surface Acoustical Wave) Filters
            6)   Others

Of the five named frequency domain filters three of them, namely
Ceramic, Crystal, and SAW filter types are fixed in bandwidth and thus
not viable for a variable rate modem. The remaining two, Active
Op-Amps and L & C Filters, can be made to change their bandwidths.
However for either type, the best that these filters can tune, cost
effectively, is probably an octive. With this knowledge, one realizes
that one must search elsewhere for a truly variable rate signal
filter.

TIME DOMAIN FILTERING

The second approach to signal filtering is the time domain method. A time domain filter is in reality a computational process in which a digital word is accepted and transformed into another digital word. Like the frequency domain approach this approach encompasses several different types.

Time Domain Signal Filter types:

1) Switched Capacitor Filters
2) Computational Filters
   a) Infinite Impulse Response Filters
   b) Finite Impulse Response Filters
3) Others

Of the two types named, the Switched capacitor filter type is currently viable for data rates up to 100 Kilo-Hertz and thus is not practical for this study. The second general type, the Computational filter is a technique known since the early 1950's but until the recent fruition of VLSI technology this approach was not cost effective.

Computational filters, or DSP (Digital Signal Processor) as they are popularly known, are mathematical devices. These devices accept a digital word as input, then mathematically manipulate (process) the word to produce another digital word as a output. The filter uses the simple mathematics of multiplication and of addition to produce its digital output. In order to produce a variable rate data filter, using this approach, requires only an increase or a decrease in the speed of the mathematics. Thus using a Computation filter is the only viable approach to a truly variable rate data filter.

TRANSMIT DATA SIGNAL FILTERS

An important consideration in the design of any type of filtering is the environment in which these filters must operate. For the NASA study, the transmission medium requires matched transmit and receive data filtering. Furthermore, the cost of satellite bandwidth dictates designs utilizing Nyquist shaping filters with bandwidth efficient alpha factors.

In consideration of the filter's operating environment and of the NASA study goals', a four point criteria guides the following development. The first criterion requires that the data filtering implementation must be capable of filtering over a continuously variable set of frequencies, thus a continuous set of data bandwidths. Secondly the approach must allow Nyquist channel filtering with various alpha factors (excess bandwidths). The third criterion being that the filters must provide more than 50 dBc suppression of out of band frequency components. With the final criterion being that the approach consider cost effectiveness.

The Transmit filter hardware implementation selected to address the goals of the NASA study was a time invariant FIR (Finite Impulse

Response) digital filter. This is the only approach examined which
will achieve the goal of being capable of variable data rate
filtering. The basic structure of the digital filter will consist of
three general blocks. Figure 1, "Transmit Data Filter Block Diagram"
graphically reveals the basic architecture.

The first hardware block in the transmit data filter is the Sequencer.
This block accepts transmit digital data and clock while outputting
control words to the computational filter at a rate "M" times faster.
The second block, the actual computational filter, processes the
control word to produce a "N" bit wide filtered word. The filtered
binary weighted word can have different alpha factors based on the
process that occurs in this block. The filtered word then becomes the
input to the third hardware block, a DAC (Digital to Analog
Converter). It is in this block that the mathematics ends and a
filtered analog signal is developed which is the ultimate goal of the
filter.

```
                        control word
        ------------------        ------------------        ----------
       |                  |      |                  |      |          |
       |  Sequencer  |      |   Computational  |  "N" | DAC  |
Data   |                  |      |                  | bits |          |
       |                  |------|    Filter        |--/---|      |-- O/P
Clock  |                  |      |                  |      |          |
       |                  |      |                  |      |          |
        ------------------        ------------------        ----------
              -- x"M" ->
```
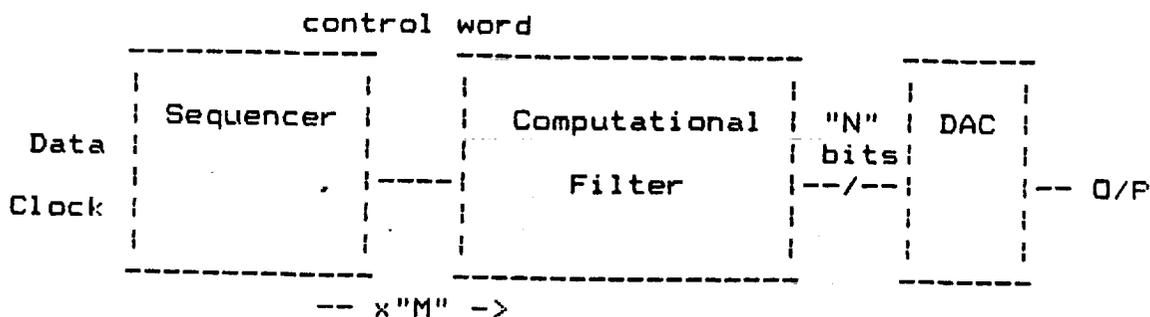
Figure 1. Transmit Data Filter Block Diagram

It is important to note that the computational filter operates at several times the speed of the incoming data to be filtered. Thus this means that somehow a "M" times faster clock must be generated on the transmitter. Additionally, this implies that the conversion rate of the DAC must be several times faster than the actual data rate and it is in this device that one will find the limiting, speed to cost, factor in the filter design.

From a cursory look at the current status of DAC and for that matter ADC (Analog to Digital Converter) there appears to be an explosion of technology growth in these devices. Both the speed and quantization levels are steadily increasing while the cost of these devices continue to fall. Hopefully another paper will be done which adequately addresses the cost penalty, as a design trade off, for more quantization levels.

Referring back to Figure 1, "Transmit Data Filter Block Diagram", there remains three all important parameter which need to be evaluated. These three parameters will ultimately define the overall performance of the digital filter. The three parameters are the number of samples per symbol ("M"), the quantization level ("N") and the FIR coefficient weightings. It is now my intent to discuss two of the three parameters, namely the number of samples per symbols and the quantization levels. I'll leave the actual determination of the coefficient weighting to a NASA Phase II contract.

Table 1. S/N Ratios Verses Quantization Levels

Quantization (Binary (Weighted)	Unique Levels	Voltage Resolution 1V = Full Scale	S/N Ratio Theoretical (in dB)
4	16	62.5 mV	24.1
6	64	15.6 mV	36.1
8	256	3.9 mV	48.2
9	512	1.9 mV	54.2
10	1,024	977 uV	60.2
12	4,096	244 uV	72.2
14	16,385	61 uV	84.3
16	65,536	15 uV	96.3

DAC QUANTIZATION LEVEL

The purpose of Table 1 "S/N Ratios Verses Quantization Level", was to identify the number of quantization levels to achieve a certain degree of out of band signal suppression. In general, more quantization levels, the greater potential signal to noise ratio. However this increase in quantization levels also relates directly to a greater cost for the overall design. Therefore the designer wishes to select a DAC which can meet his potential S/N requirement but not more, in order to be most cost effective.

From Table 1 it is apparent that theoretically in order to achieve a 50 dBc signal to noise ratio that the design must utilize a 9-bit or more binary weighted DAC. Currently most DAC's are available in even numbered inputs and in general they accept from 4 to 16 binary weighted input bits. Because of these considerations the transmit DSP filter design will be based on an architecture of a 10 or more bit wide filter word.

Note: The best DAC found to date, which meets the requirements of clock speed and of word size is 'Analog Devices' AD568 part. It is capable of a full scale transition in 11 nsec (high slew rate) and it is cost effective (about $35.00). Also it is capable of settling to within .025% in 35 nsec, which translates to a bandwidth of about 28 MHz.

SAMPLES PER SYMBOL

Table 1 gave us a handle on the number of required quantization bits, next let us consider how many samples per symbol are necessary to achieve our design goals. This number is extremely important because it and the conversion speed of the DAC will ultimately determine the uppermost speed at which the transmit digital DSP filter will operate.

The solution to this problem is not as straight forward as was the solution for the quantization levels. The reason for this difficulty lies in the realization that there is still one variable in the equation which we need to define. To digress for a moment, in the time domain a simple square wave is represented by an infinite series of harmonics in the frequency domain. Continuing, signals that are smeered in the time domain usually separate in the frequency domain and visa versa. What I'm trying to say is that in order to have sharp frequency domain separation, you need more time domain samples and visa versa. Therefore, in order to have a smaller excess bandwidth or Alpha factor the filter design must accordingly grow in samples per symbols. Stated again, in the frequency domain the sharper the desired slope at the cut-off frequency (alpha => 0) the greater the number of time domain coefficients required.

$$\text{\# of coefficients} \times \text{alpha factor} = \text{constant}$$

And, in fact, Nicholas Loy, author of "An Engineer's Guide to FIR Digital Filters" states, "For a FIR filter with virtually no ripple in the pass band and approximately -50 dB attenuation in the stop band, the number of coefficients required can be estimated by the following formula".

$$NC = 3.5 \times NT \times E(0.5) \times TWx(-1)$$

where NC = the number of coefficients in the FIR filter
       NT = the number of transitions in the frequency domain
       TW = the normalized frequency transition width (alpha/2)

Table 2. Number of FIR Coefficients Verses Alpha Factor

Classical Alpha Factor	Normalized Transition Width	Number of Coefficients	Coefficients Phase Linear Requirement
1.0	.5	7.0	7
.9	.45	7.8	9
.8	.4	8.8	9
.7	.35	10.0	11
.6	.3	11.7	13
.5	.25	14.0	15
.4	.2	17.5	19
.3	.15	23.3	25
.2	.1	35.0	35
.1	.05	70.0	71

It is apparent by the data tabulated in Table 2, that as more restrictions are placed on the amount of excess bandwidth the DSP filter design must be capable of many more coefficients. It should be noted that Table 2 above is only an estimation and that depending on the values of the coefficients selected and the quantization level of the design that these estimates may need to be increased.

SUMMARY

The primary objective of the NASA study contract is to assess currently available techniques and viable approaches towards the development of a truly variable digital satellite modem. After a quick survey of current modem vendors, it is apparent that no one has a variable rate modem. It is obvious that two parameters which elude designers of variable rate modem are the transmit and receive data filters. It was the intent of the author to surface and to discuss a viable approach to a continuously variable transmit date rate filter.

The reasons to select a time domain FIR digital filter were discussed and an architecture was outlined. The architecture was composed of three main blocks: the Sequencer, the Computational Filter and the

DAC. Next calculations showed that in order to achieve 50 dB
attenuation in the stop-band, the DAC was required to quantize 9-bits
or more. Following which the required number of FIR coefficients was
estimated. Finally, it was noted that the coefficient selected for
the FIR weights may cause either the number of samples per symbol or
the required quantization to increase.

MEMORANDUM

TO: NASA Modem Study File   DATE: July 8, 1988

FROM: George K. Bunya   MCC FILE MCC-93

SUBJECT: TRANSMIT CLOCK SYNTHESIS - File Number (NASATX.DSP)

- -

ABSTRACT

Any digital modem which incorporates digital filtering requires
designing a transmit clock synthesis circuit. This circuit is
responsible for producing a "N" times multiple of the input clock is
used in the Finite Impluse Response (FIR) digital filter to band limit
the transmit spectrum. Additionally, since this proposed modem is to
operate in the harsh environment of satellites the addition of Forward
Error Correction (FEC) coding should be considered in the design of
the clock circuit. The FEC clock is a fractional multiple of the
input data clock. Ultimately, this means that the transmit modulator
must develop two high speed clocks from the incoming data clock.
Continuing to strive towards the development of a truly variable rate
digital modem many clocking schemes were considered by only a few were
realizable. Of the clocking schemes considered, four of the approaches
have been examined below. These approaches discussed below are 1)
Diode Multiplication, 2) Frequency Domain Synthesis, 3) Multiloop
Synthesizers, and 4) Direct Numerical Synthesis.

DISCUSSIONS

Before examining the four clock synthesis approaches it is important
to identify the types and the groups of frequencies which need to be
synthesized. With this knowledge, the interested reader will better
understand some of the constraints and the problems associated with
the synthesis. To begin, the clock circuit must consider synthesizing
not one but two types of frequencies. The first frequency type would
be utilized by the FEC coder to insert redundancy information. The
second frequency type is required by the FIR filter to band limit the
modulated signal.

The FEC clock is a fractional multiple of the input clock. The
proposed satellite modem will be designed to except the common FEC
overhead rates of 1 (no FEC), 1/2, 3/4, and 7/8. This relates to the
design of a circuit with the ability of creating four unique clocking
groups for each different input clock rate. If true digital filtering
is implemented in this modem then the clock circuit must be capable of
generating these frequencies to take full advantage of the design.
For example, for a constant input data rate, the modem will be able to
increase the FEC redundancy rate by expanding the transmission rate.
This feature aids in combatting fading and improving link bit error
rate (BER), by using more coding gain and keeping the data throughput

2-1

constant. Using this technique of expanding in bandwidth, a system's designer will have a new degree of freedom in link budget calculations and thus in the design of networks.

The FIR digital filter clock is an integer multiple of the FEC clock. In general for the same input data rate, the smaller the allowed transmission bandwidth is, the higher the FIR clock must be. In a previous memo (NASATX1.DSP), it was estimated that for excess bandwidths of 1.0 > Alpha > 0.4, the required number of samples per symbol should be between 7 and 19. Therefore this clocking circuit needs to be capable of outputting 5 or 6 different FIR clock rates for every FEC clocking rate.

After the above comments it is apparent that the Transmit clock synthesizer must be capable of creating many unique frequencies in order to take full advantage of the modem's digital filtering. The proposed transmit clock circuit will support the four different FEC rates and the six different FIR rates. To support these rates the transmit clock circuit will be capable of creating 24 unique clocking frequencies for each input data rate. With the intent of designing a circuit to fulfill the above requirements several methodologies were considered like, Diode Multiplication, Frequency Domain Synthesis, Multiloop Synthesizers, and Direct Numerical Synthesis.

TRANSMIT CLOCKING METHODOLOGIES

1.   Diode Multiplication

In this method, the incoming clock is non-linearly multiplied to a "N" times harmonic. The harmonic is filtered with an analog filter and then this harmonic is divided down to the required clock frequencies for the FEC and FIR clocks.

Pros: This method is extremely quick and easy to understand. It is also cost effective.

Cons: Since this method requires analog filtering of the appropriate input clock harmonic, it is inappropriate for a variable rate modem. Figure 1, "Diode Multiplication", represents the general block diagram of this approach.

```
                              Data Rate
                               unique

                 ------------    ----------    ------------
                | Diode     |   | Analog   |  |            |
                |Multiplier |   | Filter   |  | Final      |->FIR Clock
       I/P      |           |   |   of     |  | Dividers   |
     Clock ->|  or any   |-->|  "N"     |---->|          |
                |Nonlinear  |   |          |  |            |
                | Device    |   |Harmonic  |  |            |->FEC Clock
                 ------------    ----------    ------------
```

Figure 1.   Diode Multiplication

2-2
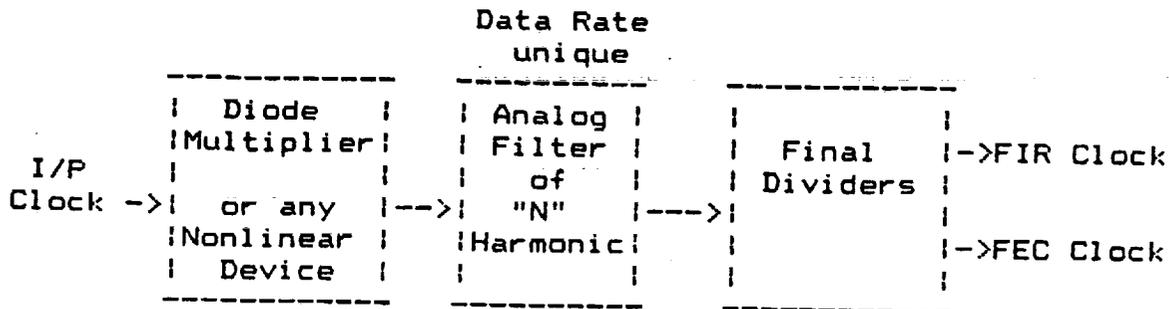
2. Frequency Domain Synthesis

A technique based on a stable set of references. Using addition, subtraction and division of these references other useful frequencies can be synthesized. Also required is a set of analog filters to remove unwanted frequencies.

Pros: Able to synthesize many frequencies.
Cons: Greater frequency resolution is costly. Many spurious frequency components to filter. May be slow to change frequencies, depends on frequency resolution (due to analog filtering). Difficult to phase lock to the input clock.

```
 ------------        ----------        -----------
|            |      |          |      |           |
|  Matrix    |-->|  Matrix    |-->|  Matrix    |-------->FIR Clock
|   of       |    |   of       |    |   of       |          |
|  Dividers  |<--|  Adders    |<--|  Analog    |      ----------
|            |    |            |    |  Filters   |     |          |
 ------------        ----------        -----------     | Divder   |
      |                                                |          |
 ------------        ----------        -----------
|            |      |  Analog  |                            |
| Oscillator |      |  Switch  |                          -->FEC Clock
|            |      |  control |
 ------------       |  circuit |
                     ----------
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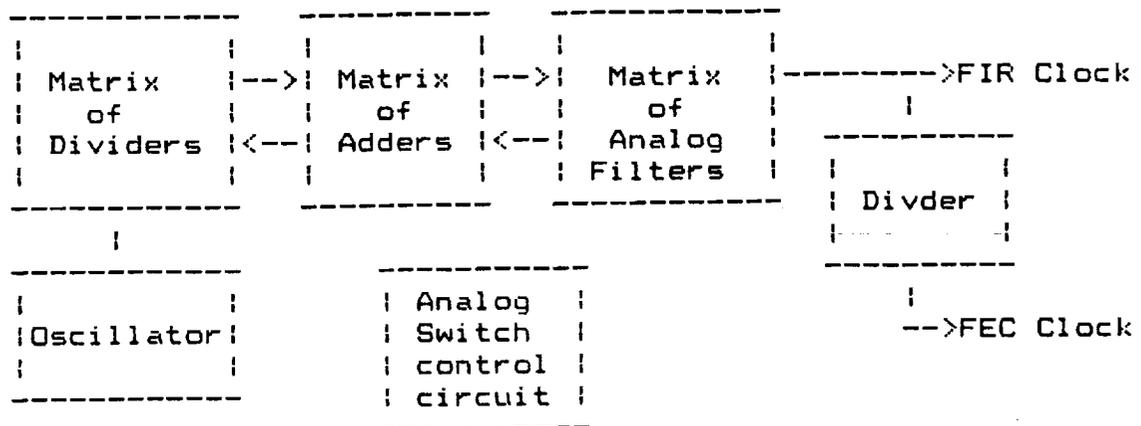
Figure 2. Frequency Domain Synthesis

3. Multiloop Synthesizer

In this method of generating fractional and higher multiples of the incoming clock there are several approaches. After considering several, a dual loop approach was examined at the best candidate. This is a classical method to synthesize small frequency step sizes and obtain the greatest spectral purity.

Pros: The method is well understood. It produces small step sizes and is spectrally clean. Has the ability to phase lock to the incoming clock and is cost effective.

Cons: Since this type of synthesizer is a phase-locked loop, the rate of new frequency synthesis is determined by the H (s) and thus will be rather slow for the frequency step size this modem requires.

2-3

```
  --------            --------            --------            --------
 :   1    :          :      :  :        :  :      :         :    1   :
 :   -    :->       ( PD ) ->:  H(s)  :--:  VCO   :------>:  -    :->FIR Clock
 :   N1   :          :      :  :        :  :      :         :    M1  :
  --------            --------            --------            --------
     ^                   ^                --------
     :                   :               :   1    :
                                         :   -    :<-:        --------
  --------    --------------------       :   N2   :  :       :    1   :
 :        :                              --------   :------>:  -    :->FEC Clock
 :  VCXO  :                              --------   :        :    M2  :
 :        :                             :   1    :  :         --------
  --------    --------                  :   -    :<-:
     ^       :      :  :      <- (PD) <-:   N3   :<--
     :-----: :  H(s) :<-       --------
              --------         --------
                    ^         :   1    :
                    :         :   -    :<--------- Input clock
                    :-----:   :   N4   :
                              --------
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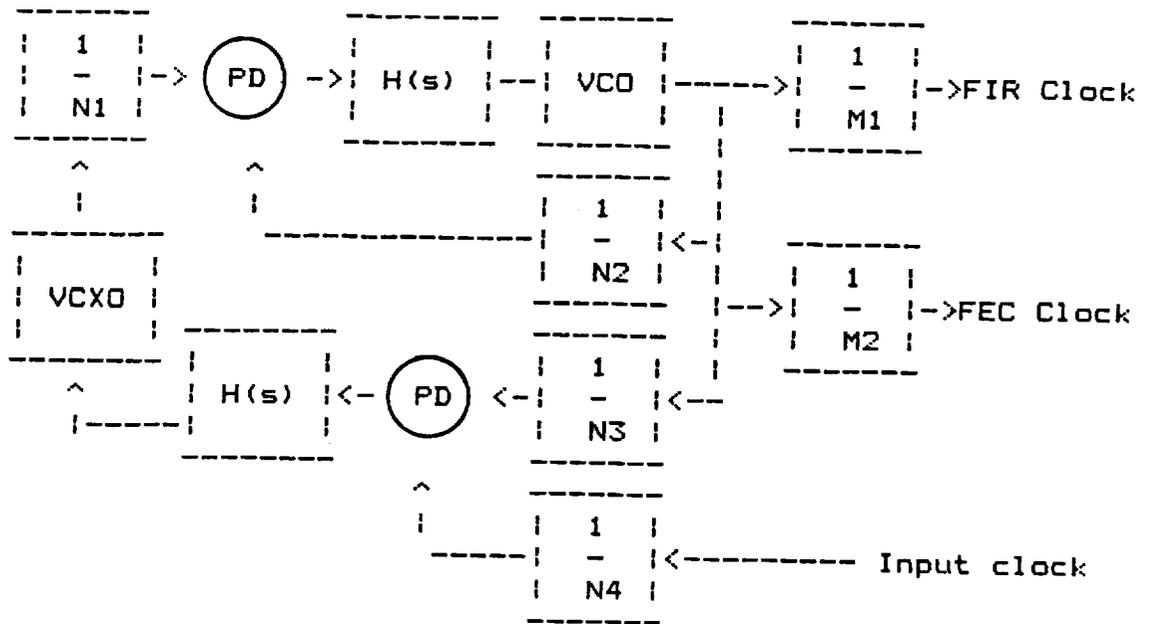
Figure 3. Multiloop Synthesizer

4. Direct Numerical Synthesis

In this approach a sinusoidal waveform is generated with a Read Only Memory (ROM), a phase register and a high speed DAC. The method reconstructs a time domain representation of a sine wave from the ROM table and creates the waveform in the DAC.

```
                --------        --------
               :        :      :        :
               :  ROM   :      :  DAC   :
            -->:Look-up :--->:  :        :----------->FIR Clock
               : Table  :      :        :   :
               :        :      :        :   :
                --------        --------    :
  -------------------------------        :  V
 :                              :        --------
 :     --------    --------     :       :        :
 :    :       :   :        :    :       : Divider :
 -->: Adder  :   : Phase   :    :        --------
 -->:       :->:register :--    :          :
 :   --------    --------       :          ----->FEC Clock
 :                   ^
 Control Word        :       --------
                     :      :        :
                     ----: VCXO   :
                            :        :
                             --------
```
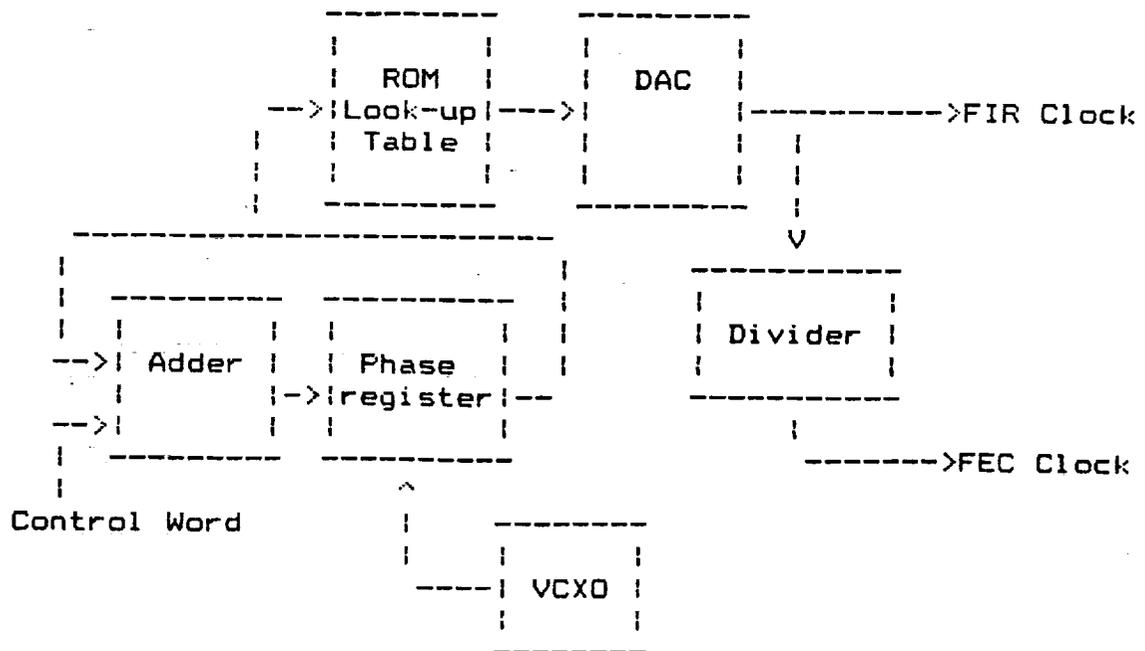
Figure 4. Direct Numerical Synthesis

The frequency of the waveform is changed by the speed at which the phase register is incremented.

Pros: This method is capable of synthesizing all required frequencies. This is the fastest method for changing the clock rates and will support burst to burst data rate changes. Also the approach will allow phase-locking to the incoming data clock and is of moderate cost.

Cons: This method is difficult to understand and may have some spurious response to combat.

Direct Numerical Synthesis is a technique known for years but it was not until the recent advancements in VLSI that density and complexity levels were reached to make this approach cost effective. Additionally, there are currently available several commercial products capable of synthesizing frequencies in the 100's of Megahertz's using this technique. This is, arguable, the best candidate for transmit clock synthesis for developing the FEC and the FIR clocks.

SUMMARY

Any digital modem which incorporates digital filtering requires designing a transmit clock synthesis circuit. For this modem, the digital filtering is to be done in a FIR (Finite Impulse Response) which requires a "N" time multiple of the input clock. Additionally because this modem will operate in the harsh environment of satellites, the transmit clock circuit should also consider synthesizing a FEC (Forward Error Correction) clock, so that redundancy information can be inserted. Therefore the transmit clock synthesis circuit must synthesize two frequencies.

For the transmit clock synthesis four approaches were examined in this paper. The approaches were Diode Multiplication, Frequency Domain Synthesis, Multiloop Synthesizers and Direct Numerical Synthesis. Each approach was briefly outlined and some of the pros and cons were identified. Diode Multiplication is not a candidate for a variable rate modem because it requires a data rate unique filter for each synthesis. Frequency Domain Synthesis is not cost effective and it is difficult to phase-lock the multiple oscillators to the incoming clock. Multiloop Synthesizer is a viable candidate yet it is limited in its ability to change frequencies on a burst to burst basis. The final approach examined, Direct Numerical Synthesis, is another viable candidate and has the ability to instantaneously change clock rates. The results of this paper indicate that Direct Numerical Synthesis has merit and is the best choice for the Transmit clock synthesis.

MEMORANDUM

TO: NASA Modem Study File   DATE: August 31, 1988

FROM: George K. Bunya   MCC FILE MCC-93

SUBJECT: CARRIER SYNTHESIZER - FILE NUMBER (NASACS.PLL)

- -

ABSTRACT

A modem operating in a shared satellite transponder environment needs
to have the capability to change its carrier frequency. This
capability is required in case the satellite bandwidth is reallocated.
Changing carrier frequencies is normally accomplished by one of two
means, either by exchanging fixed crystal oscillators or by frequency
synthesis. Today frequency synthesis is the accepted standard. This
paper will discuss important aspects of carrier frequency synthesis as
they relate to the design of a variable rate satellite modem design.

BACKGROUND

The purpose of this study is to investigate and to identify viable and
cost effective approaches toward the development of a truly variable
rate digital satellite modem. Towards achieving this goal, carrier
frequency synthesis is proposed and is required in this modem. And in
fact, the majority of satellite modem vendors provide methodologies for
changing their modem's carrier frequency. This ability to change
carrier frequencies is important because if a carrier frequency is
unavailable or if the bandwidth of a transponder must be reallocated
then an operating modem will be required to alter its carrier
frequency. This paper will discuss important aspects of carrier
frequency synthesis as they relate to the design of a variable rate
satellite modem. The topics to be discussed are: agility verses
tunability, possible implementation techniques and technical issues.

RADIO FREQUENCY VERSES INTERMEDIATE FREQUENCY TUNABILITY

For a variable rate modem design, when considering carrier frequency
synthesis there are several design decisions. One decision is where
the frequency synthesis is implemented. It can occur in the Radio
Frequency (RF) terminal or it can occur in the modem at the
Intermediate Frequency (IF). To the satellite, both approaches produce
identical results, which is a modulated spectrum at a particular RF
carrier frequency. In the past, system's engineers have implemented
one or the other and sometimes both approaches in the same radio link.
Because of the higher cost of working in the RF arena, carrier
synthesis will be more cost effectively accomplished at IF. This is
done by designing carrier synthesis as an integral part of the modem.

DUAL CONVERSION

Another consideration is the method of modulating the carrier
frequency. The simplest method is to directly modulate the desired IF
carrier. In this method the filtered baseband signal is mixed directly
onto the desired carrier and the modulation is complete. A second
method, known as dual conversion, uses a two step approach. In the
first step the filtered baseband signal is modulated onto a fixed
carrier, then in a second step an IF synthesizer is used to frequency
translate the modulated spectrum to a particular carrier frequency.
Figure 1 reveals the modulation process known as dual conversion.
Notice that this method requires an additional mixer and oscillator,
however it does have advantages over the direct modulation method. One
practical advantage is that for QPSK the circuitry to create a
quadrature LO need only to operate at one frequency, therefore the
quadrature can be ideal.

```
Digital :           :                           :          :  Modulated
   data :   FIR     :                           : Analog   :     IF
 ----->:  filter    :--->( X )--->( X )--->: filter   :-------->
       :            :     ^          ^        :  BPF     :
       :            :     :          :        :          :

            : Fixed :  :     :       IF       :
            :  OSC  :--     : Carrier         :
            :       :   :   : Synthesizer     :
```
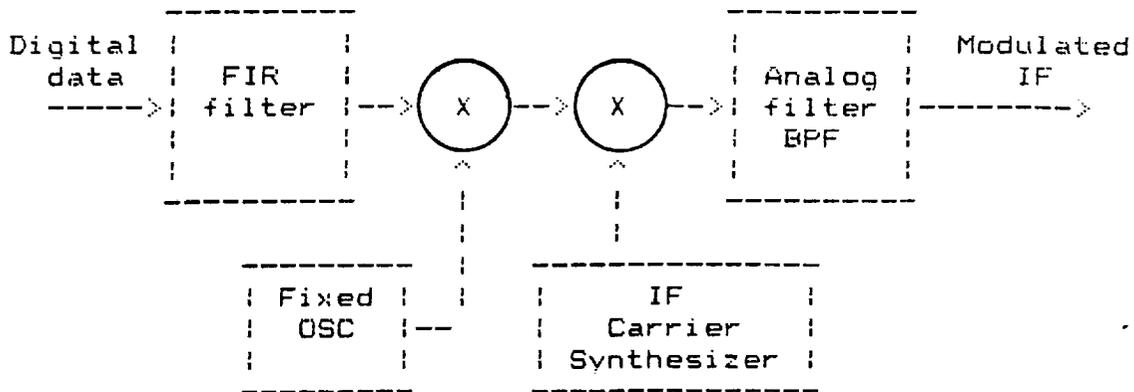
Figure 1.   Dual Conversion Frequency Modulation

In the demodulator, the same dual conversion principle can be utilized to gain frequency agility but allow the critical carrier and bit timing recovery circuits to process at a single carrier frequency. The job of the receive carrier synthesizer is to provide the proper LO frequency to downconvert a desire carrier to a common IF frequency, this is the reverse process of the modulator synthesizer. With the transmit and receive carrier synthesizer implemented in this manner, carrier agility is achieved with minimum effects to the critical circuits of the modem.

FREQUENCY AGILITY VERSES TUNABILITY

Today many modem manufacturers advertise that their modems are carrier agile, this may be true for a continuous modem or a burst modem which rarely changes frequency. For a burst modem which must receive and transmit on different carrier frequencies on a burst to burst basis, the term agility takes on a new meaning. In essence the majority of modem vendors have had "tunable" carrier frequency modems, where an operator may adjust his carrier frequency through dip switches or thumb wheel dials to effectively tune the modem to operate at a different carrier. Now, in terms of this burst modem technology, true carrier agility is the capability to do signal processing on different carriers on a burst to burst basis. With this definition many modem vendors could not advertise their modems as carrier agile.

The four implementation techniques mentioned below all call be configured to yield carrier agile designs. After considering the complexity and cost to implement each approach, it will be recommended that carrier synthesis be implemented as a digital phase-locked loop, in both the modulator and the demodulator.

IMPLEMENTATION TECHNIQUES

The goal of this variable rate modem is to design a carrier frequency synthesizer which will allow this modem to be truly frequency agile. Common frequency synthesizer implementation techniques include:

    a)   Direct Frequency Synthesis
    b)   Direct Digital Synthesis
    c)   Phase-Locked Loops
    d)   Combinations of the above

These techniques were described in detail in a previous memo (File Number Nasa TX.Clk). Many of the comments made in that memo apply here as well, although the final recommendation is different. After considering some of the technical issues, like the minimum carrier spacing, the required frequency range and the phase noise requirements resulted in a recommendation of a Digital Phase-locked Loop approach to carrier synthesis.

TECHNICAL ISSUES

When designing Carrier Synthesis for a digital satellite modem, there are technical issues which when considered will determine the best circuit solution. A synthesizer design for a variable rate modem should address issues like: the range of output frequencies, the minimum carrier spacing, the rate at which it must change frequencies

and the requirements of phase noise and of spurious responses. Upon examining these technical issues, a recommendation of a Digital Phase-locked Loop approach is made.

° Range of Output Frequencies

In satellite communications there are two standard modem interface frequency bands. They are centered at 70 and 140 MHz. For satellites currently operating in the C-band (4 - 6 GHz) the general standard IF interface occurs in the frequency band of 70 ± 18 MHz. Those satellites operating in the Ku-band (12 - 14 GHz) have a standard IF bandwidth of 140 ± 36 MHz. Any proposed carrier synthesizer approach must be capable of frequency synthesis in both bands. Here one should note that presently an approach utilizing a Numerical Controlled Oscillator which was proposed for the transmit clock synthesis must be ruled out, due to the high frequency range required for the synthesis.

° Minimum Carrier Spacing

The frequency resolution of the synthesizer design will equal the minimum carrier spacing. In general there are three design goals in selecting a target resolution. They are the satellite transponder translation uncertainty, the carrier stacking efficiency and of course cost.

In the past, Intelsat has specified that over the lifetime of a satellite the worst case satellite translation uncertainty will be ±43 KHz. Today's modern satellites have less frequency uncertainty. Therefore a modem which does not want to be restricted in its usage must have a carrier recovery technique to remove this broad uncertainty. Thus it does not make sense to have a carrier synthesizer with smaller resolution. For example, a 19.2 Kbps modem which operates in the worst case translation can not be stacked any closer than the uncertainty, otherwise a demodulator could acquire the wrong carrier.

A second factor in selecting a frequency resolution for the synthesizer is the stacking efficiency. For data rates which occupy bandwidths greater than the satellite translation uncertainty, large step sizes equate to potential wasted satellite bandwidth. For example, a QPSK 64 Kbps data rate which occupies 64 KHz of bandwidth, and a carrier synthesizer which has 100 KHz step sizes wastes 36 KHz of bandwidth for each additional like carrier. This second factor seems to indicate that small step sizes are worthwhile. However the third factor, the cost reveals that for any and all synthesizer approaches the greater the resolution, the greater the cost to implement. Therefore in a compromise solution 25 KHz was selected as the frequency resolution which is approximately one quarter that of the satellite translation error.

° Phase Noise and Spurious Requirements

Every oscillator in the satellite link, (modulator's synthesizer LO, the earth stations up and down converters, the satellite frequency translator, the demodulator's synthesizer LO and the demodulator's

carrier recovery oscillator) has its own characteristic phase noise. Each time the modulated spectrum is translated by one of these oscillators additional phase noise is added. In the receiver's carrier recovery process, the effective noise bandwidth must be large enough to track and to remove some of this phase noise for a non-degraded coherent bit detection performance. On the otherhand, to diverge for a moment, the effective noise bandwidth should be small to prevent thermal noise degradations.

Regardless of the carrier recovery bandwidth, what is apparent is that there is an ultimate noise floor which when crossed results in performance degradation. Because the transmit and the receive carrier synthesizers are part of the satellite link their phase noise must be controlled. Several authors have explored and have reported the effects of various degrees of phase noise on coherent bit detection. As a result of these effects, the Intelsat organization has specified a phase noise mask for their satellite links which pass digitally modulated data. Figure 1, Continuous Single Sideband Phase Noise Requirement, is from the Intelsat IESS-308 (Rev. 3) document. Previous work by this author has shown that digital phase-locked loops can be built to be at least 10 decibels better in phase noise response than this specification.

Besides phase noise, spurious responses can have a negative effect on coherent bit detection. By definition, spurious responses are coherent tones which are produced by an oscillator. These tones, at their worst, can steal carrier power and can appear as in-band adjacent carrier interferers which will lower the performance of the satellite link.

SUMMARY

For digital satellite modems, the ability to operate over a wide range of frequencies is often achieved by the incorporation of an IF carrier synthesizer in both the transmitter and in the receiver. This feature allows the modem operating in a shared transponder to quickly change its carrier frequency. Furthermore, if designed so, the synthesizer can offer burst to burst carrier agility.

In the design of a variable rate satellite modem, it was recommended that an IF carrier synthesizer be designed in both the transmitter and the receiver. Also it was mentioned that dual conversion in both the modulator and in the demodulator has performance advantages over direct modulation. This was followed by discussions on three technical issues. First the two most common interface frequency ranges were mentioned: the 70 ± 18 MHz and the 140 ± 36 MHz. Secondly, the minimum carrier resolution was identified to be 25 KHz. Finally, the deleterious effects of phase noise and of spurious responses were explained.
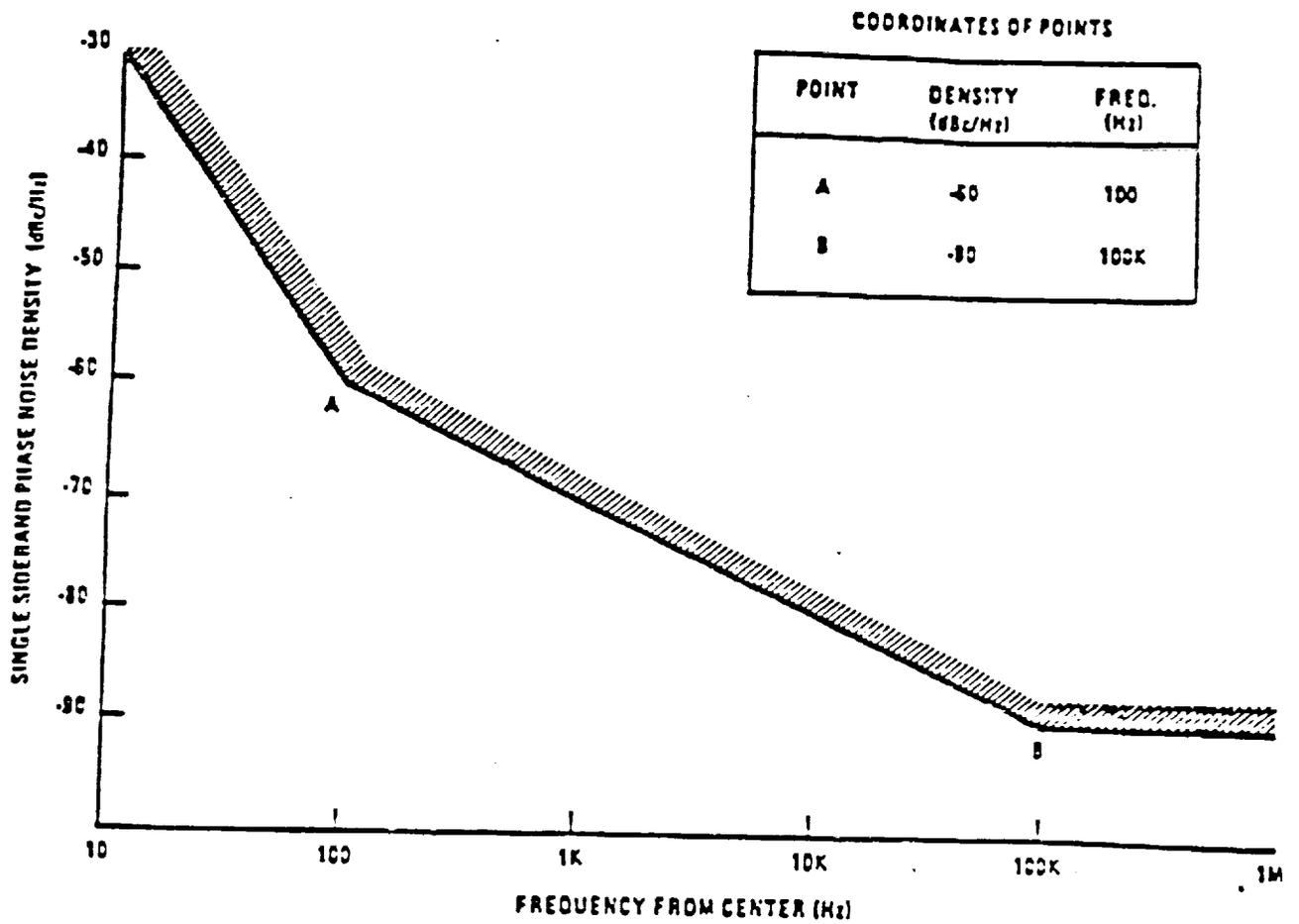
Figure 2

CONTINUOUS SINGLE SIDEBAND PHASE NOISE REQUIREMENT
(for carriers with information rates less than or equal to 2.048 Mbn/s)

★ The transmitted phase noise requirement may be satisfied by meeting either of two limits (See Section 2.1). The above phase noise density requirement is mandatory only in the case that Limit 1 has been selected by the earth station applicant, and only in the case of the transmit earth station.

multipoint communications corp.

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MEMORANDUM

TO: NASA Modem Study File   DATE: September 15, 1988

FROM: George K. Bunya   MCC FILE MCC-93

SUBJECT: DEMODULATOR's AUTOMATIC GAIN CONTROL (NASA Rx 3.AGC)

- -

ABSTRACT

The input of a receiver must be designed with sufficient gain to properly amplify the weakest signal that it wishes to demodulate. For optimum demodulation at the lowest possible Eb/No levels the carrier and bit timing recovery circuits, within modern satellite receivers, require nearly constant input signal level. The performance of these circuits may be effected by as little as a few tenths of a decibel level change. Even a satellite link (the path from the modulator through the satellite and into the demodulator) once properly configured will experience a path attenuation variations of 5 or 6 decibels (due to rain fading). The incorporation of an Automatic Gain Control (AGC) circuit will prevent these events from causing an outage of service due to loss of carrier or of bit timing. Furthermore an AGC circuit will ease field installation requirements and compensate for path variations due to aging circuits. The purpose of this paper is to discuss AGC circuit issues as they apply to a Burst and a Continuous mode digital satellite receiver.

BACKGROUND

Nearly all modern day receivers have some type of Automatic Gain Control (AGC) circuitry to remove any level variations present at their input. From a system's point of view the circuit should consider two types of gain variations. One type, dynamic, is related to the operation of a Burst mode receiver where the AGC must quickly level an incoming IF burst, hold the level for proper demodulation and then just as quickly aid in disabling demodulation as the signal ends. A second type, static, are those variations which are experienced by the receiver as amplifiers age, or as transmit power is adjusted or when the receiver is installed.

In addition to coping with the dynamic and the static input signal variations, an AGC circuit must be capable of properly amplifying the received signal with minimum distortions. One type of common amplifier distortion, noise figure, must be carefully considered. This distortion if left unchecked can actually lower the input signal quality. This paper will discuss system level and circuit level design considerations as well as three commonly used AGC circuit implementation techniques.

AGC CONSIDERATIONS

° Fast AGC

The vast majority of satellite modems operate in a continuous fashion
or mode. In these modems a modulated signal is continuously available
in the receiver for the AGC circuit to monitor. Therefore these AGC
circuits can derive their amplitude control information by examining
tens of thousands of symbols. Using this information in a feedback
loop allows these circuits to optimally level their incoming IF
signals.

Even though these are the vast majority, there does exist a second
group of satellite modems. They are known as burst modems, burst
modems quickly turn on, broadcast its site's data and then just as
quickly turn off. Burst modems are more difficult to design than
continuous modems. Normally burst type modems are used so that many
different transmitting sites can share the same RF carrier frequency.
Sometimes these bursts event for a burst modem may be over in less than
a thousand symbols, therefore the AGC circuit must be re-thought and
re-designed to respond in a matter of tens of symbols.

° AGC Range

An AGC circuit which operates over large variations in gain must have
the ability to fully amplify the smallest signals while at the same
time the ability to reduce its gain to accommodate the input signal as
it becomes large. A key factor in the design of any AGC circuit is to
fully understand the amount of dynamic range required.

To understand the required range, let us examine the factors which
contribute to level variations. First, for a continuous or for a burst
modem, there are path attenuation variations due to atmospheric water
vapor. For those satellite links operating in the Ku-band of
frequencies (14 GHz) this can relate to 5 or 6 decibels of additional
path attenuations. And as you might guess, as the RF carrier frequency
is increased, so is the attenuation due to rain. In a Time Division
Multiple Access (TDMA) burst modem scenario where each participating
station broadcasts in a time sequence then the AGC circuit will
experience full burst to burst variations due to this rain. This is
because the rain event may be localized to only one site.

A second factor which increases the required AGC range is a direct
result of designing a variable rate modem. This is due to the dynamics
of bit rate changes. As an example, a particular variable rate
demodulator wants to process two alternating bursts on the same carrier
frequency. The first data rate is 2.048 Mbps while the second is 64
Kbps, both operating at the same operational Eb/No. In this scenario
the receiver would be required to change its gain up or down by at
least 15 decibels on a burst to burst basis.

Another factor which would effect an AGC circuit's dynamic range is the
composite operating point of a shared satellite transponder. For those

satellites driven deeply into the non-linear region of saturation the effective signal level for individual carriers will change each time another carrier is removed or is added. Rather than sending a field engineer to every site to optimally readjust the demodulators input signal, an AGC with greater dynamic range could be designed to remove this additional variation.

Additional factors which may effect the required dynamic range of the AGC will be lumped into a final factor. This will include the effects of amplifier aging, AGC circuit variations, field installation differences and others.

The factors listed here are both static and dynamic effects which describe the total dynamic range required by the demodulator's AGC circuit. For the continuous mode of operation, the dynamic range described could be implemented through slower circuit techniques because the rate of AGC change is slow. However it is desired that this modem work in the burst mode as well, and thus allowing the receiver to process different data rates on a burst to burst basis requires a fast AGC with greater dynamic range. From a cursory overview it appears that the AGC circuit design should consider a dynamic range of at least 30 decibels.

° Amplifier Distortions

It is readily apparent that any level variations in a digital satellite demodulator which utilizes digital filtering and soft decision FEC decoding will reveal itself as bit error degradation. But besides failing to correctly level an IF signal, it is possible that an AGC circuit can introduce other types of signal distortions. Because an AGC circuit is composed of amplifiers the possible distortions are those related to amplifiers. One of the most common distortions in an AGC circuit is noise figure.

A simple gain control circuit can consist of a step attenuator followed by an amplifier. As a small signal enters the circuit the attenuation is removed to obtain the desired amplifier output level. At high input signal levels the attenuator must incrementally be increased to keep the same output signal level, this however will increase the noise figure for the circuit.

Equation 1. "Friss' Formula" describes the relationships between the noise figures and gains of the various stages of gain.

$$NF = NF1 + \frac{NF2-1}{A1} + \frac{NF3-1}{A1xA2} + \cdots + \frac{NFn-1}{A1xA2x...An-1}$$

The important concept to note is that the majority of the noise figure is determined in the first stage of the overall system. Therefore the conclusion one should draw is that in the design of an AGC circuit the first element should be a large gain device with low noise figure.

GAIN CONTROL: Practical Gain Control Circuits

° Pin Diode

The unique feature of a Pin Diode is that at RF frequencies it has the characteristic of being a resistor. In fact the amount of resistance varies with the amount of dc current flowing through the diode. A circuit can be composed to offer current controlled attenuation with these diodes. In the frequency range, typically below 10 MHz Pin Diodes conduct and rectify signals thus they distort signals. Therefore, all approaches using Pin Diodes will be circuits operating at IF or RF frequencies. Figure 1, "Pin Diode AGC", reveals a typical configuration for a RF gain controlled block. The resistance of the diode will change more than 2 decades thus resulting in at least 20 decibels of AGC range.
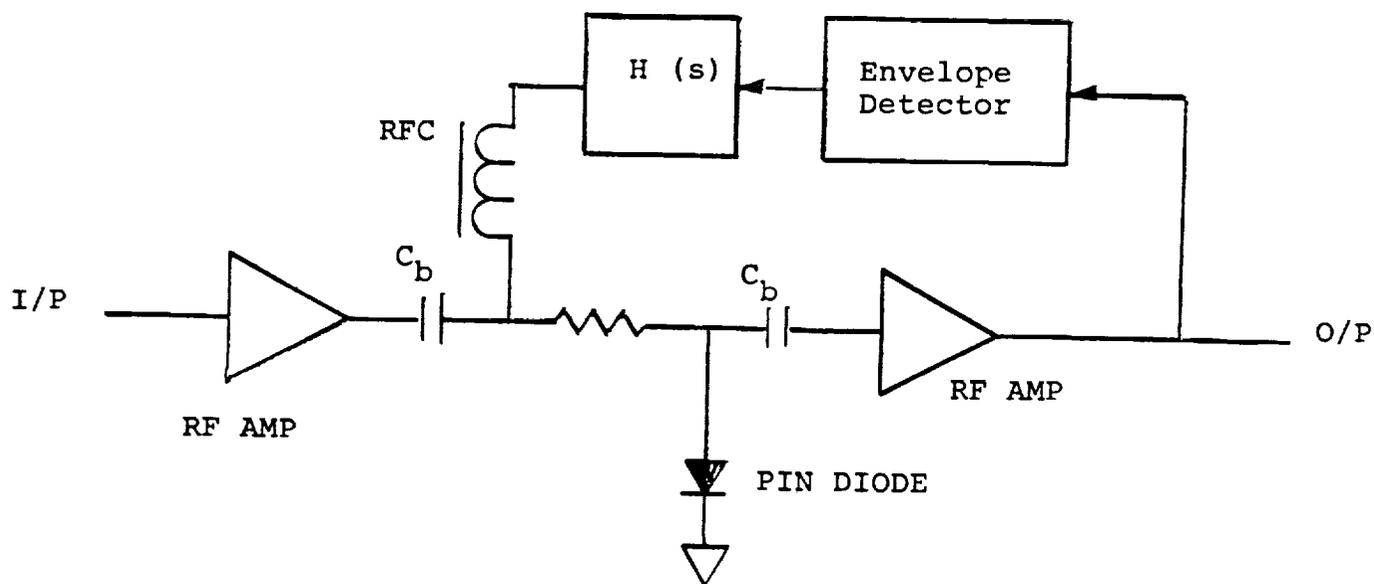
Figure 1. Pin Diode AGC

° Field Effect Transistor

Similar to his brother the bipolar transistor, the Field Effect
Transistor (FET) has more than one mode of operation. For most
applications, the device is operating in its saturated (constant
current) region. In a second mode of operation known as non-saturated,
the FET has a unique feature that it functions like a voltage
controlled resistor. In this mode of operation, the gate to source
voltage Vgs controls the drain to source resistance. This quality
makes it well suited for use in a variable gain stage.

As a component in a practical gain stage it has some limitations.
Typical FET's can change its resistance 100:1, but to remain linear the
range is reduced. Practical FET's have junction capacitance and this
results in upper frequency response cut off's. Figure 2, "JFET AGC",
shows a typical configuration for a FET gain controlled block.
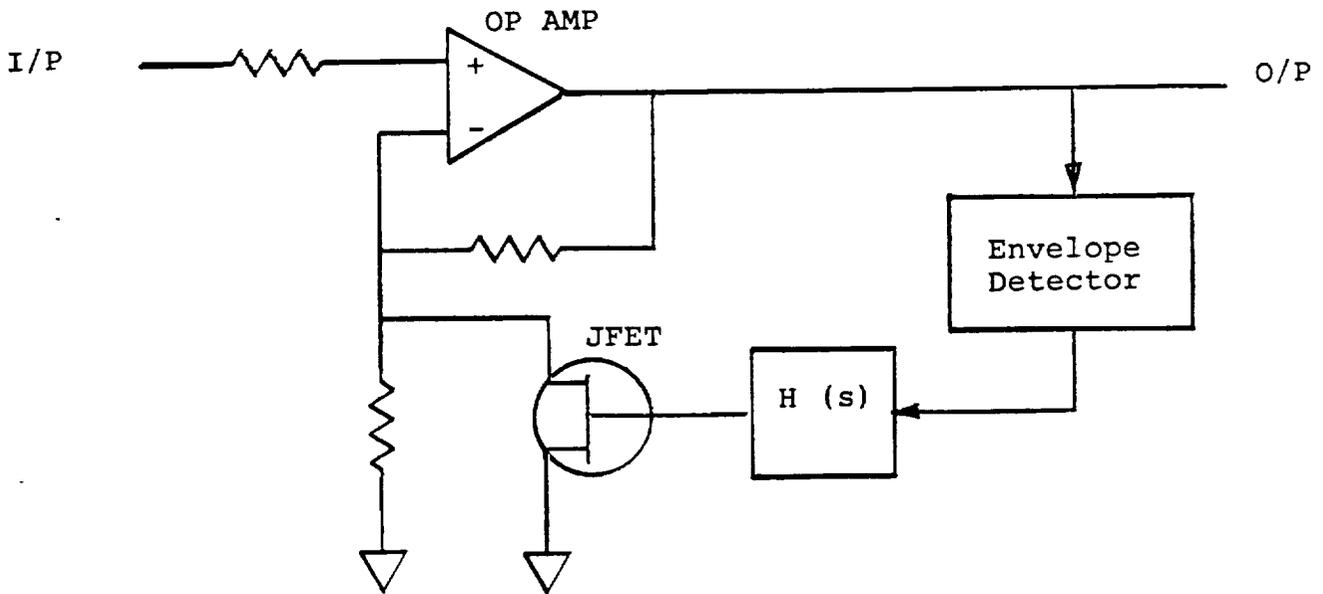
Figure 2. JFET AGC

° Relays

A broadband approach to attenuate a signal can involve utilizing attenuator "pads". A resistive pad can be modelled as a two port network. It has three resistive elements and can offer better input or output notches to physical generators and to loads. A pad can offer attenuation and impedance match over a broad range of frequencies, from dc to rf. However this fixed attenuation block must somehow be made variable so that it can be used in a variable gain block scenario. One common methodology to obtain variable gain with fixed blocks is to use relays to switch in different attenuation value pads, this is shown in Figure 3. An elegant feature of this approach is that any amount of attenuation is obtainable with just three resistors.
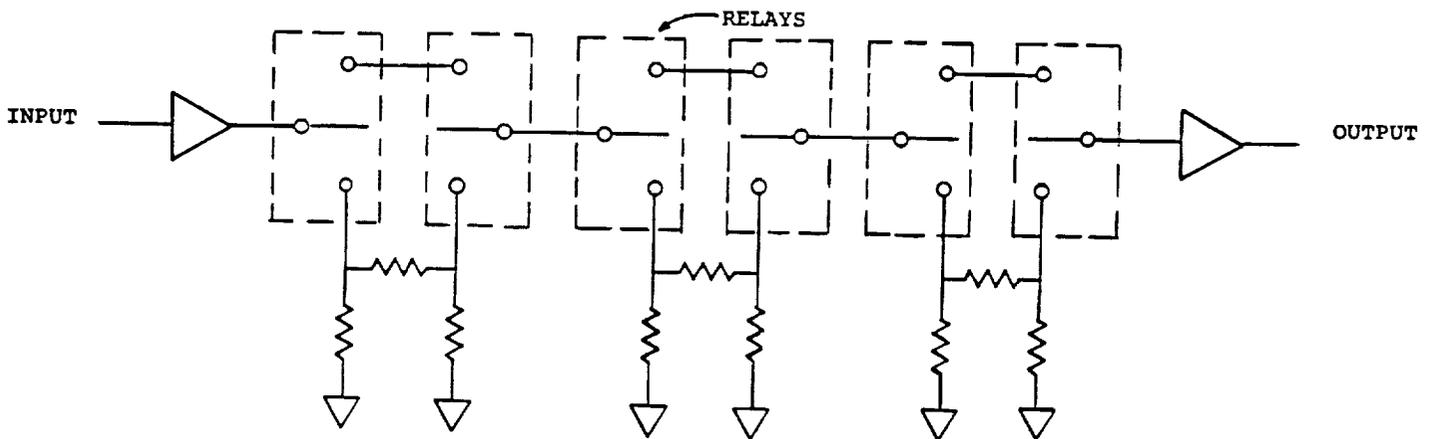
Figure 3

° AGC Circuit Placement

The location and the design structure of the AGC circuit will be
determined by the receiver's carrier recovery approach. The recovered
carrier may be designed to directly down convert the input signal,
therefore the AGC circuit would operate on the baseband signal. But
also carrier recovery may dictate the addition of a secondary IF stage.
In an approach using dual or tri frequency conversions may result in an
IF AGC circuit.

In the broadest sense, the AGC circuit must be located in the receiver
somewhere before the Analog to Digital Conversion (ADC) takes place.
There is no doubt that the quicker the incoming signal has been
levelled, the better. The problem that there is not a best and unique
circuit place is not because gain or attenuation can not be achieved,
but because of the detector. The detector used to control the amount
of gain and attenuation may process energy from adjacent carriers and
thus be fooled into attenuating the desired signal.

In an analog modem where the input signal is first processed by the
receive sides data filtering then the AGC circuit can only process the
desired carrier and this is ideal. In a digital receiver the input
signal must be levelled first before digital filtering therefore all
approaches must have some clever form of level detection to prevent
from AGC'ing on multiple signals.

For the proposed variable rate digital satellite modem there are only
two viable scenarios for AGC circuit placement. As was stated before
the receiver's carrier recovery design will determine which one will be
implemented. The reason for suggesting that there are only two viable
approaches is a result that no signal filtering takes place in the
receiver until after both I and Q channels have been ADC.

For the first scenario carrier recovery directly down converts the
input spectrum to baseband. In this scenario the signal level detector
will be done digitally after the FIR filters. The control signal will
be fed back to the AGC circuit which will be placed after the
anti-aliasing filters, but before the ADC.

In the second scenario carrier recovery is done at a constant IF
frequency, thus the receiver is designed with more than one IF stage.
It may be desirable, in this approach, to have some type of variable
bandwidth carrier selective filtering. After the signal passes through
this filter, the noise bandwidth and thus possible extraneous signals
will be reduced and prevented from fooling the AGC detector.

Either scenario outlined above is viable. Each has its own unique
qualities, some of them not mentioned. Ultimately the approach selected
will depend upon the receivers carrier recovery design.

CONCLUSION

The Automatic Gain Control (AGC) circuit of a receiver must be designed
with sufficient gain to properly amplify the weakest signal that it
wishes to demodulate. At the same time the circuit must have the

ability to reduce its gain for large input signals without causing measurable signal distortion. In this paper, three AGC considerations were discussed; they were Fast AGC, AGC range and possible distortions. The importants of a Fast attach AGC was discussed as it relates to the Burst Mode of modem operation. From a cursory overview of AGC range it appears at least in 30 decibel AGC is required for this design. As a final consideration noise figure for the AGC circuit was discussed.

Following these discussions, three practical AGC circuit implementations were described. The three circuits were Pin Diode, FET and Relay switched PAD's. There exists other techniques but the circuit choice will come from one of these three. In the final section, AGC circuit placement was discussed. This section described implementation problems and that the approach will be dictated by the demodulator's carrier recovery architecture.

MEMORANDUM

TO: NASA Modem Study File   DATE: June 2, 1988

FROM: George K. Bunya   MCC FILE MCC-93

SUBJECT: RECEIVE DSP DATA FILTERS - FILE NUMBER NASARX1.DSP

- -

ABSTRACT

An approach to solve the problem of a variable data rate filter, in a
digital satellite demodulator, is presented. Currently available
satellite receivers sidestep the issues associated with variable rate
filtering by offering factory tuned plug-in filters. By implementing
digital signal processing (DSP), the receive filters in a satellite
demodulator can be designed to offer a truly variable rate scheme. It
is the intent of the author to surface and to discuss a viable
approach to a truly variable rate receiver filter. With the focal
point of the discussion being the importance of over sampling and of
analog anti-aliasing filters.

TIME DOMAIN FILTERING

In general there are two basic signal filtering classes. One class is
the well known and practiced method of signal filtering in the
frequency domain. This class of filters use frequency differentiation
to separate and to attenuate frequency components. However, in
general this class of filters can not be made to offer variable rate
filtering therefore for the present discussion this class is ignored.

Time domain filters are the second general class of signal filters. A
time domain filter is in reality a computational process in which a
digital word is accepted and transformed into another digital word.
These Computational filters, or DSP (Digital Signal Processor) as they
are popularly known, are mathematical devices. These filters use the
simple mathematics of multiplication and of addition to produce its
digital output. In order to produce a variable rate data filter,
using this approach, requires only an increase or a decrease in the
speed of the mathematics.

RECEIVE DIGITAL SIGNAL FILTERS

Unlike the transmit filters, the receive signal filters must accept a
signal which has been corrupted by noise in the transmission media and
possibly by the presence of other modulated signals. For the digital
receiver, the proposed filter structure will be simular to that of the
transmit's architecture. Figure 1, "Receive Signal Filter
Architecture" reveals the main blocks associated with the design.

```
                          Transfer at
                            "M" times
          _____   _____   _____
         |              | |       | |     |            |
         | Analog       | | ADC   | | "N" | Computational |
         | Anti-        | |       | | bits| Filter        |
  I/P --| Aliasing     |---|     |---/--|               |-- Filtered
         | Filter       | |       | |     |            |    Data
         |              | |       | |     |            |
          _____   _____   _____
              - analog
              signal -->
```

Figure 1. Receive Signal Filter Architecture

The anti-aliasing filter is unique to the receive DSP filters. Its
purpose as will later be described is to prevent the phenomenon of
frequency foldback. The Analog to Digital Converter (ADC) is the
inverse function of the transmitters DAC and thus is responsible for
converting the analog input signal to a time sampled digital quantity.
The receiver's computational filter is a Finite Impulse Response (FIR)
digital filter. The computational filter of the receiver will involve
"N" bit wide multiplications and additions therefore it is to the
interest of the design to limit "N" to as small a number as possible.

ANTI-ALIASING FILTER

The irony of all digital filters is that they all require a good
analog filter. The analog filter is required to remove frequency
components above one half the sampling rate of the ADC. Frequency
components above one half of the sampling rate, if not properly
attenuated, are folded or aliased back to lower frequencies. For
example if the sampling rate for a particular digital receiver was 100
KHz and if there was no anti-aliasing filter and the ADC was exposed
to a 99 KHz frequency component than the apparent output from the ADC
would appear as 1 KHz. Since an input of 99 KHz and of 1 KHz both
appear as a 1 KHz output then there is ambiguity and the digital FIR
computational filter will not be capable of properly filtering the
signal. If the analog filter is placed at exactly one half of the
sampling rate then the aliasing of high frequency components to lower
ones no longer occurs.

A second criteria related to the cut off frequency of the
anti-aliasing filter is the Nyquist criterion. The criterion requires

that the sampling rate of the ADC be at least twice as fast as the highest frequency component of interest. After pondering this statement, then one realizes that the minimal solution is an anti-aliasing filter at half of the sampling rate where the highest frequency component of input signal is allowed. Or stated differently, that the anti-aliasing filter is in reality the Nyquist filter with an alpha factor of zero (theoretical brick wall filter). And this solution is the same as the pure analog receiver with "N" level soft decision bits.

In this design approach to a variable rate filter it is here that a stumbling block appears. Before, we noted that when the clock speed of the computational filter changed we had a variable rate filter. But now in order to change the rate of the filter a new and unique anti-aliasing filter must be added. This implementation of changing anti-aliasing filters for every data rate is no better a solution to a variable rate filter design than is exchanging factory tuned plug-in filters and thus not an acceptable approach. Therefore we will diverge from the present path to introduce and to explore the concept and over sampling to again strive for a true variable rate filter design.

OVER SAMPLING

A key element to understanding the proposed continuously variable rate receive signal filter is the concept and the process of over samplings. Using the concept of over sampling, in the design of our digital filtering will allow us to digitally filter several different signal rates with the same analog anti-aliasing filter. A brief example to follow will demonstrate the process of over sampling in a variable signal rate filter scenario. And like most things, there are some negative aspects to note about over sampling such as lowering the uppermost signal filtering rate of the design. However, in order to achieve a truly continuously variable rate signal filter, this appears to be the only viable approach.

The concept of over sampling is as simple as it sounds and it has some extremely positive effects when designing a variable rate digital filter. Simply put, the principle is to digitally sample an analog signal at a rate much faster than that which is required. For example, sampling at 20 times the highest frequency component of a signal is 10 times more than that which is required by Nyquist first criterion. It is logical to ask the question: What is gained when a digital filter designer decides to over sample a waveform If the digital filter design operates at only one sampling rate then the answer is very little. However, in a variable rate digital filter, this over sampling will allow using the same anti-aliasing filter for several different sampling rates.

The process of over sampling allows several different sampling rates to use the same anti-aliasing filter. To follow is an example of over sampling and an example of its greatest benefit. Suppose a 10 KHz signal waveform is to be digitally filtered, but rather than sampling at a 20 KHz rate it is sampled at a 100 KHz clock rate (over sampled). Therefore, the signal has been over sampled by a factor of 5 and the

maximum cutoff frequency of the anti-aliasing filter allowed is 50 KHz. Next suppose a 11 KHz signal is to over sampled at the same factor of 5. Thus the sampling rate is 110 KHz and all frequencies above 55 KHz need to be removed to prevent frequency aliasing. Now the question is it possible to use the same anti-aliasing filter for both sampling rates? The answer is obvious and it is the direct effect of over sampling which will allow us to design a variable rate receive filter. Table 1 "Effects of Constant Over Sampling by 5" tabularizes the above sample.

Table 1. Effects of Over Sampling by 5

Signal Rate (Highest Freq Component)	Over Sampling Rate by 5	Aliasing Frequency	Anti-Aliasing Filter
10 KHz	100 KHz	50 KHz	50 KHz
11	110	55	50
15	150	75	50
25	250	125	50

However over sampling a wave form requires an Analog to Digital Converter (ADC) which has a much greater bandwidth. And as was the case in the transmit filtering, this conversion to and from an analog waveform (DAC or ADC) is the gating factor in cost and in defining the uppermost speed limit of the digital filter design. For example when we sampled a 10 KHz waveform at a 100 KHz rate we over sampled by a factor of 5, this ultimately cost buying an ADC with 5 times greater bandwidth. A second cost to over sampling which is noted here but will not be explained is the additional stress placed on the considerations of clock recovery in the receiver.

The process of over sampling outlined above is one of many possible schemes. In one scheme over sampling can be extended such that only one anti-aliasing filter is required. But to understand this approach requires introducing the processes of decimation and/or of complex coefficient schemes. Disregarding these processes and continuing with a constant factor over sampling, Table 2 "N Anti-Aliasing Filter Scheme" reveals how 7 analog anti-aliasing could be utilized to achieve a continuously variable rate digital signal filter.

Table 2. N Anti-Aliasing Filter Scheme

Digital Data Rates Between	ADC Sampling Rates	N	Anti-Aliasing Filter Bandwidth
64 - 128 KBPS	.64 - 1.28 MHz	1	320 KHz
128 - 256 KBPS	1.28 - 2.56 MHz	2	640 KHz
256 - 512 KBPS	2.56 - 5.12 MHz	3	1.28 MHz
512 - 1024 KBPS	5.12 - 10.24 MHz	4	2.56 MHz
1.024 - 2.048 MBPS	10.24 - 20.48 MHz	5	5.12 MHz
2.048 - 4.096 MBPS	20.48 - 40.96 MHz	6	10.24 MHz
4.096 - 8.196 MBPS	40.96 - 81.96 MHz	7	20.48 MHz

In the above example the signal waveform was over sampled by a
constant factor of 5, other values are possible and are probably more
desirable. It is also possible to increase the tuning range of the
data rate, which means that there is nothing special about tuning over
an octive. Furthermore the over sampling rate will relate the number
of coefficients in the FIR filter, which directly relates to the alpha
factor of the filter. Therefore the above example assumes many
factors which need to be more closely examined, in order for the
filter design to be complete.

SUMMARY

The primary objective of the NASA study contract is to assess
currently available techniques and viable approaches towards the
development of a truly variable digital satellite modem. One viable
approach to solve the problems associated with the design of a truly
variable rate signal filter was presented. The paper stressed he
importance of over sampling the input analog signal to the receiver
digital filters. The results of over sampling were two fold. First
it allowed us to create an approach which utilizes the same
anti-aliasing filter to digitally filter several input data rates.
Second, we found that over sampling resulted in lowering the upper
most frequency at which we could filter. It also reminded us that the
ADC (Analog to Digital Converter) is going to be the limiting cost
factor in the receive filter design. Additionally it was mentioned
that this type of over sampling, by a constant factor, was only one of
the many types. It was the intent of the author to surface and to
discuss a viable approach to a continuously variable receive signal
rate filter.

multipoint communications corp.

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June 2, 1988

TO: NASA SATELLITE MODEM STUDY FILE

FROM: R. L. WALLACE

SUBJ: SATELLITE LINK RF OSCILLATOR PHASE NOISE IMPACT ON CARRIER
        RECOVERY OF PROGRAMMABLE RATE DIGITAL SATELLITE MODEM

The carrier recovery network used in coherent demodulation of BPSK/QPSK
signals must have sufficient bandwidth to track the phase noise of the
down link translated carrier to minimize performance degradations caused
by RMS phase error jitter. On the other hand, the larger this bandwidth
the less signal to noise improvement, i.e., the higher the thermal noise
performance degradations at low Eb/No's. Based upon these conflicting
requirements a minimum carrier recovery bandwidth can be identified
which is dependent on the RF frequency band used and the specific
carrier recovery implementation. Once this bandwidth is identified, the
respective lower data rate limit can be identified.

This memo outlines a simple methodology for calculating this minimum
carrier recovery bandwidth. In addition, both positive and negative
points will be highlighted on candidate carrier recovery techniques
which support both burst/continuous modes of operation.

The composite phase noise density for a satellite link can be assessed
by adding on a power basis the phase noise density plots of the transmit
earth station up converter, the satellite translator oscillator and the
receive earth station down converter.

For Ku-Band (14/12 GHz) transmission INTELSAT documents IESS-308 and
IESS-405 define worst case phase noise density masks for earth stations
processing digital carriers with data rates up to 2048 KBS. Figures 19
and 4 depict these masks for the spacecraft and earth station frequency
converters respectively. Also shown in Figure 19 is a plot of the
composite satellite link. For K_a band operation (30/20 GHz) the
composite phase noise density will be shifted higher by about 6∿8 dB.

Since PSK is a suppressed carrier modulation scheme, non-linear
processing of the received signal to create a recovered carrier is
required for coherent detection. Numerous authors have identified
viable recovered carrier implementation techniques which have merit;

COORDINATES OF POINTS

Point	Density (dBc/Hz)	Frequency (Hz)
A	-33	10
B	-62	100
C	-81	1k
D	-84	2k
E	-84	10k
F	-84	100k
G	-84	1M

−25dBc/Hz

Composite Satellite Link

−56dBc/Hz

−74dBc/Hz

PHASE NOISE ENVELOPE

−86dBc/Hz

20dB/Decade

SINGLE SIDEBAND PHASE NOISE POWER DENSITY (dBc/Hz)

FREQUENCY OFFSET FROM CARRIER (Hz)
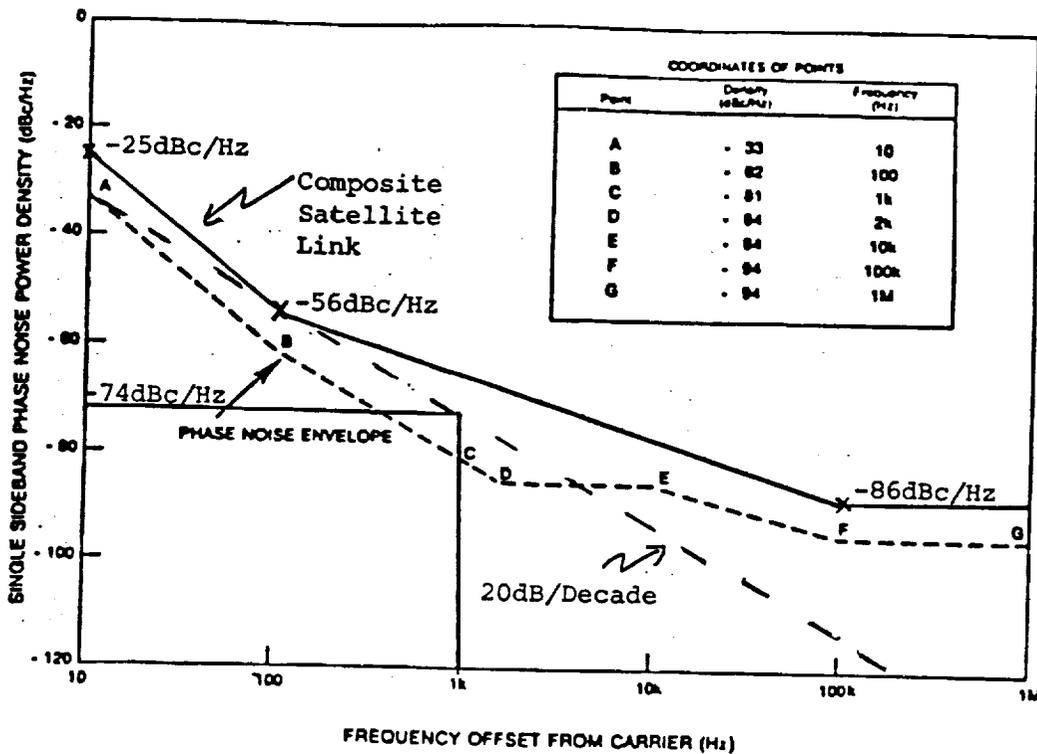
Figure 19
INTELSAT VA
Continuous Component of Phase Noise

COORDINATES OF POINTS

POINT	DENSITY (dBc/Hz)	FREQ. (Hz)
A	-60	100
B	-90	100K

SINGLE SIDEBAND PHASE NOISE DENSITY (dBc/Hz)

FREQUENCY FROM CENTER (Hz)
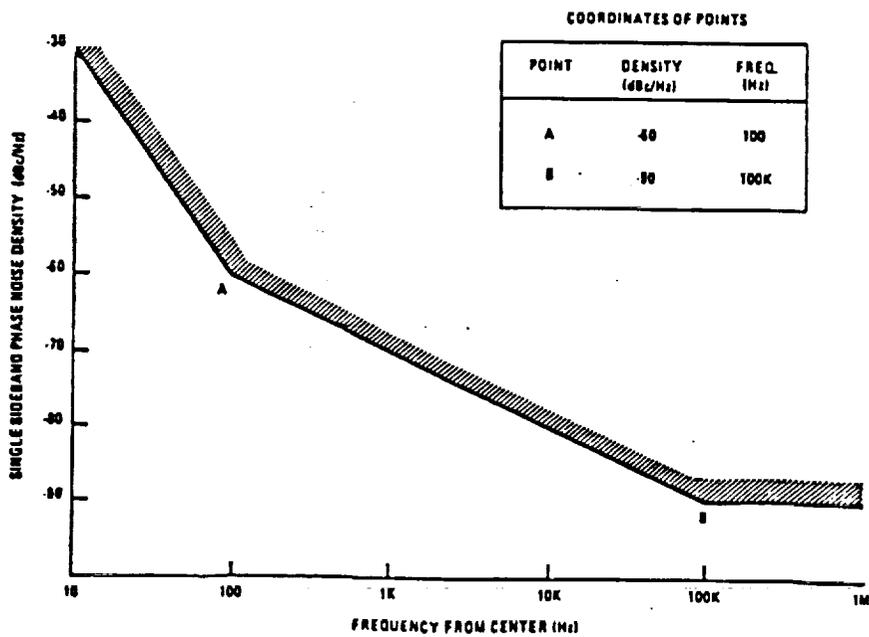
Figure 4
CONTINUOUS SINGLE SIDEBAND PHASE NOISE REQUIREMENT
(for carriers with information rates less than or equal to 2.048 Mbit/s)

these include the XN multiplier, inverse modulator (remodulator), COSTAS, and digital baseband processing schemes.

The multiplier and inverse modulator schemes generate a "raw" recovered carrier component which is narrow bandpass filtered to improve its C/N prior to demodulation. For transmission rates below ≅ 5 MBS a phase locked loop is generally used for this narrow filtering due to finite "Q" limitations of discrete filters at I.F. The inverse modulator scheme becomes unpractical at these lower rates since this technique requires a broadband delay of the IF PSK signal indicative of a symbol period.

The COSTAS and digital baseband processing schemes all utilize a voltage controlled oscillator which is phase locked to a reference phase position, coherent with the PSK signal by non-linear processing of the demodulated baseband information.

If it is desirable for the programmable rate digital modem to operate at rates below 5 MBS some type of phase locked loop carrier recovery filter scheme is highly probable.

A disadvantage worth noting at this time is that the XN multiplier carrier recovery schemes spread the phase noise spectral density plots over N times the input bandwidth; hence X2 (X4) schemes necessitate 2 (4) times the minimum phase locked loop bandwidth respectively for the same degradation as compared to the other techniques previously discussed.

The phase noise power spectral density, $G\phi(f)$, of the received downlink PSK signal consists of the sum of frequency flicker noise - $G\phi_A(f)$, white frequency noise - $G\phi_B(f)$ and white phase noise - $G\phi_C(f)$. Mathematically, this can be expressed as follows:

$$G\phi(f) = G\phi_A(f) + G\phi_B(f) + G\phi_C(f) \; ; \; f > 0$$

$$= \frac{K_A}{f^3} + \frac{K_B}{f^2} + K_C \; ; \; f > 0$$

The carrier recovery PLL tracking errors for each terms is now calculated given the composite satellite link phase noise density of Figure 19 (Non-multiplier technique assumed). The tracking error for the phase locked loop where H(jw) is the closed loop transfer function is defined as:

$$\sigma_\epsilon^2 = \int_0^\infty G\phi(f) \left[1 - H(jw)\right]^2 df$$

$$= \sigma_{\epsilon A}^2 + \sigma_{\epsilon B}^2 + \sigma_{\epsilon C}^2$$

Table 12-4 from reference [1] depicts the magnitude of each of these tracking errors for a second order loop with 0.707 damping factor.

Table 12-4 PHASE-LOCKED TRACKING OF PHASE NOISE FOR A
PHASE-LOCKED LOOP WITH DAMPING $\zeta = 0.707$,
AND NOISE BANDWIDTH $B_n = 0.53\omega_n$

Type of Phase Noise	Phase-Noise Spectral Density	Phase Error — Second-Order Phase-Locked Loop, $\zeta = 0.707$ $\sigma_e^2 = \int_0^\infty \frac{\omega^4/\omega_n^4}{1 + (\omega/\omega_n)^4} G_\phi(f)\, df$
Frequency flicker noise	$\frac{k_a}{f^3}$	$\frac{k_a\pi^3}{\omega_n^2} = \frac{k_a\pi^3}{(1/0.53)^2 B_n^2} = \frac{8.71 k_a}{B_n^2}$
White frequency noise	$\frac{k_b}{f^2}$	$\frac{3.70 k_b}{B_n}$
White phase noise	$k_c, f < f_h$	$k_c f_h$

Inspection of the composite satellite link phase noise spectral density shown in Figure 19 identifies K_A and K_C as follows:

$$K_A = \left(\text{Log}_{10}^{-1} \; \frac{-25\text{dB}}{10} \right) (10 \text{ Hz})^3$$

$$K_A = 3.16$$

and

$$K_C = \left(\text{Log}_{10}^{-1} \; \frac{-86\text{dB}}{10} \right)$$

$$K_C = 2.51 \times 10^{-9}$$

Since the plot shows a 10dB/decade not 20dB/decade rolloff between 100 Hz to 100 KHz, a worst case value of -74dBc/Hz at 1 KHz will be used to determine K_B since this value intersects the composite curve at the 100 Hz specification point.

[1] "Digital Communications By Satellite" by James J. Spilker, Jr., 1977 Prentice-Hall, Inc., (Pages 336 through 357).

Table 1 identifies the RMS tracking phase jitter between the recovered carrier and the PSK signal verses carrier recovery noise bandwidth. The performance impact of the white phase noise term $\sigma_{\epsilon c}$ is a function of f_H, where f_H is the one sided noise bandwidth of the demodulators filtering prior to the phase locked loop input. For a COSTAS type loop this f_H bandwidth would be equal to the baseband data filter bandwidth prior to demodulation/detection which would have an upper bound equal to the symbol rate for practical modems.

Table 1 indicates a minimum BN of 1000Hz at Ku-Band for $\leq 1.0°$ phase jitter due to link RF oscillator phase noise. If a X2 (X4) multiplier recovered carrier scheme is used, BN minimum translates to 2000Hz (4000Hz) respectively.

The low data rate limit of a programmable rate digital satellite modem can now be assessed by multiplying BN_{min} times the C/N ratio improvement of the recovered carrier network for the termal noise performance objectives of the modem desired.

Typical continuous satellite modems have a C/N ratio improvement of a factor of 100, this would result in a lower data rate limit of 100KBS for a non-multiplier type carrier recovery at Ku-Band.

For KA Band operation a trade off between thermal noise and RF oscillator phase noise should result in a 200 KBS lower transmission rate limit using a C/N ratio improvement factor of 50 for the carrier recovery.

TABLE 1

BN (Hz)	$\sigma_{\epsilon C}$			$\sigma_{\epsilon}A$	$\sigma_{\epsilon}B$	σ_{ϵ} TOTAL = RMS PHASE JITTER		
	$f_H = 25$ KHz	$f_H = 50$ KHz	$f_H = 100$ KHz			$f_H = 25$ KHz	$f_H = 50$ KHz	$f_H = 100$ KHz
10Hz	7.9×10^{-3}RAD	1.12×10^{-2}RAD	1.58×10^{-2}RAD	5.2×10^{-1}RAD	1.2×10^{-1}RAD	5.3×10^{-1}RAD (30.6°)	5.3×10^{-1}RAD (30.6°)	5.3×10^{-1}RAD (30.6°)
100Hz	7.9×10^{-3}RAD	1.12×10^{-2}RAD	1.58×10^{-2}RAD	5.2×10^{-2}RAD	3.8×10^{-2}RAD	6.5×10^{-2}RAD (3.7°)	6.5×10^{-2}RAD (3.7°)	6.63×10^{-2}RAD (3.8°)
200Hz	7.9×10^{-3}RAD	1.12×10^{-2}RAD	1.58×10^{-2}RAD	2.6×10^{-2}RAD	2.7×10^{-2}RAD	3.83×10^{-2}RAD (2.2°)	3.9×10^{-2}RAD (2.2°)	4.0×10^{-2}RAD (2.3°)
500Hz	7.9×10^{-3}RAD	1.12×10^{-2}RAD	1.58×10^{-2}RAD	1.0×10^{-2}RAD	1.7×10^{-2}RAD	2.1×10^{-2}RAD (1.2°)	2.27×10^{-2}RAD (1.3°)	2.53×10^{-2}RAD (1.45°)
1000Hz	7.8×10^{-3}RAD	1.12×10^{-2}RAD	1.58×10^{-2}RAD	5.2×10^{-3}RAD	1.2×10^{-2}RAD	1.5×10^{-2}RAD (0.87°)	1.72×10^{-2}RAD (0.99°)	2.05×10^{-2}RAD (1.2°)
2000Hz	7.6×10^{-3}RAD	1.09×10^{-2}RAD	1.58×10^{-2}RAD	2.6×10^{-3}RAD	8.6×10^{-3}RAD	1.18×10^{-2}RAD (0.67°)	1.4×10^{-2}RAD (0.81°)	1.82×10^{-2}RAD (1.04°)
5000Hz	7.1×10^{-3}RAD	1.06×10^{-2}RAD	1.54×10^{-2}RAD	1.0×10^{-3}RAD	5.4×10^{-3}RAD	9.0×10^{-3}RAD (0.51°)	1.2×10^{-2}RAD (0.68°)	1.6×10^{-2}RAD (0.94°)
10000Hz	6.1×10^{-3}RAD	1.00×10^{-2}RAD	1.50×10^{-2}RAD	5.2×10^{-4}RAD	3.8×10^{-3}RAD	7.2×10^{-3}RAD (0.41°)	1.07×10^{-2}RAD (0.61°)	1.55×10^{-2}RAD (0.89°)

TABLE 1

RMS TRACKING PHASE JITTER BETWEEN
RECOVERED CARRIER AND PSK SIGNAL
VERSUS BN (PLL NOISE BANDWIDTH)

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MEMORANDUM

TO: NASA MODEM STUDY FILE   DATE: October 13, 1988

FROM: Robert L. Wallace   MCC FILE MCC-93

SUBJECT: MODEM FREQUENCY CONVERSION AND RECEIVE SIDE CARRIER
           SELECTION

- -

INTRODUCTION

The objective of this memo is to identify a viable transmit and
receive side frequency conversion methodology which can be utilized by
a Programmable Rate Digital Satellite Modem operating with carrier
agility in a shared, multi-carrier satellite transponder environment.
The Frequency Conversion impact on Receive Side Carrier Selective
Filtering will also be assessed.

BACKGROUND

Typical satellite Digital Modems interface to Radio Frequency
Terminals (RFT) at either the 70 MHz ± 18 MHz or 140 MHz ± 36 MHz I.F.
bands. The choice as to which band to use is determined by the actual
Satellite Transponder Bandwidth offered. Older satellites utilize 36
MHz wide Transponder channels which in turn necessitates use of the 52
MHz to 88 MHz I.F. band. Newer satellites offer 72 MHz Transponder
bandwidths at both "C" and "Ku" bands which necessitates use of the
104 to 176 MHz I.F. band. Future trends in satellite communications
indicate higher RF frequency bands and high spacecraft power amplifier
capabilities which in turn will drive the Transponder bandwidth higher
and higher.

Typical deployments configure the Frequency Converters in the RFT to
center the selected Transponder Channel in the middle of the I.F.
Interface. The Digital Satellite Modem in turn is responsible for
carrier generation on the transmit side and carrier selection on the
receive side. Typical carrier stacking bandwidths are at 1.4 times
the symbol rate for multi-carrier satellite applications. This
necessitates the need for modem carrier agility with ≈ 50 KHz step
size for data rates ≥ 64 KBS with QPSK modulation.

This modem carrier agility can be provided in one of two ways: By direct Modulation/Demodulation at the selected Carrier Frequency or by using a Fixed Frequency Modem which is frequency translated to/from the selected I.F. Carrier Frequency by an IF Synthesizer. We will now assess the merits of both these alternatives for the transmit and receive sides of the Programmable Rate Modem.

TRANSMIT SIDE

The modulator requirements affected by this choice are as follows:

1) Common implementation approach which supports Carrier Agility in both the 70 MHz and 140 MHz I.F. Bands.

2) Maintain at least -50 dBc signal purity outside the information signal band within the transponder bandwidth.

3) Minimize the complexity of analog signal processing which relates to increased cost.

4) Minimize the performance distortions caused by amplitude and delay distortions which result from additional filtering.

Figure 1 details functional block diagram of both alternatives using Baseband Spectral Shape Filtering for the QPSK Modulator. The direct modulation scheme necessitates that all elements of the modulator operate over the full I.F. Synthesizer Frequency range. The only element which can be classified as narrow band is the 90° Phase Shifter. Typical analog implementations utilize either a Quadrature Hybrid or a Bandpass Filter for this function. The former device enables operation over an octive bandwidth maximum, which supports operation over either I.F. band but not both with one type of device and the latter device only supports operation for one carrier frequency. Another alternative which utilizes digital logic processing is shown in Figure 2A. "D" type flip-flops are used to generate quadrature local oscillators. This technique is broadband and is only limited by the logic speed used. This technique also requires that the I.F. Synthesizer span four times the bandwidth at four times the center frequency which may necessitate slightly high cost. In summary, this alternative using either 100K or GaAs ECL Logic provides a common viable implementation which supports both I.F. bands. Figure 2B shows yet another implementation alternative for generating broad band quadrature agile carriers. Here the conventional I.F. synthesizer is used to generate the inphase (0°) carrier component. A broadband power divider is used to couple out a portion of this signal which is phase compared to the output of another identical I.F. VCO circuit. A double balanced mixer used as a phase detector generates a cosine type error signal. This error signal is used to lock the other I.F. VCO to the same frequency as the I.F. synthesizer output however the phase will be in precise quadrature. This technique eliminates the need for generating signals at four times the desired I.F. and is easily accommodated with the addition of multiple circuits of the same type.
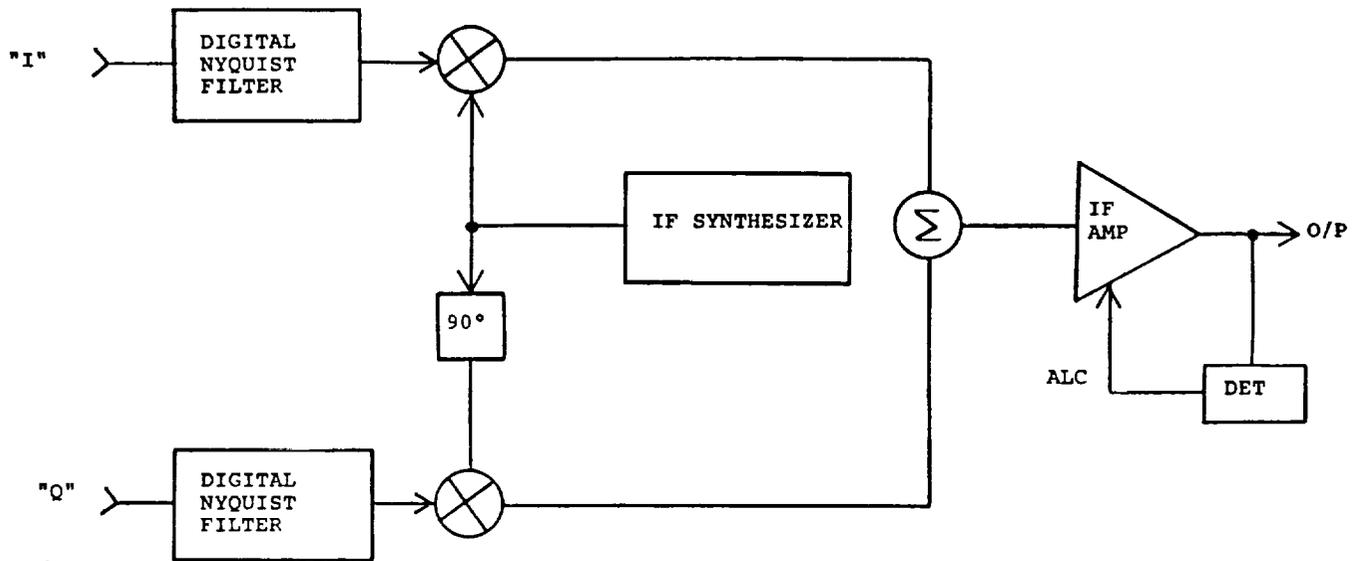
Figure 1a.   Functional Block Diagram of Direct QPSK
Modulator
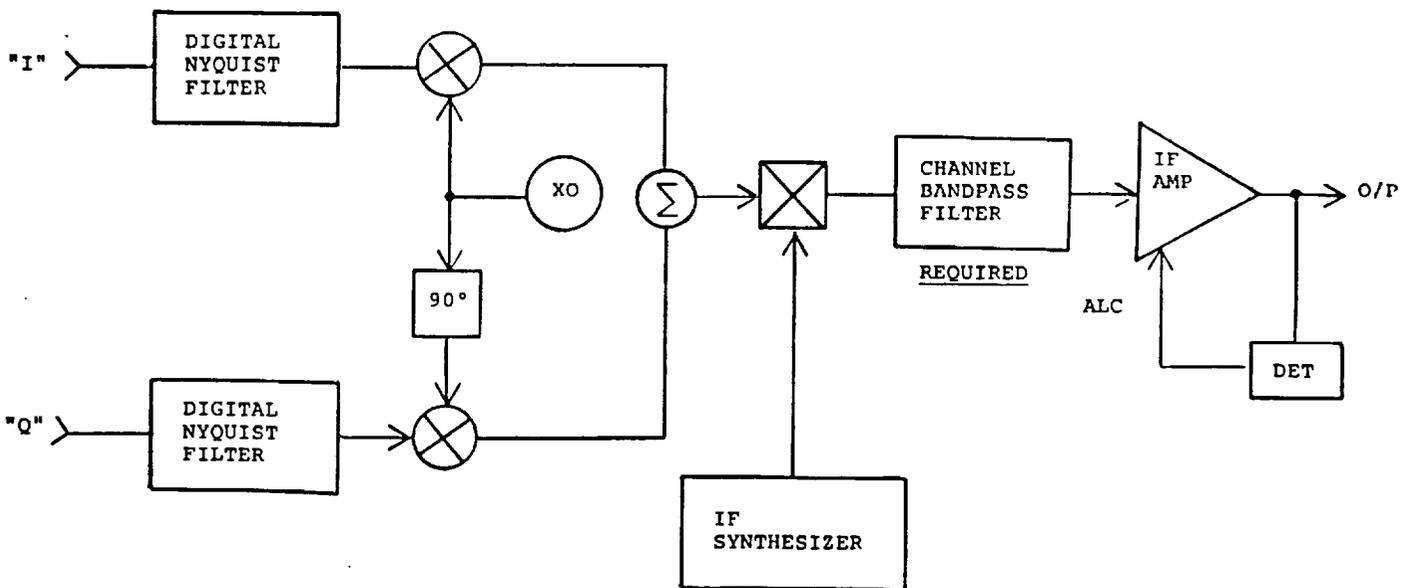
Figure 1   Functional Block Diagram of Frequency
Translated QPSK Modulator

7-3
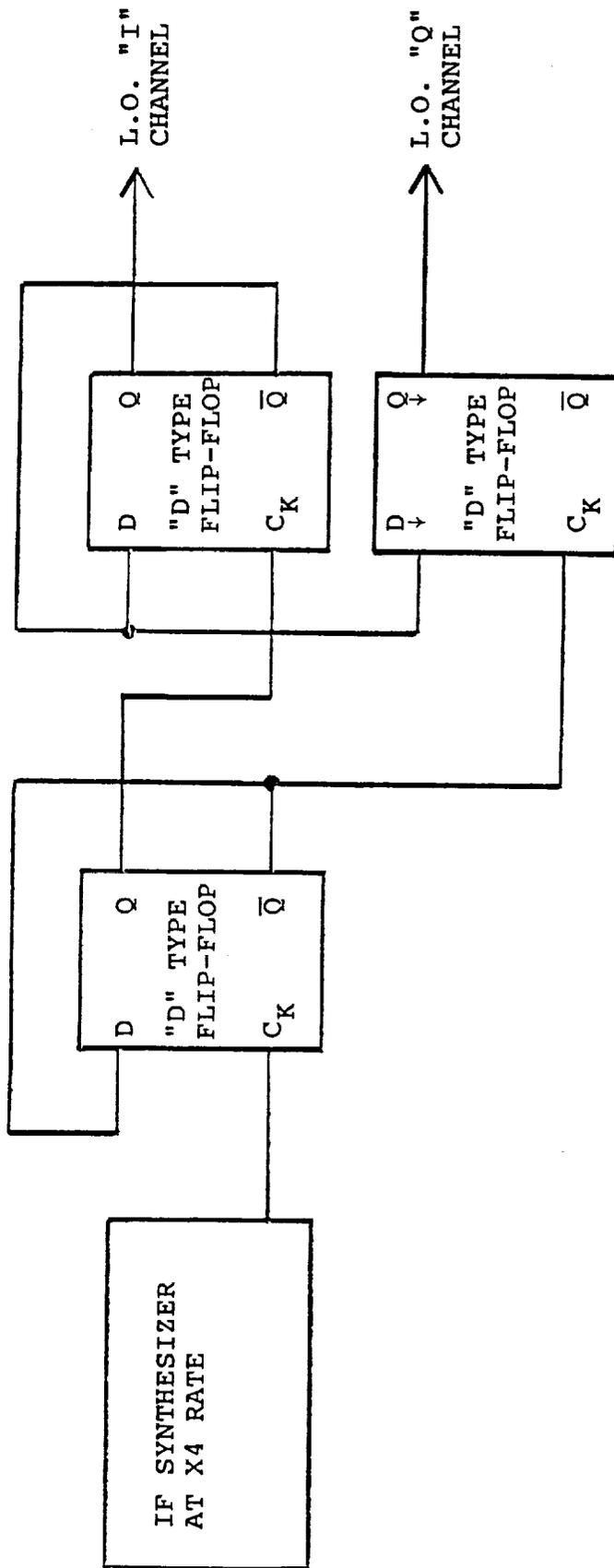
Figure 2A. Broadband Quadrature Local Oscillator Generator
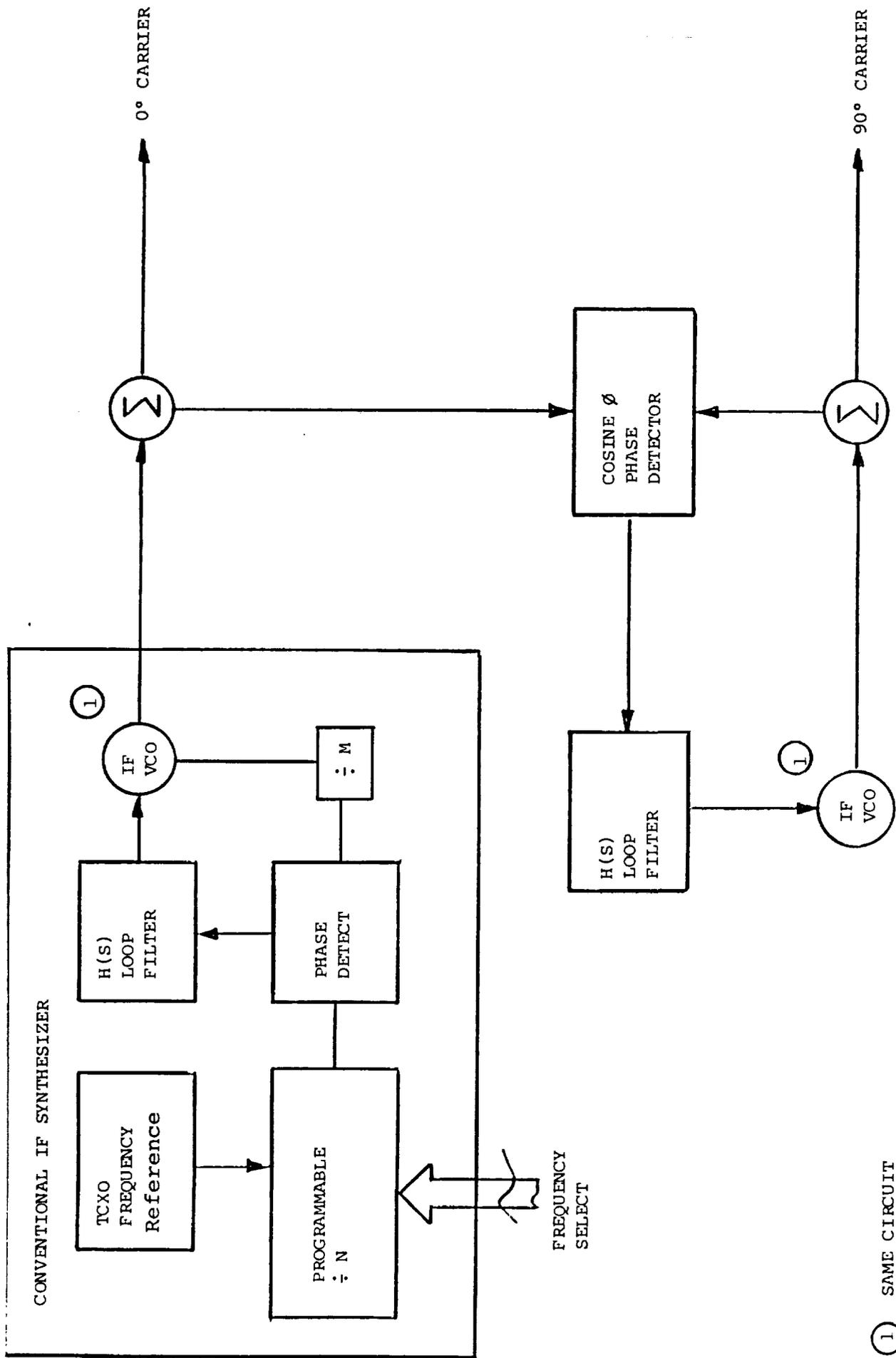
FIGURE 2B

BROADBAND QUADRATURE
LOCAL OSCILLATOR GENERATOR

Ideally the direct modulation scheme will only generate the desired carrier at the modulator output and the carriers spectrum will be defined by the Digital Nyquist Filters used at baseband. Therefore, this technique does not require any additional filtering at I.F. which in essence satisfies all the requirements quite well.

The frequency translated approach allows a Fixed Carrier Frequency Modulator to be utilized which is then translated to the respective I.F. Band by an I.F. Synthesizer. We now examine the constraints on this frequency choice as they relate to a common hardware implementation which supports both the 70 MHz and 140 MHz bands.

Table 1 summarizes the modulator frequency restrictions necessary for each band based upon the respective translation equation chosen. The first equation does not support a common solution for both I.F. bands, however, the other two equations do. To determine which frequency choices are viable necessitates a calculation of mixer intermodulation products to determine if the -50 dBc in-band spurious requirement is satisfied. In addition to this effort, one needs to assess the I.F. Synthesizer implementation feasibility as well as the Channel Bandpass Filter requirements. Typical I.F. Synthesizers provide up to an octive tuning range and are more cost effective the lower the frequency range.

The second equation shown in Table 1 is satisfied with practical I.F. Synthesizers in the 142 - 178 MHz and 194 - 266 MHz range for the 70 MHz and 140 MHz I.F. bands respectively, assuming F_{MOD} of 90 MHz. The third equation requires $F_{MOD} > 352$ MHz for practical I.F. Synthesizers, since operation at $176 < F_{MOD} < 204$ MHz results in more than octive tuning range for the upper band local oscillator. Based upon these results, the second Frequency Translation equation appears to be the most practical.

Table 1. Modulator Frequency Restrictions

Translation Equation	70 MHz Band Restrictions	140 MHz Band Restrictions
IF Band $= F_{LO} + F_{MOD}$	36 MHz ① $< F_{MOD} <$ 52 MHz ②	72 MHz ① $< F_{MOD} <$ 104 MHz ②
IF Band $= F_{LO} - F_{MOD}$	$F_{MOD} >$ 36 MHz ① and $F_{MOD} <$ 52 MHz ② -or- $F_{MOD} >$ 88 MHz ②	$F_{MOD} >$ 72 MHz ① and $F_{MOD} <$ 104 MHz -or- $F_{MOD} >$ 176 MHz ②
IF Band $= F_{MOD} - F_{LO}$	$F_{MOD} >$ 88 MHz ② and $F_{MOD} <$ 104 MHz ① -or- $F_{MOD} >$ 176 MHz ①	$F_{MOD} >$ 176 MHz ② and $F_{MOD} <$ 208 MHz ① -or- $F_{MOD} >$ 352 MHz ①

① Limit determined by in-band leakage by L.O.

② Limit determined by in-band leakage of F_{MOD}.

The direct modulation technique also requires two IF Synthesizer bands at slightly lower frequencies. One can therefore conclude neither scheme offers any advantage in this area.

The Channel Bandpass Filter rejects undesirable spurious signals and harmonics which fall outside the specified IF band. Typical requirements are specified out to 500 MHz and are -50 dBc to -70 dBc down. Spurious signals in this frequency range can be processed by the earth station RFT Upconverter and HPA. These units usually provide full band capability. As a result they translate the spurious into RF interference which could fall in-band on other transponder channels on the satellite. For the frequency translated approach the Channel Bandpass Filter shape factor requirements can be calculated by taking the overall specification minus the rejection provided by the translation mixer at the modulator output for all frequencies of interest. This sounds complicated, however, only the spurious singals which related to mixer intermodulation products are leakage terms and are the only ones that dictate filter issues. An example of this calculation will be shown later for the receive side.

Ideally, there are no additional filtering requirements for the direct modulation approach. However, practically speaking, the Symbol Clock and odd harmonics of the IF Signal are present. The former signals will be under 10 MHz and can be filtered out by judicious choice of coupling capacitors in the design implementation. The odd harmonics of the IF Signal can be practically removed with a Low Pass Filter. Since the third harmonic of the low end of the 70 MHz band falls within the upper end of the 140 MHz band, two filters will be required. The complexity of these filters however is far less than that required by the frequency translated approach.

In summarizing our assessment thus far, we can conclude that the direct modulation implementation is less complex (i.e, more cost effective) and readily insures spectrum quality and purity without concerns of carrier agility or stringent additional filtering. Based upon these attributes, this approach should be selected.

RECEIVE SIDE

The Demodulator requirements affecting frequency conversion are quite different than those of the Modulator. The Demodulator is not very concerned with signal purity outside the information signal band, rather it is concerned with demodulating only "one" carrier out of "many" sharing the transponder channel. The implementation must be agile in center frequency, such that any carrier within the IF band can be selected. In addition to this requirement, the implementation should support programmable data rates from 100 KBS to 10 MBS.

These issues define the Demodulator requirements as follows:

1) Common implementation approach which supports carrier selection in both the 70 MHz and 140 MHz IF Bands.

2)   Provide minimum performance degradations due to many
     carriers sharing the common channel.

3)   Downconvert the selected carrier such that Carrier Recovery
     and Demodulation are viable.

4)   Assess the performance impact of adjacent channel
     interference verses carrier selective filtering for
     programmable data rates from 100 KBS to 10 MBS.

5)   Minimize the complexity of analog signal processing which
     relates to increased costs.

In order to separate the desired carrier from a composite signal
containing many carriers closely stacked, one must downconvert the
selected carrier to a frequency which will support some degree of
selective carrier filtering. Ideally, the optimum carrier selective
filter should satisfy Nyquist criteria and be "matched" to the
carriers transmit PSK spectrum. With this methodology only the
desired carriers information is passed on to the carrier recovery and
demodulation circuitry. Two alternatives are viable for this carrier
selection process. First, downconvert the desired carrier to DC and
utilize baseband filtering for the "matched" filters (i.e. direct
demodulation); secondly, downconvert the desired carrier to an
intermediate frequency which will support bandpass carrier selective
filtering followed by a fixed center frequency demodulator. The
former alternative raises questions on how to implement carrier
recovery. However, this technique is quite attractive when
considering digital filtering and programmable rates. The latter
alternative has been conventionally used for fixed rate modems and
requires partitioning of I.F. and baseband receive side filtering to
satisfy both carrier selectivity and optimum data filtering
requirements. Analog bandpass filter techniques do exist for fixed
rate modems which achieve true cosine response shapes. Multipoint
Communications burst demodulator is configured using this principle
with alpha factor equal to 0.4. This design choice has shown to be
more tolerant to adjacent carrier interference than one which provides
less (more) filtering at I.F. (baseband) respectively. Based upon
these conflicting issues, one can see why existing modem manufacturers
offer a limited number of multiple data rates rather than a true
variable rate design.

Direct Demodulation

The direct demodulation scheme allows for carrier selective filtering
as well as matched filtering to be implemented at one place which is
desirable. Since this location is at baseband, digital filtering
techniques are viable and are the optimum implementation choice when
considering programmable data rates. Since these filters are
"matched" to the desired PSK carriers spectrum minimum performance
impact to adjacent channel interference will result. In fact, one
should be able to stack the carrier at (one plus the alpha factor)
times the symbol rate without noticeable performance degradations.

The "one" and "major" concern with this scheme is the impact on carrier recovery. All the carrier recovery techniques published thus far assume that the input signal is a PSK signal at I.F. In this scheme, there is no I.F. therefore all the "raw" carrier recovery techniques (i.e. XN multiplier, inverse modulator and pilot tone) cannot be supported. The costas loop, decision directed and other types of carrier recovery techniques which process the demodulated symbol data generate a steering voltage to control the phase and frequency of a VCO or NCO. The only controllable oscillator available is the IF synthesizer, which is already operating in a closed loop fashion to generate the proper local oscillator frequency. Inspection of this operation reveals that the I.F. synthesizer output frequency is determined by its reference oscillator as shown in Figure 2B and is non-coherent with the received signal.

We propose this idea, suppose that we replace this reference oscillator [which is usually a free running temperature compensated crystal oscillator (TCXO)] with a voltage controlled type (i.e. VCXO) and use the carrier recovery steering voltage to synchronize the I.F. synthesizer to be coherent in both frequency and phase with the desired PSK carrier. This technique looks attractive and at first glance operation appears to be feasible. More analysis is necessary, especially in the phase control information through the divide by N function, to justify that this scheme will work. Figure 3 details a simplified block diagram of this approach. We anticipate at this time that the scheme will require a long acquisition time since we have frequency selection, frequency and phase settling constraints when operating in the burst mode. However, we suggest more analysis in this area prior to firming up any implementation since the other attributes of this approach seem to satisfy all the other work study objectives.

Intermediate Frequency Translation

The choice of intermediate frequency for the demodulator must be high enough to pass the suppressed carrier PSK signal bandwidth yet low enough to perform practical bandpass filtering. This frequency choice is normally based upon the data rate, channel bandwidth and position of adjacent carriers which determine the filter "Q" and pole selectivity. Given the scenario where the desired carrier is rate programmable over a two decade range make this issue a lot more severe than for a fixed rate modem. One alternative is to utilize as many analog bandpass filters as data rates; this yields an unpractical solution which is analog complexity intense.

A practical solution to this problem, bearing in mind carrier recovery issues and the utility of digital filtering and DSP is one where the composite receive filtering is partitioned between the carrier selective filter and the digital baseband data filter. Ultimately, the optimum performance will be a tradeoff between the degree of carrier selective filtering prior to demodulation and the robustness of the carrier recovery technique verses adjacent channel interference.
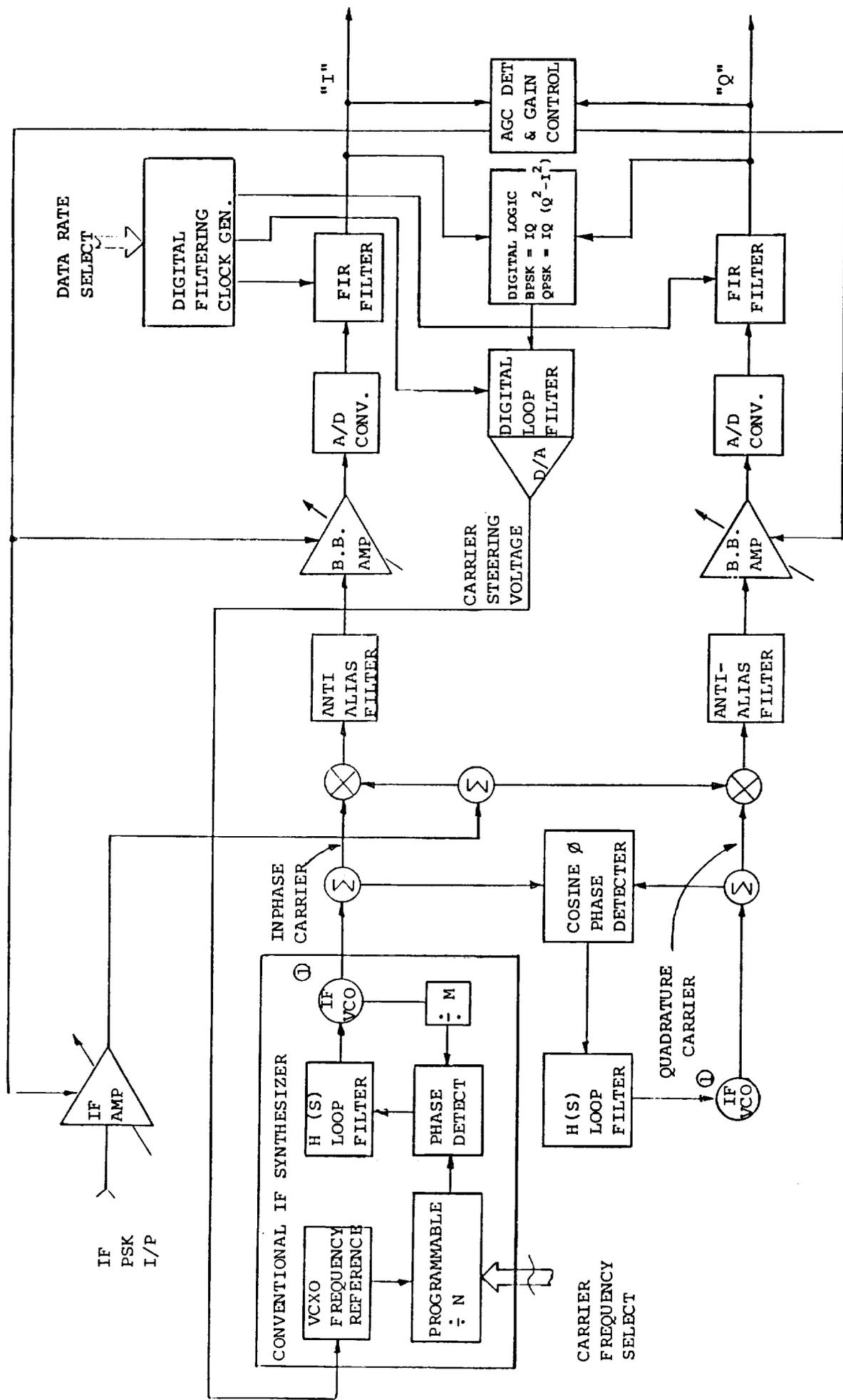
PROPOSED SIMPLIFIED BLOCK DIAGRAM
OF DIRECT DEMODULATION TECHNIQUE

FIGURE 3

7-11

We initiate our investigation by examining the appropriate locations for adjacent carrier selective filtering.

When the implementation provides no selective filtering prior frequency conversion, the Demodulators intermediate frequency is bound on the low end by half the transponder bandwidth. This comes about when the "image" frequency folds over right on top of the desired signal. As a result, this technique dictates $F_{DEMOD} \geq 36$ MHz assuming both the 70 MHz and 140 MHz bands are to be supported in a common design. In addition to this frequency requirement the practical implementation must insure that the signal handling capabilities of all active devices (i.e., amplifiers and mixers) used prior to selective filtering are sized to handle the maximum composite power rather than that of the desired signals.

Practical fixed bandwidth bandpass filters at this center frequency can achieve $3 \leq "Q" \leq 40$ (where $Q = f_o/f_{3dB}$). This will support a symbol rate range of 600 KBS to 8 MBS (assuming an F_{3dB} of 1.5 BT where BT is the symbol rate product) which overlaps pretty well with the high end of the study objectives. To determine the actual center frequency of the demodulator, one needs to check the worst cast C/IM ratio due to the mixer.

INTERMODULATION PRODUCT ASSESSMENT

Tables 2 and 3 define the typical and worst case IM product term levels for both IF bands for commonly used double balanced mixers. Tables 4 and 5 provide a representative assessment of the location and level of the IM products generated for both IF bands. The analysis shown assesses a common demodulator frequency of 36 MHz and a particular carrier selective bandwidth of 1.0 MHz. The skirt selectivity of this filter will ultimately determine how closely the carriers can be stacked. On the other hand, the bandwidth of this filter dictates the maximum data rate which can be processed (i.e., 1.0 MHz bandwidth can support $\cong$ 670 KBS symbol rate). In addition, the passband delay dispersions of the filter directly relate to additional performance degradations if left unequalized.

For the case at hand, the calculations indicate a worst case C/IM interference ratio of 36 dB. Figure 4 shows that the performance impact of this interference is less than 0.2 dB degradation down to 1×10^{-8} BER for QPSK. Therefore, one can conclude that this frequency translation choice satisfies carrier agility over both of the IF bands of interest.

In order to satisfy operation below 600 KBS symbol rate, a lower demodulator translation frequency is necessary. This can be only accommodated by using a pre-selector filter prior to the frequency conversion process. The pre-selector filter primarily removes the image signal from reaching the frequency translation mixer. This filters passband can be relatively wide compared to the desired signals bandwidth, however its center frequency must be tuned to that of the desired carrier which can be dynamically selected anywhere in the IF band.

Table 2. Typical Mixer I.M. Products

	0	1	2	3	4	5	6	7	8
7	>70	>70	>70	68	>70	68	>70	60	>70
6	>70	>70	>70	>70	>70	>70	>70	>70	>70
5	>70	62	>70	52	>70	48	>70	48	49
4	>70	64	>70	>70	>70	68	>70	68	>70
3	53	42	55	42	58	52	66	47	68
2	64	59	67	66	66	66	67	61	68
1	31	0	43	15	50	27	68	48	62
0		34	52	46	64	59	68	64	>70

Harmonics of the L.O.
+7 dB L.O. Level

Typical SRA-1 and SAM-3 intermodulation products; distortion levels are indicated by the number of dB below the output level of $f_{RF} \pm f_{LO}$.

Table 3. Worst Case Mixer I.M. Products

	0	1	2	3	4	5	6	7	8
7	>60	>60	>60	58	>60	58	>60	50	>60
6	>60	>60	>60	>60	>60	>60	>60	>60	>60
5	>60	52	>60	42	>60	38	>60	38	39
4	>60	54	>60	>60	>60	58	>60	58	>60
3	43	32	45	32	48	42	56	37	58
2	54	49	57	56	56	56	57	51	58
1	21	0	33	5	40	17	58	38	52
0		19	37	31	49	44	53	49	>55

Harmonics of the L.O.
+7 dB L.O. Level

Worst case SRA-1 and SAM-3 intermodulation products distortion levels are indicated by the number of dB below the output level of $f_{RF} \pm f_{LO}$.

NOTE: Worst case I.M. product are estimated at 10 dB worse; except for harmonics of the L.O. term which could be 15 dB worse.

Table 4. Receive Side (RF Band 70 MHz ± 18 MHz)

52.5 MHz ≤ RF ≤ 87.5 MHz
88.5 MHz ≤ LO ≤ 123.5 MHz
IF = 36 MHz

Worst Case IM Product	IM Freq/ BW	IM Tone Energy	In Modulation Energy	Carrier Selective Filter Attn.*	Net Atten.
1 fLO	88.5 MHz/ 0 MHz	-19 dBc	0 dB	-40 dB	-59 dBc
1 fRF	52.4 MHz/ 1 MHz	-21 dBc	0 dB	-40 dB	-61 dBc
2 fLO - 1 fRF	89.5 Mhz/ 1 MHz	-33 dBc	0 dB	-40 dB	-73 dBc
	(Worst Case Exists for 2(88.5) - 87.5 = 89.5 MHz)				
1 fLO - 1 fRF	36 MHz/ 1 MHz	0 dBc	0 dB	0 dB	0 dBc
3 fLo - fRF	178 MHz/ 1 MHz	-5 dBc	0 dB	-40 dB	-45 dBc
	(Worst Case fLO = 88.5 & fRF = 87.5 MHz) = 178 MHz				
fRF - FLO	37 MHz/ 3 MHz	-32 dBc	-4.8 dB	-6 dB	-42.8 dB
	(Worst Case fRF @ 53.5 Interference, LO @ 123.5 MHz)				
3 fRF - 2 fLO	36 MHz/ 3 MHz	-45 dBc	-4.8 dB	0 dB	-49.8 dBc
3 fRF - 3 fLO	36 MHz/ 3 MHz	-32 dBc	-4.8 dB	0 dB	-36.8 dBc
	(Exists for Carriers 12 MHz Lower than L.O.)				
5 fRF - 3 fLO	36 MHz/ 5 MHz	-42 dBc	-7.0 dB	0 dB	-49 dBc
	(Exists for Interference Carrier at 60.3 MHz where L.O. is at 88.5 MHz)				

* Filter Ultimate Attenuation of 40 dB.

Table 5. Receive Side (RF Band 140 MHz ± 36 MHz)

$$104.5 \text{ MHz} \leq RF \leq 175.5 \text{ MHz}$$
$$140.5 \text{ MHz} \leq LO \leq 211.5 \text{ MHz}$$
$$IF = 36 \text{ MHz}$$

Worst Case IM Product	IM Freq/ BW	IM Tone Energy	In Modulation Energy	Carrier Selective Filter Attn.*	Net Atten.
1 fLO	140.5 MHz/ 0 MHz	-19 dBc	0 dB	-40 dB	-59 dBc
1 fRF	104.5 MHz/ 1 MHz	-21 dBc	0 dB	-40 dB	-61 dBc
2 fLO - 1 fRF	105.5 Mhz/ 1 MHz	-33 dBc	0 dB	-40 dB	-73 dBc
(Worst Case Exists for 2(140.5) - 175.5 RF = 105.5 MHz)					
1 fLO - 1 fRF	36 MHz/ 1 MHz	0 dBc	0 dB	0 dB	0 dBc
1 fLO - fLO	35 MHz/ 1 MHz	0 dBc	0 dB	-40 dB	-40 dBc
(Exist for fLO @ 140.5 RF Interference Carrier at 175.5 MHz Interference at 35 MHz only Place)					
3 fLo - fRF	246 MHz/ 1 MHz	-5 dBc	0 dB	-40 dB	-45 dBc
3 fRF - fLO	102 MHz/ 3 MHz	-32 dBc	-4.8 dB	-40 dB	-76 dB
3 fRF - 2 fLO	36 MHz/ 3 MHz	-45 dBc	-4.8 dB	0 dB	-49.8 dBc
3 fRF - 3 fLO	36 MHz/ 3 MHz	-32 dBc	-4.8 dB	0 dB	-36.8 dBc
(Exists for Carriers 12 MHz Higher than L.O.)					
5 fRF - 3 fLO	36 MHz/ 5 MHz	-42 dBc	-7.0 dB	0 dB	-49 dBc
(Exists for Interference Carrier at 104.5 MHz where L.O. is at 162 MHz)					

* Filter Ultimate Attenuation of 40 dB.

One can see that if the L.O. is below the RF band by 36 MHz (which simplifies synthesizer design) we have:

Table 5. Receive Side (RF Band 140 MHz ± 36 MHz)
(Continued)

104.5 MHz ≤ RF ≤ 175.5 MHz
68.5 MHz ≤ LO ≤ 139.5 MHz
IF = 36 MHz

Worst Case IM Product	IM Freq/ BW	IM Tone Energy	In Modulation Energy	Carrier Selective Filter Attn.*	Net Atten.
$3f_{LO} - f_{RF}$	36 MHz/1 MHz	-5 dBc	0	0	- 5 dBc <u>Disaster</u>
		Exists for 68.5 ≤ f_{LO} ≤ 80.5 MHz)			
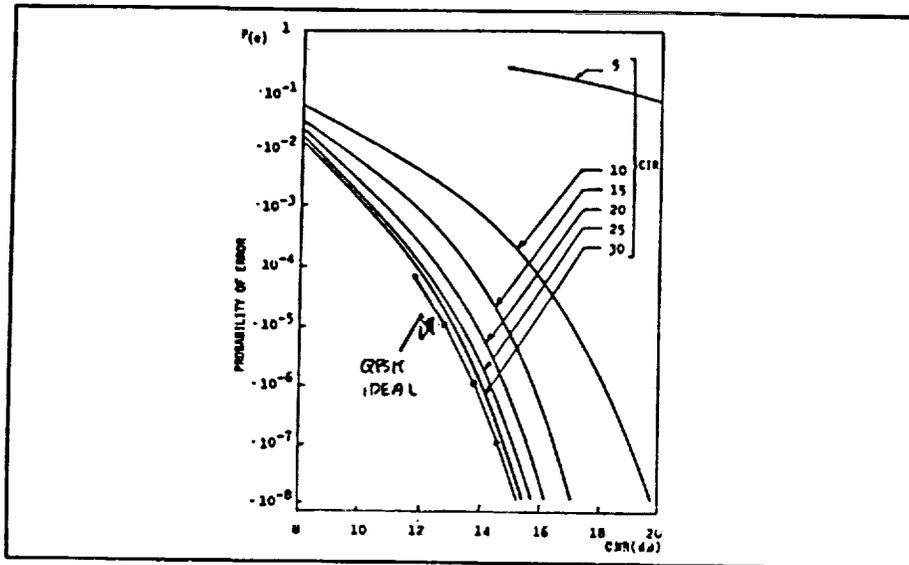
Figure 4A. P(e) as a Function of the CNR and CIR
in Coherent QPSK Systems (Noise measured
in the Doublesided Nyquist Bandwidth =
0.5 of the Bit Rate).
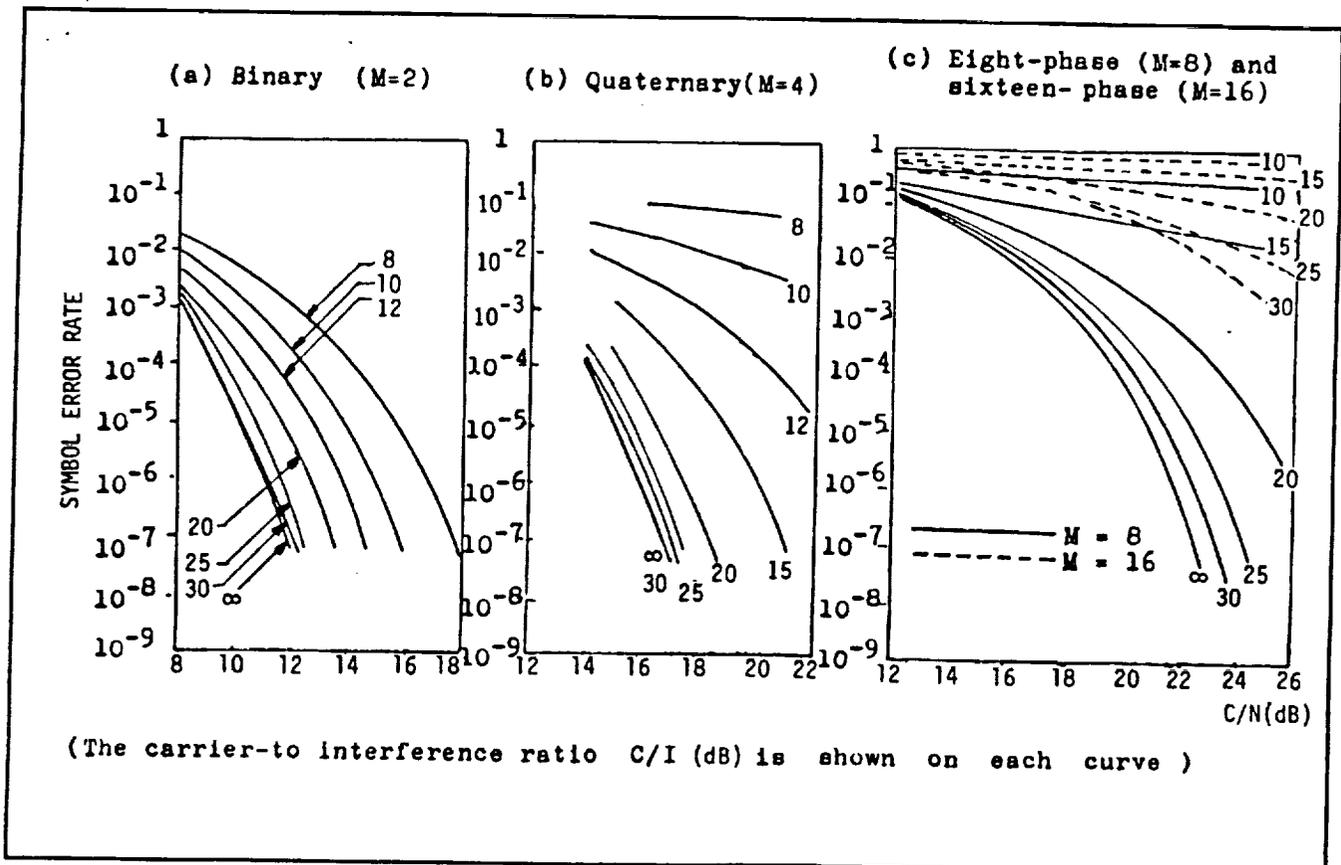
(The carrier-to interference ratio C/I (dB) is shown on each curve)

Figure 4B. Interference to M-ary Differential Coherent
PSK Signals from Angle Modulated Signals.

Another positive attribute of using a pre-selector is that only those carriers within the bandwidth of the preselector reach the mixer; thereby reducing the overhead dynamic range requirements of the active devices. On a negative point, the preselector is yet another analog filter which needs to tune with carrier position. This relates to more analog complexity.

Lets consider the practical ramifications of operating at 50 KBS symbol rate. Since this rate is twelve times lower than the lower limit viable at F_{DEMOD} = 36 MHz, then an F_{DEMOD} of about 3.0 MHz maximum is necessary. This choice relates to an upper limit of 1 MBS maximum symbol rate.

Summary

In conclusion, we have shown that the demodulator requires carrier selective filtering prior to carrier recovery and data demodulation when operating in a multi-carrier environment. Analog signal processing (i.e., bandpass filtering) is currently required for practical agile carrier applications. We have shown that the location and bandpass filter complexities are data rate dependent and that a programmable rate implementation is only viable over a twelve to one rate change factor. An attractive implementation has been identified which requires only a variable bandwidth fixed center frequency bandpass filter which supports programmable rates over 600 KBS to 10 MBS symbol rates.

HARDWARE RELATED ISSUES

° Variable Bandwidth Bandpass Filter

A practical variable bandwidth bandpass filter implementation viable in the 30 MHz to 70 MHz center frequency range is shown in Figure 5. This network provides a two pole filter shape with capacitive coupling. A Bessel or Gaussian response shape is invisioned such that intersymbol interference degradations caused by group delay are minimized. The source and load impedance of the tank circuits is determined by the pin diodes "on" resistance. This defines the "Q" or f3dB bandwidth. The coupling value between the tanks is controlled by the variable diode capacitor in such a fashion as to maintain the same passband shape factor. Since the control signals required are non-linear, digital "proms" are used to map the selected rate to the proper digital values. D to A Converters are then used to convert the control information to analog form.

Another viable approach is to use switched in fixed bandwidth filters which can provide a range of bandwidths. This is not elegant, however it may be practical assuming a 3 to 1 range of data rates being processed by one band pass filter could yield a design which only have four or five switchable filters.
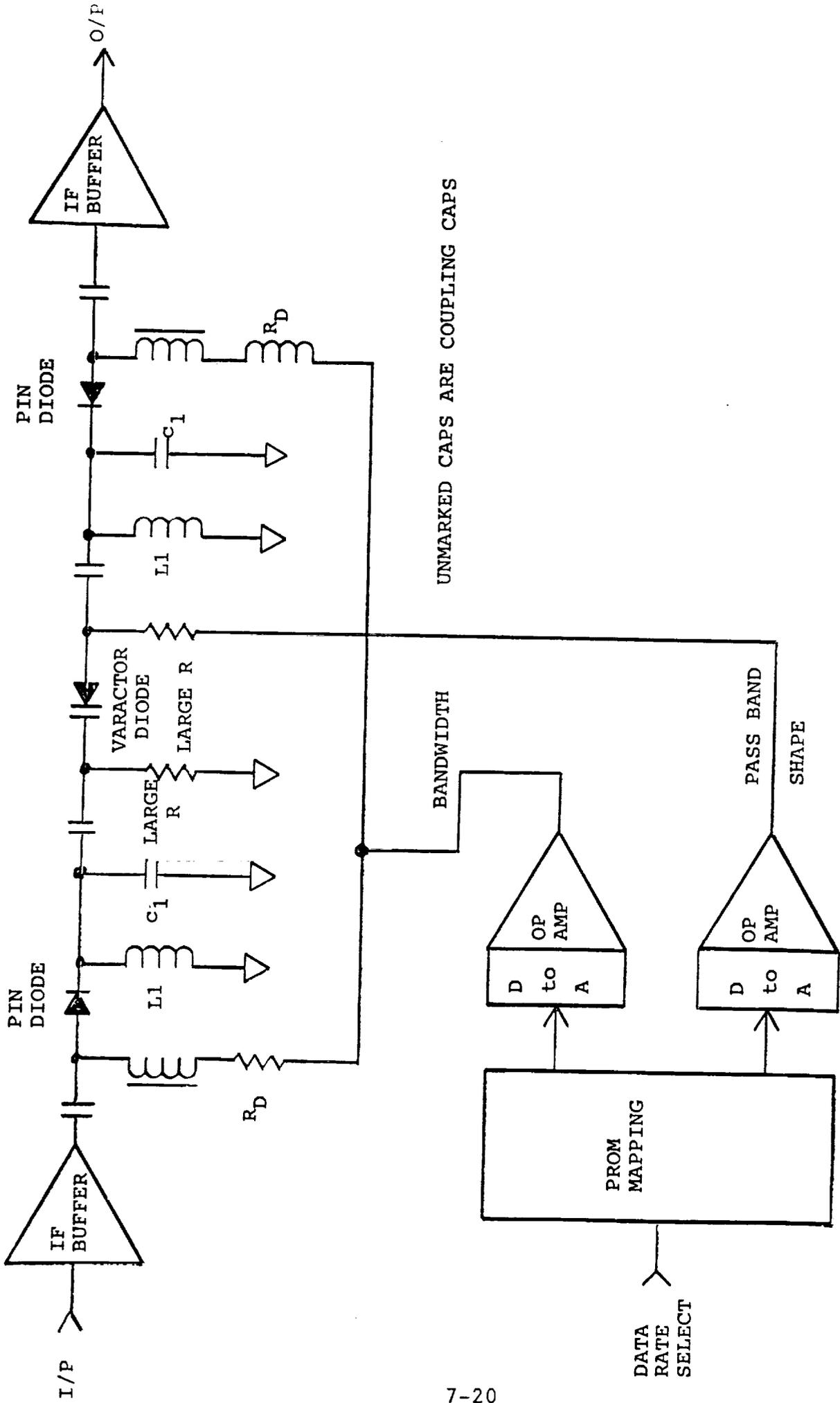
Figure 4. Variable Bandwidth Bandpass Filter

° Automatic Gain Control

The performance of Carrier Recovery techniques utilizing baseband processing and soft decision detection are strongly dependent on the signal level regulation of the symbol data streams. As a result Automatic Gain Control (AGC) is necessary. This topic will be discussed elsewhere in this study, however it is important to note the constraints put on AGC by receiver selective filtering issues. Typical detection and regulation of signal levels can occur at IF, Baseband or a combination of both (i.e., Baseband Detection with IF Regulation). Since the dominant receive filter is at baseband, this necessitates where final detection is required.

The signal level dynamic range at the Demodulators input is not only a function of the desired signals dynamic range but that of the composite signal power in the transponder. The former is usually bound by 20 dB for satellite applications. However the latter is a function of the number of carriers and their respective power allotment sharing the common channel. The bandwidth of the carrier selective filter will remove most, but not all, of the adjacent carrier energy, therefore baseband regulation is still required.

An implementation using IF AGC after the carrier selective filter is highly desirable because this scheme removes the input signal path variation and passes on only minor level variations which are easily handled by a limited range baseband AGC network.

MEMORANDUM

TO: NASA MODEM STUDY FILE

FROM: Robert L. Wallace

SUBJECT: CARRIER RECOVERY

DATE: October 14, 1988

MCC FILE MCC-93

- -

INTRODUCTION

In general, Digital Satellite Modems are characterized by providing the lowest possible Bit Error Rate (BER) for a given Bit Energy per Noise Density (Eb/No). Typically these modems are implemented with robust BPSK or QPSK Modulation and high overhead Forward Error Correction such that error-less performance can be realized over the satellite link which is characterized with high noise.

In order to support this objective, these digital modems utilize Coherent Demodulation and optimum detection with low implementation losses. Coherent Demodulation is accommodated by multiplying the received PSK signal with a locally generated recovered carrier replica. This recovered carrier replica must have sufficient noise improvement quality and precise phase alignment with the specific PSK modulated signal being processed in order to support low implementation loss BER degradation. Since PSK is a suppressed carrier type of modulation, some type of non-linear signal processing is necessary to regenerate a coherent carrier reference. This process is the topic of this memo and is referred to as "Carrier Recovery".

We initiate our effort in this study area by assessing current and proposed Carrier Recovery schemes which are viable candidates for BPSK and QPSK Modulation. Next, we turn our attention towards the specific requirements of the work study, i.e., a Carrier Recovery implementation which:

1)   Supports Programmable Data Rates;
2)   Operates with BPSK or QPSK Modulation;
3)   Supports both Burst and Continuous Modes of Operation;
4)   Minimizes the constraints on Clock Recovery/Bit Synchronization;
5)   Allows for digital filtering techniques prior to data detection;
6)   Can be implemented with Digital Signal Processing Techniques as compared to Analog Signal Processing; and
7)   Is viable in satellite communications.

In the following sections, an assessment of the characteristics of each viable Carrier Recovery scheme to the study specific requirements is made.

A candidate Carrier Recovery scheme selection is then made based upon the one which has the most favorable characteristics.

We conclude our effort in this study area by presenting a feasible hardware implementation of our candidate Carrier Recovery scheme.

ASSESSMENT OF CARRIER RECOVERY SCHEMES

Since the late 1960's numerous authors have written articles relating to various Carrier Recovery techniques and their performance attributes viable for PSK Demodulation. Table 1 summarizes these techniques as well as their classification type and noise bandwidth improvement methodology. The group classified as generating a "raw" carrier component were in general the first ones implemented and required Analog Signal Processing at either IF or IF and Baseband.

The other group classification does not generate a "raw" carrier component but rather a steering voltage for a Phase Locked Loop Oscillator. In this group only Baseband Signal Processing is used. With exception to the original Costas Loop, these techniques are only realizable with some form of Digital Signal Processing implementation.

As mentioned earlier, many papers by noteworthy authors have been written on this subject matter. It is beyond the scope of this study to mention each author and all his works. However, a list of references is provided which references technical information relating to the study requirements.

° PILOT TONE

The basic Pilot Tone Carrier Recovery technique requires transmission of a Residual Carrier Tone at a precise reference phase to that of the PSK modulated signal. This technique allocates the available power between the PSK Modulated Signal and the Pilot Tone. Carrier Recovery is accommodated simply by narrow bandpass filtering the pilot tone from the composite received signal. Fixed/Tracking Filters or a Phase Locked Loop can be used to improve the recovered carriers Signal to Noise Ratio (SNR). Reference [1] has shown that the performance of a Pilot Tone System depends critically upon the Tracking Loop Bandwidth and the power allocated between the Pilot and the PSK Signal. In no case considered does the Pilot Tone System out-perform the X2 Multiplier scheme for the same smoothing Filter Bandwidth. It can be shown that the increased phase estimate variance resulting from the X2 operation is more than offset by the decreased data channel SNR which occurs if part of the available power is diverted to transmit a Pilot Tone.

The best power allocation to employ, in practice, in a Pilot Tone scheme depends upon the tracking loop time constant to be used. This dependence can be explained in terms of two issues relating to the power division, which contribute to the system error rate.

```
                                                    ○ COSTAS LOOP

                                                    ○ DECISION DIRECTED COSTAS
                                                      LOOP

                                                    ○ DSP OF DEMODULATED SYMBOL
                                                      STREAMS


┌──────────────┐         ┌──────────────┐    ┌──────────────┐    ┌──────────────┐
│              │         │ DOES NOT     │    │              │    │              │
│              │         │ GENERATE     │    │ NOISE        │    │ PHASE        │
│              │────────▶│ A RAW CARRIER│───▶│ BANDWIDTH    │───▶│ LOCKED       │
│              │         │ COMPONENT    │    │ IMPROVEMENT  │    │ LOOP ONLY    │
│ PSK  CARRIER │         │              │    │ ALTERNATIVES │    │              │
│ RECOVERY     │         └──────────────┘    └──────────────┘    └──────────────┘
│ TECHNIQUES   │
│              │
└──────────────┘
```

○ XN MULTIPLIER

○ INVERSE MODULATOR
  (REMODULATOR)

○ PILOT TONE

```
┌──────────────┐    ┌──────────────┐         ┌──────────────┐
│              │    │              │         │ PHASE        │
│ GENERATES    │    │ NOISE        │    ┌───▶│ LOCKED       │
│ "RAW"        │    │ BANDWIDTH    │    │    │ LOOP         │
│ CARRIER      │───▶│ IMPROVEMENT  │────┤    └──────────────┘
│ COMPONENT    │    │ ALTERNATIVES │    │
│              │    │              │    │    ┌──────────────┐
└──────────────┘    └──────────────┘    │    │ NARROW       │
                                        └───▶│ BANDPASS     │
                                             │ FILTER       │
                                             └──────────────┘
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8-3
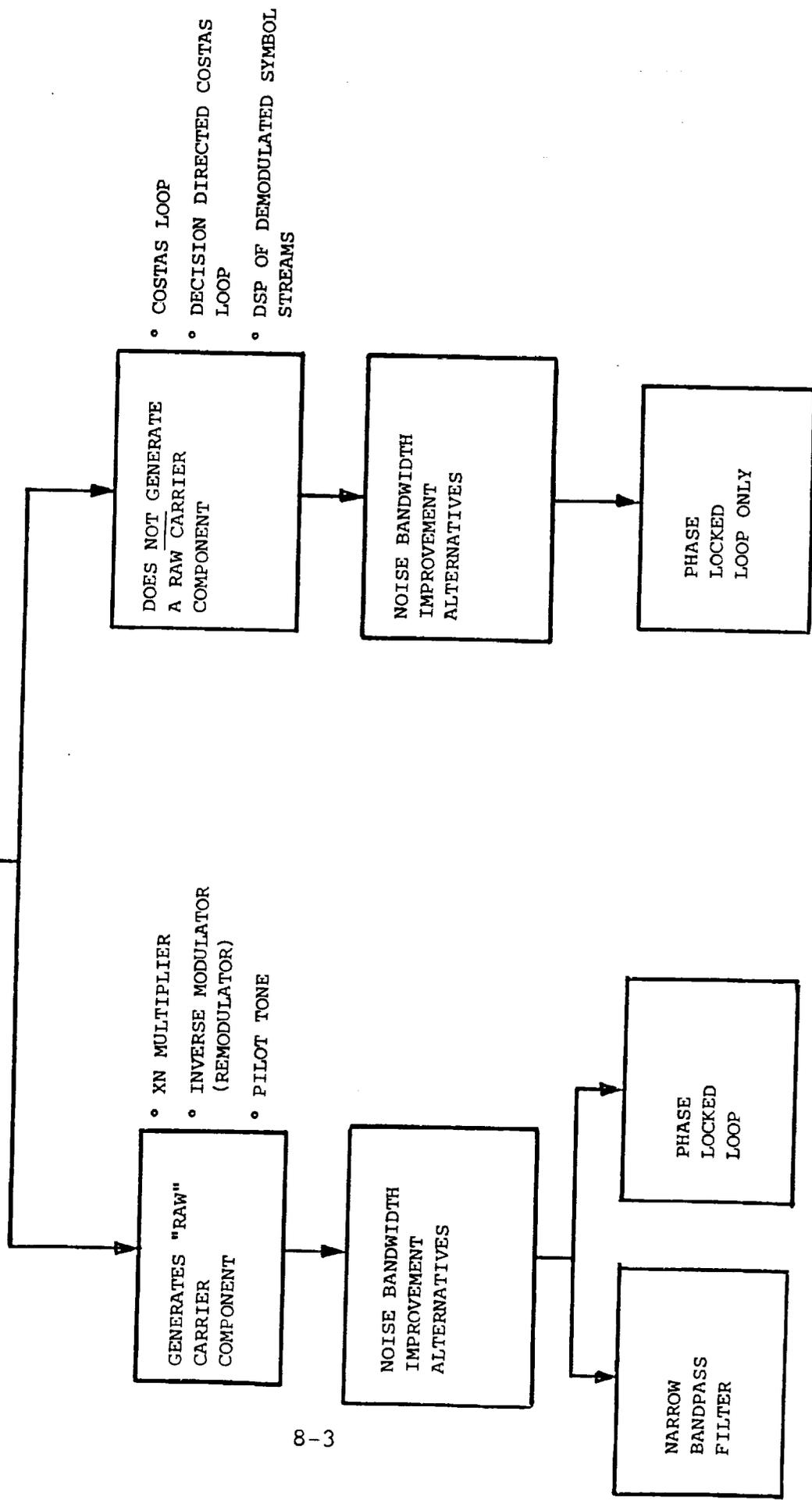
Table 1

a) If most of the power is allocated to the message sidebands, then the data channel SNR may be satisfactory, but the reference signal may be very noisy. When the reference is noisy, it may contribute significantly more to the Error Rate than the lower SNR in the data channel.

b) If a large portion of available power is allocated to the Residual Pilot Carrier, then the data channel SNR will be degraded with a resultant increase in Error Rate. In this case even a fast Wide-Band Tracking Loop might provide a reference having negligible noise compared to the data channel noise.

Figure 1 (from [1]) shows the BER -vs- Eb/No for BPSK comparing differential detection (DPSK), X2 Multiplier (squaring) and Pilot Tone (verses its percent of power allocation) Carrier Recovery techniques.
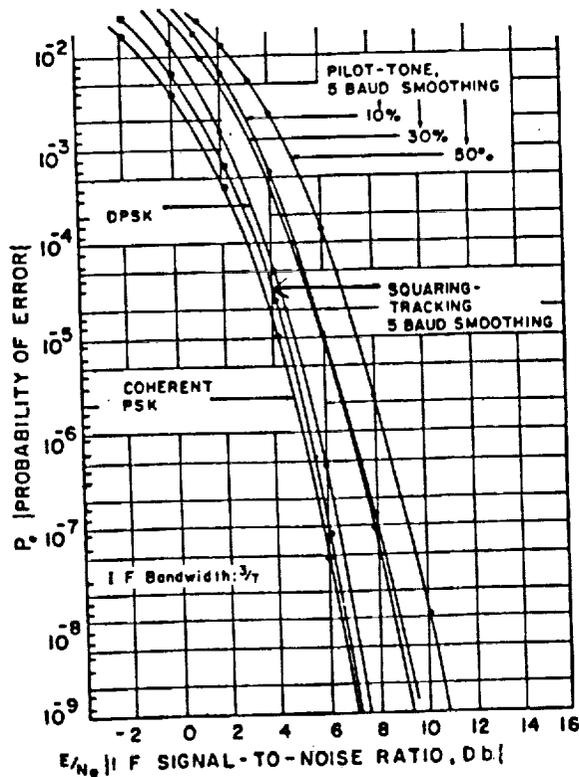
Figure 1

Now lets assess the characteristics of a Pilot Tone Carrier Recovery scheme to the specific work study requirements.

Since the performance is a strong function of pilot power allocation and loop bandwidth, one can conclude that this technique will not support programmable data rates with static settings. The Pilot Tone technique however will support both either BPSK or QPSK and should perform more favorably with QPSK when compared to an X4 Multiplier. Both burst and continuous modes of operation should be viable with the Pilot Tone technique. Since a Phase Locked Loop is not mandatory, potential false lock situations in the burst mode are avoided which is an advantage. The Pilot Tone Carrier Recovery does not require the use of symbol clock or Bit Synchronization to operate. In addition, it does not constrain the type or degree of baseband filtering used in the demodulation process. This scheme is implemented with Analog Signal Processing, not digital, and would be inferior in BER performance over a satellite link when compared to X2 Mmultiplier scheme.

° XN MULTIPLIER

In BPSK (QPSK) Systems, the set of phase states generated is a multiple of $2\pi/N$, where N=2 (4) respectively, and passing the received PSK signal through a Nth power non-linearity will provide a carrier component at N times the PSK carrier frequency. The carrier recovery process entails passing the PSK received signal through this XN non-linearity, filtering in a narrow bandpass filter followed by a limiting amplifier to remove amplitude fluctuations and finally frequency dividing by N to yield a coherent reference at the PSK carrier frequency.

Numerous narrow bandpass filter implementations have been used. Among the most popular are Phase Locked Loops, Fixed Bandpass Filters with AFC compensation, Tracking Bandpass Filters and Synthetic Bandpass Filters with AFC (also referred to as Zero Frequency-Bandpass Filter with AFC [2]).

The X2 (X4) Multiplier Carrier Recovery technique for BPSK (QPSK) respectively have been labelled as the standards for performance comparison and have been used heavily in past satellite communications, especially in burst mode applications where acquisition time and reliable burst to burst synchronization is a high priority.

The XN multiplier is deficient in one main area when compared to other Carrier Recovery techniques. As a result of this multiplication process, the carriers frequency uncertainty and phase noise spectral density are spread N times those of the input PSK signals. For moderate to high data rate systems, this deficiency poses no practical limitations. However for low data rate systems (i.e., data rates comparable to the PSK frequency uncertainty) a heavy penalty exists (see NASA Modem Study Memo "Satellite Link RF Oscillator Phase Noise Impact on Carrier Recovery of Programmable Rate Digital Satellite Modem").

In a similar manner as before, we now assess the characteristics of the XN Multiplier Carrier Recovery scheme to the specific work study requirements.

The XN Multiplier can support programmable data rates without
implementation changes provided that the Carrier Recovery Noise
Bandwidth is large enough to pass the composite RF Oscillator Phase
Noise used in the satellite link and small enough to provide minimum
performance degradation caused by recovered carrier jitter. The former
issue was addressed in the above referenced memo which indicates a
minimum noise bandwidth of 4 KHz (8.5 KHz) for Ku-Band (Ka-Band)
respectively using a X4 Multiplier. Figure 2, taken from Reference [2],
details the implementation loss -vs- Carrier Recovery Bandwidth for
QPSK. Allocating a 0.25 dB loss due to Finite Carrier Recovery
Bandwidth translates into a minimum data rate of 100 KBS (215 KBS) for
Ku-Band (Ka-Band) respectively. The XN multiplier principle is capable
of supporting M-ary PSK [3], however, the implementation frequency of
the Carrier Noise Bandwidth Filter changes as well as the order and
frequency range of the nonlinearity. A positive advantage of this
technique when used without a phase locked loop is that it is the
standard technique used for burst mode (TDMA) applications. Similar to
the pilot-tone scheme the XN Multiplier does not hinder or put
constraints on Clock Recovery/Bit Synchronization or the methodology
used for receive side data filtering. This technique however is not
supported with digital signal processing technique and is visioned as an
analog implementation scheme. This technique is however well suited for
satellite communications and is currently used in many early digital PSK
modems.

° INVERSE MODULATOR (RE-MODULATOR)

The Inverse Modulator Carrier Recovery scheme generates a "raw" carrier
component at the same PSK Carrier Frequency by removing the modulation
from the received PSK signal by remodulating the IF PSK Signal with the
demodulators output symbol data. In essence, the demodulator is
composed of a demodulator and a remodulator function. Figures 3A and 3b
detail functional block diagrams of this technique [2, 4]. Figure 3a
details a configuration using a Fixed Frequency Bandpass Filter for
carrier recovery noise improvement while Figure 3b uses a Phase Locked
Loop type Filter. This technique does not suffer, the signal quality
degradations and center frequency increases as those of the XN
Multiplier scheme. This can be seen by re-inspecting Figure 2, i.e.,
the Inverse Modulator Carrier Recovery Noise Bandwidth can be twice that
of the X4 Multiplier for 0.25 dB degradation allocation at 10^{-4} BER.
However, this technique suffers in two main areas: First, the added
complexity of the additional modulator function increases the product
cost. Second, the broadband IF PSK signal delay tends to become
unpractical at low data rates. These issues tend to limit the use of
this technique to high data rate systems (i.e., > 10 MBS).

Maintaining our assessment criteria to the work study requirement we
draw the following conclusions:

The Inverse Modulator does not support programmable data rates unless
certain restrictions are made: First, a lower data rate limit of
approximately 10 MBS (QPSK) based upon practical hardware I.F. delay
considerations are necessary, and second, the Baseband Arm Filters need
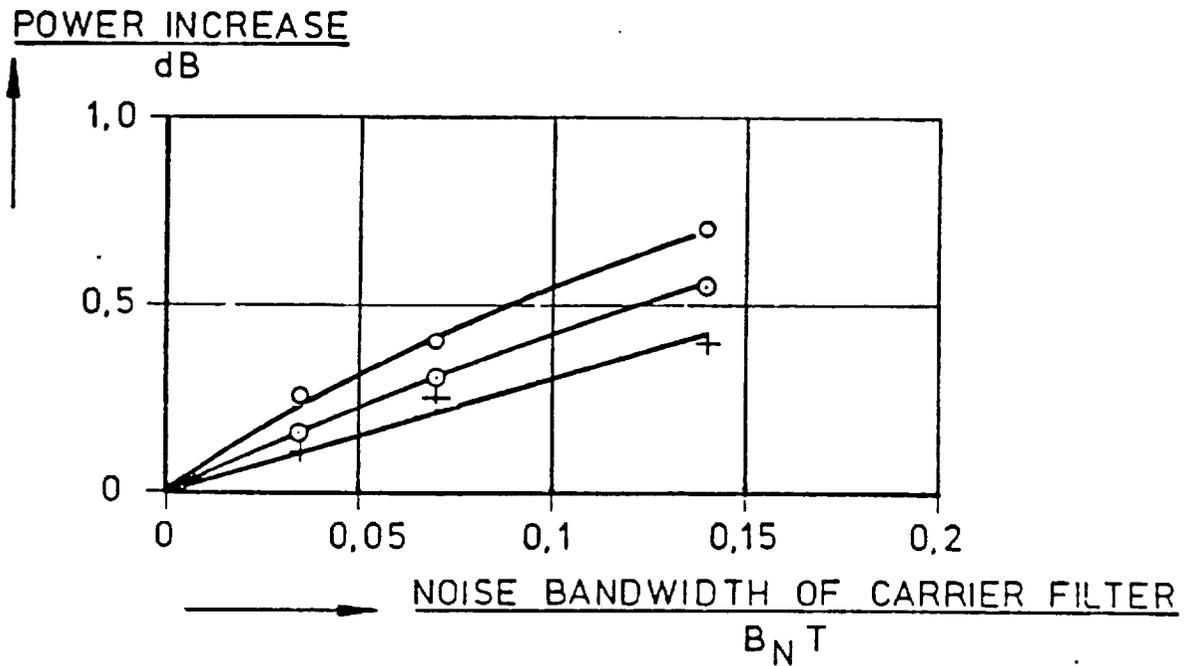
Figure 2.   Loss Caused by Carrier Recovery

Increased Power Required to Maintain Bit – Error
Probability = 10^{-4} In Steady State

o x4 Multiplier: 4th – Law Device
⊙ x4 Multiplier: Absolute Value Device
+ Remodulator

Where: T   =   Symbol Duration
        B_N =   Noise Bandwidth of Carrier Filter
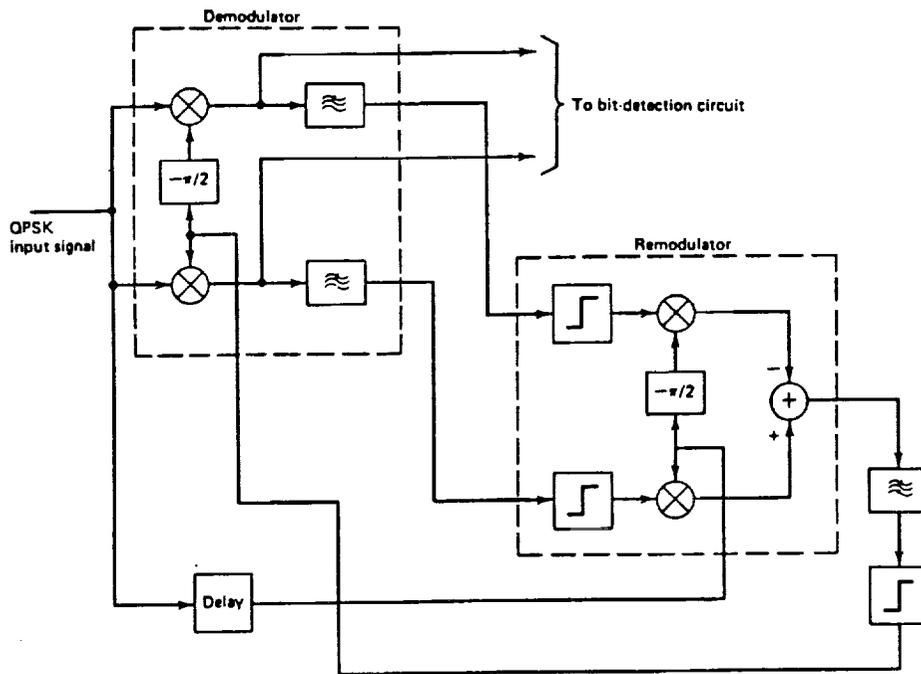
Figure 3a.   Demodulator/Remodulator
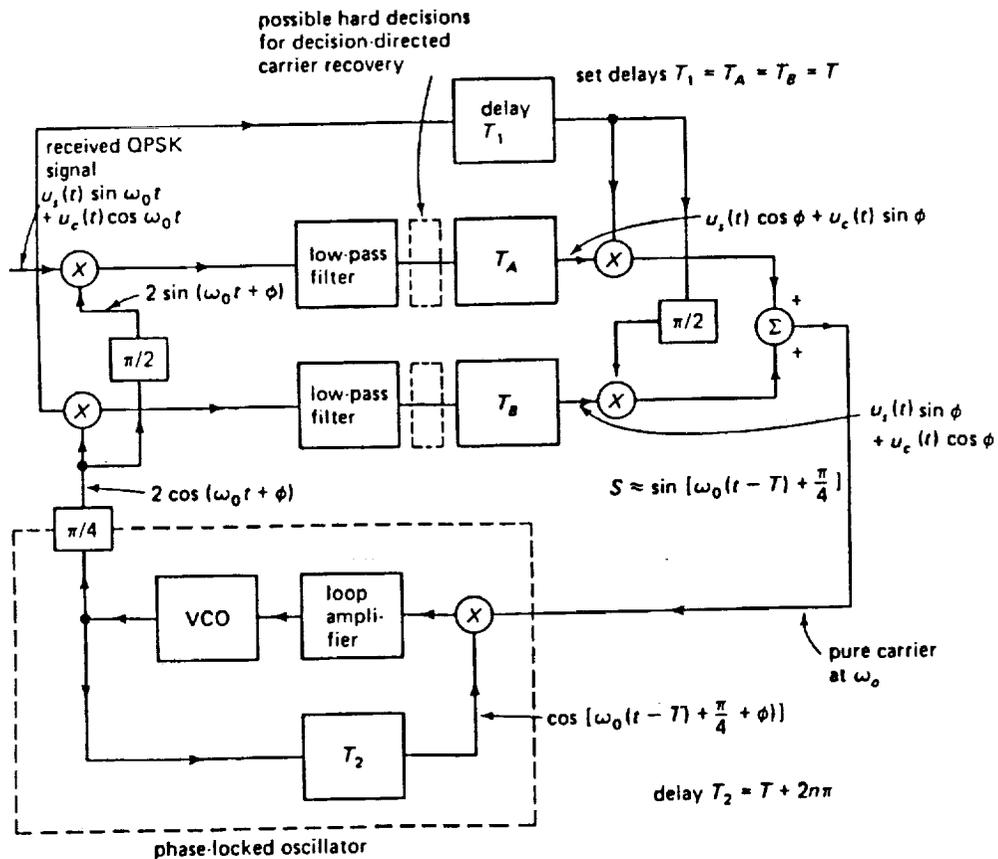
Figure 3b.   QPSK carrier recovery using reverse modulation and a phase-locked oscillator. Decision-directed carrier recovery can be performed by making hard decisions as shown in the dashed boxes in the diagram.

to be static for all data rates (i.e., optimized for the highest data rate). The time delay of these filters must be precisely matched and in essence necessitates the broadband PSK signal delay value needed (i.e., limiters, multipliers and combiners are typically broadband devices which provide little delay).

The Inverse Modulator scheme will support both BPSK and QPSK Modulation formats with simple switchable modifications to the remodulator circuitry (i.e., only one multiplier needed for BPSK). The Inverse Modulator utilizes the demodulated symbol streams which have been noise filtered to create the "raw" carrier component. Typically these filters are those used to optimumly filter the symbol data prior to detection. Traditionally, frequency domain type filters have been utilized. With this type of Inverse Modulator Carrier Recovery scheme no constraints are placed on Clock Recovery or Bit Synchronization.

If Integrate and Dump type Arm Filters are utilized, then the Carrier Recovery requires the Symbol Clock to operate. This necessitates a design implementation which supports either parallel independent Clock and Carrier Recovery processing or an implementation where both Clock and Carrier Recovery can occur simultaneously. In the latter case, one must safeguard that acquisition and synchronization of both Carrier and Clock occurs with robustness in order to be viable for Burst Mode Applications. The Inverse Modulator scheme does not lend itself well to standard Programmable Rate Digital Filtering techniques in the Arm Filter Paths since the time delay of this filtering process is related to the symbol rate. If we were to "pad" the Digital Filter Delay for all rates to be equal to that of the lowest data rate a viable implementation could be supported with a single common PSK Time Delay. "Pad" in this context is delay time which can be implemented digitally via shift registers. With this approach, Programmable Data Rates which are integer multiples of the lowest data rate would be viable. Another alternative is to utilize independent digital filtering on the symbol data prior to detection outside (in parallel with) the Arm Filter Paths of the Remodulator. In general, only small portions of the Inverse Modulator (i.e., Baseband Processing) can be implemented with Digital Signal Processing. Most of the implementation still requires Analog Processing. The Inverse Modulator Carrier Recovery scheme is viable in satellite communications for higher data rates and has been shown to out perform the X4 Multiplier scheme in acquisition response time for Burst Mode Applications [2].

COSTAS LOOP

The Costas Loop was the first Carrier Recovery technique used which does not generate a "raw" carrier component. With this technique (and those to follow) a VCO Steering Voltage is generated by non-linear signal processing of the Baseband Demodulated Symbol Streams. This steering voltage synchronizes the VCO phase to be at the precise reference for optimum demodulation. The conventional Bi-Phase and Quadriphase Costas Loop Function Block Diagrams are shown in Figure 4. The output of the Control Signal Multiplier in the Bi-Phase Costas Loop is IQ or SINØ times COSØ, where Ø is the Phase Error from nominal.

8-9
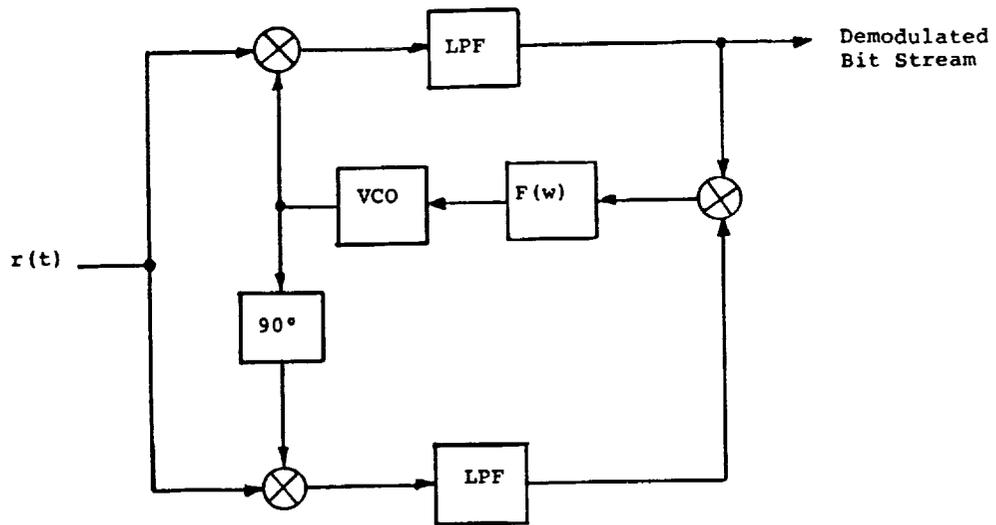
Figure 4a.   BPSK Costas Loop
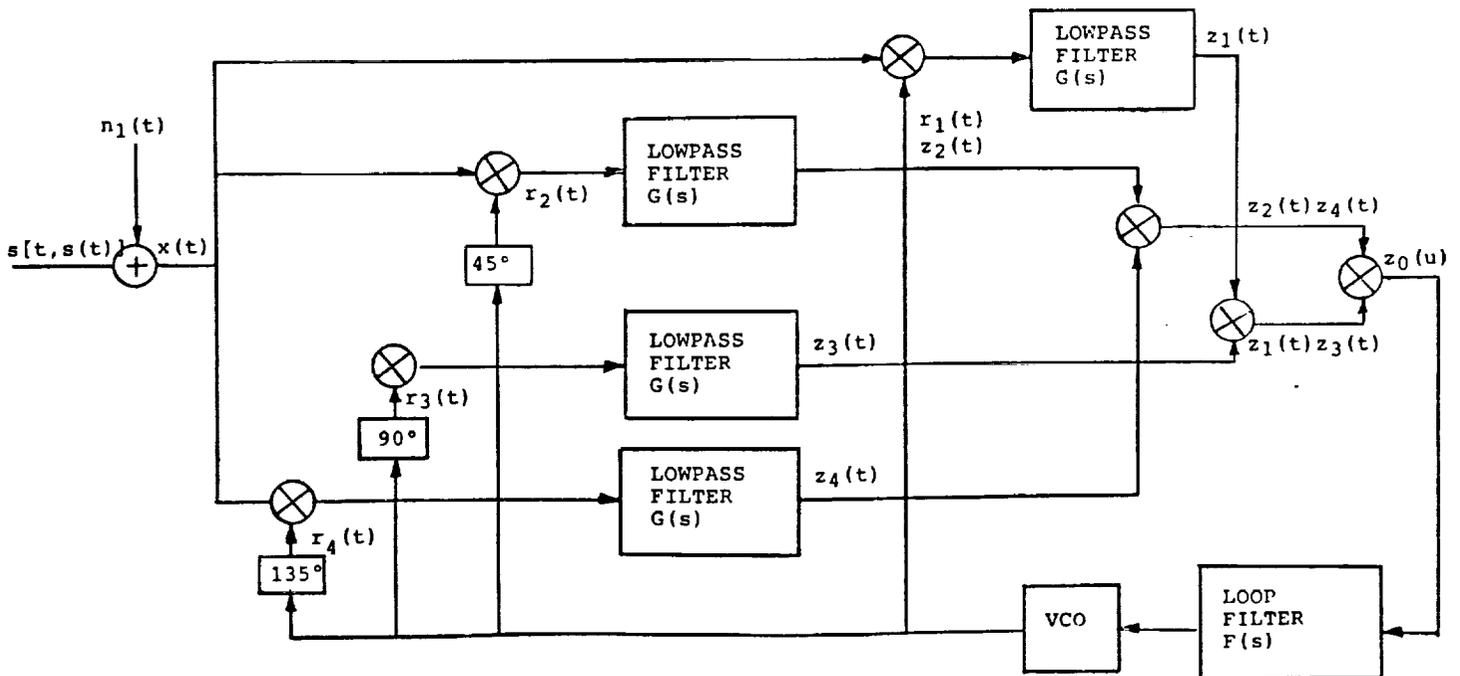
Figure 4b.   A Conventional Quadriphase Costas Loop

The Bi-Phase Costas Loop has been shown to have the same performance as the squaring loop (X2 Multiplier) assuming equivalent bandwidth filtering. The Costas Loop is often preferred over the previously mentioned techniques because it is a closed loop scheme which minimizes recovered carrier phase offsets due to center frequency uncertainty, alignment movements and such. One must however, be careful to match the group delay of the arm filters for optimum performance. The conventional Quadri-Phase Costas Loop complexity has resulted in many modifications to simplify its implementation. Figure 5 from Reference [3] details a block diagram of a decision directed 4th order Costas Loop using Integrate and Dump Filtering (also called Quadri-Phase Decision Feedback Loop). In this diagram, the steering voltage control equation is $I\hat{Q} - Q\hat{I}$ where I and Q are the analog symbols and $\hat{I}$ and $\hat{Q}$ are concurrent symbol state estimates.

The Integrate and Dump Loop Arm Filters can be replaced with Passive Low Pass Filters thus eliminating the need for symbol clock and the baseband symbol delay processing. Numerous papers have been written regarding acquisition enhancements and lock detection for various forms of Costas Loop implementations [5], [6], and [7].

Although the conventional Costas type loops do not require the analog IF Signal Processing as the techniques which generate a "raw" carrier component, they still need Analog Four Quadrant Multipliers at baseband. This one issue is the key stumbling block which prevents the techniques thus far discussed from being implemented with true Digital Signal Processing.

In assessing the Costas type Carrier Recovery schemes (decision directed as well) to the work study requirements, the following conclusions can be made.

The conventional Costas type loops support programmable data rates provided that the In-Phase and Quadrature Arm Filters have identical shapes and time delays. Decision feedback lessens the requirements of the Analog Four Quadrant Multiplier to one of a "chopper" type, at the expense of adding an analog baseband time delay. This time delay is required on the analog signal path such that the decision signal is coincident in real time. With Non-Integrate and Dump Filtering, this delay can be made short and constant (i.e., high speed comparator propagation delay). When using Integrate and Dump Filtering this time delay will be one symbol duration and varies with the data rate selected. As a result of this variation we can conclude that a decision directed Costas Loop with Integrate and Dump Filtering does not support a modem with true programmable rate structure.

Some questions arise with this scheme and other ones which do not generate a "raw" carrier as to their ability to acquire properly in the burst mode (i.e., the phantom hang-up problem of the phase lock loop when initial loop phasing is precisely 180° off). These questions can only be answered after rigorous testing of the design implementation. No constraints are placed on Clock Recovery and Bit Synchronization unless Integrate and Dump type Filters are used. Standard digital
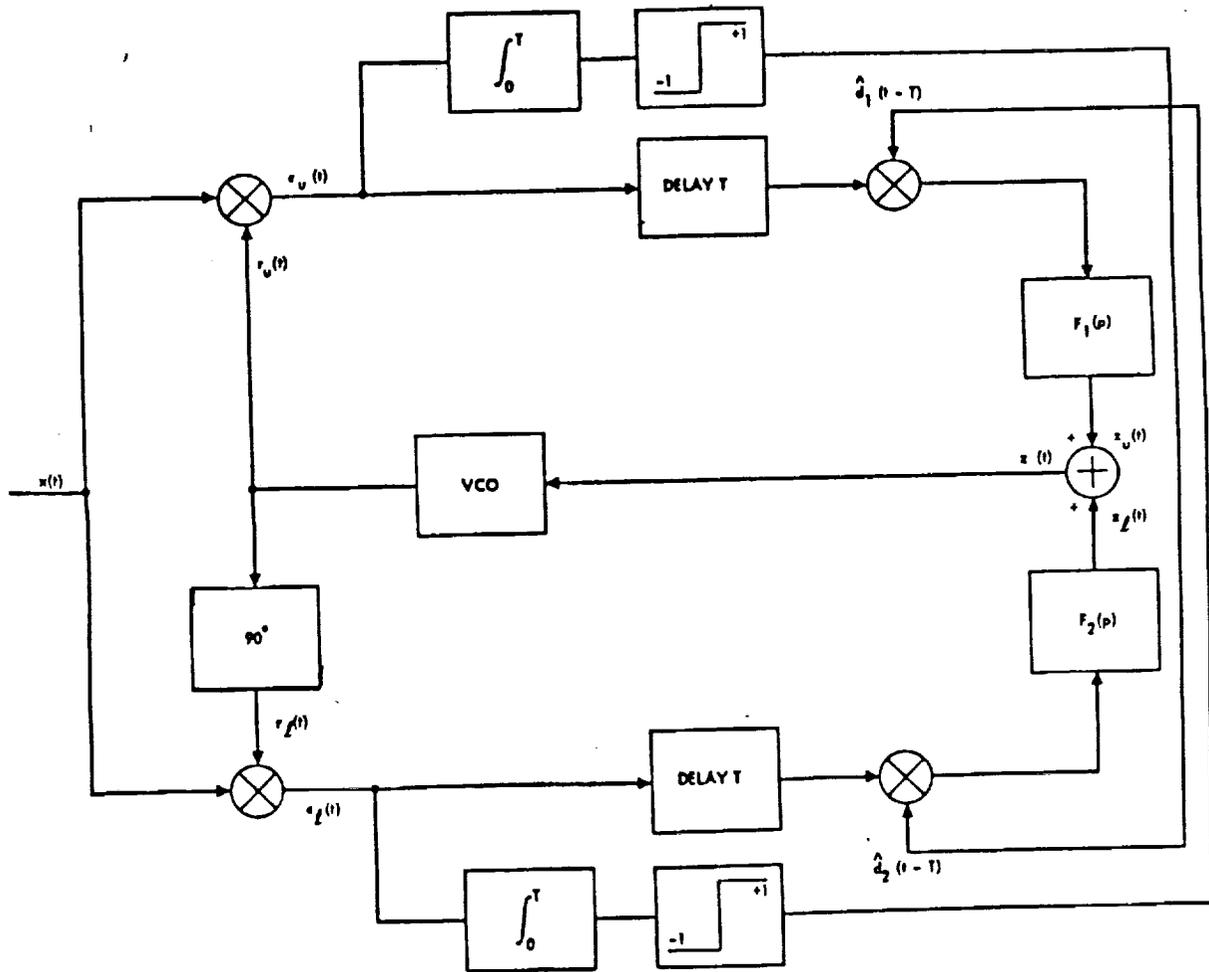
Figure 5. Decision-Directed 4th Order Costas Loop with Integrate and Dump Filtering

filtering techniques are supported in the Costas Loop Arm Filters provided that the time delay and shape factor differences through the In-Phase and Quadrature Legs is minimized. These requirements are easily satisfied with digital filtering assuming that the same coefficients, length and clock is used in both arm legs.

Costas type techniques lend themselves well in the utility of DSP in hardware implementations when compared to the "raw" carrier schemes mentioned thus far. Finally, the Costas type techniques are viable in both high and low SNR applications. The latter implementations are viable for satellite communications and presently are the most popular techniques used for continuous mode applications of both low and high data rate systems.

° DSP OF DEMODULATED SYMBOL STREAMS

Recent technology trends in satellite communications and the line of sight digital radio areas have extended digital modems bandwidth efficiencies beyond 6 bits/hz. As a result, much work has been done regarding carrier synchronization for M-ary PSK and quadrature shift keying (QASK) modulation formats. The thrust of most of the recent work in this area focuses on carrier recovery/synchronization techniques based upon practical implementations of the well known Maximum A Posteriori (MAP) estimation technique of deriving "optimum" receiver structures.

Figure 6 from Reference [8] shows the functional block diagrams of MAP Estimation Carrier Recovery Loops for BPSK and QPSK modulations. In general, closed loop structures have been impractical because of the difficulty of implementing the hyperbolic tangent non-linearity. As a result, practical designs employing approximations of

$$TAN\ H\ (X)\ =\ Sign\ (X) \qquad High\ SNR$$

$$and \qquad TAN\ H\ (X)\ =\ (X) \qquad Low\ SNR$$

are found. The author shows that by approximating the hyperbolic tangent non-linearity by the first two terms in the power series, i.e.,

$$TAN\ H\ (X)\ =\ X\ -\ X^3/3$$

an interesting practical realization of this loop results which applies at low SNR ratio's (see Figure 7). Indeed, the Error Signal in this loop is formed by multiplying the Error Signal and Lock Detector Output Signal of a Conventional Bi-Phase Costas Loop. We also note from Figure 7 that such a Quadriphase Loop can be constructed using only a pair of Quadrature Reference Signals and a pair of Arm Filters, as opposed to the four required in conventional Quadriphase Costas Loops (see Figure 4b). The loop of Figure 7 also has the advantage that it can easily be switched from BPSK to QPSK mode which is a study objective.

The author shows that the conventional Costas Loop, the X4 Multiplier and the configuration shown in Figure 7 are all low SNR realizations of
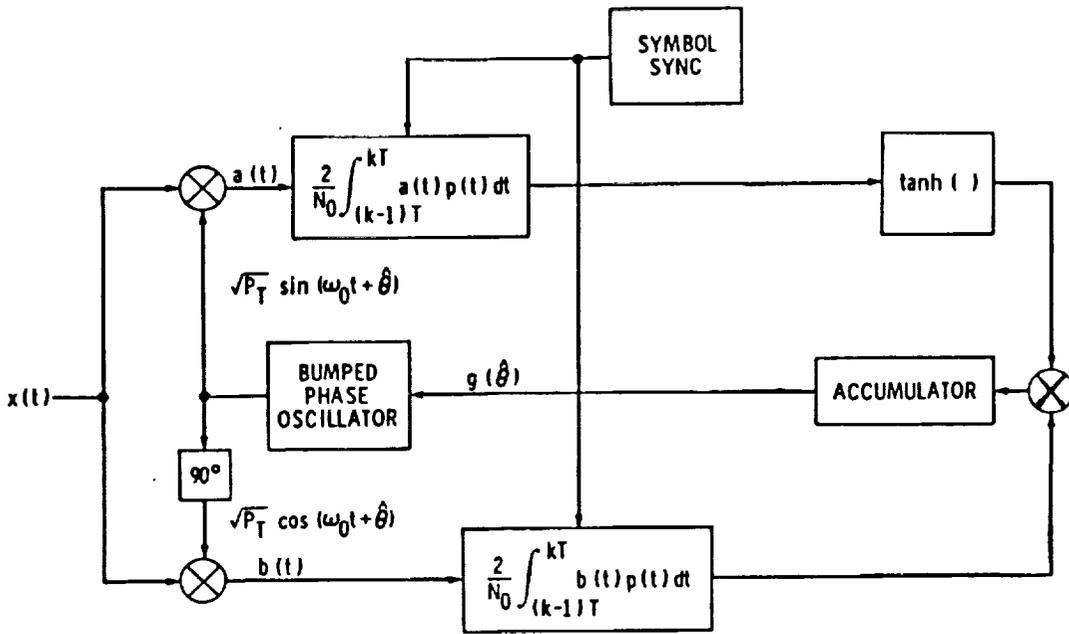
Figure 6a. The MAP Estimation Loop for
Carrier Phase (BPSK)
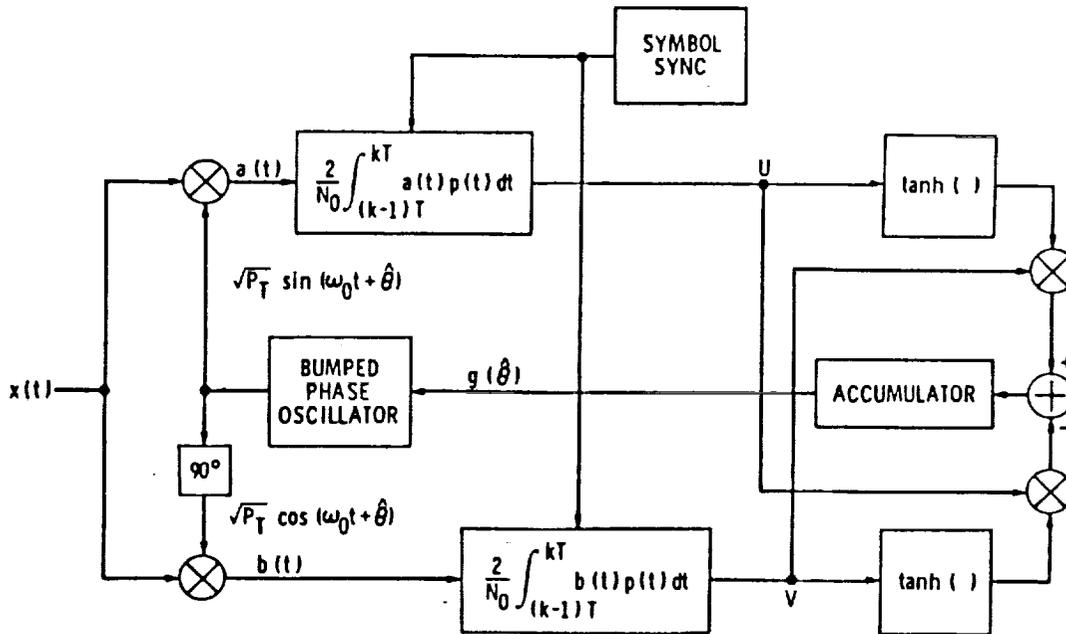
Figure 6b. The MAP Estimation Loop for
Carrier Phase (QPSK)
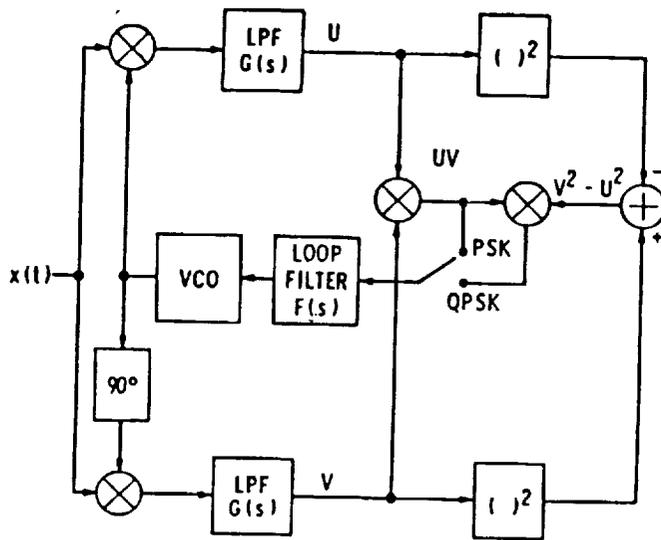
Figure 7. A Practical Realization
of the MAP Estimation
Loop, Passive Arm Filters,
Small SNR

the MAP Estimation Loop for QPSK and that the decision directed (polarity type) is a high SNR realization of the MAP Estimation Loop (Non-Integrate and Dump Arm Filters assumed).

Figure 8 from Reference [9] illustrates a universal Carrier Recovery technique viable for QASK and PSK Signal sets. This technique can be implemented digitally by baseband processing of the In-Phase and Quadrature Symbol Streams using only comparators, "EX OR" Gates and Adders (summers).

Figure 9 from Reference [10] illustrates yet another practical implementation which is truly digitally implemented. The block diagram shown is the Carrier Recovery scheme implemented for a 16 QAM Demodulator. For QPSK configurations, the Selective Gate Signal is not required and the hardware simplifies to the Error Signal being directly connected to the Loop Filter Input (i.e., Full Wave Rectifier Paths and Flip Flop are deleted). Multipoint Communications Corporation utilizes this Network to regulate the phase of the recovered carrier from an X4 Multiplier Tracking Filter Carrier Recovery scheme in its current Partial Band TDMA Burst Modem. The EXOR Control Output Signal is sampled only when a burst is present and held otherwise. This Network dynamically compensates for practical hardware Phase Shift variations over time in the Carrier Recovery circuitry via closed loop feedback thus insuring optimum recovered carrier phasing.

Many other digital implementations have been suggested which can be shown to be derivatives of the ones previously stated. The performance of these latter digital implementations are characterized only for the line of sight radio applications which are considered high SNR by MAP Estimation standards. Their performance at low SNR is uncertain, therefore, their application in digital satellite communications with high performance Forward Error Correction systems is questionable at this time.

In assessing the DSP of Demodulated Symbol Stream Carrier Recovery schemes to the study requirements, the following conclusions can be made.

Practically speaking, programmable data rates can be supported by all of these techniques assuming that Non-Integrate and Dump Arm Filters are used (following the same rationale described under the Costas type Carrier Recovery). Most of the techniques described support PSK and QASK Modulation formats. Simon [8] has shown a common hardware implementation which supports both BPSK and QPSK with minor hardware modifications (i.e., Figure 7). For Burst Mode Operation, one needs to include provisions for fast acquisition and lock detection. Many enhancements and implementation modifications to the phase locked loop Carrier Recovery schemes have been presented which should insure robust and fast acquisition. The issues remaining in this area relate to hardware design complexity verses the degree of acquisition robustness. These techniques are no different than the others regarding constraints on Clock Recovery/Bit Synchronization (i.e., it is an integrate and dump issue not a carrier recovery one). These schemes relate best when considering Digital Signal Processing and Digital Filtering implementations.
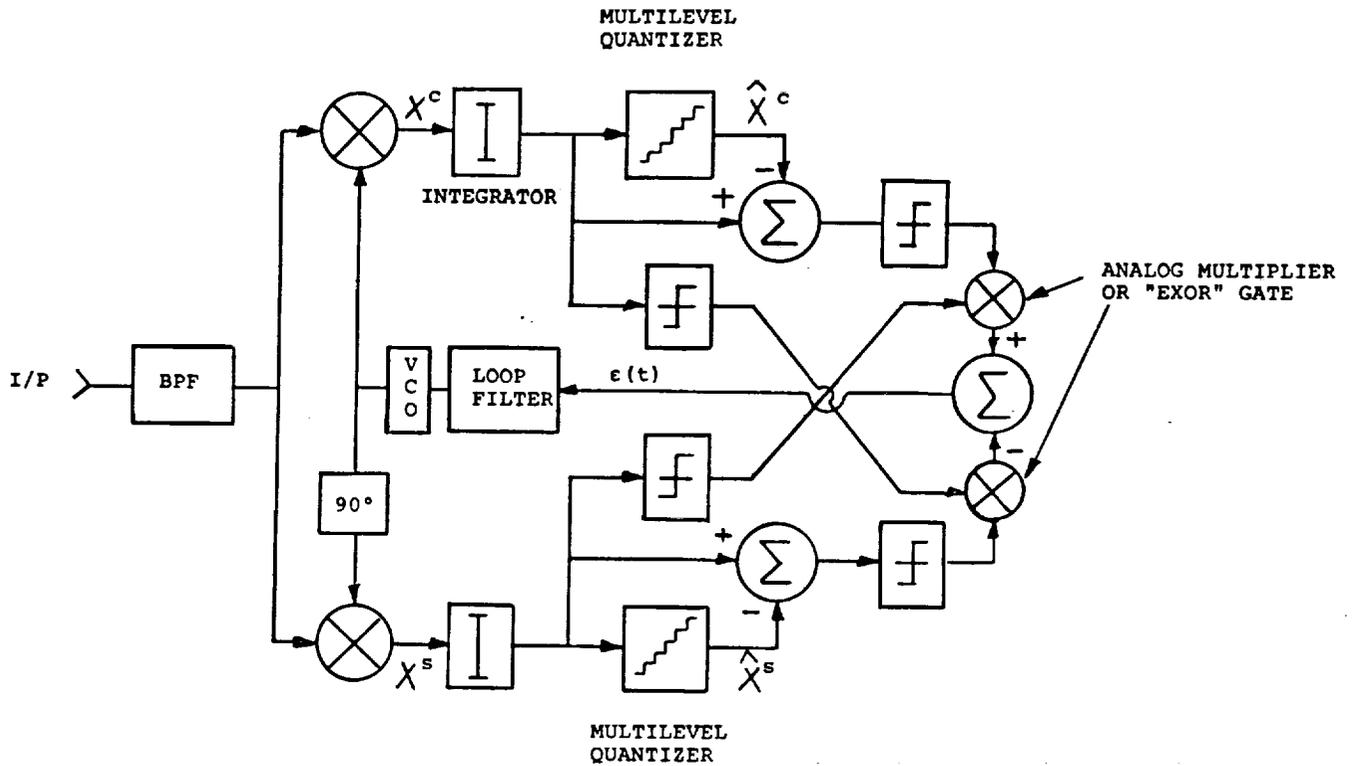
Figure 8. Block Diagram of the Carrier Recovery with Selective Gated PLL
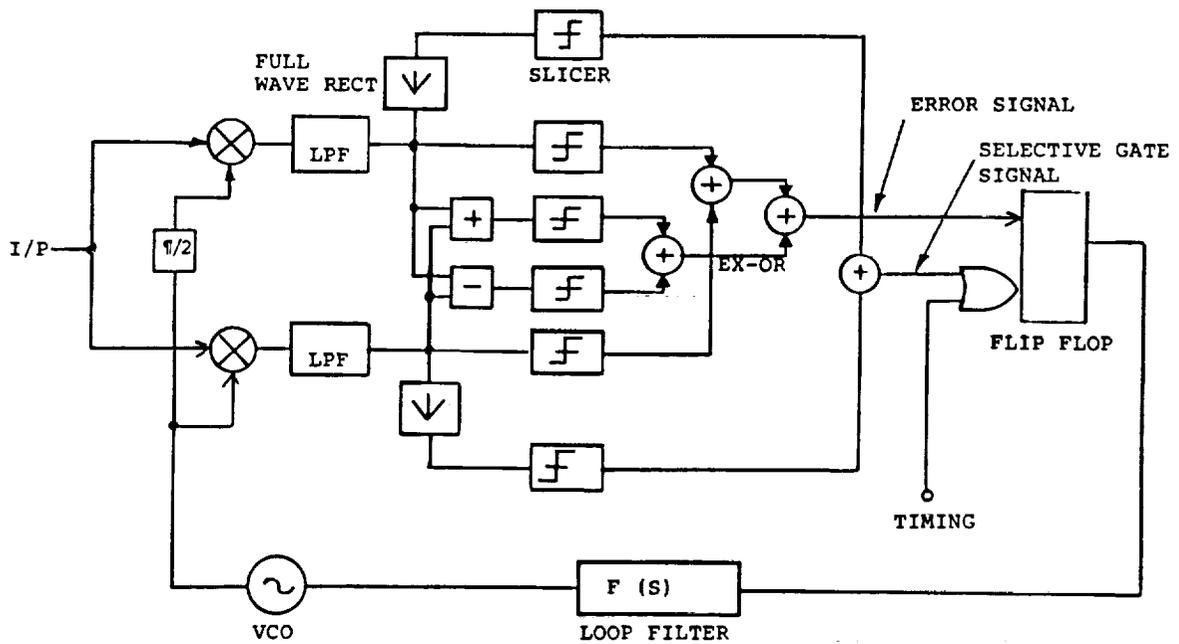
Figure 9. Proposed Carrier Recovery Loop Diagram

CANDIDATE CHOICE SUMMARY

No one candidate Carrier Recovery scheme is superior to the others in satisfying all the study requirements. In fact, alot of the Baseband Signal Processing schemes are so similar that they could be classified as a single set type. We make our choice based upon prioritizing the importance of the individual study requirements given our practical knowledge of hardware in the evolution of digital satellite modem products.

Priority	Requirement
1	Viable in Satellite Communications
2	Supports Programmable Data Rates
3	Supports Digital Filtering Techniques prior to Data Detection
4	DSP Implementation as compared to analog
5	All others

Based upon this priority structure, the MAP Estimation Loop approach detailed in Figure 7 is chosen.

IMPLEMENTATION

The hardware implementation approach suggested is illustrated in Figure 10. The Arm Filters of the Carrier Recovery Loop would be the receive side Nyquist Filters which would be implemented with digital filtering techniques as discussed under a separate topic in this study report. Provisions are included for Baseband Clock Recovery if needed here, thus maintaining design flexibility. The Nyquist Digital Filter outputs feed the Carrier Recovery Digital Logic as well as the detection circuitry with soft decision symbol streams. The implementation shown allows for baseband processing without "detected" symbol data. However, simple modifications to include processing with detected soft decision data are easily accommodated. Both version are suggested in the implementation in order to investigate whether or not noise performance advantages and joint acquisition of clock and carrier acquisition response time penalties exist. The digital logic function would generate a digital word implementation of the mathematical steering voltage equations shown.

The arithmetic multiplier and squarer functions will be implemented digitally either in high speed "proms" or digital multiplier devices depending on the top end speed requirement which are set by the highest data rate and word size. The digital error signal will then be processed by the loop filter which is configured as another digital filter whose coefficients are fixed and whose clock rate can change with rate. This approach allows for optimizing the recovered carrier noise bandwidth verses rate by simple selection of the clock frequency. The

Figure 10. Proposed Carrier Recovery
Hardware Implementation Diagram

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recovery carrier oscillator itself can be implemented as a numerically controlled oscillator which can be driven directly from the digital loop filter or an analog VCO. In the latter case the digital loop filter output will be converted back to analog using a D to A converter.

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[2] "Carrier and Clock Synchronization for TDMA Digital Communications", F.M. Gardner, European Space Agency Rep., ESA TM-169 (EST EC), December 1976.

[3] "Carrier Synchronization and Detection of Poly Phase Signals", W.C. Lindsey and M.K. Simon, IEEE Trans. on Communications, June 1972.

[4] "Carrier Synchronizer for Coherent Detection of High Speed Four-Phase-Shift-Keyed Signals", H. Yamamoto, K. Hirade and Y. Watanabe, IEEE Trans. on Communications, August 1972.

[5] "Hangup in Phase-Locked Loops", F.M. Gardner, IEEE Trans. on Communications, October 1977.

[6] "Improving Frequency Acquisition of a Costas Loop", C.R. Cahn, IEEE Trans. On Communications, December 1977.

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[8] "Optimum Receiver Structures for Phase Multiplexed Modulations", M.K. Simon, IEEE Trans. on Communications, June 1978.

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[10] "Design and Performance of a 200 MBS/S 16 QAM Digital Radio System, I. Horikawa, T. Murase and Y. Saito, IEEE Trans on Communications, December 1979.

MEMORANDUM

TO: NASA Modem Study File

FROM: Robert L. Wallace

SUBJECT: TIMING RECOVERY AND DATA SAMPLING

DATE: October 19, 1988

MCC FILE MCC-93

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INTRODUCTION

The objective of this memo is to identify the most favorable Timing Recovery Technique and its performance attributes which can be utilized by a Programmable Data Rate Digital Satellite Modem operating in a Multi-Carrier Transponder environment. We initiate our discussion by identifying the various types of Timing Recovery Techniques which are described in technical literature and used in digital communications. The operational characteristics and features of each Timing Recovery Scheme will be presented and a comparison to the study requirements will be made.

A candidate scheme will then be chosen based upon the one which offers the most favorable attributes. The performance impact of the candidate Timing Recovery Scheme on Soft Decision Data Sampling (detection) will also be assessed.

Lastly, viable hardware design techniques which utilize DSP Technology will be described for the various functions required in the implementation of the technique. This is concluded with an overall implementation diagram of the proposed Hardware Timing Recovery approach.

ASSESSMENT OF TIMING RECOVERY TECHNIQUES

Timing Recovery Techniques are defined as those which recover a Synchronous Symbol Clock Signal from Non-Linear Signal Processing of either the IF PSK Signal or the Demodulated Baseband Symbol Streams (the latter type is also referred to as Bit Synchronization). Following this Non-Linear Signal Processing is some type of narrow filter centered at the Symbol Clock Frequency which is used to enhance the signal to jitter and noise ratio of the Recovered Clock Signal. Typical applications utilize either a fixed bandpass filter followed by a limiter to remove envelope variations or some form of Phased Locked Loop.

The former type is characterized as one using Analog Signal Processing and has been used exclusively for burst mode applications where clock acquisition robustness and lock-up time consistencies are mandatory. The Phase Locked Loop type filter is used exclusively in all Continuous

Mode applications and has the advantage that it can be implemented with DSP Technology. For burst mode applications, the conventional Phase Locked Loop Filter suffers from loop "hang up" (i.e., long acquisition time if incident burst phase is 180° out of phase). However minor modification to the loop have been described (1), (2) which elevates this problem issue and insures consistent acquisition properties.

There are a vast number of different types of Timing Recovery Techniques presented in technical literature and used in existing equipment. However, all of these types fall into only two different classes (i.e., either open loop or closed loop). Both class types use non-linear processing to synchronize a local clock reference, however the closed loop class insures precise symbol clock phasing with the demodulated symbol data, which is a positive advantage when soft decision detection is required.

Clock recovery techniques can occur subsequent to or coincident with Carrier Recovery. In the former case, recovery circuits operate on the demodulated (not necessarily detected) baseband waveforms, whereas in the latter case, the recovery process operates directly on the PSK Carrier. For burst mode applications, such as TDMA the time devoted to Carrier and Bit Timing Recovery is an overhead that should be kept at a minimum to maximize the traffic throughput. As a result of this speed requirement, parallel, simultaneous Carrier Recovery and Timing Recovery Techniques are commonly utilized.

Timing Recovery Techniques have for the most part followed a similar evolution as those of Carrier Recovery. The Optimum Synchronization Technique for a signal received with additive Gaussian noise is based upon a Maximum A Posteriori (MAP) estimation of symbol location and has been described in reference (3). The MAP Synchronizer performs a correlation or matched filter operation with a non-linear weighting by the natural log of the hyperbolic cosine function (i.e., l_n COSH (x)). Practical Timing Recovery Techniques using approximations to implement the MAP Synchronizer are the "square law" and "absolute value" non-linearity types.

Since,

$$l_n \text{ COSH } (x) \cong \begin{cases} \dfrac{x^2}{2} & ; \text{ for } |X| \ll 1 \\[3mm] \dfrac{|X|}{2} & ; \text{ for } |X| \gg 1 \end{cases}$$

Another type of Open Loop Timing Recovery Scheme uses Amplitude Envelope Detection of the IF PSK Carrier when the PSK Spectrum is band limited. An example of this technique is explained in Reference 5. It can be shown that this technique is a form of even law non-linearity implemented at IF.

Yet another type of Open Loop Timing Recovery scheme which has received a lot of attention is the Delay-Line Detector. Here a clock component is generated by multiplying the received signal by its own delayed replica.

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Yet another type is labelled the Zero Crossing Detector. Here a clock component is generated by a pulse train consisting of unipolar pulses (i.e., pulse width < symbol duration) for each symbol zero crossing.

Recent attention has turned toward Closed Loop Timing Recovery Techniques because of their improved detection performance and ease of implementation using DSP Technology. Three popular schemes will be described, namely the Data Transition Tracking Loop (DTTL), also called In-Phase/Mid-Phase Bit Synchronizer; the Early-Late Gate Synchronizer; and the Binary Quantized Digital Phase-Locked Loop.

Each technique mentioned will now be described in more detail. The characteristics of the respective technique will also be assessed to the modem study requirements.

"SQUARE LAW"/"ABSOLUTE VALUE" NON-LINEARITY TYPES

Figure 1 depicts the various functional block diagrams commonly used for the "Square Law"/"Absolute Value" Non-Linearity Timing Recovery Technique. Both IF and Baseband Schemes are viable with either non-linearity type. For a band limited system a filter matched to the received PSK Signal maximizes the SNR at the sampling instant. However, this filter type produces a larger degree of Zero Crossing Jitter on the Symbol Data Streams the more the band limiting. It follows that the best data demodulation filter is not necessarily the optimum for Clock Recovery. Reference (4) has shown that the amplitude of the Recovered Symbol Clock using a Nyquist pre-filter and a "Square Law" non-linearity is proportional to the roll-off factor Alpha (using QPSK Modulation). On the other hand, the amplitude of the Recovered Symbol Clock using an IF Envelope Detector is inversely proportional to the roll-off factor alpha (i.e., the lower alpha the more symbol clock AM).

A Digital Satellite Communications Link was simulated in Reference (4) consisting of a QPSK Modulator whose output was band limited (i.e., cosine shape, alpha factor equal to 0.5). Two Symbol Timing Recovery Non-Linearity Pre-Filters were compared. First, matched filter (i.e., cosine shaped, alpha factor equal to 0.5), second a flat filter having an equivalent baseband bandwidth of 0.8 times the symbol rate. Figure 2 shows the RMS recovered symbol clock jitter verses Eb/No for both types of non-linearities and both types of pre-filters. The clock output filter used is a single tank having a noise bandwidth symbol interval product $B_N T = 0.07$. The results show the inferiority of using the optimum demodulation filter for the Clock Recovery Pre-Filter. In addition, the results indicate that the "Absolute Value" type is superior to the "Square Law" type for the same filter type.

The author also found that either "Square Law" implementations (i.e., IF or Baseband) and the IF Envelope Detectors in general are insensitive to Carrier Phase and can be used independently of Carrier Recovery. This is not true for the "Absolute Value" Non-Linearity. In addition, the author ran simulations with perfect recovered carrier and jitter free recovered clock to assess the Eb/No degradation due to fixed timing offsets in the detection process. These results are shown in Figure 3 for QPSK Modulation.

9-3
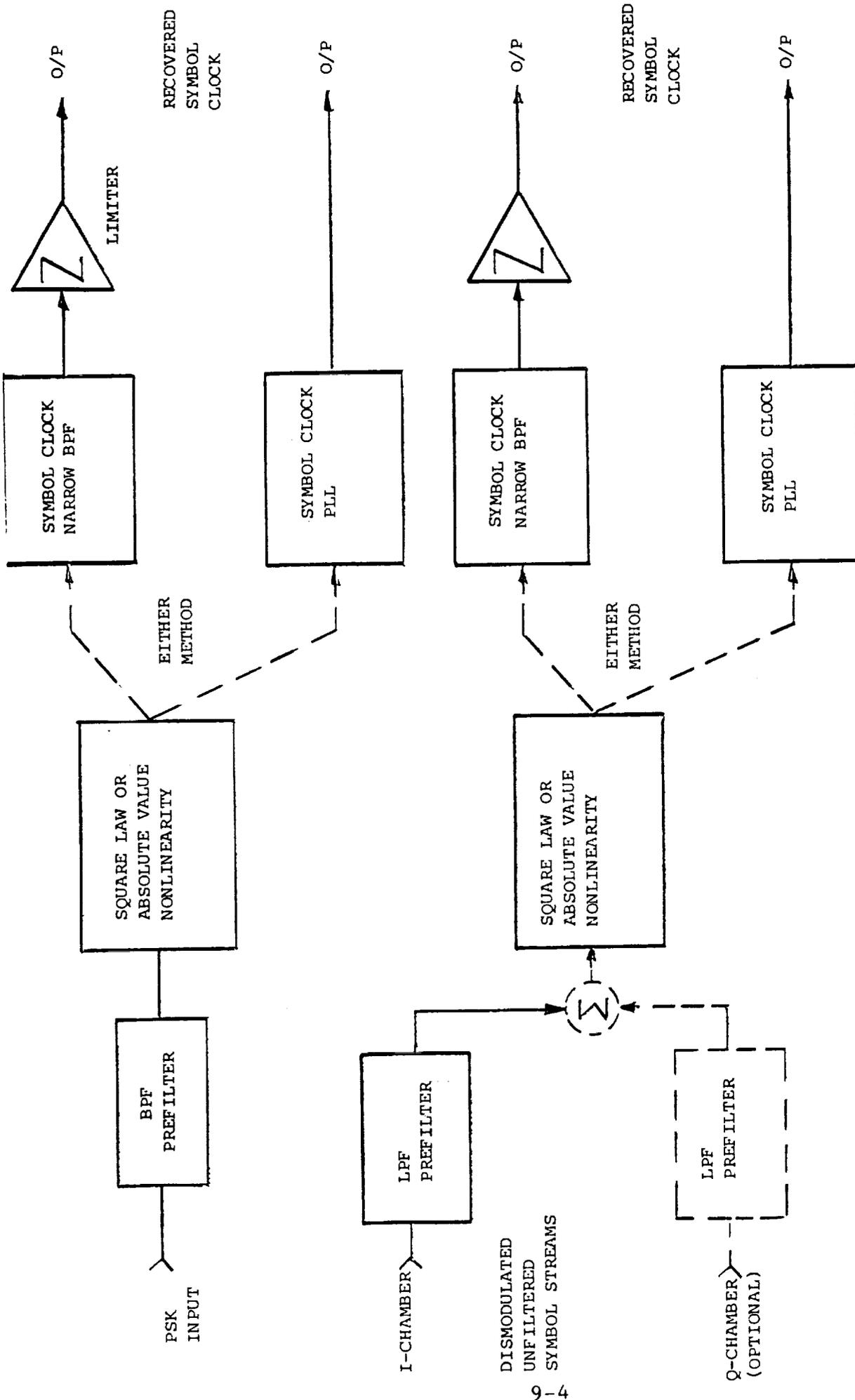
FIGURE 1

"SQUARE LAW"/"ABSOLUTE VALUE"
NONLINEARITY
TIMING RECOVERY SCHEMES

LPF - LOW PASS FILTER
BPF - BANDPASS FILTER
PLL - PHASE LOCKED LOOP

9-4
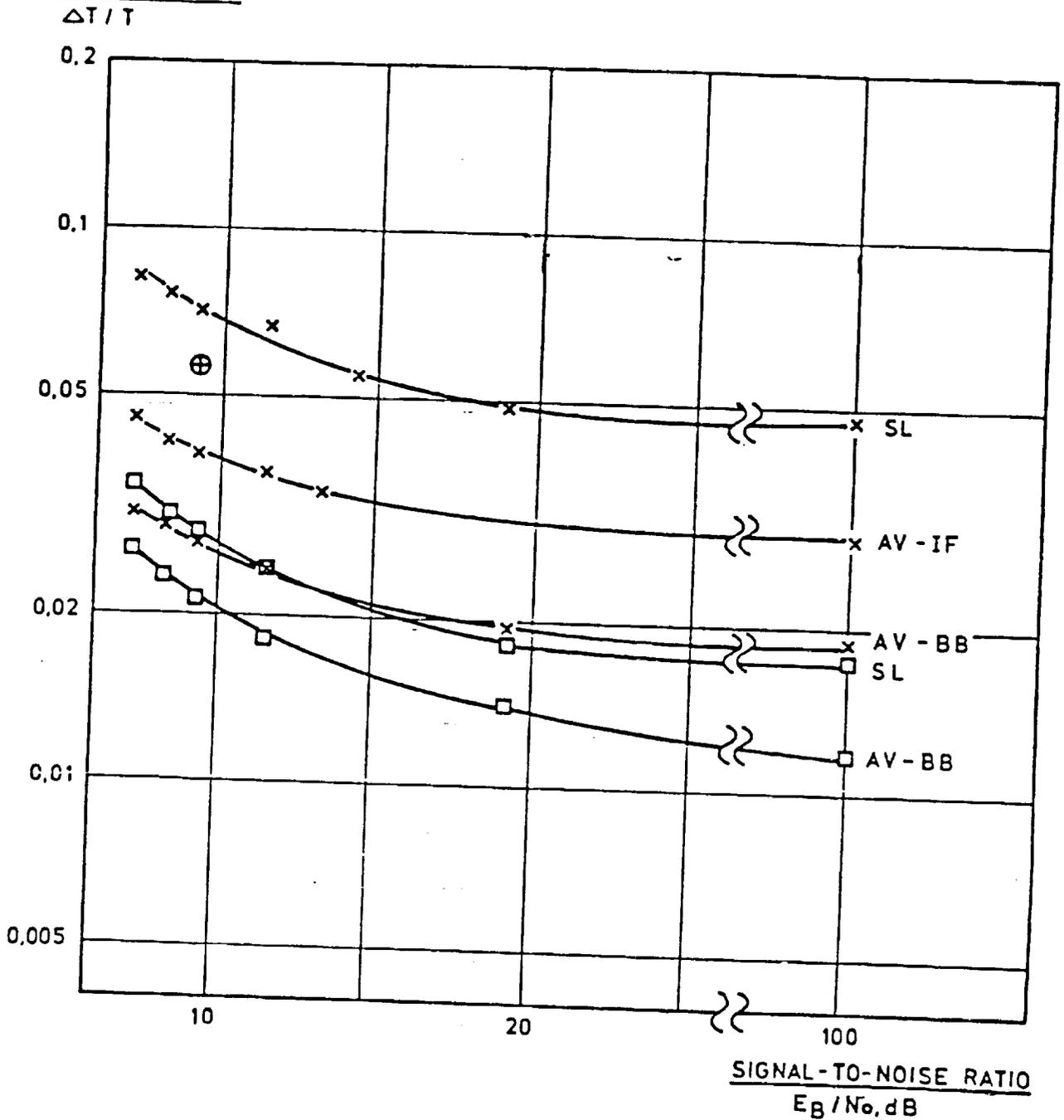
FIG. 2   TIME JITTER OF REFERENCE CLOCK

BANDWIDTH OF CLOCK FILTER ; $B_N T = 0.07$
RECEIVER FILTER :
□   FLAT (0.8 BT BANDWIDTH AT BASEBAND)
×   NYQUIST (COSINE SHAPE ALPHA = 0.5 AT BASEBAND)
SQUARE-LAW RESULTS ARE CONTAMINATED WITH
CARRIER JITTER.
SL = SQUARE-LAW
AV = ABSOLUTE VALUE
BB = BASEBAND
IF = IF
⊕ = SQUARE-LAW, NYQUIST, NO CARRIER JITTER
MODULATOR OUTPUT BANDLIMITED (I.E. COSINE FOLLOFF ALPHA = 0.5)
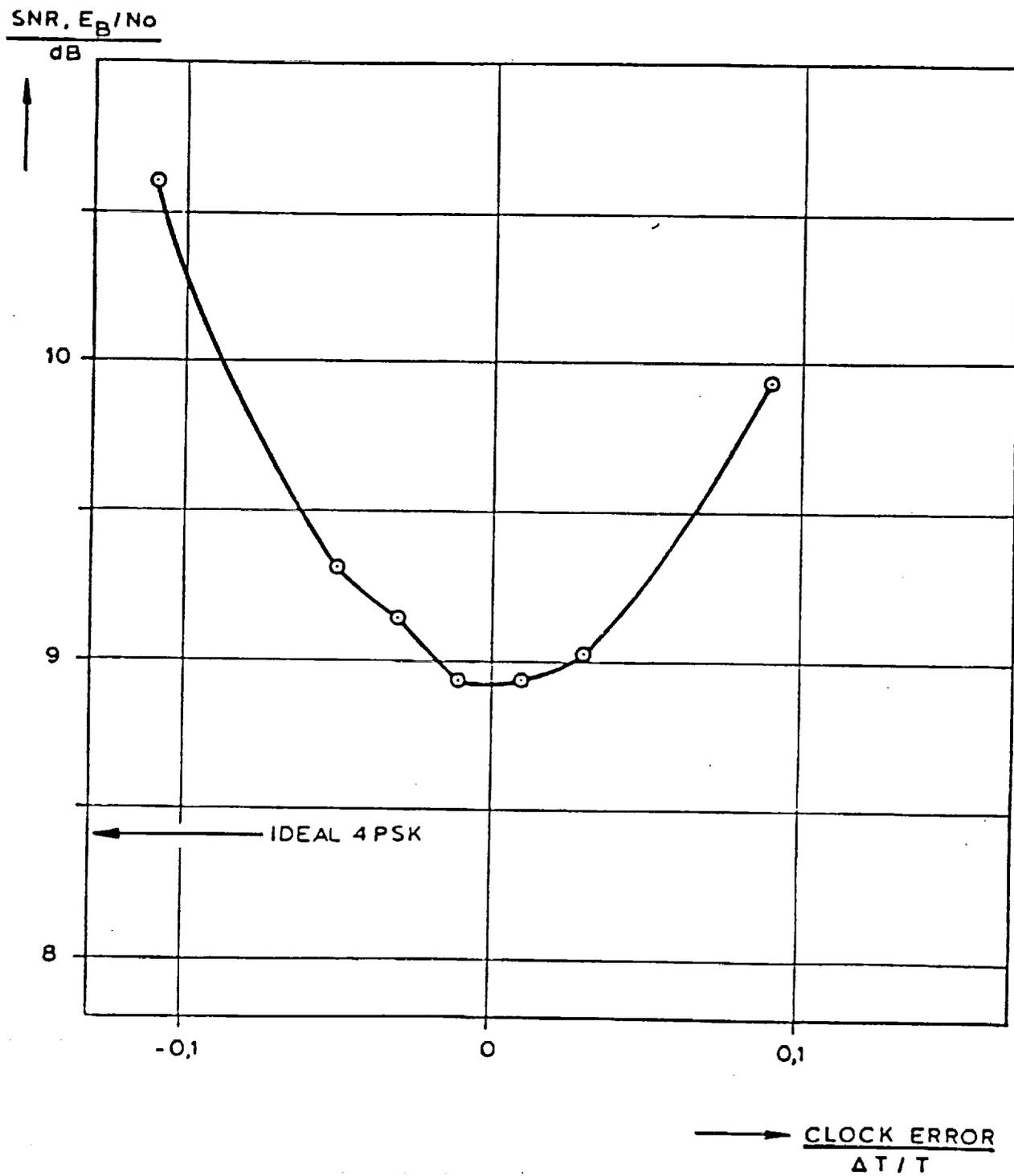
SIGNAL-TO-NOISE RATIO, E_B/N_0, NEEDED FOR $P_B = 10^{-4}$ (SIMULATION RESULTS)

FIG. 3   EFFECT OF CLOCK ERROR ON BIT ERROR

We now compare the characteristics of this timing recovery technique to those of work study objectives. The specific requirements are as follows:

° Supports Programmable Data Rates
° Supports both Burst and Continuous Modes of Operation
° Minimizes the Constraints on Carrier Recovery
° Supports an Implementation using DSP as compared to Analog Signal Processing
° Is viable in Satellite Communications

In order to support Programmable Data Rates, both the Pre-Filter Bandwidth and the Center Frequency of the Narrow Bandpass Filter after the non-linearity must tune with data rate. The former filter requirements can be satisfied either at IF or Baseband. At IF, constraints can be put on the adjacent carrier selective filter to address Clock Recovery shape requirements as well. At Baseband, another set of digital filters can be used to process the "raw" demodulated symbol streams whoses coefficients are tailored to maximize the Symbol Clock energy. The clock for this digital filter will be the same one used for the Digital Data Filters previously discussed in the Carrier Recovery section. The latter filter requirements, i.e., Variable Center Frequency Bandpass Filter, presents the real design challenge. We will outline in the hardware section of this memo two practical alternatives to this troublesome area.

The Fixed Bandpass Filter/Limiter implementation readily supports either burst or continuous modes of operation. The conventional Phase Locked Loop Bandpass Filter can suffer from the "hang-up phenomenon" which unaddressed would result in inferior burst mode performance. Many authors have addressed this issue (see Carrier Recovery Section of this study report) and have shown solutions to the phenomenon with simple hardware modifications to the basic loop.

Assuming independent clock pre-filters from Carrier Recovery Arm Filters none of the implementations constrain the Carrier Recovery methodology. On a positive note, Reference (4) has shown that the "Square Law" and Envelope Detector Scheme are truely independent of Carrier Recovery. This allows for faster burst mode acquisition properties when implemented with parallel processing.

The baseband implementation is superior to the IF implementation when considering digital rather than analog signal processing, primarily due to the frequency band of the pre-filter and non-linearity used.

All these techniques have shown to be viable in satellite communications. The bandwidth of the bandpass filter used directly relates to the jitter magnitude, which in turn relates to BER Performance degradations. A disadvantage of this technique is that it is an "Open Loop" Scheme. Other circuitry is required to properly align the recovered clock with the demodulated symbol data in the detection process.

DELAY-LINE DETECTOR

Figure 4 depicts a functional block diagram of the Delay-Line Detector which can be configured at IF or at Baseband. With this technique, the received PSK Signal (or Baseband Symbol Stream) is multiplied by its delayed replica to generate a raw symbol clock component. Following this non-linear process is a narrow Bandpass Filter centered at the Symbol Clock Frequency. The required characteristics and implementation methodology of the Bandpass Filter is identical to that needed in the Non-Linearity Timing Recovery Technique previously described, therefore its impact on the work study requirements will be the same.

The IF Implementation of this technique has received a lot of attention in technical literature for Burst Mode applications using parallel processing for Carrier and Timing Recovery. Reference (6) shows that the optimum delay value (i.e., one which maximizes SNR is a function of Carrier Frequency and not the symbol period).

Specifically,

$$\text{SNR (Maximum) occurs when } \Delta T = \frac{N}{2 f_c}$$

$$\text{SNR (Minimum) occurs when } \Delta T = \frac{(2N + 1)}{2 f_c}$$

where f_c is the carrier frequency and N is any positive integer.

Reference (7) provides updated information on this same technique operating at IF when the Channel Filter has cosine - roll off shape. This type of channel filtering is exactly what we have proposed for the modem under consideration. Figure 5 shows the Recovered Symbol Clock Jitter as a function of delay ΔT, normalized Symbol Clock Bandpass Filter Bandwidth and cosine roll off factory alpha. From these figures, we see that the jitter variance is practically independent of delay for alpha factors ≤ 0.5. In conclusion it appears that with a cosine roll off channel (alpha ≤ 0.5), minimum jitter is achieved with zero delay, whatever Eb/No is used. This situation defaults to that of the "Square Law" multiplier rectifier previously discussed.

Reference (8) describes a baseband implementation of this technique using an "Exclusive OR" gate as a multiplier. Here the ratio of the discrete symbol clock power is compared to the nearby continuous spectral power. It is shown that this ratio equals the quality factory of the Narrow Bandpass Filter following the Ex-OR gate and that it does not depend on the value of the delay element.

In evaluating this technique against the work study requirements we draw the following conclusions. Since the working environment of the proposed modem is a band limited cosine shape channel with alpha equal to 0.4, any delay value will provide optimum performance. In order to simplify hardware complexity a zero value is most optimum. This value however defaults this technique to that of the "Square Law" Multiplier previously discussed.

BAND PASS FILTER
Fo @ SYMBOL RATE

RECOVERED
SYMBOL
CLOCK

O/P

SYMBOL
CLOCK
PLL

O/P

DELAY
ΔT

IF
OR
BASEBAND INPUT

9-9
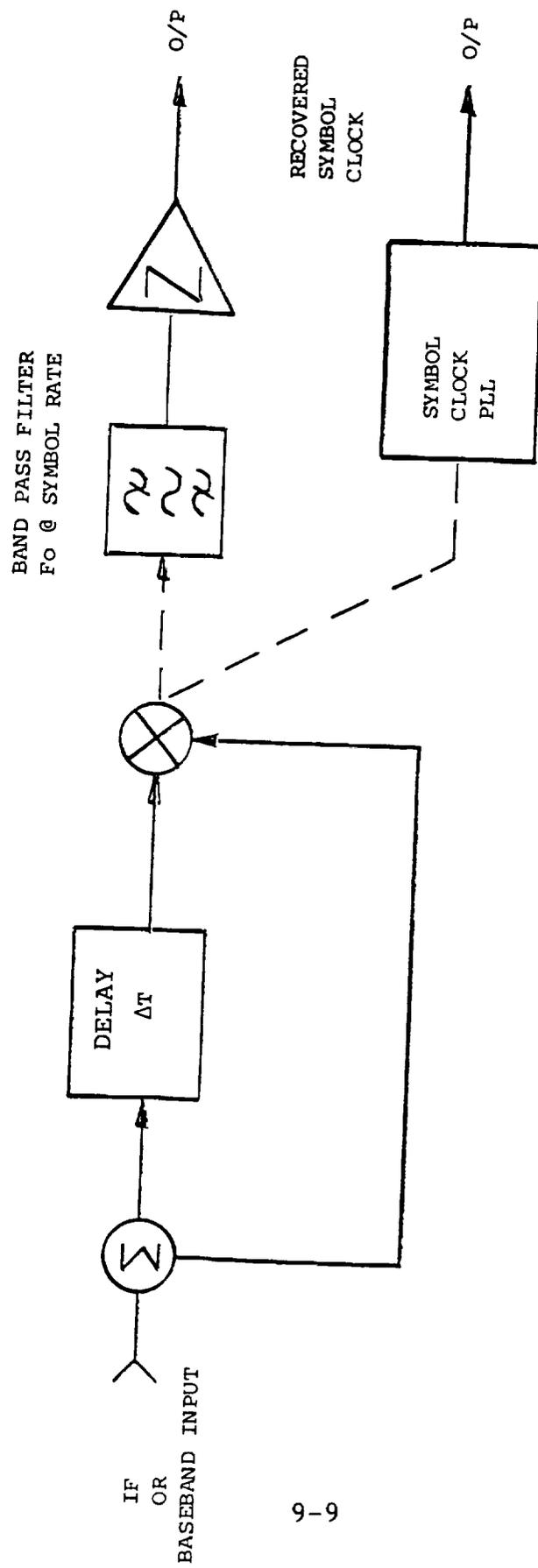
DELAY-LINE DETECTOR
FUNCTIONAL BLOCK DIAGRAM

FIGURE 4
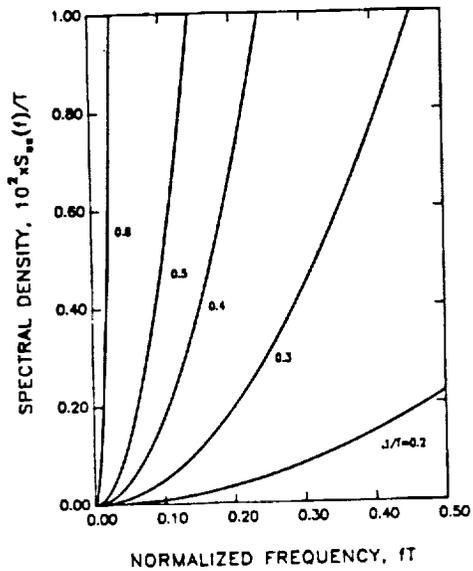
Fig. 5A. Jitter spectral density for 4-PSK with rectangular pulses.
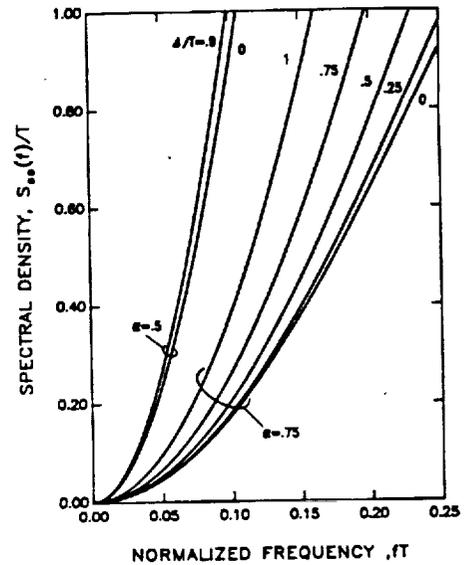
Fig. 5B. Jitter spectral density for 4-PSK with cosine rolloff channel.
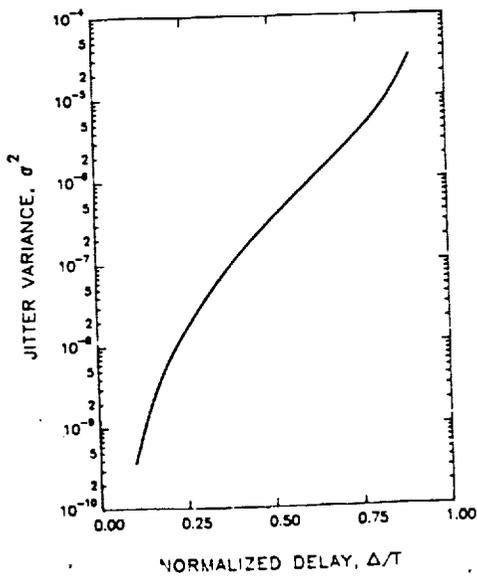
Fig. 5C. Jitter variance versus line delay for 4-PSK with rectangular pulses. Brickwall filter with bandwidth $BT = 10^{-2}$.
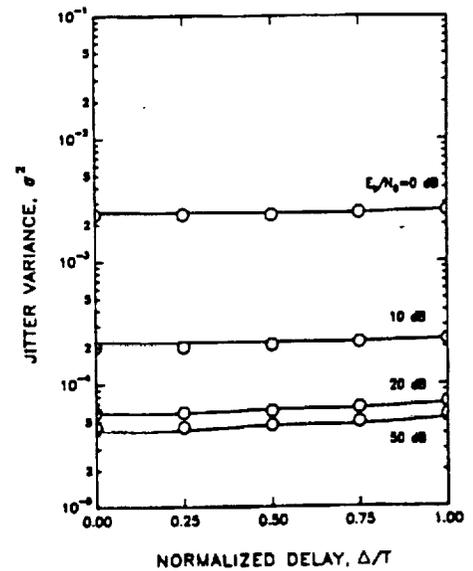

Fig. 5D. Jitter variance for $\alpha = 0.5$ and $Q = 100$. Circles represent simulation results.

FIGURE 5

ZERO-CROSSING DETECTOR

A Zero-Crossing Detector capitalizes on the Zero Crossing transitions of the baseband symbol streams to generate a raw clock component which is narrow bandpass filtered with one of the processes previously described.

Figure 6 shows a representative implementation of this technique. The Demodulated Symbol Stream(s) is (are) pre-filtered with low pass filters which minimize the Zero Crossing Jitter of the symbol transitions. (Note: These filters have the same characteristics, thus the same implementation as those described using the Baseband Non-Linearity Timing Recovery Technique). A hard decision is made whose transition triggers a re-triggerable one shot multi-vibrator. Both zero crossing directions are sensed and both channels can be used with QPSK Modulation. A simple "Or Gate" Function can be configured to select the active one shot output in real time. The "Or Gate" Output Signal will contain unipolar pulses whose width is determined by the one shot delay which are repetitive at the symbol rate. Assuming radomized data, this signal will generate a raw clock component.

This Open Loop Technique also requires both a Pre-Filter and Narrow Bandpass Filter whose characteristics are tailored to the symbol rate. The Non-Linear Processing however is implemented with simple Digital Logic Processing. Figure 7, characterizes the typical time and frequency domain plots of the "Or Gate" output signal. One can see from this data that a fixed pulse width ΔT (i.e., tailored to say half the highest symbol rate width) can support programmable rates.

Comparing this scheme to the work study objectives the following conclusions can be made. From a Programmable Data Rate point of view, this scheme offers no real improvement over the others previously considered. Since the technique uses demodulated data, Serial Processing Carrier and then the clock recoveries is embedded in the acquisition process. As a result, its burst mode applications will be inferior to those techniques which use parallel processing. Although carrier synchronization is required for clock synchronization, this technique adds no additional constraints to the carrier recovery arm filters. This scheme has been used in digital line of sight radio modems in the past. Its viability in satellite communications is uncertain, however, no serious penalties are foreseen at this time.

DATA TRANSITION TRACKING LOOP (DTTL)

The Data Transition Tracking Loop was one of the first Closed Loop Clock Recovery Synchronizers ever used and is probably the most popular type given its performance attributes.

Figure 8 shows a block diagram of this technique (also called Inphase-Midphase Bit Synchronizer). The Inphase Branch determines the polarity of the bit transitions and if they occur, while the Midphase Channel determines the magnitude of the Bit Timing Error. Use of both channels in the multiplier is necessary and provides the correct sign for the Timing Error. The Midphase Error Signal z_k is multiplied by $I_k = \pm 1$ if a transition has been sensed or by $I_k = 0$ if no transition occurs.
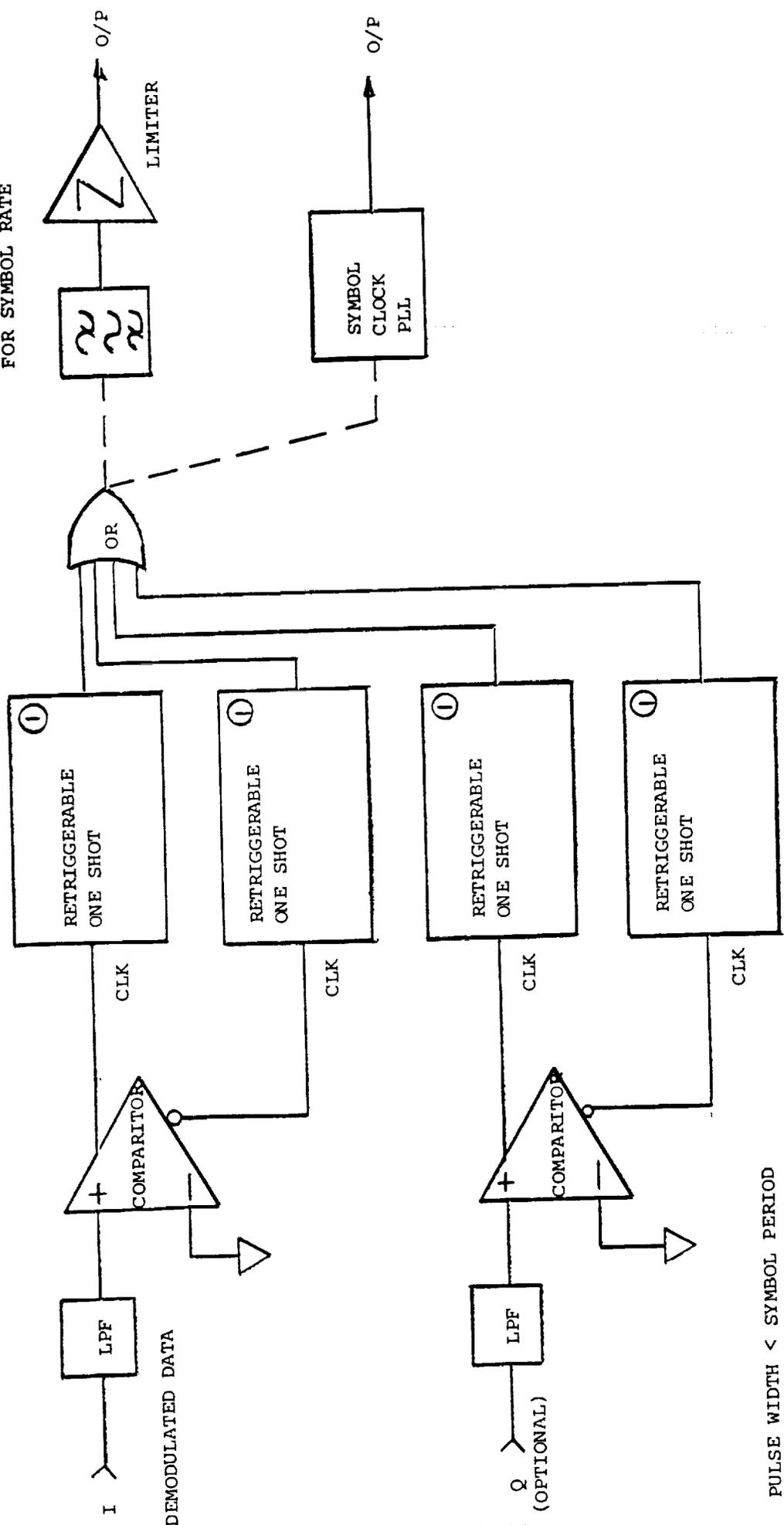
FIGURE 6

ZERO CROSSING DETECTOR
TIMING RECOVERY TECHNIQUE
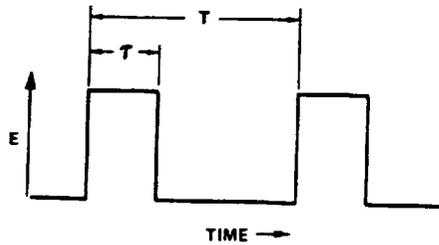
1   PULSE WIDTH < SYMBOL PERIOD

Fig. 7A. Periodic rectangular pulse
train.

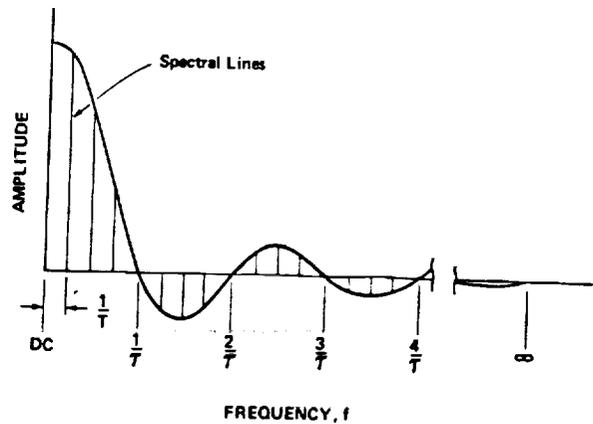The envelope of this plot follows a function of the basic form: $y = \dfrac{\sin x}{x}$

Fig. 7B. Spectrum of a perfectly rectangular pulse. Amplitudes and phases of an infinite
number of harmonics are plotted, resulting in smooth envelope as shown.
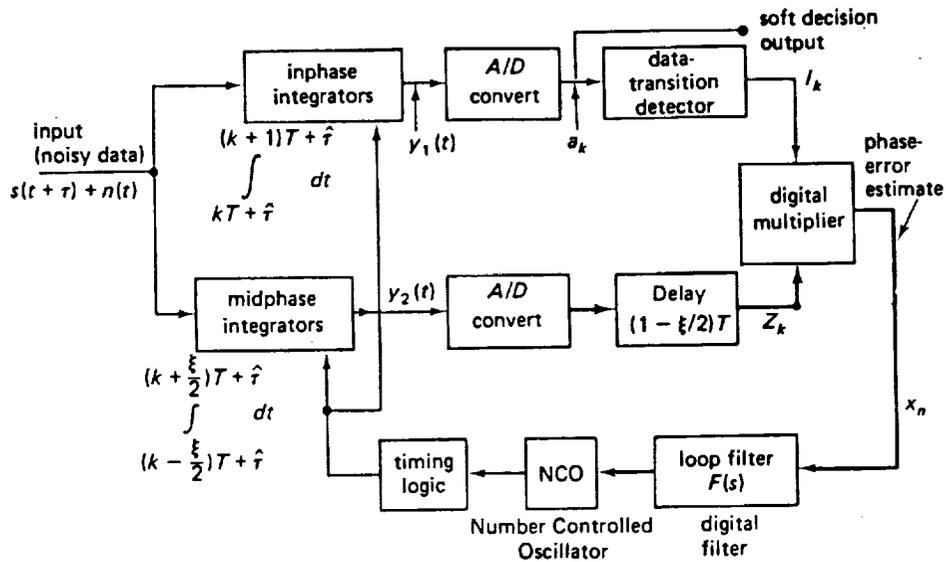
FIGURE 7

C-2

Fig. 8 In-phase/Mid-phase bit synchronizer with inphase and midphase channels. The input clock offset is τ, and the clock phase estimate is $\hat{\tau}$. The midphase integrator window width is ξT sec. The timing error is $\epsilon \triangleq \tau - \hat{\tau}$.

FIGURE 8

Reference (9) has utilized this technique for a coded satellite channel application and indicates that it operates an SNR of -5 dB over a range of data rates from 5.6 Kbs to 250 Kbs. Further more, the system is rate independent since the digital filter gains are automatically proportional to the symbol rate. The only limitations noted were posed by circuit speeds. Figure 9 details the authors practical implementation. Considering the progress made in DSP Technology to date, we believe that the same implementation approach is viable at rates above 10 MBS.

References (9) and (10) show that by adjusting the quadrature channel gain along with the integration interval (Midphase only), a significant improvement in Phase Noise and Clock Cycle Skipping performances can be achieved over that system which integrates in the quadrature channel over the full symbol period.

A suggested implementation methodology for the Programmable Rate Band-limited Modem is to configure the Inphase and Midphase integrators on the actual outputs of the recovered carrier arm filters which are matched to the cosine shaped Input PSK Signal. This approach removes the need and complexity of additional Clock Recovery Pre-Filters and automatically aligns the recovered clock phase to the detection symbol data (i.e., two positive advantages). The only disadvantage of this technique compared to the other schemes thus far discussed is its acquisition performance in burst mode applications suffers because of serial processing of carrier and clock recovery. Acquisition speed improvements can however be made by allowing the Midphase integration window to be wider initially (during the burst preamble) and then narrowed (during the data portion of the burst).
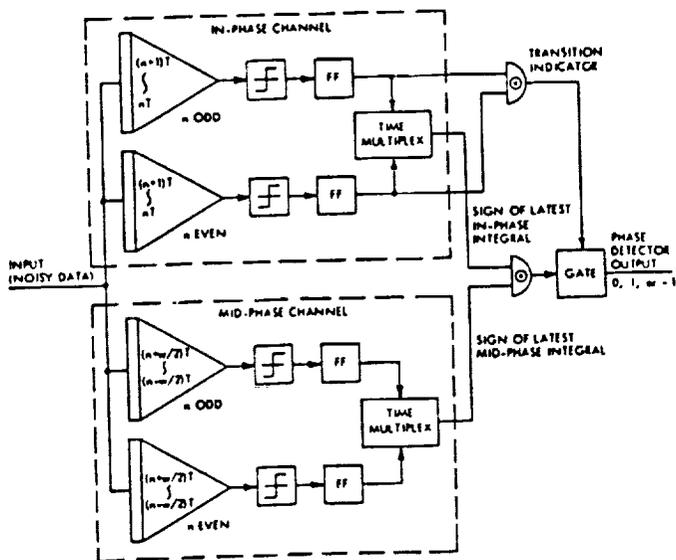
EARLY-LATE GATE SYNCHRONIZER

The absolute value early-late synchronizer shown in Figure 10 also utilizes two integrate and dump circuits. Here each integrates over a pulse interval (T), with one starting $\Delta_o T$ earlier relative to the transition time estimate and the other starting $\Delta_o T$ later. The integrator outputs pass through hard limiters. The limiter outputs are multiplied by their respective inputs to remove the sign of the integrate and dump outputs. The subtraction of the multiplier signals generates the error signal e_k which is basically a measure of the difference in output magnitudes of the two channels. The instantaneous frequency of the VCO (or NCO) is then advanced or retarded in proportion to this difference.

The implementation methodology and complexity of the early-late gate is similar to that of the data transmission tracking loop previously discussed. The advantage of this approach is that it is less sensitive to DC offsets and may be somewhat simpler to implement. It can be shown however, that the early-late gate technique is inferior to the data transition tracking loop in noise tracking performance and acquisition response time.
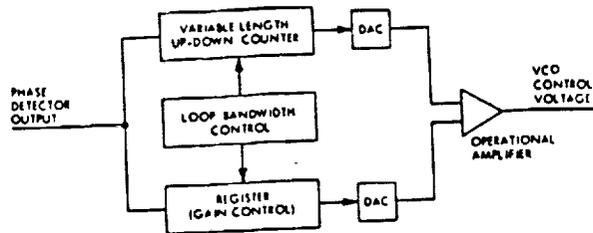
Since this technique offers no real advantages over the data transition tracking loop when considering the requirements of the study objectives no further analysis is considered.
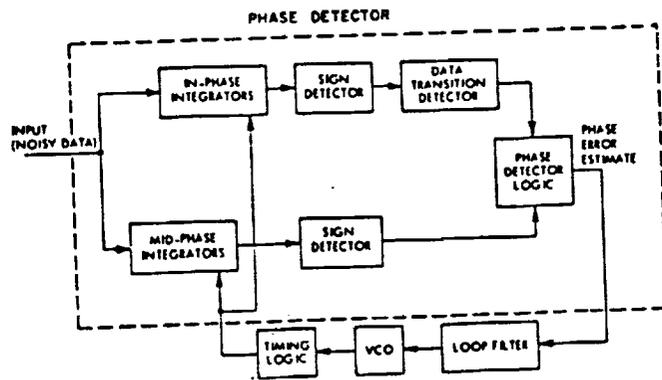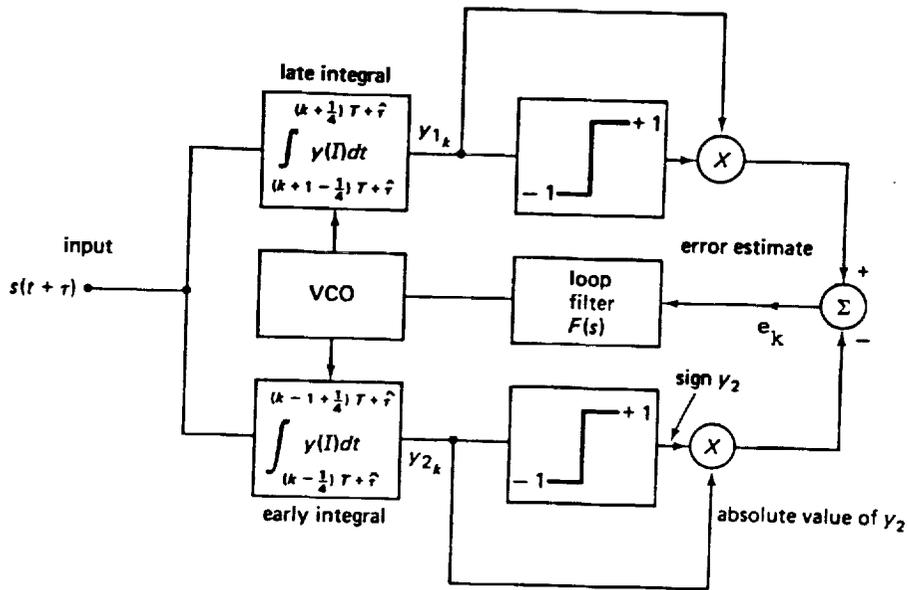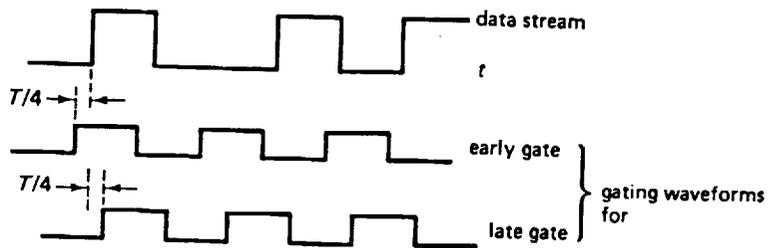
Symbol synchronizer.

Phase detector.

Loop filter.

FIGURE 9

PRACTICAL IMPLEMENTATION OF DIGITAL TRANSITION
TRACKING SYMBOL SYNCHRONIZER
FROM REFERENCE 9

(a)

(b)

Fig. 10. Block diagram and waveforms for an absolute-value early- late-gate bit synchronizer. (a) Block diagram; the $T/4$ overlap used can be shown to be optimum. (b) Waveforms for $\hat{\tau} = \tau$
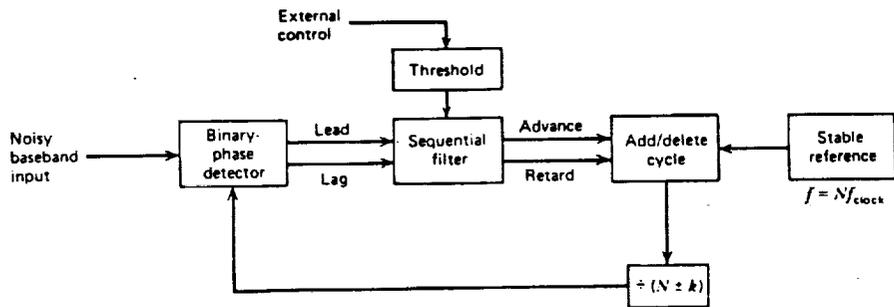
Fig. 11. Binary quantized digital phase locked loop (BQDPL).

Since the digital transition tracking loop is a closed loop system, the effects on performance degradations are only limited to clock jitter and cycle skips and not static phase error. Careful tradeoffs between acquisition parameters and jitter still need to be addressed for a viable implementation using this technique.

Based upon this methodology, one should focus attention on hardware realizations using both digital phase locked loops and digital filtering techniques for bandpass filters at the symbol clock rate prior to making a firm decision for timing recovery.

VIABLE HARDWARE IMPLEMENTATION

We conclude this study topic by presenting some insight into viable alternatives for the narrow bandpass filter symbol clock function for the programmable rate modem under study. Through out this memo we have eluded to various digital signal processing implementations for all functional areas but this one.

° Bandpass Filter Using Digital Filtering Techniques

It can be shown that a bandpass filter can be implemented with a Finite Impulse Response Filter (FIR) using an anti-aliasing filter prior to the analog to digital converter function, similar to the configuration used in a digital low pass filter. With current technology devices, bandpass filter center frequencies up to 25 to 30 MHz should be realizable. Since our symbol clock fall within this range, a viable implementation should be feasible at this time. The advantage to replacing analog L, C type filters with digital filters are many. The greatest benefit realized is that changing the clock rate automatically changes the center frequency which is exactly what we need. Another benefit is that as the center frequency is changed, the "Q" of the filter (i.e., ratio of center frequency to 3 dB bandwidth) remain constant. This allows the clock jitter to remain constant as different rates are programmed, which is highly desirable. Yet another advantage of digital filtering here is that the recovered clock can be readily obtained from the MSB of the output of the FIR filter.

A potential disadvantage of using digital filtering techniques here is that in order to obtain the filter "Q's" required may dictate a digital filter structure with a high number of coefficients. However, a brief examination of this issue indicates that the "Q's" should be realizable if the coefficients and a proper windowing function is selected.

° Phase Locked Loop Bandpass Filter

This circuit function necessitates some form of controllable oscillator which is capable of tuning over two decades of center frequency variation. This oscillator function can be achieved in a variety of different circuit methods. Possible implementation methodologies do include direct digital synthesis, direct frequency synthesis, crystal frequency division and phase-locked loops.

After considering the merits of each of these implementations and weighing them against the design objectives for the digital variable rate modem a design recommendation using Direct Digital Synthesis is proposed. Direct Digital Synthesis (DDS) is also referred to as a Numerically Controlled Oscillator (NCO). Several manufacturers have designed in VLSI nearly complete NCO solutions. Presently these "state of the art" chip sets are capable of synthesizing frequencies up to about 100 MHz. They have frequency resolutions of better than 1 Hz with excellent phase noise and frequency stability characteristics. With these and other positive attributes NCO's are the idea choice.

When the receiver operates in a continuous modes the NCO will have to be adapted to phase-lock onto the incoming data stream. This phase-locking is to prevent loss in bit count integrity. In this mode, the time to phase-lock the loop is not critical and does not effect performance. However, in the burst mode the time to lock this loop may be prohibitively too long. There are methodologies to circumvent this problem. The simplest is to require high transmit clock frequency stabilities and assume that during the time of the burst that the clock is synchronous. Using a NCO in the clock recovery loop may dictate the use of this technique to issue robust acquisition properties.

1. "Hangup in Phase-Locked Loops", by F.M. Gardner, <u>IEEE Transactions on Communications</u>, October, 1977.

2. "Burst - Mode Quaternary PSK Coherent Demodulator for Regenerative Payloads", by A. D'Ambrosio and G. Alletto, <u>AIAA 12th International Communication Satellite System Conference</u>, March, 1988.

3. "Performance of Optimum and Sub-Optimum Synchronizers", by P. Wintz and E. Luecke, <u>IEEE Transactions on Communications</u>, June, 1969.

4. "Carrier and Clock Synchronization for TDMA Digital Communications", by F.M. Gardner, <u>European Space Agency Report ESA-TM-169 (ESTEC)</u>, December, 1976.

5. "Carrier and Clock Recovery for 8 PSK Synchronous Demodulation", by C. Hogge, Jr., <u>IEEE Transactions on Communications</u>, May, 1978.

6. "A New Symbol Timing Recovery Technique for Burst Modem Applications", By K. Feher and G. Takhar, <u>IEEE Transactions on Communications</u>, January, 1978.

7. "Performance Analysis of Delay-Line Clock Regenerator", by A. D'Andrea and U. Mengali, <u>IEEE Transactions on Communications</u>, April, 1986.

8. "A Digital Approach to Symbol Timing Recovery Systems", by T. Le-Ngoc and K. Feher, <u>IEEE Transactions on Communications</u>, December, 1980.

9. "Digital Transition Tracking Symbol Synchronizer for Low SNR Coded Systems", by W. Hurd and T. Anderson, <u>IEEE Transactions on Communications</u>, April, 1970.

10. "Optimization of the Performance of a Digital Data Transition Tracking Loop", by M. Simon, <u>IEEE Transactions on Communications</u>, October, 1970.

11. "Phase Noise and Transient Times for a Binary Quantized Digital Phase Locked Loop in White Guassian Noise", by J. Cessna and D. Levy, <u>IEEE Transactions on Communications</u>, April, 1972.
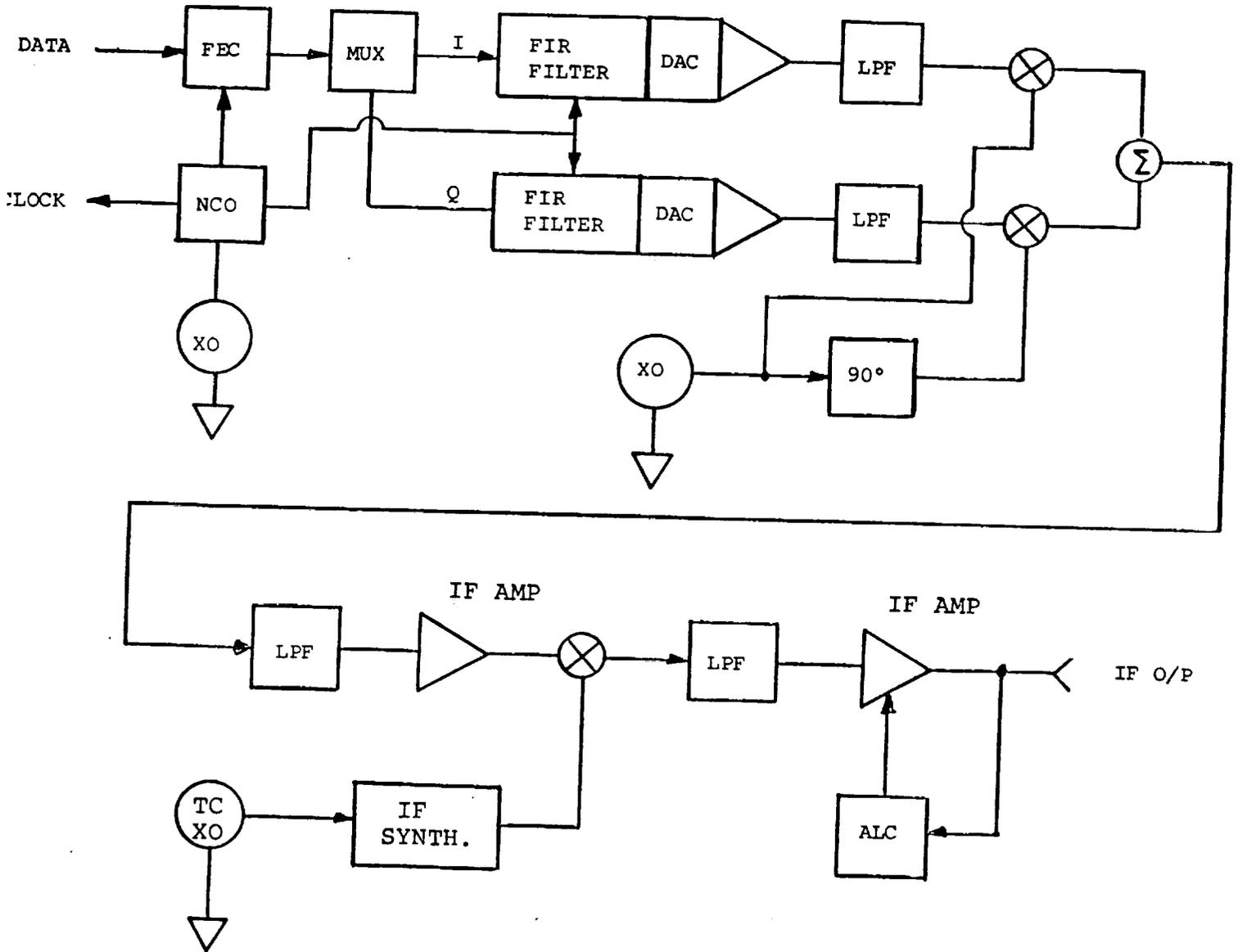
FIGURE 1

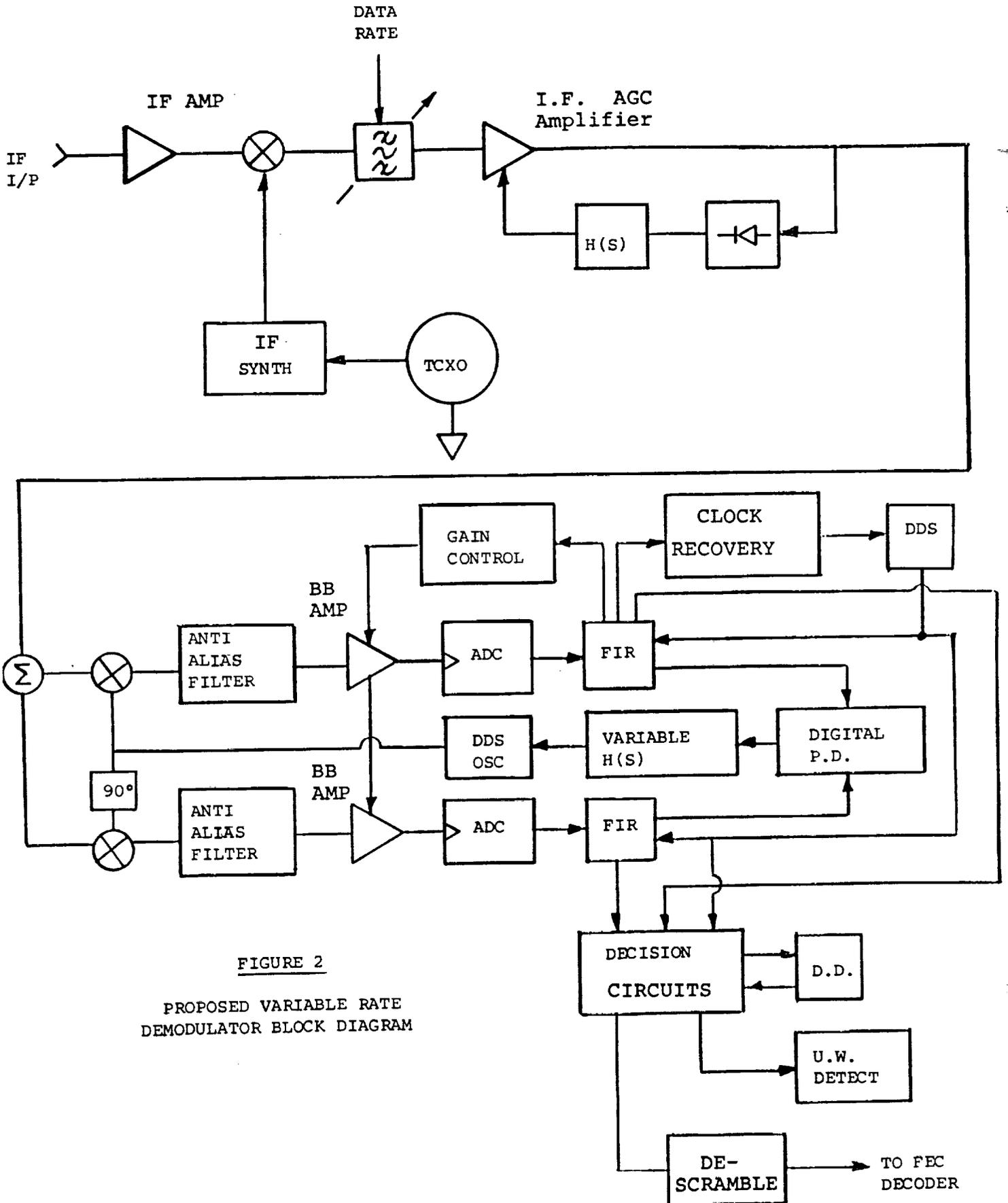PROPOSED VARIABLE RATE MODULATOR BLOCK DIAGRAM

FIGURE 2

PROPOSED VARIABLE RATE
DEMODULATOR BLOCK DIAGRAM

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Report Documentation Page

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16. Abstract

The engineering development study to follow was written to address the need for a Programmable Rate Digital Satellite Modem capable of supporting both burst and continuous transmission modes with either BPSK or QPSK modulation. The preferred implementation technique is an all digital one which utilizes as much digital signal processing (DSP) as possible. The majority of this report consists of outlining design tradeoffs in each portion of the modulator and demodulator subsystem and of identifying viable circuit approaches which are easily repeatable, have low implementation losses and have low production costs. The research involved for this study was divided into nine technical papers, each addressing a significant region of concern in a variable rate modem design. Trivial portions and basic support logic designs surrounding the nine major modem blocks were omitted. In brief, the nine topic areas were: (1) Transmit Data Filtering; (2) Transmit Clock Generation; (3) Carrier Synthesizer; (4) Receive AGC; (5) Receive Data Filtering; (6) RF Oscillator Phase Noise; (7) Receive Carrier Selectivity; (8) Carrier Recovery; and (9) Timing Recovery. It was the intent of each paper to address a specific modem issue and to discuss and to examine techniques which effected the choice of a viable circuit implementation approach. All of these papers achieved this goal and have specific recommendations on realizable circuit designs. A programmable rate digital modem design operating in the burst and the continuous mode has several potential applications in the future of satellite communications. This modem or one similar will be a vital part of the Next Generation VSAT-based DAMA systems. Current and future international networks could benefit from the design concepts here within. The proposed modem would allow networks to utilize new and power advanced satellite features such as those of the ACTS spacecraft.

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