INTEGRATED CIRCUIT RELIABILITY TESTING

Contractor: Jet Propulsion Laboratory

JPL Case No. 17393
NASA Case No. NPO-17393-1-CU

Inventors: Martin G. Buehler and
Hoshyar R. Sayah

October 4, 1988

AWARDS ABSTRACT

The invention enables testing integrated circuits on a wafer, for the reliability of their conductors which extend over regions of different heights.

A test area 14 (Fig. 1) on a wafer includes a long serpentine assay conductor 20 (Fig. 2), formed at the same time as conductors of the integrated circuits on the wafer. The assay conductor 20 extends over regions 24, 26 of different heights, so it includes multiple steps 22 where thinning (e.g., 22' in Fig. 5) and necking (e.g., 22N in Fig. 3) may be present that could reduce reliability. A measurement is taken of the resistance of the assay conductor between its ends 30, 32; a resistance much greater than expected indicates defects. The test area also includes a test conductor 65 that extends along a region of uniform height, and that is formed at the same time as the assay conductor. A measurement of the resistance of the test conductor 65 indicates the resistance per unit length that should be expected from the assay conductor 20. An additional test conductor 63 is provided that extends over a region of a different uniform height, to account for the possibility that there is a different resistance per unit length at different heights.

A major novel feature is forming a test conductor 65 at the same time as a serpentine assay conductor 20 that extends over multiple steps, the test conductor being used to indicate the expected resistance of the serpentine conductor.

Serial No. 279,676
Filing Date 12/5/88
Contract No. NAS7-918
Contractor Caltech/JPL
Pasadena (City) CA. (State) 91109 (Zip)

FIG. 2

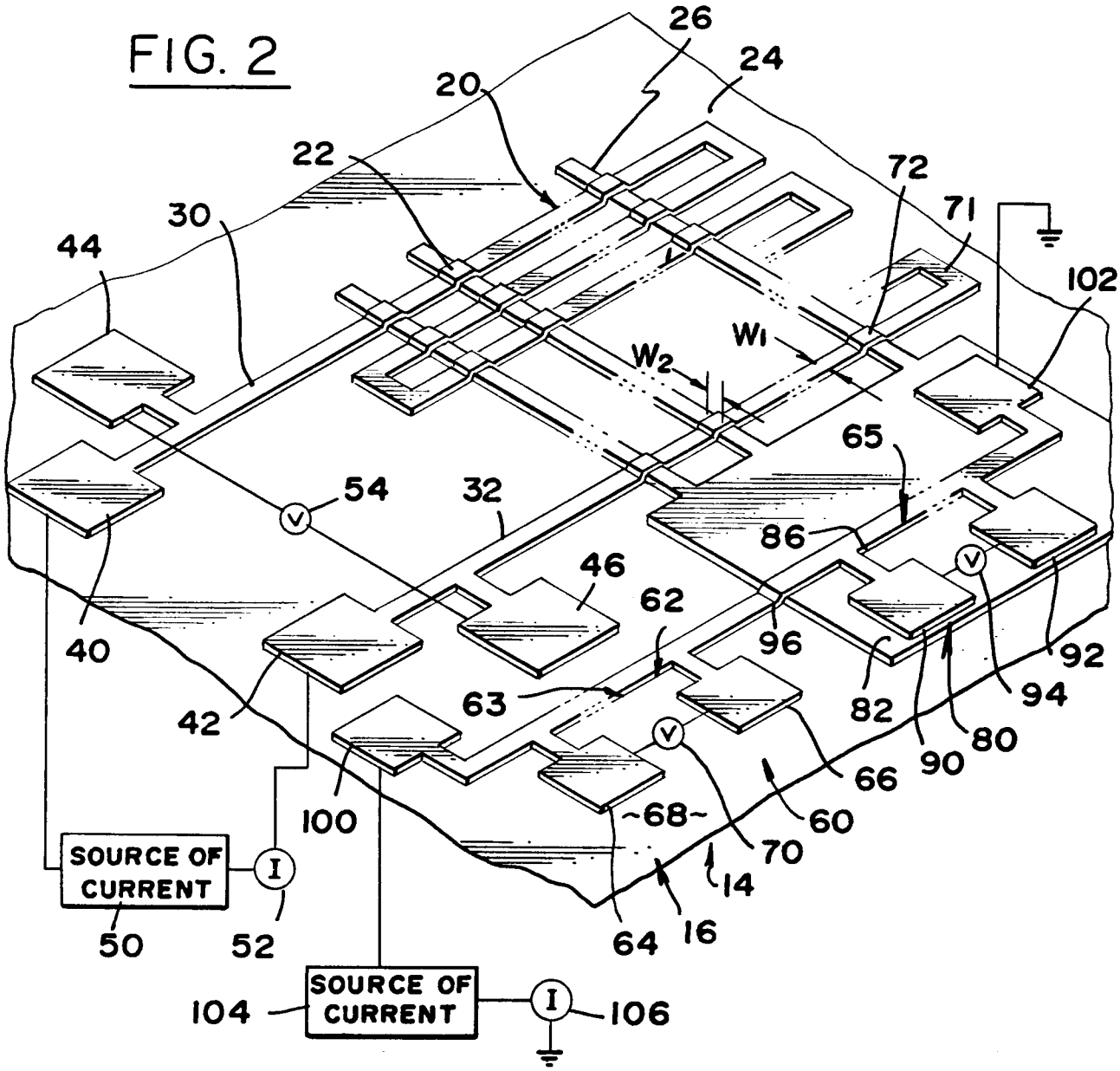


FIG. 4

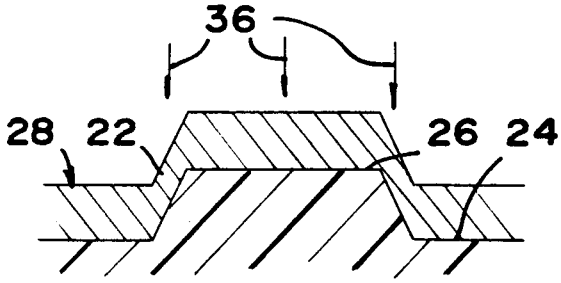
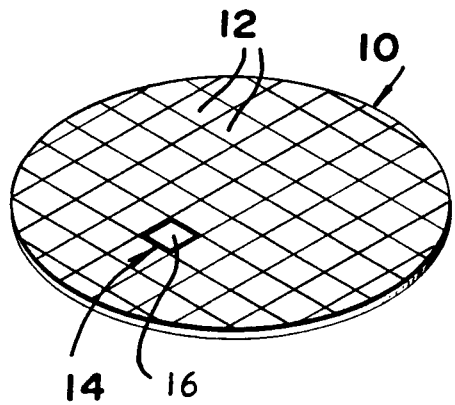


FIG. 1



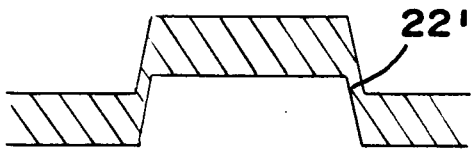
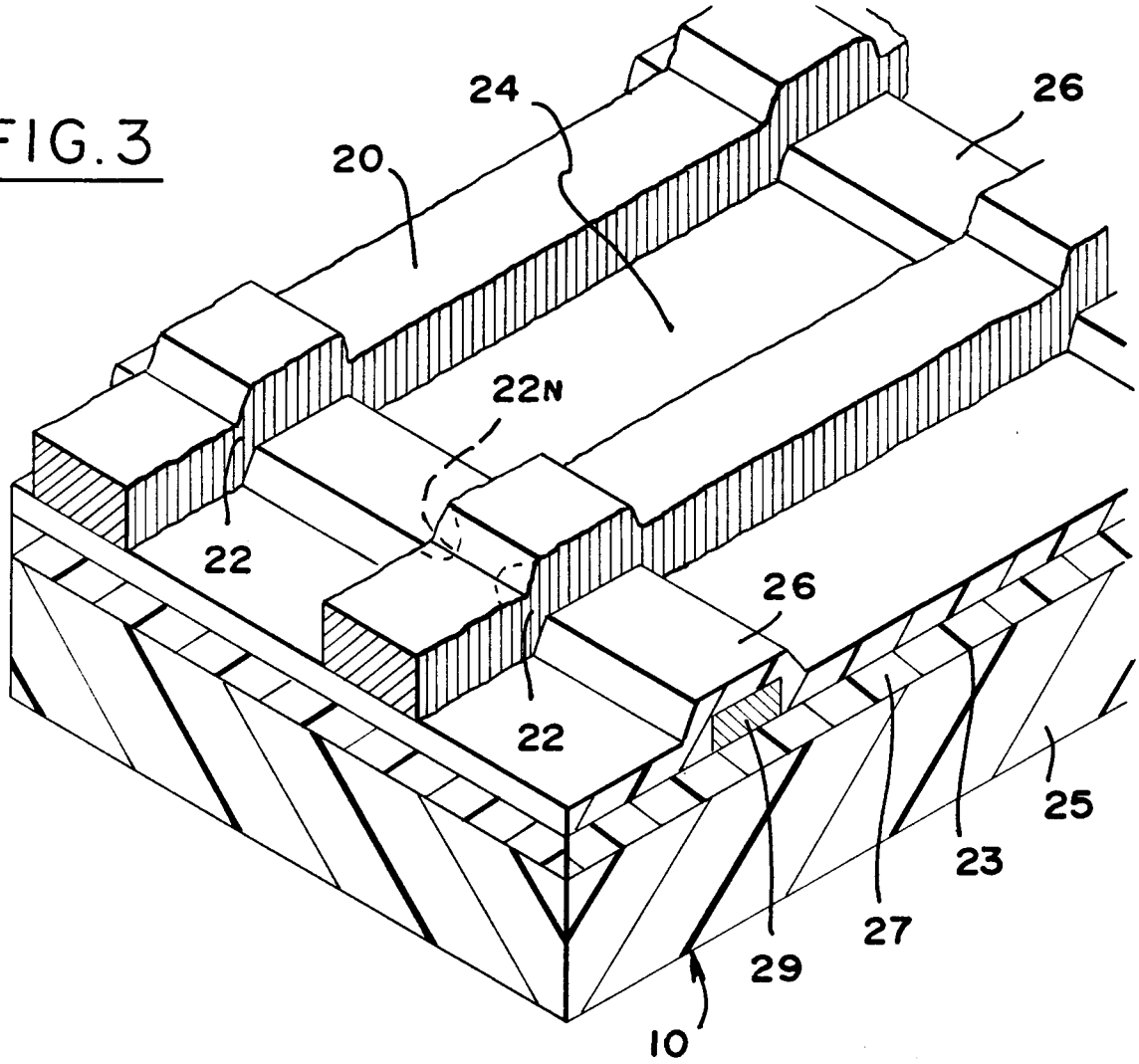


FIG. 5

FIG.3


24
26
20
22N
22
26
22
25
23
27
29
10

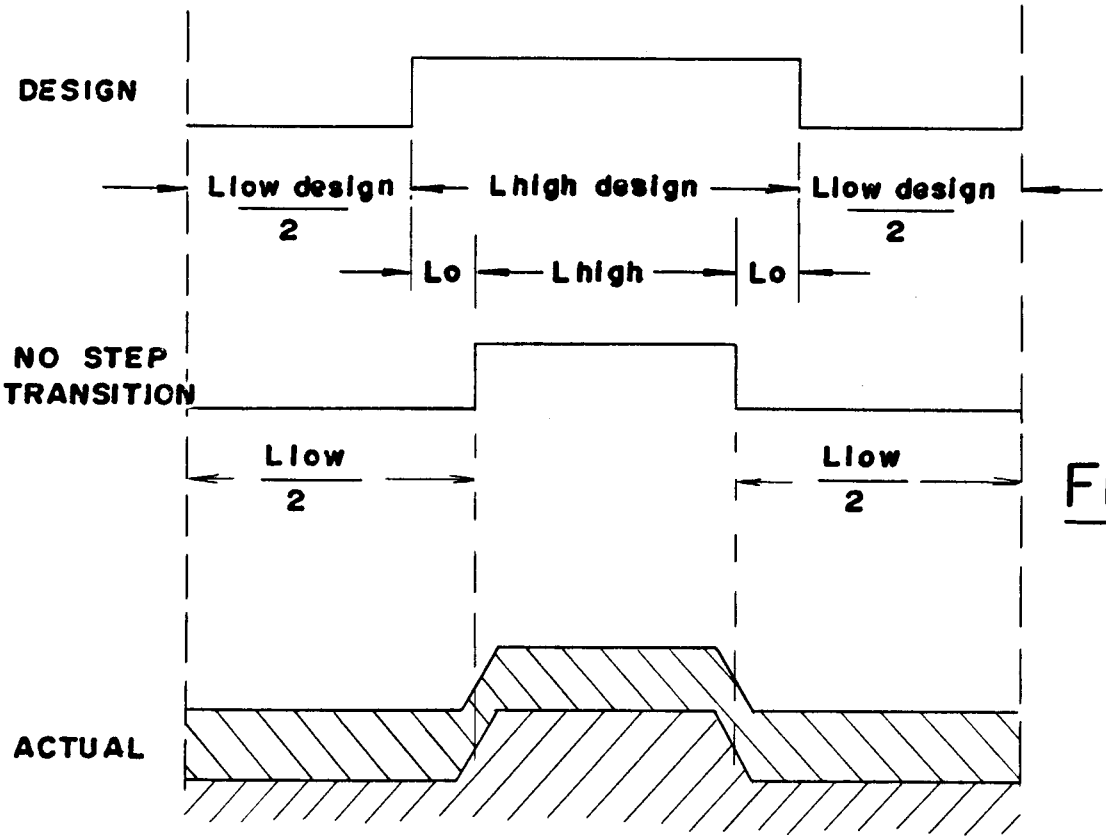

DESIGN
Llow design / 2
Lhigh design
Llow design / 2
Lo
Lhigh
Lo
NO STEP TRANSITION
Llow / 2
Llow / 2
ACTUAL

FIG.6

JPL Case No. 17393
NASA Case No. NPO-17393-1-CU
Docket No. 87/396

INTEGRATED CIRCUIT RELIABILITY TESTING

Origin of the Invention

The invention described herein was made in the performance of work under a NASA contract, and is subject to the provisions of Public Law 96-517 (35 USC 202) in which the Contractor has elected not to retain title.

Technical Field

This invention relates to techniques for testing the reliability of integrated circuits.

Background Art

The reliability of microscopic conductors deposited on integrated circuits formed on a wafer, can be evaluated by forming a long serpentine resistance structure or assay conductor on the same wafer and measuring the resistance between the ends of the serpentine assay conductor. The resistance between the ends of the serpentine conductor determines the "measured length" of the serpentine conductor. This measured length is then compared to the design length of the serpentine conductor which is known from the design layout of the serpentine conductor, to determine discrepancies that may indicate defects in the serpentine conductor. A similar method is to compare the resistance between the ends of the serpentine conductor and the level of resistance that would be expected in the absence of defects, of an ideal serpentine conductor. Both methods are equivalent and can be used interchangeably.

In some integrated circuits, the microscopic conductors of the circuit pass along steps connecting regions of different heights. There is a considerable possibility of defects in a conductor along the steps

where the conductor extends between the regions of different heights. Also, the conductor may have different widths at the different heights, due to masks through which light is passed to define the conductors, being out of focus. A higher than expected resistance for a serpentine assay conductor extending along the multiple steps, could be due to the conductor having a smaller than expected width, which does not indicate unreliability. A testing method and apparatus which enabled assessment of the causes of a discrepancy between the ideal and the measured resistance of the serpentine assay conductor, would be of considerable value.

Statement of the Invention

In accordance with one embodiment of the present invention, a method and apparatus are provided for indicating the reliability of microscopic conductors on integrated circuits that pass across regions of different heights. The apparatus includes an elongated assay conductor on the integrated circuit device, which extends along multiple steps between regions of first and second heights. The apparatus also includes a test structure with an elongated test conductor on the integrated circuit device, which extends along a region of uniform height. A measurement is taken of the resistance of the assay conductor. A measurement is also taken of the resistance of the test conductor, which indicates the resistance per unit length that should be expected from the assay conductor. The test conductor is formed at the same time as the assay conductor, so they have the same width and thickness. The test structure may include two test conductors, each extending along a region of

different uniform height (so there are no steps along a test conductor), to account for possible differences in resistance per unit length of the regions of different heights.

The novel features of the invention are set forth with particularity in the appended claims. The invention will be best understood from the following description when read in conjunction with the accompanying drawings.

Brief Description of the Drawings

Fig. 1 is a perspective view of an integrated circuit device with which the present invention is useful.

Fig. 2 is a perspective view of the test area of the device of Fig. 1.

Fig. 3 is an enlarged perspective and sectional view of a portion of the test area of Fig. 2.

Fig. 4 is a sectional view of a portion of the circuit of Fig. 3.

Fig. 5 is a view of circuit similar to that of Fig. 4, but showing a higher degree of thinning.

Fig. 6 is a view similar to that of Fig. 4, for a theoretical assay conductor which has a single high region and a single low region, and showing the difference between design and actual assay conductor lengths.

Detailed Description of the Invention

Fig. 1 illustrates an integrated circuit device 10 which includes a silicon wafer on which numerous integrated circuits 12 have been formed. The device also includes a test area 14 where a test apparatus is formed that is useful in testing the reliability of portions of the integrated circuits. Fig. 2 illustrates the test area 14, showing a test apparatus 16 that is

useful in testing the reliability of microscopic conductors that must pass over steps extending between areas of different height. The apparatus includes an assay conductor 20 that extends over multiple steps 22 between regions such as 24 and 26 of different heights. The assay conductor 20 extends in a serpentine configuration, to provide a long length of conductor in a limited area. In one example, the width W_1 of the conductor along most of its length is about 5 microns, and the assay conductor has a total length between its opposite end portions 30, 32 of 10cm. Similar conductors extending over surface areas of different height occur in the circuits of the integrated circuit device. As shown in Fig. 3, the regions 26 of greater height, relative to the surfaces 23 of an insulative base 25 and of an insulative layer 27 thereon, lie over embedded cross-conductors 29.

As indicated in Fig. 4, an actual integrated circuit conductor 28, like the assay conductor 20, is formed by depositing it on the uneven surface 34 of the integrated circuit device, arrows 36 indicating the direction of material motion during its deposition. After deposition, typical prior art methods are used, such as depositing a photoresist, exposing the photoresist through a mask washing away only the exposed or unexposed areas, and etching away the areas unprotected by photoresist. Thinning can occur at the steps 22. Fig. 5 illustrates a situation where the transition between the different heights is steep and thinning is more pronounced at steps 22'. In addition, "necking" can occur, where the width of the conductor along the step is narrow as indicated at 22 N in Fig. 3. The reduced cross sectional area along the steps introduces higher conductor resistance and is a major source of defects in such integrated circuits.

Another mechanism that introduces higher assay

conductor resistance compared to the ideal conductor is that the assay conductor length increases due to undulations of the assay conductor in going over steps. However, this length increase is considered negligible compared to the total length of the assay conductor.

By measuring the resistance along the long serpentine assay conductor 20 (Fig. 2), the "measured length" of the serpentine assay conductor is calculated. Such calculation can be made by knowledge as to how the serpentine assay conductor was formed and the resistance per unit length of the assay conductor over the regions of first and second heights. The resistance per unit length of the assay conductor over the regions of first and second heights are derived from the test conductor resistance measurements. The measured length of the assay conductor includes the effects of the steps and the step transitions, and of necking and thinning, each of which introduce higher assay conductor resistance measurements when present. The design length of the assay conductor is derived from the design layout of the assay conductor (which assumes no defects). By comparing the assay conductor "measured length" to its design length, it is possible to obtain an indication of the reliability of an assay conductor extending over steps. In one example, if the measured length of the assay conductor exceeds 150% of the design length of the assay conductor, then this indicates excessive resistance along the steps. The percentage by which the measured length exceeds the design length, at which the integrated circuit device will be discarded, depends on the required reliability of the integrated circuit.

Equations 1 through 4 written below, show how one calculates the measured serpentine length (for an assay conductor), the measured serpentine resistance, the difference between actual and design serpentine

lengths for low or high regions, and the design serpentine length.

$$Lserp.meas = \frac{(Rserp.meas * Lserp.design)}{(R'low * Llow.design + R'high * Lhigh.design)} \quad \text{Eq. 1}$$

$$Rserp.meas = R'low * Llow.design + R'high * Lhigh.design + 2Lo(R'low - R'high) + 2Rstep \quad \text{Eq. 2}$$

$$2Lo = Lhigh.design - Lhigh = Llow - Llow.design \quad \text{Eq. 3}$$

$$Lserp.design = Llow.design + Lhigh.design = Llow + Lhigh \quad \text{Eq. 4}$$

Lserp.meas	= measured serpentine length
Lserp.design	= design serpentine length
Rserp.meas	= measured serpentine resistance
R'low	= resistance per unit length over the low region
R'high	= resistance per unit length over the high region
Rstep	= step resistance due to necking, thinning and undulation
Llow.design	= design serpentine length over the low region
Lhigh.design	= design serpentine length over the high region
Llow	= actual serpentine length over the low region
Lhigh	= actual serpentine length over the high region
2Lo	= difference between actual and design serpentine length over low or high regions

Fig. 6 shows the quantities above for a theoretical conductor having a single high region and a single low region.

As shown in Fig. 2, the assay conductor 20 is formed with assay conductor pads at its opposite end portions 30, 32. These pads include a current pad 40, 42, and a voltage pad 44, 46 at each end portion of the

assay conductor. A source of current 50 is connected through a current meter 52 between the two current pads 40, 42 to pass a measured current along the length of the assay conductor. A voltmeter 54 is connected between the opposite voltage pads 44, 46 to measure the voltage between the end portions of the assay conductor. Of course, the measurements of voltage and current enable a determination of the resistance along the length of the assay conductor.

Where a relatively small percentage change in measured length, such as from 140% to 160% of designed length, is enough to change from an acceptable to an unacceptable level, it is important to determine the measured length of the assay conductor with accuracy. The factors that affect accuracy of determination of the measured length, are the actual width, the actual thickness, and the proportions of raised and lowered areas of the assay conductor.

The assay conductor and the conductors of the integrated circuits are formed by techniques that require a mask to define the placement and width of the conductors. If the mask is not formed or positioned precisely, the width of the conductors will vary from the intended width. Thus, the width W_1 along the low region may turn out to be 4 microns or 6 microns instead of the intended 5 microns.

Applicant determines the resistance per unit length of the assay conductor over the first and second height regions by forming two test structures 60, 80 (Fig. 2) which includes a test structure conductor 62 with two portions 63, 65. The test structures 60, 80 are formed at the same time as the assay conductor 20, using the same equipment and setup, and with the equipment designed to make the test conductor and assay conductor of the same width, when over a region of the same height. The test conductor portion 63 is formed on

an area 68 of uniform height which is the same as region 24. The test conductor portion 65 is formed on an area 82 of uniform height which is the same as region 26. The test structure 60 includes a pair of voltage pads 64, 66, and the test structure 80 includes a pair of voltage pads 90, 92. A measured current is passed along the length of the test conductor 62 and the voltage drop along its length is measured as by a voltmeter 70, 94 connected between the voltage pads. The precise distance between the locations where the voltage pads contact the test conductor 62 is known, and the voltage and current measurements enable a determination of the resistance per unit length of the test conductor over the regions of raised and lowered heights.

The assay conductor includes multiple lower portions such as 71 of a lower height and multiple raised portions 72 of an elevated height, as well as multiple step regions connecting them. It is possible for the widths W_1 and W_2 of the lower and raised portions 71, 72 to differ. This may be due to a mask being in focus at one level but out of focus at another level.

As seen in equation 1, the assay conductor measured length Lserp.meas depends on the proportion of the assay conductor over the lower and raised areas. Due to processing events, for example over/under-etching of layers, the actual proportion of the assay conductor over the lower and raised areas in not easily known. Fig. 6 shows how the design and actual steps can differ. Applicant uses the design proportions of the assay conductor as a good estimate of the actual proportions of the assay conductor when determining the measured length of the assay conductor. Where the resistance per unit length of the assay conductor over the raised and lowered regions differ

and the design proportions of the assay conductor do not provide a good estimate of the actual proportion of the assay conductor over the regions of different heights, the measured length of the assay conductor can be shorter or longer than the design length (assuming no thinning and necking at the steps). An optical measurement technique, such as SEM, may be used to determine the proportions of the assay conductor lying over the raised and lowered areas to eliminate the assay conductor length increase/decrease due to over/under-etching of layers during the fabrication process. Where the step transition is gradual and thinning and necking do not occur, so that Rstep = 0, the difference between the actual and design serpentine assay conductor length over low or high regions, $2L_o$, is determined from equation 2.

Thus, the invention provides a method and apparatus for indicating the reliability of circuit conductors which have been formed on an uneven surface of an integrated circuit device. An elongated assay conductor extends along multiple steps between regions of first and second different heights on the integrated circuit device and instruments are used to measure the resistance between the opposite ends of the assay conductor. A test structure is also provided, which includes an elongated test conductor which extends along a region of substantially constant height on the integrated circuit. The equipment is also used to measure the resistance of the test conductor, to thereby determine the resistance per unit length of the assay conductor. The apparatus preferably includes two test structures, each with a test conductor at a different one of the two heights along which the assay conductor extends, to take account of the fact that the resistance per unit length can vary with the height of the surface on which a conductor is formed. The test

conductors of the two test structures can be connected in series, with each having a current pad, so current can flow through the two test conductors in series, to simplify testing and reduce the size of the test structure.

Although particular embodiments of the invention have been described and illustrated herein, it is recognized that modifications and variations may readily occur to those skilled in the art and consequently it is intended to cover such modifications and equivalents.

INTEGRATED CIRCUIT RELIABILITY TESTING

ABSTRACT OF THE DISCLOSURE

A technique is described for use in determining the reliability of microscopic conductors deposited on an uneven surface of an integrated circuit device. A wafer containing integrated circuit chips is formed with a test area having regions of different heights. At the time the conductors are formed on the chip areas of the wafer, an elongated serpentine assay conductor is deposited on the test area so the assay conductor extends over multiple steps between regions of different heights. Also, a first test conductor is deposited in the test area upon a uniform region of first height, and a second test conductor is deposited in the test area upon a uniform region of second height. The occurrence of high resistances at the steps between regions of different height is indicated by deriving the "measured length" of the serpentine conductor using the resistance measured between the ends of the serpentine conductor, and comparing that to the design length of the serpentine conductor. The percentage by which the measured length exceeds the design length, at which the integrated circuit will be discarded, depends on the required reliability of the integrated circuit.

FIG. 2

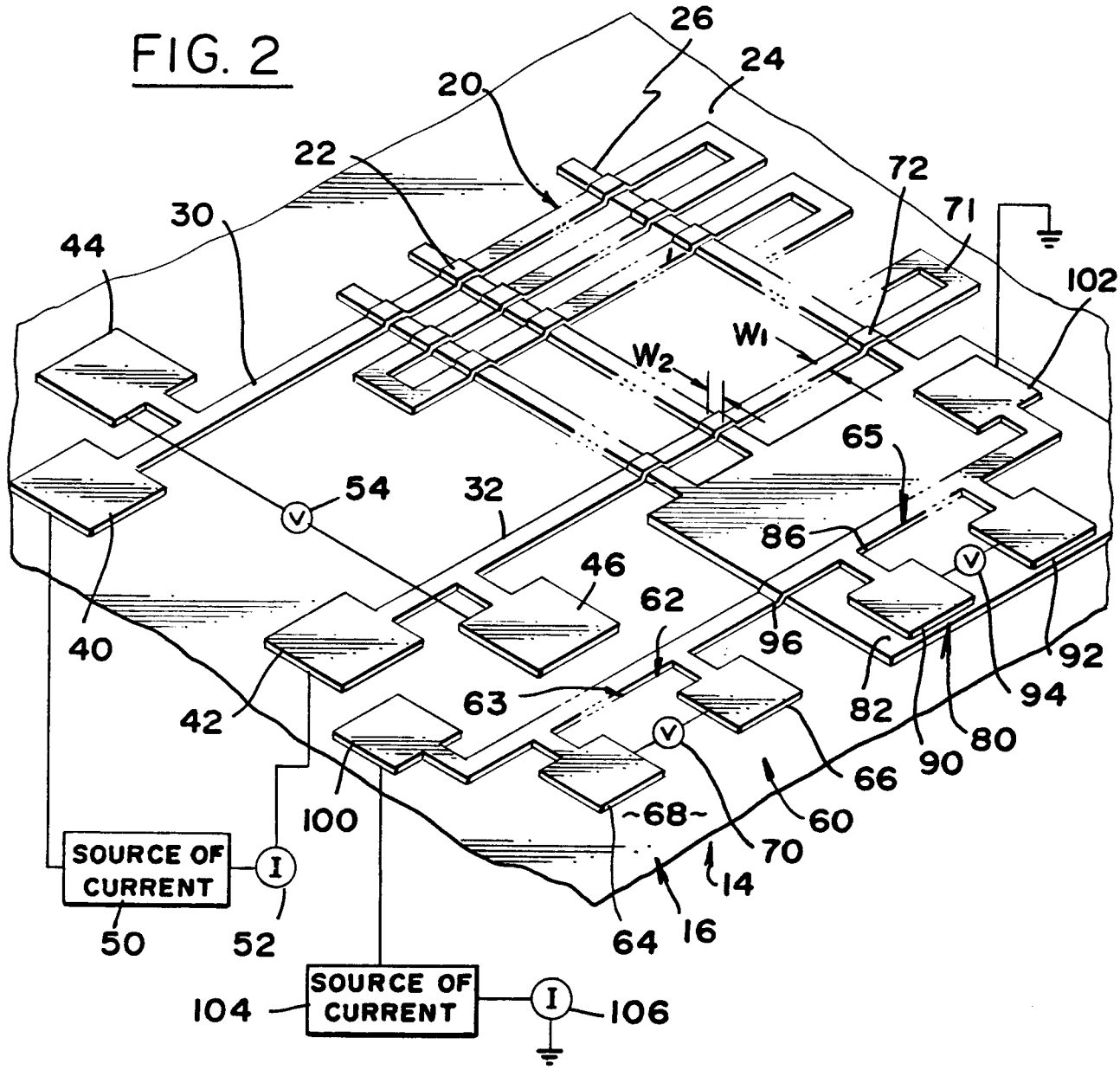


FIG. 4

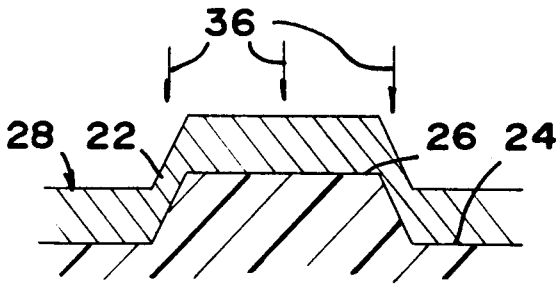
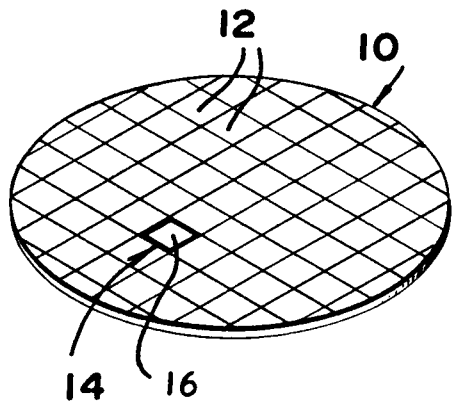


FIG. 1



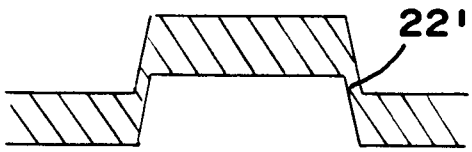


FIG. 5

NASA CASE NO. NPO-17393-1CU

PRINT FIG. 2

NOTICE

The invention disclosed in this document resulted from 14 Page research in aeronautical and space activities performed under programs of the National Aeronautics and Space Administration. The invention is owned by NASA and is, therefore, available for licensing in accordance with the NASA Patent Licensing Regulation (14 Code of Federal Regulations 1245.2).

To encourage commercial utilization of NASA-owned inventions, it is NASA policy to grant licenses to commercial concerns. Although NASA encourages nonexclusive licensing to promote competition and achieve the widest possible utilization, NASA will consider the granting of a limited exclusive license, pursuant to the NASA Patent Licensing Regulations, when such a license will provide the necessary incentive to the licensee to achieve early practical application of the invention.

Address inquiries and all applications for license for this invention to NASA Resident Office-JPL, NASA Patent Counsel, Mail Code 180-801, 4800 Oak Grove Dr., Pasadena, CA 91103. Approved NASA forms for application for nonexclusive or exclusive license are available from the above address.

PAT. APP.
IN-22
21592-B

NRO-JPL