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on

MATERIAL GROWTH AND CHARACTERIZATION FOR  
SOLID STATE DEVICES

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## ABSTRACT

### FINAL REPORT

on

### MATERIAL GROWTH AND CHARACTERIZATION FOR SOLID STATE DEVICES

NSG-1390

During the period of this research grant, the process of liquid phase electroepitaxy (LPEE) was used to grow ternary and quaternary alloy III-V semiconductor thin films. Selective area growth of InGaAs was performed on InP substrates using a patterned sputtered quartz or spin-on glass layer. The etch back and growth characteristics with respect to substrate orientation were investigated. The etch back behavior is somewhat different from wet chemical etching with respect to the sidewall profiles which are observed.

LPEE was also employed to grow epitaxial layers of InGaAsP alloys on InP substrates. The behavior of Mn as an acceptor dopant was investigated with low temperature Hall coefficient and photoluminescence measurements.

A metal-organic vapor phase epitaxy system was partially complete within the grant period. This atmospheric pressure system will be used to deposit III-V compound and alloy semiconductor layers in future research efforts.

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## I. INTRODUCTION

This is a final technical report describing the research activities of NASA Grant NSG 1390. The three-year program began December 1, 1983 and was extended on a no-cost basis to May 31, 1988. The proposed program involved the efforts of four faculty members and four MSEE graduate students. One of the investigators (E. K. Stefanakos) left the University in August 1985. The third year funding was reduced from \$175,000 to \$150,000 due ostensibly to funding cutbacks within NASA.

The proposed research program involved the deposition of thin semiconductor layers by the process of liquid phase electroepitaxy (LPEE), the characterization of these layers, and fabrication of electronic devices. The proposed tasks were:

TASK I: Multilayer growths by LPEE, with an investigation of dopants and selective area growth procedures. Also, hybrid multilayer growths were to be performed with a metalorganic vapor phase epitaxy (MOVPE) system which was being developed.

TASK II: Electronic device fabrication. A metal-insulator-semiconductor field effect transistor (MISFET) was to be fabricated if a feasible gate insulator deposition process could be developed.

TASK III: Fabrication of a p-i-n diode structure for photosensor applications. This structure would utilize a selected area mesa growth and a diffused junction.

The above tasks were modified throughout the grant period to reflect changes in process development, funding and personnel expertise. The next section reviews the various technical accomplishments.

## II. TECHNICAL DISCUSSION

The various research efforts during the grant period are reviewed here, with emphasis upon the more recent results. Previous results were presented in the preceding Annual Technical Reports.

### A. Selective Area Etch Back and Growth

It was desired to investigate the growth of InGaAs in localized regions of an InP substrate as a means of creating device mesa structures or isolated dopant regions. The masking material must withstand the growth temperature cycling and be a suitable, noncontaminating electrical insulator. Both ion beam sputtered quartz and a commercial spin-on silicon dioxide were utilized. The research efforts described here include the selective area etch back of InP substrates and selective area growth of InGaAs layers lattice-matched to (100) oriented InP substrates by the current controlled liquid phase epitaxial technique (also known as electroepitaxy).

#### 1. Selective Area Etch Back

The interest in selective area etch back of the substrate lies with the inherent capability of establishing isolated channels and/or trenches which can be refilled with another lattice-matched semiconductor compound. These isolated semiconductor regions can then be used as optical waveguides (long, narrow channels), or for device mesa structures (trenches).

To study the etch back properties in (100) oriented Fe-doped InP substrates, the substrates were pattern masked with ion beam sputtered quartz ( $\text{SiO}_2$ ). The InP islands defined by the  $\text{SiO}_2$  mask were of various sizes (80x1000  $\mu\text{m}$  to 3000x3000  $\mu\text{m}$ ) and different geometries (narrow and

wide strips, square, circular). The mask pattern used in this study is shown in Fig. 1.

To perform the etch back, the patterned substrate was first cleaned with organic solvents before it was loaded into the etch back/growth boat. The etch back was performed at a constant furnace temperature of 640 °C by passing a direct electric current from the substrate to the melt (In-InP melt). For growth the current is passed in the opposite direction. Current densities used were from 5 to 15 A/cm<sup>2</sup> for periods from 15 to 60 minutes.

Electroepitaxial etching profiles are examined by cleaving the (100) InP substrate in orthogonal directions along the (011) and (011) planes. Figure 2 is a composite photomicrograph of a cleaved section along the (011) plane. The figure shows six narrow channels 45-160 μm wide and one wide channel 840 μm wide. The narrow channels etched very uniformly which resulted in a flat bottom (about 17 μm deep) while the wide channel etched nonuniformly. This etch nonuniformity is typical in channels wider than 200 μm. The etch-revealed walls in all channels are (111)B and (111)B planes. Sections cleaved along the (011) plane show that the etch-revealed walls are (111)A and (111)A planes. Consequently, a trapezoid-shaped profile is obtained in either cleavage direction. In addition, the lateral etch-rate in the [011] directions is about the same, i.e., the etch proceeds up to the (111)B, (111)B, (111)A, and (111)A planes at about the same rate. This implies that electroepitaxial etching, unlike chemical etching, is not influenced by the difference in chemical activity between the {111}A and the {111}B planes. The difference in chemical activity between these planes

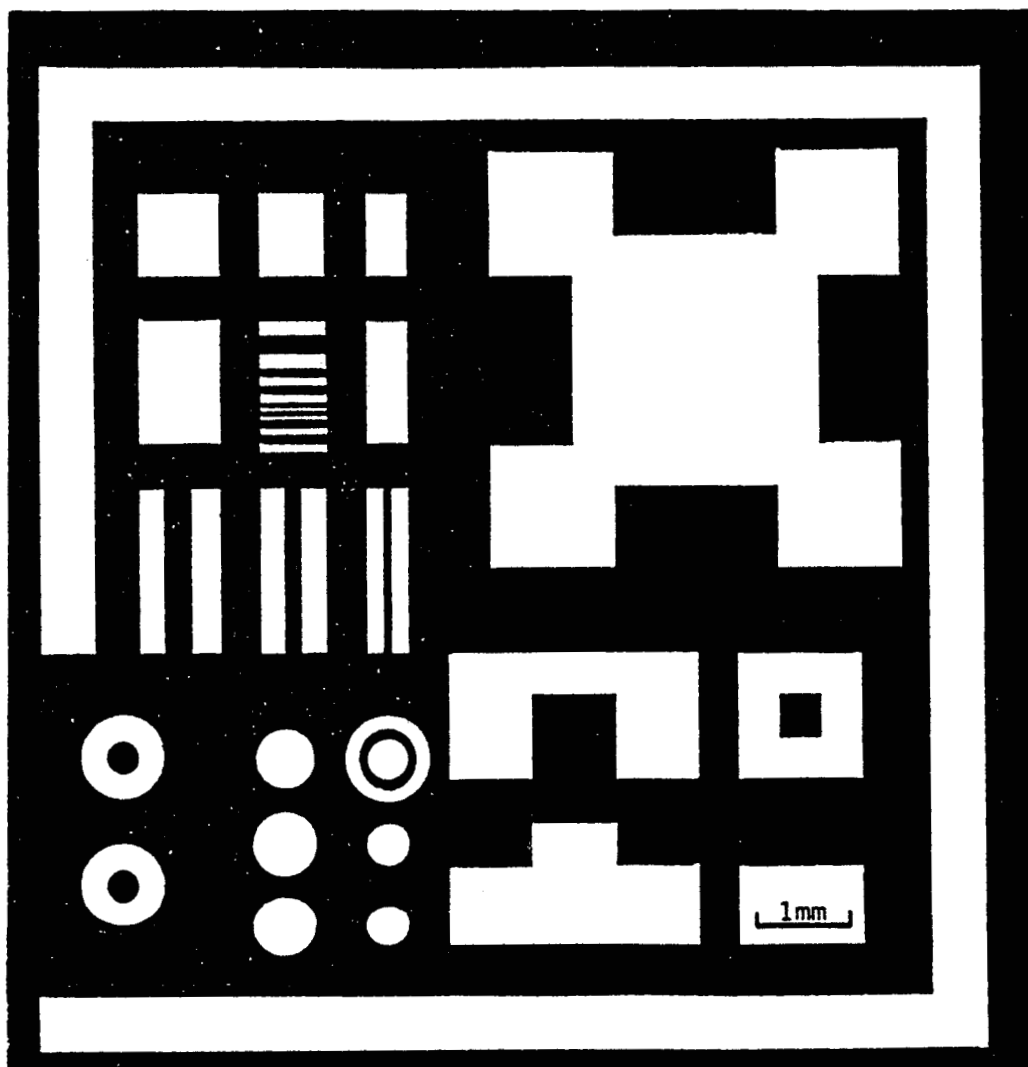


Fig. 1. Schematic diagram of mask pattern.  
The dark areas are the  $\text{SiO}_2$  masking layer.

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Fig. 2. A composite Nomarski phase contrast photomicrograph of a cleaved section. The narrow channels are from 45 to 160  $\mu\text{m}$  wide. The wide channel is about 840  $\mu\text{m}$  wide. The channels were etched at 640  $^{\circ}\text{C}$  using 5  $\text{A}/\text{cm}^2$  for 60 min.



results in different etch profiles in chemically etched InP. A trapezoid-shaped profile is obtained in one direction and a dovetail-shaped profile in a perpendicular direction.

Figure 3 is a SEM photomicrograph of an etched channel which shows the masking oxide ( $\text{SiO}_2$ ), the sharp definition of the side walls, and the flat bottom (100) plane. The side walls are identified as  $(111)B$  and  $(111)A$  planes.

The etch by electroepitaxy is preferential. Narrow channels <200  $\mu\text{m}$  wide and small trenches <200 x 200  $\mu\text{m}$  oriented parallel or perpendicular to the [011] direction etched uniformly in the [100] direction revealing the (100) plane. At the same time, side etching proceeded up to the  $\{111\}A$  and  $\{111\}B$  planes, i.e., the  $(111)A$ ,  $(111)A$ ,  $(111)B$ , and  $(111)B$  planes. Consequently, a trapezoid-shaped profile is obtained whose sides form an angle of  $54^\circ 58'$  with respect to the (100) surface. The side etch proceeded fastest in the [110] directions. The ordering of the etch rate was  $\{110\} > \{100\} > \{111\}B > \{111\}A$ , while in chemical etching (in 1%  $\text{Br}_2$ ) the ordering of the etch rate was  $\{011\} > \{111\}B > \{100\} > \{111\}A$ , and the etch rate on the  $\{111\}A$  planes was very slow.

Slight misalignment of the mask (a few degrees off the [011] direction) resulted in side etching which proceeded up to the  $\{111\}$  planes. This is shown in Fig. 4. The figure also shows the misalignment of the  $\text{SiO}_2$  mask (Fig. 4b shows the  $\text{SiO}_2$  mask on substrate before etch back) and the etched channels. The side walls are identified as  $(111)B$  and  $(111)B$  planes. In all misaligned channels the lateral etch realigned the etched channels parallel or perpendicular to

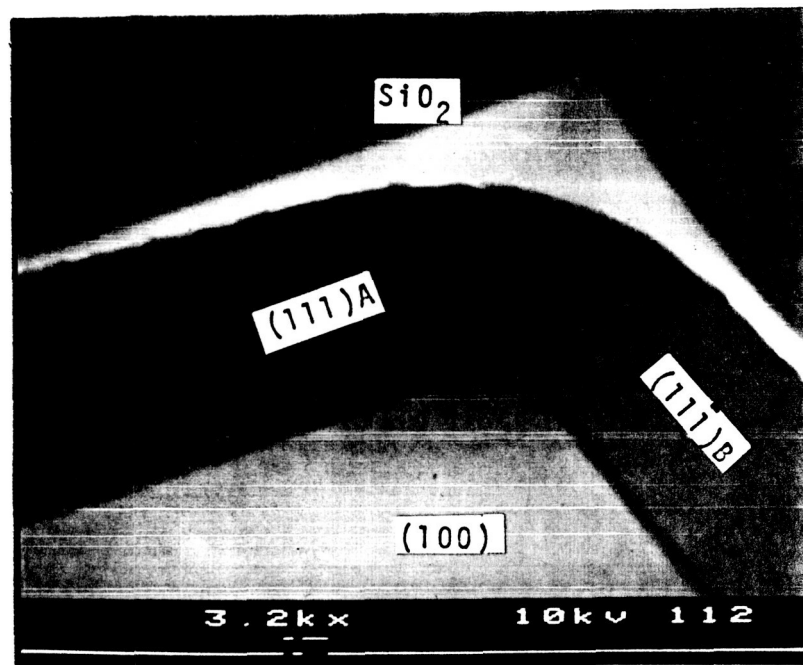


Fig. 3. SEM photomicrograph of LPEE etch morphology in (100) InP. The channel was etched at 640 °C and 5 A/cm<sup>2</sup> for 30 min. The SiO<sub>2</sub> mask overhangs the (111)B and (111)A sidewalls from about 1 μm in the <011> directions to about 20 μm in the <110> directions.

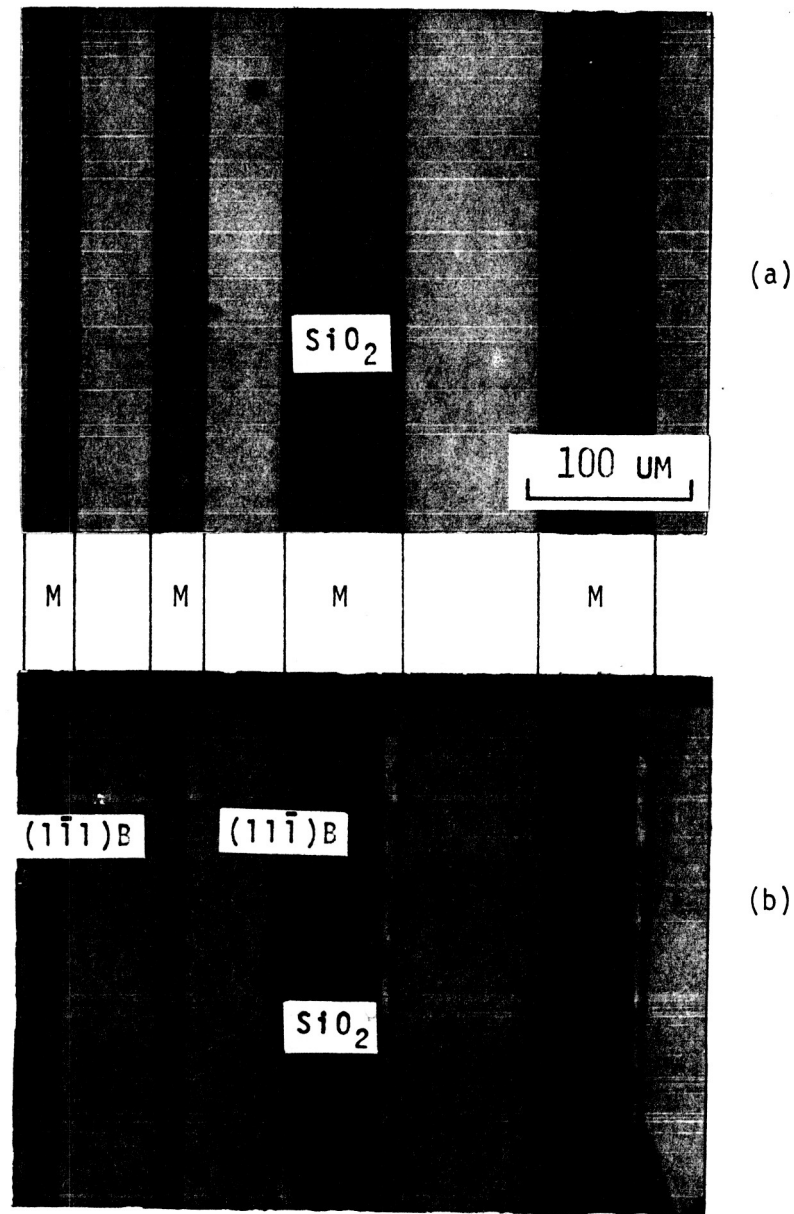


Fig. 4. Nomarski phase contrast photomicrographs of etch morphology with etch mask aligned about  $2^\circ$  off the  $[011]$  direction. (a) Unetched narrow strips. (b) Post-etch morphology. M indicates the  $SiO_2$  mask region.

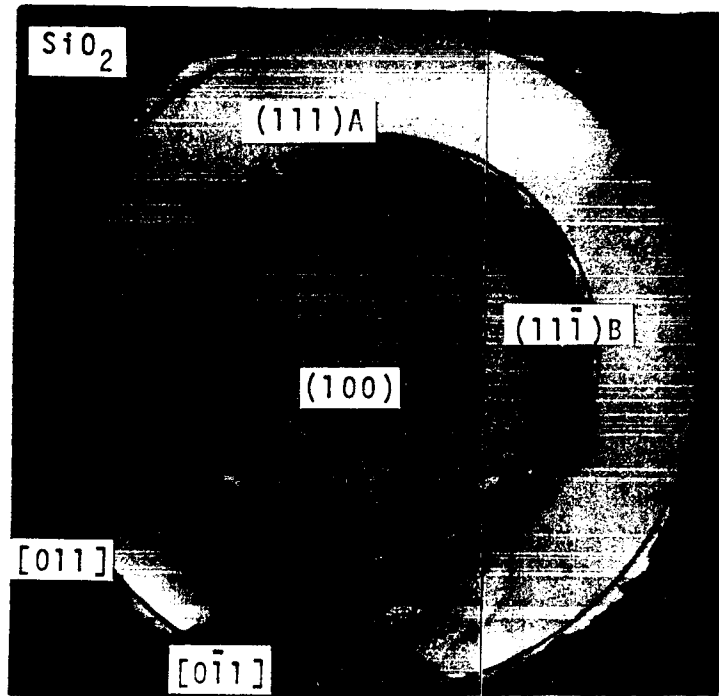
the [011] direction; consequently, wider channels were produced with well-defined trapezoid-shaped profiles.

Preferential etch by electroepitaxy was also demonstrated in etching circular and annular islands of InP. Figures 5a and 5b are examples of these geometries. Figure 5a shows that the lateral etch proceeded beyond the circle defined by the SiO<sub>2</sub> mask in the [110] directions, consequently transforming the circle into a square with well-defined sidewalls, i.e., the (111)A, (111)A, (111)B, and (111)B planes. The etch in the [111] directions, as the photo shows, is negligible when compared to the etch in the [110] or the [100] directions. Figure 5b also shows the lateral etch in the [110] directions. As the lateral etch proceeds in both directions, the outer circle gradually transforms into a square. In the annular region the lateral etch proceeded from both directions (inner circle and outer circle) in the [110] directions, thus tunneling under the SiO<sub>2</sub> mask. This resulted in transforming the annular region into four triangular-shaped islands. The side walls on the inner circle side are {111} planes, and a combination of {211}, {321} and other higher order planes on the outer circle side. The etch in the [100] direction produced a very flat surface (100) plane.

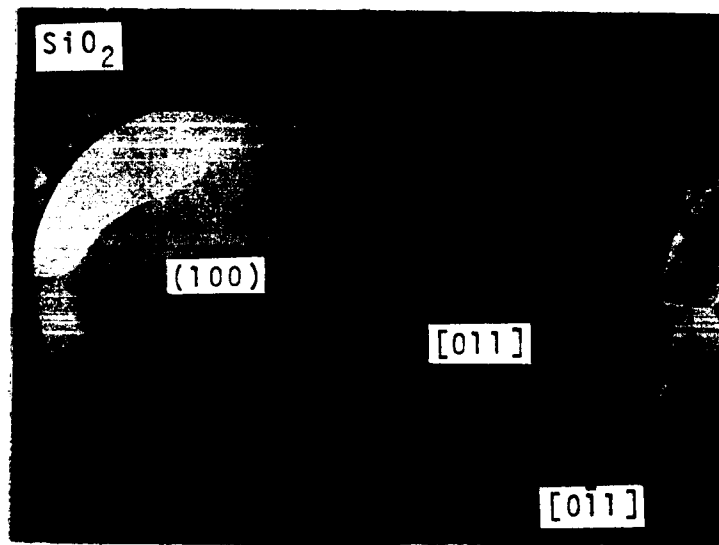
The results of this part of the study show that electroepitaxial etch is preferential and can produce uniform channels and trenches with well-defined shape. V-shaped grooves can also be etched by making the channel narrower.

## 2. Selective Area Etch Back and Growth

Channels and trenches formed by electroepitaxially etching the



(a)



(b)

Fig. 5. Nomarski phase contrast photomicrographs of etch morphology in (a) annular geometry, and (b) circular geometry masks. The  $\text{SiO}_2$  mask overhang is about  $1 \mu\text{m}$  in the  $\langle 011 \rangle$  directions and about  $30 \mu\text{m}$  in the  $\langle 110 \rangle$  directions.

masked substrate were refilled with lattice-matched InGaAs by first sliding the substrate to make contact with the InGaAs growth melt and then reversing the direction of DC electric current. The etch back melt used in this study was an In-InP melt. A melt carry-over caused the precipitation of polycrystalline InGaAsP instead of lattice matched InGaAs. Figure 6 is an example of this type of growth. To grow lattice matched alloy it was necessary to wipe clean the etched channels and trenches before making contact with the InGaAs melt. This was accomplished using another InGaAs melt as an intermediate wipe melt. Growth experiments performed this way produced lattice matched layers. Figures 7 and 8 are examples of selective etch back and growth. The growth completely refilled the etched channels and the substrate-growth interface is very uniform. The side walls of the grown layers are  $\{111\}$  planes, i.e.,  $(1\bar{1}1)B$  and  $(11\bar{1})B$ , whereas the side walls of the etched channels are  $(1\bar{1}1)B$  and  $(11\bar{1})B$  planes. The shape of the growth above the original level of the mask is the result of the fact that the  $\{111\}$  planes are slower growing than the  $\{100\}$ . A similar electroepitaxial growth result with GaAs has been reported by Yang, et al. [1]. The surface morphology of most layers is rough. This is attributed to a combination of rapid growth, some melt contamination from the wipe-melt and the In-InP etch-melt, and incomplete wipe after the growth is terminated. Better surface morphology is obtained when low current densities ( $<5A/cm^2$ ) were used.

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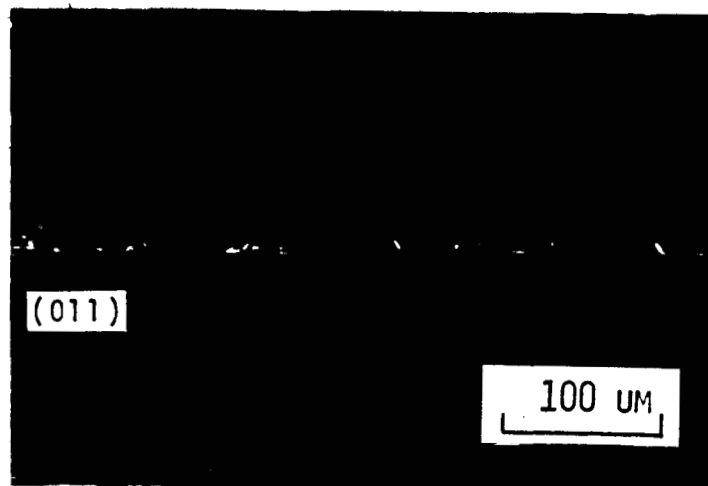


Fig. 6. Nomarski phase contrast photomicrograph of a cleaved and stained section of etched channels and selective growth. The growth is isolated in small areas and polycrystalline as a result of incomplete wipe-off of the InP etch-back melt.

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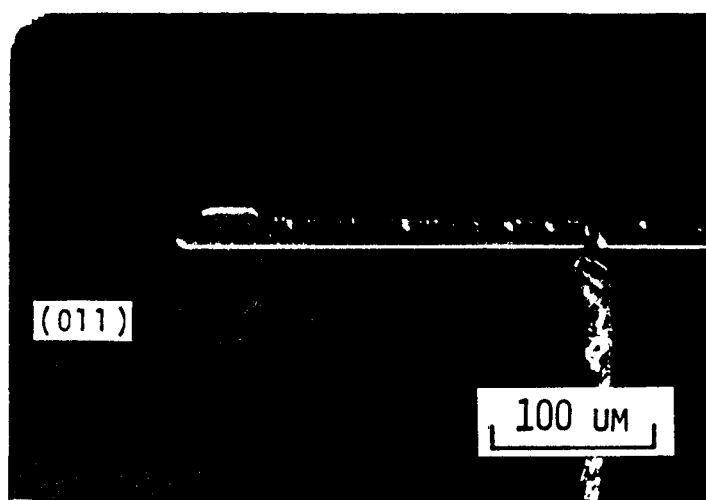


Fig. 7. Nomarski phase contrast photomicrograph of cleaved and stained section of etch-back and growth of lattice-matched InGaAs. The channel is about 7  $\mu\text{m}$  deep and 450  $\mu\text{m}$  wide. The growth is 18-27  $\mu\text{m}$  thick. The growth interface is very uniform; however, the surface is rough due to carryover of the etch-back melt.



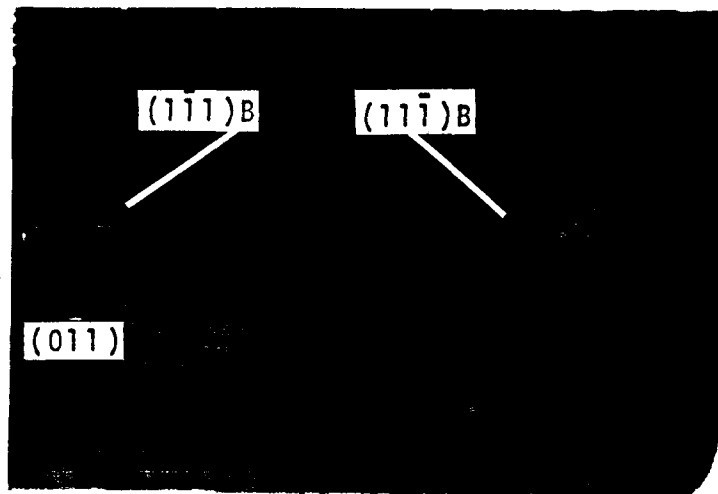


Fig. 8. Nomarski phase contrast photomicrograph of cleaved and stained section of etch-back and growth of lattice-matched InGaAs. The channels are 40-50  $\mu\text{m}$  wide (at the  $\text{SiO}_2$  level) and 7-10  $\mu\text{m}$  deep. The etch-back and growth were performed at 640  $^\circ\text{C}$  and 10  $\text{A}/\text{cm}^2$  for 60 min., and 5  $\text{A}/\text{cm}^2$  for 30 min., respectively.

## B. Growth and Characterization of InGaAsP

InGaAsP quaternary alloys with compositions corresponding to 1.31  $\mu\text{m}$  and 1.52  $\mu\text{m}$  have been studied in detail. These alloys have applications in devices for optical fiber communications since the fibers exhibit desirable transmission and dispersion properties in these wavelength regions.

### 1. Growth of InGaAsP Alloy Layers by LPEE

The epitaxial InGaAsP layers were grown lattice matched to (100) InP substrates using the LPEE technique at 645  $^{\circ}\text{C}$ . The melt composition calculations were based upon information for the InGaAsP system by Hsieh [2]. Two solidus compositions were grown:  $\text{In}_{.60}\text{Ga}_{.40}\text{As}_{.25}\text{P}_{.15}$  (corresponding to a wavelength of 1.52  $\mu\text{m}$ ) and  $\text{In}_{.73}\text{Ga}_{.27}\text{As}_{.60}\text{P}_{.40}$  (corresponding to a wavelength of 1.31  $\mu\text{m}$ ). Growths were performed at a constant furnace temperature of 647  $^{\circ}\text{C}$  with a direct current density of 3 to 15  $\text{A}/\text{cm}^2$ .

The growth rate was found to be a function of the composition of the quaternary layers. The growth rate of the  $\text{In}_{.60}$  layers was almost six times larger than that of the  $\text{In}_{.73}$  layers. Furthermore, layers thicker than 3  $\mu\text{m}$  could not be grown for  $\text{In}_{.73}$  layers. The low growth rate of this material has been attributed to the fact that this composition lies in the miscibility gap region. A similar trend of decrease in growth velocity with increasing P content in the solid was also observed in conventional thermal LPE.

Analytical values of the growth velocity for different compositions were calculated using the Bryskiewicz model [3]. It was assumed that electromigration/electrotransport is the dominant mechanism contributing

to the growth process. The differential mobility and diffusion of Ga were used as the fitting parameters and a good fit to the experimental data was obtained. It was found that the diffusion coefficient of P and the differential mobility of P were the rate limiting factors for LPEE grown layers as in the case of thermal LPE.

In order to avoid the miscibility gap in the phase diagram, growths of the 1.3  $\mu\text{m}$  alloy were performed at 685 °C. Various melt baking sequences were tried in order to reduce the residual carrier concentration. A low concentration of  $1 \times 10^{18} \text{ cm}^{-3}$  has been achieved.

## 2. Characterization of Mn-Doped InGaAsP Layers

Another objective of the proposed research was the investigation of suitable p-type dopants for device applications. Manganese was chosen since it has been found to be the best suited for practical applications, especially for quaternary compositions closer to the ternary  $\text{In}_{.53}\text{Ga}_{.47}\text{As}$  [4,5]. P-type InGaAsP layers with doping levels varying from  $8 \times 10^{16}$  to  $4 \times 10^{18} \text{ cm}^{-3}$  with excellent surface morphology were grown by LPEE. The layers were characterized using X-ray diffraction, and Hall and photoluminescence measurements at low temperatures (77 K). Analysis of the temperature dependence of the carrier concentration data permitted the determination of the activation energy of the Mn acceptor energy level, and the donor and acceptor densities in the epilayer. The activation energy of the Mn acceptor level decreased from 57 meV to 32 meV with increasing hole concentration from  $1 \times 10^{17}$  to  $1.2 \times 10^{18} \text{ cm}^{-3}$ . The temperature dependence of the mobility data was analyzed in terms of different scattering mechanisms prevalent in the layer. This also provided information about the

acceptor and donor densities. In undoped layers, ionized impurity scattering is dominant for temperatures lower than 120 K, while polar optical phonon and alloy scatterings account for the variation in mobility at higher temperatures. In Mn doped layers, a good fit to the experimental data is obtained only when non-polar optical phonon and acoustic lattice mechanisms were taken into account as shown in Fig. 9. Both the Hall mobility and Hall constant data indicated a lower donor to acceptor concentration ratio than normally observed in p-type layers using other dopants, indicating that Mn is an efficient acceptor for InGaAsP layers.

The van Roosbroeck-Shockley model [6] describes fairly well the spectral line shape of the photoluminescence spectrum from the undoped quaternary layer if the absorption coefficient is assumed to vary exponentially with the energy below the band gap. The qualitative features of the Mn level were deduced from the temperature and incident excitation power level studies of the photoluminescence spectral peaks from doped layers.

Copies of two published papers regarding the characterization of the InGaAsP alloy material appear in Appendix A.

### C. Deposition of Aluminum Oxide for Use as a Gate Insulator

The objective of this task was the evaluation of a low temperature deposition process for the formation of insulating layers on InGaAs. This layer could potentially be used as the gate insulator in a MISFET structure which would take advantage of the high electron mobility of the InGaAs alloy which is lattice-matched to InP. The features of this deposition process are the pyrolytic decomposition of aluminum

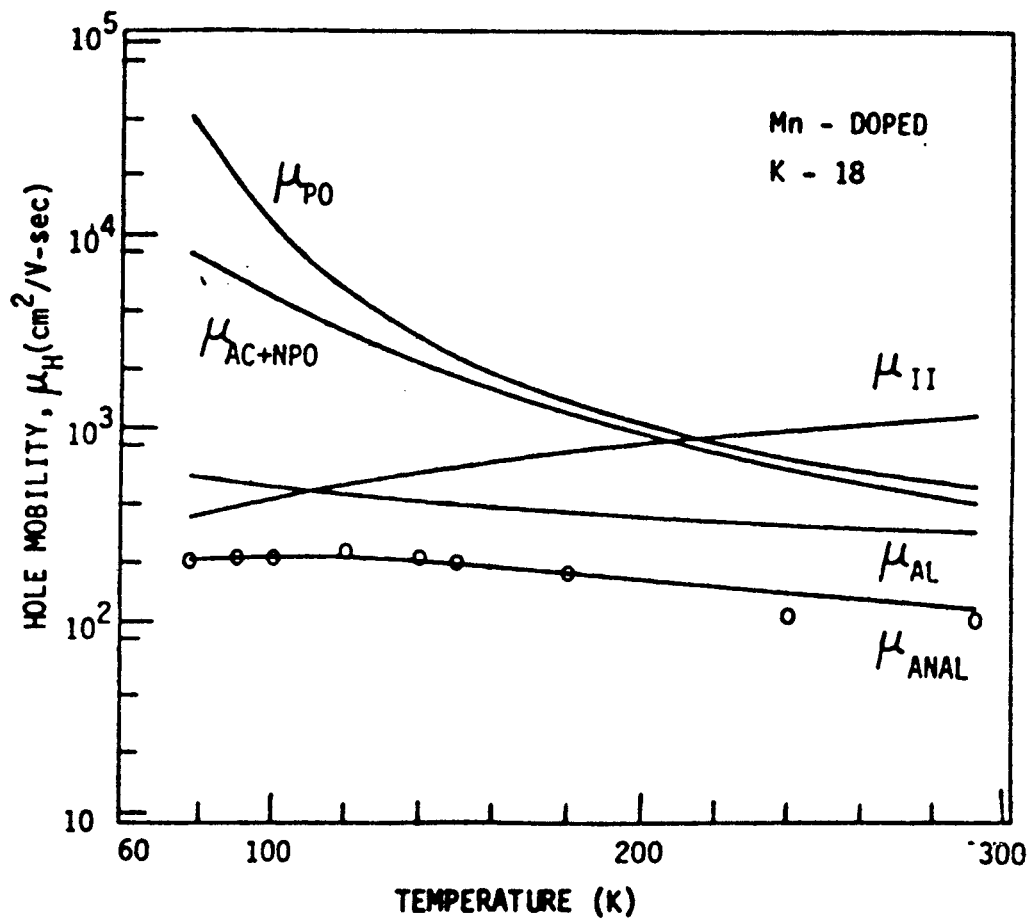


Fig. 9. Analytical temperature dependences of the various scattering mechanisms in the quaternary material. The open circles indicate experimental mobility data.

isopropoxide vapor at approximately 300 °C in an argon atmosphere. The deposition process and the characterization of the insulator by capacitance-voltage measurements have been described in a previous report [7]. MIS capacitor structures on Si and InGaAs exhibited considerable hysteresis in the depletion regime of the C-V curves. This effect is related to the difficulties observed by others in the use of deposited alumina as the gate insulator in MISFET's [8,9]. Interface states are apparently the cause of the hysteresis effect and the resulting temporal drain current instability in FET devices fabricated with an alumina insulator. An in situ etch of the InP substrate surface with a high concentration of HCl vapor prior to the alumina deposition has been reported to result in a much more stable drain current characteristic [10].

A C-V characteristic of an Al-Al<sub>2</sub>O<sub>3</sub>-pInGaAs MIS capacitor is shown in Fig. 10. The hole concentration in the InGaAs is about  $2 \times 10^{17} \text{ cm}^{-3}$ . Because of the poor quality of the insulator-semiconductor interface, this gate insulator deposition process was abandoned after the second year of the research effort. Since the process is relatively simple to implement, it may remain useful for situations requiring a masking layer as part of a processing sequence.

#### D. Metal-Organic Vapor Phase Epitaxy System

As part of this research, hybrid growths of device structures were to be performed with the LPEE and metal-organic vapor phase epitaxy (MOVPE) systems. Some of the MOVPE system development and installation work was accomplished in this research grant. However, the grant period expired before the system could be made completely operational. Thus,

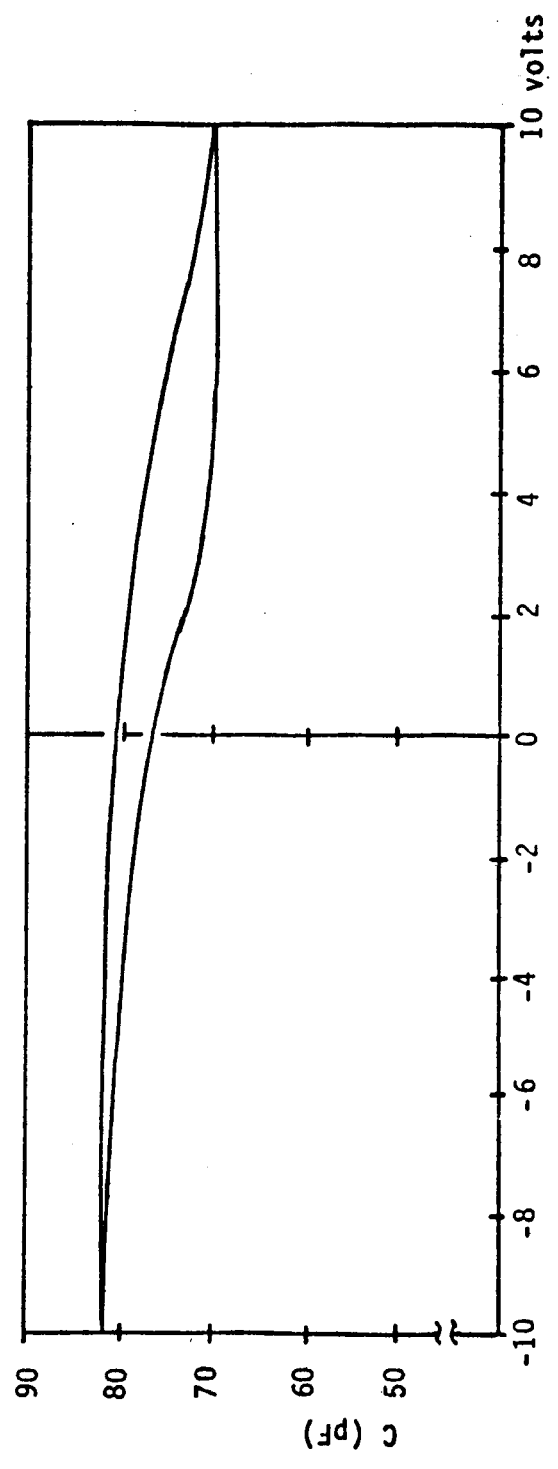


Fig. 10. C-V characteristics of an Al-Al<sub>2</sub>O<sub>3</sub>-pInGaAs capacitor measured at 1 MHz. The bias sweep rate is 4.5 V/s.

the hybrid growth aspects of the research tasks could not be completed. The additional work required is minor, but actual MOVPE system operation will be delayed until appropriate research funding can be acquired to support the consumables and toxic waste management expenses. A schematic diagram of the MOVPE system is shown in Figure 11.

The MOVPE system has been somewhat modified with respect to the originally purchased system, primarily with respect to the control and safety interlock circuitry. A liquid metal eutectic (In-Ga-Al) purifier has been purchased for addition to the arsine inlet line to remove contaminants which are reactive with the aluminum. The system will operate at atmospheric pressure with a RF-heated pyramidal susceptor in a vertical configuration. The present capabilities include three liquid source channels (e.g., gallium, aluminum and zinc dopant) and two gas source channels (e.g., arsine and hydrogen selenide dopant). Gas flow is controlled by electronic mass flow controllers and Nupro three-ported air-operated valves.

Ultimately, it will be desirable to include a phosphine channel, perhaps with a cracking furnace, for the growth of (III)-P compounds and alloys.



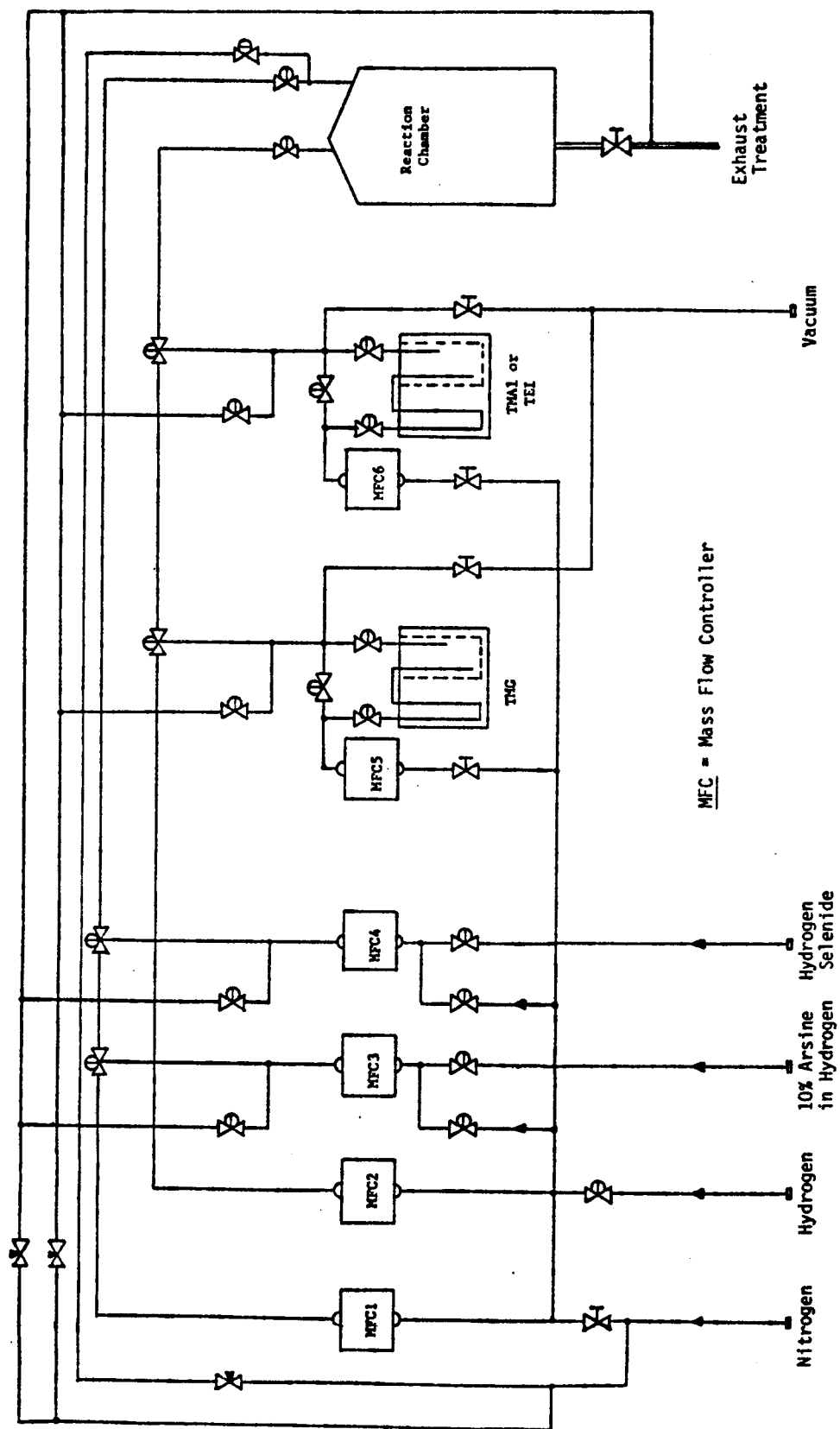


Fig. 11. Schematic diagram of metal-organic vapor phase epitaxy system.

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**APPENDIX A: PUBLISHED ARTICLES**

"Characterization of Mn-Doped InGaAsP Grown by LPEE,"  
Shanthi N. Iyer, Ali Abul-Fadl, Ward J. Collis and Mohammad N.  
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Films, 163, p. 427 (1988).