PRELIMINARY DESIGN DOCUMENT

GROUND BASED TESTBED FOR AVIONICS SYSTEMS

for Marshall Space Flight Center

Contract Number NAS8-37578

Definition of Avionics for a

Heavy Lift Cargo Vehicle

Document Requirement 7

February, 1989

GENERAL DYNAMICS
Space Systems Division

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1.0   INTRODUCTION

The Preliminary Design Document (PDD) was developed by the Space Systems Avionics group of the Space Systems Division of General Dynamics as Data Requirement 7 of the "Definition of Avionics Concepts for a Heavy Lift Cargo Vehicle" study for Marshal Space Flight Center under contract NAS8-3578. This requirement was added to the contract in November of 1988.

1.1   SCOPE

This document contains the design and interface requirements.for an avionics Ground Based Test bed (GBT) to support Heavy Lift Cargo Vehicles (HLCV). It also contains data on the vehicle subsystem configurations that are to be supported during their early, pre-PDR developmental phases. Several emerging technologies are also identified for support. A Preliminary Specification Tree is also presented.

1.2   BACKGROUND

The HLCV study emphasis shifted to a thorough definition of the requirements and resulting design of the GBT mid way through the study with official approval preceding the third Quarterly Review. The Avionic Systems for the HLCV Reference vehicles have been defined to the level required to size the GBTs main processor, G&N Extension, and interconnecting buses and networks. A target implementation schedule was provided by MSFC in October linking the HLCV GBT and the Marshall Avionics System Test bed (MAST) efforts. This schedule also defined specific functional support levels with dates and projected budget allocations (see Figure 1.2-1). A candidate site for the GBT was also provided (see Figure 1.2-2). The third Quarter Review reflected these inputs and specifically costed the Phase 1 lab configuration. The Preliminary Design Document is structured to cover all the elements identified in the final or Target GBT configuration but only gives detailed specifications for these elements in the Phase 1 configuration.

1.3   ORGANIZATION

Figure 1.3-1 shows the Target GBT configuration. The PDD is organized around this final functional configuration. The GBT Core, Display Center, Avionics Hardware Test Bed and Instrumentation Test Set are the four main sections of the GBT. The Software Development facility, Guidance and Navigation Lab, Image Processing Extension and Power System Extension are co-located lab resources. Special interface accommodations have been provided to support the existing or soon-to-be-developed Propulsion Systems Lab, Actuator Lab and Fluids and Pneumatics Lab.

It is important to note that though all of the above mentioned GBT components will be included in this document, only those components shown in Figure 1.3-2, "GBT Phase 1 Configuration" will be covered in detail.
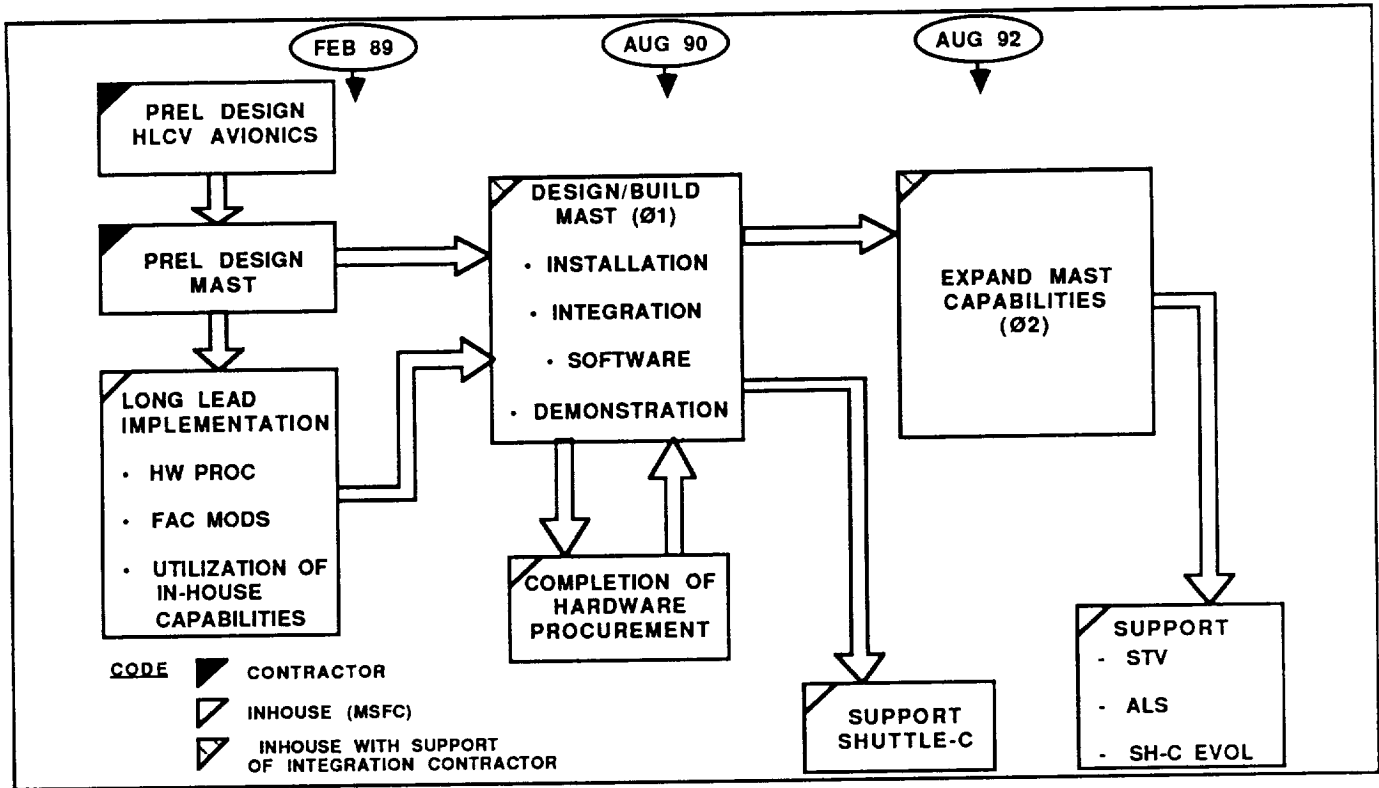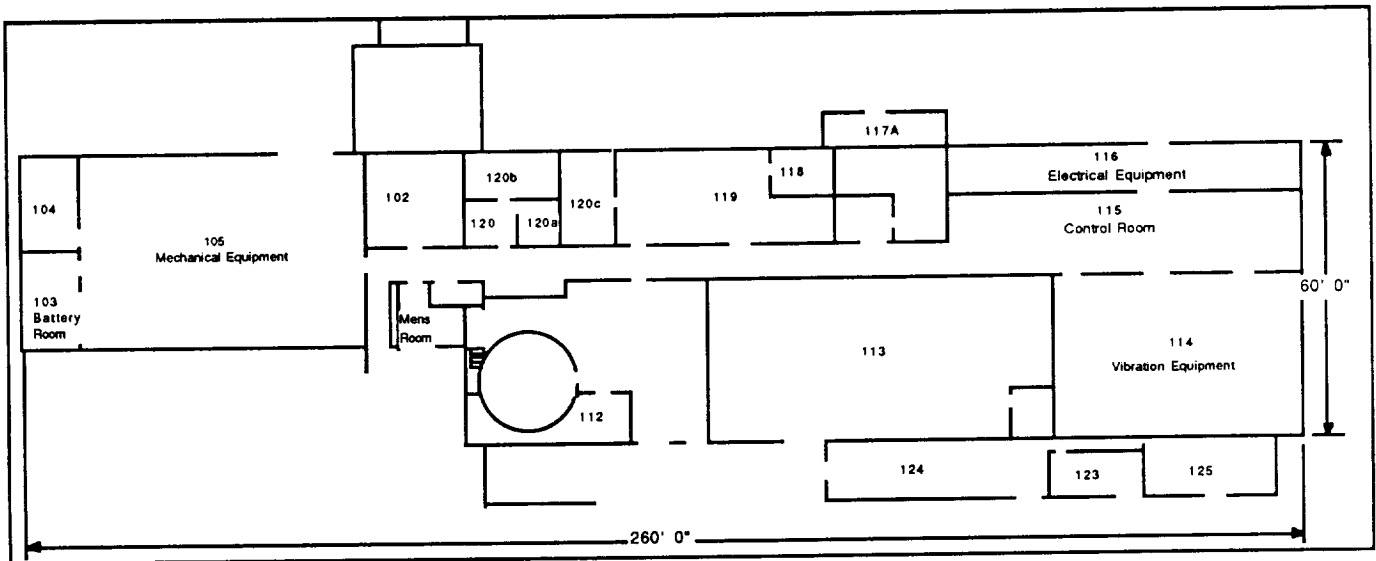
Figure 1.2-1. MAST Implementation Flow

Figure 1.2-2. Proposed GBT Site - Building 4476
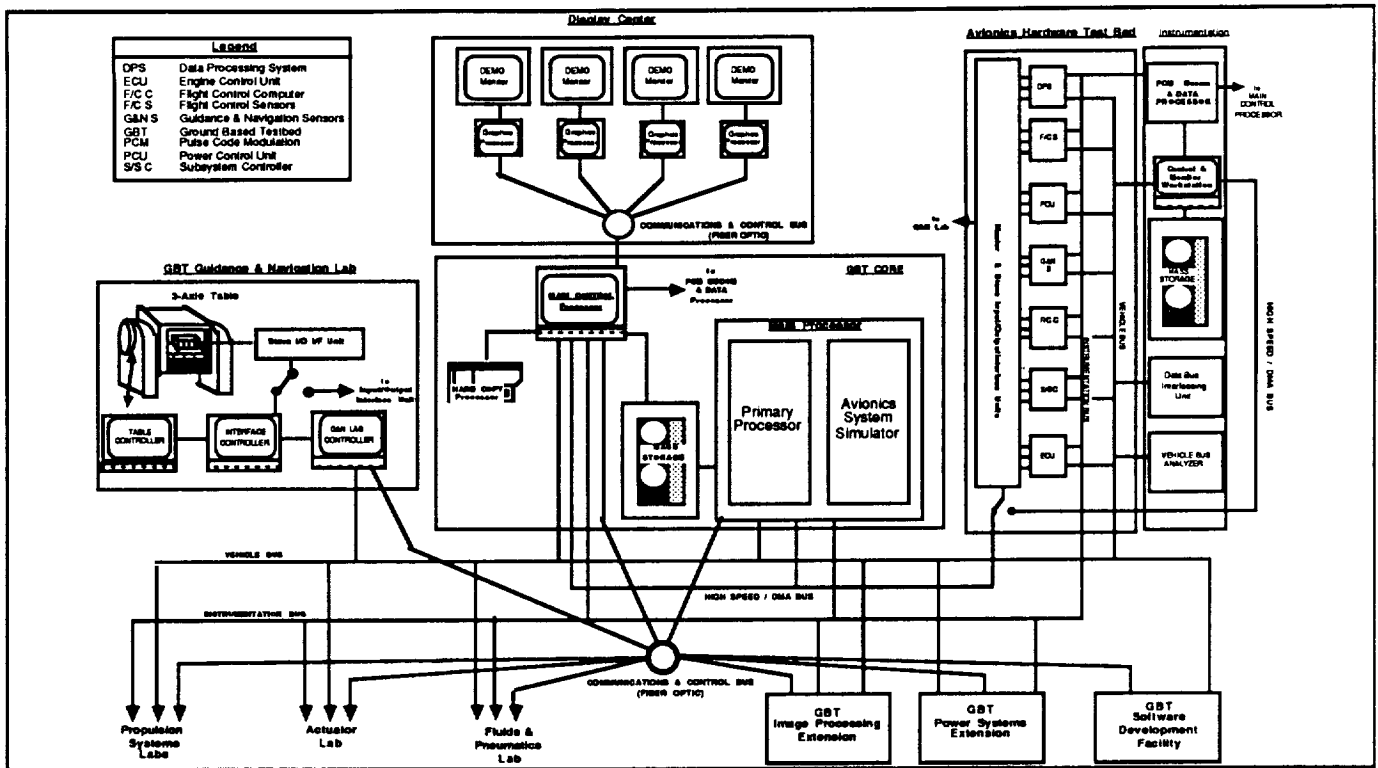
Figure 1.3-1.   GBT Target Configuration
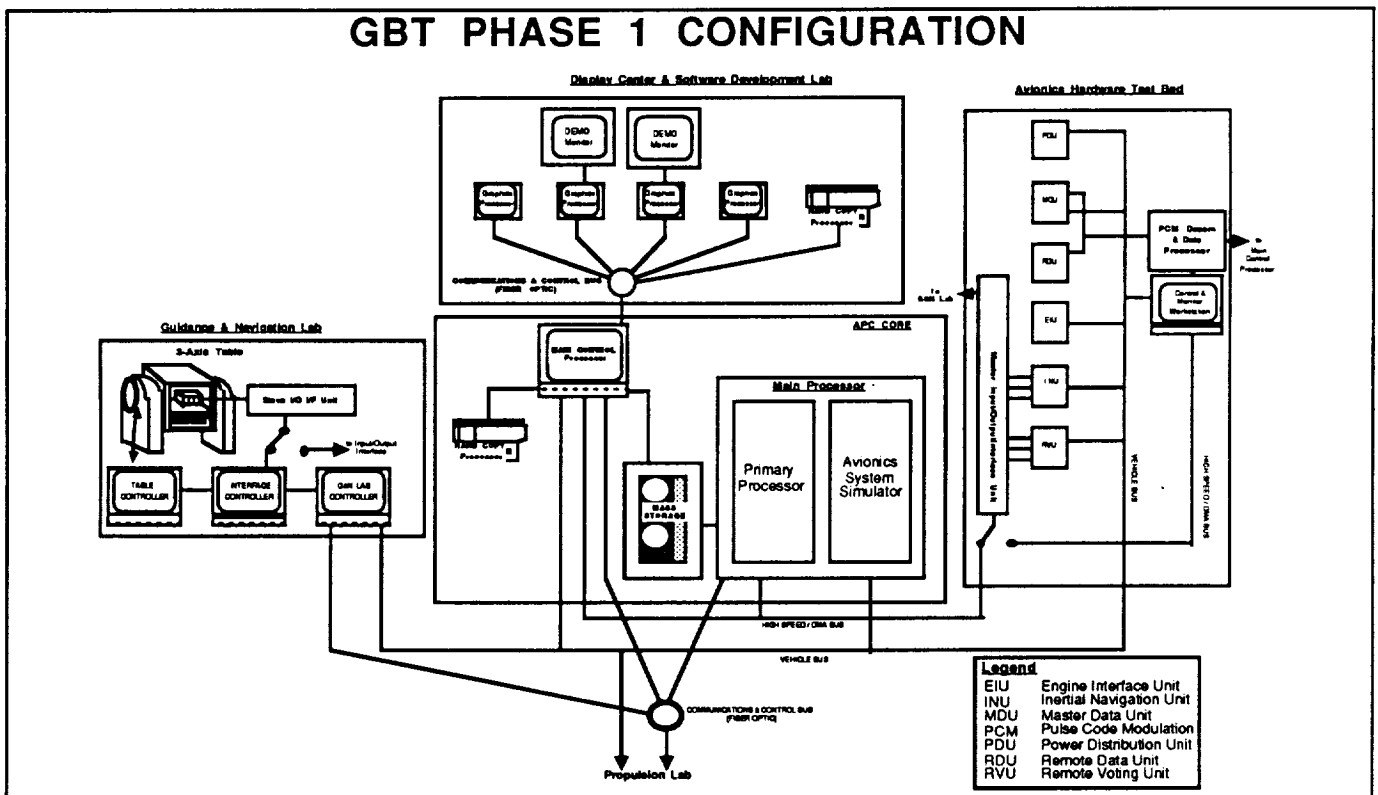
Figure 1.3-2.   GBT Phase 1 Configuration

2.0   REQUIREMENTS

2.1   GENERAL

The GBT goal or Target configuration was determined by several types of requirements. These requirements ranged from specific, program support driven performance specifications to the more philosophical user friendly,easy accessibility type. The following sections cover this range of requirements, starting with the more general, top level types. The more specific requirements are focused on the early, Phase 1 configuration.

2.1.1 GBT OBJECTIVES

The GBT was envisioned as a general resource facility providing to new vehicle programs a cost effective method of evaluating the avionics concepts and technologies employed in their design. This resource would permit complete end-to-end simulations of system operation in the simulated mission environment desired.

The GBT was to be set up to encourage use by all HLCV era vehicles during their initial design phases. Review of past projects involving total vehicle or subsystem development have repeatedly shown the need for such a readily accessible and powerful test and evaluation facility. The traditional dedicated test and development facilities have not been able to support their projects early enough to optimize system requirements and design. New projects must initially use facilities dedicated to other projects . Seldom do such facilities provide all the necessary testing capabilities or time for the required work.

The key to the HLCV GBT success is seen to simply be: <u>Cost Effectiveness</u>. To obtain this objective, the Lab must be readily accessible at the time when the new projects traditionally didn't have their own dedicated facilities. GBT access must be simple and bound with a minimum of red tape. Once accessed, the GBT must provide a user friendly environment, an environment that can quickly be configured to access the required testing and logging resources. The resources must be capable of evaluating the concepts, technologies or designs to the required level of accuracy and against recognized performance benchmarks. Finally, the GBT must provide not only easy replication of the testing, but also provide the ability to thoroughly analyze the results and to report the results in forms which effectively communicate their significance.

The GBT objectives are summarized below:

- To provide an avionics integration, test, and demonstration facility for the future

- Support future vehicles
  - HLCV (2ES, 2RS, FBB & PRCV)
  - ALS (All concepts)
  - Upper Stages (Centaur, STV, OMV extensions)
  - Shuttle Payloads/Experiments -
  - Lunar/Mars transfer vehicles

- Evaluate systems and subsystems designs and performance
  - New avionic subsystem technology

- Evaluate effects on systems of a particular avionics subsystem or unit
  - Benchmark testing

- Demonstrate the "integration-ability" of "new" subsystems, both avionics and all vehicle controls
  - Between subsystems, end-to-end functions
  - Within subsystems, redundancy management
  - Operations, A/B & GSE

- Expandable
  - Initial configuration
  - Growth capability

2.1.2 GBT PHILOSOPHY

The major points upon which the GBT design philosophy is based are:

- a. Reconfigurable Design
- b. Real Time
- c. Functional Testing of hardware & software
- d. Modular Design
- e. Flexible
- f. Demonstration Oriented
- g. User Friendly

The first point addresses the non-project dedicated nature of the GBT design. It must be an evolving facility, capable of supporting several current and near term avionic systems. This translates to a firm requirement for rapid reconfigurability. The GBT must not only be able to switch from one test configuration to another, but it also must have sufficient capability to support several parallel efforts simultaneously. These efforts will include everything from basic evaluation of single units in an open loop environment, to full up, multi-string system simulation.

To be truly useful to a number of projects simultaneously, the GBT must accommodate a variety of software and hardware configurations. The current implementation plan establishes an August 1990 IOC for Shuttle-C. In actuality, the GBT will have more than half of its total planned capability at this point. The software tools and models developed for the Shuttle-C are basically generic in nature, with separate data files supplying the unique values for this vehicle, its subsystems, and mission profiles. In most cases, only data set value changes would be required to switch from one vehicle configuration to another.

The other limiting factor would be the hardware status. The GBT is modular at all software and hardware functional levels so, as it develops and the support requirements change, the lab can add or access the required resources. This translates to the GBT being able to

accommodate any vehicle or system simulation of similar complexity to the then current defined reference vehicle and systems.

2.2   VEHICLE/PROGRAM DRIVEN REQUIREMENTS

The GBT was conceived to provide support to new vehicle/spacecraft programs primarily before their respective Preliminary Design Reviews, (PDRs), or when the nature of the required support was beyond the capabilities of their local, dedicated facilities. Figure 2.2-1 outlines some of the requirements associated with these vehicles and their mission profiles. Figure 2.2-2 gives an evolutionary perspective of an early ALS program development plan and some of the concepts/configurations explored.

Vehicle	Shuttle C	ALS Core	ALS LRB	FRWB
Reusability	SRB's	None	BRM	Full Reuse
IOC	1995	1998	1998	2002
Engines	3 + 2 SRB	3	7	6 + 6 A/B
Man Rating	TBD	0.99981	0.99995	TBD
Reliability	Cargo carrier Prox OPS & De-orbit	Deorbit to ocean. FO/FS Manned Cargo	Sub-orbital FO/FS Manned Cargo	Return & Landing FO/FS Manned Cargo
Max Mission Duration	6-1/2 hours plus s.s ops	Core de-orbit T + 98 min.	T + 162 seconds	Less than 1 hour
Mission/Year	Few	Many	Many	Many
Number of Vehicles	Moderate	Many	Many	Few
Integrated Systems	Separate LPS, GSE Prod C/O	UNIS for Integrated Data	UNIS	UNIS
Launch Processing	LPS	Expert System App	Expert Systems App.	Near Autonomous
P/L and Vehicle I/F's	Shuttle Bay Interface	None	None	None
Vehicle Management	Central computers O.S Command Uplink	Mission manager Expert Systems	Controlled from Core	Near Autonomous Manual Backup
Rendezvous & Docking	OMV Assisted	None	None	None
Data Flow	TBD Fairly low rate	GN&C 3 - <1 MBPS Instru 1 - 256 KBPS	Interface to Core	GN&C 3 - <10 MBPS Instru 1 - 320 KBPS
Processing	300 KOPS	GN&C 3 - 3 MIPS Propulsion 3 - 1 MIPS Instru 1 - 3 MIPS Miscellaneous < 1 MIPS	Share core GN&C Propulsion 7 - 1 MIPS Share core Instru Miscellaneous <1 MIPS	GN&C 3 - 6 MIPS Propulsion 6 - 1 MIPS Instru 1 - 3 MIPS Imaging 10 MIPS Miscellaneous <2 MIPS

Figure 2.2-1. Heavy Lift Cargo Vehicle Avionics Requirements
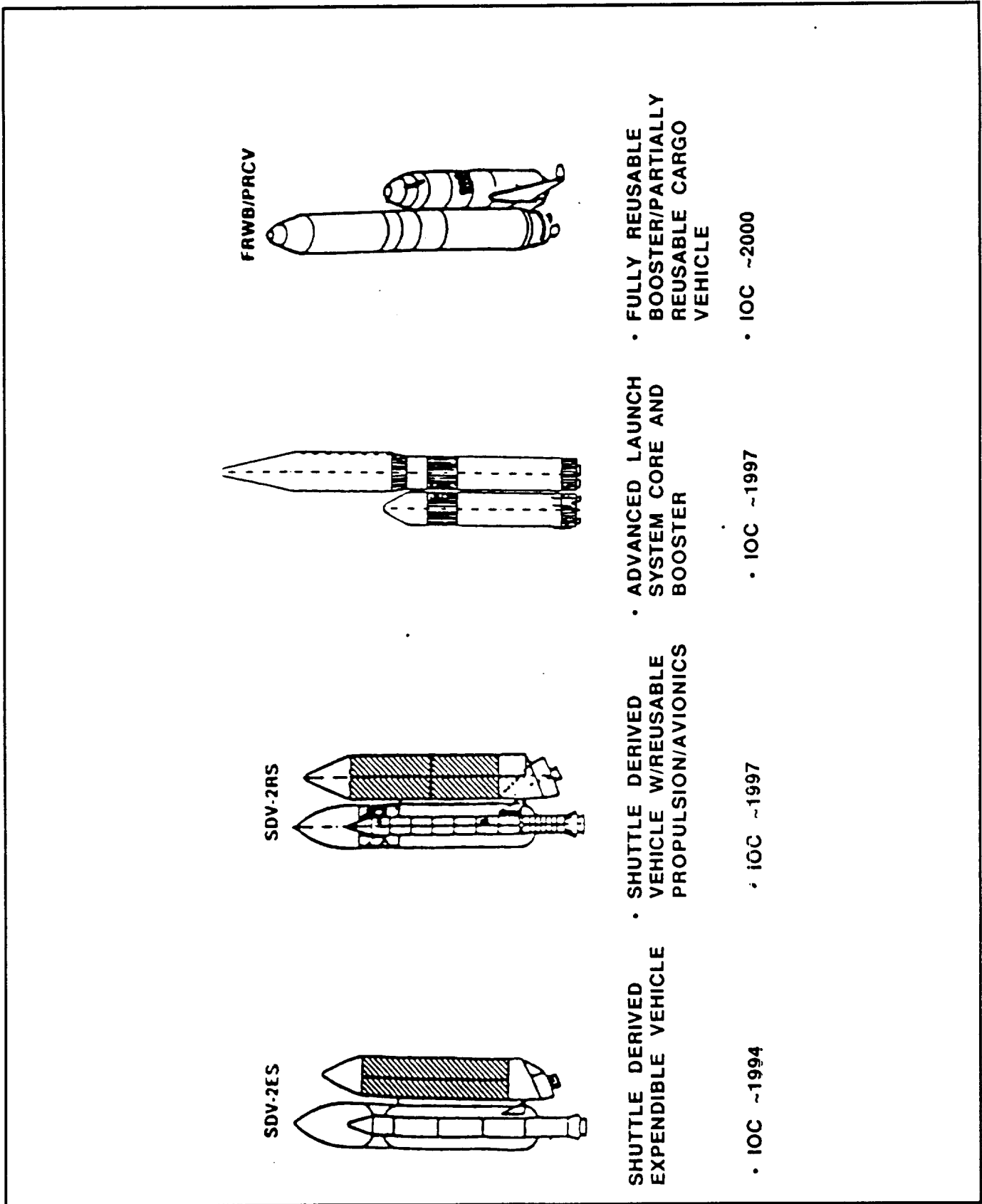
Figure 2.2-2.   HLCV Era Candidate Vehicle Configuration
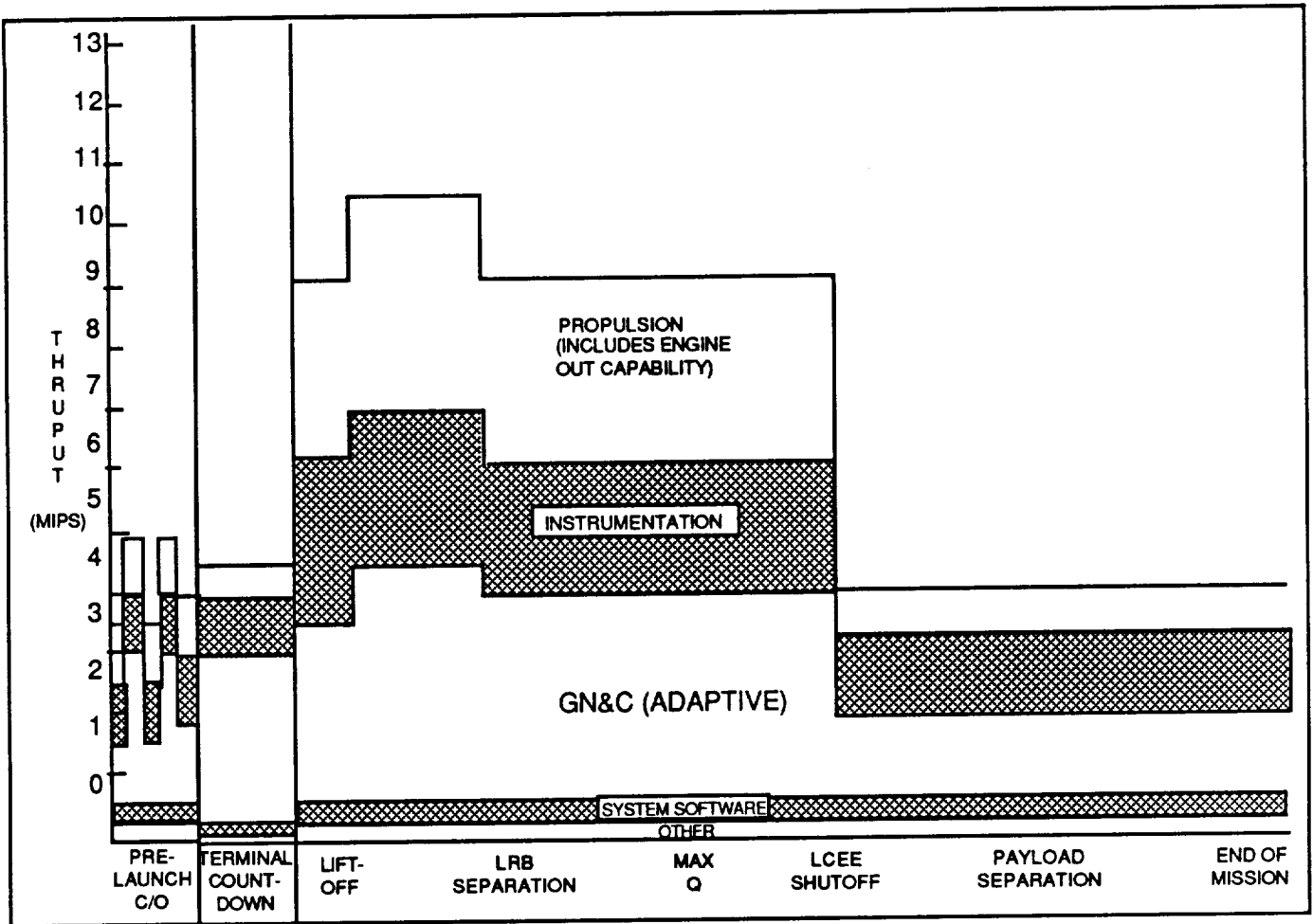
Figure 2.2.2-5.   ALS Core Processing Timeline

2.2.1   PHASE 1 (STV, SHUTTLE C, SDV 2ES)

The HLCV expendable booster, (SDV-2ES), Shuttle-C, and Space Transfer Vehicle developmental programs are the basis for the Phase 1 GBT functional requirements. Figure 2.2.1-1 shows the phase1 capabilities and constraints. The Initial Operational Capability, (IOC), of the GBT is currently set for August 1990. The Shuttle-C with non STS avionics was agreed upon to serve as the forcing function for the Phase 1 lab. The functional block diagram for this three-string avionics system is shown in Figure 2.2.1-2. Its accompanying design reference missions are shown in Figure 2.2.1-3 and 2.2.1-4. Figure 2.2.1-5 outlines some of the Shuttle-C design guidelines.

1.   MISSION MODELS - (2DV-2ES)
      •   LAUNCH
      •   ASCENT
      •   ON ORBIT (MANEUVER)
      •   ENTRY

2.   SYSTEM TEST
      •   SDV REFERENCE SYSTEM
             •   IMU
             •   COMPUTER
             •   DAS
             •   MDU
             •   RDU
             •   MDM * INTERFACE ONLY
             •   EIU * INTERFACE ONLY

3.   OUTSIDE RESOURCES
      •   SSME LAB INTERFACE
      •   EMA (OPTION)

Figure 2.2.1-1.   Phase I Capabilities & Constraints
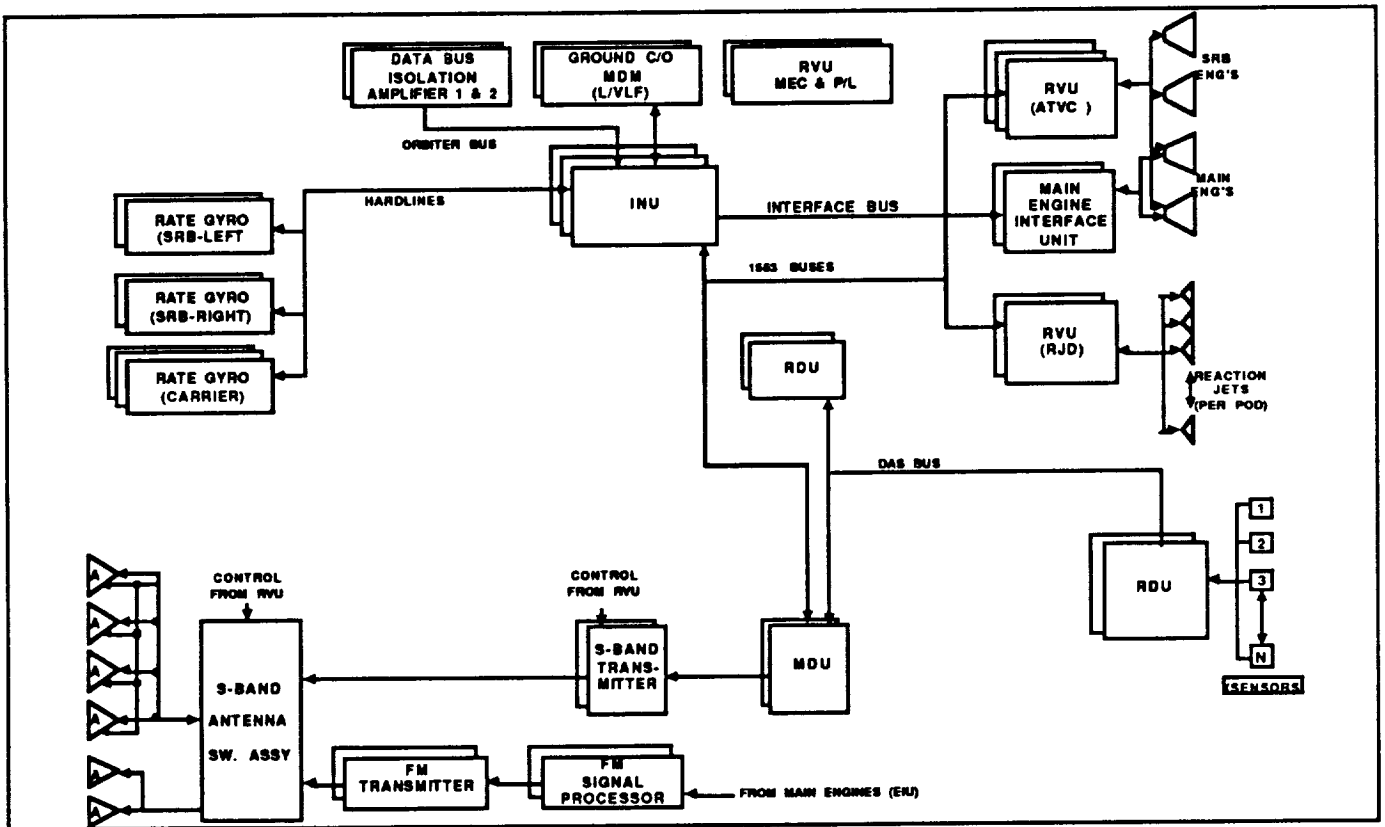
Figure 2.2.1-2.   GBT Phase I Shuttle-C Avionics Baseline

DISCRIMINATING CHARACTERISTICS	DESIGN REFERENCE MISSIONS (DRM'S)			PERFORMANCE REFERENCE MISSIONS (PRM'S)	
	(1) UNMANNED SPACE STATION ASSY W/OMV	(2) ORBITAL DEPLOY	(3) SUB-ORBITAL DEPLOY	(1) POLAR LAUNCH FROM ETR	(2) POLAR LAUNCH FROM WTR
LAUNCH SITE	ETR	ETR	ETR	ETR	WTR
SECURE	NO	POSSIBLY	POSSIBLY	POSSIBLY	YES
INCLINATION	28.5'	28.5'-63.5'	28.5'	98.7'	98.7'
RENDEZVOUS & PROX OPS	YES	NO	NO	NO	NO
REFERENCE ALTITUDE	220 nmi	110 nmi	≥ 100 nmi	100 nmi	100 nmi
DOCK/BERTH	YES	NO	NO	NO	NO
ON-ORBIT STAY TIME	APPROX. 14 DAYS	1 DAY	UNSPECIFIED	≤2-1/2 HR	≤2-1/2 HR
CIRCULARIZATION	YES	YES	NO	YES	YES
PAYLOAD DEPLOYED	NO	YES	YES	YES	YES
PAYLOAD EXTRACTED	YES	NO	NO	NO	NO
MANNED PRESENCE	YES	NO	NO	NO	NO
MIXED CARGO	YES	POSSIBLY	NO	POSSIOBLY	POSSIBLY
OMV	YES	POSSIBLY	NO	NO	NO
MINIMUM INJECTED WEIGHT @ REFERENCE ALTITUDE	100,000 LB	80,000 LB	100,000 LB	TBD	TBD
INSERTION	DIRECT	STANDARD	SUBORBITAL	UPSPECIFIED	UNSPECIFIED

Figure 2.2.1-3.   Shuttle-C Reference Missions
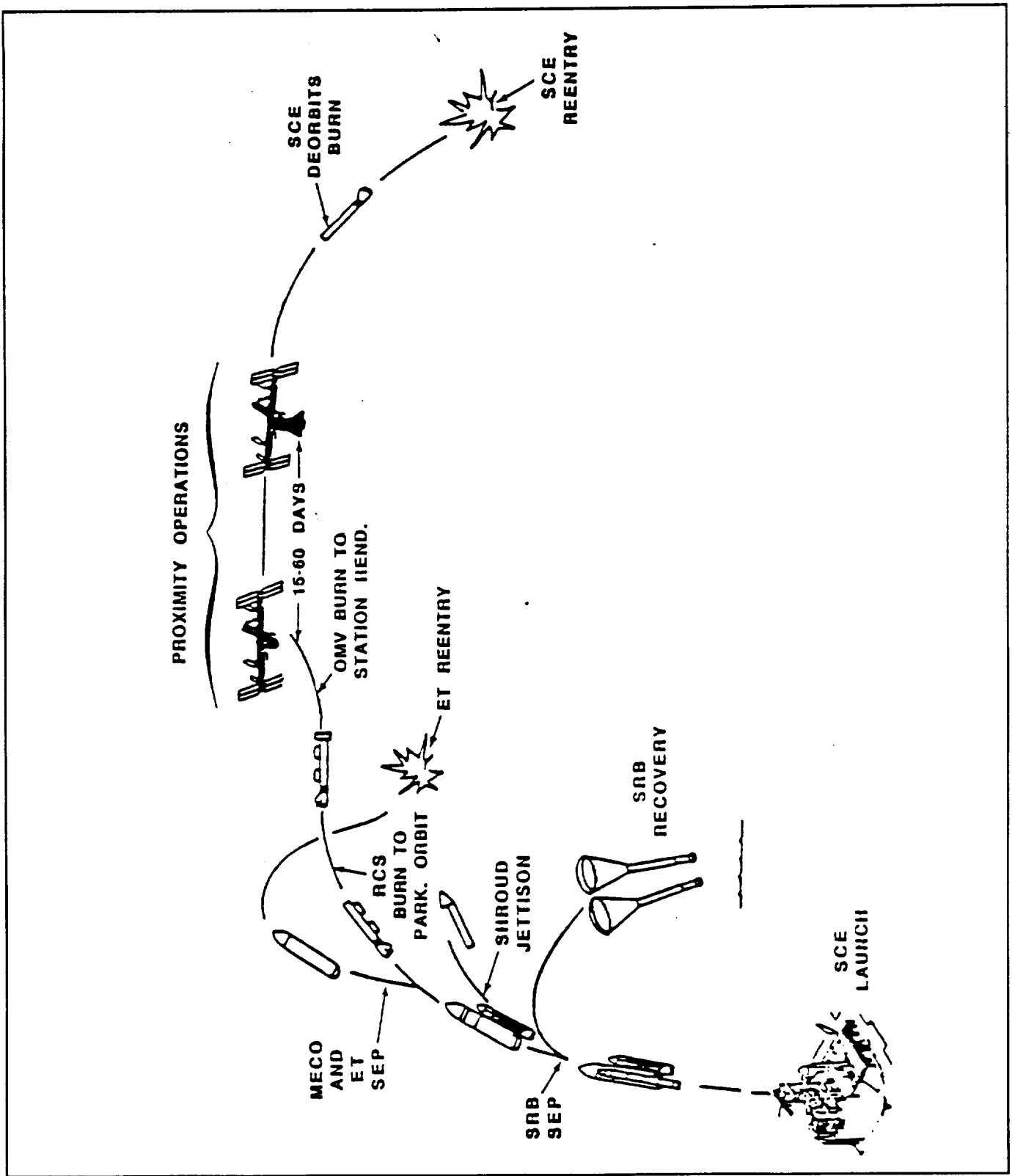
Figure 2.2.1-4. SCE Mission Profile

- AUTONOMOUS FLIGHT CONTROL TO ORBITAL INSERTION, CIRICULARIZATION AND DEORBIT
  - Simplex Shuttle-C Mission Control Center
  - Basic Shuttle-C Avionics for This Function
  - Precursor Mission Planning (Simplex), Payload Integration to Cargo Bay Shuttle-C

- ORBITAL DEPLOY MISSIONS (e.g., PLANETARY AND OTHER FREE FLYING SPACECRAFT
  - Payload developer responsible for operations from POCC after payload separation

- SPACE STATION MISSIONS
  - Precursor mission (Δ on orbit) planning done as part of OMV/SS activity
  - OMV/Space Station Control Center responsible for rendezvous, prox-ops, docking, Mission operations (e.g., Assembly) and deorbit from SS/OMV control center or multi-purpose control center
  - Very limited "kit on" shuttle-C delta avionics including batteries, etc.

Figure 2.2.1-5.   Shuttle-C Flight Operations

2.2.2   PHASE 2 (ALS CORE, ALS BOOSTER, SDV 2RS)

The Phase 2 IOC is set for August 1992. The Phase 2 GBT will be sized to support the ALS Core and Booster, SDV-2RS, and an upgraded Shuttle-C. Since the ALS Core and Booster closely fit the SDV-2RS functional requirements, they were chosen for the reference vehicles for the Phase 2 GBT. Figures 2.2.2-1 through 2.2.2-3 shows the ALS Core and Booster avionics systems and the associated vehicle processing requirements. Figure 2.2.2-4 associates the ALS Core throughput requirements with its design reference mission timeline.

1. MISSION MODELS - SHUTTLE-C, ALS, (GENERIC)
   - LAUNCH
   - ASCENT
   - ON ORBIT (STV) MANEUVER, RENDEZVOUS & DOCKING
   - ENTRY (CONTROLLED AND PRECISION)

2. SYSTEM TEST - SHUTTLE-C, ALS, STV (GENERIC)
   - G/NS
   - F/CS
   - F/CP
   - DAS
   - PC
   - S/SC

3. OUTSIDE RESOURCES
   - SSME LAB INTERFACE
   - ACTUATOR LAB

Figure 2.2.2-1.   Phase II Capabilities/Constraints

Figure 2.2.2-2. Avionics and Power System

ALS CORE

SUBSYSTEM (WITH HEALTH MONITORING)	WITH LIMITED EXPERT SYSTEMS			
	THRUPUT (MIPS)	TOTAL MEMORY (MBYTES)	I/O DATA RATE (MBPS)	I/O DEVICES (QUANTITY)
PROPULSION	3 (IMIPS/ENG)	0.288	0.375	819
FLUIDS	<0.1	<0.1	0.216	241
POWER	<0.1	<0.1	<0.01	100
# INSTRUMENTATION	<3	<0.002	0.256	1500
GN&C (ADAPTIVE)	4.063	0.988	0.153	600
SYSTEMS SOFTWARE	0.21	0.59	--	--
COMMUNICATIONS	<0.1	<0.1	<0.01	100
VEHICLE ELEMENT INTERFACE	<0.1	<0.1	0.072	262
TOTAL	10.47	2.06	1.09	3622
SHUTTLE COMPARISON	0.343	0.42	NA	~4000

INCLUDES SENSOR PROCESSING NOT COVERED UNDER THE OTHER SUBSYSTEMS.
NOTE: REDUNDANCY INCLUDED ONLY WHERE KNOWN (E.G., PROPULSION)

NOTE: THE PROCESSING REQUIREMENTS DO NOT INCLUDE ANY ALLOWANCE FOR MARGIN, OR FAILURE TOLERANCE. (EXCEPT FOR PROPULSION)

Figure 2.2.2-3. Vehicle Processing Requirements Processing Summary

ALS LRB

SUBSYSTEM (WITH HEALTH MONITORING)	WITH LIMITED EXPERT SYSTEMS			
	THRUPUT (MIPS)	TOTAL MEMORY (MBYTES)	I/O DATA RATE (MBPS)	I/O DEVICES (QUANTITY)
PROPULSION	7 (IMIPS/ENG)	0.672	0.875	1911
FLUIDS	--	--	0.216	241
POWER	--	--	<0.01	75
# INSTRUMENTATION	--	--	0.100	750
GN&C (ADAPTIVE)	--	--	0.153	300
SYSTEMS SOFTWARE	0.10	0.20	--	--
COMMUNICATIONS	--	--	--	--
VEHICLE ELEMENT INTERFACE	<0.1	<0.1	0.072	262
TOTAL	7.2	0.972	1.426	3539
SHUTTLE COMPARISON	0.343	0.42	NA	~4000

INCLUDES SENSOR INTERFACING NOT COVERED UNDER THE OTHER SUBSYSTEMS.
NOTE: REDUNDANCY INCLUDED ONLY WHERE KNOWN (E.G., PROPULSION)

NOTE: THE PROCESSING REQUIREMENTS DO NOT INCLUDE ANY ALLOWANCE FOR MARGIN, OR FAILURE TOLERANCE. (EXCEPT FOR PROPULSION)

Figure 2.2.2-4. Vehicle Processing Requirements Processing Summary

2.2.3   TARGET (FBB, FWFBB, PRCV)

The Phase 3 or Target configuration IOC has not been set, but if it is tied to the Fixed Wing Recoverable Booster (FWFBB), Fly Back Booster (FBB), and the Partially Reusable Cargo Vehicle (PRCV) programs, it should be in the 1994 to 1996 time frame.

Figure 2.2.3-1 outlines the Processing Requirements for the FBB while Figure 2.2.3-2 associates the throughput requirements with the FBB mission timeline. The FBB avionics system is designed to be fully autonomous from launch to landing and roll-out. The GBTs capability to support FWFBB and PRCV development must start long before the 1994-1996 Target IOC. The GBT functions, shown in Figure 2.2.3-3, must include FBB/PRCV related inputs in both Phase 1 and Phase 2. Typical of these inputs are:

(1)   Electromechanical Actuator applications in vehicle aero control and Thrust Vector Control systems;

(2)   Redundancy Management using Expert Systems and a distributed processing system; and

(3)   An autonomous, robust GN&C system capable of near all-weather launches and minimum tailoring of software mission to mission.

These technology driven requirements are discussed in the next section.

FULLY REUSABLE WINGED BOOSTER (FRWB)				
	WITH LIMITED EXPERT SYSTEMS			
SUBSYSTEM (WITH HEALTH MONITORING)	THRUPUT (MIPS)	TOTAL MEMORY (MBYTES)	I/O DATA RATE (MBPS)	I/O DEVICES (QUANTITY)
*PROPULSION	6 (IMIPS/ENG)	1.152	06	3264
FLUIDS	<0.1	<0.1	0.32	380
POWER	<0.1	<0.1	<0.01	180
# INSTRUMENTATION	<3	0.0048	0.320	4000
GN&C (ADAPTIVE)	5.199	1.264	0.394	1225
SYSTEMS SOFTWARE	0.24	0.79	--	--
COMMUNICATIONS	<0.1	<0.1	<0.01	120
VEHICLE ELEMENT INTERFACE	<0.1	<0.1	0.0256	5
TOTAL	14.64	3.42	1.67	9174
SHUTTLE COMPARISON	0.343	0.42	NA	~4000

* PROCESSING IS TIME SHARED BETWEEN BOOSTER ENGINES AND AIR BREATING ENGINES.
# INCLUDES SENSOR PROCESSING NOT COVERED UNDER OTHER SUBSYSTEMS.
NOTE: REDUNDANCY INCLUDED ONLY WHERE KNOWN (E.G., PROPULSION).

NOTE: THE PROCESSING REQUIREMENTS DO NOT INCLUDE ANY ALLOWANCE FOR MARGIN, OR FAILURE TOLERANCE (EXCEPT FOR PROPULSION).
NOTE: THE PROCESSING REQUIREMENTS DO NOT INCLUDE THE IMAGING SENSOR PECULIAR PROCESSING WHICH IS ASSUMED TO BE SELF CONTAINED.

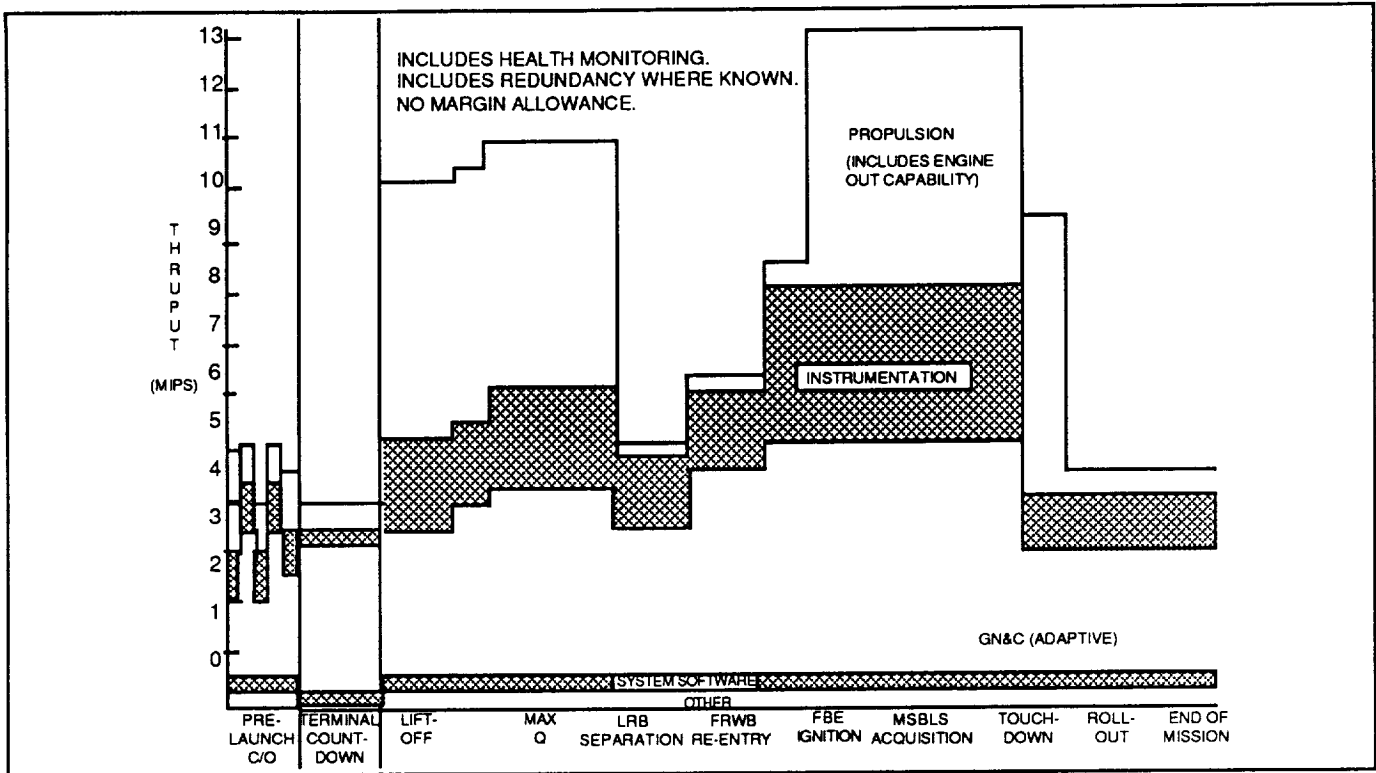**Figure 2.2.3-1.   Vehicle Processing Requirements Processing Summary**

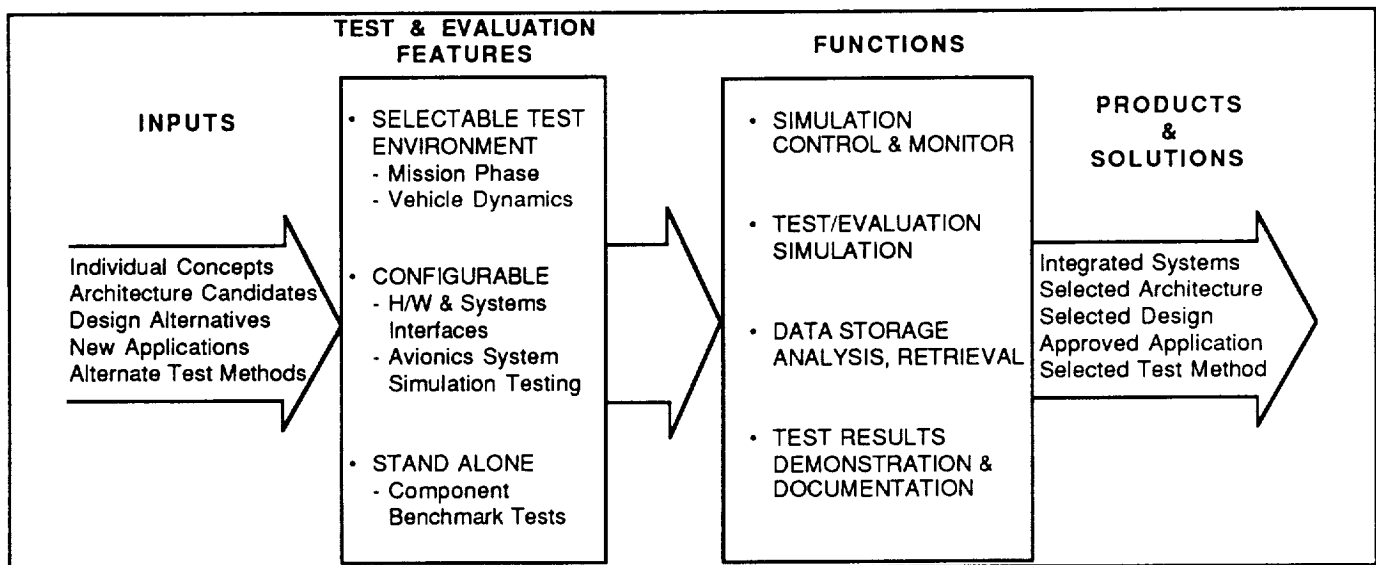**Figure 2.2.3-2.   FRWB Processing Timeline**

Figure 2.2.3-3.   GBT Functions

2.3   TECHNOLOGY DRIVEN REQUIREMENTS

Figure 2.3-1 lists some of the pacing technologies investigated during the initial stages of this study. Each was associated with their specific application on the HLCV era avionics systems and prioritized as to their role in achieving the design goals. The following paragraphs show their impact on the GBT design and at what stage of implementation they will be supported.

2.3.1 SYSTEM ARCHITECTURES/REDUNDANCY MANAGEMENT

One of the most fundamental drivers of the GBT processing/throughput requirements involves the basic vehicle architectures to be simulated and the operational environment in which they must be tested. The basic Phase 1 through the complex Target GBT configuration had to be sized to full-up, end-to-end, real-time vehicle system simulations. This translates into a throughput requirement for the lab of approximately 150 million instructions per second (MIPS) for the Phase 2 GBT. The processor assigned to model the system architecture had to be able to model a parallel, distributed, multi-string system; duplicate the redundancy management logic of that system and be able to monitor, control and provide external stimuli to the system under test. The FBB avionics system is fully autonomous and, therefore, includes Integrated Health Monitoring (IHM), a high precision launch to roll-out GN&C system that may incorporate a multi-spectral Image Processing System. Much of the traditional GSE functions will be performed by the FBB system. All these factors will drive the GBT throughput and parallel processing capacity well beyond the 150 MIPS of the Phase 2 lab. This mandates a main processing capacity which can be expanded incrementally without having to replace the original equipment.

```
•   GENERAL AVIONIC SUBSYSTEMS
    –   Processors & Architectures
    –   Integrated Health Monitoring
    –   Power System Conditioning & Management
    –   RF Instrumentation
    –   Pyrotechnics

•   GUIDANCE & NAVIGATION
    –   Adaptive Guidance, Navigation & Control
    –   Autonomous Navigation & Attitude Sensors

•   FLIGHT CONTROLS
    –   Actuators & Controllers

•   PROPULSION
    –   Embedded Controls & Monitoring
```

Figure 2.3-1.   Pacing Technologies

2.3.2 POWER DISTRIBUTION, CONDITIONING AND MANAGEMENT

The HLCV era vehicles are required to perform over a wide ranging series of missions that last from 90 minutes to several months. The reliability required of the supporting power systems plus the new demands of cost effectiveness have driven a re-examination of traditional solutions and a source for new designs. The increasing demand for power by electromechanical actuators and the new designs being utilized in their attendant power supplies have elevated this once stable design area into new activity. The GBT power extension will be able to evaluate alternate power sources (batteries, fuel cells and solar cells), power distribution system architectures, redundancy management schemes, and different methods of power conditioning and management.

2.3.3 ELECTRO MECHANICAL ACTUATORS

The clustered rocket engines of many of the HLCV vehicles have accelerated development of fast response high power (> 50 hp) electromechanical actuators. The HLCV GBT will support this effort in Phase 2. Development will be in the power supply design as well as that of the basic actuator.

The integration of actuator development and testing in the total vehicle development program involves several areas. The end-to-end testing would, in its highest fidelity mode, require the actuator under test to be dynamically loaded. This loading would be controlled in part by inputs from the missions environmental and vehicle dynamic models. The dynamic load cell and its attendant support equipment could represent a prohibitively high investment. Use of existing or dedicated actuator labs may prove the most cost effective method of providing this resource. A high data rate, broadband data link to the GBT could be used in closed loop testing. EMA power supply development could be accommodated in the GBT Power Systems extension.

2.3.4 ADAPTIVE GUIDANCE, NAVIGATION & CONTROL

HLCV traffic models force a more robust launch capability. Not only do vehicles have to be easy to process and launch, they must be strong enough and smart enough to handle less favorable environmental conditions. Supporting Adaptive Guidance, Navigation & Control would include everything from concept evaluation through sensor design testing. Primary impact of this technology support by the GBT would be in the area of software development, and attendant processor capacity and flexibility. Special software analysis tools may be required in the investigation of various load relief concepts, sensor applications and vehicle dynamic control modeling.

2.3.5 IMAGE PROCESSING

The application of image processing to HLCV functions seems particularly attractive in the areas of rendezvous & docking and approach & landing. The delays and subsequent risks involved in the remote docking techniques used in OMV can be potentially mitigated with a "smart" docking system. Such a system could be used on the STV or retrofitted on the OMV. Use of image processing to detect/identify the target, its range and orientation are well within current state-of-the-art capabilities. Application in the FBB approach & landing functions is another application to be investigated.

Impact to the GBT design would include software tools required for high fidelity 3D Target modeling and animation. Hardware requirements would include prototype sensors, TV camera, large, high resolution graphic monitor and an image processing workstation.

3.0   GROUND BASED TEST BED DESIGN

3.1   TARGET, GBT DESIGN

The GBT Target or Phase 3 design is designed to support the Fixed Wing Recoverable Booster, (FWRB), and the Partially Reusable Cargo Vehicle (PRCV) era vehicles. Early estimates place these projects in the 2000 to 2010 era. One should note that Shuttle-C and ALS share this pair of HLCV design concept vehicles. The avionics of both the FWRB or Fly Back Booster, (FBB), and the PRCV or Core will require little ground support both during prelaunch processing and mission operations. The development of this autonomous system will require innovative use of many emerging technologies ranging from distributed system architectures that link redundancy management with expert systems to launch to roll-out precision guidance systems that team multi-spectral image processing with inertial navigation and control. Simplified ground processing and the use of clustered rocket engines demand simpler engine controls and thrust vector control methods. All of these factors have contributed to the Target GBT configuration.

3.1.1 FUNCTIONAL DESCRIPTION

The GBT shall be broken up into a number of modules based on function: the GBT core and the special test extensions. The GBT core contains the hardware and software to support system development and integration of a complete Avionics suite. The GBT special test extensions contain specialized test equipment for testing new technologies in guidance and navigation , power systems, actuators, image processing sensors, fluids components and systems. These GBT extensions shall be linked to the core facility with a high speed communication network described in section 3.2.2.7.2.2. A diagram of the components and links of the core lab and the additional test facilities is shown in figure 3.1.1-1.

3.1.2 CORE CONFIGURATION

The core lab segment contains the programmable interfaces, processing power and analysis power to simulate and test a complete avionics suite for the vehicles specified in Section 2.2. The Core segment consists of a control processor, four graphic processors, a main simulation processor, input/output interface extensions, the instrumentation processing segment, mass storage and reproduction, internal lab interfaces, avionics test bed interfaces, and supporting software. The operation of the lab is best shown by the following examples.

An example of open loop testing of an avionics component in the core facility is described below and shown in Figure 3.1.2-1. The Avionics analog & discrete interfaces are connected to the I/O interface for switching. The I/O interface connects to the main simulation processor which computes the parameters to support the avionics input requirements for the hardline interfaces. The avionics MIL-STD-1553 interfaces are connected to the core facility vehicle bus. The vehicle bus connects to the main simulation processor and control processor. The main processor computes parameters to support avionics input requirements from vehicle bus interface   The control processor allows user manipulation and checkout of the avionics.
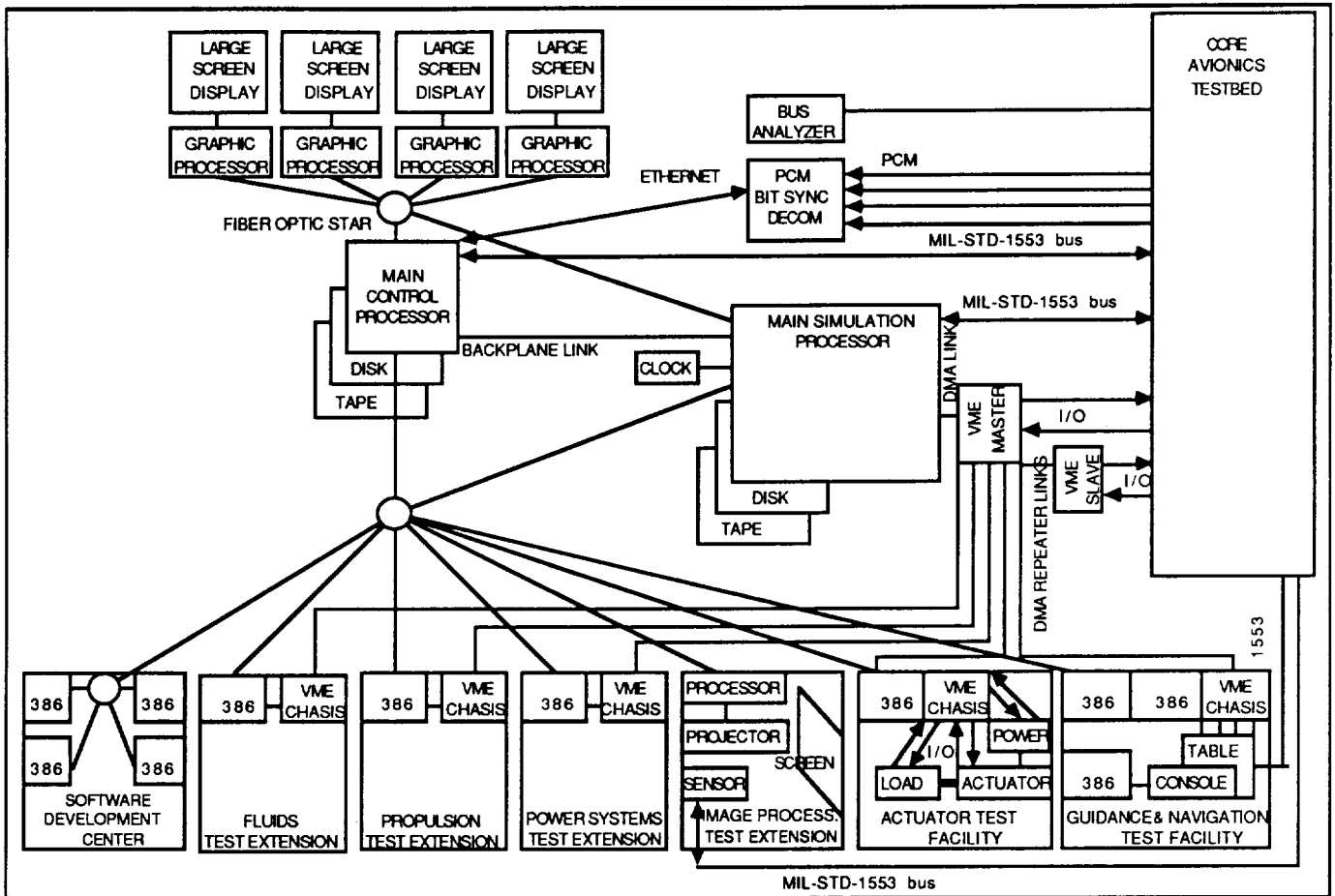
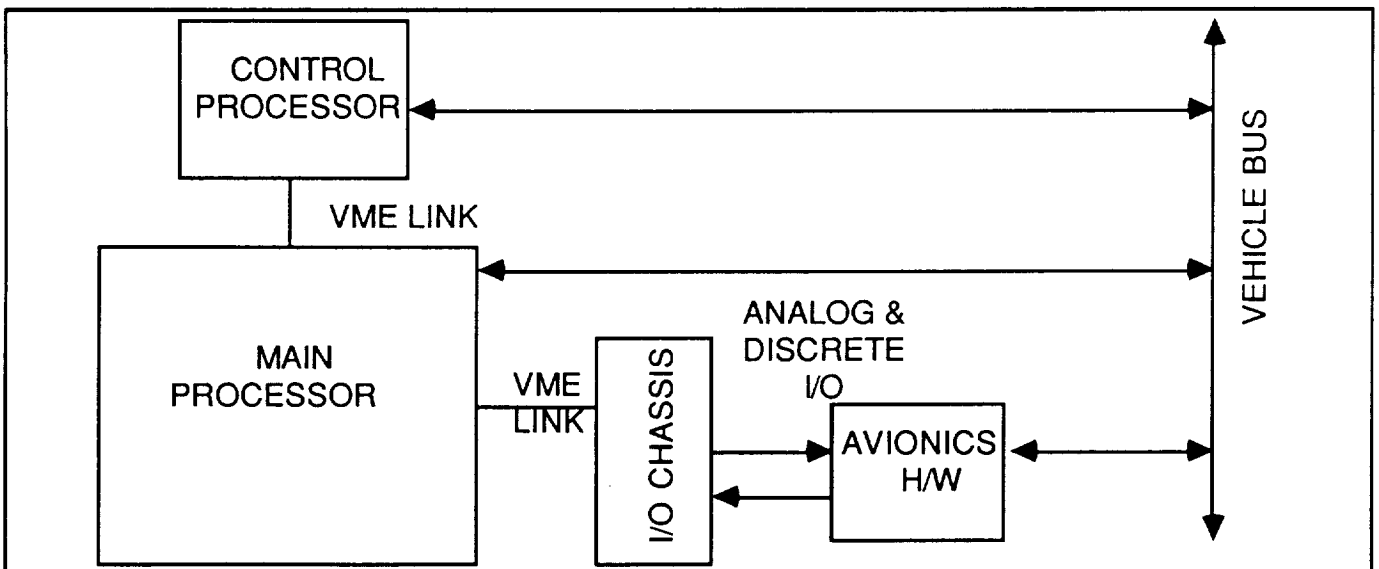**Figure 3.1.1-1.   Target Lab Functional Diagram**

Figure 3.1.2-1.   Open Loop Avionics Testing in Core Facility

An example of integrated closed loop testing of avionics in the core facility is described below and shown in figure 3.1.2-2. The avionics analog & discrete interfaces are connected to the I/O interface for switching. The I/O interface connects to additional hardware in the testbed and the main simulation processor. The main processor computes the hardline interface values not supplied by the hardware in the testbed. The avionics MIL-STD-1553 interfaces are connected to the core facility vehicle bus. The vehicle bus connects to additional hardware in the testbed, the main simulation processor, and the control processor. The main processor computes the vehicle bus parameters not supplied by the avionics in testbed. The control processor allows user manipulation and checkout of the avionics.
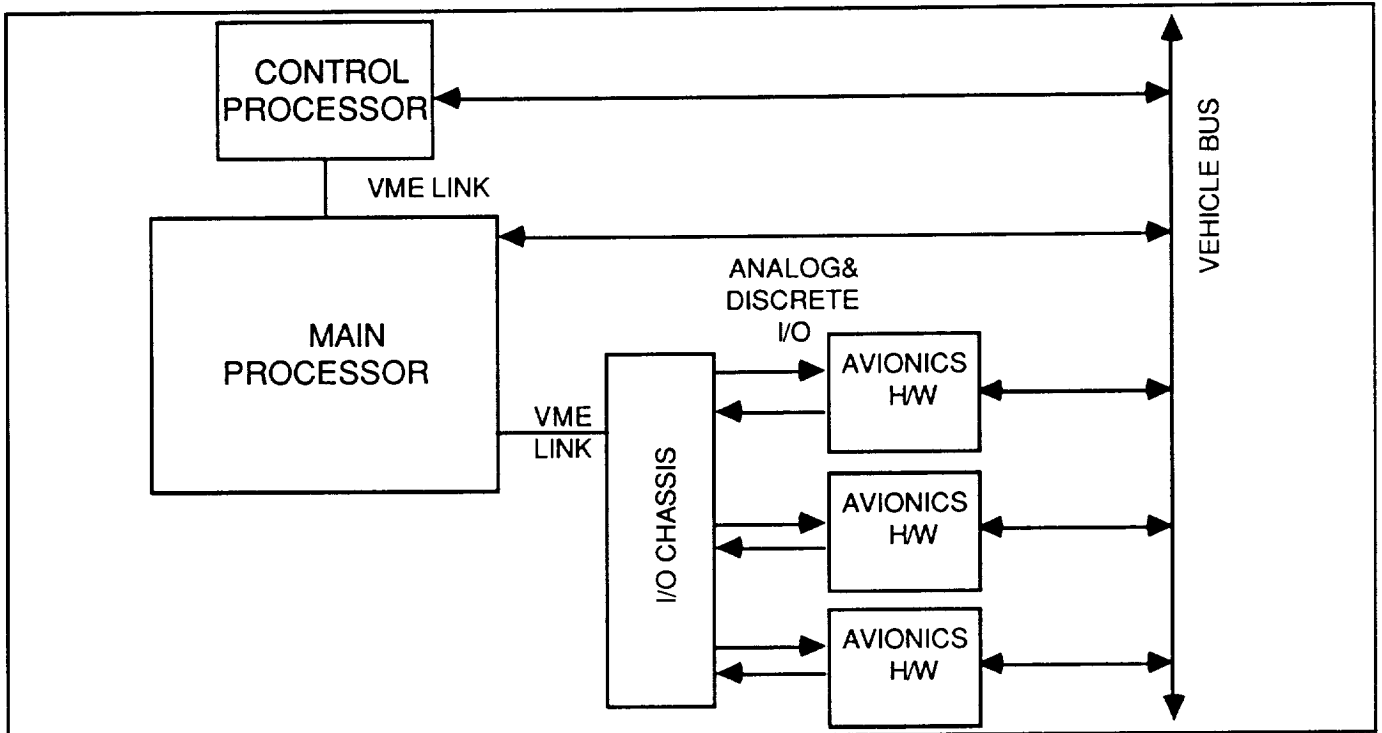
Figure 3.1.2-2.   Closed Loop Avionics Testing In Core Facility

An example of integrated testing of avionics components in the core facility testbed and a special test facility is described below and shown in Figure 3.1.2-3. The avionics analog & discrete interfaces are connected to the I/O interface in the special test facility for switching. The facility I/O interface connects to the special test facility processor and the core facility I/O interface. The core facility I/O interface links to additional hardware in the core testbed or to the main simulation processor to support the avionics requirements. The facility processor computes hardline interface values not supplied by hardware in the testbed or the main processor. The avionics MIL-STD-1553 interfaces are connected to the core facility vehicle bus which connects to the facility processor, the main simulation processor, additional hardware in the testbed and the control processor. The main simulation processor or the facility processor computes the parameters to support the avionics input requirements from the vehicle bus interface. The control processor and facility processor allow user manipulation and checkout of the avionics.
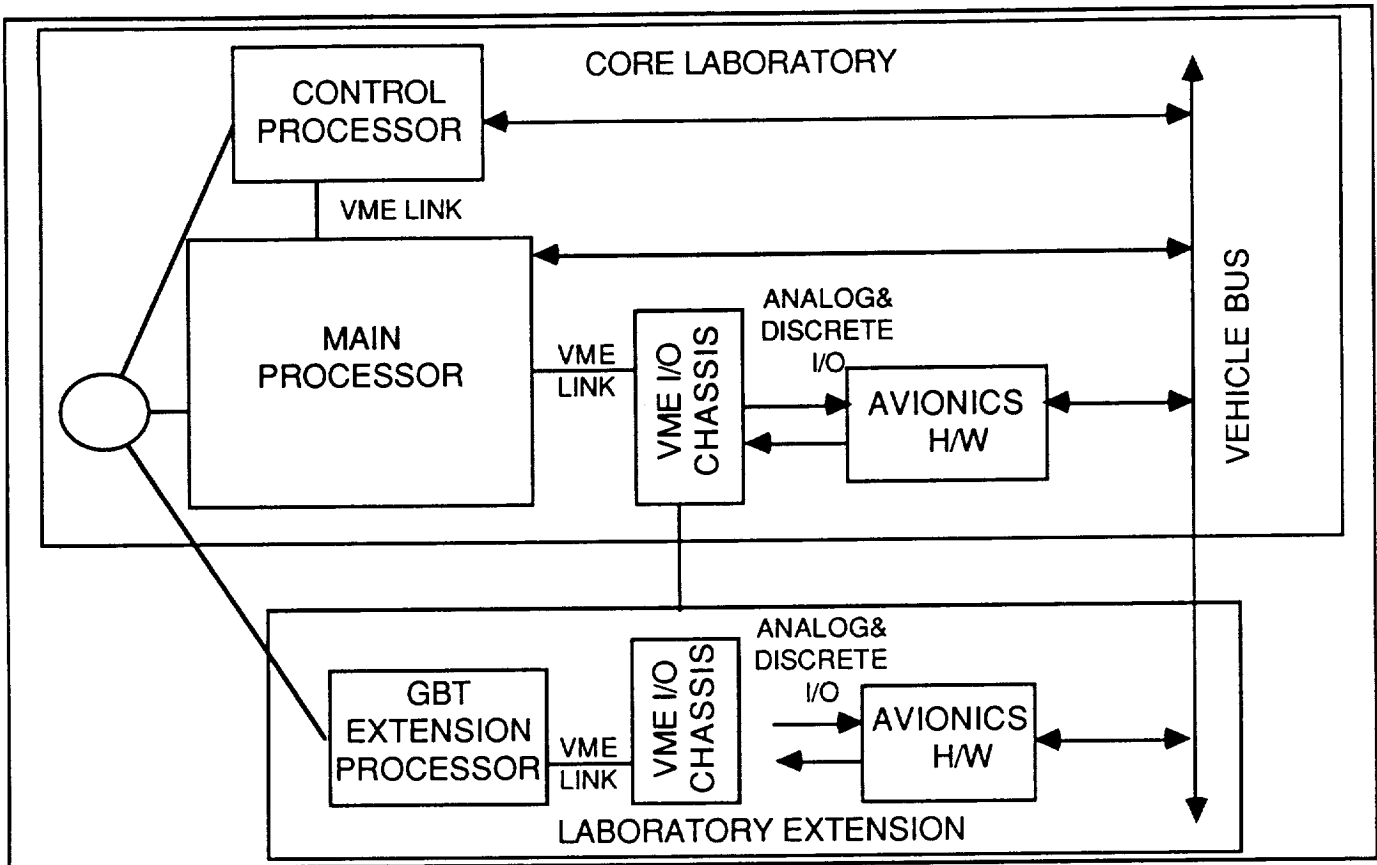
Figure 3.1.2-3. Integrated Testing with Extension Facility

An example of the onboard instrumentation testing in the core facility is described below and shown in Figure 3.1.2-4. Connect the PCM output of the Flight Instrumentation hardware to the instrumentation processing station. The instrumentation processing station processes the data and sends it to the control processor. The analog & discrete interfaces of Instrumentation hardware are connected to the I/O interface for switching. The I/O interface connects to additional hardware in the testbed and the main simulation processor. The main simulation processor computes the hardline interface values not supplied by the hardware in the testbed. MIL-STD-1553 interfaces of instrumentation hardware are connected to the core facility vehicle bus, which connects to the main simulation processor, additional hardware in the testbed and the control processor. The main simulation processor computes the vehicle bus parameters not provided by additional hardware to support the instrumentation hardware. The control processor allows user manipulation and checkout of the hardware.

An example of testing avionics components with orbiter bus interface in the core facility is described below and in Figure 3.1.2-5. The orbiter bus interfaces are connected to a custom-built VME to orbiter bus interface in the main simulation processor I/O slot. The main simulation processor computes the parameters necessary to support the avionics. The avionics analog & discrete interfaces are connected to the I/O interface for switching. The I/O interface connects to additional hardware in the testbed and the main simulation processor. The main simulation processor computes the hardline interface values that are not supplied by the hardware in the testbed.
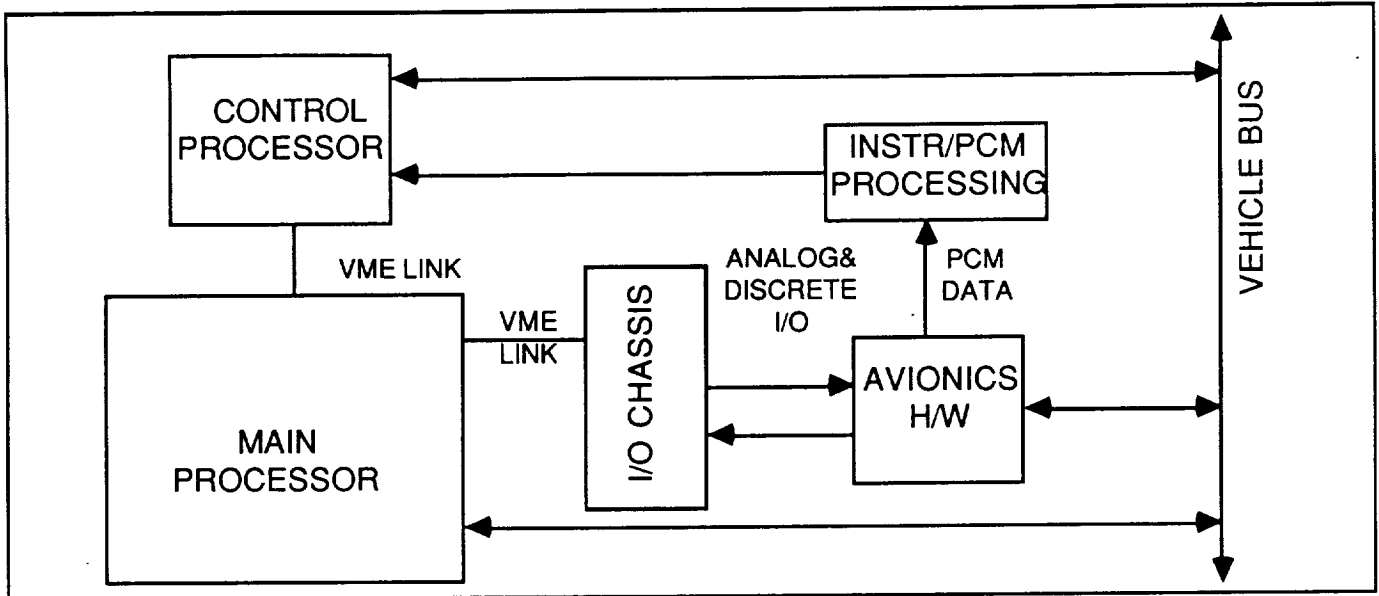
Figure 3.1.2-4.   Instrumentation Hardware Testing
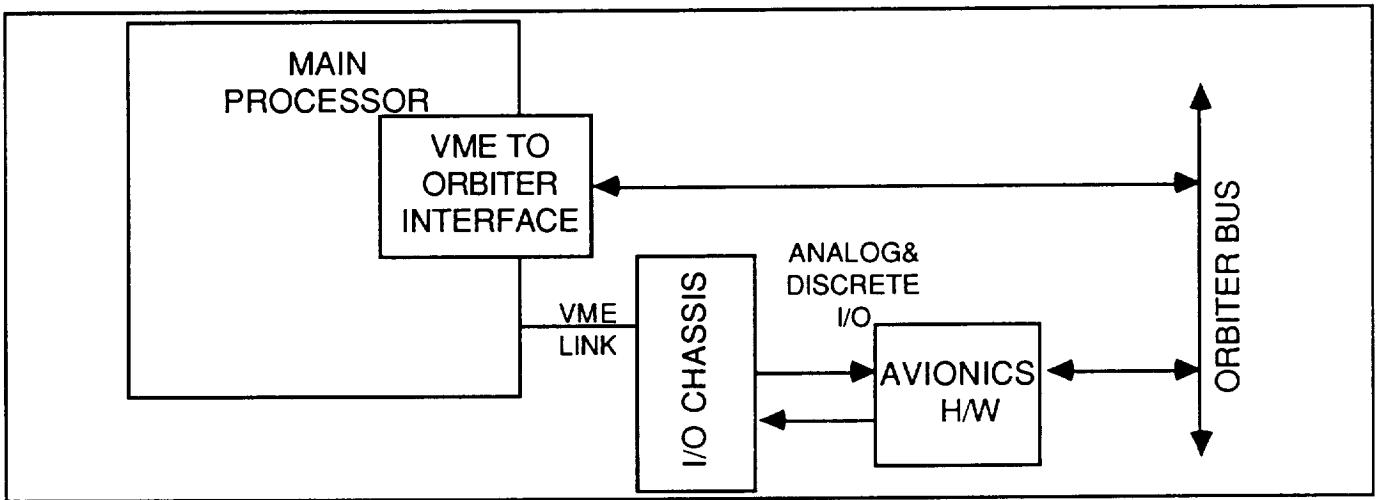
Figure 3.1.2-5.   Component Testing with Orbiter Bus in Core Facility

3.1.2.1   MAIN SIMULATION PROCESSOR

The Main Simulation Processor (MSP) handles the simulation of the environment and vehicle dynamics for the main testbed and the specific test facilities when integrated. The MSP also hosts the software for the avionics architecture design and interfaces. A diagram of the main simulation processor and its interfaces is shown in Figure 3.1.2.1-1.
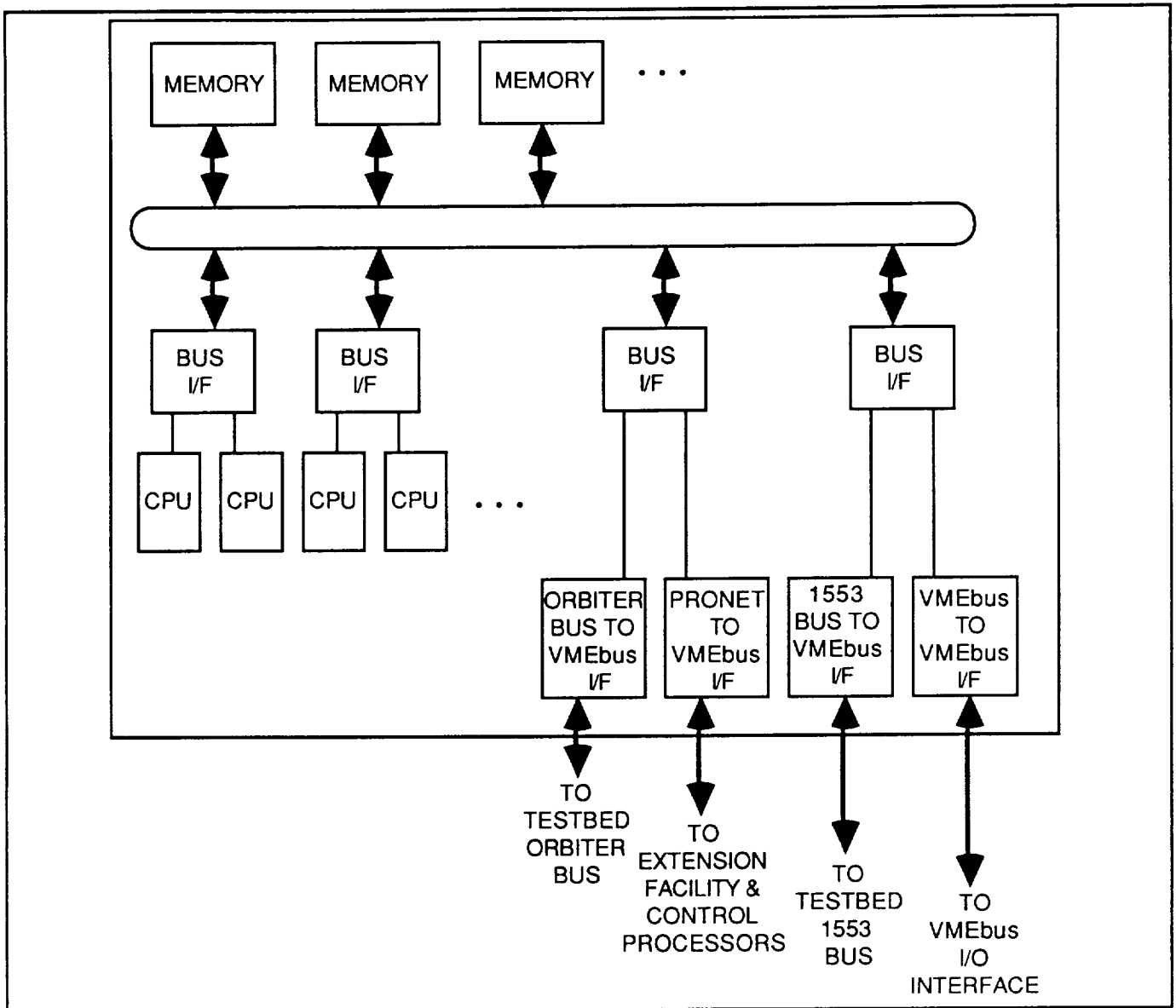
Figure 3.1.2.1-1.   Main Simulation Processor

3.1.2.1.1   Characteristics. The MSP shall be a scaleable multi or parallel processor that has a real time operating system, and global or shared memory support.

3.1.2.1.1.1   General

3.1.2.1.1.1.1 Operating system. The OS 32 or UNIX real time operating system shall be used.

3.1.2.1.1.1.2 Processor Backplane. The MSP shall have a VME backplane.

3.1.2.1.1.1.3 Memory. 32 Mbytes minimum.

3.1.2.1.1.1.4 Input/Output ports. Minimum 4 ports into the VME backplane.

3.1.2.1.1.1.5 Data Storage. The MSP processor shall have two 256 Mbyte or greater removable disks, one 6200/3200/1600 BPI tape, and one fixed 650 MByte or greater disk drive as specified in Section 3.2.2.6.

3.1.2.1.1.2   Performance

3.1.2.1.1.2.1 Integer Instructions per second. 75 MIPS for phase 1 configuration, 150 MIPS minimum for target configuration.

3.1.2.1.1.2.2 Floating point instructions per second. 75 MFLOPS for phase 1 configuration, 150 MLOPS minimum for target configuration.

3.1.2.2   CONTROL PROCESSOR

The Control Processor shall function as the lab configuration controller, the avionics controller and preprocessor for the monitors. Figure 3.1.2.2-1 is a diagram of the control processor and the interfaces to other components.
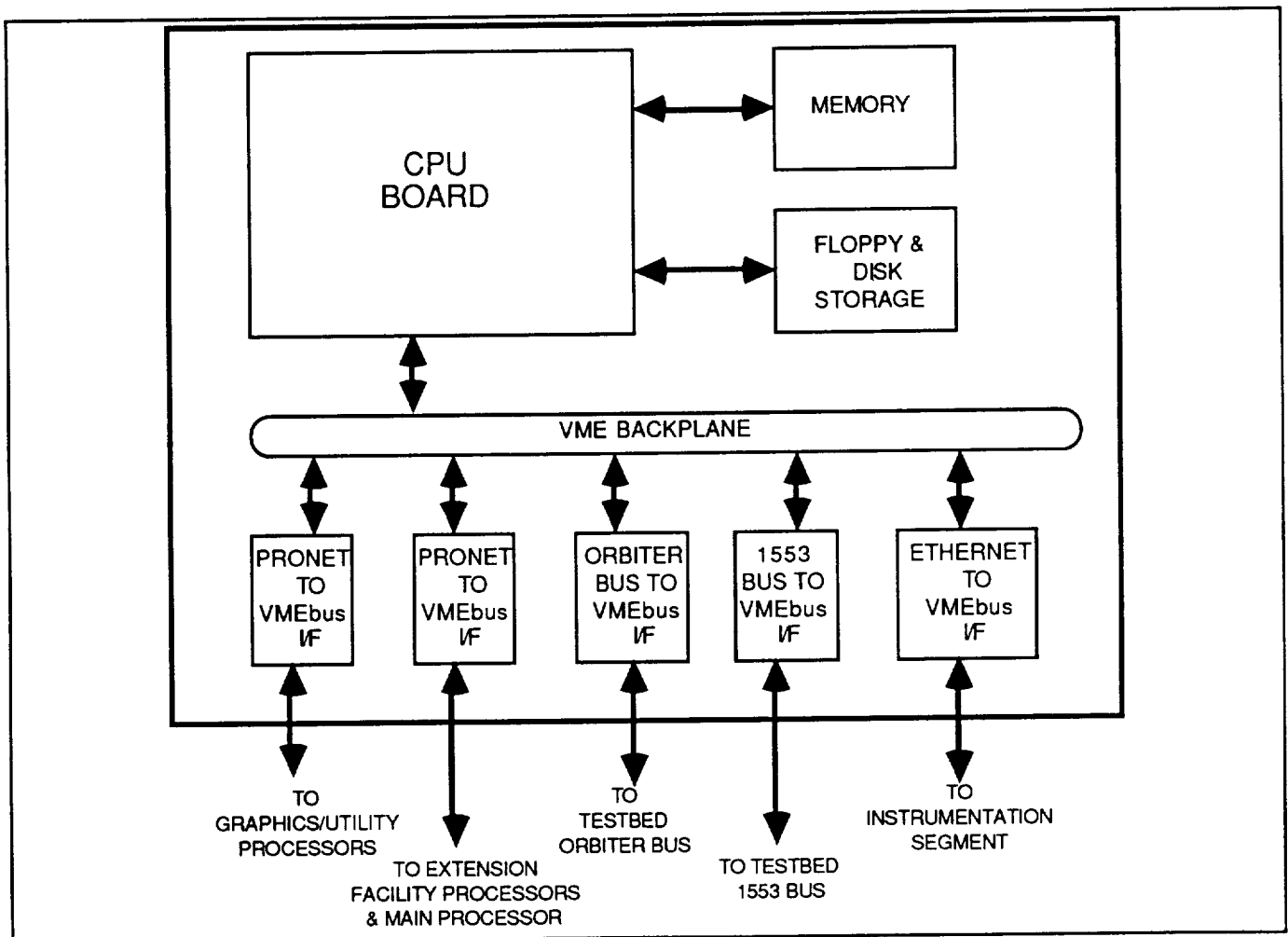
Figure 3.1.2.2-1.   Control Processor

3.1.2.2.1   Characteristics

3.1.2.2.1.1   General

3.1.2.2.1.1.1 Operating system. The operating system must be Real time with multi-tasking capabilities.

3.1.2.2.1.1.2 Processor backplane. In order to be fully compatible with the main simulation processor the Control Processor shall have a 24 MBPS VME backplane.

3.1.2.2.1.1.3 Memory. 10 Mbytes minimum.

3.1.2.2.1.1.4 Input/Output ports. Minimum 4 ports into the VME backplane.

3.1.2.2.1.1.5 Data Storage. The controller processor shall have two disk controllers and two 300 Mbyte removable disk drives.

3.1.2.2.1.2   Performance

3.1.2.2.1.2.1 Integer Instructions per second. 10 MIPS for phase 1 and target configuration.

3.1.2.2.1.2.2 Floating point instructions per second. 10 MFLOPS for phase 1 and target configuration.

3.1.2.3   INPUT/OUTPUT INTERFACE

The Input/Output interface handles the interfaces between simulation and avionics hardware for the analog and discrete signals. The target I/O interface consists of three master chassis with host processor links, six slave chassis with repeater links, and the input and output cards necessary to integrate the I/O interface with the various avionics components. The phase 1 I/O interface consists of one master chassis with host processor link, one slave chassis with repeater link, and the various I/O and processor cards. The VME Input/Output interface is shown in figure 3.1.2.3-1.

3.1.2.3.1   Characteristics

3.1.2.3.1.1   General

3.1.2.3.1.1.1 Operating system. The I/O interface shall have an intelligent I/O operating system for easy configuration and manipulation.

3.1.2.3.1.1.2 Input/Output ports. 15 useable slots per master chassis and 19 useable slots per slave chassis. 159 total useable I/O slots.
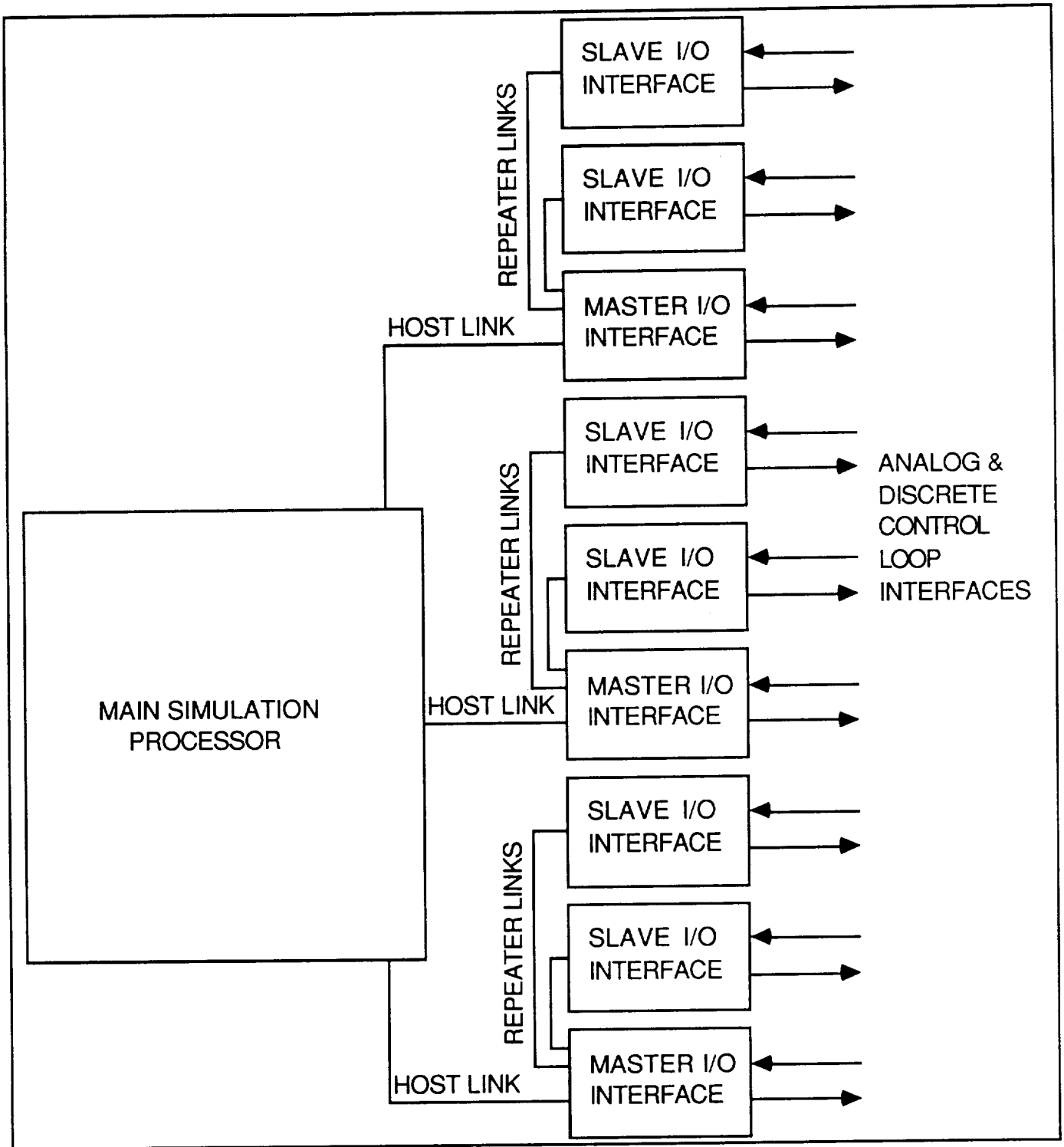
Figure 3.1.2.3-1.   Input/Output Interface

3.1.2.3.1.1.3 Chassis backplane. The I/O interface chassis consist of three buses; the VMEbus, the VSB-VME, and the VMSbus. The system is shown in figure 3.1.2.3.1.1.3-1.

3.1.2.3.1.1.3.1   VMEbus. The VMEbus is the system bus. It supports processor architectures up to 32 bits wide for address and data. the asynchronous, non-multiplexed bus

protocol allows data transfer up to 40 Mbyte/sec in a 4 GByte linear address space. for complex applications the VMEbus is extended by the VSB and the VMSbus.

3.1.2.3.1.1.3.2   VSB-VME. The VSB-VME is the subsystem bus. It forms a 32 bit wide local bus extension to implement fast local systems, especially local memory extensions, which are connected via the VMEbus.

3.1.2.3.1.1.3.3   VMS. The VMS is the serial sub-bus. It allows an additional serial connection between the VME modules. The main uses of the VMSbus are the exchange of short messages,(e.g. interrupt vectors, semaphores),connection of widely separated subsystems as well as construction of redundant systems.
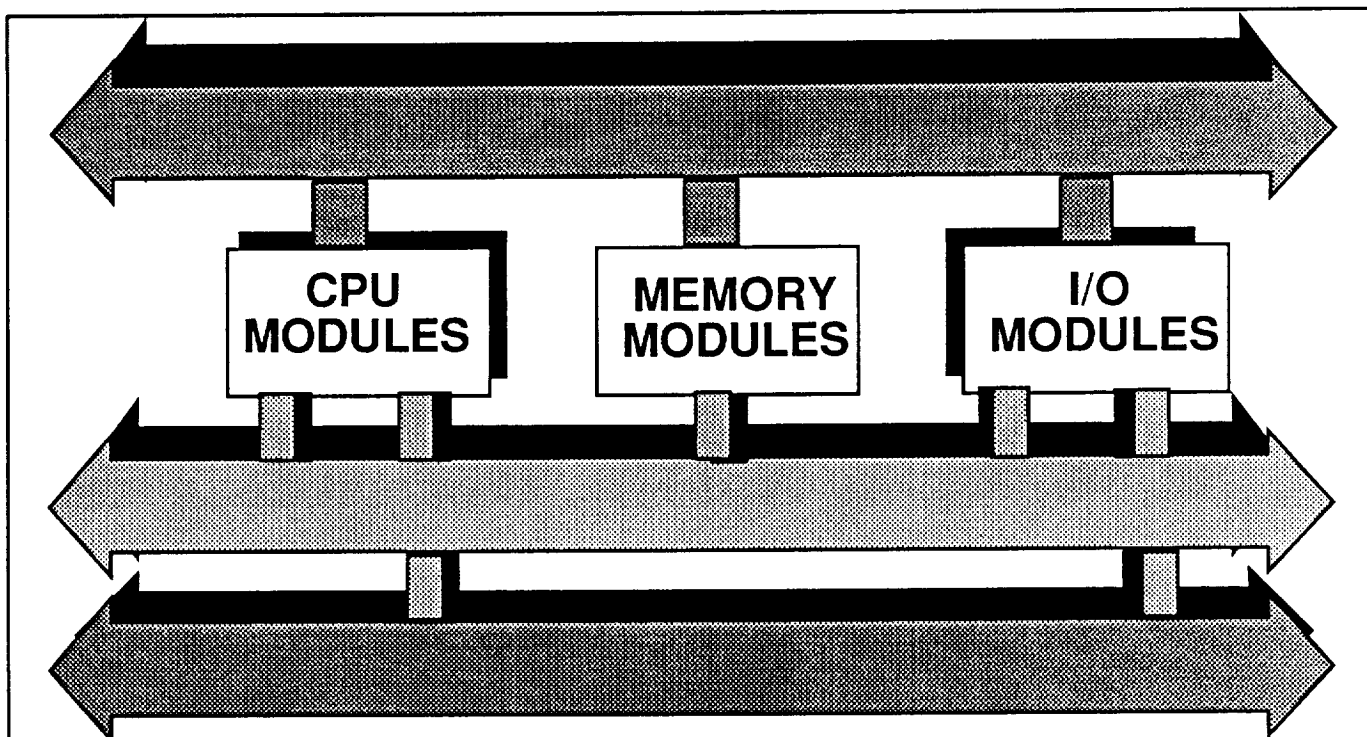
Figure 3.1.2.3.1.1.3-1 The VMEbus System

3.1.2.3.1.1.4 Processor cards.

3.1.2.3.1.1.4.1   CPU. Motorola MC68030

3.1.2.3.1.1.4.2   Co-processor. Motorola MC68882

3.1.2.3.1.1.4.3   Memory. 4MByte DRAM
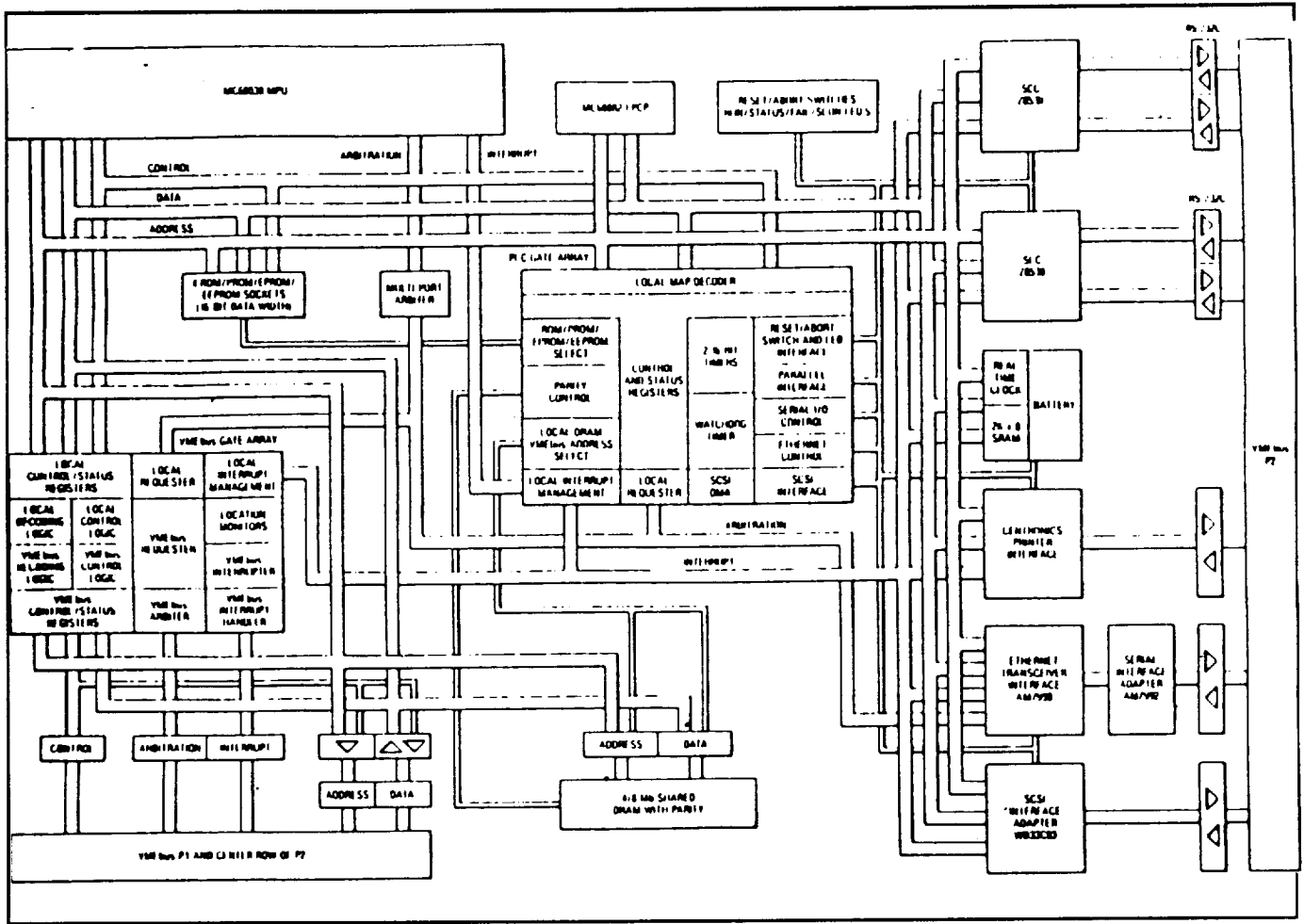
Figure 3.1.2.3.1.1.4-1 Processor Card Block Diagram

3.1.2.3.1.1.4.4   Performance: 25 MHz operation, 80ns DRAM

3.1.2.3.1.1.4.4.1   Timing:

Read VMEbus to DRAM: 13 cycles, 50ns

Write DRAM to VMEbus: 11 cycles, 420ns

MPU to DRAM read: 4-5 cycles

MPU to DRAM write: 4-5 cycles

3.1.2.3.1.1.4.5   Physical connection: Double high, double wide Eurocard which is fastened via mounting panel to card cage.

3.1.2.3.1.1.5 Analog to Digital Conversion Cards.

The phase 1 GBT shall contain 3 I/O cards that meet or exceed the following specifications. The target configuration shall contain 51 such cards to support the 1632 analog or discrete control loop signals.

3.1.2.3.1.1.5.1   Functional Characteristics:

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3.1.2.3.1.1.5.1.1   Compatibility: The Analog-to Digital converter board shall be a standard, double high, printed circuit board which is compatible with the VMEbus.

3.1.2.3.1.1.5.1.2   Data Conversion: Conversion shall be initiated under program control or upon receipt of an externally generated trigger pulse. Mode selection control shall be available to enable or disable the external trigger feature. A channel can be selected and conversion can be initiated by writing a single word.

3.1.2.3.1.1.5.1.3   Test Mode: The board shall contain internal precision voltages which can be used for fault detection and isolation.

3.1.2.3.1.1.5.1.4   Channels: The interface board shall contain 32 single ended input channels or sixteen differential input channels from the front panel.

3.1.2.3.1.1.5.2   Electrical Specifications:

3.1.2.3.1.1.5.2.1   Resolution: The interface board shall have a resolution of 12 bits minimum.

3.1.2.3.1.1.5.2.2   Conversion Time: Conversion shall occur in less than 2μsec.

3.1.2.3.1.1.5.2.3   Analog acquisition time: Software selectable;9μsec thru 6μsec.

3.1.2.3.1.1.5.2.4   Monotonicity: Monotonic over full operation temperature range.

3.1.2.3.1.1.5.2.5   Accuracy: 0.04% of (full scale range)**2±2mV with manual calibration. 0.03% of (full scale range) **2 ± 80μV ±.5 least significant bit over the full operating range with automatic calibration.

3.1.2.3.1.1.5.3   Physical specifications: Standard VME double-width Eurocard board (160mm X 233.5mm)

3.1.2.3.1.1.6 Digital to Analog Conversion Cards.

The phase 1 GBT shall contain 6 I/O cards that meet or exceed the following specifications. The target configuration shall contain 102 such cards to support the 1632 analog or discrete control loop signals.

3.1.2.3.1.1.6.1   Functional Characteristics:

3.1.2.3.1.1.6.1.1   Compatibility: The Digital-to-Analog converter board shall be a standard, double high, printed circuit board which is compatible with the VMEbus.

3.1.2.3.1.1.6.1.2   Data transfer:

3.1.2.3.1.1.6.1.3   Test Mode:

3.1.2.3.1.1.6.1.4   Channels: The interface board shall contain sixteen analog output channels.

3.1.2.3.1.1.6.2   Electrical specifications:

3.1.2.3.1.1.6.2.1   Resolution: The interface board shall have a resolution of 12 bits minimum.

3.1.2.3.1.1.6.2.2   Conversion Time: Conversion shall occur in less than 8μsec.

3.1.2.3.1.1.6.2.3   Monotonicity: Monotonic over full operation temperature range.

3.1.2.3.1.1.6.2.4   Accuracy:

Gain: 0.05% of (full scale range)**2

Offset: 0.025% of (full scale range)

Linearity error: ± .25 least significant bit

Differential linearity error: ± .5 least significant bit

3.1.2.3.1.1.5.3   Physical specifications: Standard VME double-width Eurocard board (160mm X 233.5mm).

3.1.2.4   DATA STORAGE AND REPRODUCTION

The GBT shall contain one high capacity non removable hard disk drive, two removable disk drives, one streaming tape drive, and one laser printer.

3.1.2.4.1   Fixed Hard Disk. The high capacity fixed hard disk drive handles the general system software and data storage needs for the lab.

3.1.2.4.1.1   General Characteristics

3.1.2.4.1.1.1   Storage Capacity. 650 MByte minimum

3.1.2.4.1.2   Performance

3.1.2.4.1.2.1   Throughput. 30 MByte/sec

3.1.2.4.1.2.2   Seek time. 30 MByte/sec

3.1.2.4.2   Removable disk drives. In order to handle the data storage requirement for long duration tests and test that require large amount of data, the GBT shall contain two removable disk drives. The disks can be switched from one to the other when one is full to provide a virtually unlimited storage capability. The selection of the removable disk drives should not preclude the use of optical or Winchester disk drives that meet the storage criteria.

3.1.2.4.2.1   General characteristics

3.1.2.4.2.1.1   Storage capacity. Minimal 256 MByte storage capacity

3.1.2.4.2.2   Performance characteristics

3.1.2.4.2.2.1   Throughput

3.1.2.4.2.2.2   Seek time

3.1.2.4.3   Streaming Tape. The streaming tape drive handles the transfer of software and data to and from other labs. Additionally, the streaming tape provides a means for low cost data storage.

3.1.2.4.3.1   General characteristics

3.1.2.4.3.1.1   Recording media. 0.5" x 7, 8.5 or 10.5" open reel mag tape.

3.1.2.4.3.1.2 <u>Tape velocity</u>. 75 IPS streaming

3.1.2.4.3.1.3 <u>Capacity</u>. Minimum 40 MByte per reel for PE or 1600 bpi recording, minimum 140 MByte per reel for group coded recording (GCR) 6250 bpi.

3.1.2.4.3.2 <u>Performance characteristics</u>

3.1.2.4.3.2.1 <u>Transfer Rate</u>. Minimum 120 KByte/sec sustained transfer rate for phase encoded, minimum 469 Kbyte/sec sustained transfer rate for group coded recording.

3.1.2.4.4   <u>Laser Printer</u>. The HP LaserJet or equivalent printer handles the hard copy needs of the lab.

3.1.2.4.4.1   <u>General Characteristics</u>

3.1.2.4.4.1.1 <u>Resolution</u>. The printer shall have a 300 dot/inch resolution minimum.

3.1.2.5   GBT INTERFACES

The GBT shall contain all buses/networks to fully integrate the system internally, and have the capability to interface with complete avionics assemblies or any component or combination of components for the vehicles specified in section 2.2.

3.1.2.5.1   <u>Avionics Testbed Interface Requirements</u>

The GBT shall have the capability to support power requirements, analog and discrete interface requirements, instrumentation bus interface requirements, and any additional interfaces for the vehicles specified in section 2.2. Figure 3.1.2.5.1-1 shows a diagram of the Avionics test bed interfaces.

3.1.2.5.1.1   <u>Analog and discrete control loop interfaces</u>. The GBT shall have the capability to support all analog and discrete signals required for a complete vehicle or any component thereof.

3.1.2.5.1.1.1 <u>Core laboratory Analog/Discrete interfaces</u>. The core facility shall contain a number of VMEbus chassis as specified in section 3.1.2.3 to support 1632 analog or discrete inputs and 1632 analog or discrete outputs.

3.1.2.5.1.1.2 <u>G&N extension Analog/Discrete interfaces</u>. The Guidance & Navigation extension shall contain a VMEbus chassis as specified in section 3.1.3.2 to support 160 analog or discrete inputs and 160 analog or discrete outputs.

3.1.2.5.1.2   <u>Avionics Buses</u>. The GBT shall have the MIL-STD-1553 bus interfaces to provide the capability to integrate, analyze and simulate avionics components that use this bus.

3.1.2.5.1.2.1 <u>Interface the Central Control Processor</u>. The GBT shall contain one MIL-STD-1553 to VMEbus interface card with software and 30' twisted shielded pair cable to interface the main control processor and the avionics bus.

3.1.2.5.1.2.2 <u>Interface the Main simulation processor</u>. The GBT shall contain one MIL-STD-1553 to VMEbus interface card with software and 30' twisted shielded pair cable to interface the main simulation processor and the avionics bus.

3.1.2.5.1.2.3 Interface the G&N extension. The GBT shall contain one MIL-STD-1553 to PC interface card with software and 15' twisted shielded pair cable to interface the G&N processor and the inertial unit under test.

3.1.2.5.1.2.4 Interface core and G&N extension. The GBT shall contain one 100' twisted shielded pair cable to link the core lab to the G&N extension.

3.1.2.5.1.2.5 MIL-STD-1553 to VMEbus interface card.

3.1.2.5.1.2.5.1   Operation Modes. The bus interface unit shall be capable of operating as a bus controller, a remote terminal or a bus monitor. The mode of operation shall be under the control of the system software. When operating as a bus controller, the interface unit shall be responsible for sending data bus commands, participating in data transfers, receiving status responses, and monitoring system status. When operating as a remote terminal, the interface unit shall be operated in response to valid commands from the bus controller. When operating as a bus monitor, the interface unit shall receive bus traffic and extract selected information.

3.1.2.5.1.2.5.2   Memory buffering. The onboard memory shall be double buffered to prevent partially updated data from being read by subsystem or transmitted to the 1553 bus.

3.1.2.5.1.2.5.3   Self Test. The bus interface shall perform test loops to insure its operational state. When operating as a bus controller, the last word transmitted shall be received back and compared for accuracy. When operating as a bus controller or remote terminal, the the last word transmitted shall be decoded and compared. A bus controller will generate an error interrupt and a remote terminal will set a terminal bit flag if an error is detected.

3.1.2.5.1.2.5.4   Mode Codes. The bus interface shall support the following MIL-STD-1553 mode codes.

    00000 Dynamic bus control
    00001 Synchronize
    00010 Transmit status word
    00100 Transmitter shut down
    00101 Override transmitter shutdown
    01000 Reset remote terminal
    10000 Transmit vector word from memory
    10001 Synchronize from memory
    10010 Transmit last command from protocol
    00110 Inhibit terminal flag
    00111 Override inhibit terminal flag
    00011 Initiate self test

3.1.2.5.1.2.5.5   VMEbus command registers. The bus interface shall contain command registers to read and write commands and status words

3.1.2.5.1.2.5.6 Bus timing. The main timing for the bus interface unit is a 6 MHz clock. Typical bus interface timing is shown in figure 3.1.2.5.1.2.5-1. Typical remote terminal and bus controller timing diagrams are shown in figures 3.1.2.5.1.2.5-2 and 3.1.2.5.1.2.5-3.
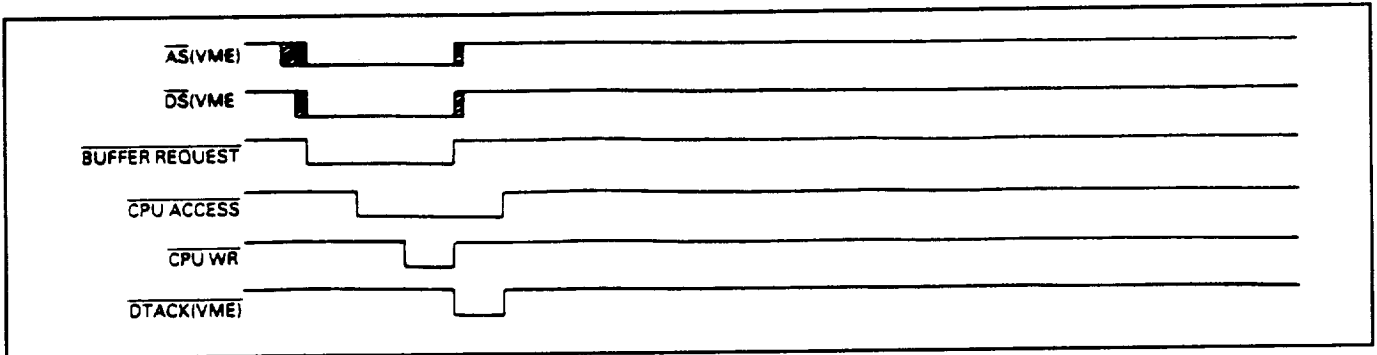
Figure 3.1.2.5.1.2.5-1.   Typical Bus Interface Timing
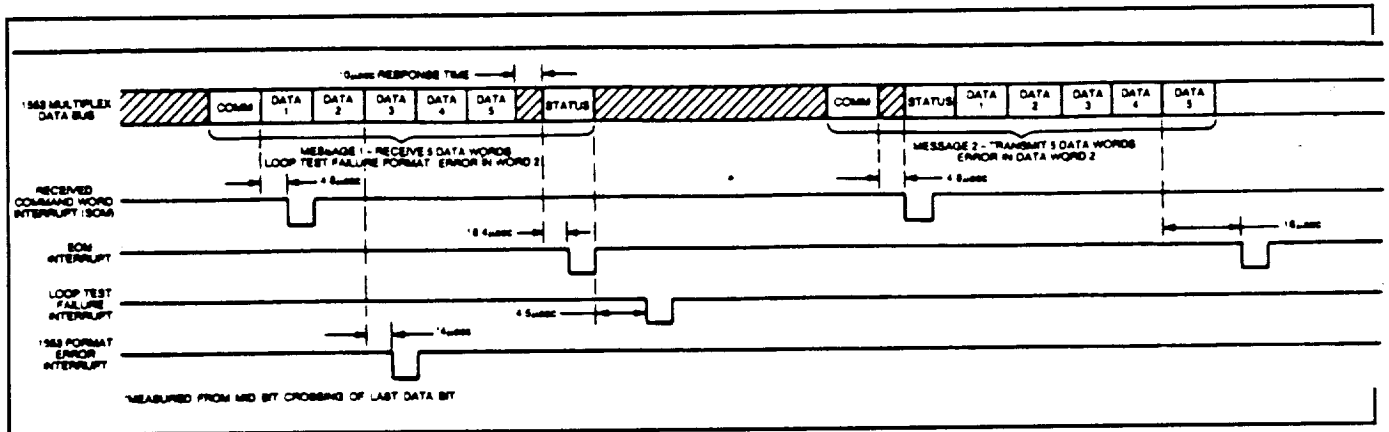
Figure 3.1.2.5.1.2.5-2   Typical Remote Terminal Interrupt Timing
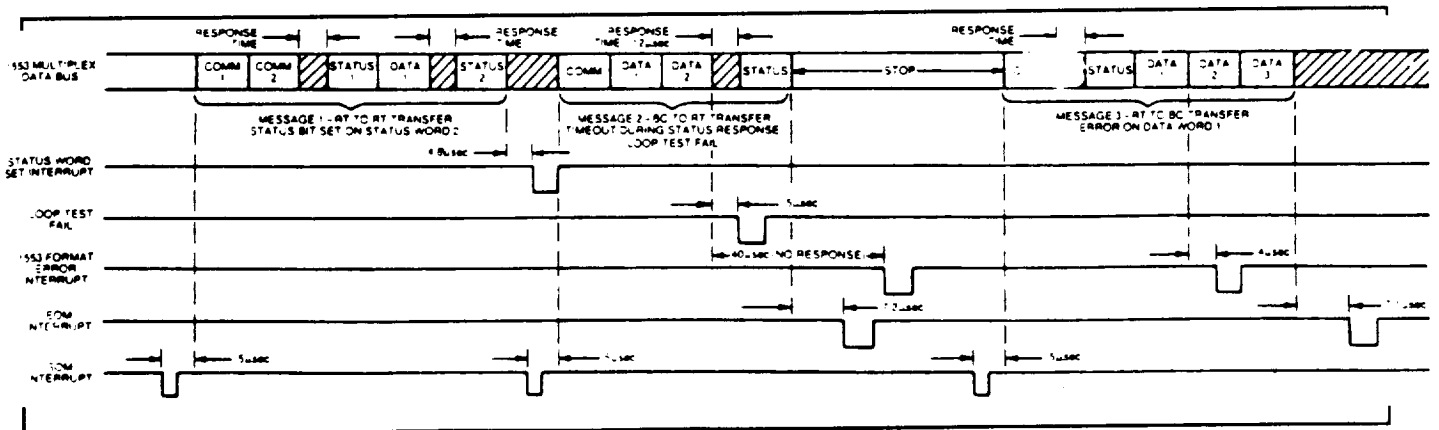
Figure 3.1.2.5.1.2.5-3   Typical Bus Controller Interrupt Timing
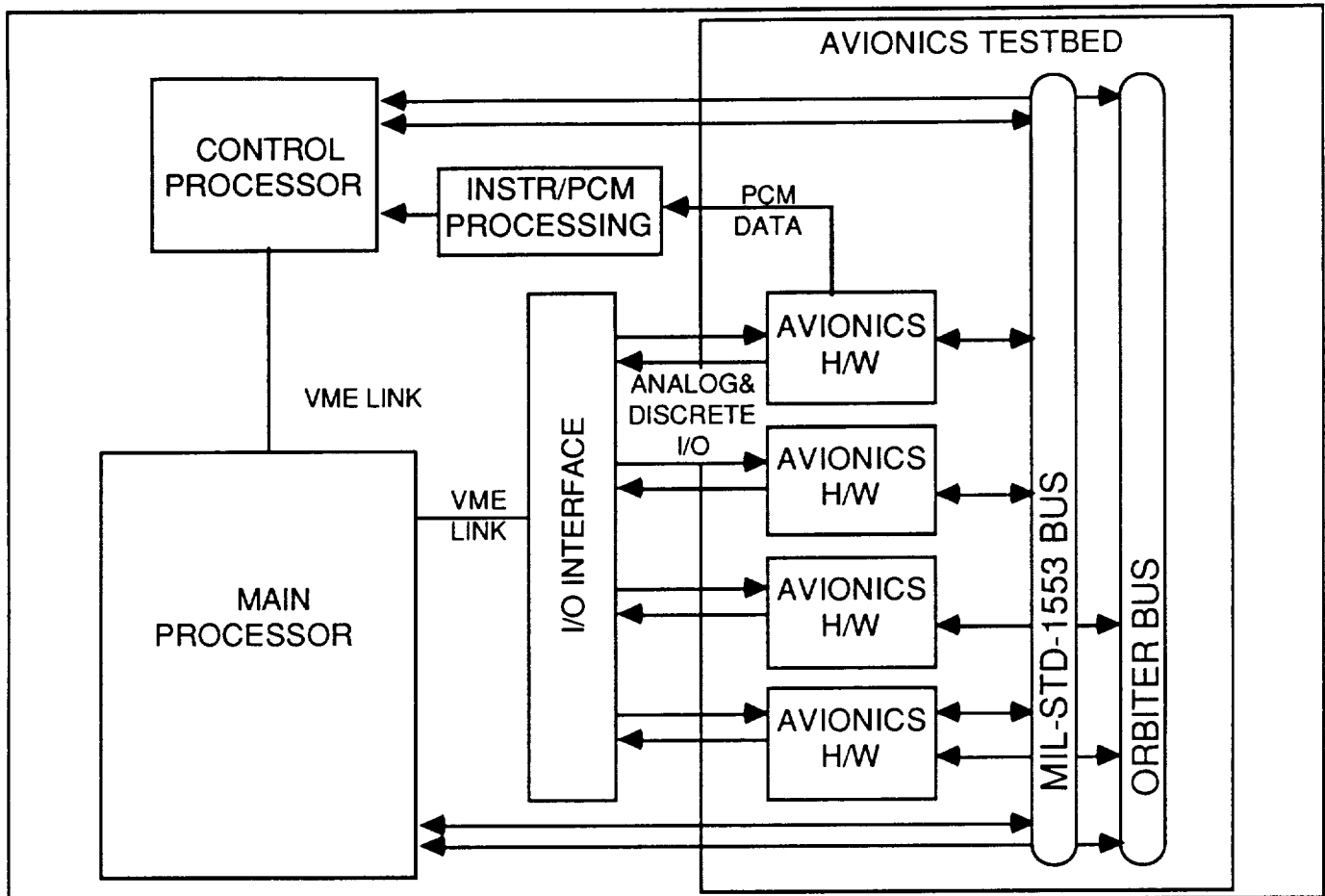
Figure 3.1.2.5.1-1.   Avionics Testbed Interfaces

3.1.2.5.1.3   Orbiter Avionics Buses. The GBT shall have the orbiter data bus interfaces in order to provide the capability to integrate, analyze and simulate the shuttle-type avionics components.

3.1.2.5.1.3.1 Interface the Central Control Processor. The GBT shall contain one Custom Orbiter Bus to VMEbus interface card with software and 30' twisted shielded pair cable to interface the main control processor and the avionics bus.

3.1.2.5.1.3.2 Interface the Main simulation processor. The GBT shall contain one Custom Orbiter Bus to VMEbus interface card with software and 30' twisted shielded pair cable to interface the main simulation processor and the avionics bus.

3.1.2.5.1.4   Instrumentation Interfaces. The GBT shall have the capability to support four 15 MBPS PCM data streams from the flight instrumentation hardware with the multiplexed bus instrumentation processing chassis specified in section 3.1.4.

3.1.2.5.2   Internal lab interfaces

The GBT shall have the following networks to integrate the processors and test equipment in each functional module in addition to linking extension facilities to the core laboratory segment to form a completely integrated lab.

3.1.2.5.2.1 Communication Network #1. The Graphic/Utility Processors shall be linked to the main Control Processor using an 80 MBPS fiber optic network in the star configuration.

3.1.2.5.2.1.1 Wire Center. The GBT shall contain one ProNET six node wire center to link the fiberoptic lines of communication network #1.

3.1.2.5.2.1.2 Central Control Processor Interface. The GBT shall contain one ProNET to VMEbus interface card with interface software and 10' ProNET fiber optic cable to interface the control processor to the wire center of communication network #1.

3.1.2.5.2.1.2 Graphics/Utility Processor Interface. The GBT shall contain four ProNET to PC interface cards with interface software and four 20' ProNET fiber optic cables to interface the graphics/utility processors to the wire center of communication network #1.

3.1.2.5.2.2 Communication Network #2. The extension facilities shall be linked to the Central Control Processor using an 80 MBPS fiber optic network in the star configuration.

3.1.2.5.2.2.1 Wire Center. The GBT shall contain one ProNET twelve node wire center to link the fiberoptic lines of communication network #2.

3.1.2.5.2.2.2 Central Control Processor Interface. The GBT shall contain one ProNET to VMEbus interface card with interface software and 10' ProNET fiber optic cable to interface the control processor to the wire center of communication network #2.

3.1.2.5.2.2.3 G&N Processor Interface. The GBT shall contain one ProNET to PC interface card with interface software and one 100' ProNET fiber optic cable to interface the G&N control processor to the wire center of communication network #2.

3.1.2.5.2.3 VMEbus I/O extension integration. The VMEbus I/O extensions in the core facility and in the extension facilities shall be integrated using host processor links to tie the extensions to the facility processors, repeater links to share data on close proximity chassis and fiberoptic links to link distant extensions.

3.1.2.5.2.3.1 Main Simulation Processor I/O interface. The GBT shall contain three VMEbus host processor DMA interface cards with interface software and 10' parallel bus cables to interface the Main simulation processor to the the VMEbus Master I/O chassis.

3.1.2.5.2.3.2 Core lab VMEbus master to slave chassis interface. The GBT shall contain six VMEbus master repeater cards, slave repeater cards, and 10' repeater cables to share data on the VMEbus master and slave chassis in the core lab segment.

3.1.2.5.2.3.3 Core lab to G&N extension VMEbus interface. The GBT shall contain the following hardware to interface the I/O chassis in the core lab segment to the I/O chassis in the Guidance and Navigation extension facility: one long distance VMEbus master repeater card, slave repeater card, and 250' repeater cable.

3.1.2.5.2.4 Instrumentation to control processor interface. To provide decommutated PCM data to the Control, Demo, & GSE segment processor. The control processor is linked to the instrumentation/PCM processing chassis using a 10 MBPS Ethernet coaxial cable link.

3.1.3 AVIONICS BENCHMARK HARDWARE

In order to facilitate development of new avionics systems, the lab should contain some benchmark hardware. This hardware can be used on early development stages of various projects such as Shuttle-C or ALS before actual flight hardware is available from vendors. It is suggested that the following types of avionics hardware be included in the testbed: Guidance and Navigation sensors, a Flight Control Processor, a Subsystem Controller, a Data Acquisition system and Flight Control system.

3.1.4 INSTRUMENTATION PROCESSING STATION

The Instrumentation Processing Station (IPS) shall synchronize and decommutate the PCM data from the onboard Instrumentation and transmit the data to the control center for monitoring. The IPS also shall have the capacity to time slice data, compress, and decompress data as desired. The IPS shall consist of a Multiplexed bus chassis, data processing cards, bit synchronization, and decommutation modules and I/O cards. Figure 3.1.4-1 shows a diagram of the functional breakdown of this module and its interfaces.
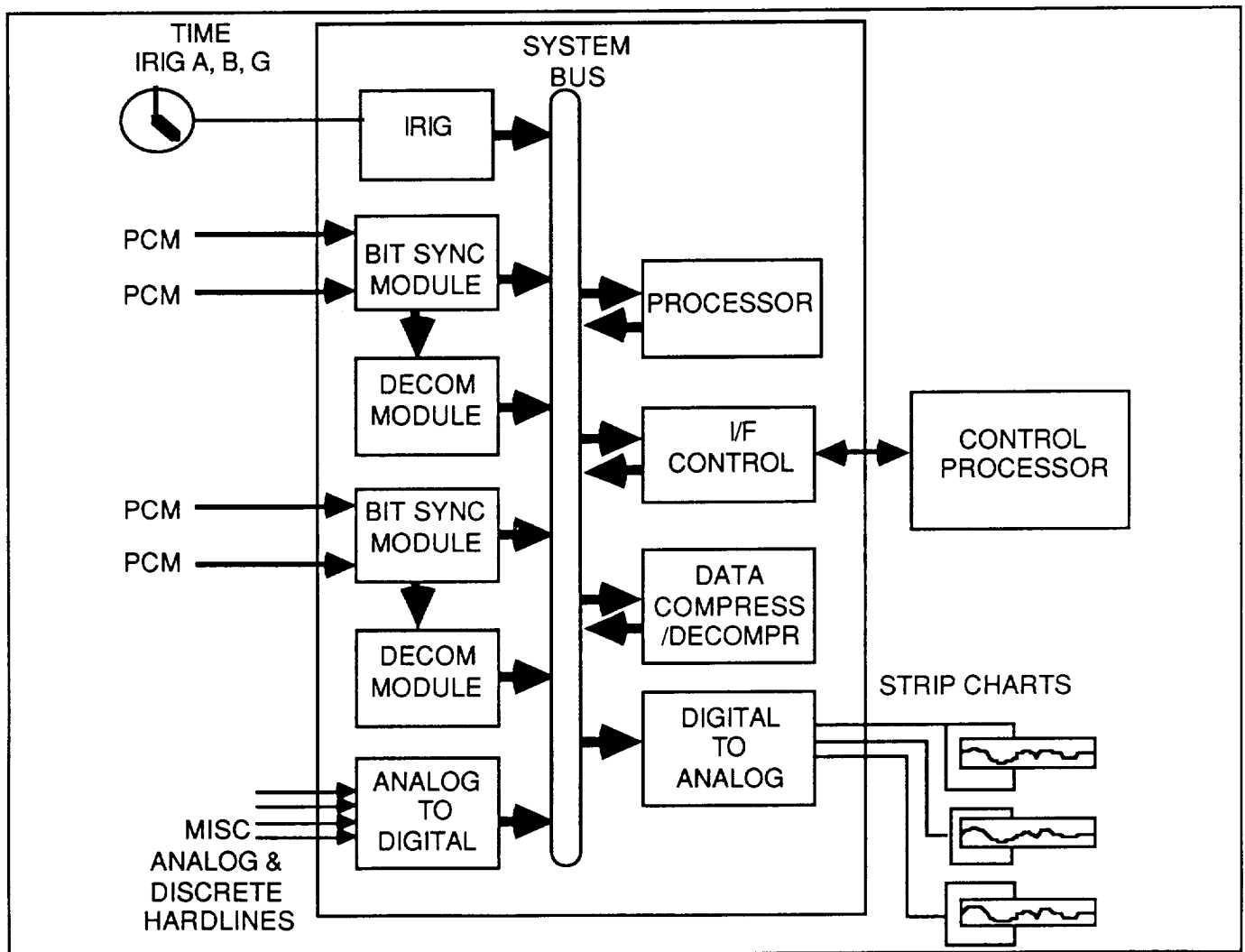
Figure 3.1.4-1. Instrumentation/PCM Processing Segment

3.1.4.1   Characteristics. The IPS shall be a modular, scaleable system that supports data processing, including compression and decompression.

3.1.4.1.1   General

3.1.4.1.1.1   Operating system

3.1.4.1.1.2   Backplane. The IPS shall have a 192 MBPS, 32 bit, multiplexed bus backplane.

3.1.4.1.1.3   Memory. 512 kbytes per processor.

3.1.4.1.1.4   Chassis slots. 15 slots per telemetry front end chassis. one slot used for the data processor module, one slot used for the data compression/decompression module, six slots used for the two bit synchronization modules, four slots used for the two decommutation modules, and one slot used for the ethernet controller.

3.1.4.2   Performance. The IPS subsystems shall have the following performance characteristics:

3.1.4.2.1   Bit-synchronization and decommutation throughput. Four channels at 15 MBPS.

3.1.4.2.2   Data compression/decompression throughput

3.1.4.2.3   Processor floating point instructions per second. 5 million minimum.

3.1.4.2.4   Communication link throughput. 10 MBPS.

3.1.5 DEMONSTRATION/DISPLAY CENTER (DDC)

The DDC is a centrally located room in the lab that contains equipment necessary for effective presentation. This phase 1 equipment consists of four graphic/utility processors, four 14" monitors, a laser printer, and a line printer. The Target configuration contains Four additional large display monitors, video recorders, a viewing screen, viewgraph projectors, tables and chairs. Figure 3.1.5-1 shows a diagram of the demonstration and display center.

3.1.5.1   Graphic/Utility Processors:

The four Graphic/Utility processors shall display realworld and computer values of guidance, navigation, control and environmental parameters in a manor for easy assimilation. These processors are also useful for software development when not being used for graphics.

3.1.5.1.1   Characteristics:

3.1.5.1.1.1   General:

3.1.5.1.1.1.1 Operating system. The operating system shall be MS DOS.

3.1.5.1.1.1.2 Processor backplane. The Graphic/Utility processors shall be PC compatible machines for reasons of cost and software support and therefore have a PC backplane.

3.1.5.1.1.1.3 Memory 4 Mbytes minimum.

3.1.5.1.1.1.4 <u>Input/Output ports</u> Minimum 1 ports into the PC backplane.
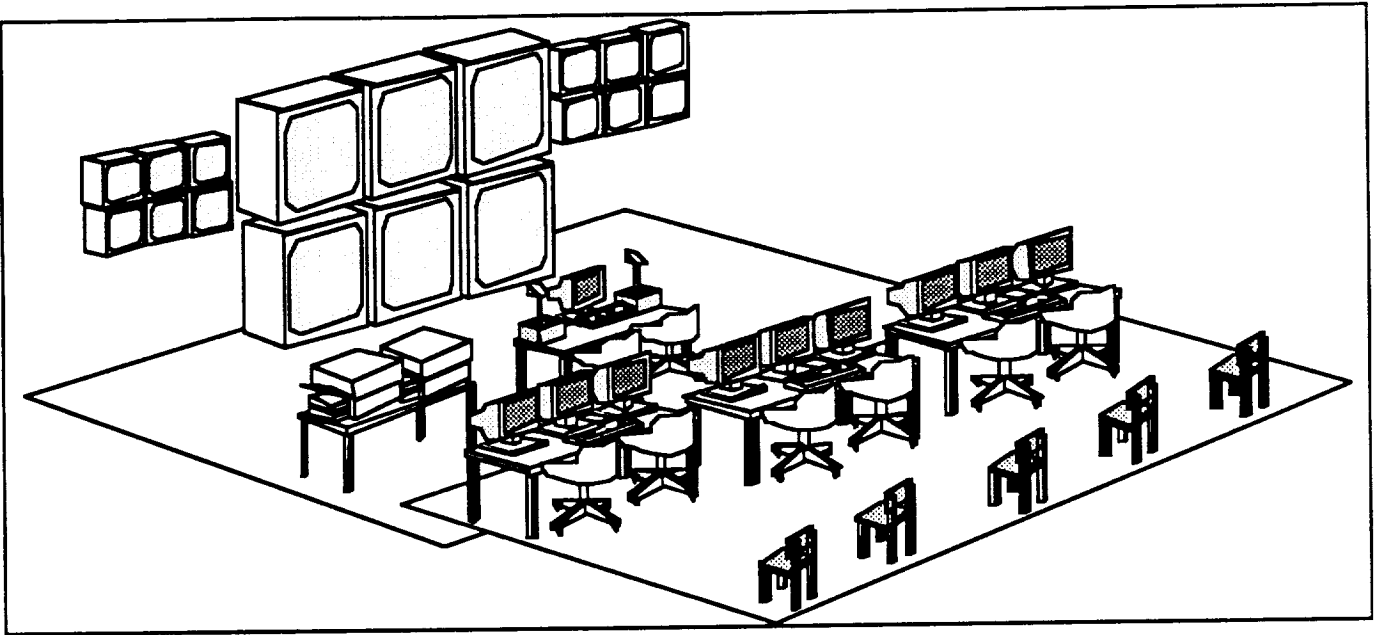
Figure 3.1.5-1. Demonstration and Display Center

3.1.5.1.1.1.5 <u>Video Extension</u> VGA extension with a screen resolution of at least 720X480, and a color pallet with at least 256 colors.

3.1.5.1.1.1.6 <u>Data Storage</u> Each processor shall have one 300 Mbyte hard disk and one floppy disk.

3.1.5.1.1.2 <u>Performance</u>:

3.1.5.1.1.2.1 <u>Integer Instructions per second</u>: 5 Million minimum.

3.1.5.1.1.2.2 <u>Floating point instructions per second</u> 5 Million minimum.

3.1.5.1.2 <u>Data displayed on monitors for Phase 1 Lab</u>

    (A) Guidance and navigation hardware parameters
        Effective time (seconds)
        Incremental velocity in sensor frame (X, Y, & Z components)
        Incremental angular attitude in sensor frame (X, Y, & Z)
        Body to navigation quaternion(magnitude, X, Y, & Z components)
        Filtered body attitude rate (Roll, Pitch, & Yaw components)
        IMS mode
        Data message
        IMS BIT status
        Gyro temperatures
        Accelerometer temperatures
        IMS power supply voltages
        PLC reset enable/inhibit status
        Filter coefficients

Mounting to body quaternion
Sensor to navigation quaternion
Latitude
Gravity
Accelerometer bias deltas

(B) Guidance
Targets (C1, C2, HT, Theta, WT)
Thrust integrals
Guidance integration cycle
Steering position commands
Steering rate
Airframe steering limit
Actual steering position

(C) Environmental parameters
Atmospheric density
gravity magnitude and direction
temperature
winds
Timetag
Vehicle position M50
Vehicle velocity M50
Sensor position Error
Sensor velocity Error
Vehicle velocity sum

(D) Orbital parameters
Altitude of apogee (NMI)
Altitude of perigee (NMI)
Radius of apogee (NMI)
Radius of perigee (NMI)
Eccentricity (%)
Time to apses (sec)
Orbit time (sec)

(E) Redundancy Management
Failure thresholds for each redundant component
current values to be compared to thresholds
failure flags for each component

(F) Vehicle Dynamics Parameters
Vehicle mass
Mass flow each engine
Mass flow rate each engine
Thrust vector each engine
Dynamic pressure
Vibration
Lift
Drag ·

(G) Statistical information
Mean position and velocity error (U, V, W, UDOT, VDOT, WDOT)
3 sigma position and velocity error (U, V, W, UDOT, VDOT, WDOT)
Maximum position and velocity error (U, V, W, UDOT, VDOT, WDOT)
Inplane error

3.1.5.2   Display Monitors. The Display monitors handle the presentation of computer generated graphics and information on a scale large enough to be viewed by all occupants of the DDC simultaneously.

3.1.5.2.1   Characteristics

3.1.5.2.1.1   Color. The monitors shall be color.

3.1.5.2.1.2   Size. The screens shall be a minimum of 44" diagonal.

3.1.5.2.1.3   Resolution. The screens shall have a resolution of TBD.

3.1.6 TARGET LAB SOFTWARE

3.1.6.1   TEST CAPABILITIES

3.1.6.1.1   Real-time Simulations multi-processor based. The software developed shall support real-time, multi-processor based simulations of existing or new unmanned vehicles including but not limited to Shuttle-C, Centaur, OMV, STV, and ALS. The software shall be structured to take advantage of the multi-processor host computer to meet the simulation speed requirements. Additionally, the software shall be structured to allow variable frame-times for the individual software modules. An example of the multi-processor, variable frame time structure is shown in figure 3.1.6.1.1-1.

3.1.6.1.2   Phases of Flight. The software shall be structured to allow the capability to simulate any phase of flight including but not limited to pre-launch, ascent, on-orbit, re-entry and landing. This capability shall allow the simulation of both individual flight phases and an integrated mission consisting of multiple flight phases.

3.1.6.1.3   Integration of Avionics hardware into real-time simulations. The software shall provide interface routines to drive appropriate I/O hardware. These routines and associated I/O hardware shall have the capability of reading from and writing to existing and/or new avionics hardware in a real-time manner. The avionics hardware to be supported includes but is not limited to Guidance and Navigation systems, Controls interface, data acquisition system and power systems.

3.1.6.1.4   Real time simulation of avioinics hardware. Software modules shall be provided to perform real-time and non-real-time simulations of existing or new avionics hardware. These modules shall be in varying levels of fidelity to meet necessary real-time requirements. The software shall allow the simulation of multi-string avionics hardware by the use of multiple software modules and/or actual hardware.

Instructions per frame

Processor													
Processor #1	Input 1501	Act 1 (400)	Eng 1 (141)	Vehicle Dynamics (1481)	Act 1 (400)	Eng 1 (141)	Vehicle Dynamics (1481)	...	Act 1 (400)	Eng 1 (141)	Vehicle Dynamics (1481)		Output (625)
Processor #2	Input 1501	Act 2 (400)		ACS 1-10 (1240)	Act 2 (400)		Atmosphere Gravity Grav Grad Aero (1468)		Act 2 (400)		Mass Proos 10-15 (1100)		Output (625)
Processor #3	Input 1501	Act 3 (400)	Eng 2 (141)	ACS 10-20 (1240)	Act 3 (400)	Eng 2 (141)	ACS 10-20 (1240)		Act 3 (400)	Eng 2 (141)	Body Bending (1000)		Output (625)
⋮		⋮											⋮
Processor #40	Input 1501	Act 40 (400)			Act 40 (400)				Act 40 (400)				Output (625)

├──────────────── 2 msec (500 Hz) ────────────────┤

- Fastest processing requirements in processor #1
  - 41215 instructions / 2 msec => 20.6 MIPS
- Other processor requirements
  - Actuator and engines computations
    - 11595 instructions / 2 msec => 5.8 MIPS / processor
- Low frequency computations (atmosphere, gravity, etc.)
  - Performed in any available time "slots"

Figure 3.1.6.1.1-1. Typical Parallel-Processing Timing Diagram (Single Vehicle, Medium Fidelity, 3-String Autopilot Avionics)

3.1.6.1.5   Fault insertion capabilities. The software shall allow for the simulation of vehicle/subsystem faults and avionics hardware faults. Manual, pre-canned and random fault-insertion capabilities shall be provided.

3.1.6.1.6   Stand-alone avionics hardware testing. The software shall provide the capability to perform stand-alone testing of existing and/or new avionic hardware. This capability shall be independent of the main simulation, though individual simulation routines may be used if necessary. The stand-alone testing shall have an acceptance test procedure (ATP) type of format, providing stimuli to the hardware and monitoring appropriate hardware responses. The software shall be structured to allow for a variety of test lengths and shall include automatic, semi-automatic and manual test capabilities. The semi-automatic and manual test modes shall be such that an operator can manually select which hardware inputs to stimulate and which hardware outputs to monitor. Additionally, the operator may manually start the execution of any pre-programmed automatic test sequences.

3.1.6.1.7   User friendly interface. The software shall provide a user-friendly interface based on a tree-structure and utilizing multiple window displays.

3.1.6.1.8   Multiple users. The software shall provide multiple user capability. This capability shall allow separate users to perform simultaneous independent simulations, LRU tests and software development within the performance constraints of the host computer, bus traffic and I/O constraints and avionics hardware availability.

3.1.6.2   LAB CONFIGURATION SOFTWARE

3.1.6.2.1   <u>Program status</u>. The lab configuration software shall maintain a consistent structure during the development of the lab. The structure shall allow for a flexible simulation development and execution environment. This structure shall be based on the use of generic simulation modules and application-specific data files.

3.1.6.2.2   <u>Tree-based multi-level menus</u>. The lab configuration software shall incorporate the tree-structured elements shown in Figure 3.1.6.2.2-1, -2 and -3.

- **Each block represents an individual main program module and menu**
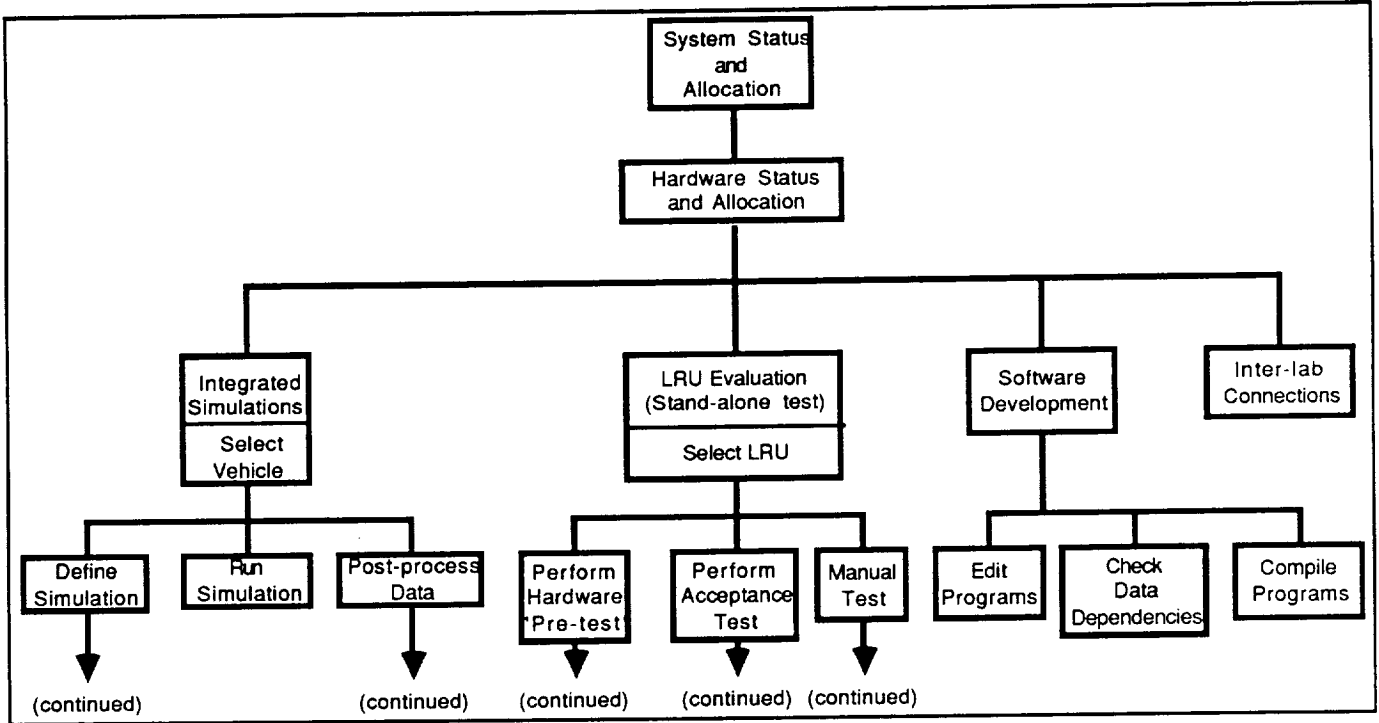
Figure 3.1.6.2.2-1. LAB CONFIGURATION SOFTWARE: GBT TARGET AND PHASE 1 DESIGNS - PROGRAM / MENU STRUCTURE

• Each block represents an individual main program module and menu
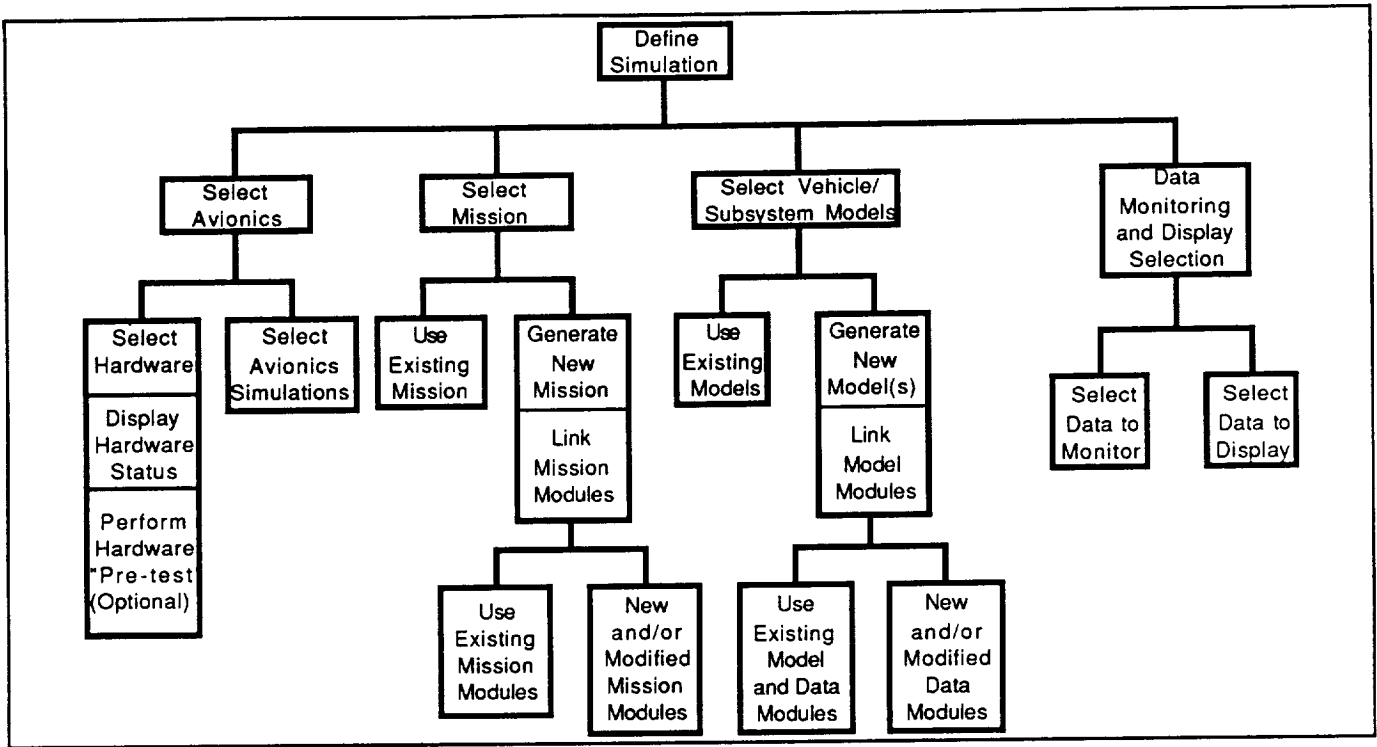
Figure 3.1.6.2.2-2. LAB CONFIGURATION SOFTWARE: GBT TARGET AND PHASE 1 DESIGNS - PROGRAM / MENU STRUCTURE (cont)

• Each block represents an individual main program module and menu

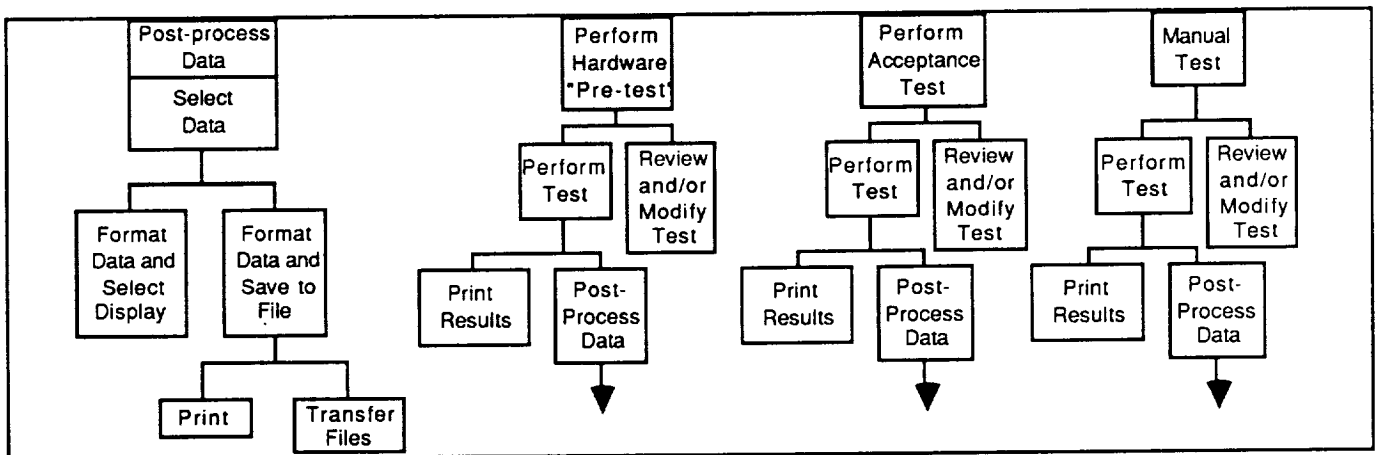**Figure 3.1.6.2.2-3. LAB CONFIGURATION SOFTWARE: GBT TARGET AND PHASE 1 DESIGNS - PROGRAM / MENU STRUCTURE (cont)**

3.1.6.2.3   Elements. All program modules and menus shall be generic, i.e., the menu structure shall change for different simulations and lab configurations. All elements are data driven either by user defined data files and/or user commands from the keyboard. The

software design goal shall be to not require new software modules to be written (coded) as a new simulation is defined.

3.1.6.3   SIMULATION MODELS

3.1.6.3.1   Mission/Vehicle/Environment Models. Simulation software shall be provided to support avionics testing in simulated ascent, orbital and controlled reentry phases. The fidelities and frame types of the software modules shall be variable and selectable using data files. As a minimum, software modules shall be provided to support components shown in figure 3.1.6.3.1-1.

SIMULATION MODULE DESCRIPTIONS

- 6 DOF Dynamics - propagates 6 dof dynamics for each vehicle
- Mass properties - calculates time varying vehicle mass properties based on fuel consumption and vehicle staging / separation events
- Aerodynamics - calculates aerodynamic forces using lower and upper atmospheres and reentry models
- Body bending - calculates vehicle bending effects based on vehicle stiffness and/or bending modes
- Slosh - calculates fuel slosh effects on vehicle accelerations and cg
- Main engines - calculates engine thrust and fuel use based on low and high fidelity engine models
- Reaction control system (RCS) - calculates RCS effects and fuel use based on low and high fidelity RCS and RCS fluids models
- Actuators - calculates actuator positions based on low and high fidelity electro-mechanical actuator models
- Thrust vector control (TVC) - calculates thrust vector forces based on engine thrust, actuator positions, and vehicle bending effects
- Environment - calculates atmospheric parameters based on altitude, simulates disturbances and wind effects
- Hardware / software interfaces - provides I/O routines for hardware in the loop, I/O simulations for simulated hardware

**Figure 3.1.6.3.1-1.   PHASE 1 SIMULATION MODELS: -
MISSION / VEHICLE / ENVIRONMENT MODELS**

3.6.1.3.2   Avionics Simulation Models. Simulation software shall be provided to functionally simulate avionics hardware. The software models shall be structured to allow for the testing of redundancy concepts such as multiple sets of avionics (hardware and/or software simulation), cross-channel communications, synchronization and shielding. As a minimum, software modules shall be provided to support the components shown in figure 3.6.1.3.2-1.

> - **Descriptions**
>
> - **NAVIGATION** - simulates inertial sensors and flight control processor functionality and interface electronics
> - **VOTING LOGIC** - simulates voting logic functionality and interface electronics
> - **DATA ACQUISITION** - simulates data acquisition, reduction and transmission and interface electronics
> - **ENGINE CONTROLLER** - simulates engine controller functionality and interface electronics
> - **RGU and AA** - simulates rate gyros and accelerometers
> - **Cross-channel communications** - provides cross-channel data link between avionics modules (hardware and/or software models)
> - **Synchronization and skewing** - synchronizes with hardware and provides artificial skewing to software models
> - **Instrumentation** - simulates data necessary for DAS operation

Figure 3.1.6.3.2-1.   PHASE 1 SIMULATION MODELS: - AVIONICS SIMULATOR MODELS

3.1.7 GUIDANCE & NAVIGATION EXTENSION

General Information: The term, Extension, refers to a lab that is co-located with the GBT. Generally any extension may operate either open loop or closed loop. This meets the philosophy that a Technology under test or a unit under test may be evaluated independently without exclusively using all lab resources. The main elements within the G&N Extension are:

(a)   Three-axis table(s), with thermal chamber(s), and alignment equipment.

(b)   Slave Input/Output Interface Box (VME)

(c)   Unit under test (IMU)

(d)   Interface and Control Processors

(e)   Software

3.1.7.1   3-AXIS TABLE

Three-Axis Table Specification Summary (Model 53M-3C)   Sections 3.1.7.1.1 through 3.1.7.1.4 summarize the specifications for the Model 53M-3C Three-Axis table. Sections 3.1.7.1 and 3.1.7.1.2 present the overall physical and mechanical specifications of the simulator. Included in Section 3.1.7.1.2 are the mechanical performance specifications such as bearing wobble and axes orthogonality. Section 3.1.3.1.3 summarizes the major control mode performance specifications. Section 3.1.7.1.4 gives the data readout specifications including the specifications for the encoder, display, and serial I/O.
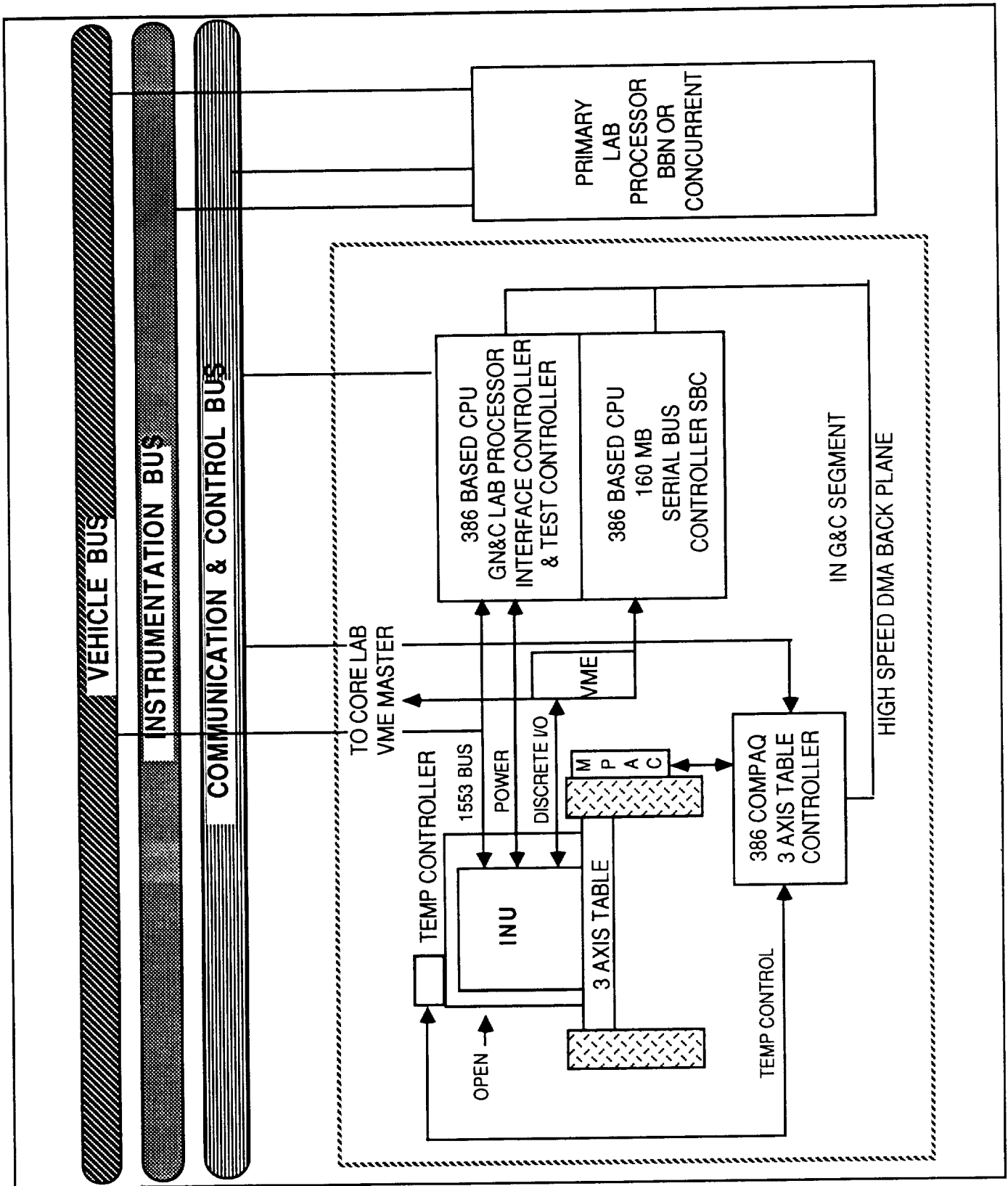
Figure 3.1.7-1.   Top Level Layout, G&N Extension Open-Loop/Closed-Loop
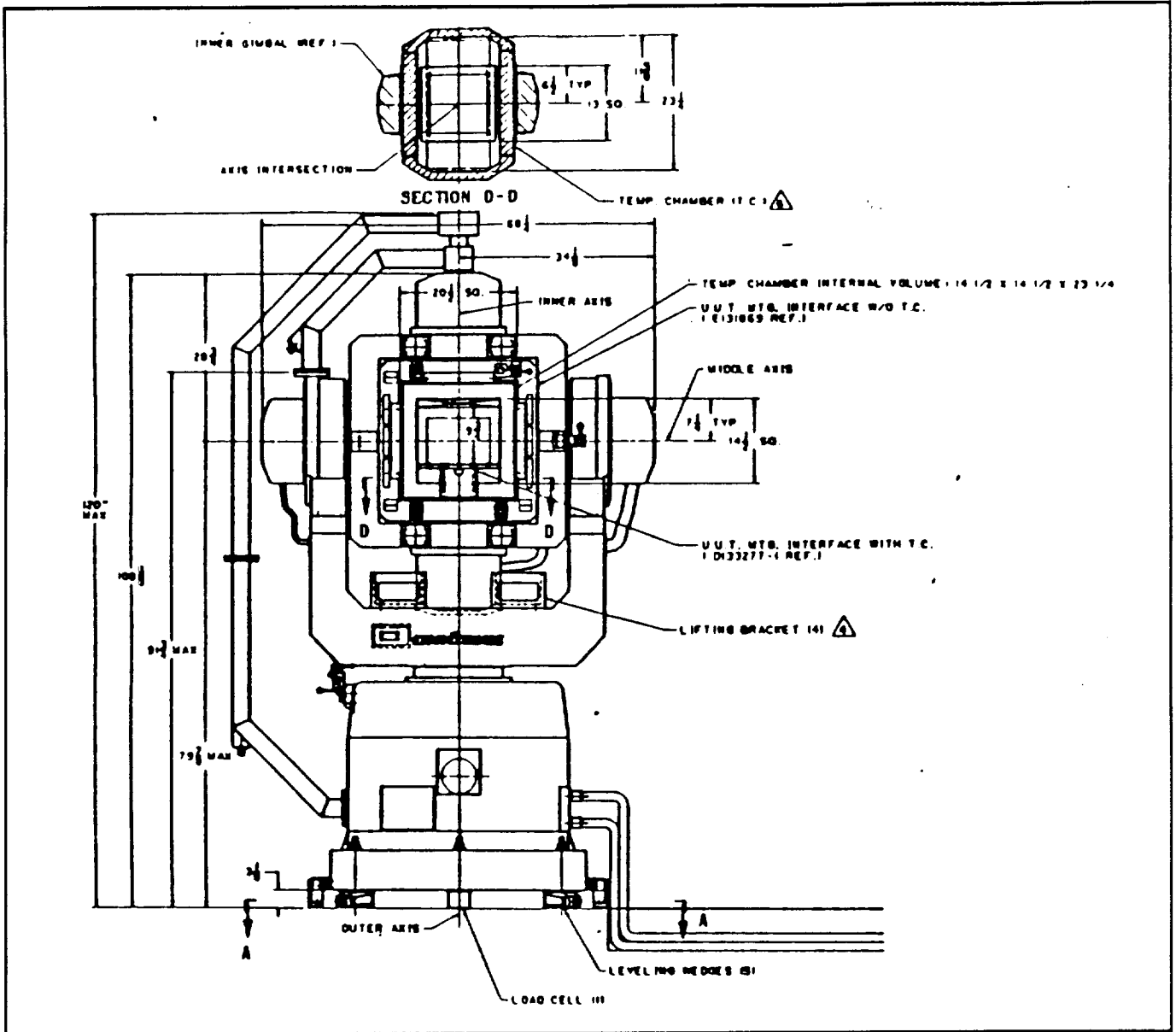
Figure 3.1.7.1.1-1.   Model 53M-3C Motion Simulator Without Environmental Chamber

3.1.7.1   Physical Specifications

Motion Simulator
        Size   See figure 3.1.7.1.1-1
        Weight   3000 lbs, approximately

Control Console
        Type   Standard 19" rack-mount, single-bay console
        Size   84" H x 72" W x 17" D
        Weight   < 1500 lbs

3.1.7.1.2   Payload Specifications

Without Environmental Chamber
    Maximum Size   20" x 20" x 20" cube or 20" dia x 24" long cylinder
    Maximum Weight   300 lbs plus counterweights

With Environmental Chamber
    Maximum Size   11" W x 22" L x 9" H
    Maximum Weight   200 lbs plus counterweights

Axis Balancing
    Method   Bolt-on counterweights
    Resolution   Within friction torque of the axis
    Readout   Electronic readout showing imbalance magnitude &
                        location

Electrical Access to UUT   142 lines total: 60 twisted shielded pairs @ 5 amps/line;

                        22 AWG: 4 single ground lines @ 5 amps/line; 22 AWG:
                        6 channels of MIL-STD-1553 (3 lines each)

Operating Environment
    Temperature   70 degrees ± 15 degrees F
    Relative Humidity   10 to 95% non-condensing

Base Leveling
    Range   ±0.5 degrees
    Resolution   1 arc second

Base Azimuth Adjustment
    Range   ±1 degree
    Resolution   1 arc second

Axis Freedom (all axis)   Unlimited

Axis Orthogonality   2 arc seconds, maximum

Axis Intersection   0.010-inch radius, sphere, maximum

Bearing Wobble (all axis)   2 arc seconds, peak-to-peak @ 0.04 deg steps over 1 deg
                        2 arc sec p-p @ 14.4 deg steps over 360 deg (lo speed)

                        5 arc seconds, peak-to-peak @ 0.04 deg steps over 1 deg
                        5 arc sec @ 14.4 deg steps over 360 deg (hi speed)

Rate Transducer (all axis) 0.1% ripple DC tachometer

Position Transducer
    Coarse (all axis)   ±3 arc minutes, 2-pole resolver
    Fine (all axis)   ±1 arc second, 720-pole Inductosyn

Rate Range (all axis)   0.0000 to 999.999 deg/sec

Peak Acceleration (with temperature chamber, without load)

Outer Axis	11.5 rad/sec^2 (660 deg/sec^2)
Outer Axis	10.3 rad/sec^2 (590 deg/sec^2)
Outer Axis	29.0 rad/sec^2 (1660 deg/sec^2)

3.1.7.1.3   Control modes specifications

A. TACHOMETER RATE MODE (EACH AXIS)

Transducer	DC Tachometer
Rate Command Range	0.01 to 999 deg/sec
Resolution	0.1% on each range
Data Format	3-digit keyboard entry
Short Term Stability	±0.75% over 10 deg, ±0.5% over 360 deg
Rate Limit	An adjustable rate trip limit is provided to disconnect the axis torque motor between preselected rates of 4 and 1000 deg/sec

B. POSITION MODE (ALL AXIS)

Transducer	720 pole Inductosyn and resolver
Data	Manual keyboard input or from data bus
Range	0.0000 to 359.9909 deg (lo speed mode) 0.000 to 359.999 deg (hi speed mode)
Resolution	0.0001 deg (lo speed mode) 0.001 deg (hi speed mode)
Accuracy	2.0 arc sec, peak-to-peak 0.04 deg steps over 1 deg; 2 arc sec p-p@ 14.4 deg steps over 360 deg (lo speed mode) 5.0 arc sec, peak-to-peak 0.04 deg steps over 1 deg; 5.0 arc sec p-p@ 14.4 deg steps over 360 deg (lo speed mode)
Repeatability	0.1 arc sec
Traverse	0.1 to 30 deg/sec least path adjustable

C. PRECISION DIGITAL RATE MODE (ALL AXIS)

Rate Command Range	Lo Range	0.0001 to 199.999 deg/sec or ERU
	Hi Range	0.001 to 999.999 deg/sec or ERU
Data		Manual keyboard input or from data bus
Resolution	Lo Range	0.0001 deg/sec or ERU
	Hi Range	0.001 deg/sec or ERU

Drift (Zero Range)   Essentially zero, ±0.3 arc sec/24 hours non-cumulative

Rate Accuracy   0.001% over 360 deg
Rate Stability   0.003% over 360 deg

D.   ACCELERATION CONTROL MODE
     Command Range   0.00 to 4000 deg/sec^2

     Data   Manual keyboard input or from data bus

     Resolution   0.01 deg/sec^2

     Accuracy   0.01%

3.1.7.1.4   Data readout system specifications

3.1.7.1.4.1   Encoding mechanism and position/rate readout display

Axis Display Format   7-digit available to display absolute position

Display Update Frequency   100 Hz

Position Update Frequency   The fine and coarse position transducer outputs are
                            continually locked to the fine and coarse positions. The
                            complete position is sampled by data buffers @ 2.4 kHz

Position Encoder Short   0.18 arc sec (lo speed)
   Term Stability   1.8 arc sec (hi speed)

Quantization   0.36 arc sec (lo speed)
                            3.6 arc sec (hi speed)

Encoding Mechanism   0.5 ppm
Timebase Long-Term
   Stability

Readout Lag due to   1 arc sec/rad/sec (when sampled at submultiples of the
   Velocity   reference frequency)

Readout Lag due to   2 arc sec/rad/sec^2
   Acceleration

Position Display Range   0.0000 to 359.9999 deg (lo speed)
                            0.000 to 359.999 deg (hi speed)

3.1.7.1.4.2   Asynchronous serial I/O specifications

Format   RS-232 compatible

Baud Rate   Switch selectable baud rates are:
                            75   300   1800

110	600	2400
150	1200	4800

3.1.7.1.4.3   Encoder Output Specificaitons

These outputs are available at the MPACS rear mounted multi-pin connectors.

LSB Position Pulse (TTL)

Quantization	0.0001 deg, 0.36 sec up/down (lo speed) 0.001 deg, 3.6 sec up/down (hi speed)
Rate Range	0.0000 to ±199.9999 deg/sec (lo speed) 0.000 to ±199.999 deg/sec (hi speed)
Accuracy	±1.0 arc sec (lo speed) ±2.5 arc sec (hi speed)

LSB Directional Signal

High (2.4-5 VDC)	Counterclockwise
Low (0-0.8 VDC)	Clockwise

3.1.7.1.5   Temperature chamber

3.1.7.1.5.1   Temperature control chassis (TCC)

Size	Industry standard 19-inch wide, 7-inch high rack mountable chassis
Input Power	220 VAC, 50 or 60 Hz
High Temperature Limit	Manually adjustable between 80-90 degrees C Setting
Low Temperature Limit	Manually adjustable between -50 and -60 degrees C Setting
Temperature Setting	Adjustable manually or via an IEEE-488 standard interface to a resolution of 0.1 degrees F -55 and +85 degrees C
Indications for exceeding temperature limits, chamber door open, chamber door closed, power on, heat on, cool on	Indicator lights mounted to chassis for front panel.

3.1.7.1.6   Electronic control system description. The electronic control system of the 53M-3C is configured into three subsystems:

1. Control Console, housing the Model 30H MPACS (Modular Precision Angular Control System), and Interlock Control Panel.
   The Control Console will be 2-bay, 30-inch deep, 6-ft high, Markhon Styleline 4100 series.

2. AC Motor Drive Console

3. Console to mount and inter-console cables

3.1.7.1.7   Equipment List

3.1.7.1.7.1   Model 30H MPACS Assembly and interlock control panel. The Model 30H MPACS Assembly consists of the following modular components:

a. Main Frame (Dual)
b. Power Supply Module (2 req.)
c. Transducer Excitation Module (lo speed)
d. Transducer Excitation Module (hi speed)
e. Zero crossing detector module
f. Rear connector panel
g. Reference module
h. Asynchronous Encoder Module (3 req)
i. Parallel Data Interface Module
j. 7-digit display (3 axis)
k. Position command Module with Digital Rqte (3 req)
l. Servo Control Module (3 req)
m. IEEE-488 GPIB Interface Module
n. Acceleration Control Modules (3)
o. 3-Axis Microprocessor Controlled Keyboard Control Module
p. Hi/Lo TXA switch
q. Hi/Lo TXA cable
r. Front and rear module Extender Kit (Calibration and Service Equipment)

The Model 30H MPACS is contained in a 19-inch console assembly along with the Interlock Control Panel. This panel provides both control of interlock functions, as well as a visual display of all interlock states. On the 53M-3C, the following interlock states are displayed for each axis.

a. Rate Trip Status
b. Motion Lock Status (Stow Lock)
c. Motor/Drive Status (conditions monitored include motor temperature, motor RMS current, drive temperature, drive voltage, etc.)
d. Mount Disable Status
e. Servo Status (ON/OFF)

Control of the following functions is provided:

a. Servo On/Off
b. Rate Trip Reset
c. Drive Fault Reset

3.1.7.1.7.2 <u>AC Motor drive console</u>. The AC motor drives are contained in a NEMA enclosure. This enclosure is specially designed to reduce EMI generated by the high-power PWM (pulse-width modulated) motor drives.

The AC motor drives utilized are the Contraves MACS (Modular AC Servo) drives. These units feature:

1. Closed-loop torque control

2. High power outputs (up to 18 kW continuous per drive)

3. Sine wave outputs (PWM generated) for maximum, ripple-free optimum delivered power

4. Regenerated energy control

3.1.7.1.7.3 <u>Console to mount and inter-console cable assemblies</u>. With the exception of some of the high power motor drive cables, all cable assemblies feature plug-in connectors to allow easy separation of the major system components. Thirty feet of cabling is provided between the mount and the consoles, twenty-feet of cabling is provided between the consoles.

3.1.7.1.8 <u>Model 30H mpacs assembly discussion</u>. The Model 30H MPACS in this system provides maximum system function and versatility in a minimum space. The design of this system ensures easy expansion in the field by the simple addition of plug-in modules. The modular construction eases troubleshooting and maintenance.

3.1.7.1.9 <u>Parallel data interface module</u>. The Parallel Data Interface (PDI) reads and stores position data from the axis encoder modules and rate data from the optional Direct Rate Readout modules. The PDI update sequence may be initiated from a remote source or internally programmed for rates up to 2.4 kHz. When the update is initiated, the module checks the busy line and begins sequencing the addresses and storing the data in the selected register. It continues until all buffers have been filled and then waits until another update is initiated. The parallel data may be used as inputs to a printer or to an unbuffered display.

3.1.7.1.10 <u>7-digit display panel</u>. The display panel is a 19" x 3.5" panel containing three sets of 7-digit fluorescent 7-segment displays. The display exhibits information presented by the PDI. Push buttons on the display panel allow the operator to elect to view either rate or position data for each axis. One display panel is required for three axis of readout.

3.1.7.1.11 <u>Position Command Module</u>. The Position Command module receives the phase-modulated Inductosyn and resolver outputs along with either the digital commands from the keyboard or CPU I/O, or incremental commands from the rate generator, to generate servo error signals. The continuous analog signal output is proportional to the difference between the command angle and the measured feedback.

3.1.7.1.12 <u>Servo module</u>. The Servo module provides the control modes and produces an analog voltage output to the power amplifier which is scaled to produce maximum torque. It consists of a digital logic card which receives the mode, command and digital input data via the internal address/data bus. An analog control card contains all of the active filters required for multi-mode control and dynamic test conditions on loop variables that initiate

control mode changes. Typical control modes are position (analog/digital) and rate (analog/digital).

3.1.7.1.13   <u>3-axis microprocessor controlled keyboard module</u>. The Programmable Keyboard Control module consists of a double width key panel assembly and utilizes a single slot to interface with the MPACS bus. The module printed circuit assembly consists of a single card containing all circuitry and firmware to interconnect to the MPACS bus, the RS-232 serial port, and the user key panel.

Microprocessor circuitry features a 6802 microprocessor unit, versatile interface adapters, 1K of non-volatile random access memory, a keyboard scanner, and direct interrupt service capabilities.

The key panel incorporates 24 axis-oriented, generic control keys. Sixteen additional keys are provided for data entry and special keyboard control functions; three of these keys are used to extend key functions for a total of 4 functions per key (a total of 160 controllable functions). The functions for each key may be independently enabled or disabled in the field.

An 8-digit display is provided to display 7-segment numbers and pseudo-alpha characters. Two switches provide degrees per second/Earth Rate Unit selection, and Local/Remote control.

Pre-programmed sequences may be entered in two modes: Learn and Monitor. The Learn mode allows an operator to key in a sequence by depressing those keys that would give the desired response in the normal Manual mode. A Memory Monitor allows key codes to be entered directly into the program storage blocks. In addition to the system control functions are dwell, loop and block execute commands.

Programming may be performed in Local or Remote modes, starting at any of six contiguous blocks.

Execution of pre-programmed steps is performed in the Auto (automatic) mode.

All programmed sequences are temporarily stored in a random access memory, and may be preserved in non-volatile memory by executing a SAVE command.

A detailed description of the keyboard capabilities is found in CGC document IM-11500.

3.1.7.1.14   <u>Front and rear extender kit</u>. The extender kits provide a means for trouble-shooting, calibration, and general servicing of modules. The extender incorporates serial jumper plugs allowing disconnection of any bus/connection to a module. Construction is of an aluminum housing and heavy duty printed circuit cards.

3.1.7.1.15   <u>IEEE-488 GPIB interface module</u>. The IEEE-488 GPIB Interface module provides an interface between the MPACS Standard Bus Matrix (SBM) and an IEEE-488 data bus. All MPACS display and control systems are connected to the SBM, allowing computer control of all MPACS drive control and display functions. The GPIB module relies on an internal microprocessor (6802) and a CMOS interface chip (68488) to implement incoming and outgoing IEEE-488 standard bus data.

3.1.7.1.16   <u>Acceleration control module</u>. The Acceleration Control Module provides the system with angular acceleration and deceleration control capability when in the Precision Rate mode. Profiling of acceleration is accomplished by entering data via the Keyboard

Control module (or external computer) in the acceleration mode prior to entering a rate in the RATE mode.

3.1.7.1.17   Status and matrix control module (not included). This optional module is not included in this system.

3.1.7.1.18   Gyro servo module (not included). This optional module is not included in this system.

3.1.7.1.19   Direct rate readout module (not included). This optional module is not included in this system.

3.1.7.1.20   Input/Output Panel (not included). This optional module is not included in this system.

3.1.7.1.21   Interlock chassis. The Interlock Chassis provides the operator with the ability to monitor all interlocks associated with the motion control system. It also controls the relays that apply power to the motion simulator torquers.

3.1.7.2   SLAVE INPUT/OUTPUT INTERFACE BOX

The VME Input/Output extension handles the interfaces between simulation and avionics hardware for the analog and discrete signals. The I/O extension consists of a VME chassis with a host processor link, a repeater link to the core lab, and the input and output cards necessary to integrate the VME I/O extension with the avionics component.
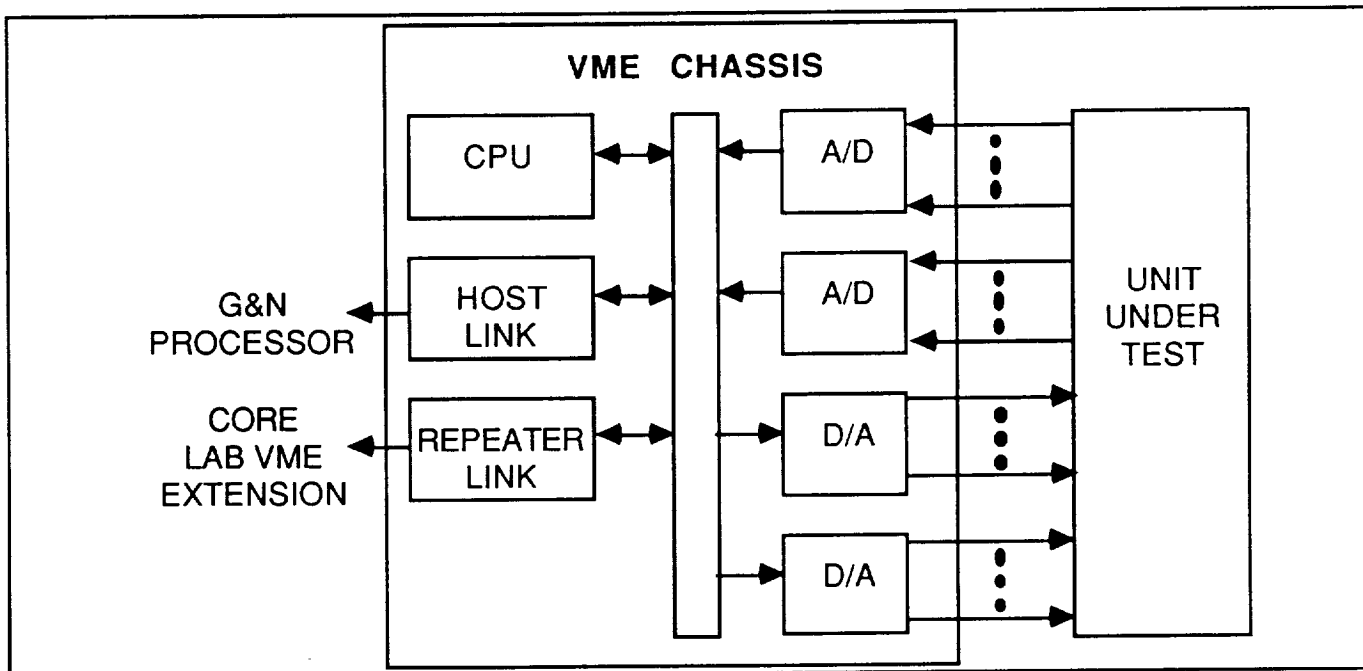
G&N Input/Output Interface Box config 3.1.7.2

3.1.7.2.1   Characteristics:

3.1.7.2.2   <u>General:</u>

3.1.7.2.3   <u>Operating System.</u> The Input/Output Extension intelligent I/O operating system for easy configuration and manipulation.

3.1.7.2.4   <u>Backplane.</u> The Input/Output Extension shall have a 24 MBPS VME backplane.

3.1.7.2.5   <u>Memory.</u> 512 kbytes per processor.

3.1.7.2.6   <u>Input/Output Ports.</u> 19 useable slots.

3.1.7.2.7   <u>Performance.</u> For high speed data switching, the VME IOC shall have six processors with the following performance characteristics:

3.1.7.2.7.1   <u>Integer Instructions per second:</u> 5 million per processor minimum.

3.1.7.2.7.2   <u>Floating Point Instructions per second:</u> 5 million per processor minimum.

3.1.7.3   G&N LAB CONTROLLERS AND INTERFACE PROCESSORS

The G&N extension is mechanized utilizing three 80386 Compaq to provide a Serial Bus Controller (SBC), an interface (1553) controller, and a test controller (TC). The configuration of the each computer is shown below.

TABLE 3.1.7.3

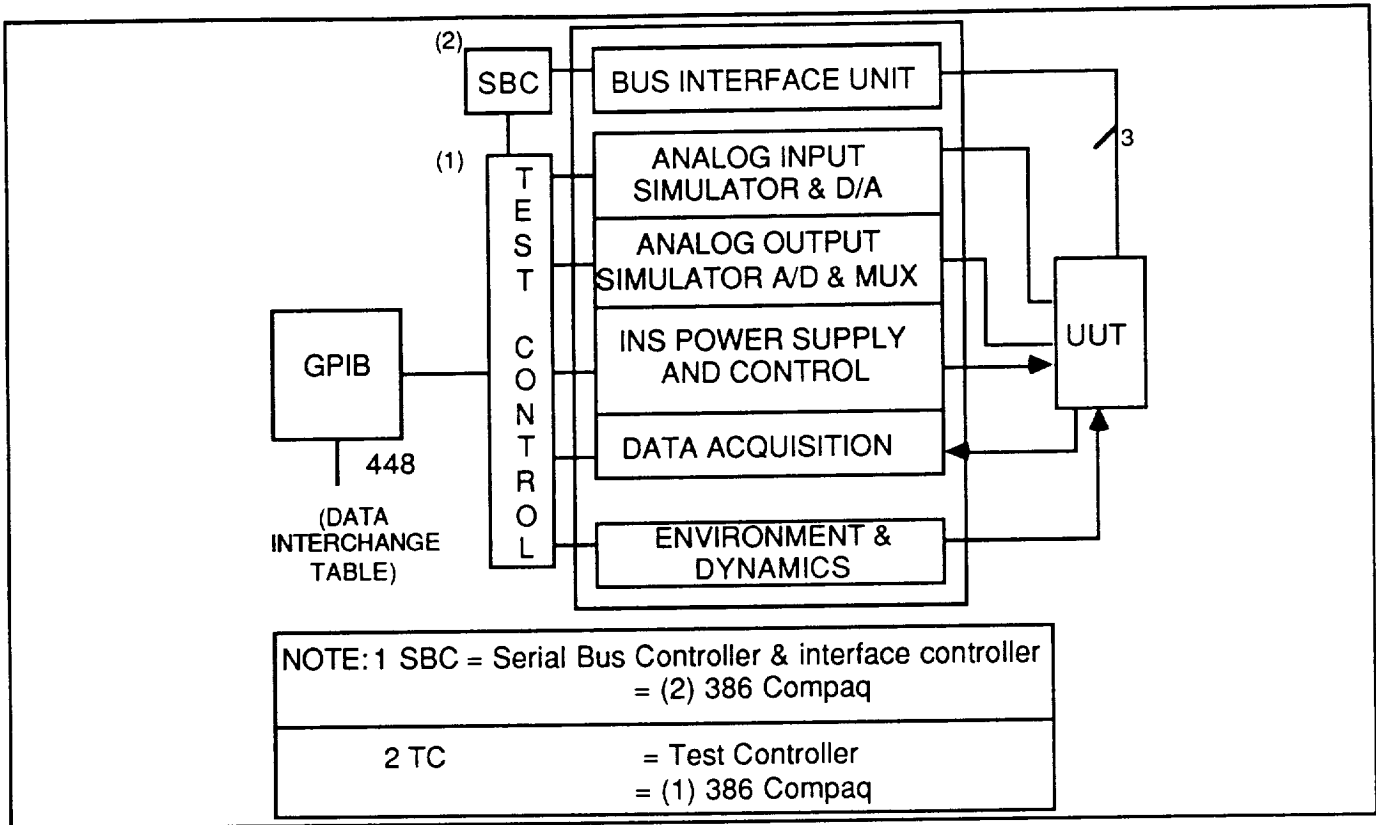| ITEM	SBC	TC
Computer	80386 AT	80386 AT
Memory	2 MB	2 MB
Co-Processor	80387	80387
Hard Disk	160 MB	40 MB
Floppy Disk	1.44 MB	1.44 MB
Monitor	Zenith ZMC/1490	Zenith ZMC/1490
Printer	Laserjet	Dot Matrix
GPIB Interface	Two	Two
Arcnet	One	One
Serial I/O	Two	Two
EGA Card	One	One
Enhanced Keyboard	One	One
Mouse	None	One
Cassette Tape	One	None

Figure 3.1.7.3-1.   Guidance & Navigation Extension Open Loop Configuration

3.1.7.3.1   Open loop testing. The G&N extension shall be required to verify the proper operation of the UUT. Proper operation will be verified by a box level, non-dynamic test which operates each of the interfaces.

In addition the G&N extension shall provide the capability to perform the special INU Dynamic I/O test. The dynamic testing shall consist of a series of 20 millisecond intervals. Each 20 millisecond interval shall consist of 10 tests which dynamically exercise the interface signals listed below:

  • 20 V Discrete inputs

3.1.7.4   G&N LAB ALIGNMENT EQUIPMENT

3.1.7.4.1   Item definition. The table alignment equipment consists of:

  a. Auto Collimation Prism where GDSS is ordering "Wild Heerbrugg Gap 1 from Servo Co. (714-546-0606).

  b. Wild thermat T3000 electronic precision theodolite which has RS-232 input/output which allows data transfer to computers. Has built-in auto collimation.

  c. Master stand, also via Servco. Model 1009

3.1.7.5   POWER INTERFACE

Inertial tester prime power shall be supplied from a single output and shall be 120 VAC ±10%, 60 Hz.

3.1.7.5.1   <u>Uninterruptable Power Source (UPS)</u>. A 1000 watt UPS shall be provided for power backup to the three computers and their expansion chassis in the test console. Backup protection shall be provided for fifteen minutes at full power.

The UPS shall provide indication of the following:
> UPS Battery Voltage Low
> UPS Fault
> UPS Power Activated (input line voltage low or missing)

3.1.7.5.2   <u>INU Power</u>. The inertial tester shall provide the INU power as described below
> 22 to 32 VDC
> 500 watts maximum
> ripple voltage < 20 mv rms or 100 mv pp maximum

3.1.7.5.3   <u>INU Power Control</u>. Automatic control shall be provided for the following INU power states:

a. INU power off

b. INU power on (nominal)

c. Set INU voltage to 28 VDC +0.1 VDC, -0 VDC

d. Set INU voltage to 22 VDC +0.1 VDC, -0 VDC

e. Set INU voltage to 32 VDC +0.1 VDC, -0 VDC

It shall be possible to override the automatic control of the INU power from the TDS front panel. A discrete shall be provided indicating the state of the front panel INU power control override. It shall be possible to measure the INU input power voltage to within ±1%. The INU power source shall provide for over voltage and current protection. A loss of power to the autonatic control circuits shall result in removal of the INU power.

The prime power input shall be manually selectable between 20 and 32 VDC, as a minimum. The prime power input to the INU shall be 0 VDC at the inertial tester power turn on or station master clear.

An HP6032A HPIB system power supply from Hewlett-Packard shall be ordered to satisfy the above requirements and also to provide the capability of measuring the applied power supply voltage and current and putting the data on the IEEE-488 Bus.

3.1.7.6   G&N LAB SOFTWARE

3.1.7.6.1   <u>Target Lab Software</u>. Computer programs shall be written in Microsoft C 5.0 "C" language. Any required time critical code may be assembly language.

The test equipment shall tie to the Central GBT computer and shall be equipped with a proNET-80 Network Interface Board and shall appear as a workstation on the LAN.

3.1.7.6.1.1   Software Drivers. Drivers to control table functions and MIL-STD-1553 to IEEE-488 GPIB I/O for data, command and control must be written.

3.1.8   ACTUATOR TEST EXTENSION

The actuator test extension is a phase 2 potential that was eliminated from Phase 1 due to cost considerations.

3.1.8.1   ACTUATOR TEST LAB PROCESSOR AND INTERFACE UNIT

The Lab processor will be that of the GBT Core processor. The interface unit will be of the VME type.

3.1.8.2   HYDRAULIC POWER UNIT

Shall be hydraulic cart

3.1.8.3   BENCHMARK HYDRAULIC ACTUATOR

Benchmark load cells shall be a low horsepower unit.

3.1.8.4   DYNAMIC LOAD CELLS

A dynamic load cell shall be required if a dynometer cannot be supplied.

3.1.8.5   EMA POWER SUPPLY

Shall be high current sufficient to drive EMA @ 28V, 400 Hz.

3.1.9   IMAGE PROCESSING/NAV AIDS EXTENSION

Phase 2 implementation. A 3 million dollar high tech proximity simulator that could be generic real-time and flexible. See HLCV Second Quarterly Review, Thursday 22 September 1988 for details.

3.1.10 POWER SYSTEM TEST EXTENSION (PSTE)

The PSTE is a GBT extension facility capable of testing new technologies in Power Systems components and architectures. The PSTE shall contain a facility computer, a VMEbus, input/output interface chassis, a programmable load bank, a strip chart recorder, a number of precision milliammeters with various shunts to handle up to 250 amps, a number of precision voltmeters and an oscilloscope.

3.1.11 FLUIDS AND PNEUMATIC TEST EXTENSION (FPTE)

The FPTE is a GBT extension facility that contains this hardware and special test equipment to test new technologies in Fluids and Pneumatic architectures and components. The FPTE shall contain flow and pressure sensing equipment, pressure regulation equipment, electronic valves, a facility processor, a VMEbus input/output interface chassis, and bottled fluids and gases. The FPTE shall be rated for LN_2, not LO_2 and LH_2 since LO_2 and LH_2 present an explosive hazard and the Lab is in close proximity to other labs and a great number of people. The extension facility shall have thick safety walls and a pressure pit for this high pressure LN_2. The facility shall also be capable of running remote when operating with the high pressure. Figure 3.1.11-1 shows a diagram of the General Dynamics Fluids and Pneumatic SIL layout.
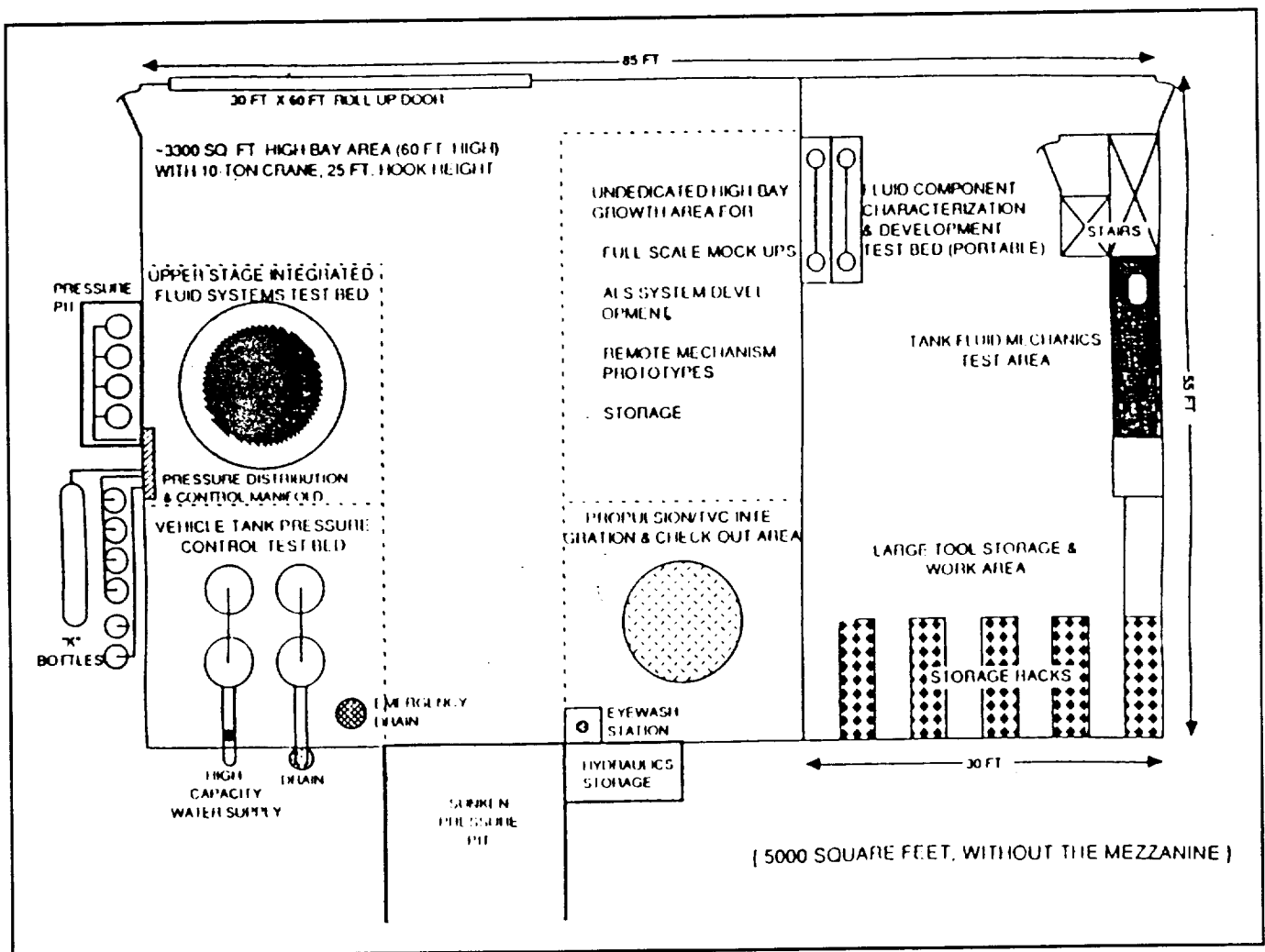

Figure 3.1.11.   Fluids SIL Layout

3.1.12 SOFTWARE   DEVELOPMENT   FACILITY

The software development facility is defined as that portion of the lab in which development of simulation software (as opposed to flight software) occurs. During Phase 1, the facility may be co-located within the simulation facility. The lab Target Configuration shall include a separate software development facility.

3.1.12.1   SOFTWARE DEVELOPMENT WORKSTATIONS

3.1.12.2   DATA STORAGE AND REPRODUCTION FACILITIES

3.1.12.3   NETWORK/BUS FACILITIES

3.1.12.4   SOFTWARE DEVELOPMENT TOOLS

As a minimum, the software development tools shown in figure 3.1.12.4-1 shall be provided.

- **4 PC based 25 MHz 386 workstations with 5 MIP throughput and 300 MByte disk**
  - **4 MBYTE memory expansion**
  - **30387 and/or Weitek co-processor**
  - **Video graphics extension**
- **Line Printer**
- **Laser Printer**
- **Local Fiber Optic Star Network linking to Main Processor**

- **MS OS standard version 1.0**
- **Microsoft windows**
- **Microsoft "C" compiler**
- **Microsoft macro assmbler**
- **Pronet to PC software**
- **Pronet to VME software**

- **Develop and run software in remote location or on main processor nodes**
- **Develop and test graphics**

Figure 3.1.12.4-1.   Environment/Systems Simulation
Resource & Facilities Requirements Summary

4.0   APPENDIX

4.1   HLCV GBT WORK BREAKDOWN TREE STRUCTURE

WBS Task No.	SOW Task No.	WBS No.	PDD ELEMENT SPECIFICATION	Outline No.
1000	5.1	1/1	HEAVY LIFT CARGO VEHICLE PROGRAM	2.0
—	—	1/2	—	
3000	5.3	/12	Flight Vehicle	
3000	5/3	1/2	System Test and Evaluation	
—	—	3	—	
	(NA)	3	Flight Test	
4000	5.4	1/3	Ground Test (Ground-Based Lab)	
6000	6.0	1/4	GBL Management	
5000	5.5	2/4	Systems Engineering (Design & Integration)	3.0
5000	5.5	3/4	Activation	
5000	5.5	4/4	Test Facilities	
5000	5.5	4.1/4	Facility A&#	
5000	5.5	4.2/5	Facility Construction	
5000	5.5	4.3/5	Facility Equipment	
4000	5.4	5/5	Test Equipment and Computers	3.1.2
4000	5.4	5.1/5	Primary Lab Computer	
4000	5.4	5.2/5	Primary Lab Data Storage Units	
4000	5.4	5.3/5	Avionics System Simulation Computer	
4000	5.4	5.4/5	Graphics Processor	
4000	5.4	5.5/5	Avionics System Workstations	
4000	5.4	5.6/5	Avionics Hardware Support & Interface Assy	
4000	5.4	5.7/5	Avionics Benchmark Hardware	
4000	5.4	5.8/5	Demonstration Center Control & Display H/W	
4000	5.4	5.9/5	Inertial Instrument Test Assy	
4000	5.4	5.10/5	Flight Control Sensor Test Assy	
4000	5.4	5.11/5	Actuator Dynamic Test Assy	
4000	5.4	5.12/5	Fluids & Pneumatics Test Assy	
4000	5.4	5.13/5	Power System Test Assy	
4000	5.4	5.14/5	Instrumentation Sys Processing & Test Assy	
4000	5.4	6/4	Test Software	3.16-.12
4000	5.4	6.1/5	G&N	
4000	5.4	6.2/5	Environment/Vehicle	
4000	5.4	6.3/5	Navigation Aids	
4000	5.4	6.4/5	Demo Control Center	
4000	5.4	6.5/5	Hot Bench	
4000	5.4	6.6/5	Communication & Instrumentation	
4000	5.4	6.7/5	Ground Support Equipment	
4000	5.4	6.8/5	Flight Control	
4000	5.4	6.9/5	Propulsion	
4000	5.4	6.10/5	Fluids & Pneumatics	
4000	5.4	6.11/5	Other	
6000	6.0	7/4	Test Operations and Support	
6000	6.0	7.1/4	Test Conductance/Evaluation	
6000	6.0	7.2/4	Test Utilities/Services	

4.2   SPECIFICATION TREE

Level No. 1.0   Heavy Lift Cargo Vehicle

This Work Breakdown Structure (WBS) element encompasses the complete life cycle cost (LCC) of the Heavy Lift Cargo Vehicle (HLCV) system. LCC includes the cost of system RDT&E, Production (nonrecurring and recurring) and/or Procurement, and Operations and Support. The HLCV system consists of one or more launch vehicle systems, such as Shuttle C and the Advanced Launch Systems, and the effort needed to combine these systems into an integrated space program which meets future heavy lift cargo requirements. For this study, only the HLCV Ground-Based Lab (GBL), under the System Test and Evaluation WBS element, is included in the cost estimate at this time. Costs allocated to the O&S phase are not included in this estimate.

Level No. 1.0   Flight Vehicle

This WBS element refers to the launch vehicle sin the HLCV program. These vehicles may be of a single-stage or multiple stage configuration. The elements includes the cost of launch vehicle design, development and production. Launch vehicle testing is included under the System Test and Evaluation WBS element. The Flight Vehicle WBS element is not included in the HLCV GBL cost estimate.

Level No. 1.0   System Test and Evaluation

The System Test and Evaluation element refers only to the prototype, pathfinder, or specifically fabricated hardware utilized in system-level tests to obtain or validate engineering data on the performance of the HLCV program. This element includes all material and effort required for the detailed planning, test conduction, support, data reduction, and documentation from such operations. Also included is all effort associated with the design and production of models, specimens, fixtures and instrumentation in support of the test program. Product acceptance testing is excluded from this WBS element and should be included under the appropriate hardware category. Component-level (card-level) acceptance and miscellaneous other testing which is directly associated with lower hardware or software elements may be included in this category. Costs accrued under this WBS element should be allocated to the program phase in which the effort occurs.

Level No. 1.0   Flight Test

This WBS element refers to the effort required to flight test vehicles within the HLCV program. This cost is not included in the HLCV Avionics cost estimate.

Level No. 1.0   Ground Test

This element refers to all effort relating to system ground testing of the HLCV program. In particular, this element includes the cost of design, construction and activation of a Ground-Based Lab (GBL) built to test HLCV avionics hardware and software. Ground testing of other vehicle elements is excluded from the HLCV GBL cost estimate.

Level No. 1.0   GBL Management

The project management element refers to the integration of the GBL from the technical and administrative planning, organizing, directing, coordinating, integrating, controlling and

approval actions designated to accomplish overall project objectives which are not included in the Systems Engineering element. Examples of these activities are maintenance management, transportation and shipping management, cost/schedule/ performance management, contract management, data management, vendor liaison, contract WBS, etc. Project Management applies to all phages, with allocation determined by the phase in which the effort is performed.

Level No. 2.0   Systems Engineering

The Systems Engineering element refers to the technical engineering effort involved in the design and integration of GBL facilities, equipment, hardware, software and operations. System Engineering applies to all phases, with allocation determined by the phase in which the effort is performed.

Level No. 3.0   GBL Activation

This WBS element refers to the effort involved in activating, checking out and validating the GBL and preparing it for operation, including but not limited to installing and testing hardware and software prior to initial testing activities. GBL Activation cost is allocated to the nonrecurring cost phases.

Level No. 4.0   Test Facilities

This WBS item refers to the design and development, site purchase or lease, and construction or modification of a site or building or provide HLCV avionics testing facilities (BGL). These facilities are required for the performance of the various developmental tests necessary to prove the design and reliability of specific systems or subsystems.

Level No. 4.1   Facility A&E

This element refers to the architectural and engineering design effort required for construction/modification of a GBL facility. Facility A&E costs are allocated to the RDT&E phase.

Level No. 4.2   Facility Construction

This WBS element refers to the material and labor required to construct a new facility or to modify an existing facility into a GBL. Included are site purchase or lease, permanently installed equipment and utilities such as plumbing, water and air conditioning. Portable equipment is included in the Facility Equipment WBS element. Facility construction costs are allocated to the RDT&E phase. Facility maintenance is allocated to the O&S phase.

Level No. 4.3   Facility Equipment and Computers

This element refers to operable equipment/furnishings and computer hardware/software which is installed after facility construction and which is not designed specifically for HLCV avionics testing purposes. General office furniture, equipment and personal computers, if not used primarily for testing, are included in this category. Procurement of facility equipment is allocated to the RDT&E phase. Facility equipment maintenance is include din the O&S phase.

Level No. 5.0   Test Equipment

This WBS item refers to the design, development, production, procurement (if applicable) and maintenance of all equipment specific to the system test effort. General office furniture and

equipment not specifically designated for the test effort should be included in the Facility Equipment and Computer WBS element. Test equipment design, development, production and/or procurement is allocated to RDT&E. Equipment maintenance is included in the O&S phase.

Level No. 5.1   Primary Lab Computer

This WBS item refers to the mainframe processor which controls lab operations and provides demonstration capability of test results.

Level No. 5.2   Primary Lab Data Storage Units

This item refers to the mass storage units associated with the mainframe processor in WBS 6.1. Simulation models and test results reside on such units.

Level No. 5.3   Avionics System Simulation Computer

This WBS element refers to the processor which performs the simulations for avionics system testing.

Level No. 5.4   Graphics Processor

This element refers to the processor which provides graphics capability for test demonstrations and displays.

Level No. 5.5   Avionics System Workstations

This WBS item refers to the computer workstations which provide lab users with access to either the avionics systems simulator or the main processor.

Level No. 5.6   Avionics Hardware Support and Interface Assembly

This item refers to the interface equipment needed to support a hot bench capability for the GBL. Examples of such items might be a vehicle bus, instrumentation bus or I/O processor.

Level No. 5.7   Avionics Benchmark Hardware

Avionics hardware required for benchmark testing is listed in this category. Example pieces of hardware might include inertial navigation units (INUs), rate gyro units (RGUs), remote voter units (RVUs) or master data units (MDUs).

Level No. 5.8   Demonstration Center Control and Display Hardware

This WBS element refers to any equipment required to support the Demonstration Control Center other than the main processor, avionics system computer, graphics processor and computer workstations included in other WBS elements. Display monitors, data recorders and communications and control networks are listed here.

Level No. 5.9   Inertial Instrument Test Assembly

This element refers to the equipment necessary to support guidance and navigation development. Equipment such as three-axis table with optical alignment and thermal capabilities would be included in this category.

Level No. 5.10   Flight Control Sensor Test Assembly

This WBS item refers to the equipment needed to test flight control systems.

Level No. 5.11   Actuator Dynamic Test Assembly

This element refers to the equipment required to test actuators in the GBL. This category includes such items as load cells, interface cards and sensors.

Level No. 5.12   Fluids and Pneumatics Test Assembly

This WBS element refers to the equipment necessary to develop fluid and pneumatic system controls. Fluid and pneumatic controllers and load racks are listed here.

Level No. 5.13   Power System Test Assembly

This item refers to the equipment needed to test power systems.

Level No. 5.14   Instrumentation System Processing and Test Assembly

This WBS item refers to the equipment required to develop systems which measure the performance of critical system elements. Such equipment might include instrumentation cards, data processing cards, and I/O processing cards.

Level No. 6.0   Test Software

This item refers to the design, development, validation, procurement (if applicable) and maintenance of all software specific to the system test effort. Software not used primarily for testing purposes is included in the Facility Equipment and Computers WBS element. Test software development, validation and procurement is included in the RDT&E phase. Software maintenance is include in the O&S phase.

Level No. 6.1   Guidance and Navigation Software

This element refers to the software required to support guidance and navigation system development. An IMU model might be an example of G&N software.

Level No. 6.2   Environment/Vehicle Software

This WBS element refers to the software which simulates system environments, vehicle dynamics and mission phases. Launch/ascent, on-orbital, re-entry and acceleration models might be included in this category.

Level No. 6.3   Navigation Aids Software

This item refers to the software needed to provide navigational support for lab operations and to demonstrate navigational systems. GPS and image processing models are included here.

Level No. 6.4   Demonstration Control Center Software

This WBS item refers to the software necessary to control lab operations and to provide demonstrational capability of test results. Operating systems, data base and resource managers, simulation control programs and graphics development software would be listed in this category.

Level No. 6.5   Hot Bench Software

This element refers to the software required to simulate generic avionics hardware such as RGUs and RVUs.

Level No. 6.6   Communication and Instrumentation Software

This WBS element refers to the software necessary to support development of communication and instrumentation avionics. Such software might simulate transmitter and receiver hardware.

Level No. 6.7   Ground Support Equipment Software

This item refers to the software needed to test avionics GSE, Computer-Controlled Launch Set (CCLS), Integrated Health Monitoring (IHM) and expert systems software are included in this category.

Level No. 6.8   Flight Control Software

This WBS item refers to the software which manages flight control systems test equipment. This category would include software simulations of actuators, controllers, reaction control systems and aerosurfaces.

Level No. 6.9   Propulsion Software

This element refers to the software required to test propulsion control systems. Engine simulation models are included here.

Level No. 6.10   Fluid and Pneumatic Software

This WBS element contains software simulations of fluids and pneumatic systems.

Level No. 6.11   Other Software

This item refers to test software not included in previous categories, such as Liquid Rocket Booster (LRB) and Solid Rocket Booster (SRB) simulations.

Level No. 7.0   Test Operations and Support

This WBS element refers to the operations and services required to run the system test effort. All costs in this category are allocated to the O&S phase. This element is not included in the HLCV GBL cost estimate.

Level No. 7.1   Test Conductance/Evaluation

This element refers to all effort required to perform the system testing.

Level No. 7.2   Test Utilities/Services

This WBS item refers to any material and effort that supports test activities but is not included under direct test support in WBS 1.Y.B.7.1. Examples included leased computer or satellite services.