N90-19446

TDA Progress Report 42-99

November 15, 1989

Big Viterbi Decoder (BVD) Results for (7,1/2) Convolutional Code

J. Statman, J. Rabkin, and B. Siev
Communications Systems Research Section

The Big Viterbi Decoder (BVD), capable of decoding convolutional codes with constraint lengths of up to 15, is under development for the DSN. As part of the development, a commercial single-chip (7,1/2) Viterbi decoder is used to enable early start of system integration. Tests of the integrated partial system (including simulator, input interfaces, output interfaces, and computer controls) were recently completed at the DSN Compatibility Test Area (CTA-21) at JPL. This article describes the system elements used for the demonstration and test results.

I. Introduction

The Big Viterbi Decoder (BVD) is under development for the Deep Space Network (DSN) [1]. It is intended to provide up to 1.8 dB improvement in link margin through the use of convolutional codes with larger constraint lengths. Specifically, the BVD is designed to operate with any convolutional code with constraint length of $K \leq 15$ and code rates $1/2, 1/3, \ldots, 1/6$. In contrast, the current equipment is designed for the standard DSN code, $K = 7$ and rate $1/2$. The BVD prototype will be used in a May 1991 demonstration in conjunction with the Galileo mission. Following a successful demonstration, the decoder will be inserted into the DSN for use with Galileo and future missions.

A block diagram of the BVD, as initially planned, is shown in Fig. 1(a). The core of the decoding processing is performed in the Processor Assembly using 256 or 512 identical custom VLSI chips. All the other functions are performed in the Controller Assembly. These include transforming of input soft symbols, buffering data to the Processor Assembly, interfacing to output devices, and providing full self-test capability. Early on it was recognized that the Processor Assembly, especially the VLSI chips, is the time-critical element in the development schedule since no meaningful DSN-compatibility tests could be conducted without having a "decode" capability, which requires a full Processor Assembly. To overcome this bottleneck, a secondary "decode" path was introduced as shown in Fig. 1(b). The additional path uses a commercial QUALCOMM Q1401 (7,1/2) decoder chip and enables testing of many BVD functions well before the Processor Assembly is ready. A partial BVD, shown in Fig. 1(c), was completed and tested in the laboratory and in the DSN Compatibility Test Area (CTA-21) at JPL,

verifying decoder operation for (7,1/2) code and current DSN interfaces.

II. Functional Block Description

The system under test consists of a MULTIBUS I chassis with six boards: an Intel 80386/21 CPU and five custom digital boards. Figure 2 shows a more detailed functional block diagram of the five custom boards. These boards include functions required in DSN operation, as well as functions needed during development and testing. Some of the latter are especially critical during diagnostics and fault isolation, enabling failures to be traced to a specific board. The following is a description of these functions, by board.

A. Memory Board

This board includes 1 Mbyte of Electrically Erasable Programmable Read-Only Memory (EEPROM) and is used for object code and key parameter storage. It enables the BVD to accept program updates without a major interruption: the new code is downloaded from an IBM PC/AT computer into RAM and stored in the EEPROM. Upon reset, the program is read from the EEPROM into RAM and executed. This approach eliminates the operational problems associated with removing boards and replacing EPROMs (which must be erased under an ultraviolet light). The board also stores critical mission parameters to allow easy restart after a power glitch. If additional memory is required, multiple boards can be installed.

B. Encoder Board

The encoder (simulator) board provides a flexible source for encoded data test sequences for BVD self-test. In operation, a fairly comprehensive self-test with several million bits can be run at 1.1 Mbit/sec, requiring only a few seconds. The board includes an uncoded data source, encoder, and circuitry that gets calibrated noise samples from an external noise source. All functions are fully programmable. Simulated symbols are generated by passing bits from a programmable sequence generator through an encoder, and summing them with properly scaled noise. The encoder is implemented as a computer-loaded RAM, where each state of the encoder shift-register corresponds to an address of the RAM. This allows implementing of any convolutional encoder for $K \leq 15$ and $1/n$, $n \leq 6$ through a single computer loading of the RAM.

Other functions that the board performs are monitoring the mean and variance of simulated noise samples (received from an external source), generation of simulated bit and symbol clocks, and transfer of simulated bits to the comparator board.

C. SSA/BBA Interface Board

This board includes circuitry that generates system clocks, interfaces to the Symbol Synchronizer Assembly/ Baseband Assembly (SSA/BBA) for input symbols, reclocks input signals, and interfaces to the Time Code Translator (TCT) for time tagging. It also provides a simulated symbol RAM that allows testing of the SSA/BBA interface.

D. SNR Estimator Board

The circuitry on this board collects data for symbol signal-to-noise ratio (SNR) estimation. The approach is similar to that used in the Symbol Stream Combiner (SSC)[1] and requires computation of sum-of-squares and sum-of-absolute-values of the received symbols. Computing symbol SNR internal to the BVD provides an important diagnostic tool as well as a monitor of BVD health during real-time operation.

The board includes a scale RAM and an alternate symbol sign-flipper to allow for computer-controlled adjustment of these symbol attributes. The scale RAM allows one to scale the input symbols by a constant, which also enables testing for possible inversion in the SSA/BBA (the Galileo (15,1/4) code is nontransparent). The alternate symbol sign-flipper is required to compensate for the sign flipping used in encoders on board most JPL spacecraft. Another feature on this board is a coded data test RAM that allows the CPU to read and store symbols from either the SSA/BBA (in real time) or the simulated signal generated by the encoder board.

The board also includes provisions for future interfaces to the DSN through a First-In, First-Out (FIFO) buffer. This interface will be utilized when the new Telemetry Processor Assembly (TPA), currently under development, is sufficiently defined.

E. Comparator Board

The comparator board includes a (7,1/2) Viterbi decoder, a comparator that allows bit error rate (BER) data

[1] S. Dolinar, "A Lot of Things You Always Wanted to Know About Signal-to-Noise Estimation Methods (but Didn't Bother to Ask)," JPL Interoffice Memorandum 331-85.2-109 (internal document), Jet Propulsion Laboratory, Pasadena, California, January 22, 1986.

collection, symbol rate estimation circuitry, and various output interfaces.

The (7,1/2) Viterbi decoder section is centered on a QUALCOMM Q1401 commercial chip, and includes additional circuitry to provide for computer-controlled node synch. The Q1401 is designed for the Goddard (7,1/2) code, which uses the same polynomials as the DSN code but in a reversed order. A circuit that allows the BVD to operate with either polynomial order had been designed but had not been installed during the tests. It will be tested separately later.

The comparator function compares the decoded bit stream to a delayed version of the simulated unencoded bit stream. It includes a variable-delay buffer (used to align the two streams) and a set of counters that allows for collection of data for BER versus E_b/N_0 evaluation.

The output interface circuit receives decoded bits and status data from the (7,1/2) decoder chip or from the Processor Assembly, records these in a test RAM, and channels the data to external devices through a Frame Synchronization Subsystem (FSS) driver or a FIFO. The FIFO will be used for interface to the new TPA. An optional differential decoder is also part of the output circuit.

F. Other Boards

To complete the BVD, several more boards will be designed and manufactured. The Controller Assembly will have two more boards: the Processor Assembly Interface board and the Node Synch board. The Processor Assembly will have seventeen boards mounted in a complex custom backplane. The backplane is being designed and manufactured by Teradyne Connector Systems to JPL specifications, while the seventeen boards are being designed by JPL. Sixteen of these boards will be identical and will house custom VLSI chips, while the seventeenth will perform traceback and interface functions.

III. Laboratory and CTA-21 Test Results

Tests were conducted in the laboratory and in CTA-21 to validate BVD operation and compatibility with the DSN. It is important to note that as DSN interfaces are upgraded, similar tests will need to be conducted with the new interfaces. However, the interfaces validated here are the minimal set needed for the planned 1991 demonstration in DSS-14, namely symbol input from SSA/BBA and command/control through an RS232 to a terminal.

During the CTA-21 test, the BVD was connected as part of a telemetry string (Fig. 3). The test was conducted at high SNR and the BVD was connected to the station's SSA, replacing the current maximum-likelihood convolutional decoder (MCD). Successful decoding was demonstrated for several input sequence formats. The test used the Goddard code, i.e., reverse order for code polynomials, and will be repeated when the circuit is modified to handle both the DSN and Goddard codes. However, the key objective of verifying DSN compatibility was achieved.

IV. Conclusions

A partial BVD was constructed that has the capability to decode (7,1/2) convolutional codes. It was demonstrated in the laboratory and in the CTA-21 environment, validating DSN compatibility for the planned May 1991 demonstration.

Reference

[1] J. Statman, G. Zimmerman, F. Pollara, and O. Collins, "A Long Constraint Length VLSI Viterbi Decoder for the DSN," *TDA Progress Report 42-95*, vol. July–September 1988, Jet Propulsion Laboratory, Pasadena, California, pp. 134–142, November 15, 1988.

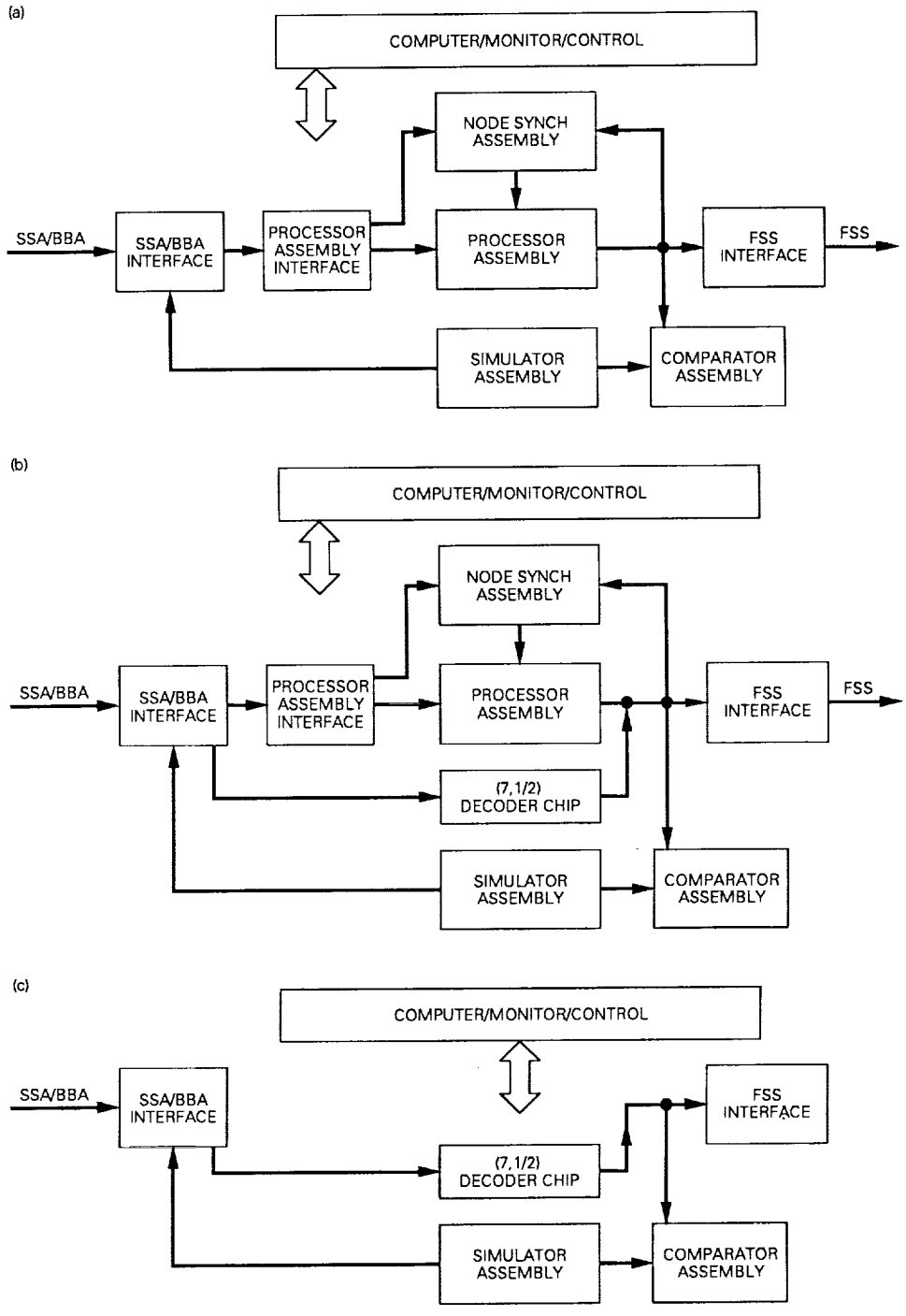

Fig. 1. Functional block diagram of Big Viterbi Decoder: (a) original, (b) modified to include (7,1/2) decoder chip, (c) during test.

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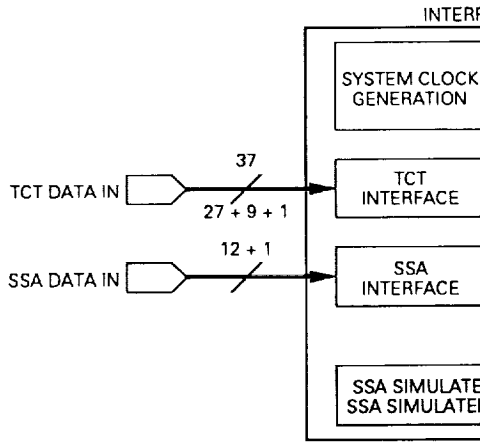

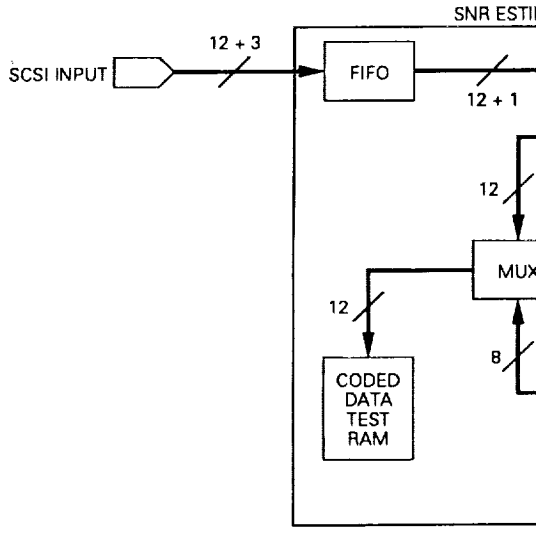

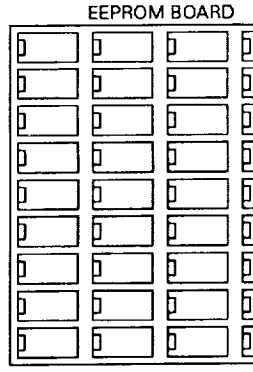

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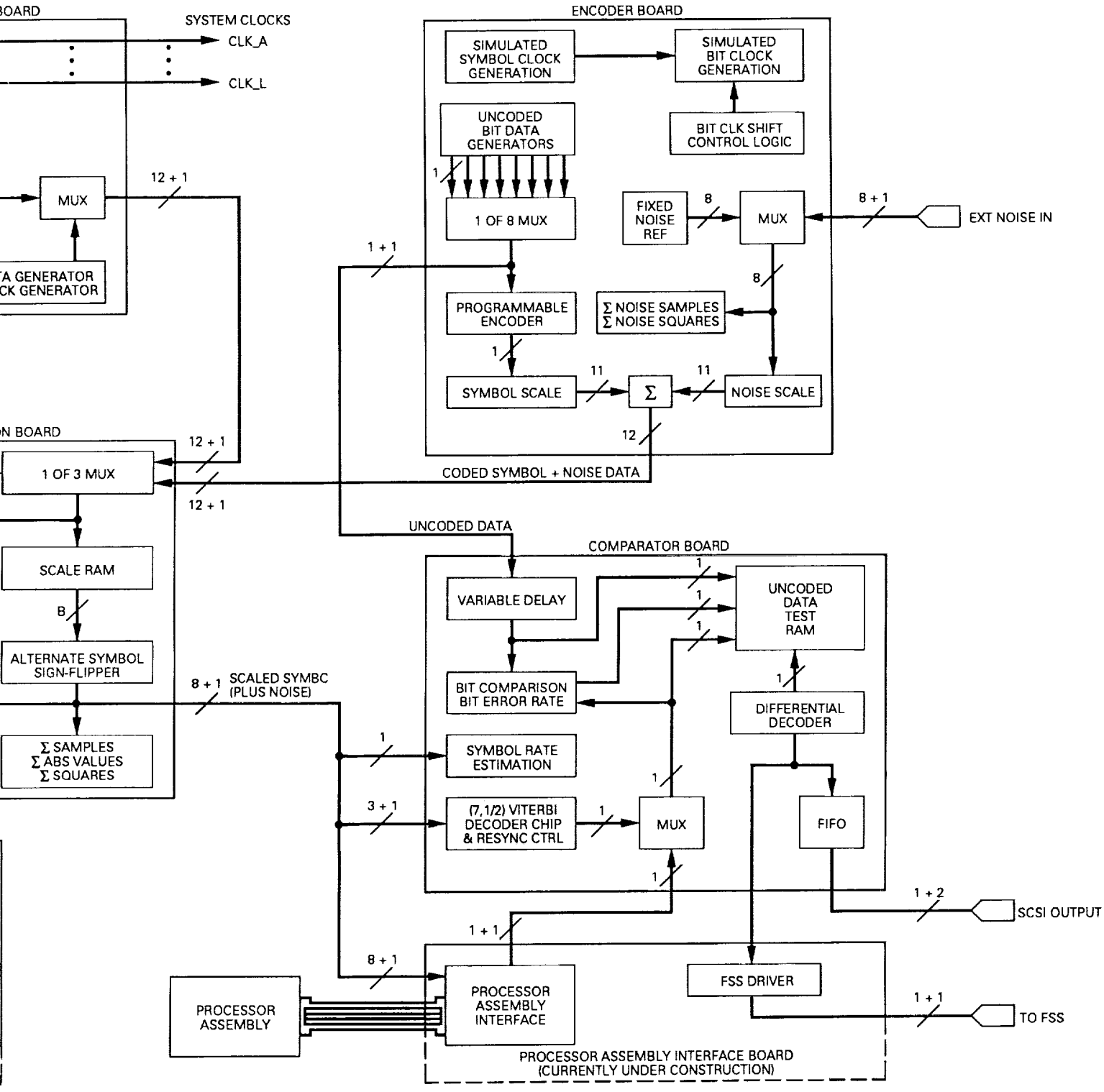

Fig. 2. Detailed block diagram of Big Viterbi Decoder.

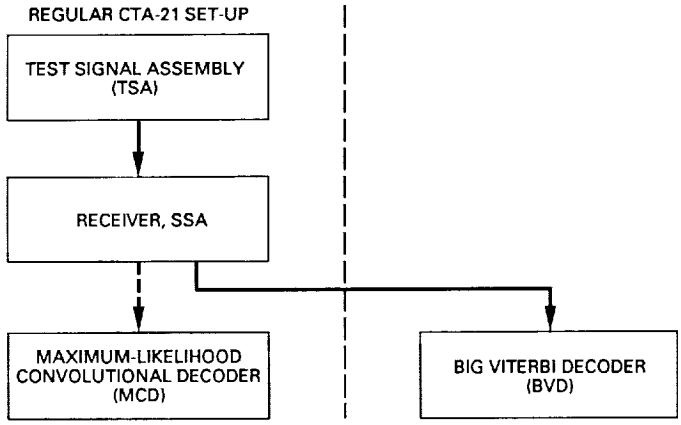

Fig. 3. CTA-21 test setup.