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Product Assurance Technology for Procuring Reliable, Radiation-Hard, Custom LSI/VLSI Electronics

Report for Period: October 1984 – September 1986

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Prepared for

Defense Advanced Research Projects Agency,
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Abstract

In this effort, advanced measurement methods that use microelectronic test chips are described. These chips are intended to be used in acquiring the data needed to qualify Application Specific Integrated Circuits (ASICs) for space use. This work represents the collaborative effort of integrated-circuit (IC) parts specialists, device physicists, test-chip engineers, and fault-tolerant-circuit designers. Their efforts were focused on developing the technology for obtaining custom ICs from CMOS/bulk silicon foundries. In pursuit of this goal a series of test chips has been developed: a Parametric Test Strip, a Fault Chip, a set of Reliability Chips, and the CRRES (Combined Release and Radiation Effects Satellite) Chip, a test circuit for monitoring space radiation effects.

The technical accomplishments of this effort include:

1. Development of a Fault Chip that contains a set of test structures used to evaluate the density of various process-induced defects. In addition, procedures were developed to determine which defects are most likely to cause failures in concurrently fabricated circuits. In the reporting period, seven versions of the fault chip have been prepared.

2. Development of new test structures and testing techniques for measuring gate-oxide capacitance, gate-overlap capacitance, and propagation delay.

3. Development of a set of Reliability Chips that are used to evaluate failure mechanisms in CMOS/Bulk: interconnect and contact electromigration and time-dependent dielectric breakdown.

4. Development of MOSFET parameter extraction procedures for evaluating subthreshold characteristics.

5. Evaluation of Test Chips and Test Strips on the second CRRES wafer run. This data was used to analyze wafer-level test structure requirements demonstrating that sufficient data to characterize the wafer run could be acquired from a limited number of drop-in sites (for example, nine).

6. Two dedicated fabrication runs for the CRRES Chip flight parts. Flight parts from these runs were shipped to the CRRES program in March, 1986. Radiation tests (Total Integrated Dose and Single Event Upset) were performed on these parts.

7. Publication of two papers: one on the Split-Cross Bridge Resistor and another on Asymmetrical SRAM Cells for Single-Event Upset Analysis.

Acknowledgements

The present address of C. A. Piña is University of Southern California/Information Sciences Institute, Marina del Rey, California and the present address of G. A. Jennings is Department of Computer Engineering, University of Lund, Sweden.

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Chapter 1

Introduction

The goal of this effort is to develop a product assurance methodology that will allow the procurement of reliable, radiation-hard, custom LSI/VLSI circuits from silicon foundries and permit their use in critical applications such as spacecraft.

The use of test chips by integrated circuit manufacturers and customers is widespread for they are essential for process control, for quantifying reliability parameters, and for providing a basis for wafer acceptance. Currently, test chips are being contemplated for use in the military standards system as a means of evaluating the quality of a manufacturing process. This approach promises to allow the qualification of custom and Application-Specific Integrated Circuits (ASICs) in a timely and cost-effective manner.

This report describes a CMOS Product Assurance Technology to characterize and evaluate particular foundry runs which is based on one test strip and three test chips: the CMOS Process Monitor Test Strip used to characterize process parameters and to extract SPICE parameters, the Fault Chip used to analyze initial defect density and to identify the most common defect type, the Reliability Chip used to characterize the expected long-time reliability and to identify the expected long-time failure modes, and the CRRES Chip used to characterize the response of the fabrication to radiation. The CRRES (Combined Release and Radiation Effects Satellite) will be launched in the early 1990s. Its Microelectronics Package (MEP) contains 12 JPL-designed chips to analyze the effect of radiation on microelectronics. This family of structures and the associated test methodology form the basis for integrated circuit qualification procedures.

One key element in this methodology is the development of statistical procedures to determine sample size and frequency, parameter distribution functions, and outlier exclusion methods. This is important due to the limited area of a wafer which is available for use for test structures. As part of this effort we developed a special test structure to measure contact resistance which allows the statistical characterization of 464 contacts of four different types using a much smaller area than that needed for individually probed contacts. This "smart" test structure, incorporating row and column addressing, allows individual access to all 464 contacts. Simulation study of the Time-Dependent Dielectric Breakdown Structure revealed that 1600 or more test structures must be analyzed in order to minimize errors in predicting time to failure values.

Another key element in this methodology is the establishment of a parameter data base. This allows one to compare parameter mean and standard deviation values with those measured on previous runs, and to decide if the parameters are on target and if the process tolerances used to characterize them are acceptable. As part of this effort, test chips on an entire 3-μm CMOS/Bulk p-Well wafer

run were evaluated. For this particular run, the lot tolerances were: for the gate linewidth, 0.18 μm, for the threshold voltage, 0.017 mV, and for the conduction factor, 7 percent. From Cobalt 60 testing, the radiation damage factor was found to be about 32 mV/krad(Si). In our estimation, these are excellent values for microelectronics intended for use in a natural space environment.

A final element in this methodology is the development of innovative test structures that allow one to quickly measure key parameters. During this period three structures of note were developed: (a) the contact resistor matrix mentioned above, (b) the gate-oxide capacitor (round and race track versions) and (c) electromigration test structures (a 15-segmented structure for metal, and a 16-element string for contact evaluations).

In order to "exercise" the product assurance technology, a chip was designed for the CRRES MEP and two dedicated foundry runs undertaken for these parts. On each foundry run Process Monitor Test Strips and drop-in Test Chips (containing a set of structures from the Process Monitor and the Fault Chip) were included alongside the CRRES Chips. From the second run, four 3-μm CMOS p-Well wafers were analyzed in detail. Numerous parameters were mapped across the wafers and results obtained from nine drop-ins were compared with those from about 90 Process Monitors. This analysis led to the conclusion that nine sites placed in a 3×3 grid are sufficient to characterize the wafer and to distinguish acceptable wafers from unacceptable wafers for current CMOS processing.

The reader is encouraged to study the following report. For those with questions, the technical staff of the VLSI Technology Group is happy to discuss technical details and can be reached at (818) 354-2083.

Chapter 2

Test Chip Sets

2.1 Introduction

As a result of the Product Assurance Technology (PAT) effort over the past several years, a set of test structures has been developed to provide the information required to evaluate custom or semi-custom VLSI circuits. In the conduct of this effort, it has become evident that an efficient method that prepares the methodology for industrial use is to develop test chips, each of which is designed for a specific application or use. To this end, we have developed three general families of test chips: a parametric test chip, a fault test chip and a reliability chip. Although individual test structures can be added or deleted from these chips if necessary, their composition is adequate to cover the CMOS critical parameter set [1]. Geometrical descriptions of these chips in Caltech Intermediate Form (CIF) can be easily generated for different design rule sets using the JPL Test Chip Assembler (TCA).

In this section we list the parameters needed to perform wafer or lot evaluations, as well as those required to model the behavior of devices and/or circuits. These parameters are determined from specially designed test structures. Although the list of parameters is large, less than twenty morphologically different types of test structures are needed to extract the required set. Table 2.1 lists the critical parameters and the structures used to obtain the parameters. The symbols for each test structure are explained in Table 2.2. The parameters are arranged into the following six categories which were first described elsewhere [1] and have proven to be a good classification scheme:

1. PROCESS PARAMETERS. These parameters are used to monitor the stability of a process by measuring those parameters of a manufacturing process that determine some of the significant process variables such as dopant concentrations, oxide thickness, linewidth control of the different layers, and interlayer contact resistances. Some of these same quantities are required as inputs by the level 2 and 3 SPICE MOSFET models used in circuit and device simulation. The structures used to determine these parameters and the test methods used are described in the previous PAT final report [2] and in Sections 3.1 and 3.4 of this report.

2. DEVICE PARAMETERS. The majority of these parameters are obtained from measurements of the simplest device found in MOS circuits: the MOSFET. The device parameters provide process control information and are used as inputs to device and circuit simulation programs. The test structures and test methods used to determine these parameters are described in the previous PAT final report [2].

Table 2.1: Critical parameters and associated test structures.

Parameters	Test Structure Abbreviation
1. Process Parameters	
1.1 Layer Sheet Resistance	XBR
1.2 Layer Linewidth	XBR, SXBR
1.3 Metal-Layer Contact Resistance	CR, CR-ARR
1.4 Oxide Thickness	CAP, RO-TR
1.5 Substrate Dopant Density	CAP, TR
1.6 Field Oxide Threshold Voltage	TR
1.7 Layer-layer Alignment	ALI
1.8 Junction Breakdown Voltage	TR, DI
1.9 Bulk Resistivity	PFPR
1.10 Bulk Lifetime	DI, CAP
1.11 Gate Oxide Breakdown	CAP
2. Device Parameters	
2.1 VTO (Threshold Voltage)	TR
2.2 Gamma (Body Effect Factor)	TR
2.3 KP (Conduction Factor)	TR
2.4 WE (Effective Channel Width)	TR
2.5 LE (Effective Channel Length)	TR
2.6 Lambda (Channel Length Modulation)	TR
2.7 IDSO (Channel Leakage Current)	TR
2.8 IDBLEAK (Source-Drain Diode Leakage)	TR
2.9 VDBBD (Source-Drain Diode Breakdown)	TR
2.10 CGSO (Gate-Source Capacitance)	RTR-TR, ROTR
2.11 CGBO (Gate-Body Capacitance)	RTR-TR, ROTR
2.12 CGDO (Gate-Drain Capacitance)	RTR-TR, ROTR
2.13 CJ (Junction Capacitance)	RTR-DI
2.14 MJ (Exponential Factor)	RTR-DI
2.15 CJSW (Junction Sidewall Capacitance)	RTR-DI
2.16 MJSW (CJSW Exponential Factor)	RTR-DI
2.17 VPT (Punch-through Voltage)	TR
2.18 VBG (Gate-Oxide Breakdown Voltage)	CAP

Table 2.1: Critical parameters and associated test structures (Continued).

Parameters	Test Structure Abbreviation
3. Circuit Parameters	
3.1 VH (Inverter VHIGH)	INV, INV-ARR
3.2 VL (Inverter VLOW)	INV, INV-ARR
3.3 VINV (Inverter VIN = VOUT)	INV, INV-ARR
3.4 GAIN (Inverter Gain)	INV, INV-ARR
3.5 VNM (Inverter Noise Margin)	INV, INV-ARR
3.6 Tau (Gate Delay)	RO, TS
4. Layout Rules	
4.1 Layer Linewidth	XBR
4.2 Layer Spacing	SXBR, CS
4.3 Contact Size	CR
4.4 Poly Gate Extension Over Field Oxide	TR, CS
4.5 Metal Overlap of Contact	CR, CS
4.6 Active Area Overlap Of Contact	CR
5. Defect Density	
5.1 Oxide Defects	CAP-ARR
5.2 Layer Bridging	CMB
5.3 Open Layer at Step	STP
5.4 Contact Resistance	CR, CR-ARR
5.5 Inverter Variability	INV-ARR
6. Reliability	
6.1 Time-Dependent Dielectric Breakdown	TDDB
6.2 Radiation Hardness	RO-TR
6.3 Electromigration	CR, CMB
6.4 Oxide Instabilities	TR, CAP
6.5 Contact Reliability	CR, CR-ARR
6.6 Latch-Up	LUTR

Table 2.2: Abbreviations used for the parametric test structures.

Abbreviations	Structure
ARR	Array
CAP	Capacitor
CMB	Comb structure
CS	Collision structure
CR	Contact resistor
DI	Diode
INV	Inverter
LUTR	Latch-up transistor
RO	Ring oscillator
RO-TR	Round, Annular transistor
RTR	Racetrack transistor
TDDB	Time dependent dielectric breakdown
TR	Transistor
TM	Timing sampler
STP	Step structure
XBR	Cross-bridge resistor

3. CIRCUIT PARAMETERS. These parameters, which are essential to the circuit designer, provide timing information in the form of gate delay measurements for circuit simulation. Typically these parameters are determined using an inverter or a simple combination of inverters, such as a ring oscillator. Other simple gates or combinations of simple gates may be used to obtain the timing information so essential to circuit design. The structures used to determine these parameters and the test methods used are described in Section 3.2 of this report.

4. LAYOUT RULES. The information provided by these measurements is important to both circuit designer and circuit user. The parameters in this group determine whether or not a circuit can be designed using a given set of layout rules. Although their prime purpose is not that of process control, these parameters can provide important information on the ability of a given manufacturing process to consistently produce devices within a given set of geometrical design rules. The structures used to determine

these parameters and the test methods used are described in Section 3.3 of this report.

5. DEFECT DENSITY. These parameters characterize the faults that reduce circuit yield. The structures provide a measurement of defect density, expressed in terms of elements per defect. Defect densities for gate oxide pinholes, contact integrity, bridging faults, metal opens, and metal step-coverage faults can be determined. Section 2.2 contains a discussion of the types of structures and test methods.

6. RELIABILITY PARAMETERS. These parameters characterize the faults that either reduce circuit performance or limit circuit life. These parameters can be used to predict circuit life. Chapter 4 details the test for layer and contact electromigration and time-dependent dielectric breakdown.

In the course of this effort, five test chips were developed.

2.2 Fault Test Chip

2.2.1 Abstract

A Fault Chip has been developed to characterize defects found in the 3-μm CMOS/bulk integrated circuit (IC) processes. These defects originate in starting wafers, in the incomplete deposition and removal of layers, and in the faults induced by photolithographic patterning of layers. Knowledge of the defect density is essential to proper design, simulation, and testing of integrated circuits. To this end, the Fault Chip enables estimation of defect densities based on a Poisson distribution of defects. Defect densities can be used to determine the likelihood of each fault type for a specified circuit based on the circuit's layout geometry. Fault Chip analysis has enabled the characterization of a number of different faults from oxide pinholes to contact resistance distributions. It has also enabled the simulation of timing degradation of simple gates due to a resistive oxide pinhole fault.

2.2.2 Introduction

The goal of this effort is to prioritize faults found in test structures in a 3-μm CMOS/bulk process before stressing; to develop static CMOS/bulk fault models; and to develop suitable test circuits to verify the correctness of the models in predicting circuit degradation resulting from physical failures.

Our approach has been to develop a Fault Chip to characterize defects found in a 3-μm fabrication process. This chip is fabricated monthly through the MOS Implementation Service (MOSIS), Information Sciences Institute, University of Southern California (USC). A special wafer chuck was developed so the chips can be tested by an automated wafer prober and parametric data acquisition system. After the data is analyzed, a summary report is issued. When fully developed, the Fault Chip will be used in conjunction with foundry wafer acceptance procedures to form the basis for deciding if a given wafer fabrication process meets the requirements for space qualified microcircuits.

The current industry standard for fault simulation of integrated circuits uses a stuck-at fault approach. This approach introduces a hard fault on a circuit node which is either pulled to the power supply voltage or to ground. Further, it is assumed that stuck-at faults are the only faults. The Fault Chip is the first systematic attempt to measure the nature of such defects. Traditionally, fault information data bases have been derived from field failure reports. A novel approach is taken here where faults are directly characterized as they appear on foundry wafers in order to establish realistic integrated circuit tests.

The general categories of the test structures found on the Fault Chip are listed in Table 2.3. Notice that the first four test structures have been grouped according to whether a structure characterizes a defect between the same or different conducting layers. In a 3-μm CMOS/bulk single-metal process, a layer is either metal, poly-silicon, diffusion, or a bulk region. The design, layout, and testing of each of these structures is discussed in greater detail in a later section.

From the analysis of the Fault Chip, we have been able to distinguish between good and bad foundry runs, and have observed many noteworthy phenomena. For example, in one case we saw an abnormally large number of broken metal wires due to poor step coverage and were able to correlate this with the low yield of accompanying circuits. In another case, analysis of oxide pinholes resulted in the discovery that pinholes are terminated in n-type diffusion in the silicon which implies that the electrical characteristics of faulty n-MOSFETs are different from those of faulty p-MOSFETs. In another case, analysis of open-gated transistors showed that floating gates tend to have a small positive charge; thus, floating-gate n-MOSFETs are turned off and floating-gate p-MOSFETs are turned on.

The Fault Chip has also provided new insight into test structure design. For example, the original approach for evaluating contact integrity was a long string of contacts which does not provide information on parametric yield. The current approach, using several hundred individual contacts, allows determination of the mean contact resistance, the spread in values, and the probability of encountering an open contact.

Table 2.3: The Fault Chip test structures and associated parameters.

Structure	Parameter	Element	Analysis
Pinhole Array Capacitor	Different Layer Pinhole Resistance	Transistor	Elements/Defect
Comb Resistor	Same Layer Gap Resistance	Wire Gap	Elements/Defect
Serpentine Resistor	Same Layer Wire Resistance	Wire	Elements/Defect
Contact Matrix	Different Layer Contact Resistance	Contact	Probability of Open Contact
Inverter Matrix	Vinv, Vhigh, Vlow, and Gain	Inverter	Parameter Variability
Transistor Matrix	Timing and Different Layer Short Resistance	Transistor	Operating Domain
Open-Gate Devices	Conduction State	Transistor	Initial Gate Voltage

2.2.3 Fault Chip Organization

The Fault Chip is designed to characterize defects such as pinholes in gate and field oxides, contact integrity, and opens and shorts within layers. As seen in Figure 2.1, the chip is square, approximately 7.1 mm on a side, and contains a number of test structures. The structures included on Fault Chip No. 5 are listed in Table 2.4 along with the number of elements in each structure.

The design requires tradeoffs in the area consumed by each test structure. The objective is to include enough elements (for example, transistors or metal crossovers) to acquire meaningful fault data. This is difficult because the number of elements must increase as processing improves and defect densities become lower.

The Fault Chip has gone through five major design revisions and seven major versions to date. The major design revisions were:

Revision 1: Substrate contacts added to the p-PAC structure to collect the current injected from the gate to the substrate through oxide defects.

Revision 2: Cross-Bridge Resistor added to Metal Comb/Serpentine Resistor to

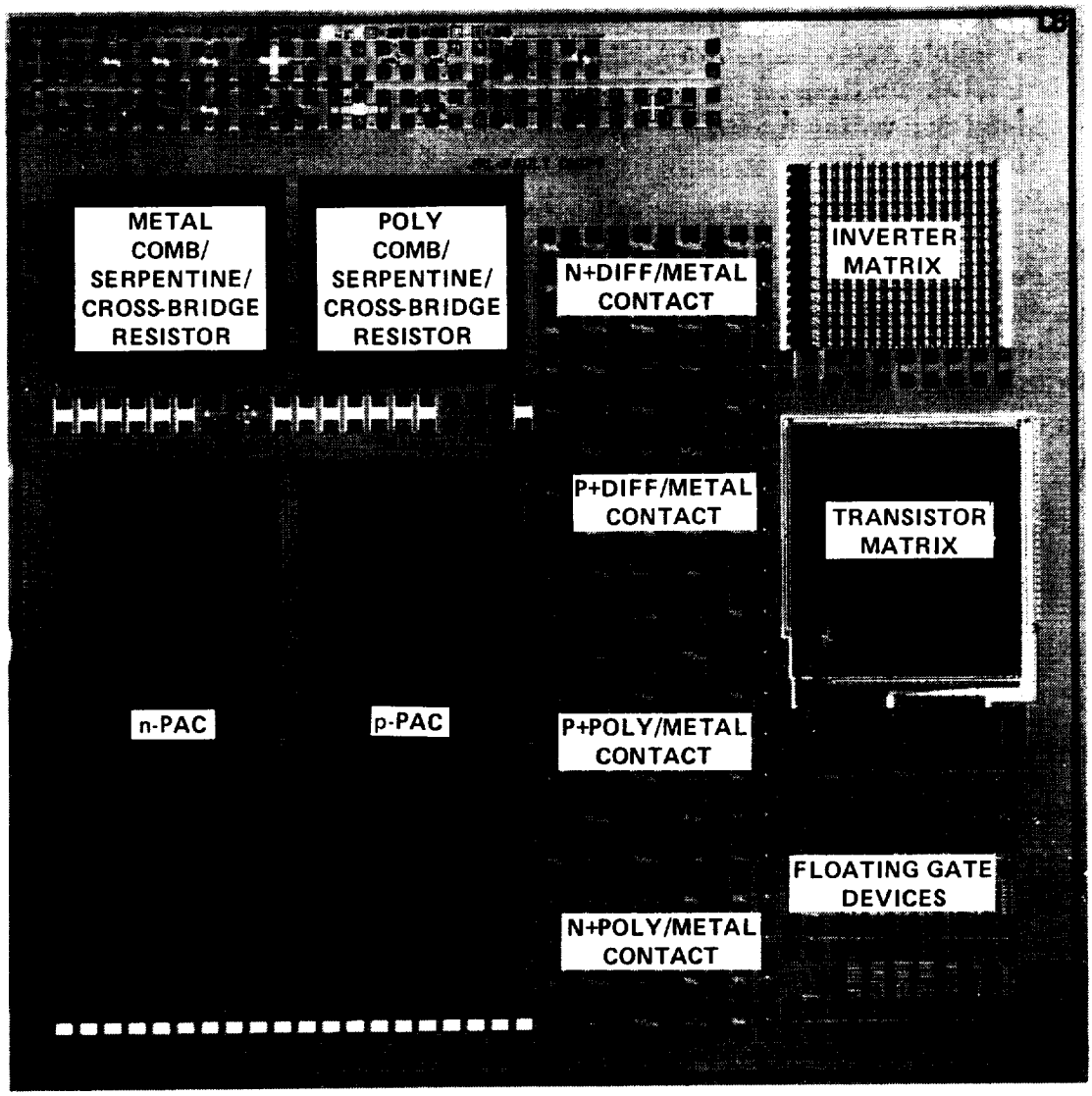


Figure 2.1: 3-μm CMOS/Bulk Fault Chip No. 5 (7.1 mm by 7.1 mm) with the MOSIS test strip shown at the top of the chip.

Table 2.4: Test structures for Fault Chip No. 5.

Test Structure	Element	# Elements	# Subarrays
1.n-Pinhole Array Capacitor	Transistor	90,558	4
2.p-Pinhole Array Capacitor	Transistor	90,558	4
3.Metal Comb Resistor	Adj. Length (μm)	218,448	5
Metal Serpentine Resistor	Step (6 μm)	18,450	1
Metal Cross-Bridge Resistor	Cross-Bridge	1	-
4.Poly Comb Resistor	Adj. Length (μm)	326,472	5
Poly Serpentine Resistor	Step (9 μm)	18,300	1
Poly Cross-Bridge Resistor	Cross-Bridge	1	-
5.Contact Chain Resistors	Contact	160	-
6.Inverter Matrix	Inverter	223	-
7.Transistor Matrix	Transistor	2,600	-
8.Open-Gate Devices	Transistors	144	-
	Inverters	2	-

locally measure the sheet resistance and wire width.

Revision 3: Poly Comb/Serpentine/Cross-Bridge resistor added to provide fault information on the poly layer.

Revision 4: Contact Matrix structures replaced by Contact Chain and Contact Chain Matrix structures. The Contact Chain Matrix provides more data points in less silicon area than individual contacts.

Revision 5: Floating gate transistor arrays replaced by isolated floating gate transistors to eliminate neighbor effects.

Figure 2.2 shows the latest version of the Fault Chip, No. 7, which includes all of the revisions discussed above. Structures included on Fault Chip No. 7 are listed in Table 2.5. The most noteworthy change between Fault Chip No. 7 and No. 5 is that the number of contacts has increased from 160 on No. 5 to 920 on No. 7.

In this discussion, a distinction is made between array-type and matrix-type test structures. In array-type structures, a large number of elements are tested simultaneously to assess whether a fault has occurred. In such structures, the parametric value of the fault can be characterized but the fault cannot be located

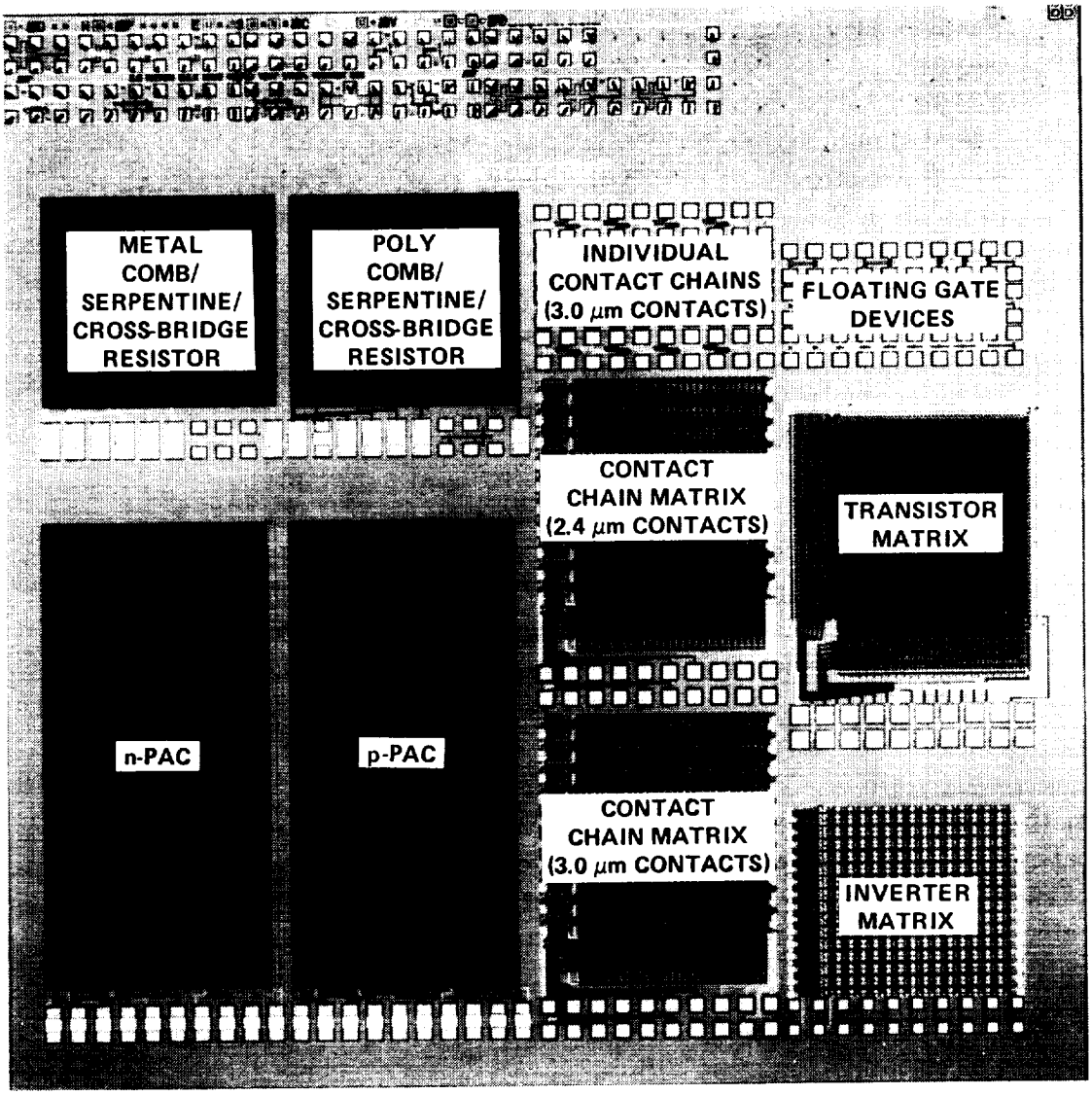


Figure 2.2: 3-μm CMOS/Bulk Fault Chip No. 7 (7.1 mm by 7.1 mm) with the MOSIS test strip shown at the top of the chip.

Table 2.5: Test structures for Fault Chip No. 7.

Test Structure	Element	# Elements	# Subarrays
1. Pinhole Array Capacitor			
n-type	Transistor	77,454	4
p-type	Transistor	77,454	4
2. Metal Comb/Serpentine/Cross-Bridge Resistor			
Comb Resistor	Adj. Length (μm)	218,448	5
Serpentine Resistor	Step (6 μm)	18,450	1
Cross-Bridge Resistor	Cross-Bridge	1	-
3. Poly Comb/Serpentine/Cross-Bridge Resistor			
Comb Resistor	Adj. Length (μm)	326,472	5
Serpentine Resistor	Step (9 μm)	18,300	1
Cross-Bridge Resistor	Cross-Bridge	1	-
4. Contact Chain Resistor Matrix			
	Contact (3.0 μm)	464	-
	Contact (2.4 μm)	464	-
5. Contact Chain Resistors	Contact (3.0 μm)	32	-
6. Matrixed Inverters	Inverter	223	-
7. Matrixed Transistors	Transistor	2,600	-
8. Open-Gate Devices	Transistors	22	-
	Inverters	2	-

in the array for further analysis. The Pinhole Array Capacitor falls into this category. In matrix-type structures, on-chip decoding allows characterization of each element in a matrix. The Contact Chain Resistor Matrix falls into this category. In the following sections each structure from Table 2.3 is described.

2.2.4 Pinhole Array Capacitor

Description

The Pinhole Array Capacitor (PAC) described elsewhere [3] represents the state of the art in evaluating MOS device integrity. The PAC consists of a metal cap separated by deposited oxide from an underlying two-dimensional array of MOSFETs. These MOSFETs are formed by orthogonally intersecting gate and diffusion layers. The structure is arranged in four subarrays. The number of

elements in each subarray is listed in the Defect Location Map given in Figures 2.5 and 2.6. The PAC can be used to characterize gate and metal-poly oxide defects. Metal-poly oxide defects are modeled by simple resistive shorts. Experimental results show the range of these resistive shorts to be between 1 and 100 kΩ.

The origin of the gate oxide pinholes in a CMOS local oxidation process, in which silicon nitride is used for gate oxide definition, is believed to be the formation of residual nitride at the silicon surface which masks against gate oxide growth [4,5,6] (Figure 2.3). This residual nitride results in a thinning of the gate oxide at the affected regions, and allows the phosphorous from the phosphorous-doped polycrystalline silicon gate material to dope the silicon n-type.

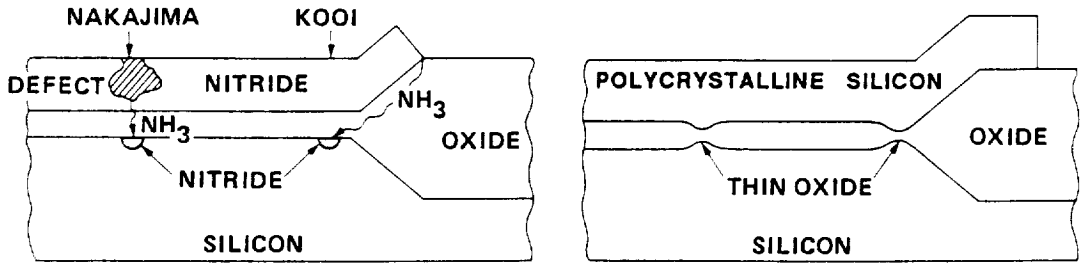


Figure 2.3: Gate Oxide defect origin, after Kooi (1976) and Nakajima (1979).

Analysis Technique

The first fault mechanism that is investigated is shorting between the metal cap and the poly gate, *IMP*. A voltage is applied to the metal cap and the current flow out the poly layer is measured.

The second fault mechanism investigated is shorting between the gate and the source/drain region. To perform this measurement, shown in Figure 2.4, a voltage is applied to various layers with the transistors either biased ON or OFF and the current measured. Four different measurements are made: *IPDON*, *IPBON*, *IPDOFF*, and *IPBOFF*. *IPD* is the current from Poly to Diffusion and *IPB* is the current from Poly to Bulk. The ON suffix indicates that a channel is present; OFF indicates that channel is absent. These four measurements allow us to identify the particular gate oxide defect as shown in Table 2.6. Two types

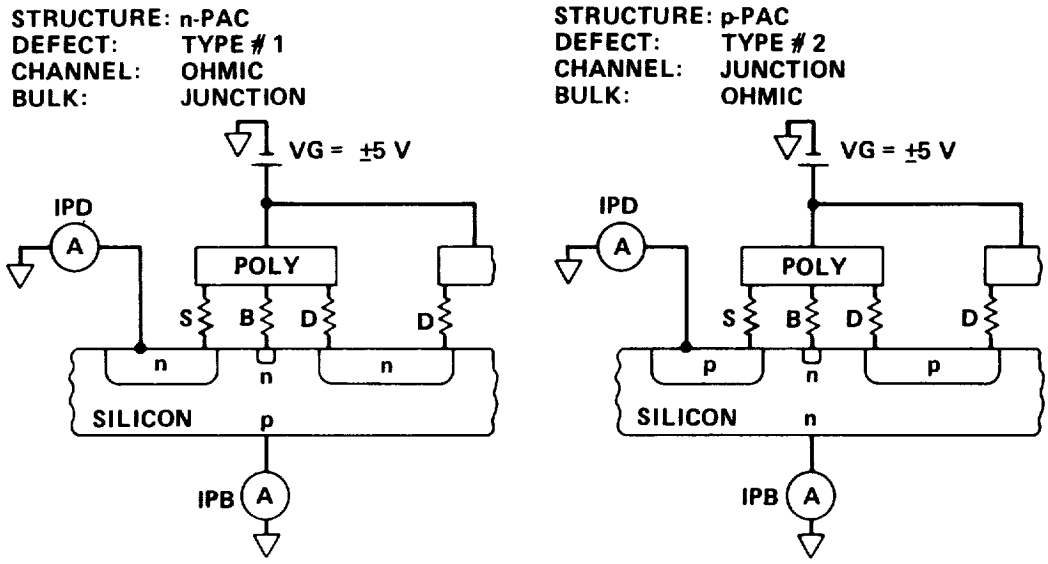


Figure 2.4: Two types of Pinhole Array Capacitor (PAC) structures where the fault type is determined by the channel conduction type.

of PAC fault models are proposed to explain the four measured currents. The type 1 defect models the n-PAC and the type 2 defect models the p-PAC. In the first type, the pinhole forms an ohmic connection to the channel and a diode connection to the bulk. In the second type, the pinhole forms a diode connection to the channel and an ohmic connection to the bulk. From these models we have prepared an expected response for the currents as shown in Table 2.7. This table was prepared for both single and multiple faults. A multiple fault (e.g., BD) is one in which two or more faults can lead to the same current path. If the measured current is greater than or equal to $I(CUTOFF)$ then it is assigned the value "1"; otherwise, it is assigned the value "0". Initially $I(CUTOFF)$ is set to 1.0×10^{-8} A, but our software can modify $I(CUTOFF)$ in the range of 1.0×10^{-9} to 1.0×10^{-7} A to better fit the data. Each modeled defect has a certain type of signature represented by four digits (see Table 2.7). From the four measured currents, one can identify the nature of the defect. In some cases other combinations of currents are observed. In these cases, the defect is not modeled by the defects shown in Figure 2.4. When this occurs the defects usually cover a large area and affect other adjacent subarrays. Notice in Table 2.7 that the p-PAC is more diagnosable than the n-PAC. Thus, if you have to choose between including a p-PAC or an n-PAC on a test chip, choose the p-PAC.

Table 2.6: Pinhole Array Capacitor defect classes.

Defect Classes	
N	No Defect Detected
B	Poly-Bulk Defect
D	Poly-Diffusion Defect
S	Poly-Diffusion Defect (Side of Array)
M	Metal-Poly Defect
P	Probing Fault
?	Other Defect

The PAC Data Analysis Program automates oxide defect categorization. Detected faults are categorized in three steps. First, a gate-oxide four-current histogram is generated, as seen in Figure 2.5. Letters of the alphabet are used as symbols to represent PAC subarrays with defects. Second, a wafer map is generated which shows the location of the faults on the wafer; see Figure 2.5. This information is used to determine whether the fault is an isolated defect or a cluster defect. Third, the defects are categorized as to the type of the defect. Finally, a value for the elements per defect, E, is calculated for each category and for all categories combined. Examples of this method for calculating these values are shown in Figures 2.5 and 2.6.

The PAC Data Analysis program was used to analyze the results from two 3-μm CMOS/bulk PACs. The total number of elements for each PAC structure is 70,434. Example results (both the raw data and the data analysis) are shown in Figures 2.5 and 2.6. These show that p-PACs have a total of 6 isolated gate oxide defects and one metal-poly oxide defect. Four of the gate oxide defects are B, BD type and two are SB type. For example, the "a" defect, highlighted in Figure 2.5, is clearly a B, BD type defect for its current exceeds $I(CUTOFF)$ in a 1101 sequence. The n-PACs have a total of one isolated gate oxide defect, four P-P clusters, one other defect, and three isolated metal-poly oxide defects. The gate oxide defect is type D, B, DB. The cluster defects are highlighted in Figure 2.6 and in the Defect Location Map shown in Figure 2.6. When defects are found in three or more adjacent subarrays, they are classified as a cluster defect.

Table 2.7: Defect identification based on four Pinhole Array Capacitor tests.

IPDON	*IPBON*	*IPDOFF*	*IPBOFF*	TYPE 1 n-PAC	TYPE 2 p-PAC
0	0	0	0	N	N
1	0	0	1	B,D,DB	D
1	0	1	1	S,SB,SD,SBD	S,SD
1	1	0	1	?	B,BD
1	1	1	1	?	SB,SBD
ALL OTHER COMBINATIONS				?	?

NOTES: ON = Channel present
OFF = Channel absent
0 = Current less than $I(CUTOFF)$
1 = Current greater than or equal to $I(CUTOFF)$

2.2.5 Comb/Serpentine/Cross-Bridge Resistor

Description

The Comb/Serpentine/Cross-Bridge Resistor is used to characterize single layer shorts and opens. This test structure consists of five combs, one serpentine, and one cross-bridge resistor. The layout of the structure is shown in Figure 2.7. Figure 2.8 shows a schematic representation of the Comb/Serpentine Resistor. The Comb/Serpentine/Cross-Bridge resistor is available for Metal and Poly layers. Prior to measuring the structure, a probe down test is performed. Notice that the probe pads for the structure shown in Figure 2.7 allow two probes to touch each pad. The probe down test is passed when the two-terminal resistance is less than some predetermined value which is usually 100 ohms.

The comb structures are used for detecting shorts between the serpentine and the comb wires which are spaced according to the design rule limit. The five combs have a different length adjacent to the serpentine. The serpentine crosses over steps made by lower level layers. For example, the Metal serpentine crosses over steps made by layers of poly and diffusion, and is used for detecting breaks in the wire due to step coverage problems.

The cross-bridge resistor is used to locally measure the sheet resistance and wire width where the bridge is formed over the highest level layer. This information is needed to analyze the serpentine resistance measurements.

M44E WAFER 4 p-PAC

FAULT CURR.	NUMBER OF OBSERVATIONS IPDON	IPBON	IPDOFF	IPBOFF	IMP
1.0×10^{-15}	0	0	0	0	0
2.0×10^{-15}	0	0	0	0	0
5.0×10^{-15}	0	0	0	0	0
1.0×10^{-14}	0	0	0	0	0
2.0×10^{-14}	1	0	0	0	0
5.0×10^{-14}	0	2	1	0	0
1.0×10^{-13}	0	0	0	0	0
2.0×10^{-13}	8	2	3 a	1	0
5.0×10^{-13}	7	3	4	0	0
1.0×10^{-12}	12	12	17	0	1
2.0×10^{-12}	8	22	19 d	24	10
5.0×10^{-12}	6	1	1 e	9	12
1.0×10^{-11}	0	0	0	6	7
2.0×10^{-11}	0	0	0	2	13
5.0×10^{-11}	0	0	0	0	2
1.0×10^{-10}	0	0	0	0	2
2.0×10^{-10}	0	0	0	0	0
5.0×10^{-10}	0	0	0	0	0
1.0×10^{-9}	0	0	0	0	0
2.0×10^{-9}	0	0	1 f	0	0
5.0×10^{-9}	0	0	0	0	0
I(*CUTOFF*)					
1.0×10^{-8}	1 d	0	0	0	0
2.0×10^{-8}	0	0	0	0	0
5.0×10^{-8}	1 a	0	0	0	0
1.0×10^{-7}	0	0	0	0	0
2.0×10^{-7}	0	0	1 b	0	0
5.0×10^{-7}	0	0	0	0	0
1.0×10^{-6}	0	0	1 c	0	0
2.0×10^{-6}	3 bef	0	0	0	0
5.0×10^{-6}	1 c	0	0	0	0
1.0×10^{-5}	0	0	0	0	0
2.0×10^{-5}	0	0	0	0	0
5.0×10^{-5}	0	1 b	0	1 b	0
1.0×10^{-4}	0	0	0	1 c	0
2.0×10^{-4}	0	4 acef	0	3 aef	0
5.0×10^{-4}	0	1 d	0	1 d	1
1.0×10^{-3}	0	0	0	0	0
2.0×10^{-3}	0	0	0	0	0
5.0×10^{-3}	0	0	0	0	0
INC/EXC	48/0	48/0	48/0	48/0	48/0

CUTOFF $< 10^{-8}$ Amps STRESS VOLTAGE = 5.0 V
LOWER BOUND SHOWN FOR HISTOGRAM INCREMENT
CURRENT SOURCE BOUND APPROX = 20 mA

Figure 2.5: P-PAC test results for run M44E, wafer 4.

```
DEFECT LOCATION MAP:

M44E      WAFER  4    p-PAC

          COL 1144488ACCDD
          ROW 582585825858
M/PP     2709 ------------
         8127 ------------
        18963 ----------M-
        40635 ------------
P/PD     2709 ------------
         8127 ------a-----
        18963 ----b-c---d-
        40635 --e---f-----
```

p-PAC DEFECT ANALYSIS

GATE OXIDE DEFECTS								
	TYPE				CLUSTERS		OTHER	TOTAL
	D	S	B,BD	SB	P-P	M-P		ELEMENTS
FAULT SITE			e a f d	b c				70434
E ($\times 10^5$)	> 3.6	> 3.6	2.1	6.0	> 3.6	> 3.6	> 3.6	1.5
ES ($\times 10^4$)	***	***	2.6	66	***	***	***	4.8

METAL-POLY FIELD OXIDE DEFECTS					
	TYPE	CLUSTERS		OTHER	TOTAL
	M	M-M	M-P		ELEMENTS
NO. OF FAULTS	1	0	0	0	70434
E ($\times 10^5$)	13	> 3.6	> 3.6	> 3.6	13
ES ($\times 10^4$)	1.4	***	***	***	1.4

Figure 2.5: P-PAC test results for run M44E, wafer 4 (Continued).

M44E WAFER 4 n-PAC

FAULT CURR.	NUMBER OF OBSERVATIONS IPDON	IPBON	IPDOFF	IPBOFF	IMP
1.0×10^{-15}	0	0	0	0	0
2.0×10^{-15}	0	0	0	1	0
5.0×10^{-15}	0	1	0	0	0
1.0×10^{-14}	0	0	0	0	0
2.0×10^{-14}	0	1	1	0	0
5.0×10^{-14}	0	0	1	0	0
1.0×10^{-13}	0	2	2	1	0
2.0×10^{-13}	0	4	2	1	1
5.0×10^{-13}	6	9	7	1	2
1.0×10^{-12}	10	9	6	6	3
2.0×10^{-12}	19	9	19	20	13
5.0×10^{-12}	5	4	3	2	15
1.0×10^{-11}	0	0	0	8	5
2.0×10^{-11}	1	1 d	0	1	3
5.0×10^{-11}	0	0	0	0	2
1.0×10^{-10}	0	1	0	0	0
2.0×10^{-10}	0	1	2 **bd**	0	0
5.0×10^{-10}	3 **abc**	0	3 **ace**	0	0
1.0×10^{-9}	1 **e**	0	0	0	0
2.0×10^{-9}	0	0	0	0	0
5.0×10^{-9}	0	0	0	0	0
I(*CUTOFF*)					
1.0×10^{-8}	0	3 **abc**	0	4 **abce**	0
2.0×10^{-8}	0	1 **e**	0	0	0
5.0×10^{-8}	0	0	0	0	0
1.0×10^{-7}	0	0	0	0	0
2.0×10^{-7}	0	0	0	0	0
5.0×10^{-7}	0	0	0	0	0
1.0×10^{-6}	0	0	0	0	0
2.0×10^{-6}	0	0	0	1 f	0
5.0×10^{-6}	0	1 f	0	0	0
1.0×10^{-5}	0	0	0	0	0
2.0×10^{-5}	1 d	0	0	0	0
5.0×10^{-5}	0	0	0	0	0
1.0×10^{-4}	0	0	0	1 d	0
2.0×10^{-4}	1 f	0	1 f	0	0
5.0×10^{-4}	0	0	0	0	2
1.0×10^{-3}	0	0	0	0	1
2.0×10^{-3}	0	0	0	0	0
5.0×10^{-3}	0	0	0	0	0
INC/EXC	47/1	47/1	47/1	47/1	47/1

CUTOFF $< 10^{-8}$ Amps STRESS VOLTAGE = 5.0 V
LOWER BOUND SHOWN FOR HISTOGRAM INCREMENT
CURRENT SOURCE BOUND APPROX = 20 mA

Figure 2.6: N-PAC test results for run M44E, wafer 4.

```
DEFECT LOCATION MAP:

M44E      WAFER  4    n-PAC

        COL 1144488ACCDD
        ROW 582585825858
M/NP   2709 --------P---
       8127 --M---------
      18963 ------------
      40635 -M------M---
P/ND   2709 a-------P---
       8127 b-----------
      18963 c-----d-----
      40635 e----------f
```

n-PAC DEFECT ANALYSIS

GATE OXIDE DEFECTS						
	TYPE		CLUSTERS		OTHER	TOTAL
	D,B,DB	S,SB	P-P	M-P		ELEMENTS
FAULT SITE	d		a b c e		f	70434
E ($\times 10^5$)	13	> 3.6	3.4	> 3.6	5.9	1.8
ES ($\times 10^4$)	140	***	14	***	15	4.1

METAL-POLY FIELD OXIDE DEFECTS					
	TYPE	CLUSTERS		OTHER	TOTAL
	M	M-M	M-P		ELEMENTS
NO. OF FAULTS	3	0	0	0	70434
E ($\times 10^5$)	2.6	> 3.6	> 3.6	> 3.6	2.6
ES ($\times 10^4$)	6.9	***	***	***	6.9

Figure 2.6: N-PAC test results for run M44E, wafer 4 (Continued).

Analysis Technique

The serpentine resistance, R_{serp}, is measured by forcing a current through the serpentine and measuring the voltage drop. The serpentine effective length, L_{serp}, is

$$L_{serp} = \frac{R_{serp} \times W_{bridge,high}}{R_{s,bridge}}$$

where $W_{bridge,high}$ is the width and $R_{s,bridge}$ is the sheet resistance. L_{serp} is compared with the as-drawn serpentine length. If the effective length is longer than 150% of the as-drawn length then the serpentine is considered to have a step-coverage problem and the site is flagged as faulty. The apparent serpentine length is due to a combination of one or more of the following:

1. Serpentine wire thinning and necking at the step.
2. Undulation due to the serpentine wire crossing over steps.
3. Width of high lying layers being different from low lying layers.
4. Under/over sizing of the underlying features due to over/under etching.

Wire shorts are detected by suppling 5 V between the serpentine and the comb wires. If the leakage current between two layers is greater than 10.0 nA, the wires are considered shorted and the site is flagged as faulty.

A software program has been developed to analyze the raw data gathered from the Comb/Serpentine/Cross-Bridge resistor. The program generates a histogram of the effective length of the serpentine wires and calculates the defect densities for the wire shorts and opens detected.

The analysis results for Poly Comb/Serpentine/Cross-Bridge resistor for run M61P are shown in Figure 2.9. No short or open defects in the poly comb were observed for the M61P run. Notice that $L_{serp} = 169931\,\mu$m which is 3.2 percent larger than $L_{as\text{-}drawn} = 164700\,\mu$m. The "P" shown for the serpentine indicates that a probing fault was encountered.

2.2.6 Contact Chain and Contact Chain Matrix

Description

The Contact Chain Structure [7] consists of eight contacts connected to form a chain. Since these contacts share the same current path they consume less silicon area than individual contacts. Figure 2.10 shows the layout of the Contact Chain Structure. The four types of Contact Chain Structures are:

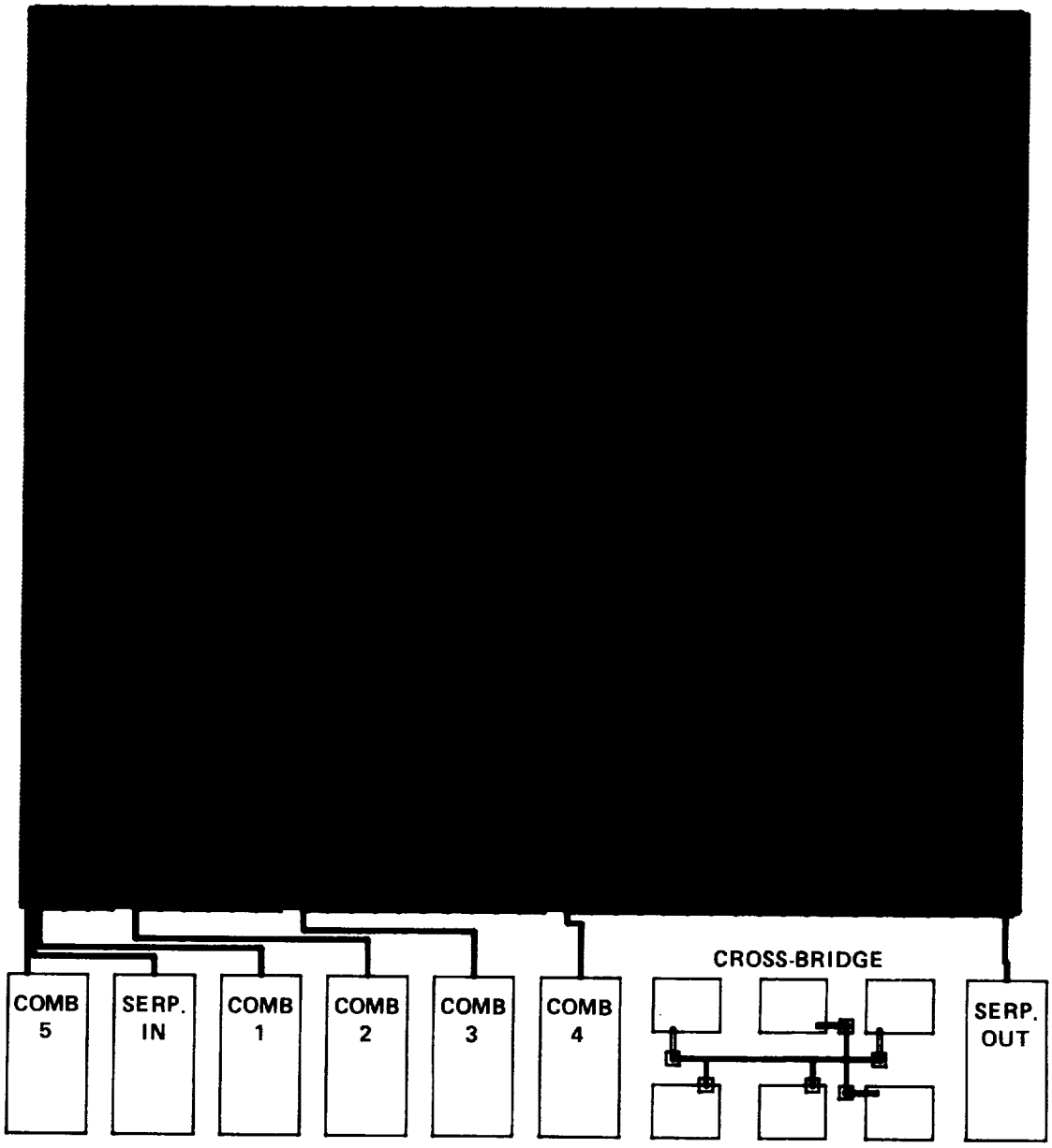


Figure 2.7: The Comb/Serpentine/Cross-Bridge Resistor in First-Layer Metal with poly crossovers.

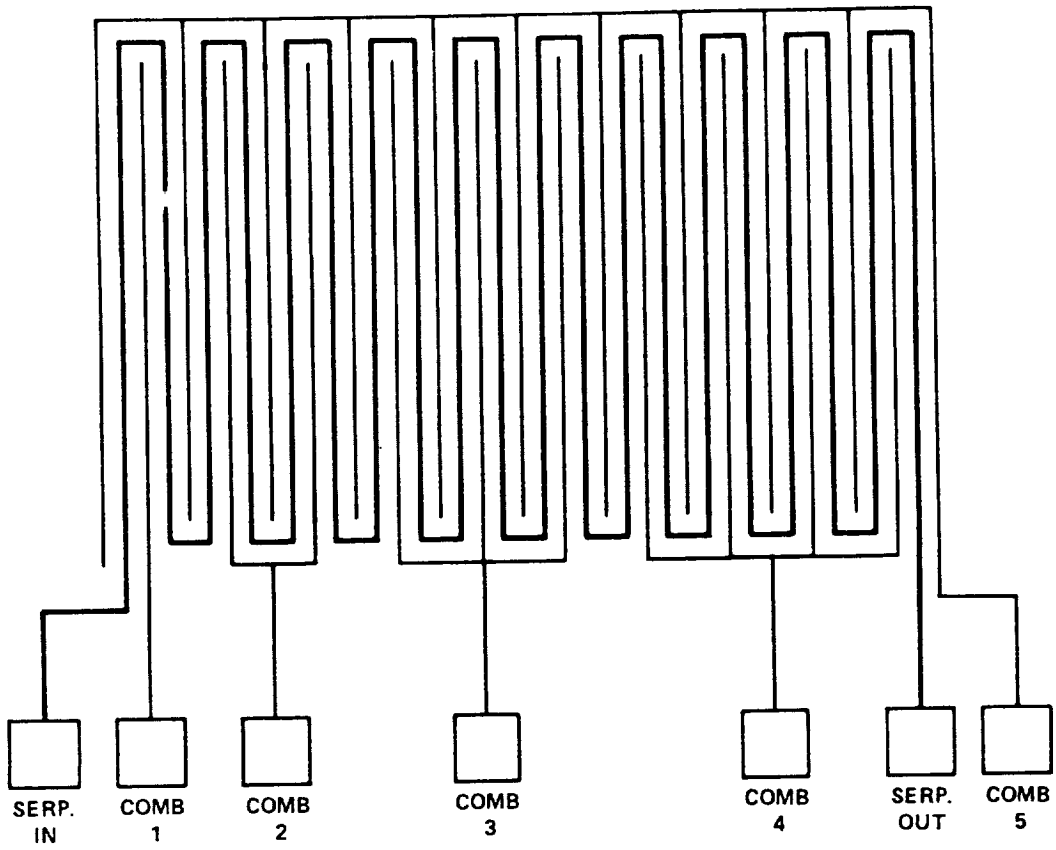


Figure 2.8: Schematic diagram of the Comb/Serpentine Resistor which is segmented into five subarrays.

1. p+Poly/Metal,
2. n+Poly/Metal,
3. p+Diff/Metal, and
4. n+Diff/Metal.

However, the Contact Chain Structure does not provide enough data on each chip to enable a meaningful contact probability analysis. Thus, the Contact Chain Matrix Structure was designed and included on Fault Chip No. 7. Figures 2.11 and 2.12 show the Contact Chain Matrix layout schematic and the Contact Chain Matrix transistor level schematic, respectively. The Contact Chain Matrix Structure included on Fault Chip No. 7 consists of four different

Identity of failed chip - by location in chip carrier

M61P	CHIP NO.	1111111112222222222 123456789A123456789A
COMB	16056	----------
	29436	----------
	50844	----------
	66900	----------
	163236	----------
SERP.	18300	--------P----------

SERPENTINE LENGTH HISTOGRAM

LENGTH (μm)	NUMBER OF OBSERVATIONS	
-	0	
166943	0	
167690	3	***
168437	3	***
169184	5	*****
169931	2	**
170678	4	****
171425	0	
172172	1	*
172919	1	*
+	0	

As-Drawn Serpentine Length = 164700 (μm)
Open Serpentine Wires = [0], High Res. Serpentine Wires = [0]
Shorted Combs = [0]
L_{serp} (μm) Avg/StDev/Inc/Exc/Inv = $169931/1.39 \times 10^3/19/0/1$
R_{serp} (Ω) Avg/StDev/Inc/Exc/Inv = $812856/3.30 \times 10^4/19/0/1$
$R_{s,bridge}$ (Ω) Avg/StDev/Inc/Exc/Inv = 14.5/1.11/20/0/0
$W_{bridge,high}$ (μm) Avg/StDev/Inc/Exc/Inv = 3.03/0.228/20/0/0

YIELD ANALYSIS (Total # Sites = 20)

	Shorts	Opens
Total # Elements	6529440 (μm)	366000 (Step: 9 μm)
Total # Shorts	0 (μm)	NA
Total # Defects	NA	0
Elements/Defect	$> 2.13 \times 10^6$ (μm/Defect)	$> 3.66 \times 10^5$ (Steps/Defect)
Std. Deviation	*******	*******

Figure 2.9: Test results of Poly Comb/Serpentine/Cross-Bridge on M61P run.

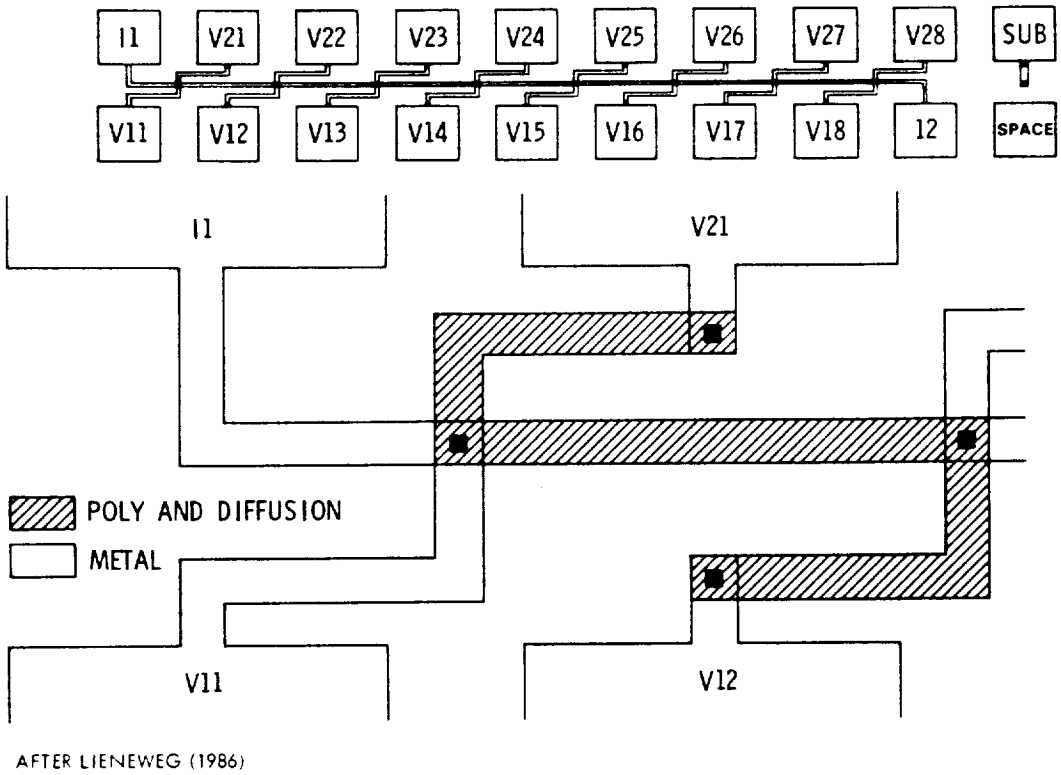


Figure 2.10: Contact Chain Structure.

types of contacts: p+ and n+Poly/metal and p+ and n+Diff/Metal. There are 116 contacts for each contact type. The Contact Chain Matrix Structure consists of 8 rows and 58 columns. The contacts in each row of the matrix share the same current path to save silicon area.

The Contact Chain Matrix Structure, by using one randomly accessible matrix, replaces the four contact matrix structures which were needed to access the different types of contacts. This saves area which would otherwise have been consumed by the necessary overhead circuitry and pads.

An early version of the Contact Chain Matrix Structure included 2nd metal to 1st metal via resistance chains. This structure was unsuccessful because excessively large currents were required to generate measurable voltages.

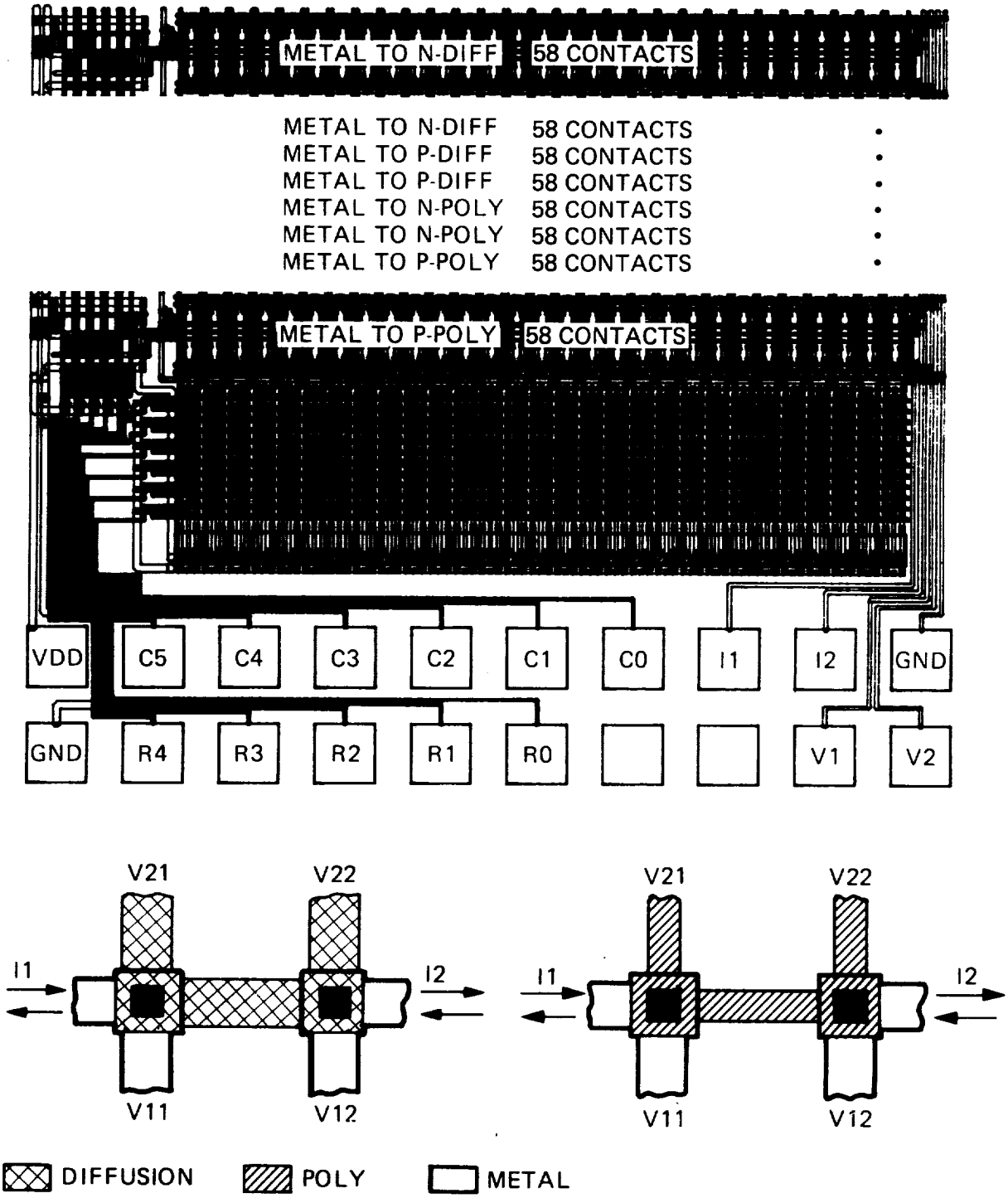


Figure 2.11: Contact Chain Matrix with 464 contacts. Developed to characterize the four types of contacts found in a single-metal 3-μm CMOS process.

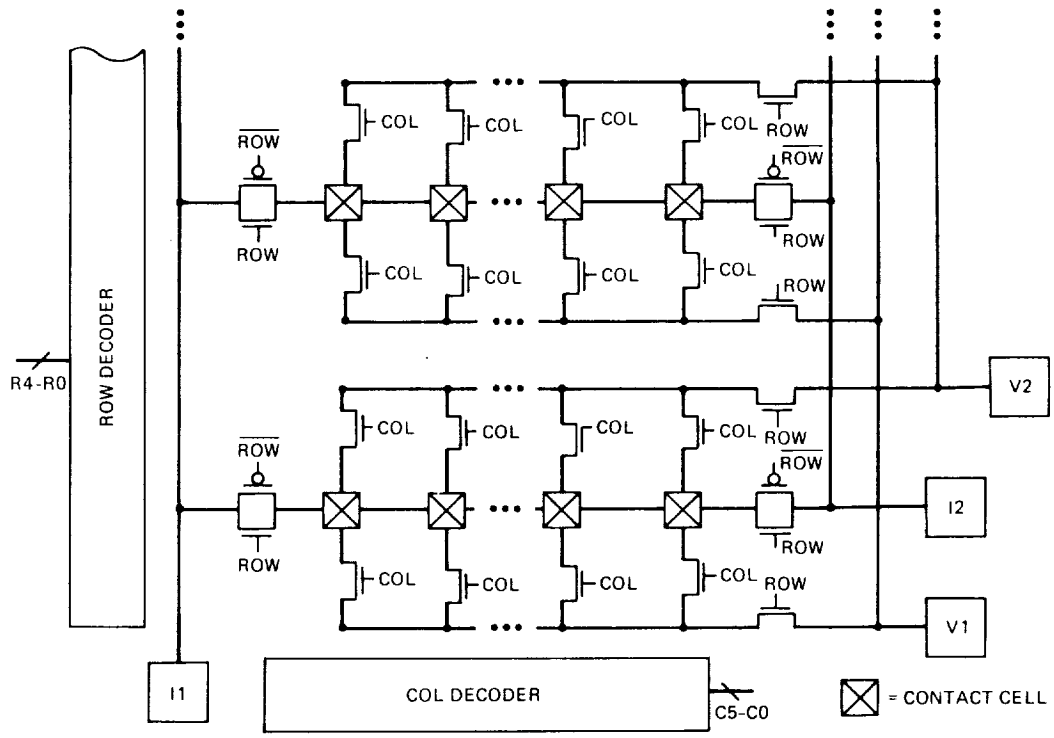


Figure 2.12: The Contact Chain Matrix, where the row and column addressing circuitry allows the measurement of each contact denoted by an X.

Analysis Technique

The test procedure calls for forcing a current of known value ($64\,\mu A/\mu m^2$) through the Contact Chain and measuring the voltage drop over the contact surface. This is a four-terminal measurement and allows accurate measurements of the contact interfacial resistance.

The contacts are characterized by three numbers: the mean, the standard deviation, and the probability of encountering an open contact, based on contact probability analysis [7]. This technique, shown in Figure 2.13, assumes a normal distribution of contact conductance. The cumulative distribution of contact conductance is plotted on the probability scale and a line is fitted using a Chi-square linear fit. The intersection of the fitted line and the probability axis is taken to represent the probability of a contact having zero conductance, i.e., the probability of an open contact. This provides a characteristic number which can be used to assess the difference between processes, and/or vendors. The

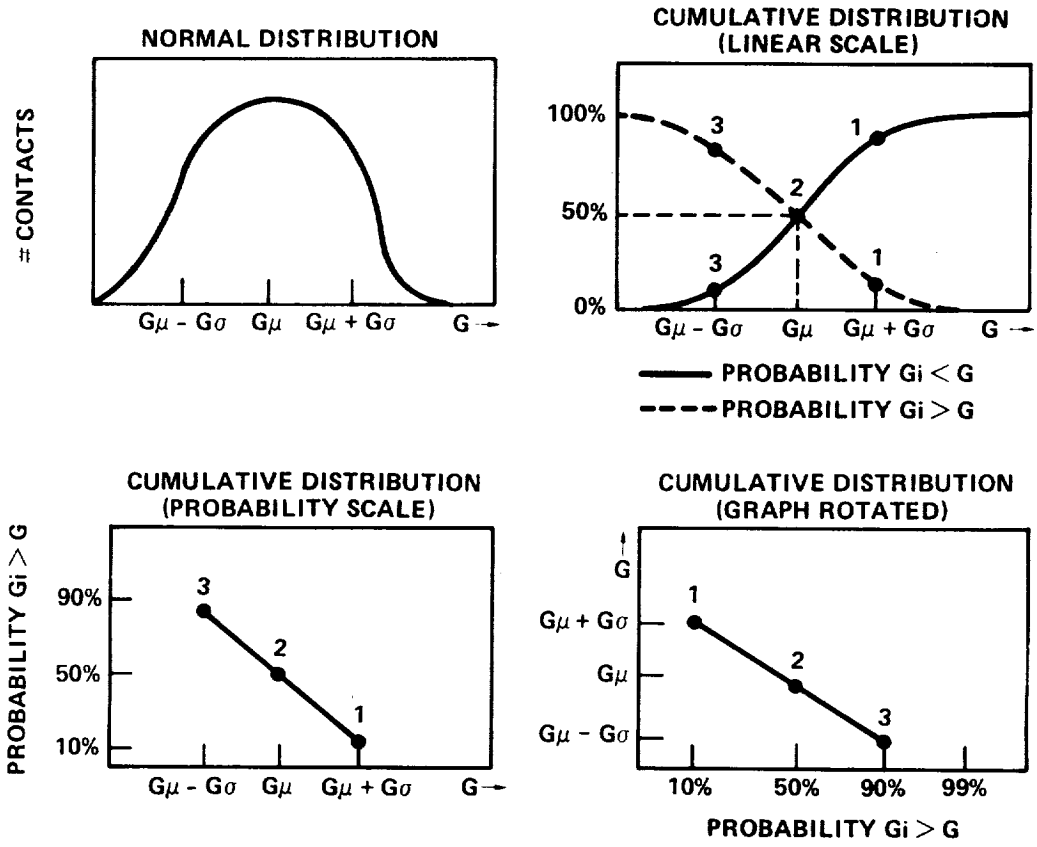


Figure 2.13: Contact resistance probability analysis method.

characteristic number depends on the ratio between the population mean and the population standard deviation. Figure 2.14 shows the contact probability analysis for 3.0-μm p+Poly/Metal contacts of run M62Z. The probability of encountering an open contact for the p+Poly/Metal contacts of run M62Z is 1.947×10^{-7}.

2.2.7 Floating Gate Transistors

Description

The floating gate transistor is a transistor with an isolated poly gate wire. The behavior of the transistor is expected to depend on the initial charge induced on the gate by the process and the charge induced from the measurement potentials. The floating gate transistor models for n- and p-channel transistors are shown in Figure 2.15. The three capacitances involved in determining the behavior of the floating gate transistors are the gate-to-drain capacitance, Cgd, the gate-to-

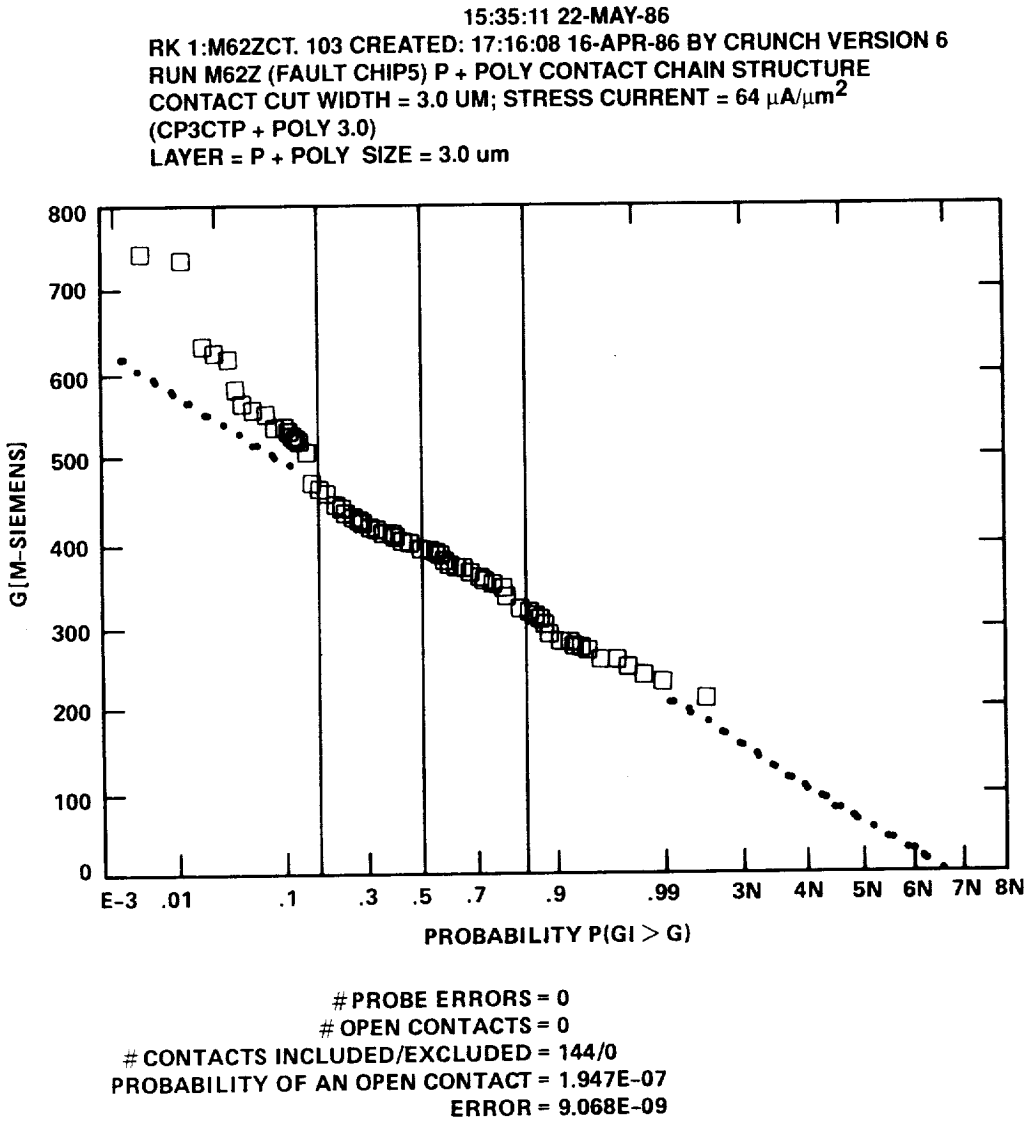


Figure 2.14: Contact Probability Analysis for p+Poly/Metal contacts of run M62Z. The analysis technique was developed at JPL by U. Lieneweg and D. Hannaman.

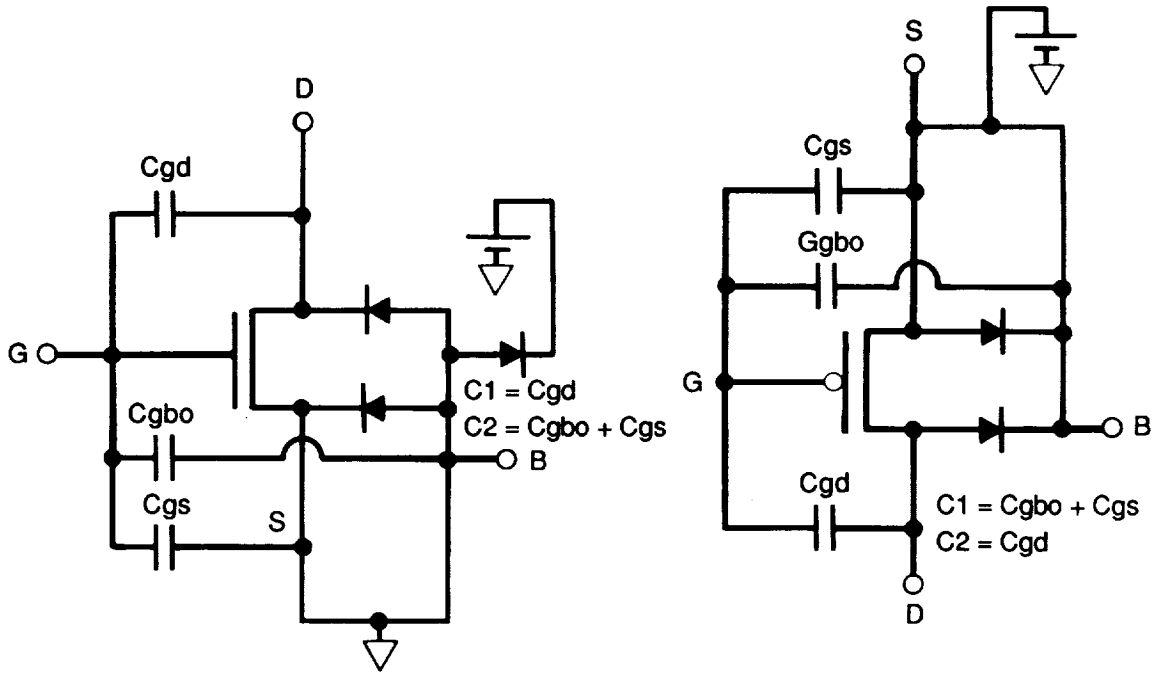


Figure 2.15: Floating gate transistor models where the body is shorted to the source.

source capacitance, Cgs, and the gate-to-bulk overlap capacitance, $Cgbo$. $Cgbo$ depends on the area of the poly over the field oxide.

Analysis Technique

The test setup for testing floating gate transistors is shown in Figure 2.16. A voltage is applied to the drain of the transistor and the resulting current through the source is measured. In run M56G the floating gate transistors with a gate length of 3 μm and a gate overlap length of 26 μm were tested with a drain-to-source voltage of 5 V. The floating gate p-channel transistors were "ON" with a channel current of about 1.0×10^{-6} A, and the floating gate n-channel transistors were "OFF." The floating gate transistor voltage is the gate voltage required to cause the same current to flow in a calibrator transistor. The calibrator

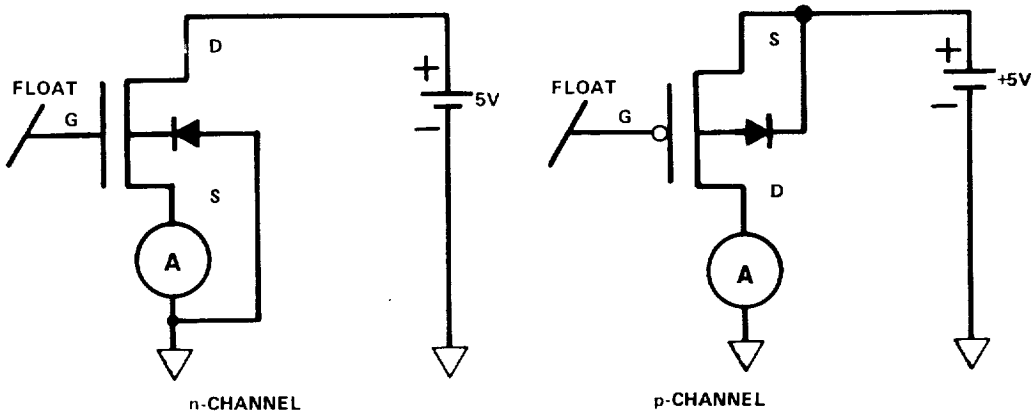


Figure 2.16: Test setup for floating gate transistors.

transistor is fully connected and provides transistor I-V curves. The floating gate device analysis using a calibrator transistor is shown in Figure 2.17. Transistor I-V curves from the calibrator transistor are used to estimate the floating gate voltage for a given drain-to-source voltage and channel current. It is estimated that for run M56G the gate voltage of the n-channel transistors is less than VTn, and the p-channel transistor $Vgd = 3.5\,\mathrm{V}$ ($Vgs = -1.5\,\mathrm{V}$). The gate voltage of the floating gate transistors is calculated from the following equation, using the capacitor-divider models shown in Figure 2.15

$$VG = VG_i + \frac{(|VDS| - VGi) \times (1 - e^{-t/RC})}{1 + C2/C1}$$

where $C = C1 \times C2/(C1 + C2)$, $C1 = Cgd$ and $C2 = Cgbo + Cgs$ for n-channel transistors ($C1 = Cgbo + Cgs$ and $C2 = Cgd$ for p-channel transistors), and VGi is the process-induced charge on the gate. Also R is the resistance in series with the external voltage source. The time constant, RC, is of the order 1.0×10^{-13} seconds. Thus for time $t \gg RC$ this equation becomes

$$VG = VGi + \frac{(|VDS| - VGi)}{1 + C2/C1}$$

Since the gate delay of the CMOS devices is much larger than the time constant RC, the transition time between the initial state and the steady state is negligible. The initial gate voltage, VGi, represents the gate-to-source voltage

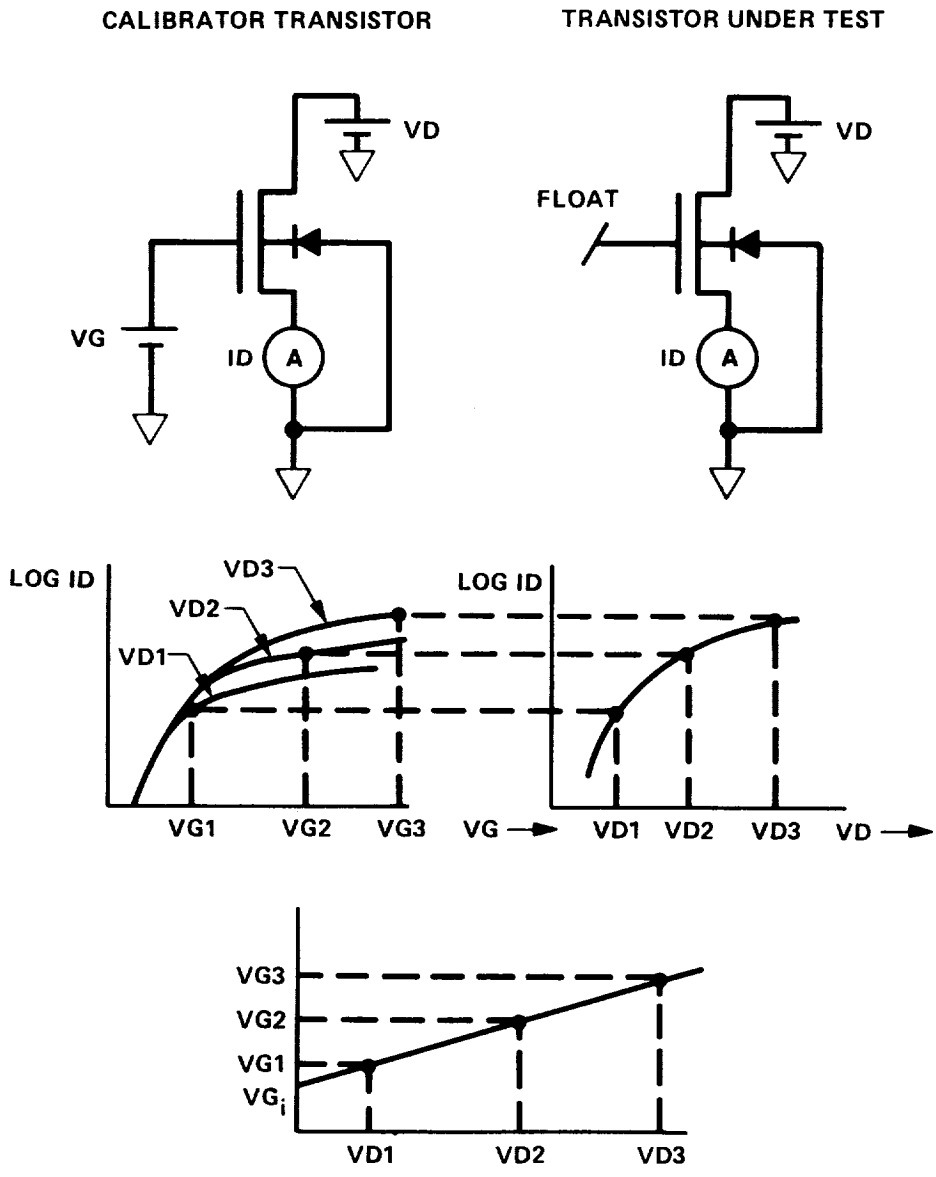


Figure 2.17: Floating-Gate device analysis.

at a drain-to-source voltage of zero volts, and is important for simulating the behavior of the floating gate transistors.

The initial gate voltage can be determined from experimental measurements when $VGi \ll VDS$, as shown in Figure 2.17. When $VGi \ll VDS$ the above equation becomes

$$VG = VGi + \frac{|VDS|}{1 + C2/C1}$$

A minimum of two floating gate voltage measurements at different drain-to-source voltages are required to estimate the initial gate voltage. In Figure 2.18 we observe that the estimated initial gate voltage for run M61P is 0.18 V and that the gate voltage for n-channel floating gate transistors is inversely proportional

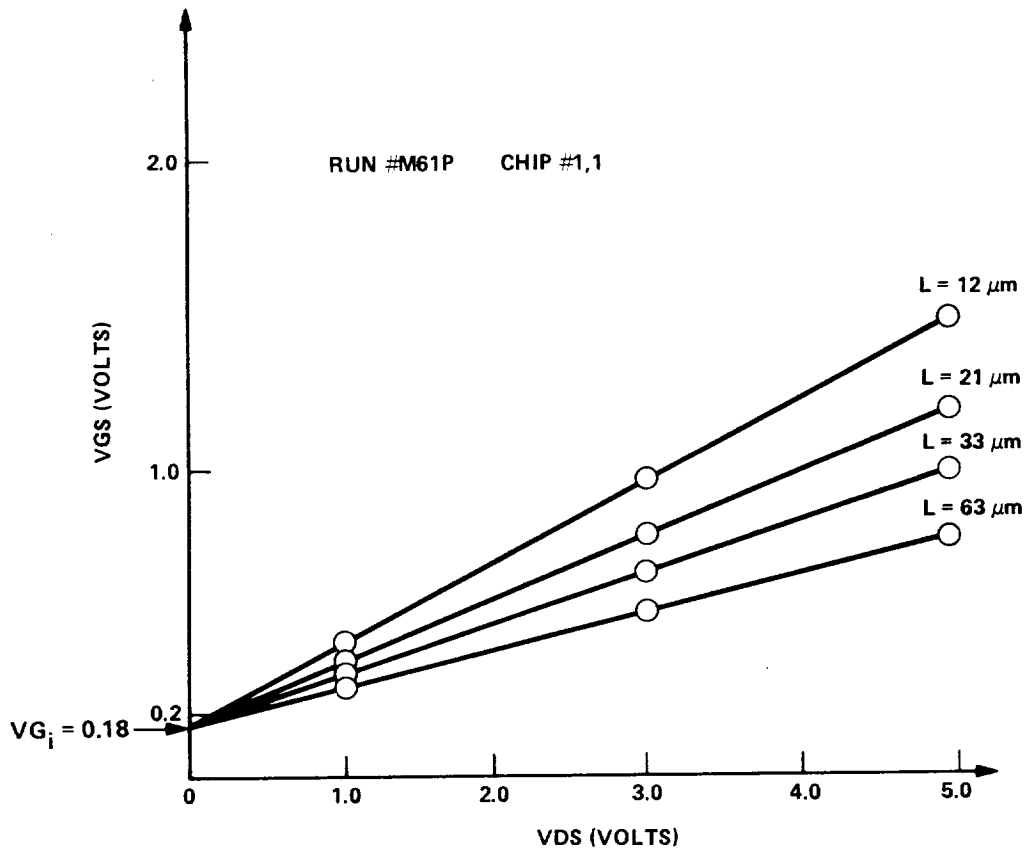


Figure 2.18: Floating gate n-channel transistor analysis of run M61P. The L is the gate poly overlap length of the floating gate transistor. The channel width and length are 4.5 and 3.0 μm, respectively.

to the gate poly length. We also observe that the gate voltage for p-channel floating gate transistors is directly proportional to the gate poly overlap length. As the gate poly overlap length increases, both the n- and p-channel floating gate transistors operate closer to their "OFF" state. Figure 2.19 shows the experimental results of the gate poly overlap length variations on the conduction state of the n-channel transistor. As expected, the results in Figure 2.19 correlate with the theoretical results.

In order to study the behavior of floating gate transistors in an inverter, we have designed faulted inverter structures. The two types of faulted inverter structures are shown in Figure 2.20. The first structure has individual floating gate poly wires for the n-channel and the p-channel transistors. The second structure has a common floating gate poly wire for the n-channel and p-channel transistors. The above equations are valid for calculating the gate voltage of the n- and p-channel floating gate transistors of the first faulted inverter structure. The common gate voltage of the second faulted inverter structure is calculated using

$$VG = VGi + \frac{(VDD - VGi)(1 - e^{-t/RC})}{1 + C2/C1}$$

where $C = (C1 \times C2)/(C1 + C2)$, $C1 = Cgs2 + Cgbo2$, $C2 = Cgs1 + Cgbo1$, and $Cgd2$ and $Cgd1$ are ignored.

At time $t \gg RC$ (RC is in the order of 1.0×10^{-13} seconds), we have

$$VG = VGi + \frac{(VDD - VGi)}{1 + C2/C1}$$

Since we can assume that $C1 = C2$ and $VGi \ll VDD$, we expect a gate voltage of $VDD/2$ for the second faulted inverter structure.

The analysis of the faulted inverter structures of the M56G run shows that the first type of faulted inverters is stuck high with an output voltage of between 4.0 and 5.0 V. This observation is consistent with the results for individual floating gate transistors: the p-channel floating gate transistor is "ON" and the n-channel floating gate transistor is "OFF" for a gate poly overlap length of about 26 μm. The second type of faulted inverters draws almost maximum current and the output voltage is at about 2.5 V or $VDD/2$. This observation implies that for this configuration the p-channel and the n-channel transistors are "ON" with the gate voltage of about 2.5 V which confirms our assumptions.

The work on the floating gate transistors is still under way; many observations have not yet been fully analyzed or understood. Better test structures have been developed and are expected to be functional on future Fault Chips.

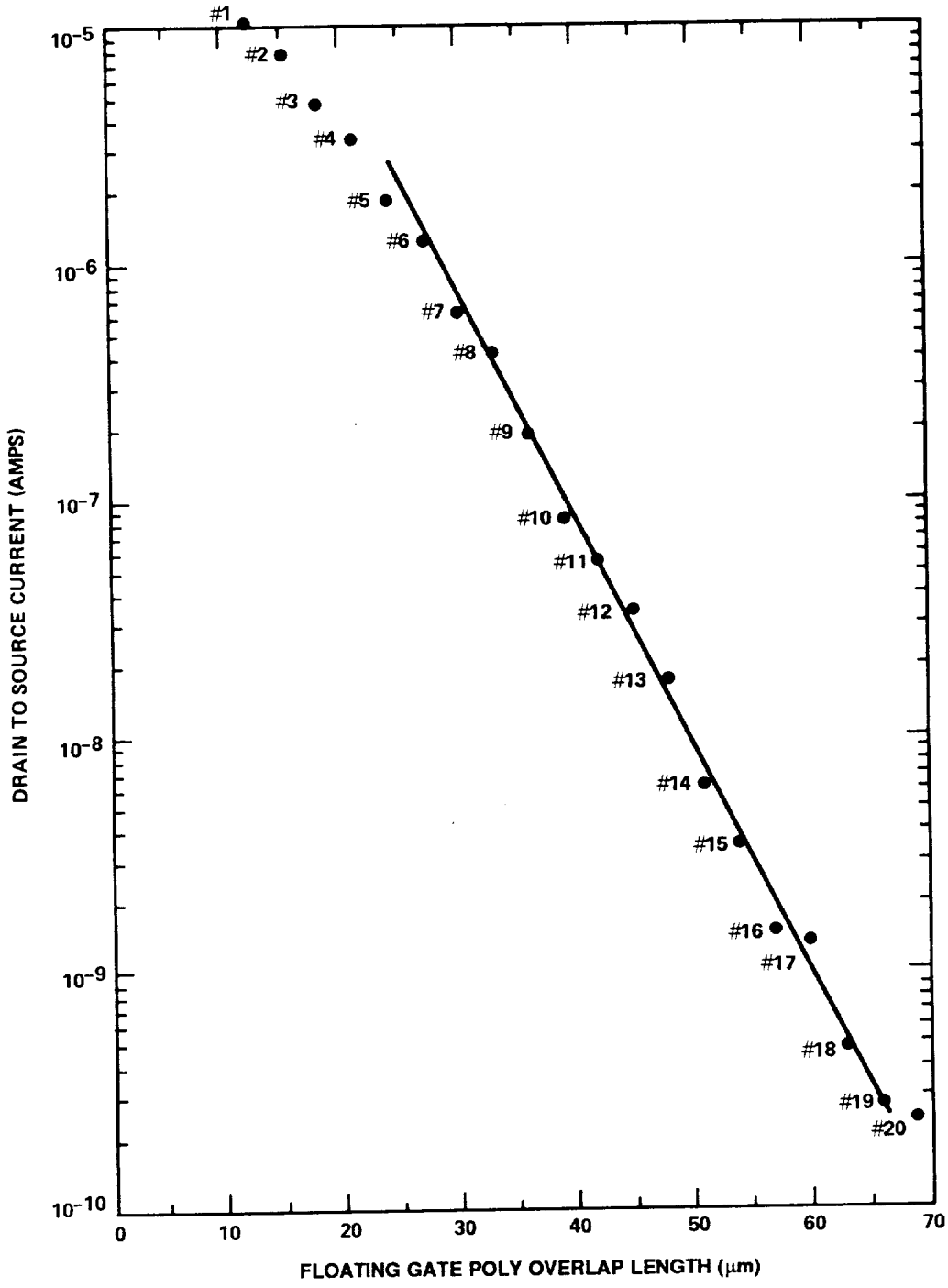


Figure 2.19: Experimental results of the gate poly overlap length variations on the conduction state of the n-channel transistor for $VDS = 5\,\mathrm{V}$. The VGi analysis for this device is shown in Figure 2.18.

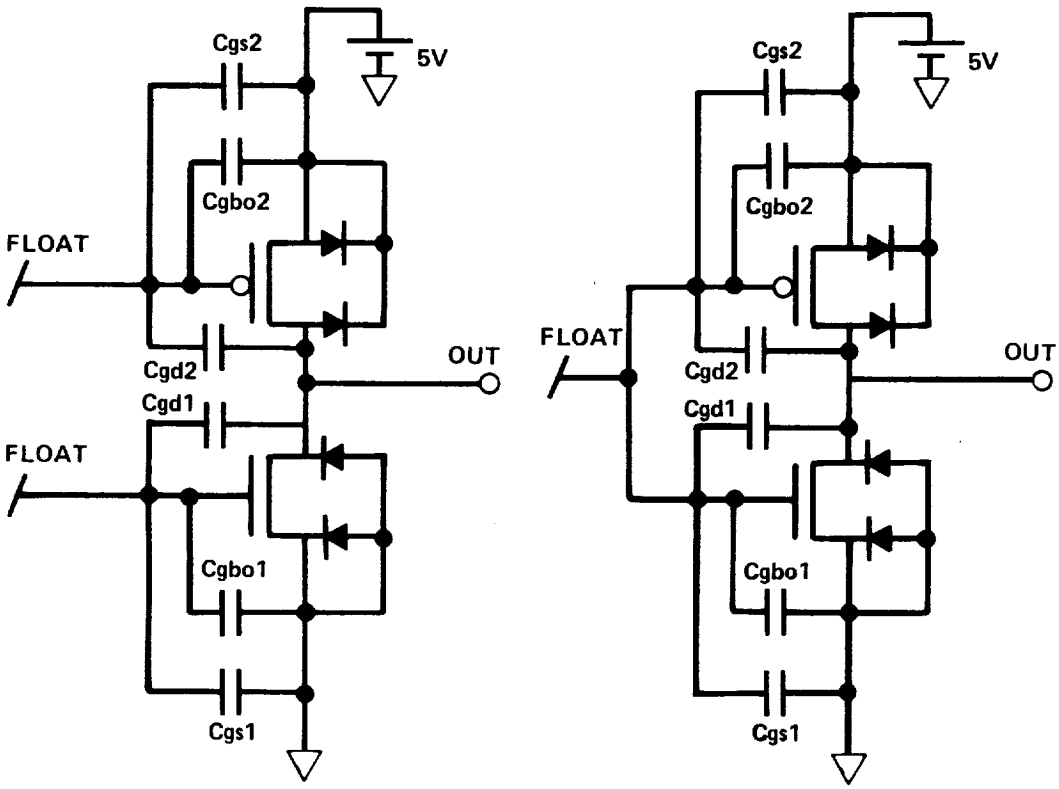


Figure 2.20: Two types of the faulted inverter structure.

2.2.8 Matrixed Inverters

The inverter matrix test structure consists of 225 randomly accessible inverters and is used for inverter parameter variability analysis [8]. This structure can also be used for inverter defect characterization. The parameters measured by this structure are: Inverter Threshold Voltage (Vinv), Inverter GAIN, Vhigh, Vlow, and Noise Margin, Vnm = $(1 - 1/\text{GAIN}) \times V$inv.

2.2.9 Matrixed Transistors

The initial Transistor Matrix test structure consists of 2600 randomly accessible n-channel transistors. A p-channel pull-up transistor is associated with each row of the matrix and can be used as a pull-up transistor to form an inverter

with the n-channel transistors. The transistor matrix is used for parameter variability analysis and for characterization of process faults and their effects on transistor parameters. The transistor parameter measurements are time consuming; therefore, the transistors are combined with the pull-up devices to form inverters. The inverter threshold measurement is fast and is used as an initial test. When problems are detected in this preliminary test, more extensive tests can follow.

The initial transistor matrix is somewhat limited in that only d.c. parameters can be tested and analyzed: gate oxide pinholes, for example, are not expected to show up in the d.c. parameters. To locate these defects the transient transistor behavior must be monitored and timing analysis must be performed. Also, a complete oxide Pinhole Test is needed to characterize any oxide defects detected.

A new transistor matrix was designed to overcome these limitations. Figure 2.21 shows the circuit schematic of this test structure and its five modes of operation. These operational modes make it possible to perform all transistor and inverter matrix functions. The five modes of operation of the new transistor matrix structure are as follows:

1. Gate oxide integrity: A quick test to detect whether any oxide defects exist.

2. Transistor d.c. parameter extraction: Parameter variability analysis.

3. Transistor transient behavior: Timing analysis to locate slow transistors.

4. Gate pinhole characterization: A complete Pinhole Array Capacitor test.

5. Inverter threshold: Parameter variability analysis.

This structure is under development and will be analyzed as time permits.

2.2.10 Fault Chip Summary Results

The Fault Chip is being fabricated on a periodic basis by MOSIS. Three summary reports are included in this section. The first summary was produced for run M61P on Fault Chip No. 3. The M61P summary results are shown in Table 2.8. The Pinhole Array Capacitor and Contact structures were not included in this report because design problems made these structures untestable. The major problem observed is a metal step coverage problem: eleven of twenty metal serpentine wires were open. (Figure 2.22 shows SEM photos of top view and cross section of broken metal serpentine wire of the M61P run.) The metal

Table 2.8: FAULT CHIP ANALYSIS FOR 3-μm CMOS/BULK

Prepared by H. Sayah(hrs), Reviewed by: M. Buehler(mgb), C. Piña(cap)
Date: 4-15-86. Revised 4-21-86.
Report No. 1. Run No. M61P. Fault Chip No. 3
Note: Fault Chip was fabricated twice on each of 10 wafers.

TABLE 1. SUBARRAY DEFECT ANALYSIS

Defect Type	E-value Elements/Defect	Std. Dev.	Sites Bad/Total	Total Elements	Element
a) Comb Resistor: (Shorts)					
Metal-Metal	$> 1.5\times10^6$	-	0/20	4368960	length(1μm)
Poly-Poly	$> 2.1\times10^6$	-	0/20	6529440	length(1μm)
b) Serpentine Resistor: (Opens)					
Metal Wire	2.3×10^4	-	11/20	369000	steps(6 μm)
Poly Wire	$> 3.7\times10^5$	-	0/20	366000	steps(9 μm)

TABLE 2. PARAMETER VARIABILITY ANALYSIS

Parameter (Dimensions)	Average Value	Std. dev.	Points Incl/Excl
a) Cross-Bridge Resistor:			
Metal Linewidth (μm)(4.5 μm)	3.06	0.32	20/0
Poly Linewidth (μm)(3.0 μm)	3.03	0.23	20/0
Metal Sheet Resistance($m\Omega/\square$)	33.	3.	20/0
Poly Sheet Resistance($\Omega/\square$)	14.6	1.1	20/0
b) Transistor/Inverter Matrix: (2500 Transistors/Chip)			
Chip# 1:Inverter VT(V)	2.44	0.08	20/0
Chip# 2:Inverter VT(V)	2.45	0.07	19/0
c) Floating Gate n-channel Transistors: (W/L = 6.0 μm/3.0 μm)			
Initial Gate Voltage (V)	0.18	-	4/0

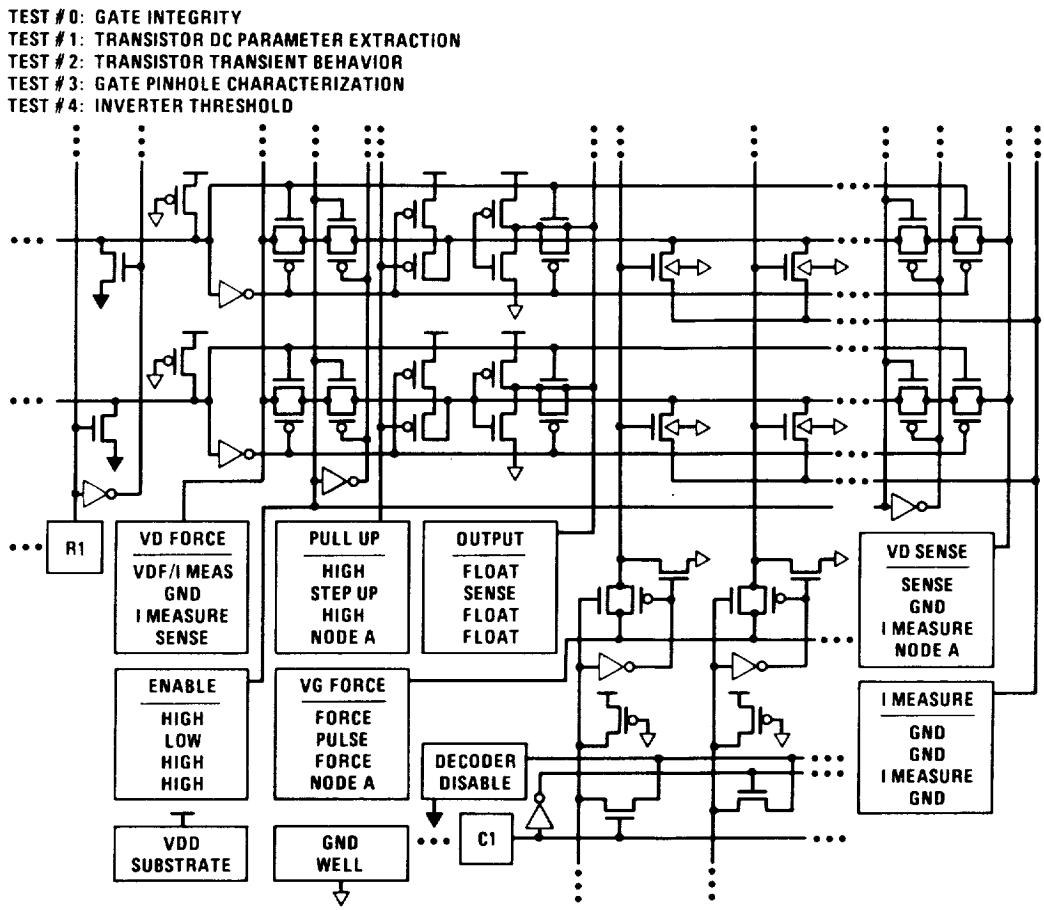
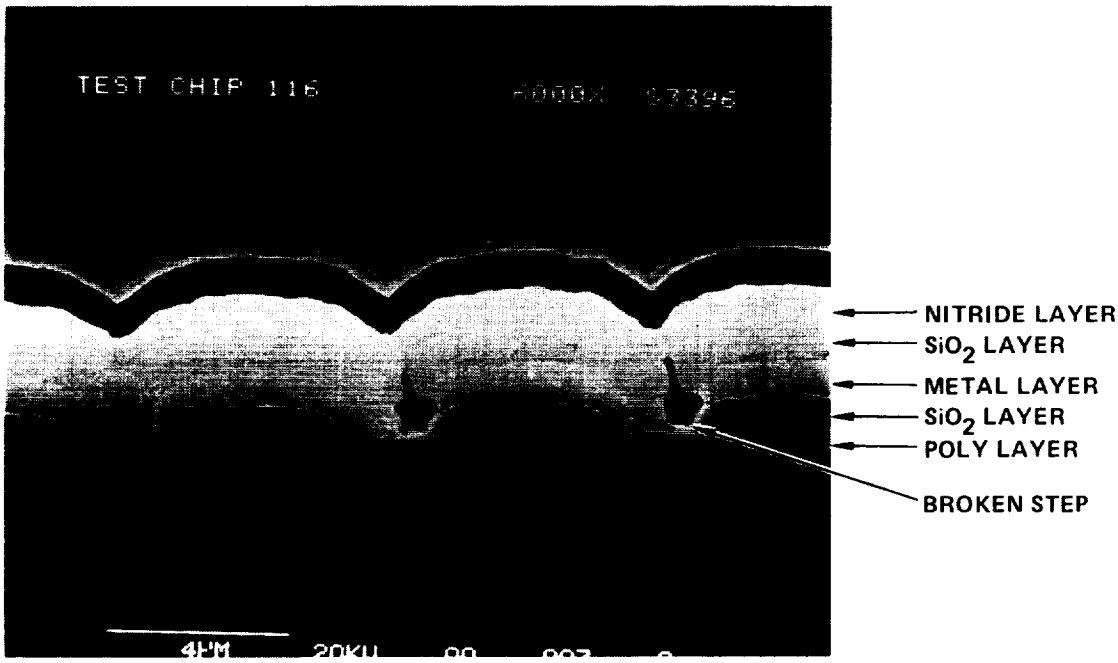


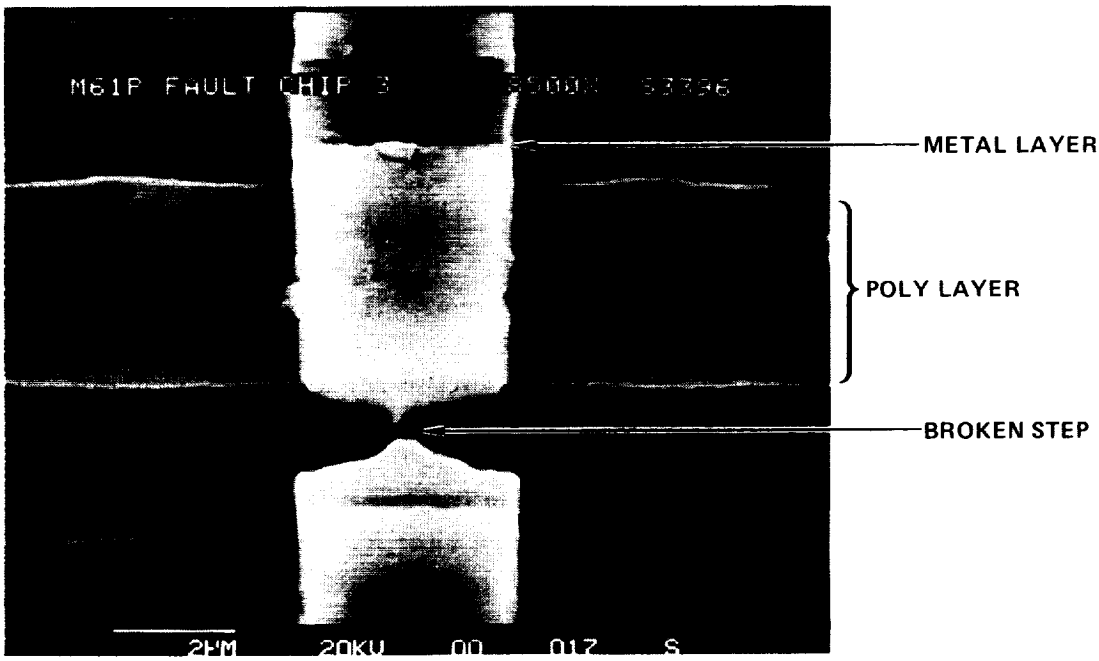
Figure 2.21: Transistor Matrix test circuit.

linewidths are undersized. As reported in Table 2.8 the nominal linewidth is 4.5 μm; whereas the measured linewidth is 3.06 μm. This may have contributed to the problem. No other defects were observed on this run and all other parametric results are normal.

The second summary report was produced for run M62Z on Fault Chip No. 5. The M62Z summary results are shown in Table 2.9. Gate oxide defects are prominent in this run: Nine out of eighteen sites have p-type gate oxide defects and two out of eighteen sites have n-type gate oxide defects. The effect of these defects on transistor performance has not yet been precisely determined. However, simulation lends evidence that these defects degrade the timing performance of active elements. The extent of such degradation depends on the defect resistance, type, and associated circuitry. The other notable information



a) CROSS-SECTION SEM PHOTO



b) TOP VIEW SEM PHOTO

Figure 2.22: Cross section and top view SEM photos of the broken metal serpentine wire of run M61P.

Table 2.9: FAULT CHIP ANALYSIS FOR 3-μm CMOS/BULK

Prepared by H. Sayah(hrs), Reviewed by: M. Buehler(mgb), C. Piña(cap)
Report No. 2. Run No. M62Z. Fault Chip No. 5. Date: 5-28-86
Note: Fault Chip was fabricated twice on each of 9 wafers.

TABLE 1. SUBARRAY DEFECT ANALYSIS

Defect Type	E-value Elements/Defect	Std. Dev.	Sites Bad/Total	Total Elements	Element
a) Comb Resistor (Shorts):					
Metal-Metal	$> 1.3\times10^6$	-	0/18	3932064	length(1 μm)
Poly-Poly	$> 1.9\times10^6$	-	0/18	5876496	length(1 μm)
b) Serpentine Resistor (Opens):					
Metal Wire	$> 3.3\times10^5$	-	0/18	332100	steps(6 μm)
Poly Wire	$> 3.2\times10^5$	-	0/18	329400	steps(9 μm)
c) p-Pinhole Array Cap.:					
Metal-Poly Shorts	2.5×10^6	2.7×10^6	1/18	1630944	capacitor
Gate Ox. Defects	9.1×10^5	5.3×10^5	2/18	1630944	transistor
d) n-Pinhole Array Cap.:					
Metal-Poly Shorts	$> 6.8\times10^5$	-	0/18	1630944	capacitor
Gate Ox. Defects	1.2×10^5	1.3×10^4	9/18	1630944	transistor

TABLE 2. PARAMETER VARIABILITY ANALYSIS

Parameter (Dimensions)	Avg. Value	Std. Dev.	Prob. of Open	Points Incl/Excl
a) Cross-Bridge Resistor:				
Metal Linewidth(μm)(4.5μm)	2.67	0.08	-	18/0
Poly Linewidth (μm)(3.0μm)	2.94	0.13	-	18/0
Metal Sheet Res. ($m\Omega/\square$)	30.	1.	-	18/0
Poly Sheet Res. ($\Omega/\square$)	14.1	0.59	-	18/0
b) Contact Array Resistor (Contact size: 3.0 μm)				
p+Poly/Metal (Ω)	-	-	1.95×10^7	144/0
n+Poly/Metal (Ω)	-	-	5.42×10^7	144/0
p+Diff/Metal (Ω)	-	-	1.53×10^6	144/0
n+Diff/Metal (Ω)	-	-	1.15×10^8	144/0

for this run is the undersized metal linewidth. The nominal wire width is 4.5 μm; the measured linewidth was 2.67 μm. However, no metal step coverage problems were observed due to the undersized metal wire.

The third summary was produced for run M63E on Fault Chip No. 5. The M63E summary results are shown in Table 2.10. From the summary report it is seen that twelve of twenty-eight sites have p-type gate oxide defects and four out of twenty-eight sites have n-type gate oxide defects. As explained previously, this type of defect could degrade the timing performance of circuits fabricated during this run.

Another observation relates to defective Diffusion/Metal contacts. The probability of occurrence of an open contact is significantly higher than in previous runs. Further, the metal linewidths are again undersized. The nominal is 4.5 μm and the measured was 2.81 μm. No metal step coverage problems were observed as a result of metal linewidth undersizing.

2.2.11 Fault Prioritization Process

It is of major significance that the defect densities generated in the Fault Chip summary reports can be used to prioritize likelihood of faults for a specified circuit based on layout geometry. Since the geometry and the number of basic cell elements are not the same for different circuits, the responses of these circuits to the process defects are different. For example, a circuit with no adjacent poly to poly layers will not experience any poly to poly layer shorts, no matter how bad the process control. Therefore, the priority of poly to poly shorts for this circuit is zero. Prioritization of faults is needed for proper design, simulation, and testing of integrated circuits. Figure 2.23 shows the process of fault prioritization. In Figure 2.23 Ei represents the estimated Elements/Defect from the Fault Chip for the ith-type defect, Ni represents the number of the ith-type elements in the specified circuit, and $Di = Ni/Ei$ is the fault priority for the ith-type defect.

For the example circuit specified in Table 2.11, we have prepared a fault priority listing, shown in Table 2.12, based on the results of the Fault Chips from the MOSIS run No. M62Z discussed in Table 2.9. The results in Table 2.12 were scaled using $Di = 10^4 Ni/Ei$. As seen in Table 2.12 the n-type gate oxide defects have the highest priority and are expected to be the major cause of problems for the example circuit.

Table 2.10: FAULT CHIP ANALYSIS FOR 3-μm CMOS/BULK

Prepared by: H. Sayah(hrs), Reviewed by: M. Buehler(mgb), C. Piña(cap)
Report No. 3. Run No. M63E. Fault Chip No. 5 Date: 7-30-86
Note: Fault Chip was fabricated twice on each of 14 wafers.

TABLE 1. DEFECT ANALYSIS

Defect Type	E-value Elements/Defect	Std. Dev.	Sites Bad/Total	Total Elements	Element
a) Comb Resistor (Shorts):					
Metal-Metal	$> 2.0\times10^6$	-	0/28	6116544	length(μm)
Poly-Poly	5.3×10^6	2.9×10^6	2/28	9141216	length(μm)
b) Serpentine Resistor (Opens):					
Metal Wire	7.7×10^4	-	6/28	516600	steps(6μm)
Poly Wire	$> 5.1\times10^5$	-	0/28	512400	steps(9μm)
c) p-Pinhole Array Cap.:					
Metal-Poly Shorts	$> 1.1\times10^6$	-	0/28	2537024	capacitor
Gate Ox. Defects	5.1×10^5	5.9×10^4	4/28	2537024	transistor
d) n-Pinhole Array Cap.:					
Metal-Poly Shorts	1.8×10^6	4.6×10^5	1/28	2537024	capacitor
Gate Ox. Defects	1.3×10^5	7.7×10^3	12/28	2537024	transistor

TABLE 2. PARAMETER VARIABILITY ANALYSIS

Parameter (Dimensions)	Avg. Value	Std. Dev.	Prob. of Open	Points Incl/Excl
a) Cross-Bridge Resistor:				
Metal Linewidth (μm)(4.5μm)	2.81	0.12	-	28/0
Poly Linewidth (μm)(3.0μm)	2.72	0.18	-	28/0
Metal Sheet Res. ($m\Omega/\square$)	28.7	1.04	-	28/0
Poly Sheet Res. ($\Omega/\square$)	12.3	0.77	-	28/0
b) Inverter Matrix ($Wn/Ln = 4.5/3.0, Wp/Lp = 6.0/3.0$):				
Vinv (V)	2.35	0.03	-	5692/329
Gain	-19.0	1.04	-	5692/329
Vlow (mV)	0.11	0.28	-	5692/329
Vhigh (V)	4.99	0.01	-	5692/329
c) Contact Resistor Array (Contact size: 3.0μm):				
p+Poly/Metal (Ω)	3.38	0.87	2.7×10^{-10}	224/0
n+Poly/Metal (Ω)	2.14	0.64	2.1×10^{-7}	224/0
p+Diff/Metal (Ω)	6.21	2.07	4.2×10^{-4}	224/0
n+Diff/Metal (Ω)	4.48	1.19	4.7×10^{-5}	224/0
d) Open-Gate n-Transistors ($W/L = 6\ \mu m/3\ \mu m$):				
Initial Gate Voltage (V)	0.16	0.05	-	4/0

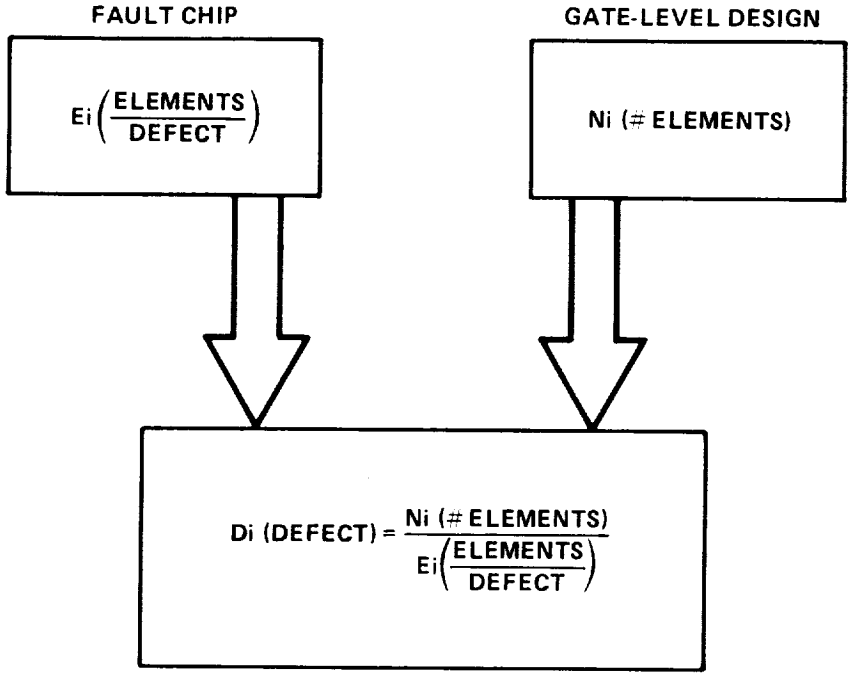


Figure 2.23: Fault prioritization process. Di represents the priority of the ith defect.

2.2.12 Circuit Timing Degradation Due to Gate Oxide Pinholes

The fault information gathered from the Fault Chip was used to develop fault models for circuit simulators such as SPICE. Fault model development is essential for proper simulation of circuits [9]. From the results of the Pinhole Array Capacitor test structures we have introduced fault models for n- and p-channel gate oxide defects. Figure 2.24 shows the proposed models for gate oxide defects of n- and p-channel transistors. The p-channel results were calculated using a bulk resistance of 1000 Ω.

In order to study the effects of these defects on the performance of logical circuits we have conducted a simulation experiment. In this experiment the gate-to-drain and gate-to-source defects are ignored; only gate-to-channel defects are studied. A more complete simulation using the same n-channel fault model and including all of the possible short defects has been prepared by Fail-Safe Technology [10] for the Jet Propulsion Laboratory. The circuit configurations used for n- and p-channel transistor fault simulation are shown in Figures 2.25

Table 2.11: Example circuit with a selected number of circuit elements.

	No. Elements	Elements
1.	10,000	transistors
2.	10,000	(μm) Metal to Metal adjacent length
3.	10,000	(μm) Poly to Poly adjacent length
4.	10,000	Poly over diffusion steps
5.	10,000	Metal over Poly and diffusion steps
6.	10,000	p+Poly/Metal contacts
7.	10,000	n+Poly/Metal contacts
8.	10,000	p+Diff/Metal contacts
9.	10,000	n+Diff/Metal contacts

and 2.26. The faulty transistor is embedded between two minimum size transmission gates to simulate practical circuit situations. The output of the faulty transistor is precharged and the faulty transistor is required to pull its output to the rail (either VDD or ground). The time it takes to pull its output to the rail is noted for each value of pinhole resistance. The circuit simulator used for this experiment is PRECISE, a commercial version of SPICE. The pinhole short resistances vary from 4 to 1000 kΩ for n-channel transistors and from 0.8 to 1000 kΩ for p-channel transistors as smaller values than these lead to circuit performance failures.

Figure 2.27 shows the timing performance of the circuit versus the pinhole short resistance value. As seen from Figure 2.27, smaller values of pinhole short resistance cause greater degradation in timing performance, until the circuit ceases to switch. As seen in Figure 2.27, the n-channel fault model does not switch for pinhole resistance values smaller than about 4.5 kΩ and the p-channel fault model does not switch for pinhole short resistance values smaller than about 0.7 kΩ. From the Pinhole Array Capacitor test results we have observed that the pinhole short resistances are between 10 and 100 kΩ. As shown in Figure 2.27, the pinhole resistance of 10 kΩ degrades the performance of the n-channel model by 4.5 ns and the p-channel model by 1 ns. Although the short resistance values in the range of 10 to 100 kΩ are not sufficiently significant to cause drastic performance degradation on the circuits used for this experiment, it must be noted that different circuits have different responses to such defects. The performance of transistors with pinhole short defects depends to a great

Table 2.12: Priority listing of likely defects for the example circuit and Run M62Z shown in Table 2.9.

Defect	Estimated Priority	
Metal-Metal shorts	< 77	
Poly-Poly shorts	< 52	
Metal wire opens	< 301	
Poly wire opens	< 304	
Metal-Poly shorts	40	
p-type Gate Oxide defects	110	
n-type Gate Oxide defects	833	< – MAX
p+Poly/Metal contacts	20	
n+Poly/Metal contacts	54	
p+Diff/Metal contacts	153	
n+Diff/Metal contacts	1	< – MIN

extent on the current drive of the circuitry driving the faulty transistor. The driver used in this experiment is a transmission gate composed of minimum geometry n- and p-transistors.

A major accomplishment of this report period is the development of fault models for circuit simulators such as SPICE. The valid range of the fault models is derived from the PAC structures of the Fault Chip, and is used to simulate the effects of these defects on the circuit of interest.

2.2.13 Fault Chip Testing

The Fault Chips are tested by our automated wafer prober and parametric data acquisition system, shown in Figure 2.28. To aid in chip testing of unpackaged Fault Chips with a wafer prober, a special Slotted-Chuck was developed. A vacuum pump is used to hold the Slotted-Chuck and the chips in a fixed location on the stage of the wafer prober. Thus it is possible to move the prober from chip to chip for extended automated testing. Figure 2.29 shows the Slotted-Chuck loaded with Fault Chips and ready for testing. The Slotted-Chuck is a circular, gold-plated, brass plate with a five-inch diameter, a 75 mil thickness and 3-7.4 mm wide slots to accommodate 48-7.1 mm × 7.1 mm unpackaged chips.

The Slotted-Chuck has undergone two major design revisions during its de-

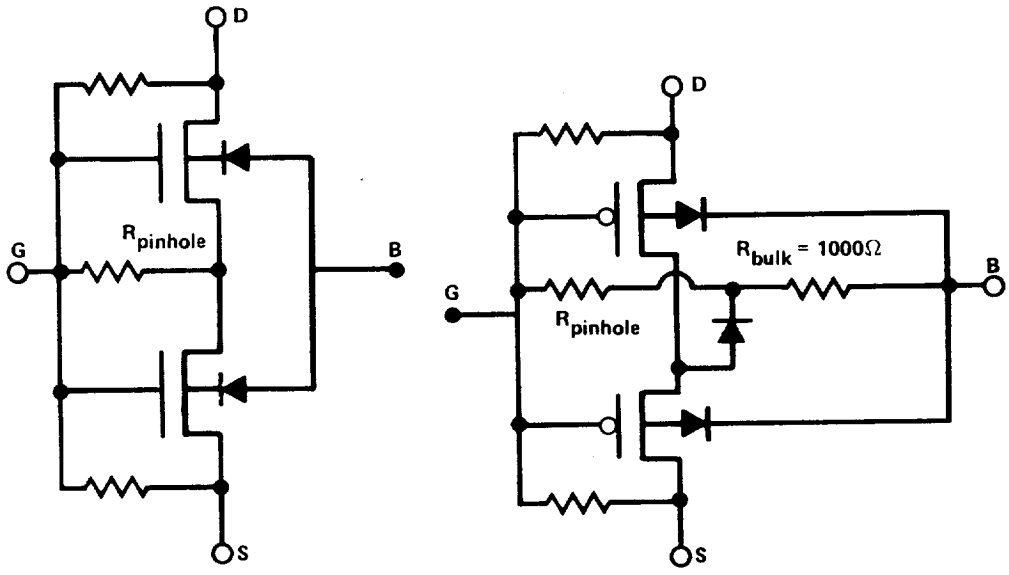


Figure 2.24: Fault models for n- and p-channel devices.

velopment period. The first revision was to reduce the weight of the Slotted-Chuck to alleviate a problem with the Slotted-Chuck sliding when the stage was moved. The second was to reduce the diameter of the vacuum holes to 10 mils to ensure proper vacuum was achieved.

After the chips are loaded on the Slotted-Chuck and placed on the wafer prober, we manually determine the location of the chips and store the chip location information in the computer memory. This information is then used by the test procedures to locate and test the structures on the chips.

Note that to avoid electrostatic discharge and oxide breakdown, a grounded wrist strap must be worn during loading and unloading of the chips.

2.2.14 Future Work

The Fault Chip is in the process of development. All test structures have been debugged and are fully functional except for the new transistor matrix and the Contact Chain Matrix Structures.

The transistor matrix structure is designed but not yet implemented in sil-

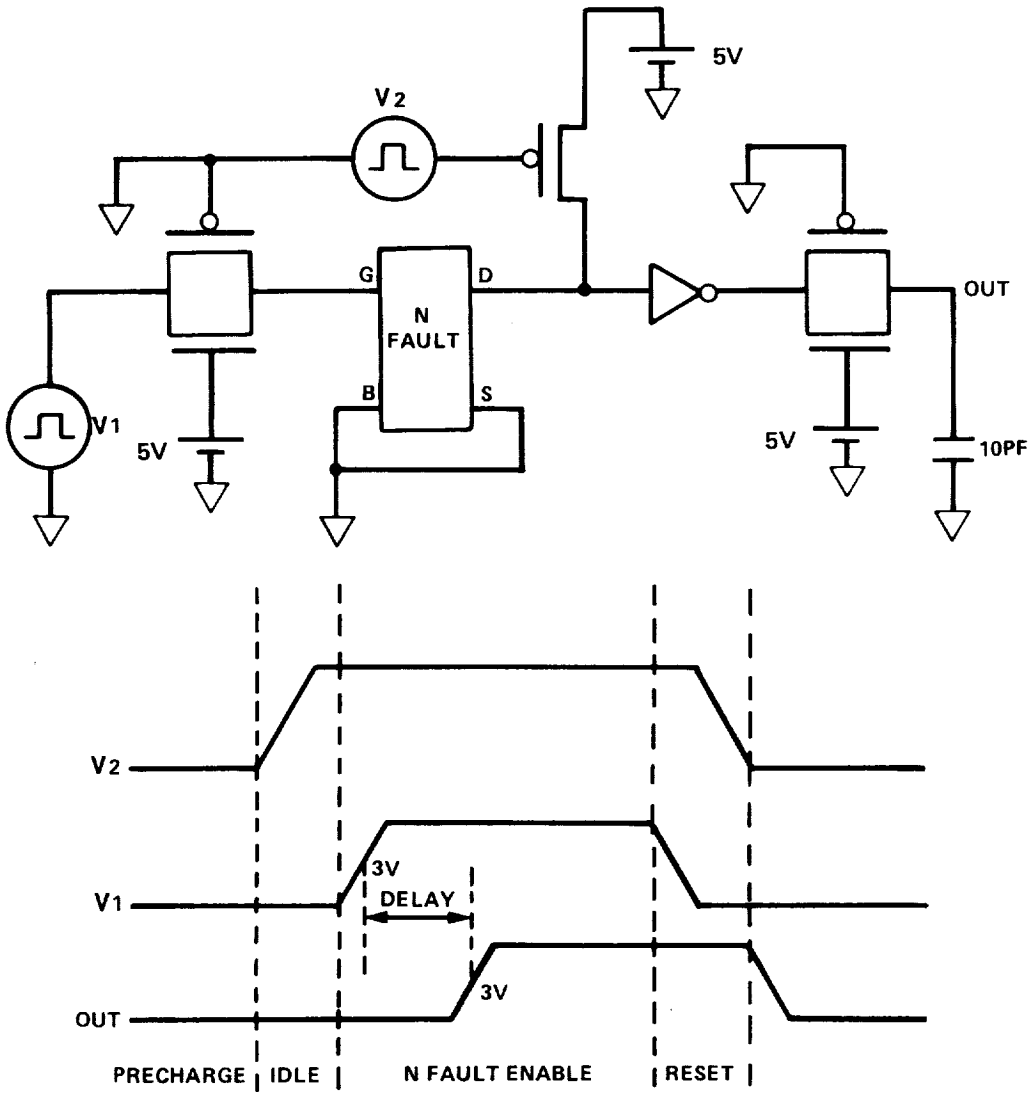


Figure 2.25: Circuit configuration and timing table used for simulating faulty n-channel transistors.

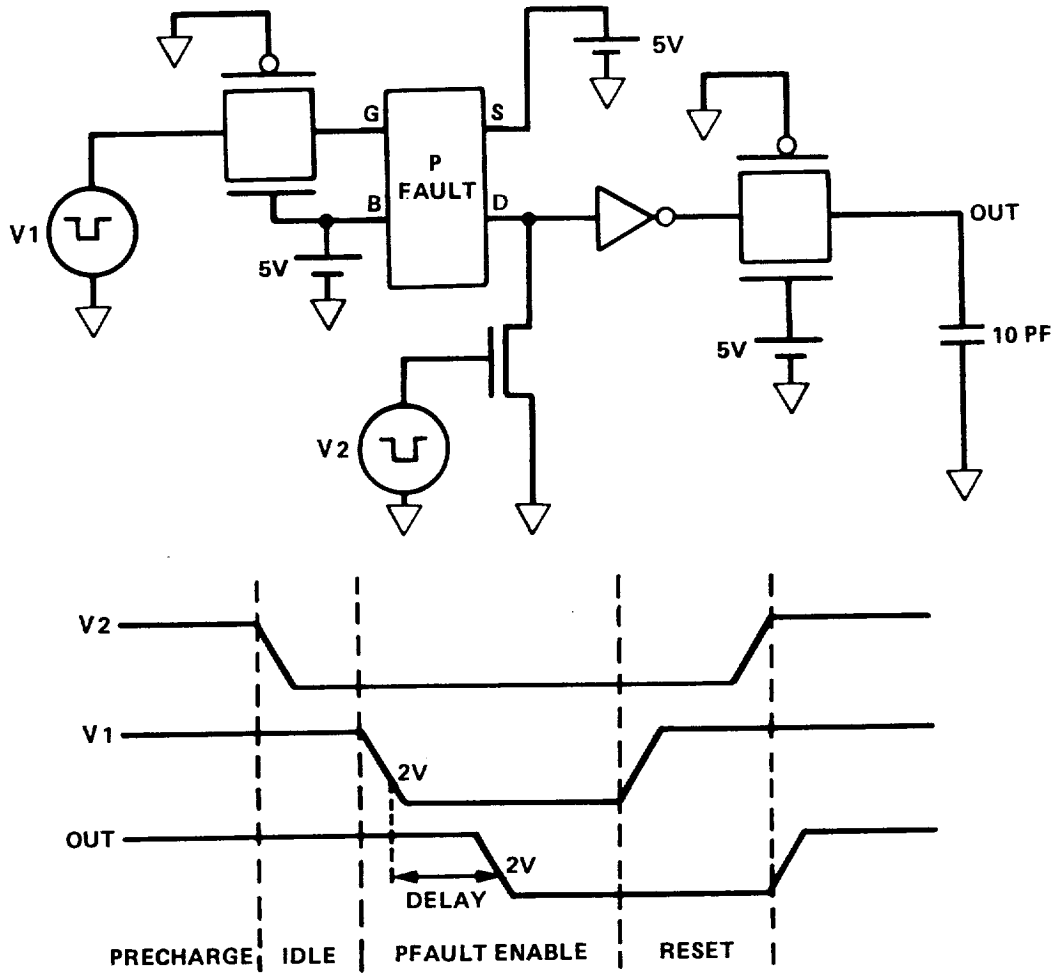


Figure 2.26: Circuit configuration and timing table used for simulating faulty p-channel transistors.

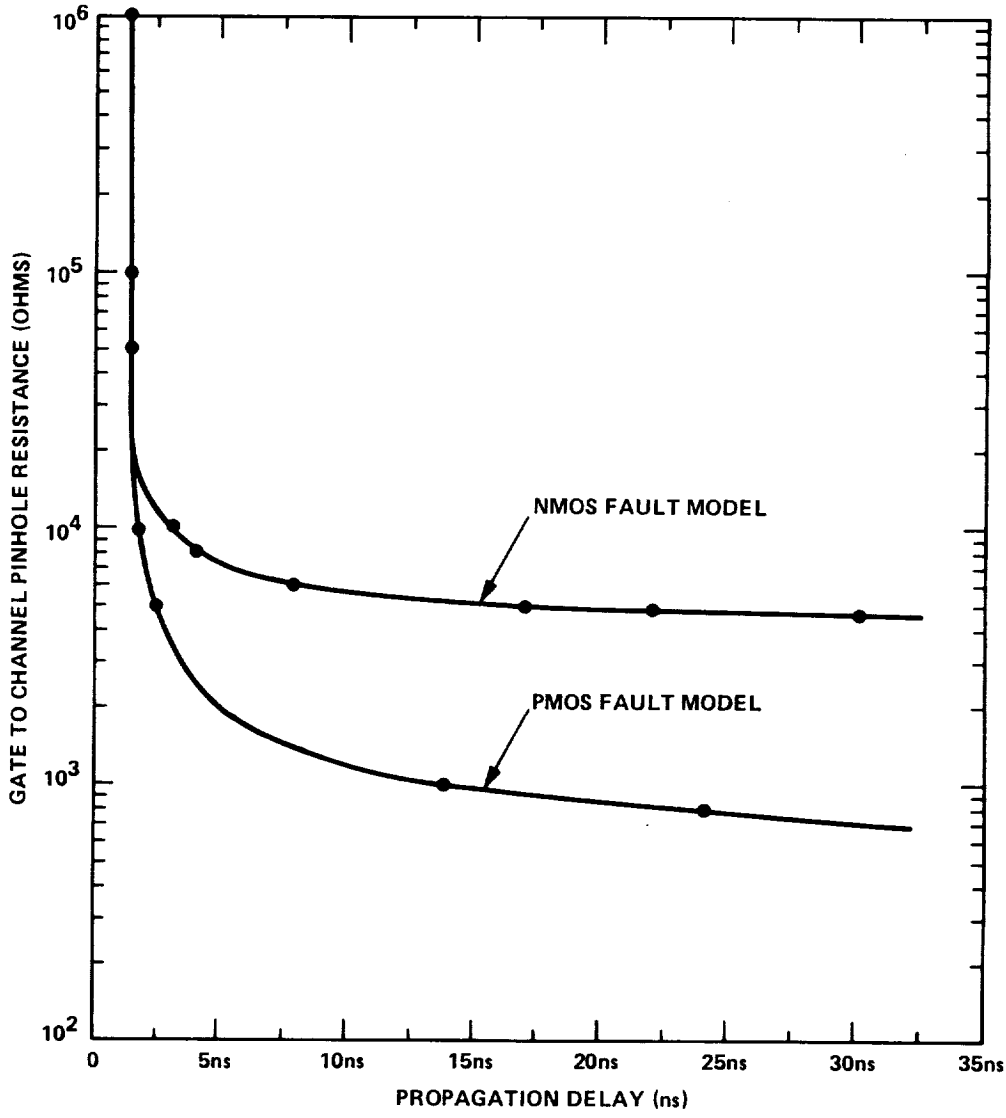


Figure 2.27: Change in propagation delay of n- and p-channel transistors due to gate oxide pinhole resistance. These typical pinhole resistances were derived from PAC test structures.

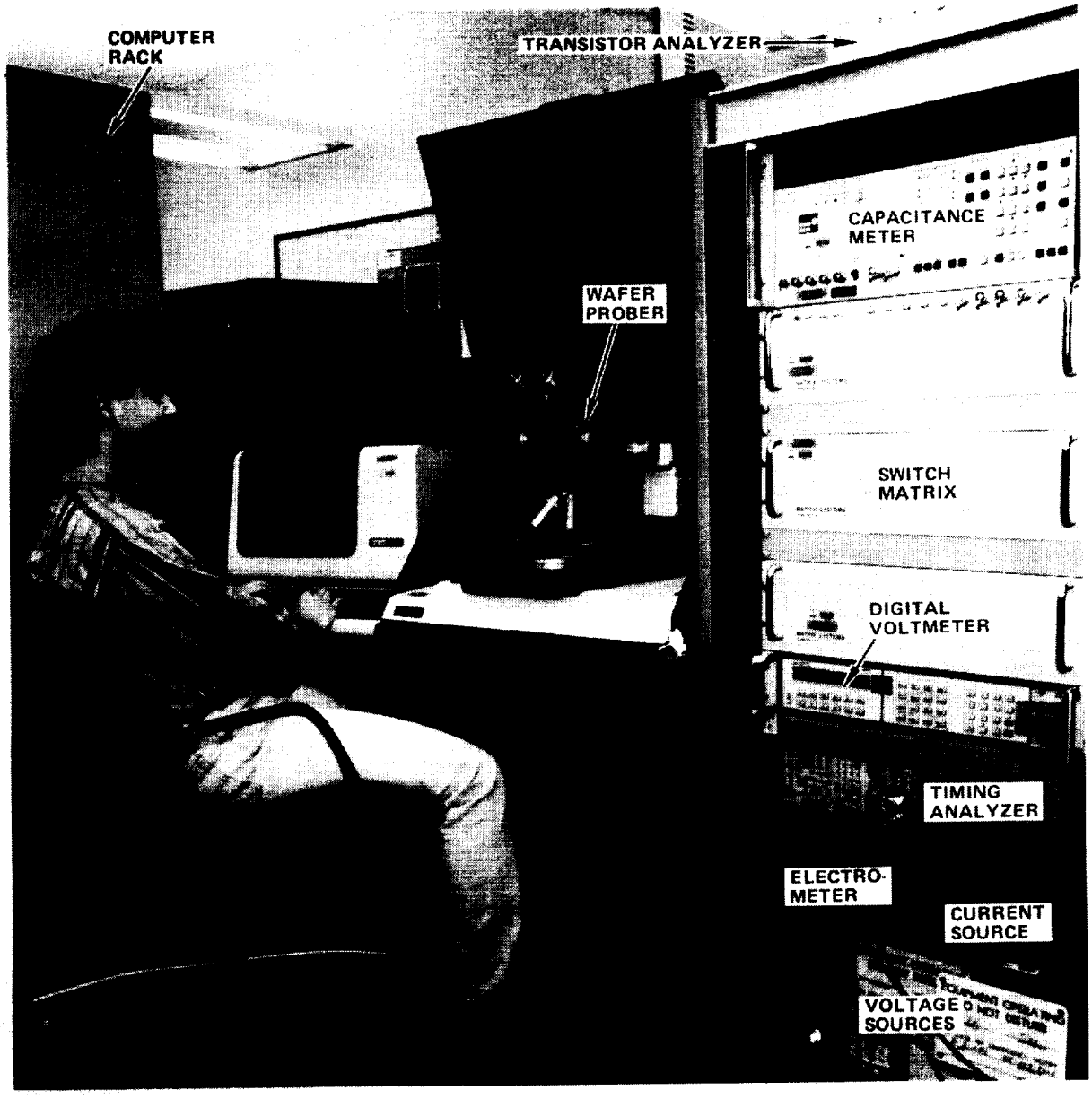


Figure 2.28: Automated wafer prober and parametric data acquisition system.

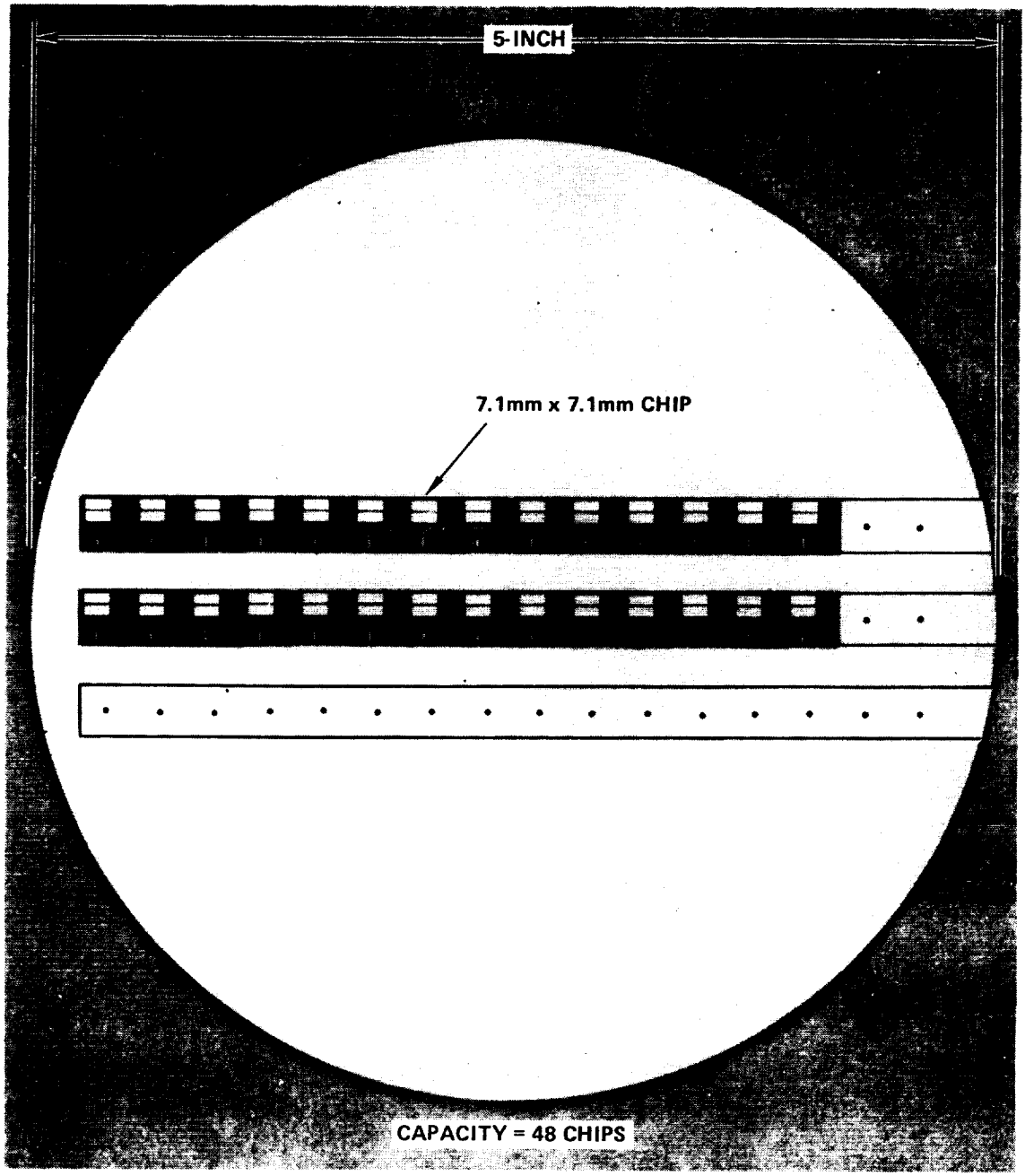


Figure 2.29: Slotted-chuck chip holder for automated chip testing.

icon. The transistor matrix will be used to monitor the transient behavior of the transistors. When completed, it is expected to provide us with valuable information on the performance of transistors with pinhole defects.

The Contact Chain Matrix is available on the latest Fault Chip design but has not yet been tested. The Contact Chain Matrix Structure will provide sufficient statistical points to perform contact probability analysis on individual chips.

The floating gate transistors and inverters also need more study and experimentation. New designs are included on Fault Chip No. 7 which should provide an improved understanding of floating gate transistor behavior.

2.2.15 Conclusion

JPL has developed a Fault Chip for characterizing defects found in a 3-μm CMOS bulk process; in addition, the structures can be used to analyze even finer line technologies. Defect characterization is essential to proper integrated circuit design, simulation, and testing. When the Fault Chip is fully developed it will be used in conjunction with foundry wafer acceptance procedures to allow wafers to be tested against wafer fabrication process requirements. By studying Fault Chip results we have characterized metal-poly oxide, gate oxide, single layer short and open contacts, and floating gate transistor faults. The statistical information from the Fault Chip is used to prioritize faults, and to identify both those faults that are most common in a given process, and those faults that are most detrimental to given circuit designs.

Chapter 3

Test Structures

3.1 Gate Oxide Capacitors

3.1.1 Introduction

Some of the most important parameters obtained from test chips come from the measurement of the gate oxide capacitance. These parameters, to be used in device or circuit simulators such as SPICE, include the gate oxide thickness, edge capacitance, oxide charge, bulk dopant density, etc.

Several approaches are used for this measurement in VLSI processes. The simplest method uses a MOS capacitor which is large enough so that the edge effects can be ignored. The measured quantities are C_b, the silicon body capacitor, and C_{ox}, the oxide capacitor. In this structure, errors can be introduced due to a large series resistance in the structure. A second technique uses a minimum geometry device and an "on-chip" amplifier [11,12,13,14] to measure C_{ox}. The disadvantages of this technique are increased test structure complexity and a requirement for on-chip analog circuitry that is typically not available in a fabrication process intended for digital ICs. A third method uses a MOSFET with large W/L ratio, so the critical dimension, the gate length, is near minimum but the total capacitance (area + edge) is large enough to be directly measured. This section will describe a method which combines the third method with a differential technique to eliminate offset capacitors [15]. A closed geometry structure eliminates end effects and an inversion measurement technique separates the various capacitances. This method allows the measurement of the gate oxide thickness and provides an upper bound for the edge capacitance.

3.1.2 Theory

For an ideal parallel plate capacitor, the capacitance is given by:

$$C = \frac{\epsilon A}{T}$$

where A is the area of the plates, T is the spacing between the plates, and ϵ is the permittivity of the insulating material and is given by $\epsilon = k\epsilon_0$ where k is the dielectric constant of the insulating material between the plates and ϵ_0 is the permittivity of free space.

In a MOSFET, there are effectively two parallel plate capacitors under the gate which are in series: C_b, the silicon bulk capacitor, which is voltage dependent, and C_{ox}, the oxide capacitor, which is voltage independent. The oxide

capacitance is given by

$$C_{ox} = \frac{\epsilon A}{T_{ox}}$$

where T_{ox} is the thickness of the oxide layer and A is the effective gate area. The capacitance under the gate is

$$C_a = \frac{C_{ox}C_b}{C_{ox} + C_b}$$

which is the series combination of C_{ox} and C_b and depends on the gate area.

In the MOSFET, there is also an edge capacitor, C_{go}, which is the capacitance between the gate and source/drain and is generally voltage and perimeter dependent.

Therefore, for a MOSFET test structure capacitor, the measured capacitance, C_m, is given as the sum of three capacitors:

$$C_m = C_a + C_{go} + C_{off}$$

where C_{off} is a voltage independent offset capacitor formed by the connection between the gate and probe pad and other instrumentation capacitances.

3.1.3 Capacitor Structure Design

To design an appropriate test structure to determine the capacitors C_a and C_{go} we must recognize that we can rewrite the above equation as

$$C_m = C'_a A + C'_{go} P + C_{off}$$

where C'_a is the capacitance per unit area, A is the area of the capacitor plate, C'_{go} is the capacitance per unit length and P is the periphery of the capacitor. If the capacitor is measured for the gate biased such that C_b is zero, then

$$C_m = (\frac{\epsilon}{T_{ox}})A + C'_{go} P + C_{off}$$

In this analysis, T_{ox} is determined from

$$T_{ox} = \frac{\epsilon W}{\left(\frac{dC}{dA}\Big|_{\mathrm{P\ =\ constant}}\right)}$$

where $\epsilon(SiO_2) = 34.5 \times 10^{-6}\,\mathrm{pF}/\mu\mathrm{m}$ is the permittivity of the gate oxide. Notice that T_{ox} can be obtained without knowing the absolute area of the structure.

Thus, errors due to the bloating and shrinking of features during fabrication are eliminated. The slope of the C_m vs. A curve is dC/dA and the intercept of this curve yields a value for $C_{go} + C_{off}$, the total capacitance due to the peripheral and offset capacitances.

This method requires the use of special test structures where the area of the structure is varied while keeping the periphery constant. Two structures that exploit this technique were designed and fabricated. Each of these structures is a closed geometry MOSFET which eliminates end capacitance effects. The description of each of these structures follows.

Annular MOSFET

The annular MOSFET is shown in Figure 3.1. The center of the gate is located on a circle of radius r. The inner and outer edges of the gate are located a distance $t/2$ from the center of the gate. Thus the gate length $L = t$. The total perimeter of the gate is given by

$$P = 2\pi(r - t/2) + 2\pi(r + t/2) = 4\pi r = \text{constant}$$

The area of the gate is

$$A = 2\pi rt$$

Note that for a fixed r and a variable t, P is constant and A varies linearly with t. The gate width is defined as $W = 2\pi r$ and the gate length is defined as $L = t$. In this study n- and p-MOSFETS with $W = 339.3\,\mu$m and and L of 6.0, 9.0, and 12.0 μm were fabricated and tested.

Racetrack MOSFET

The racetrack MOSFET shown in Figure 3.2 is topologically isomorphic to the annular MOSFET and was designed to fit inside a 2×10 pad array. The gate area is expressed as

$$A = W \times L$$

where W is the width of the polysilicon gate centerline and is the same for all test structures. L is the length of the gate and varies from structure to structure. For this study, n- and p-MOSFETs with $W = 1335\,\mu$m and L of 9.0, 13.5, 18.0, and 22.5 μm were fabricated and tested.

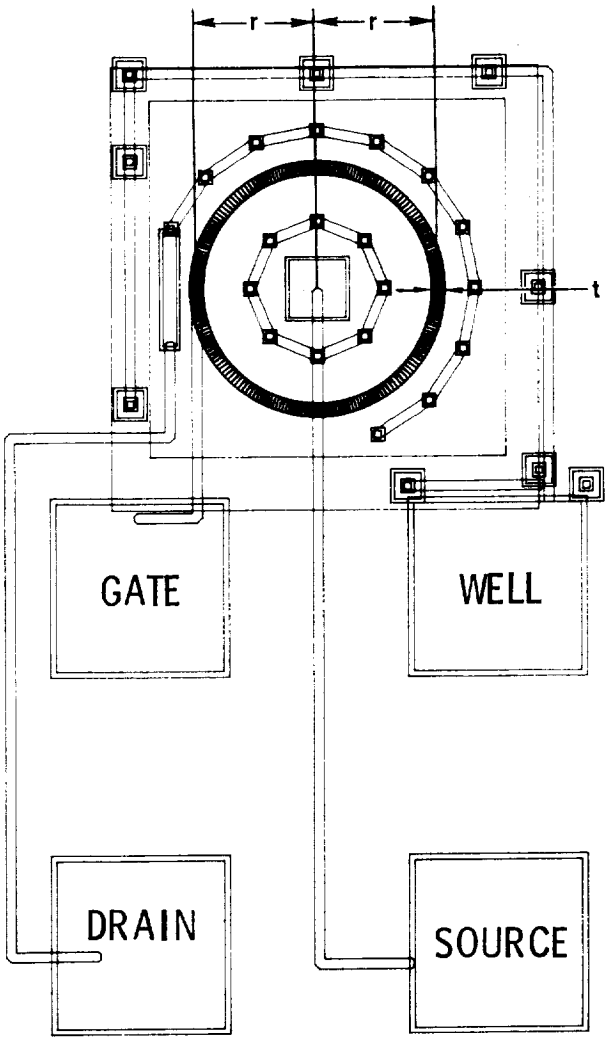


Figure 3.1: The Annular MOSFET capacitor test structure.

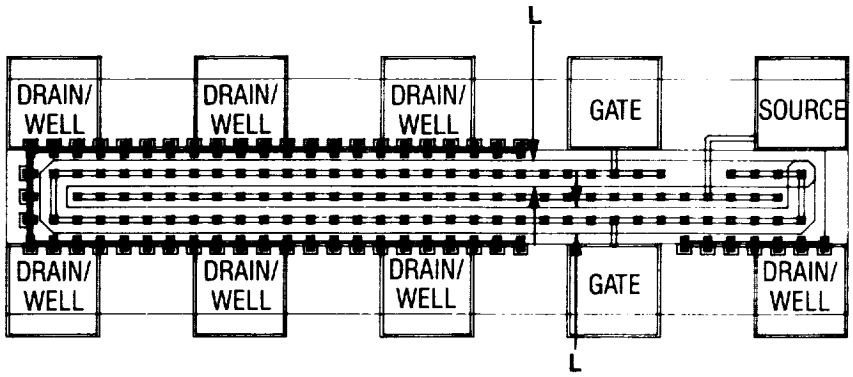


Figure 3.2: The Racetrack MOSFET capacitor test structure.

3.1.4 Measurement Techniques

An inversion layer measurement technique and the typically used accumulation measurement technique [16, for example] were used in this study. Based on the type of data desired, each of these techniques has advantages and disadvantages, which will be described below. The measurements use an HP4192A Impedance Analyzer connected to the capacitor under test through a switch matrix in a three terminal measurement configuration.

Inversion Method

When the device being tested is connected as shown in Figure 3.3, C_{ox}, C_{go}, and C_{off} can be measured directly. In this method, C_{go} can be separated from C_{off} and C_b is eliminated by grounding the body. In addition, the probe pad capacitance, C_{gb}, is eliminated by grounding the body. The measurement of C_{ox}, C_{go}, and C_{off} is accomplished by biasing the structure into three different conducting states as shown in Figure 3.4. As is seen in Figure 3.4a, when the structure is biased into inversion switches S1 and S2 (Figure 3.3) are closed and C_{ox}, C_{go}, and C_{off} are measured in parallel. When the body is depleted (Figure 3.4b), C_{ox} is decoupled from the measurement so only $C_{go} + C_{off}$ is measured. Finally, when the body is in strong accumulation, C_{off} alone is measured (Figure 3.4c).

For example, consider the measurement of an n-MOSFET. For this type of device a negative bias on the gate is applied to obtain surface accumulation and

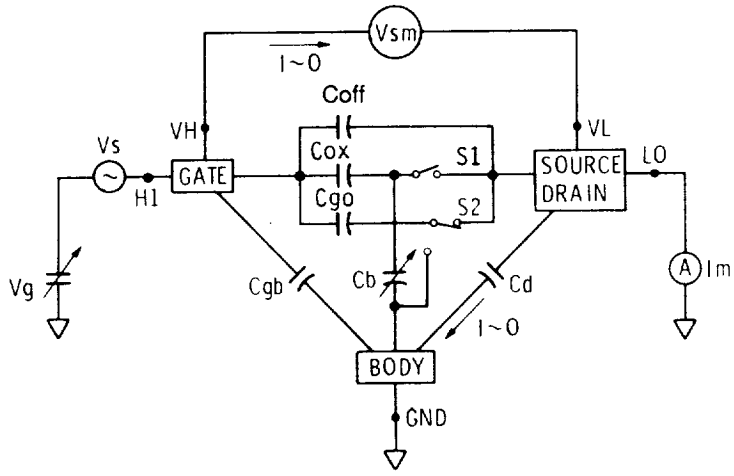


Figure 3.3: Connections to the Device Under Test while using the inversion method of measuring the capacitance.

a positive gate bias to obtain surface inversion. Figure 3.5 shows a capacitance-voltage curve for an n-MOSFET obtained using this technique. When the surface is strongly inverted (defined at VG = 5V), the oxide capacitance C_{ox} is connected to the device source and drain terminals through the channel formed under the gate. The measured capacitance is:

$$C_1 = C_{ox} + C_{go} + C_{off}$$

When the surface is depleted (defined at $VG = 0$), the measured capacitance is

$$C_2 = C_{go} + C_{off}$$

On the other hand, when the surface is accumulated (defined at $VG = -5V$), the oxide capacitance C_{ox} is decoupled from the measurement terminals by the source/drain pn junctions and only the offset capacitance, C_{off}, is measured. Thus,

$$C_3 = C_{off}$$

so one can measure C_{ox}, C_{go}, and C_{off} independently on one structure. That is, $C_{ox} = C_1 - C_2$ and $C_{go} = C_2 - C_3$.

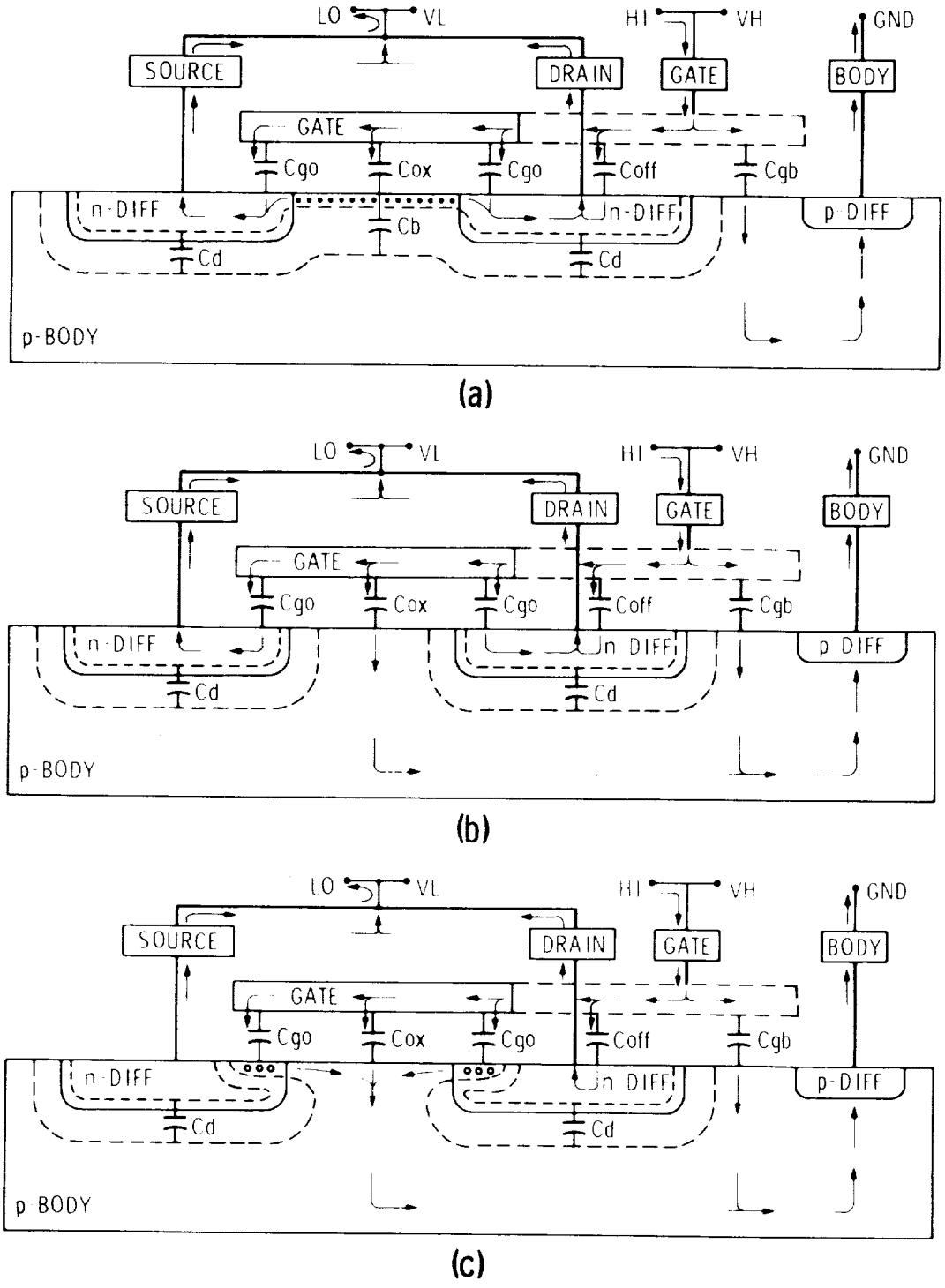


Figure 3.4: n-MOSFET behavior observed while using the inversion method of measuring the oxide capacitance, C_{ox}. (a) shows the device in inversion, (b) is the device in depletion, and (c) is the device in accumulation.

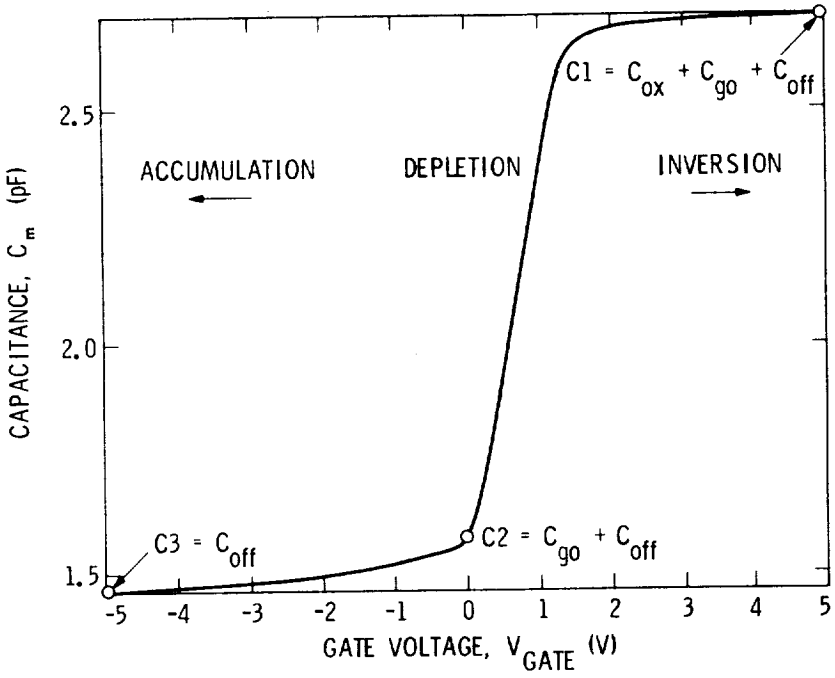


Figure 3.5: Capacitance-Voltage curve for an n-MOSFET measured using the inversion method.

An alternative method is shown in Figure 3.6 where the inversion capacitance, C_{mi}, is plotted as a function of the as-drawn gate length, L, for the annular MOSFETS described earlier. The slope yields C_{ox} and hence the oxide thickness and the intercept yields $C_2 = 1.28$ pF. To more accurately determine C_2, the data should be plotted against $L - \Delta L$, which in this case is 1.5 μm. This leads to $C_2 = 1.60$ pF, which is close to the C_2 value shown in Figure 3.5.

Accumulation Method

In making this measurement, the capacitor under test is connected as in Figure 3.7. A cross section of the MOSFET in its channel inversion and accumulation regions of operation is shown in Figure 3.8. This has long been a standard method for measuring the capacitance of MOS devices. In this measurement, the

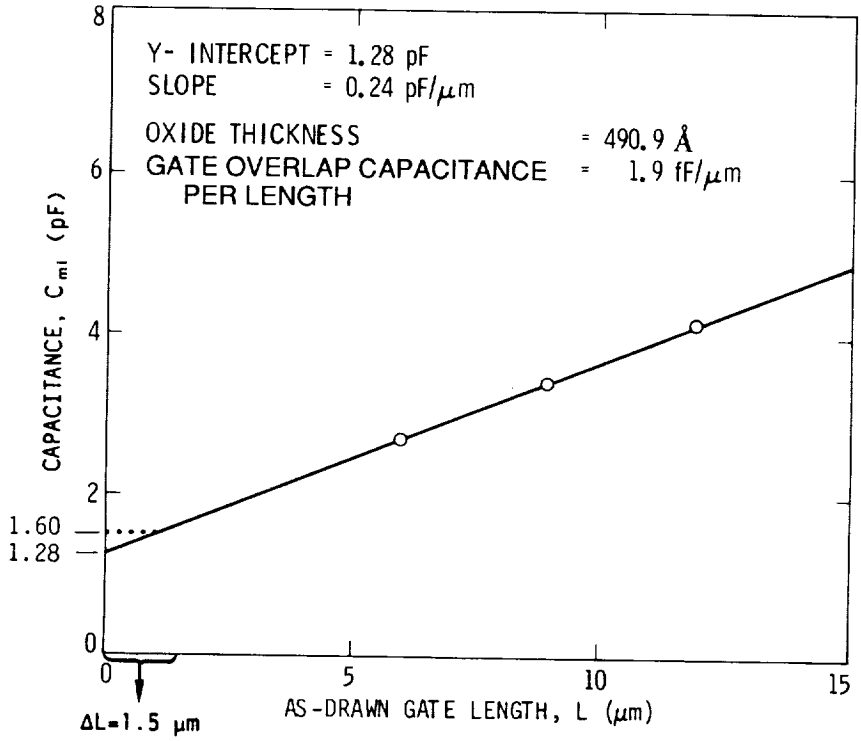


Figure 3.6: Gate Capacitance-Length plot for an annular n-MOSFET measured in inversion.

structure is biased into accumulation to eliminate C_b. The measured capacitance is:

$$C_m = C_{ox} + C_{go} + C_{off}$$

By using several MOSFETs biased into accumulation one can plot C_m vs. L. From the slope T_{ox} can be calculated and the intercept provides an estimate of $C_{go} + C_{off}$. In this method C_{go} and C_{off} can not be separated. Notice that due to the differences in measurement techniques, the C_{off} measured using this technique will differ from the value of C_{off} measured using the Inversion Method.

3.1.5 Equipment

Our measurements use an HP4192A Impedance Analyzer connected to the capacitor under test through a switch matrix. The structures were designed to

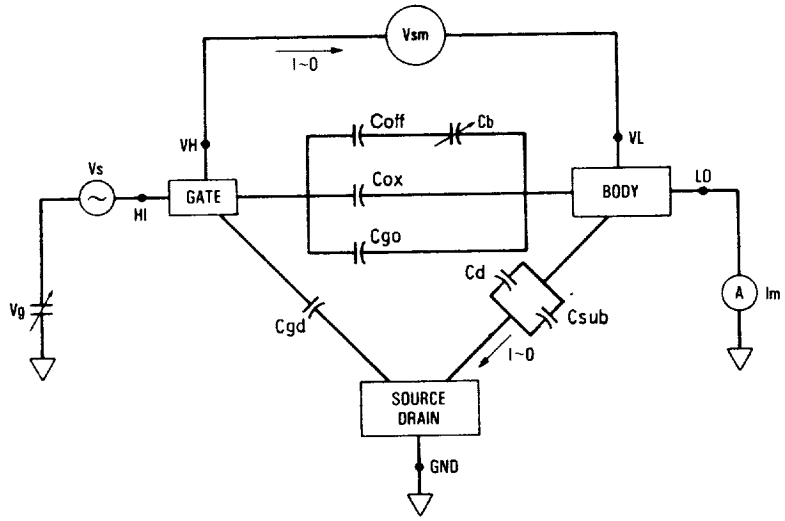


Figure 3.7: Connections to a MOSFET to perform the accumulation method of capacitance measurement.

be probed using a 2 $\times$ N pad array. Due to inherent difficulties in measuring capacitance at the wafer or chip level, several pitfalls must be recognized. First, one-meter long, matched impedance (50 Ω) cables must be used or the measurements must be made at a frequency of less than 1MHz. Otherwise, reflections in the cables which the meter automatically compensates for (assuming one meter cable) will cause a systematic error in the data. Second, measurements of similar capacitors must be made using a single group of probes and without making or breaking connections in the matrix. Different paths in the matrix and on the probe cards have different inherent impedances, leading to random errors in the data, which affect both the slope and intercept of the C vs. L function. It is advisable that measurements of different capacitors within a padframe be made by moving the probes from device to device, rather than changing connections in the matrix. Figure 3.9 shows data taken with and without moving the probes from location to location. This shows that the error introduced by not following this technique is quite large.

Finally, two calibrations of the impedance analyzer are available: short (all four inputs shorted) and open (high inputs shorted and low inputs shorted).

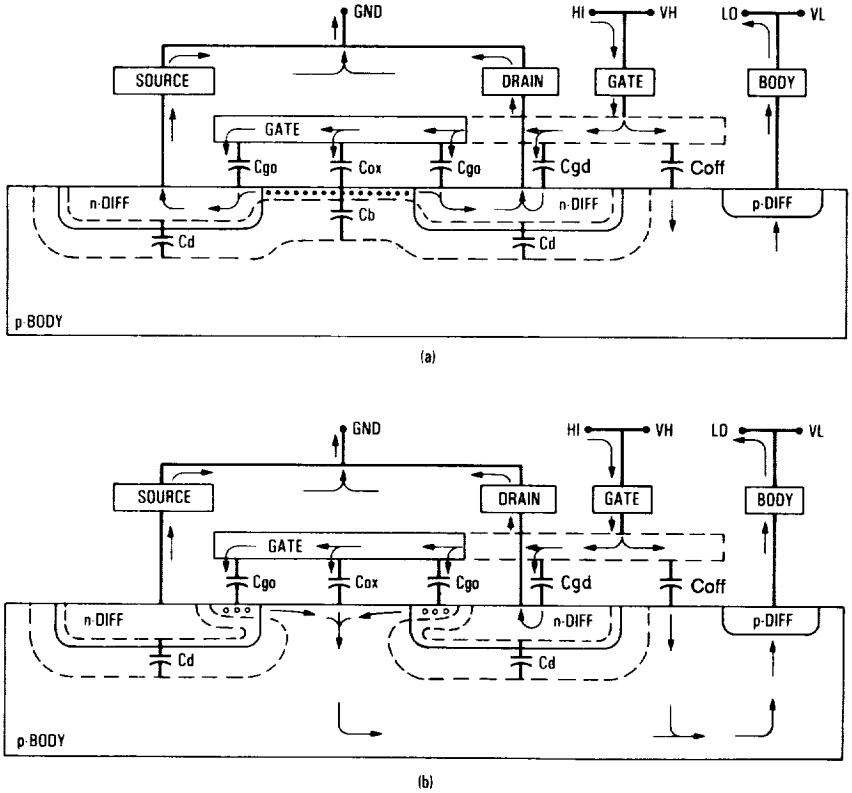


Figure 3.8: n-MOSFET behavior observed while using the accumulation method of measuring the oxide capacitance, C_{ox}. (a) shows the device in inversion (C_b = min. value) and (b) shows the device in accumulation (C_b = infinite). When the measurement is performed using a low frequency signal, the body capacitor, C_b, is measured in series with C_{ox}, however, when the measurement is performed using a high frequency signal, C_b is decoupled from the measurement when the capacitor is in inversion.

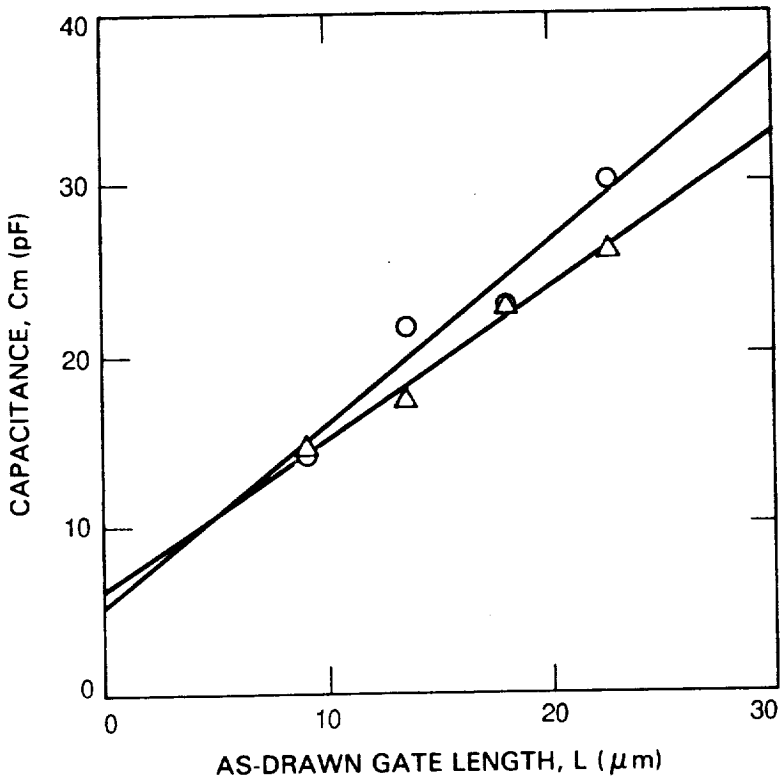


Figure 3.9: Error introduced in the accumulation capacitance measurement method by using different probe/matrix paths. In this figure the two curves were measured on the same capacitors using, in the case of the open circles, two paths through the matrix and, in the case of the triangles, a single path. Calculation of the oxide thickness gives values of 431 Å for the instance where two paths were used and 517 Å for the instance where a single path was used.

Table 3.1: Results from tests of Round MOSFETs.

Parameter	Inversion Method		Accumulation Method	
	n-Ch	p-Ch	n-Ch	p-Ch
Oxide thickness, T_{ox} (Å)	490.9	493.3	492.6	492.6
(From slope of C vs. L plot)	(Figure 3.6)			
Gate Overlap Capacitance, C_{go} (fF/μm)	1.9	5.6	0.6	3.2
(From Y-intercept of C vs. L plot)	(Figure 3.6)		(Figure 3.9)	
Gate Overlap Capacitance, C_{go} (fF/μm)	6.5	6.5	–	–
(From C-V Curve)	(Figure 3.5)			

Each is done at the measurement frequency used and adds a correction factor to the data. Thus the results are affected only in the value of the intercept (C_{go}) obtained, since calculating the slope eliminates systematic errors. The short calibration can be performed by setting the probes down on the wafer chuck. However, the open calibration can be accurately performed only if an appropriate structure (one similar to the structure being tested, but with the gate floating) is fabricated for this test.

3.1.6 Results and Conclusions

Table 3.1 lists results obtained with the test methods described earlier. As described earlier, the inversion method provides a means of checking the values obtained for the gate overlap capacitance, while no such self-check exists for the accumulation method. However, both methods provide essentially the same value for the gate oxide thickness. This value agrees very well with the manufacturer's specification of 500 $\pm$ 25 Å.

3.2 Timing Sampler Array

3.2.1 Introduction

Experience with high speed LSI circuits revealed a need for test structures to assess the circuit and device parameters critical for high-speed integrated circuit

(IC) performance. These parameters are necessary if the IC designer is to be able to design high speed circuits which perform to specification in first silicon.

One of the most important of these parameters is the on-chip propagation delay. A timing sampler test circuit has been developed to measure this key parameter. The timing sampler is a compact, low-power circuit that provides fast and repeatable measurement of circuit delays using all-digital logic. A CMOS/bulk test circuit, containing an array of timing samplers to measure delays along inverter chains, has been fabricated and tested. The resulting data has been successfully fitted to a first order circuit *tau* model. The *tau* model gives an estimation of gate delay as a function of transistor geometries, loading, and supply voltage.

Use of the timing sampler eliminates common problems that occur when measuring delays with a ring oscillator. Specifically, the timing sampler is not susceptible to oscillations in harmonic modes as is a ring oscillator. These oscillations can lead to incorrect calculation of gate delay [17,18]. In the timing sampler, delays are directly measured by means of externally generated timing events (transitions) as opposed to the internally generated timing events (oscillation) used by a ring oscillator. The timing sampler offers the additional advantages of occupying less chip area and consuming less power than a ring oscillator. Also, using the timing sampler, one can measure individual stage delay and develop the stage delay statistics (mean and standard deviation). Such analysis is not possible using the ring oscillator.

3.2.2 Direct Measurement of Circuit Delays

This section describes the traditional method for directly measuring circuit delays and discusses the problems that occur when applied to the measurement of on-chip delays. The timing sampler method is then discussed and shown to be a superior method for measuring on-chip delays.

Figure 3.10a illustrates the measurement of a delay, t_d, using the traditional method. The timer is an instrument that measures the delay between two signal transitions by means of an accurate internal clock. A transition on the START input starts the clock, and a transition on the STOP input stops the clock. Thus, the measured delay is the number of clock cycles counted between start and stop transitions multiplied by the clock period.

The timer measurement resolution is, by design, accurate to $+0$, -1 clock cycle period. The accuracy of this one-shot measurement depends on the accuracy and stability of the clock and START/STOP input comparator circuits. When the input is periodic, however, the timer can obtain higher resolution and

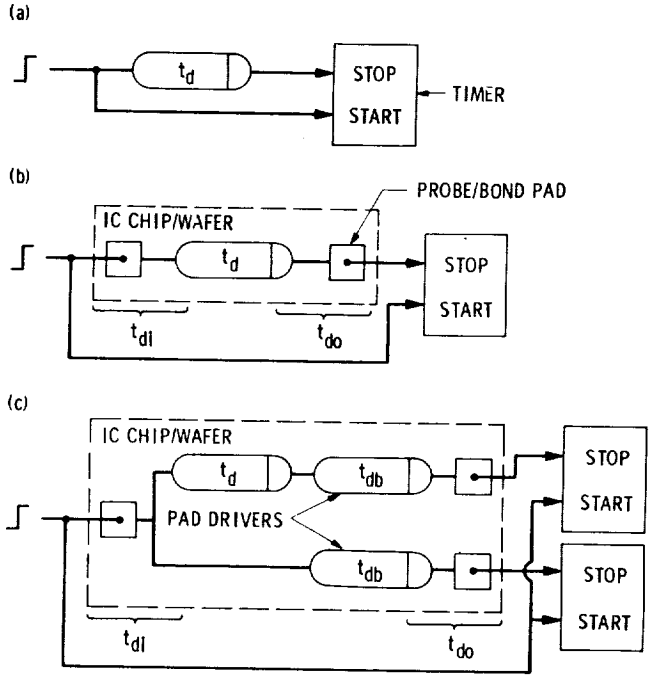


Figure 3.10: Traditional approach to delay measurement which utilizes a single step input signal.

accuracy through averaging.

The method shown in Figure 3.10a has limitations which are illustrated in Figure 3.10b. In this case, a considerable delay, t_{do}, is introduced in driving the output pad and the STOP input of the timer. This output delay could be up to six orders of magnitude larger than t_d. An additional delay t_{di} exists at the input of the t_d element. However, this delay is very small compared to t_d when the input pad is driven from a low impedance source and the wire connection from input pad to delay element is short. Thus, the timer will measure $t_{di} + t_d + t_{do}$, which, since $t_{do} \gg t_{di} + t_d$, is approximately t_{do}. To successfully implement this method, the STOP input of the timer must present a minimum load (on the order of a minimum size gate load) to the output of the delay element. To accomplish this, the timer must be integrated onto the IC chip. This is impractical, however, because of the timer complexity, size, and possible low yield for the fabrication process.

An obvious solution to this problem would be to use two parallel delay paths as shown in Figure 3.10c. Although each path contains a delay of $t_{db} + t_{do}$, only one path contains t_d, so the difference between the two measurements would yield t_d. The problem with this measurement, however, is that we are subtracting two large numbers ($t_{db} + t_{do} \gg t_d$) having a variability as large or larger than t_d. This variation in the fixed part of the delay (t_{db}) in each path is a result of local process variations on the chip. A further drawback, is that this circuit occupies a large area on the chip due to the pad drivers.

Our timing sampler method of measuring on-chip delays circumvents the problems associated with the methods just discussed. This method still uses a timer for delay measurement, but does not connect the STOP input to the t_d-delay output. Instead, the STOP input is generated by an off-chip source. The timing sampler method uses two input pads that are driven by off-chip start and stop signals. The delay between start and stop signal transitions is adjusted and accurately measured with a timer as shown in Figure 3.11. The START input drives the t_d-delay input and the t_d-delay output is connected to the timing sampler A-input. The timing sampler A-input presents a minimum load to the t_d-delay output. The timing sampler B-input is connected to the STOP input pad.

The timing sampler functions as an on-chip transition skew detector. It determines if the skew, or delay between transitions on inputs A and B, is positive or negative. Thus, it answers the question: "Did the transition on input A occur before or after the transition on input B?" Since the A signal is delayed by t_d and the B signal is not, the timing sampler output indicates if the on-chip delay t_d is greater than or less than the input delay t_{in} applied between

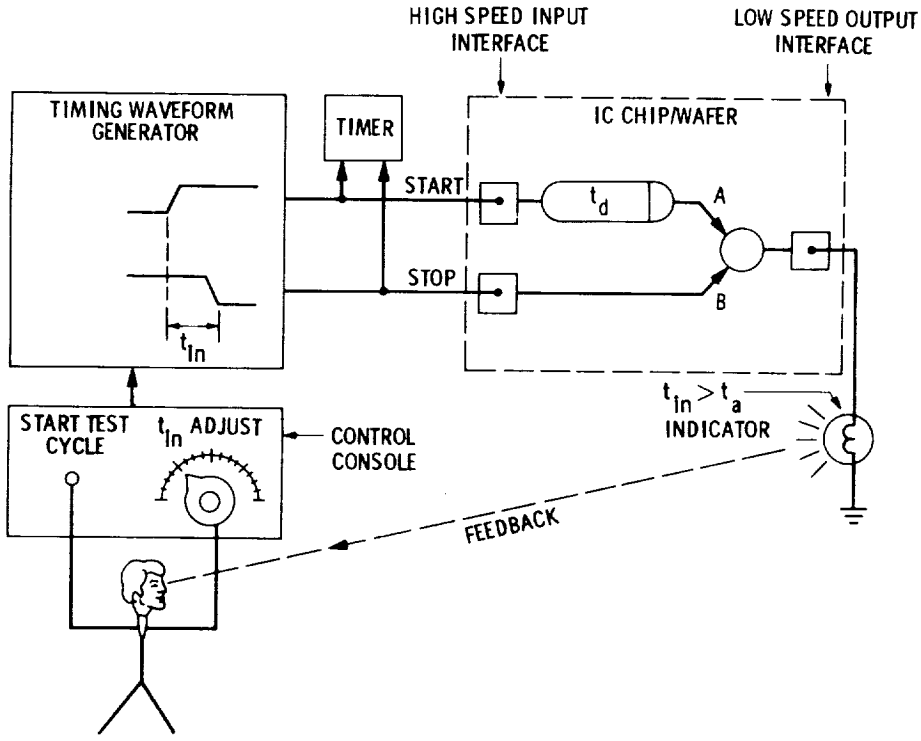


Figure 3.11: Timing sampler delay measurement which utilizes two-step input signals and an on-chip timing sampler.

the START and STOP pads.

The timing sampler output provides the information needed to adjust t_{in} so as to reduce the difference between t_{in} and t_d. Figure 3.11 illustrates an operator who presets the input delay and initiates a timing cycle. If $t_{in} < t_d$ on the previous cycle then the operator increases t_{in} and starts another cycle. When properly adjusted over many cycles, t_{in} converges (within the resolution of the timer) to t_d. At this point, the timer is read to obtain the measurement value of t_d. A binary search algorithm can be used in the adjustment of t_{in}. In this case, the feedback value (timing sampler output) and t_{in} values applied in previous cycles are used in determining the value of t_{in} for the present cycle. Generally, the operator and control console of Figure 3.11 are implemented with electronics and incorporated into the timing waveform generator.

An improved method that corrects for unknown input delay errors (due to zero calibration drift, unknown cable delays, etc.) is shown in Figure 3.12. A timing sampler element is connected to the input and output of the t_d-delay

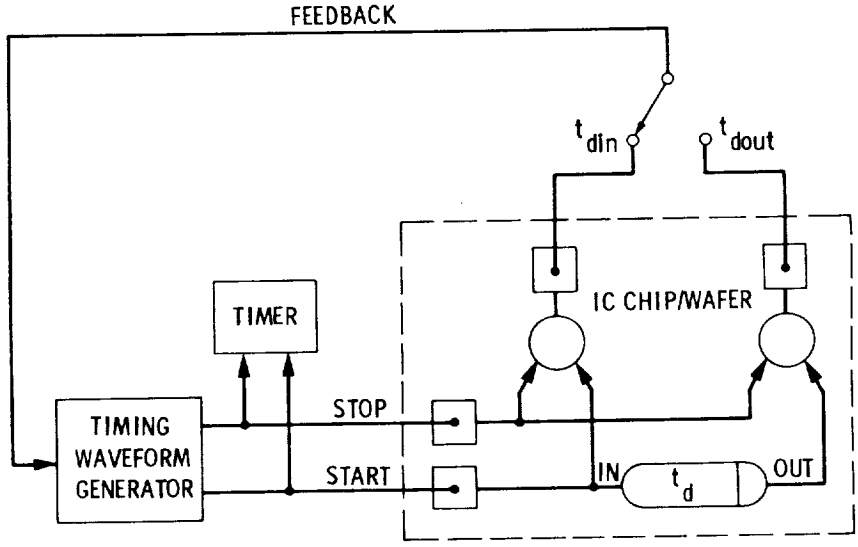


Figure 3.12: Differential delay measurement with timing sampler.

element. The input timing sampler is used to measure a baseline delay t_{din} that is subtracted from the delay obtained from the output timing sampler element t_{dout}. This differential technique yields an accurate measure of the delay $t_d = t_{dout} - t_{din}$. An application of this technique to the measurement of on-chip pad driver and pad receiver delays and the inter-chip delay is illustrated in Figure 3.13. The delay is measured when the feedback select switch is in each of

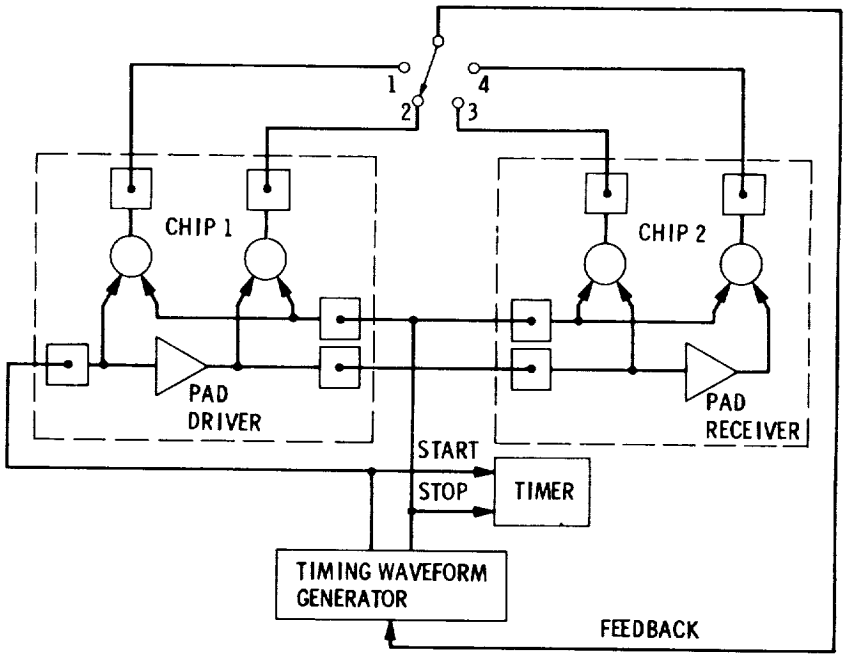


Figure 3.13: Measuring inter-chip delay.

the four positions. The difference between the position 1 and 2 measurements is the delay of the chip 1 output pad driver. The delay difference between positions 2 and 3 measurements is the inter-chip delay, and between positions 3 and 4 measurements it is the delay of the chip 2 input receiver.

3.2.3 Muller C-Element as a Timing Sampler

A timing sampler is a circuit whose output changes state if a transition on one input occurs before a transition on the second input. A 2-input Muller C-element is a circuit that behaves in this manner. The Muller C-element can be constructed from a 3-input majority gate (a circuit whose output is high when 2 or 3 of its inputs are high) by connecting one of the 3 inputs to the output as shown in Figure 3.14. This circuit is a bistable device that is the digital equivalent of a Schmitt trigger since its output displays hysteresis. The C-element behaves as a 2-input AND gate when its output is low and like a 2-input OR gate when its output is high. The digital behavior of a 2-input C-element is characterized by the transition diagram of Figure 3.14.

The C-element timing sampler can be used in the measurement of positive or negative transition delays. Timing diagrams for the measurement of positive transition delays using a C-element timing sampler are shown in Figure 3.15. The measurement timing cycle consists of a setup phase and a measure phase. The setup phase places the C-element into an initialized state. In this state, the C-element will trip, thereby causing the output to change state when a transition on input A occurs prior to a transition on input B. The setup phase consists of resetting the C-element output and then arming the A input. For positive transition delay measurement, this is equivalent to traversing through node 00 and then to node 10 on the transition diagram of Figure 3.14. For negative transition delay measurement, the setup phase corresponds to traversing through node 11 to node 01. The measure phase includes the input delay period (t_{in}) and the out period where the C-element output is sampled to see if it changed state (indicating $t_{in} > t_d$).

A practical CMOS implementation for the C-element is illustrated in Figure 3.16. This circuit is not constructed from a 3-input majority gate, therefore the output is not static. The memory action of the C-element function is provided by the capacitance C. This capacitance primarily consists of the input capacitance of an inverter connected to the output node. The output is driven towards ground when n-channel MOSFETs n_1 and n_2 are on (A and B both high), and towards VDD when p-channel MOSFETs p_1 and p_2 are on (A and B both low). When leakage paths are neglected, the output voltage remains

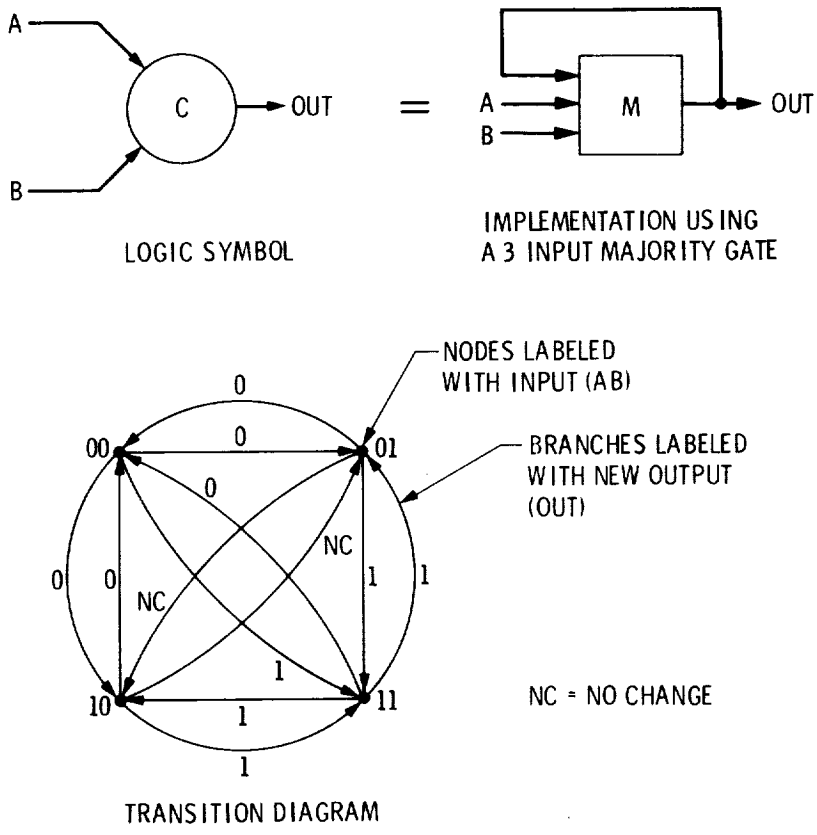


Figure 3.14: Two-input Muller C-Element as a timing sampler.

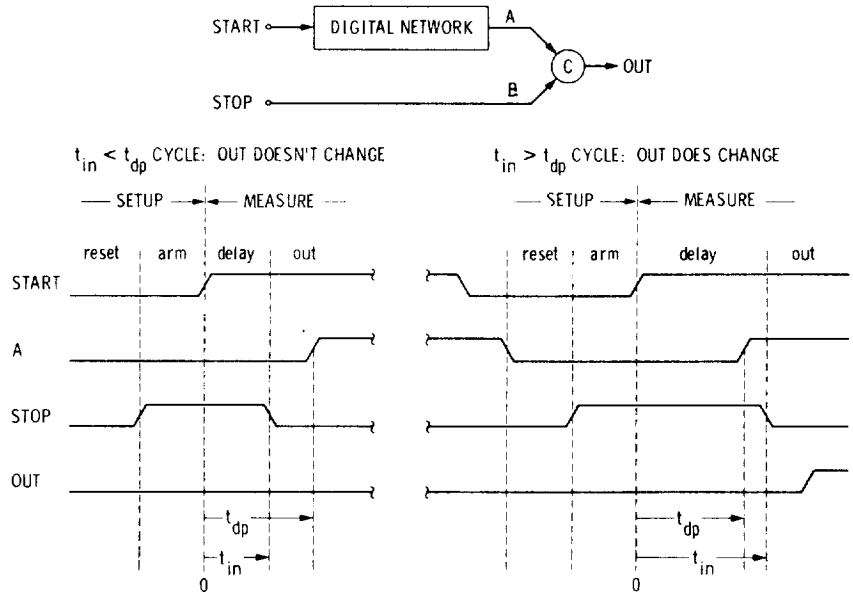


Figure 3.15: Positive transition delay measurement using a C-Element.

fixed as long as the logic levels on the two inputs (A and B) are different. The response of this circuit to step input signals is, to a first order approximation, determined by the saturation current of the MOSFET in the charge/discharge path having the smallest width-to-length ratio (W/L) and by the capacitance C. The slew rate k_c of the output to step inputs is given by $k_c = ID_{sat}/C$, where $ID_{sat} = (1/2)KP(W/L)(VDD - VT)^2$ is the saturation current of the MOSFET having the smaller W/L ratio, $KP = \mu C^*_{ox} = \mu C_{ox}/(WL)$ is the intrinsic channel conduction factor, and VT is the threshold voltage. To improve the C-element response (increase the output slew rate), the capacitance C is made as small as possible.

Because of the finite slew rate, the C-element output will not switch from one rail (VDD or ground) to the other unless the delay from the rise/fall of input A to the fall/rise of input B is greater or equal to VDD/k_c. When the delay is less than VDD/k_c then the output voltage may be a nondigital level (neither a valid logic-0 or logic-1). If the C-element timing sampler output is used as an input to on-chip logic such as a decoder (as on the CRRES chip timing sampler array) then the decoder may produce invalid outputs and draw excessive current. This can only be avoided by insuring that the output of the C-element is

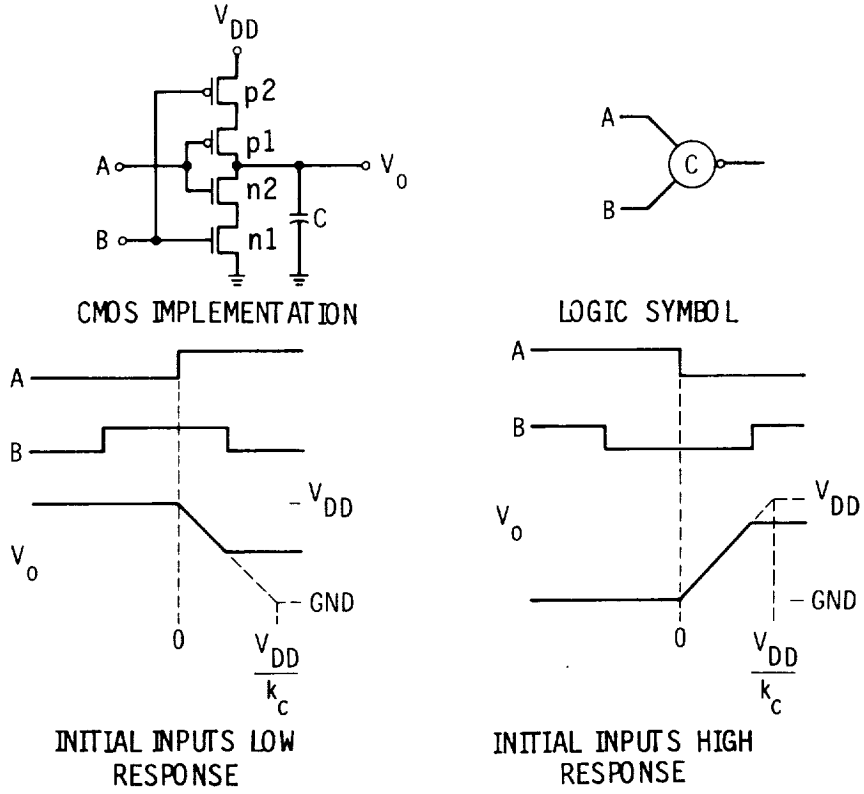


Figure 3.16: CMOS dynamic C-Element latch where k_c is the slew rate (with units of V/s).

always a valid logic level. A staticizer circuit can be used to restore a nondigital value to a valid logic level (VDD or ground). The staticizer circuit is shown in Figure 3.17 along with typical static and dynamic characteristic curves. The

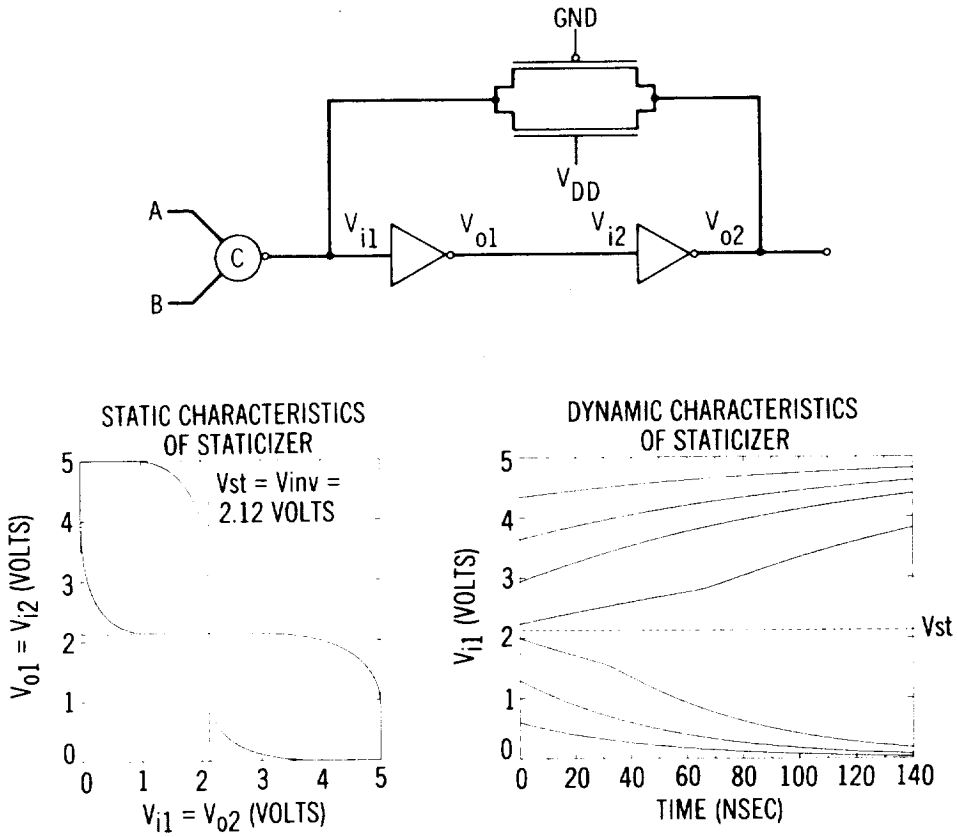


Figure 3.17: Restoring the logic level of the C-Element with a staticizer.

staticizer consists of an inverter pair with week feedback (long channel transmission gate). When the C-element initializes V_{i1} to a voltage above/below the switching threshold V_{st}, the staticizer will drive this node through the feedback element to VDD/ground. The staticizer output can still remain nondigital for a long period of time (indefinitely if V_{i1} is initialized exactly to V_{st}), so a cross coupled transistor mutual exclusion circuit can be connected to the V_{o1} and V_{o2} staticizer output nodes. The mutual exclusion circuit output does not begin to change state until the staticizer is off balanced from its switching threshold (metastable) point by at least one transistor threshold ($|V_{o1} - V_{o2}| \geq V_{th}$ which is approximately 1 volt).

This additional staticizer circuitry is unnecessary if an analog buffer, such as a source follower, is used to drive the C-element output voltage off chip. When this analog approach is used, the timing sampler measurement loop will not dither as it can with digital feedback.

A parallel array of C-element timing samplers has been designed, fabricated, and tested (Figure 3.18). Although a series connected array is preferred because

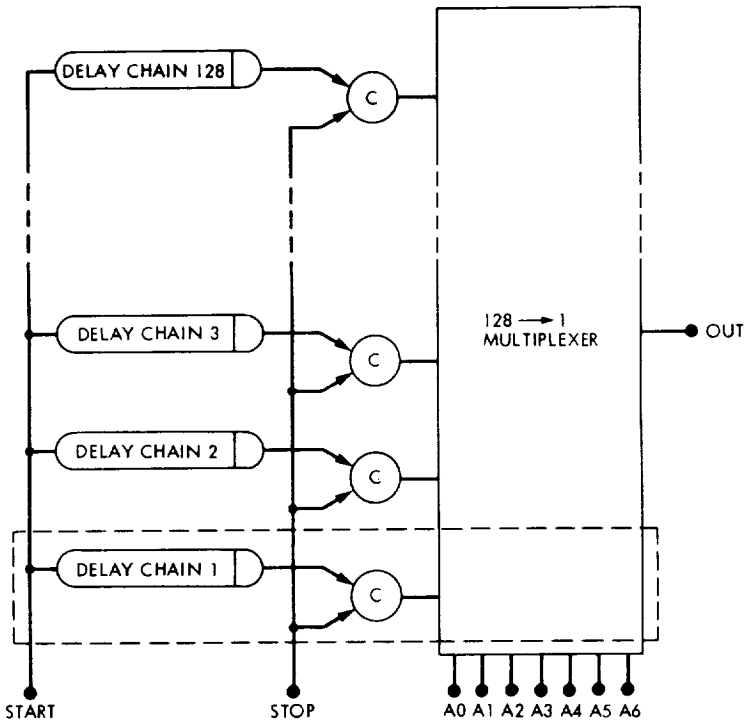


Figure 3.18: Block diagram of the Timing Sampler Array.

of the improved accuracy obtained through differential measurements, a parallel connection was used because of the limited delay range available from the waveform generator available. To improve the accuracy of the measurements, each delay chain contains 20 inverter pairs and some zero delay elements (metal wires) have been included to provide a baseline measurement.

The circuit schematic of a single stage of the timing sampler array is shown in Figure 3.19. This circuitry corresponds to the area enclosed by the dashed line in Figure 3.19.

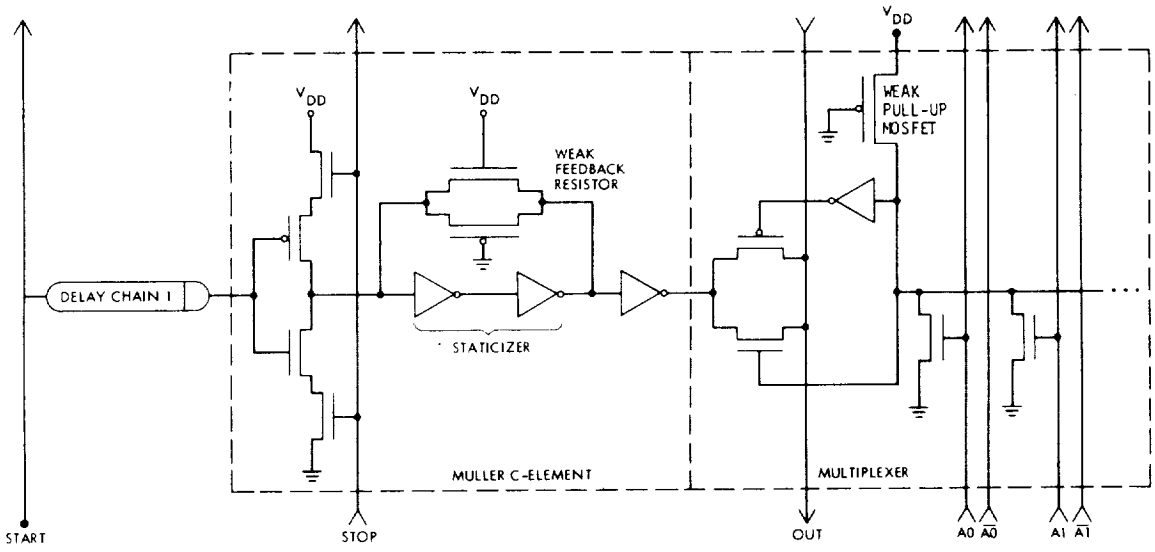


Figure 3.19: One stage of the Timing Sampler Array.

3.2.4 Data Analysis

As-measured inverter pair data obtained from the timing sampler array, shown in Figure 3.18, is displayed in Figure 3.20. This data comes from twenty inverter delay chains which have transistors whose widths, W, and lengths, L, are different. The twenty transistor sizes used in the inverter delay chains correspond to the points in the W vs. L plane whose as-drawn widths are 3, 4.5, 6, and 9 μm and whose as-drawn lengths are 3, 6, 9, and 12 μm. In each inverter, the p-channel transistor is the same size as the n-channel transistor; thus the ratio of the p-pullup MOSFET to the n-pulldown MOSFET is $r = 1.0$. Also, the second inverter of each inverter pair drives two equivalent inverters (fanout $f = 2.0$). The X marked data points in Figure 3.20 correspond to rising (0 to 5V) output transition delays, whereas the O marked data points correspond to falling (5 to 0V) output transition delays. Straight line segments have been drawn between points of the same length.

A circuit *tau* model has been applied to the raw data. Figure 3.21 illustrates the *tau* model applied to an inverter driving a fixed load capacitance C_L. This model states that the propagation delay of an inverter is proportional to the ratio of the load capacitance C_L to the gate capacitance of the charging/discharging transistor (p-channel gate capacitance C_p for output rising edges/n-channel gate

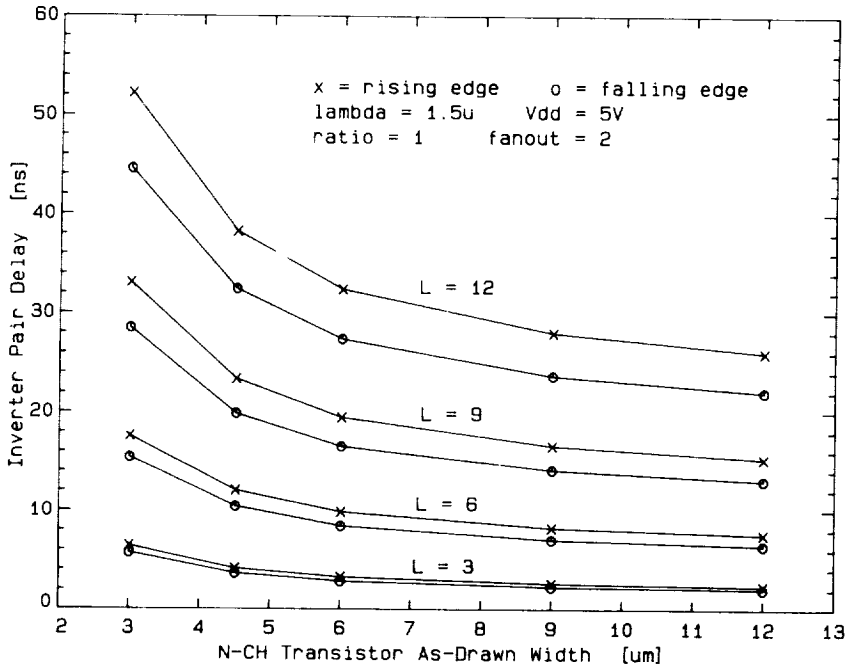


Figure 3.20: Timing sampler as-measured inverter pair data for rising and falling output transitions.

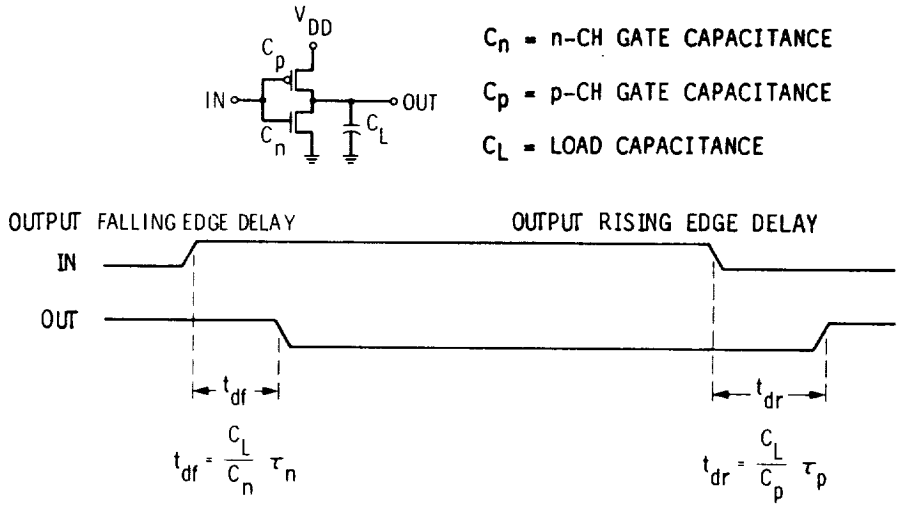


Figure 3.21: CMOS circuit delay calculations using a *tau* model.

capacitance C_n for output falling edges). The proportionality constant is τ_n of the n-MOSFET for output falling edges, and τ_p of the p-MOSFET for output rising edges[2]. This results in an output falling edge delay $t_{df} = (C_L/C_n)\tau_n$ and an output rising edge delay $t_{dr} = (C_L/C_p)\tau_p$. A simple analysis of this inverter circuit[2] shows that τ is proportional to the square of the transistor gate length, or $\tau_n = H_n L_n^2$ and $\tau_p = H_p L_p^2$ where the proportionality constants are $H_n = 2VDD/[\mu_n(VDD - V_{Tn})^2]$ for the n-channel MOSFETs and $H_p = 2VDD/[\mu_p(VDD - V_{Tp})^2]$ for the p-channel MOSFETs. H_n and H_p are expressed in terms of the n- and p-channel mobilities (μ_n, μ_p),and the n- and p-channel threshold voltages (V_{Tn}, V_{Tp}), and the power supply voltage VDD. This behavior is illustrated by the data shown in Figure 3.20.

An interesting feature shown in Figure 3.20 is that, for a given length L, the inverter pair delay increases as width W decreases. The reason for this effect is that the load capacitance to gate capacitance ratio C_L/C_p or C_L/C_n depends on W. The load capacitance C_L consists of the gate capacitance of the MOSFET making up the inverters being driven as well as the interstage wiring capacitance C_w. The MOSFET gate capacitances are proportional to gate areas $L \times W$: $C_n = \epsilon_{ox} L_n W_n / T_{ox}$ for the n-channel MOSFET and $C_p = \epsilon_{ox} L_p W_p / T_{ox}$ for the p-channel MOSFET, where ϵ_{ox} is the oxide permittivity and T_{ox} is the oxide thickness. Referring to the inverter pair in Figure 3.22, the load capacitance

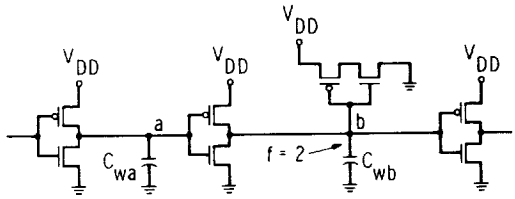


Figure 3.22: Timing sampler array inverter chain element.

at node "a" is $C_{La} = C_n + C_p + C_{wa}$ and the load capacitance at node "b" is $C_{Lb} = f(C_n + C_p) + C_{wb}$, where the fanout at node "b" is $f = 2$ (note: the fanout at node "a" is $f = 1$). When considering output rising edge delays of inverters consisting of transistors of constant length, the capacitance ratio C_L/C_p consists of a component that is independent of the width $f(C_n + C_p)/C_p$ and one that is dependent on the width C_w/C_p. It is this C_w/C_p component that accounts for the increase in the delay as the width decreases in Figure 3.20. Since C_p is directly proportional to W, the inverter delay is proportional to $1/W$. The

above argument applies to falling edge delays by replacing the denominator C_p with C_n.

Another interesting feature of the data in Figure 3.20 is that for a given length and width the rising edge delay is larger than the falling edge delay. This can be attributed to the fact that the first inverter of each pair, which drives node "a" in Figure 3.22, sees only one inverter input as a load (fanout = 1), whereas the second inverter sees two inverter inputs as a load (fanout = 2), and to the fact that p-channel transistors are slower than n-channel transistors ($H_p > H_n$ due to the differences in mobilities).

When the *tau* model is applied to the loaded inverter pair of Figure 3.22, the following rising and falling edge delays are obtained:

$$t_{df} = H_p L^2[1 + \frac{1}{r} + \frac{A_{wa}}{rWL}] + H_n L^2[f(1+r) + \frac{A_{wb}}{WL}]$$

$$t_{dr} = H_n L^2[1 + r + \frac{A_{wa}}{WL}] + H_p L^2[f(1 + \frac{1}{r}) + \frac{A_{wb}}{rWL}]$$

where

$$A_{wa} = \frac{C_{wa}}{C^*_{ox}} = A_{pa}C'_p + A_{ma}C'_m + A_{da}C'_d$$

$$A_{wb} = \frac{C_{wb}}{C^*_{ox}} = A_{pb}C'_p + A_{mb}C'_m + A_{db}C'_d$$

$$C'_p = \frac{C^*_p}{C^*_{ox}}, \quad C'_m = \frac{C^*_m}{C^*_{ox}}, \quad C'_d = \frac{C^*_d}{C^*_{ox}}$$

$$L = L_n = L_p = L_o - \Delta L, \quad W = W_n = W_o - \Delta W$$

and

$$W_p = rW_n, \quad \frac{C_p}{C_n} = \frac{C^*_{ox}LW_p}{C^*_{ox}LW_n} = r, \quad r \equiv \frac{W_p/L_p}{W_n/L_n}$$

The interstage wire capacitance is divided into three components: the polysilicon capacitance ($A_pC^*_p$), the metal capacitance ($A_mC^*_m$), and the diffusion capacitance ($A_dC^*_d$), where C^*_p, C^*_m, and C^*_d have units of capacitance per unit area and A_p, A_m, and A_d are areas. Corrections are made to the as-drawn lengths/widths (L_o/W_o) using $\Delta L/\Delta W$ to obtain the true electrical lengths/widths (L/W). The primed capacitance values, C'_p, C'_m, and C'_d in the above equations have been normalized by the oxide capacitance per unit area $C^*_{ox} = \epsilon_{ox}/T_{ox}$ and are dimensionless. Both of the equations for the inverter pair delays t_{df} and t_{dr} can be written as linear equations in $1/W$, where ($W = W_o - \Delta W$). A fitting procedure has been used to fit the as-measured data for rising and falling output edge

inverter pair delays (t_{dp} and t_{dn} as plotted in Figure 3.20) and the parameters L_o, W_o, r, f, A_{pa}, A_{ma}, A_{da}, A_{pb}, A_{mb}, and A_{db} to the model equations to obtain values for H_n, H_p, ΔL, ΔW, C'_p, C'_m, and C'_d. The finite difference Levenberg-Marquardt algorithm was used in doing this fit. Figure 3.23 shows the results

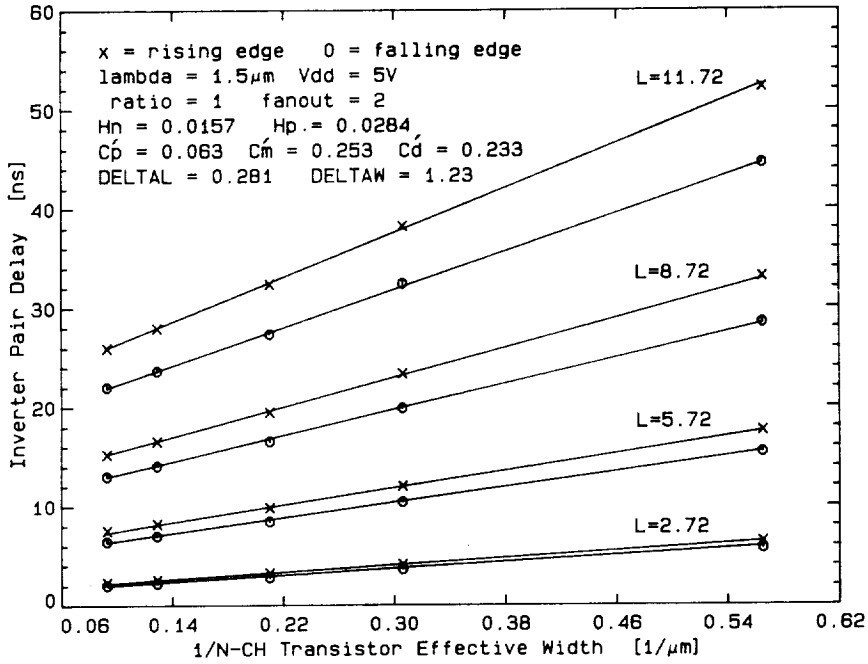


Figure 3.23: Timing sampler fitted data where H is in units of ns/μm^2, W and L are in units of μm, and C' is dimensionless.

of fitting the raw data to these equations. In this figure, the inverter pair data is plotted against $1/W$. The lines drawn through the data points are derived from the model equations using the extracted parameters shown on the top of the plot.

The *tau* model fits the data very well considering its simplicity. The extracted parameter C'_m, however, has an unrealistically high value. For the particular layout of the timing sampler, C'_m should be less than C'_d and C'_p. The values extracted for the three parameters C'_p, C'_d, and C'_m are not accurate in a physical sense because the changes in inverter pair delay due to the differences in metal, polysilicon, and diffusion capacitance from one inverter chain to the next are very small. This presents a problem in the separation of these parameters.

Another cause of this problem is that the periphery component of the diffusion capacitance was not accounted for in the model.

3.2.5 Conclusions

The timing sampler is a compact test structure that allows fast, direct, and repeatable measurements of on-chip circuit delays. It overcomes the limitations of the ring oscillator approach to delay measurement at the expense of some special external hardware. The timing sampler delay measurement is also amenable to wafer level measurements because there are no high speed outputs. Only two high speed inputs need to be applied to the wafer and this is easy to accomplish using coaxial cables and proper terminations on the probe card. Another positive aspect of the timing sampler is the ease with which it can be multiplexed. The delay data obtained from a single compact timing sampler array can be used to characterize gate delays over a range of device geometries employed in typical circuit designs using the circuit *tau* delay model.

3.3 Proximity Structures

3.3.1 Introduction

The design rules, which are related to the spacing between different layers, are not adequately tested by the common parametric test structures such as the split-cross-bridge resistor, contact resistors, transistors, etc. To overcome this deficiency, a set of very simple structures was developed and tested for the CRRES fabrication run. These structures, which use only two pads and are based on diode breakdown voltage, are termed collision test structures.

3.3.2 Structure Geometry

Figure 3.24 shows the geometry of the collision structures, with a cross section shown of each. The distance d was varied from structure to structure. In every case, d represents the "as drawn" dimension. It should be noted that because of differences between fabrication processes, the actual physical dimension d could vary between devices manufactured by different fabrication houses. The 'Active region' shown in the cross sections refers to a thin-oxide region, such as the source-drain junctions of a MOS transistor.

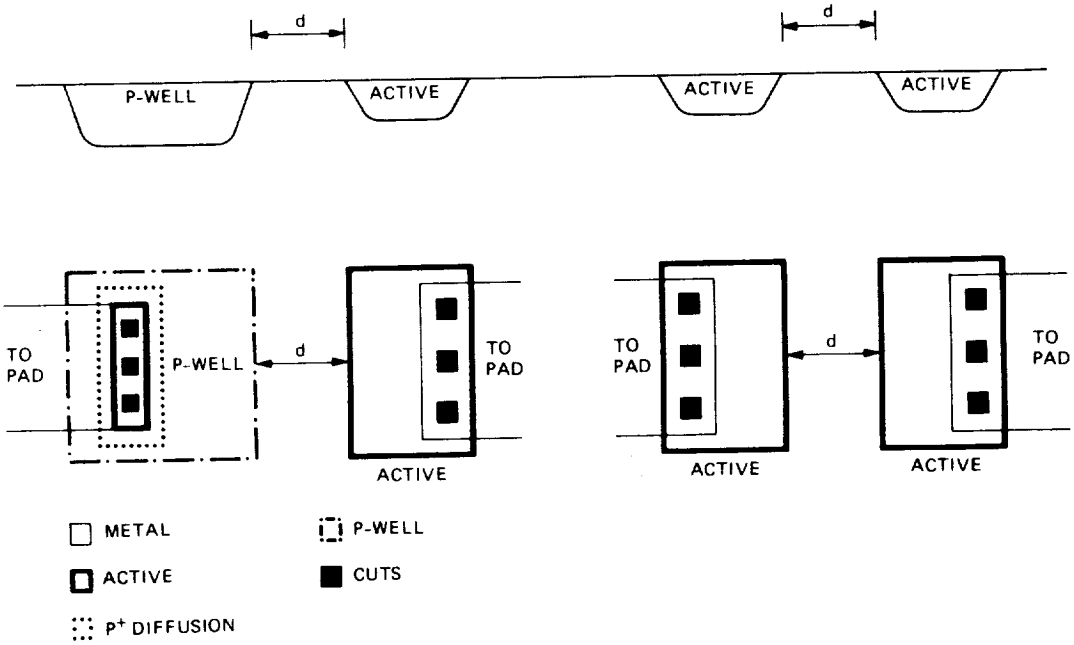


Figure 3.24: Collision Test Structures for measuring p-well-to-diffusion (active) and diffusion-to-diffusion breakdown voltage.

Table 3.2: Diode breakdown voltages of various Collision Test Structures.

– Spacing –		– Diode Breakdown Voltage (Volts) –			
lambda	μm	p-Well to p+AA	p-Well to n+AA	p+AA to n+AA	p+AA to p+AA
5	7.5	48-50	48-50	33-34	33-34
4	6.0	8-15	49	33-34	34
2	3.0	0	35	32-34	33
1	1.5	0	31-49	0	0
-1	-1.5	0	27-0	0	0

Notes: p+AA — p+ doped active area
n+AA — n+ doped active area

3.3.3 Experimental Results

A set of these structures was fabricated and the breakdown voltage of the resulting diodes measured by applying a reverse bias to the junctions (Table 3.2).

3.3.4 Conclusions

These structures offer a very simple method of verifying that a wafer manufacturer can comply with the agreed upon set of geometrical design rules for active area and well spacings. It also provides a means of determining a set of design rules that can be met by wafer vendors. Based on the above test results, one could establish a set of rules for this particular manufacturer; see Table 3.3.

Table 3.3: Design rules for manufacturer as indicated by Collision Test Structures.

Design Rule Name	Design Rule Value
p-Well to p+Active Area	8.0μm
p-Well to n+Active Area	7.0μm
p+Active Area to n+Active Area	3.0μm
p+Active Area to p+Active Area	3.0μm

3.4 The Split-Cross-Bridge Resistor

1572 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. ED-33, NO. 10, OCTOBER 1986

The Split-Cross-Bridge Resistor for Measuring the Sheet Resistance, Linewidth, and Line Spacing of Conducting Layers

MARTIN G. BUEHLER, MEMBER, IEEE, AND CHARLES W. HERSHEY

Abstract—A new test structure was developed for evaluating the line spacing between conductors on the same layer by using an electrical measurement technique. This compact structure can also be used to measure the sheet resistance, linewidth, and line pitch of the conducting layer. Using an integrated-circuit fabrication process, this structure was fabricated in diffused polycrystalline silicon and metal layers. These structures were measured optically and electrically, and these measured value were compared. For the techniques used, the optical measurements were typically one-quarter micrometer greater than the electrical measurements for the polysilicon and metal layers. Most electrically measured line pitch values were within 2 percent of the designed value. A small difference between the measured and designed line pitch is used to validate sheet resistance, linewidth, and line spacing values. Test results confirm the structure's self-checking feature based on the line pitch. That is, a small difference between the measured and designed line pitch is used to validate sheet resistance, linewidth, and line spacing values. Rules for designing the test structure are presented in detail.

I. Introduction

THIS PAPER describes an approach to measuring the sheet resistance, linewidth, and line spacing of electrically conducting lines. The approach is an extension of cross-bridge resistor [1] measurements and is based on an electrical measurement technique in which the parameters are determined from a specially designed cross-bridge resistor, termed the split-cross-bridge resistor. Alternative techniques for measuring linewidth and spacing are based on visual measurement techniques [2]. The test structure described here can be used to evaluate integrated-circuit layout rules quickly and accurately. The technique was demonstrated by fabricating 14 test structures in metal, polycrystalline silicon, and diffused silicon layers. The form of these test structures is shown in Fig. 1 and their critical dimensions are listed in Table I.

To illustrate the measurement principle, consider the polysilicon split-cross-bridge resistor shown in Fig. 1, which was designed to evaluate the line spacing between two polysilicon lines. The split-cross-bridge resistor is a combination of three structures. The upper structure is a cross resistor, the middle structure is a bridge resistor, and the lower structure is a split-bridge resistor. The bridge resistor has a single conducting channel of width, $W_b = 2W + S$. The split-bridge resistor has two conducting channels, each with a width of W so that the effective width is $W_s = 2W$. The line spacing S is deter-

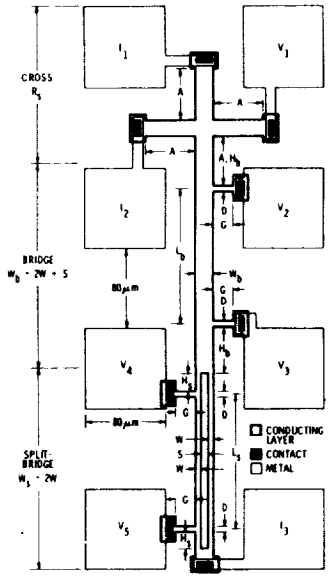


Fig. 1. Split cross bridge resistor designed to evaluate the linewidth W, line-spacing S, and sheet resistance R_s of a conducting layer.

TABLE I
SPLIT-CROSS-BRIDGE RESISTOR CRITICAL DIMENSIONS AND VOLTAGE TAP GEOMETRICAL ERRORS (E_2)

Layer	W (μm)	S (μm)	W_b/L_b	D/W_b	E_{2b}	W/L_s	D/W	E_{2s}
Poly	6.0	3.0	0.094	0.200	0.0006	0.043	0.500	0.0017
	3.0	3.0	0.056	0.333	0.0010	0.021	1.000	0.0033
Diffusion	9.0	4.5	0.141	0.133	0.0004	0.064	0.500	0.0011
	4.5	4.5	0.084	0.222	0.0007	0.032	1.000	0.0022
Metal	9.0	4.5	0.141	0.200	0.0009	0.064	0.333	0.0025
	4.5	4.5	0.084	0.333	0.0015	0.032	0.167	0.0049

L_b = 160 μm
L_s = 140 μm

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mined by subtracting the width of the split-bridge resistor ($W_s = 2W$) from the width of the bridge resistor ($W_b = 2W + S$).

II. Measurement Technique

The technique requires three electrical measurements, which are illustrated by the following idealized relationships. These relationships are uncorrected for geometrical errors, which, as discussed in a later section, can be ignored if the structure is designed properly. In the analysis, the sheet resistance R_s of the layer is needed, and this is calculated from the cross resistor using the simplified van der Pauw [3], [4] equation

$$R_s = (V_c/I_c)(\pi/\ln 2) \tag{1}$$

where the potential difference V_c is $V_1 - V_2$ for a current I_c passed into I_1 and out of I_2.

The width of the bridge resistor is determined from the idealized rectangular resistor expression

$$W_b = 2W + S = R_s L_b I_b / V_b \tag{2}$$

where the potential difference V_b is $V_2 - V_3$ for a current I_b passed into I_1 and out of I_3. The distance between the voltage taps is L_b, which is the distance specified on the photomask. The sheet resistance R_s is determined from the cross resistor and (1). The width of the split-bridge resistor is determined from

$$W_s = 2W = R_s L_s I_s / V_s \tag{3}$$

where the potential difference V_s is $V_4 - V_5$ for a current I_s passed into I_1 and out of I_3. The distance between the voltage taps is L_s. Note that the above equations require that no significant magnification occur so that L_b and L_s can be taken as their design values.

The general expression for line spacing is

$$S = W_b - W_s = R_s(L_b I_b V_s - L_s I_s V_b)/(V_b V_s) \tag{4}$$

where the sheet resistance R_s is determined from the cross resistor and (1).

For $I_b = I_s = I$ and $L_b = L_s = L$, then

$$S = R_s LI(V_s - V_b)/(V_b V_s) \tag{5}$$

The linewidth is calculated by modifying (3) and assuming $I_s = I$ and $L_s = L$

$$W = R_s LI/(2V_s). \tag{6}$$

Finally the line pitch P_t between features is determined from

$$P_t = W + S = W_b - (W_s/2)$$
$$= R_s LI(2V_s - V_b)/(2V_b V_s). \tag{7}$$

Thus, the split-cross-bridge resistor can be used to evaluate four critical parameters of a conducting layer, i.e., sheet resistance, linewidth, line spacing, and line pitch.

III. Measurement Interpretation

A physical model was developed that compares the linewidths and spacings of photomasks or wafers features measured by either visual or electrical techniques. The size of a feature may expand or contract linearly due to a number of factors, such as the bloating and shrinking of features during photomask making or lateral etching, lateral diffusion, and the coating of features of deposited layers during wafer fabrication. The model requires the use of the following eight parameters:

- W_p, S_p is the linewidth and spacing of a feature observed visually on a photomask.
- W_v, S_v is the linewidth and spacing of a feature observed visually on a fabricated wafer.
- W_e, S_e is the linewidth and spacing of a layer measured electrically on a fabricated wafer.
- V is the difference in the location of a feature edge as determined from visual measurements made on photomasks and fabricated wafers.
- X is the difference in the location of a feature edge as determined from visual and electrical measurements on fabricated wafers.

The relation among these parameters is shown in Figs. 2 and 3. Fig. 2 illustrates the fabrication of a polycrystalline silicon (poly) layer where the width of the poly layer observed on the wafer (W_e or W_v) is smaller than the width (W_p) on the photomask. The visual width W_v is shown arbitrarily at the base of the oxide, which surrounds the poly layer. The electrical width W_e is shown at the midpoint in the length of the trapezoid describing the poly layer.

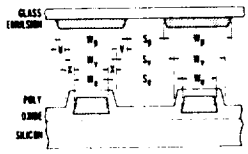

Fig. 2. Cross-sectional diagrams of a polycrystalline (poly) silicon layer and a photomask where critical dimensions are indicated.

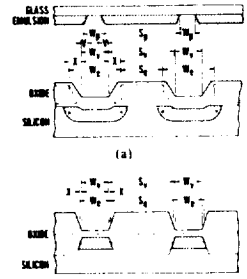

Fig. 3. Cross-sectional diagrams of two diffused layers formed (a) by a uniform oxidation, diffusion, oxidation process and (b) by a local-oxidation, diffusion, oxidation process where critical dimensions are indicated. Intermediate surfaces are shown by dashed lines.

TABLE II
COMPARISON OF LINEWIDTHS AND SPACINGS

Measured/Derived	Electrical	Visual	Photomask
Metal/Poly			
W_b	$2W_e + S_e$	$2W_v + S_v - 2X$	$2W_p + S_p - 2V - 2X$
W_s	$2W_e$	$2(W_v - 2X)$	$2(W_p - 2V - 2X)$
$W_b - W_s$	S_e	$S_v + 2X$	$S_p + 2V + 2X$
$W_s/2$	W_e	$W_v - 2X$	$W_p - 2V - 2X$
$W_b - (W_s/2)$	$W_e + S_e$	$W_v + S_v$	$W_p + S_p$
Diffusion			
W_b	$2W_e + S_e$	$2W_v + S_v + 2X$	$2W_p + S_p + 2V + 2X$
W_s	$2W_e$	$2(W_v + 2X)$	$2(W_p + 2V + 2X)$
$W_b - W_s$	S_e	$S_v - 2X$	$S_p + 2V - 2X$
$W_s/2$	W_e	$W_v + 2X$	$W_p + 2V + 2X$
$W_b - W_s/2$	$W_e + S_e$	$W_v + S_v$	$W_p + S_p$

Fig. 3 illustrates the formation of a diffused layer by either 1) a uniform oxidation, diffusion, oxidation process or by 2) a local-oxidation, diffusion, oxidation process. As illustrated in Fig. 3, the electrical width W_e includes not only the planar portion of the diffusion but a fraction of the lateral diffusion region as well.

The mathematical relationships among the eight parameters are illustrated in Table II. Note that the difference between the upper equations for metal and poly structures and the lower equations for diffused structures is the sign reversal of the V and X terms. The measured quantities W_b and W_s are shown, along with three derived quantities: $W_b - W_s$ (line spacing), $W_s/2$ (linewidth), and $W_b - W_s/2$ (line pitch). As can be seen in the table, W_e is larger or smaller than W_v or W_p depending on the nature of the layer being formed. For example, for a diffused layer, W_e is larger than W_p by $2V + 2X$. Similar comments apply to the line spacing. Such discrepancies are significant in manufacturing processes.

The line pitch, $W_b - (W_s/2)$, listed in Table II deserves special discussion. From the table it can be seen that $W_e + S_e = W_v + S_v = W_p + S_p$. This means that the line pitch measured electrically is a direct measure of the features formed on the photomask. That is, $W_e + S_e$ are not affected by V and X because they are distances between features that have the same kind of edge. For example, $W_e + S_e$ is the distance between the left edges of two parallel lines, and this distance is not affected by linear changes in photomask features (bloating and shrinking) or by wafer fabrication processes because both edges are affected in an identical fashion provided features are not magnified. If magnification can be ruled out, then $W_e + S_e$ can be used to verify that the design values for W and S were correctly implemented on the photomask and were measured correctly by the parametric test equipment. If magnification (or a change in pitch) occurs, then the design value cannot be used for L_b and L_s, and the distance between the voltage taps must be measured-visually.

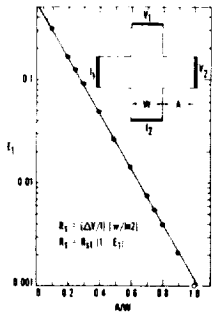

Fig. 4. The error in measuring the sheet resistance from the Greek cross due to short arms. Keeping $A >= 2W$ eliminates the geometrical error in calculating the sheet resistance from the van der Pauw equation [5, eq. (1)].

IV. Design Considerations

The design of the split-cross-bridge resistor follows from four geometrical design rules. If these rules are followed, then the equations given in Section II can be used directly to obtain results that are accurate within one percent.

The split-cross-bridge resistor was laid out so that it could be probed with a 2 by N probe array [5] where N is an arbitrary positive integer. As illustrated in Fig. 1, $N = 4$, and the probe pads are 80-μm squares separated by 80-μm spaces.

The cross resistor is constructed from two equal-width rectangles that intersect at right angles. Design rule #1 requires that the length A of each arm of the cross be at least twice the arm width W in order for the sheet resistance R_s to be calculated accurately from the idealized sheet resistance expression (see (1)). This rule follows from a detailed analysis of this structure [4]; the result of the analysis is shown in Fig. 4. The R_s as calculated from (1) is slightly less than the true sheet resistance, $R_{s'}$ as given by

$$R_s = R_{s'}(1 - E_1) \tag{8}$$

where E_1 is the geometrical error. By extrapolating the curve in Fig. 4, the error for $A >= 2W$ is seen to be negligible.

As applied to the split-cross-bridge resistor, design rule #1 requires that $A >= 2W_b$ for the cross and bridge portion of the structure. The $A >= 2W_b$ (rather than $A >= W_b$) rule was chosen to include the design of diffused structures where lateral diffusion is a factor. If a structure has an excessively large lateral diffusion (such as a p-well in a CMOS process), the designer may have to calculate a suitable A/W_b ratio to minimize errors.

The following discussion applies to both the bridge resistor and the split-bridge resistor. Bridge resistors are constructed from a conducting channel that is tapped in two places along the length of the channel. There are three design rules to be considered. They include the distance

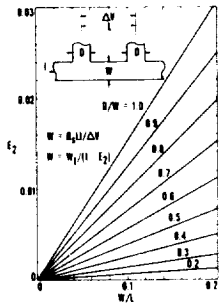

Fig. 5. The error in measuring the linewidth from a bridge structure due to perturbations in the channel current flow at the voltage taps.

between and width of the taps, the length of the taps, and the location of the tap relative to a change in the channel width.

Design rule #2 requires that the width D of the voltage taps be designed at the minimum width allowed and that the distance L between the taps be large enough so that the channel width can be calculated accurately from the uncorrected rectangular resistor expression ($W = R_s L/R$). This rule follows from a detailed analysis of the bridge resistor shown in Fig. 5.

This analysis is based upon the results of conformal mapping described by Hall [6] where the length of the tap is much larger than its width. His result [6, eq. (48)] indicates that the resistance of a bridge between the voltage taps is given by

$$R = R_{sh}(L/W)(1 - E_2) \tag{9}$$

where the geometrical error E_2 is

$$E_2 = (2W/\pi L)[(D/W)\tan^{-1}(D/2W) - \ln(1 + (D/(2W))^2)]. \tag{10a}$$

The uncorrected channel width is

$$W = (R_{sh}/R)L \tag{10b}$$

where L is the distance between the voltage taps and D is the width of the tap. From this expression

$$W = W_t/(1 - E_2) \tag{11}$$

where W_t is the true channel width. This indicates that W, as calculated from the idealized rectangular resistor equation (see (10b)), is slightly larger than the true width W_t.

The distance between and the width of the voltage taps of the bridge resistors were chosen to reduce the geometrical error to an acceptable amount. For the structures included in this study, the width of the voltage taps was taken as the minimum width allowed where $L_b = 160\ \mu m$ and $L_s = 140\ \mu m$. The errors for E_2 are listed in Table I, where E_{2b} is the error for the bridge resistor and E_{2s} is the error for the split-bridge resistor. The errors are worse for the metal layer, but even for this worst case, the error is less than one half of 1 percent.

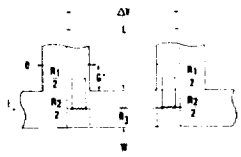

Fig. 6. Resistor model of the bridge structure used to estimate errors induced by bridge taps.

Design rule #3 requires that the length G of a tap from the current carrying channel be at least twice the width D of the tap for the channel width W to be calculated accurately from the uncorrected rectangular resistor expression ($W = R_s L/R$). This rule follows from a resistor model developed for the bridge as shown in Fig. 6. Each major area of the resistor is assigned an equivalent resistor that is calculated from the rectangular resistor equation. The objective of the model is to determine the parameter "g," which indicates the effect of the tap in diverting current from the channel. The resistor model leads to

$$R = R_{sh}[(L/W) - E_3] \tag{12}$$

where

$$E_3 = (D/W)/[1 + (W/gD)]. \tag{13}$$

The resistor model tap length is G^* where $G^* = gD$.

The parameter "g" was evaluated by finding a value for g that provides a good fit between a plot of E_3 versus D/W and an analytical expression derived from Hall's equation [6, Eq. (48)]

$$E_4 = (L/W)E_2 = (2/\pi)[(D/W)\tan^{-1}(D/2W) - \ln(1 + (D/(2W))^2)]. \tag{14}$$

This equation is applicable to the case where the tap is much longer than its width and was derived from conformal mapping theory. Equation (13) is a very good approximation to (14) for $g = 0.18$. This result indicates that only a small fraction of the tap serves to shunt the current from the main channel. The design rule requires that the design tap length $G >= 2D$. This means that the design requirement for G/D is 11.1 times larger than required by the model ($G^*/D = g = 0.18$), which should minimize errors due to terminating the taps.

Design rule #4 requires that the edge of a voltage tap be located twice the channel width from a change in the channel width for the channel width W to be calculated accurately from the uncorrected rectangular channel resistor expression ($W = R_s L/R$). As applied to the split-cross-bridge shown in Fig. 1, this rule allows one to establish the distances H_b and H_s shown in the figure. This rule follows from a detailed analysis of current flow past a discontinuity in the width of the channel as shown in Fig. 7. The analytical expression [6] for the current density $J(x)$ along the x-axis is

$$J(x) = \sqrt{1 + t}/\sqrt{1 + f^2 t} \tag{15}$$

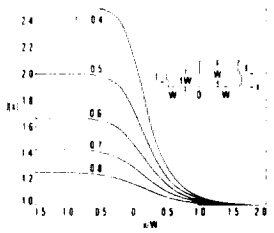

Fig. 7. Current density along the bottom edge of a conducting layer that abruptly changes width. Keeping voltage taps a distance that is twice the width of the channel from the discontinuity, minimizes this error in calculating the linewidth from (6).

where f is the ratio of the width of the smaller channel to the width of the larger channel. The distance along the x-axis is

$$x = [\ln (a/b) - f \ln (c/d)]/\pi \tag{16a}$$

$$a = \sqrt{1 + t} + \sqrt{1 + f^2 t} \tag{16b}$$

$$b = \sqrt{1 + t} - \sqrt{1 + f^2 t} \tag{16c}$$

$$c = \sqrt{1 + f^2 t} + f\sqrt{1 + t} \tag{16d}$$

$$d = \sqrt{1 + f^2 t} - f\sqrt{1 + t} \tag{16e}$$

where the parameters t and u that link the above equations are given by

$$t = \exp(-2u). \tag{17}$$

These equations were derived from Hall's equations [6, eqs. (40) and (41)] using the transformation $2 \tanh^{-1}(z) = \ln [(1 + z)/(1 - z)]$.

The results shown in Fig. 7 indicate that the current density settles out in a distance that is less than twice the channel width from the discontinuity. This is true for both the small and the large channels. Notice that design rule #4 is conservative with respect to the large channel. That is, the W shown in Fig. 7 is one-half the width of the bridge resistor.

V. Experimental Results

Measurement procedures for evaluating the sheet resistance and the electrical linewidth are detailed elsewhere [1], [3], [7]. These procedures require the bridge voltage to be measured for current flowing in both directions along the channel. This procedure is intended to eliminate errors introduced by voltage offsets due to instrumentation errors and thermal voltages at switch relays. The elimination of such errors assumes that the current reversal is accurate. Also, the sheet resistance as determined from the cross resistor should result from the average of four resistance measurements. One measurement requires currents to be forced in both directions between point I_1 and I_2 and voltages measured between V_1 and V_2. The other measurement requires currents to be forced in both directions between points I_1 and V_1 and voltages measured between V_2 and I_2 [3], [7]. A minimum of eight resistance values is required to measure R_s, W, S, and P, from the split-cross-bridge resistor. In addition, the currents forced through the structures must be adjusted to avoid various interference effects such as self-heating. These effects are discussed at length in [7]. Additional measurements can be used to determine if any of these effects are a significant factor.

The procedures for measuring the optical linewidth of the layers are given below. The procedures were developed to minimize magnification errors associated with the SEM. The test structures used for this comparison consisted of 14 different split-cross-bridge resistors arranged on a test chip. These structures were fabricated using a 3-μm CMOS bulk process. Two sizes of structures were designed for each of seven layers: metal layer, n^+ diffusion layer, p^+ diffusion layer, n^+ poly layer on field oxide (thick oxide), n^+ poly layer on gate oxide (thin oxide), p^+ poly layer on field oxide, and p^+ poly layer on gate oxide. Two different manufacturers fabricated the test chip and four test chips were randomly chosen from each run.

The linewidths on these structures were first measured electrically and then optically. The electrical measurements were made using an automatic data acquisition system with a computer controlled wafer prober. For this study, the test currents forced through each structure were 1 mA for the polysilicon on gate oxide, 500-μA for the polysilicon on field oxide and n^+ diffusion layers, 200-μA for the p^+ diffusion, and 5 mA for the metal layer.

After measuring the structures electrically, the silicon dioxide protective passivation was chemically removed from each test chip to expose metal and poly linewidths of the split-cross-bridge resistor patterns. In the process, some of the thermally grown field oxide was removed from the edges of the diffusion layer lines thus increasing the apparent optical width of these lines. The amount of this oxide removed was not strictly controlled and thus varied from chip to chip. The lines of each structure were then photographed using a SEM. The following procedures were used to minimize magnification errors while taking these photomicrographs.

All photomicrographs of each chip were taken in one continuous session. At the beginning of each session a photomicrograph was taken of an NBS linewidth standard [8] at both magnification values (2000× and 5000×) used in this study. Once the session began, the high voltage was never turned off and the chamber was never pressurized and re-evacuated as this could affect the magnification properties of the SEM. Magnification was selected by a multiposition switch only. Each discrete magnification value was therefore calibrated by using an NBS standard. No image enhancement (such as electronic focus compensation) was used. Instead, the NBS standard and test structures were focused by moving the sample into and out of the field of focus, since electronically changing the focus could change the magnification to an unknown

value. For this analysis we selected a SEM with a record of electronic stability and low magnification drift.

For the purpose of obtaining clear pictures, all samples were photographed at a tilt angle of 45 degrees to the electron beam. The tilt axis was perpendicular to all distances being measured.

Two photomicrographs were taken of each split-cross-bridge resistor structure, one of the wide bridge line and one of the split-bridge region. The second photomicrograph thus contained two lines. Thus, a total of 224 photomicrographs (2 photos × 2 bridges × 7 layers × 4 chips × 2 manufacturers) were taken of the structures providing a potential 224 independent data points (one data point per wire width). Some of the structures were damaged when the oxide layers were removed. In addition, linewidth data from all structures with an electrically measured pitch error greater than 3 percent were considered unreliable and not used. Therefore, only 199 of the photomicrographs were used in this analysis.

The linewidths were measured on the photomicrographs using a vernier caliper and a magnifying lens. The vernier provided readings in thousandths of inches. The width of each line segment was measured in three places: near the top and bottom and in the middle of the photomicrograph. This resulted in three or six measurements from each photomicrograph depending on whether the photo was of the bridge or split part of the structures.

The measurements from each photomicrograph were averaged separately and an uncertainty for each average was calculated based on the spread of the data. These uncertainties were typically less than one half of 1 percent. The averages for each of the NBS photomicrographs, along with the certified distances for the NBS standard were used to determine a multiplying factor for each chip/magnification combination. These were then used to convert the average values for each linewidth measurement to a width in micrometers. The averaged linewidth values were then used to fit the data using an unweighted linear least squares fit [9]. A separate fit was calculated for each layer from each manufacturer. These are shown in Table III. A sample set of data points are shown with their least squares fit line in Fig. 8.

Table III shows good agreement between the electrically and optically measured linewidths for metal and poly layers over a range of linewidths. The near unity slopes (M) indicate that the given intercepts (B) are representative of the offsets for the range of linewidths studied. The visual measurements are typically a quarter of a micrometer larger than the electrical measurements. The table also shows a definite correspondence between electrical and optical linewidth measurements of the diffusion layers. Because the apparent diffusion linewidth was increased when the oxide layer was removed, the offsets shown for the diffusion layers are useful only as upper limits of the expected offset. More elaborate techniques such as taking cross sections of linewidth samples are necessary to determine a more realistic expectation of offset values for the diffusion layers. Others have made similar comparisons between optical and electrical linewidth measurements of polysilicon lines for the standard cross-bridge resistor [10] and the Kelvin bridge test structure [11].

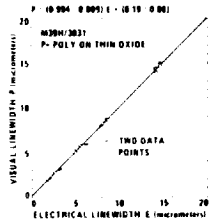

Fig. 8. Visual versus electrical linewidth measurements of p^+ poly on thin oxide plotted along with linear least squares fit line. The equation for the line is given above the plot.

TABLE III
VISUAL P (IN MICROMETERS) VERSUS ELECTRICAL E (IN MICROMETERS) LINEWIDTH RELATIONSHIP $P = ME + B$ FOR SPLIT-CROSS-BRIDGE RESISTORS

Layer	$M \pm M_\sigma$ (unitless)	$B \pm B_\sigma$ (μm)
Run M19G		
N+ Poly (Thick Ox)	1.007+/-0.009	0.46+/-0.09
N+ Poly (Thin Ox)	1.004+/-0.009	0.34+/-0.09
P+ Poly (Thick Ox)	1.012+/-0.010	0.20+/-0.10
P+ Poly (Thin Ox)	1.010+/-0.009	0.26+/-0.08
N+ Diffusion	0.987+/-0.020	1.33+/-0.23
P+ Diffusion	0.991+/-0.013	1.37+/-0.16
Metal	0.985+/-0.006	0.25+/-0.10
Run M19H		
N+ Poly (Thick Ox)	1.002+/-0.006	0.38+/-0.36
N+ Poly (Thin Ox)	1.000+/-0.009	0.30+/-0.08
P+ Poly (Thick Ox)	1.008+/-0.012	0.16+/-0.10
P+ Poly (Thin Ox)	0.994+/-0.009	0.19+/-0.08
N+ Diffusion	0.993+/-0.009	0.34+/-0.13
P+ Diffusion	0.987+/-0.016	0.31+/-0.24
Metal	1.003+/-0.014	-0.01+/-0.20

Maximum Sample Size = 8 structures/layer/run. Total Sample Size = 199 data points (two linewidth data points per structure). Test Chip 3031. M_σ and B_σ are one-sample standard deviations.

A comparison of electrical measurements with the designed values of W, S, and P_t is given in Table IV. The data are based on measurements from four structures per layer. The structures used for this comparison were the smaller of the two split cross bridges on each layer from one of the manufacturers. In order to provide a typical set of measurement values, electrical values from all of these structures were used regardless of deviations in line pitch, which in some cases exceeded our 3-percent limit. As seen in the table, the measured linewidth and line spacing values deviate significantly from the design values W_0 and S_0. In spite of this deviation, the mean line pitch errors were less than half of 1 percent, and the measured line pitch values P_{te} were for most cases, within 2 percent of the design line pitch values, $P_{t0} = W_0 + S_0$. Thus the $P_{te} - P_{t0}$ values are useful in identifying bad data.

VI. Discussion

In order to calculate R_s, S, W, and P_t from (1), (5), (6), and (7), the split-cross-bridge resistor shown in Fig. 1 must be designed according to the following layout rules.

TABLE IV
EXPERIMENTAL RESULTS: ELECTRICAL AND DESIGN VALUES FROM SPLIT-CROSS-BRIDGE RESISTORS

Layer	R_s +/- R_s ohms/sq.	$<W_e>_m$ / $W_{e\,\mu m}$	W_d μm	$<S_e>_m$ / S_e	S_d μm	$<P_{te}>_m$ / P_{te}	PITCH ERROR PERCENT
N+Poly(1)	16.8+/-0.8	2.08+/-0.11	3.0	3.92+/-0.36	3.0	6.01+/-0.09	0.16+/-1.4
N+Poly(2)	17.0+/-1.1	2.13+/-0.11	3.0	3.85+/-0.33	3.0	5.98+/-0.05	-0.37+/-0.8
P+Poly(1)	38.0+/-13.8	2.28+/-0.29	3.0	3.70+/-0.37	3.0	5.97+/-0.14	0.44+/-2.36
P+Poly(2)	37.5+/-14.1	2.28+/-0.33	3.0	3.70+/-0.32	3.0	5.99+/-0.10	-0.25+/-1.73
N+Diff.	16.6+/-0.9	5.45+/-0.04	4.5	3.57+/-0.04	4.5	9.02+/-0.01	-0.22+/-0.09
P+Diff	49.8+/-1.0	5.93+/-0.06	4.5	3.05+/-0.06	4.5	8.98+/-0.01	-0.22+/-0.08
Metal(3)	19.3+/-0.12	4.36+/-0.14	4.5	4.63+/-0.08	4.5	8.97+/-0.07	-0.29+/-0.8

$P_{to} = W_o + S_o$; $<P_{te}>_m = <W_e>_m + <S_e>_m$. Run #09H. Sample size = 4 structures/layer. (1) Thick Oxide, (2) Thin Oxide, and (3) Metal. R_s in milliohms per square. PITCH ERROR = [(<P_{te}>$_m$ - P_{to}) +/- P_{te}-P_{to}]. R_s, W_e, S_e, and P_{te} are one-sample standard deviation.

Rule #1: The length A of the arm of each cross must be at least twice the arm width W_b ($A >= 2W_b$).

Rule #2: The width D of the voltage taps of the bridge resistor must be designed at the minimum width allowed and the distance, L_b and L_v, between the voltage taps must be large enough so as to minimize error E_2; see Fig. 5.

Rule #3: The length G of the voltage taps from the current carrying channel must be at least twice the width D of the voltage taps ($G >= 2D$).

Rule #4: The distance H_b and H_v from the edge of a voltage tap to a change in the channel width must be at least twice the width of the channel ($H_b >= 2W_b$, $H_v >= 2W_v$).

The experimental results obtained for this structure are meant to demonstrate the "reduction to practice" of this structure. The results are not meant to assure the user that the structure will provide valid measurements for all possible linewidths and spaces. Some workers have suggested that small lines will be overetched more than large lines. If the etching is nonlinear in linewidth, the measured line pitch will not equal the design line pitch. This inequality will alert the user to the discrepancy. Additional experimental studies are needed to confirm the usefulness of this test structure in measuring lines in the one micrometer and smaller range. However, the results from the cross-bridge resistor [10] would encourage the use of the split-cross-bridge resistor in the submicrometer linewidth region.

VII. Conclusion

The split-cross-bridge resistor is a compact test structure for measuring the sheet resistance, linewidth, line spacing, and line pitch between various kinds of conducting lines using electrical-measurement techniques. A model was developed to relate the electrical measurements of linewidth and spacing to visual measurements. According to this model, the electrical and visual techniques give different results for the linewidth and spacing measurements due to lateral diffusions and the coating of layers. For a coated layer, the optical linewidth is larger than the electrical linewidth by about twice the thickness of the coating. For pitch measurements, the visual and electrical techniques measure the same quantity provided features have not been magnified during the photomask and wafer fabrication processes. If magnification can be ruled out, then the electrical measurement of line pitch can be used to assure that R_s, W, and S values were measured correctly. Fourteen kinds of test structures were designed to measure the sheet resistance, linewidth, line spacing, and line pitch of metal, poly, and diffused layers. These structures were measured electrically and then optically using a SEM. The optical measurements were typically a quarter micrometer greater than the electrical measurements for the poly and metal layers. More sophisticated methods, such as cross section measurements, are needed to determine the relation between electrical and optical measurements of diffusion linewidths. The electrically measured line pitch values are within 2 percent of the design values for most cases.

Acknowledgment

Several staff members assisted in the development of this project: C. Pina laid out the test structures, B. Blaes and H. Sayah wrote the test programs, and H. Sayah acquired the electrical data. Technical discussions with T. Griswold and S. Suszko, both of JPL, D. Perloff of Prometrix, L. Linholm of NBS, P. Losleben of DARPA, and the wafer fabrication services of the Information Sciences Institute are gratefully acknowledged.

References

[1] M. G. Buehler, S. D. Grant, and W. R. Thurber, "Bridge and van der Pauw sheet resistors for characterizing the line width of conducting layers," *J. Electrochem. Soc.*, vol. 125, no. 4, pp. 650-654, Apr. 1978.

[2] D. Nyyssonen, "Calibration of optical systems for linewidth measurements on wafers," *SPIE*, vol. 221, pp. 119-126, 1980.

[3] L. J. van der Pauw, *Philips Res. Rep.*, vol. 13, p. 1, 1958, also in *Philips Tech. Rev.*, vol. 20, p. 220, 1958.

[4] J. M. David and M. G. Buehler, "A numerical analysis of various cross sheet resistor test structures," *Solid-State Electron.*, vol. 20, pp. 539-543, 1977.

[5] M. G. Buehler, "Comprehensive test patterns with modular test structures. The 2 by N probe pad array approach," *Solid State Technol.*, pp. 89-94, Oct. 1979.

[6] P. M. Hall, "Resistance calculations for thin film patterns," *Thin Solid Films*, vol. 1, pp. 277-295, 1967-1968.

[7] M. G. Buehler and W. R. Thurber, "An experimental study of various cross sheet resistor test structures," *J. Electrochem. Soc.*, vol. 125, no. 4, pp. 645-650, Apr. 1978.

[8] B. Ballard and F. Ogburn, *National Bureau of Standards Certificate Standard Reference Material 484h, Scanning Electron Microscope Magnification Standard (A Stage Micrometer Scale)*. Washington, DC: National Bureau of Standards, Nov. 6, 1980.

[9] D. C. Baird, *Experimentation: An Introduction to Measurement Theory and Experiment Design*. Englewood Cliffs, NJ: Prentice-Hall, Inc., 1962.

[10] L. W. Linholm, D. Yen, and M. W. Cresswell, "Electrical linewidth measurement in the near- and sub-micron linewidth region," in *Proc. 3rd Int. Symp. VLSI Integration Sci. and Technol.*, pp. 299-308, 1985.

[11] T. F. Hasan and D. S. Perloff, "Automated electrical measurement techniques to control VLSI linewidth, resistivity and registration," *Test & Measurement World*, vol. 5, pp. 78-90, Jan. 1985.

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Chapter 4

Reliability Test Structures

4.1 Introduction

4.1.1 Electromigration

Electromigration is known to have detrimental effects on the reliability of integrated circuits. Therefore, test chips to measure the interconnect and contact electromigration mechanisms have been designed and fabricated in 3-μm CMOS/BULK for wafer level tests.

To test either type of electromigration test chip, it is placed on a temperature controlled wafer chuck and stressed by a current source. A relay matrix is used to bypass burned out segments. A computer controlled tester is used to automate the entire test sequence including stress current application, resistance monitoring, leakage monitoring and data recording. The test procedures for both test chips have been developed and preliminary interconnect electromigration tests have been performed.

4.1.2 Time-Dependent Dielectric Breakdown (TDDB)

In the TDDB studies the step-stress technique is employed to characterize the reliability and integrity of the gate dielectric. The technique consists of a series of constant field tests for a sequence of increasing field values and combines the attributes of the constant field test and the ramped voltage test.

4.2 Layer Electromigration

4.2.1 Test Structures

Figure 4.1 gives the overall layout of the test structure. It is designed for a 2×20 probe pad array and consists of fifteen electromigration stripes connected in series in the first and second metallization layers. The pad functions are listed in Table 4.1 and the metal dimensions are listed in Table 4.2. Figure 4.2 shows a cross section of the test structure, while Figure 4.3 shows an expanded view of the two metal layers. At the end of each segment is a tap which is connected to a double probe pad. Thus each segment contains a Kelvin contact which allows accurate voltage measurements. The first layer stripes run perpendicular to the second layer metal, thus providing a worst-case step coverage for the second layer. The pattern of the poly layer is identical to that of the metal two layer. This provides the steps for the metal one layer.

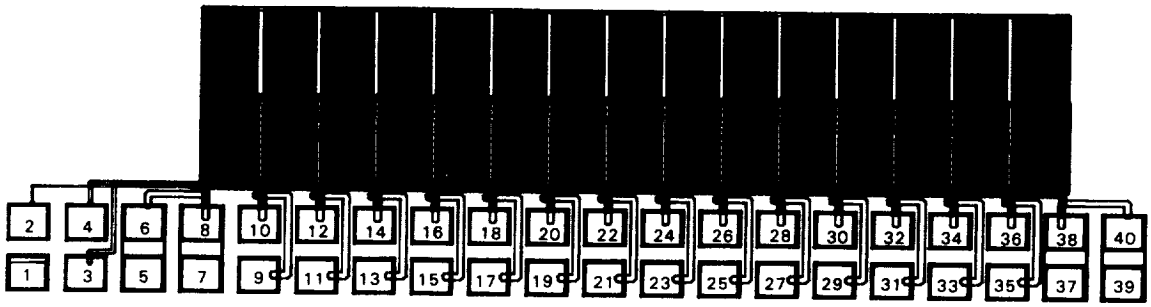

Figure 4.1: The electromigration test structure.

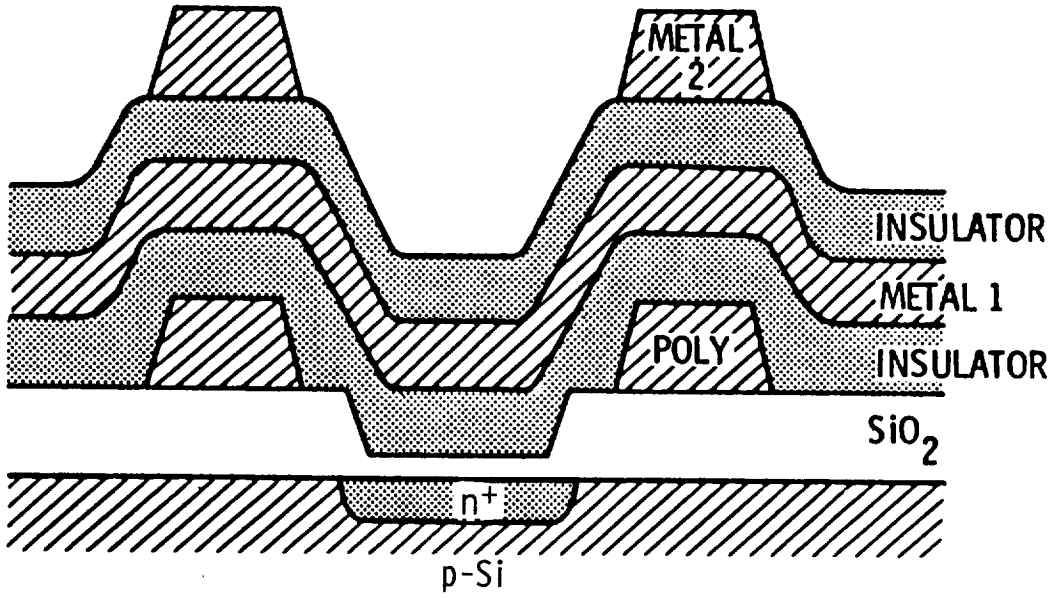

Figure 4.2: Cross section of part of the electromigration test structure.

Table 4.1: The Interconnect Electromigration Test Chip.

Pad #	Name	Pad #	Name
1	Spare	2	Poly
3	M2, Extrusion Monitor	4	M2 Extrusion Monitor
5	M1, End L*	6	M1, End L*
7	M2, End L*	8	M2, End L*
9	M1, Tap 1	10	M2, Tap 1
11	M1, Tap 2	12	M2, Tap 2
13	M1, Tap 3	14	M2, Tap 3
15	M1, Tap 4	16	M2, Tap 4
17	M1, Tap 5	18	M2, Tap 5
19	M1, Tap 6	20	M2, Tap 6
21	M1, Tap 7	22	M2, Tap 7
23	M1, Tap 8	24	M2, Tap 8
25	M1, Tap 9	26	M2, Tap 9
27	M1, Tap 10	28	M2, Tap 10
29	M1, Tap 11	30	M2, Tap 11
31	M1, Tap 12	32	M2, Tap 12
33	M1, Tap 13	34	M2, Tap 13
35	M1, Tap 14	36	M2, Tap 14
37	M2, End R*	38	M2, End R*
39	M1, End R*	40	M1, End R*

L = Left R = Right as seen in Figure 4.1

* Pads pairs 5 & 6, 7 & 8, 37 & 38, and 39 & 40 shown in Figure 4.1 are double pads to allow Kelvin measurement

Table 4.2: Dimensions of Metal Wires in Layer Electromigration Structure.

Layer	Width	Serpentine Length
Metal One	4.5 μm	2.0 cm
Metal Two	7.5 μm	1.0 cm

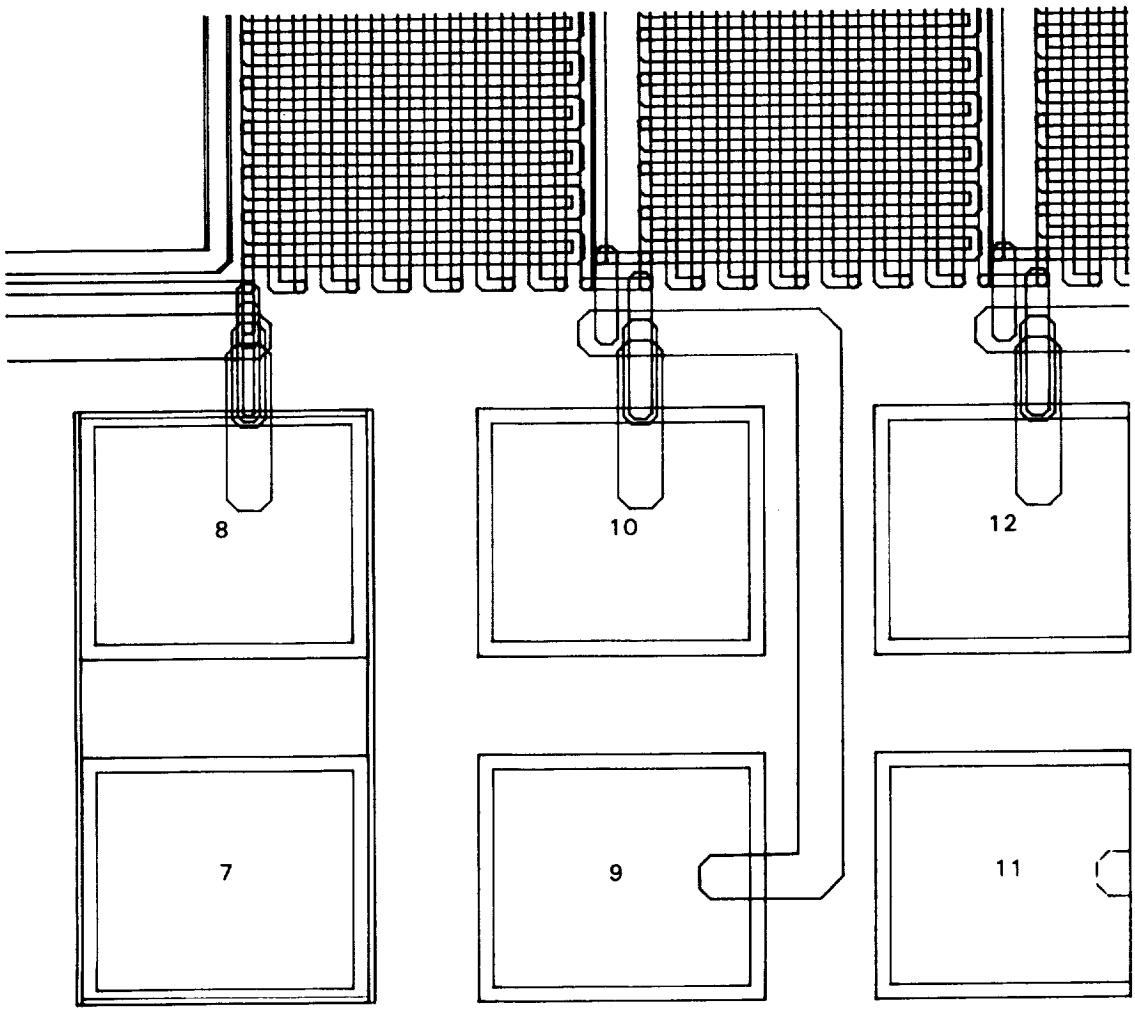

Figure 4.3: Metal one and two layers of the electromigration structure. The metal one wire snakes across the figure from left to right and the metal two wire snakes from top to bottom. As shown in Figure 4.2, the polysilicon wire is directly beneath the metal two wire to create worst-case steps for metal one.

The extrusion monitor (pad 3 or pad 4) is intended to allow a check of the minimum metal spacing design rule and to provide a test for metal extrusion. Pad 2, which is connected to the poly layer, is intended to allow a check of the insulation layers by measuring the leakage currents between layers.

4.2.2 Test Methods

The test procedure for the interconnect electromigration structure consists of several steps:

1. Tests for leakage between the various layers. A voltage is applied to one layer, and the leakage current from the other layer is measured, using the extrusion monitor to test for shorts within layers (metal 1, metal 2, and poly). Then the metal lines are tested for continuity. These tests are designed to eliminate faulty structures.

2. Using a low current (1 mA), the resistance of each of the 15 segments is measured.

3. The resistance measurements are performed at different temperatures.

4. The desired stress temperature is set, the stress current is applied, and the segment resistance is measured and compared with the segment resistance measured previously to determine the actual metal temperature.

During the stress a high current is forced through all fifteen segments. The output voltage of the current source is then monitored. An open segment causes the current source voltage to reach its compliance limit. When a segment opens, its position is determined by locating the voltage transition. In addition to the above measurements, the resistance of each segment under test is measured at one-minute intervals.

4.3 Contact Electromigration

4.3.1 Test Structure

The contact electromigration test chip consists of a total of sixteen different structures having four sizes of square contacts (3.0, 3.3, 3.6, and 3.9 μm on a side) and four contact-to-diffusion spacings (1.5, 2.25, 3.00, and 3.75 μm). A typical structure, shown in Figure 4.4, consists of eight separate p-wells connected to

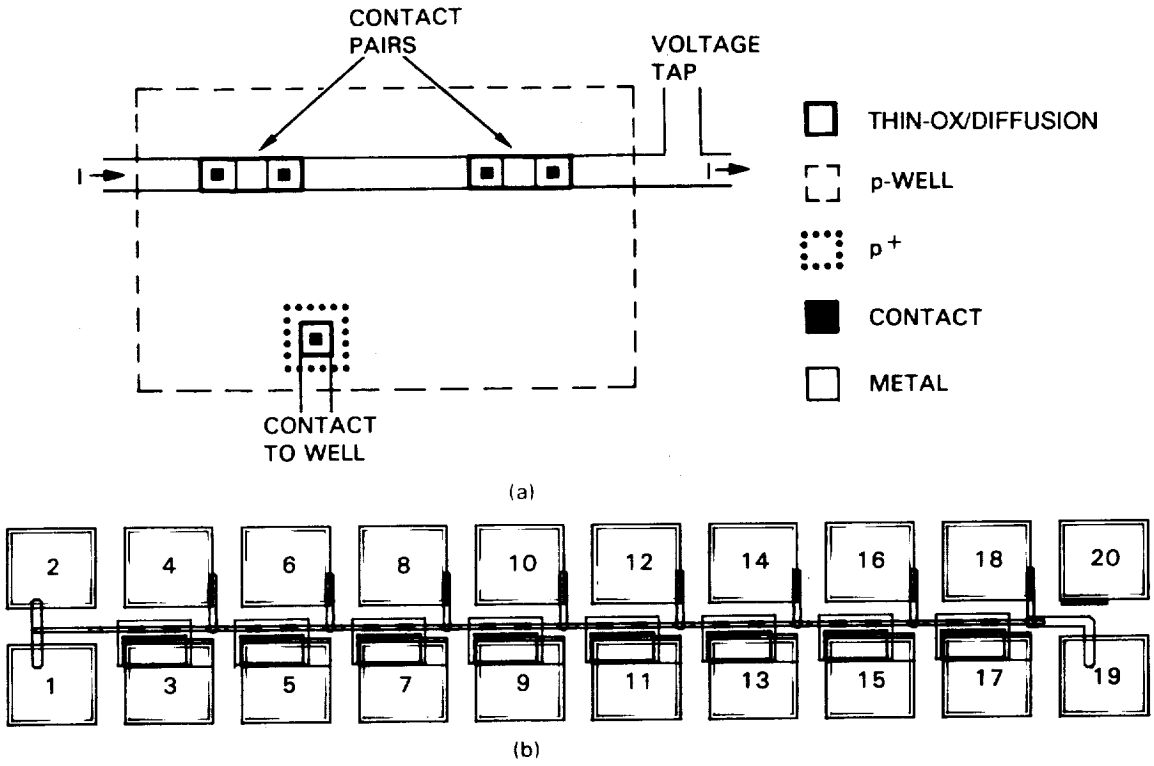

Figure 4.4: The metal–n+diffusion contact electromigration test structure.

the even-numbered pads 4 through 18. Each p-well contains an n+diffusion with contacts on each end. Current is forced between pads 1 and 20. The odd-numbered pads 3 through 19 provide taps to the metallization stripes between the p-wells which are used to monitor the resistance of each segment and also to bypass a failed segment. Aluminum spiking and the resultant reverse-bias junction leakage is monitored using the p-well contacts.

4.3.2 Test Method

To test these structures, a check of the leakage current is made for each set of contacts contained in the individual p-wells to detect initial faults. If the structure is found to be free of faults, a stress current is forced through the contact chain at elevated temperature. On regular intervals (3 minutes) the stress is interrupted and the n+ to p-well leakage current and the contact resistance of each pair of contacts is measured. If a leakage exceeds $1\,\mu$A or the resistance is found to have increased by a factor of 2.0, the contact pair is considered failed. The failed contact pair is then bypassed through an external switch matrix and the test continued.

4.4 Time-Dependent Dielectric Breakdown

4.4.1 Test Structure

The Time-Dependent Dielectric Breakdown (TDDB) structure consists of two side-by-side structures each probed by a 2×20 padblock as seen in Figure 4.5. There are 76 sub-structures, where half are n-channel and half are p-channel. These structures are essentially ganged arrays of MOSFETs. As shown below, a large number of theses structures must be measured in order to acquire a statistically significant amount of data.

The test structure also contains several large geometry gate oxide capacitors to measure the gate oxide thickness.

4.4.2 Test Method

The test structures are first screened at low voltage (3 to 5 V) for shorted capacitors which are then excluded from the life test experiment. The criterion for shorted capacitors varies with the size, oxide thickness, and other characteristics of the test device. Typically, a gate oxide leakage current in excess of one nanoampere indicates a dielectric failure.

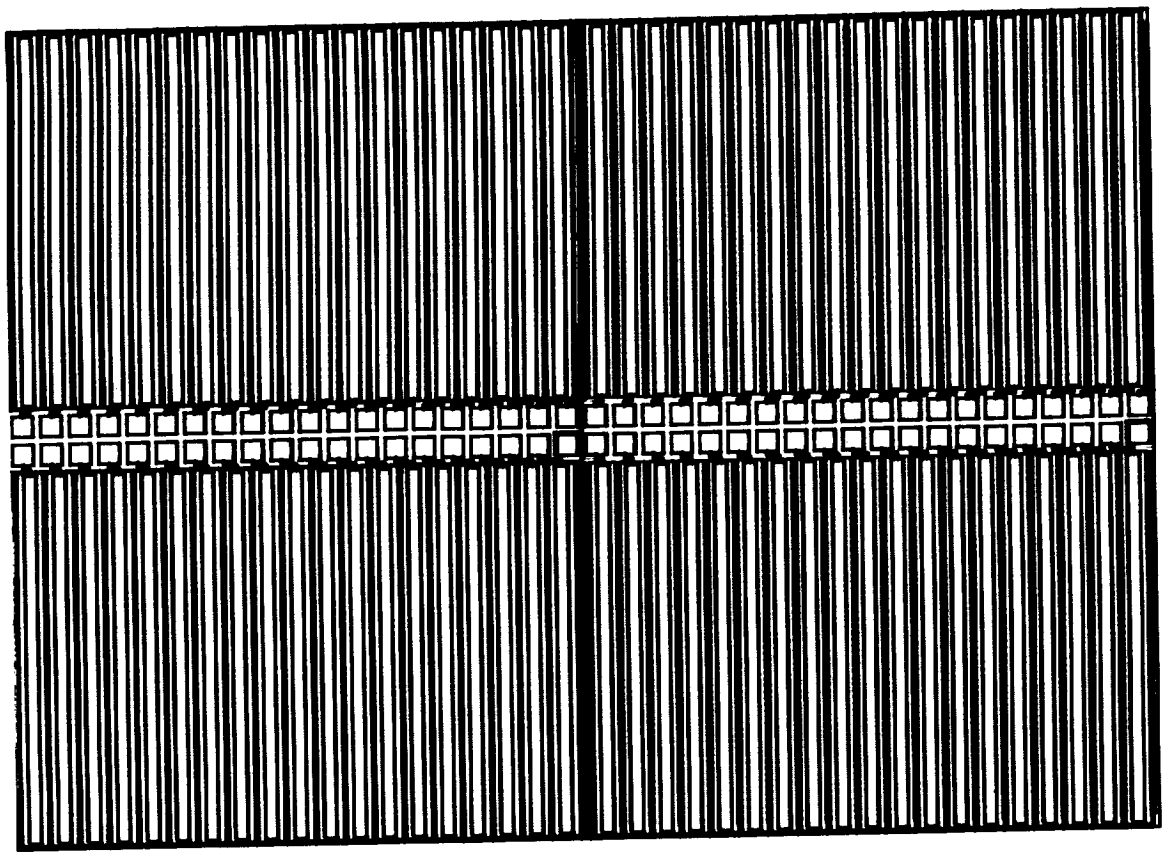

Figure 4.5: The time-dependent dielectric breakdown structure. This structure consists of two arrays, each addressed by a 2 $\times$ 20 probe pad array found in the center of the structure. Thus two probe set-downs are required to measure the 76 capacitors (38 n-channel and 38 p-channel) in this test structure.

For TDDB evaluation we use the step-stress technique [20,21]. This technique combines the conventional TDDB and the ramp breakdown measurements. For a set of oxide field values E1, E2, ..., En arranged in increasing order, the field E1 is applied to the test structure consisting of a set of 38 large capacitors. The stress is interrupted after cumulative times of, say, .01, .1, 1, 10, and 100 seconds and the individual capacitors are examined for dielectric failure. The failure data are recorded and the failed devices are disconnected using an external switch matrix after each interruption of the stress. This procedure is repeated for all of the field values in the set. As an example, the values 4.5, 5.5, 6.5, and 7.5 MV/cm constitute a reasonable set for this purpose. At the higher fields (about 7 MV/cm and above), however, the breakdown mechanism changes. At high electric fields, oxide conduction is dominated by Fowler-Nordheim currents. This introduces failure modes not present under circuit use conditions. Therefore, caution must be exercised in the analysis of high field data.

4.4.3 Analysis Method

It has been experimentally observed that the time-to-failure distribution for the gate dielectric at constant field exhibits a log-normal behavior and thus, on a log-normal plot, it is represented as a straight line. Further, it has been shown that if the stress field is varied this distribution changes only in the value of the median-time-to-failure, t_{50}, and is otherwise unaffected. The extent of the change in t_{50} in response to the change in the field is given by the acceleration factor, γ [22]. If γ were known, the step-stress data could be reduced to a sequence of equivalent times-to-failure under the normal operating field (or any other field). As discussed above, the data should then give a straight line on a log-normal plot. Therefore, one can resort to a parameter fitting algorithm to determine the acceleration factor. The analysis simply involves locating the value of γ which best fits a straight line to the entire data set. Therefore, only one parameter, the acceleration factor, needs to be fitted. Once the value of this parameter is established, the standard deviation, σ, and t_{50} of the distribution can be calculated.

Fortran codes were written to analyze the results of the step-stress experiments. The program was subsequently tested for stability and sensitivity using modeled data with known parameters. They were calculated using a random number generator. These data simulate the results of the experiments conducted on a sample population of finite size with the assumed values of the failure pa-

Table 4.3: Examples of modeled data for the step-stress oxide breakdown experiment. The assumed parameters are: $\gamma = 7.6$, $\sigma = 11.6$, $E_0 = 1\text{MV/cm}$, and $t_{50} = 1.7 \times 10^{19}$ s. For these values $\ln t_{50} = 44.3$ and $t_1 = 1$ year. For the numbers picked, time to 1% failure just happened to come out equal to one year.

	E	— Cumulative Time (s) —				
	(MV/cm)	0.01	0.1	1	10	100
Exact						
S0:	4.5	0.02725	0.04232	0.06352	0.09219	0.12948
	5.5	0.12282	0.15052	0.19311	0.25087	0.31788
	6.5	0.32349	0.35234	0.41632	0.49338	0.57202
	7.5	0.57817	0.60878	0.67143	0.73845	0.79862
Sample Size = 3200						
S1:	4.5	0.03625	0.05063	0.07344	0.10219	0.13969
	5.5	0.14281	0.15656	0.20437	0.26156	0.33781
	6.5	0.34250	0.37062	0.43281	0.50625	0.58594
	7.5	0.59219	0.62094	0.68500	0.75281	0.80813
S2:	4.5	0.02688	0.04094	0.06344	0.08781	0.12562
	5.5	0.12781	0.14312	0.18844	0.25375	0.31813
	6.5	0.32344	0.34969	0.41625	0.49469	0.56875
	7.5	0.57500	0.60281	0.66219	0.72938	0.79188
S3:	4.5	0.02313	0.04156	0.06344	0.09281	0.12344
	5.5	0.12500	0.14375	0.18375	0.24469	0.30750
	6.5	0.31406	0.34219	0.40531	0.48000	0.56000
	7.5	0.56500	0.59406	0.65500	0.72688	0.79500

rameters γ, σ, t_{50}, and a failure distribution given by

$$f(\ln t) = \frac{1}{\sigma\sqrt{2\pi}} \int_{-\infty}^{\ln t} \exp\left(-\frac{\ln t' - \ln t_{50} + \sigma(E - E_0)}{2\sigma}\right) d\ln t'$$

where E is the oxide field and E_0 is some reference field taken for simplicity to be the operating field. It can be argued that the oxide field factor should be in the form of $1/E$.

The data contains the purely statistical noise that is present in real data due to finite sample size. Table 4.3 gives an example of modeled data sets, S_i, calculated by introducing random noise. The set S_0 is from an exact (not randomly generated) calculation based on the assumed values for the parameters and corresponds to the case of an infinite sample size. For the other sets the

Table 4.3: Examples of modeled data for the step-stress oxide breakdown experiment. The assumed parameters are: $\gamma = 7.6$, $\sigma = 11.6$, $E_0 = 1\text{MV/cm}$, and $t_{50} = 1.7 \times 10^{19}$ s. For these values $\ln t_{50} = 44.3$ and $t_1 = 1$ year (Continued).

	E	— Cumulative Time (s) —				
	(MV/cm)	0.01	0.1	1	10	100
Sample Size = 1600						
S4	4.5	0.02313	0.04812	0.07312	0.10063	0.12500
	5.5	0.12562	0.13875	0.18000	0.23937	0.30187
	6.5	0.30687	0.33812	0.40250	0.47938	0.55250
	7.5	0.55687	0.59000	0.66188	0.72562	0.79250
S5	4.5	0.03625	0.04750	0.07250	0.10250	0.13500
	5.5	0.13750	0.15188	0.19437	0.24125	0.30750
	6.5	0.31500	0.34000	0.40437	0.48625	0.57000
	7.5	0.57437	0.60562	0.66938	0.74063	0.79562
S6	4.5	0.02437	0.04188	0.06000	0.09375	0.13375
	5.5	0.13750	0.15687	0.19125	0.25125	0.30812
	6.5	0.31563	0.34563	0.39562	0.47813	0.55937
	7.5	0.56687	0.59938	0.65875	0.72750	0.80125
Sample Size = 800						
S7	4.5	0.01875	0.02875	0.04000	0.05625	0.09000
	5.5	0.09500	0.10750	0.15000	0.20500	0.28125
	6.5	0.28750	0.31125	0.36875	0.46375	0.53875
	7.5	0.54625	0.57125	0.64625	0.72875	0.80000
S8	4.5	0.02625	0.04000	0.06500	0.09250	0.12500
	5.5	0.12750	0.15875	0.19375	0.24125	0.30875
	6.5	0.31625	0.36125	0.41750	0.48125	0.55625
	7.5	0.56250	0.59625	0.65500	0.73000	0.79500
S9	4.5	0.02250	0.03125	0.04375	0.06500	0.11125
	5.5	0.13375	0.13250	0.17125	0.23000	0.30750
	6.5	0.31125	0.33750	0.39625	0.49125	0.58000
	7.5	0.58375	0.60625	0.66625	0.72625	0.78500
S10	4.5	0.02625	0.04000	0.05875	0.08000	0.11625
	5.5	0.12000	0.13250	0.16625	0.22500	0.28875
	6.5	0.29375	0.31625	0.39250	0.47000	0.56250
	7.5	0.56625	0.59625	0.66500	0.74875	0.80625

Table 4.4: Results of the analysis of modeled data in Table 4.3. The assumed parameters are: $\gamma = 7.6$, $\sigma = 11.6$, and $t_{50} = 1.7 \times 10^{19} s$. For these values $\ln t_{50} = 44.5$ and $t_1 = 1.0$ year.

Sample Size	Data Set	Low γ	High γ	Passes	γ	σ	t_{50} (seconds)	t_1 (years)	E_0 MV/cm	Sig. Figs.
Exact	S0	6.48	9.19	308	7.6	11.6	44.3	1.0	1	6
3200	S1	5.21	9.60	335	8.0	12.3	45.7	0.8	1	6
3200	S2	5.79	9.72	311	7.6	11.6	44.4	1.2	1	6
3200	S3	5.41	9.52	290	7.4	11.3	43.2	0.7	1	6
1600	S4	4.79	12.32	309	7.5	11.7	44.3	0.8	1	6
1600	S5	5.09	10.40	295	8.0	12.7	46.9	1.1	1	6
1600	S6	4.24	10.57	323	7.1	11.0	42.5	0.7	1	7
800	S7	4.85	10.21	340	8.1	11.4	48.1	75	1	6
800	S8	5.46	10.15	304	7.7	11.9	45.1	1.2	1	6
800	S9	3.08	11.10	301	7.8	11.2	45.5	8.8	1	7
800	S10	4.80	10.31	291	8.0	11.9	47.2	9.5	1	7

corresponding sample size is given in Table 4.3. For each sample size, the simulations were run a number of times. For the sample size = 3200, the simulations were run three times and each run noted as S1, S2, and S3.

The results of the computer analysis of these data sets are given in Table 4.4. The table groups the data sets by the sample size and in the second column the data sets are identified (S_0, S_1, etc.). The range in which the program searched for the optimal value of the parameter is given by low and high γ which is determined by a zero order consideration of the data. The number of passes in the optimization algorithm and the resulting γ are listed in the next columns along with the corresponding values of σ and t_{50}. The last column gives the algorithm's estimate of the accuracy of the obtained γ stated in terms of significant figures. In addition there is a column for the parameter t_1. It is defined as time to one percent failure. In the study of device reliability we are really interested in the low probability region, one percent or smaller. Therefore t_1 is a more relevant parameter for comparison purposes.

Values for the various S_n are shown in Table 4.4. As can be seen, the values for the S_n vary further from the exact value of 1 as the sample size decreases. This is due to the introduction of statistical noise into the data to simulate the

finite sample size of the actual experiments.

One important variable in designing this type of experiment is the required sample size for statistically meaningful results. Using t_1 as the figure of merit, one observes that for sample sizes of 3200 and 1600, reasonably accurate results can be deduced from the data. An experiment based on 800 samples, however, yields results that may be in error by one or two orders of magnitude.

The conclusions drawn from these exercises are that the algorithm is able to perform the data analyses and appears to provide meaningful results for sample sizes of 1600 or more capacitors (40 test chips minimum). If it is found that n-channel and p-channel oxides are sufficiently alike, the data from both can be combined and only 20 chips are needed.

4.5 Summary of Results and Future Work

Test structures for the study of interconnect electromigration and contact electromigration have been designed and fabricated. Software for automated stress testing of both structures has been developed and debugged. Preliminary testing of the interconnect electromigration structure indicates that a localized self-heating effect is influencing our test results: further investigation is required to resolve this problem and obtain improved results. No test results are available for the contact electromigration structure.

Chapter 5

Device Models and Simulation

5.1 MOSFET Subthreshold Parameter Extraction

5.1.1 Introduction

The extraction of parameters in the subthreshold region is needed to model the leakage currents in SPICE simulations. In addition, the radiation effects community requires a standardized procedure for evaluating the radiation-induced interface oxide trap densities [23]. The purpose of this effort is to develop a standard analysis approach and to show that it is compatible with SPICE-like MOSFET models. The extraction method developed here separates the interface trap terms from body effect or bulk dopant terms and thus allows a more accurate evaluation of the interface state and oxide trap densities.

In this effort, we restrict our view to MOS structures where radiation induces oxide charge and creates oxide-silicon interface states but does not remove carriers from the bulk. These effects shift the threshold voltage and increase the leakage currents of MOSFETs. In order to facilitate the analysis, two reference cases were chosen and these are shown in Figures 5.1 and 5.2. For the p-MOS reference case, shown in Figure 5.1, radiation induces positive oxide charge and

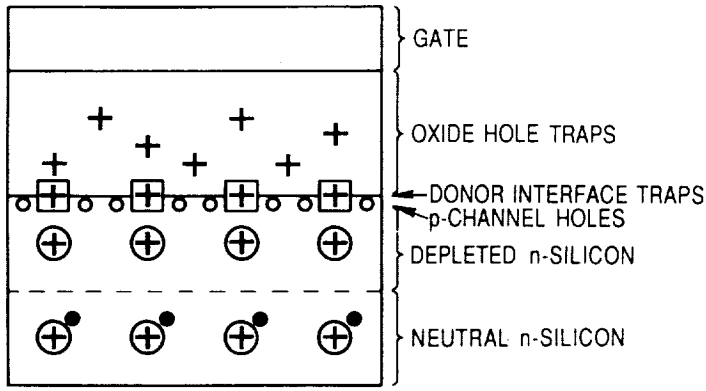

Figure 5.1: The p-MOS reference case.

positive donor interface states. For the n-MOS reference case, shown in Figure 5.2, radiation induces positive oxide charge and negative acceptor interface states [23].

The threshold voltage for a "fat" FET, where short and narrow channel

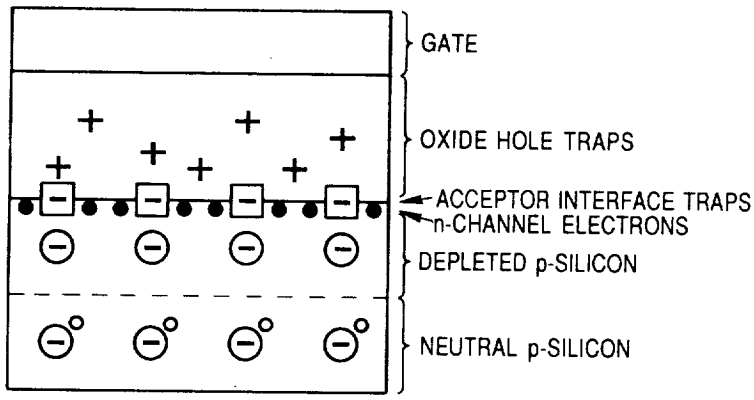

Figure 5.2: The n-MOS reference case.

effects are negligible, is:

$$VTfb = VTo + \Gamma\sqrt{2\phi f - VB} \tag{5.1}$$

where "fb" denotes a fat FET with back-gate bias, VB. For the n-MOS reference case

$$VTo = 2\phi f - Vot + Vit \tag{5.2}$$

and for the p-MOS reference case

$$VTo = 2\phi f + Vot + Vit \tag{5.3}$$

The threshold voltage for a fat FET without back-gate bias is:

$$VTf0 = VTo + \Gamma\sqrt{2\phi f} \tag{5.4}$$

In the above expressions, $2\phi f$ is the built-in potential due to the body doping, Γ is the body effect term, and Vit is the potential due to the interface state charge. Vot is the potential due to trapped oxide charge, interface implant charge, and the gate-silicon work function.

The values associated with the radiation-induced quantities, Vot and Vit, are positive when the sign of the induced charge conforms to the reference case. A negative sign for either Vot or Vit signals the buildup of charge with a sign opposite to that shown for the reference case. The following text is developed for the fat FET where $VT = VTfb$.

The effect on the subthreshold current of the buildup of radiation-induced charge is illustrated for a p-MOSFET in Figure 5.3 and for an n-MOSFET in

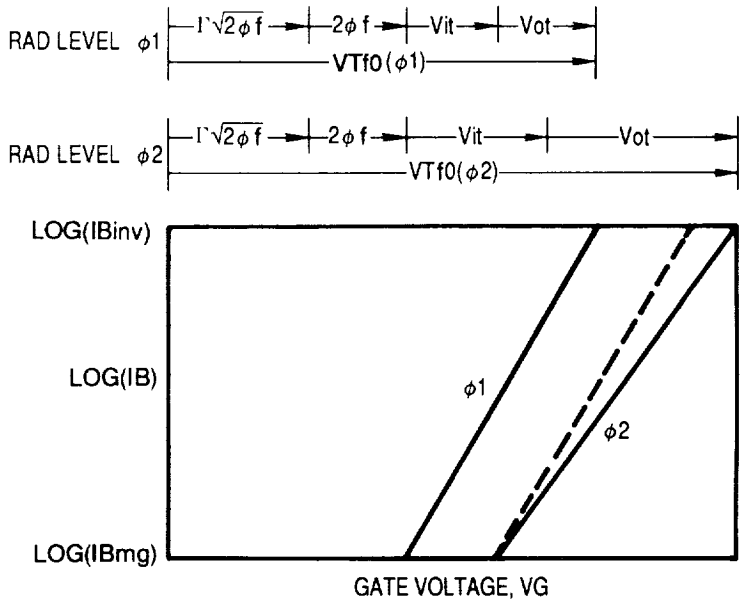

Figure 5.3: Subthreshold characteristics for a p-MOSFET at radiation levels $\phi 2 > \phi 1$. The dashed line indicates how the characteristics shift if Vot changes and Vit does not change with radiation.

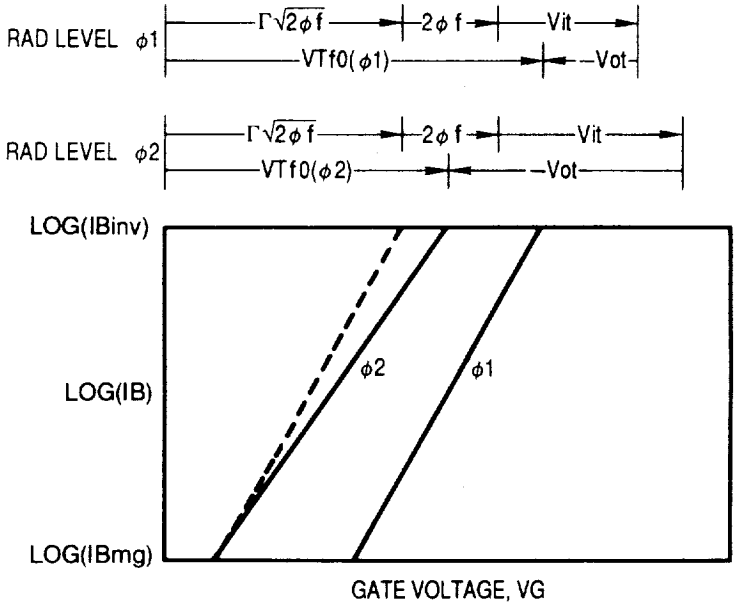

Figure 5.4: Subthreshold characteristics for an n-MOSFET at radiation levels $\phi 2 > \phi 1$. The dashed line indicates how the characteristics shift if Vot changes and Vit does not change with radiation.

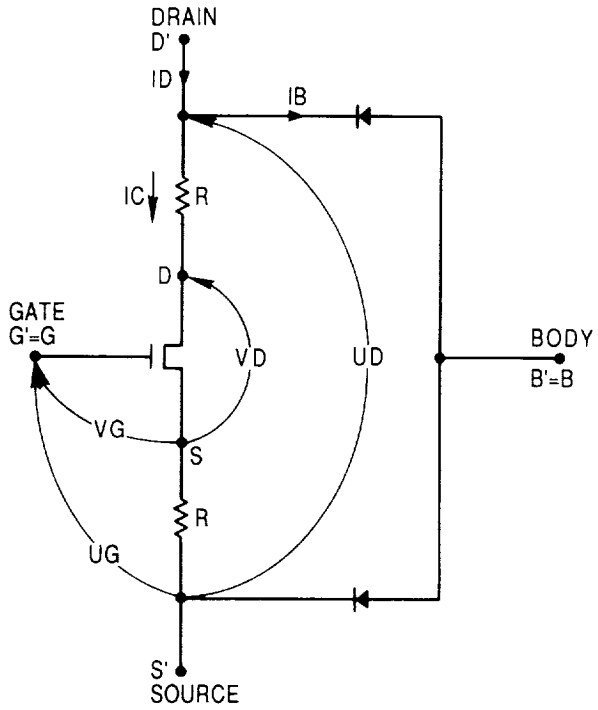

Figure 5.5: The model of an n-MOSFET where the drain and source resistance is R. The subthreshold leakage current passes through the drain-source diodes.

Figure 5.4. These schematic semi-log plots of body current versus gate voltage illustrate how the subthreshold current varies between the onset of inversion (IBinv where $VG = VT$) and the condition where the Fermi level is located at the middle of the band gap (IBmg where $VG \ll VT$). When the Fermi level is at mid gap traps are uncharged; whereas at the onset of inversion, where $VG = VT$, traps are fully charged. For the p-MOSFET, the buildup of positive oxide traps and positive interface traps causes the IB curve shown in Figure 5.3 to shift to higher gate voltages with a smaller slope. For the n-MOSFET, the buildup of positive oxide traps and negative interface traps causes the IB curve shown in Figure 5.4 to shift to smaller gate voltages with a smaller slope.

In the model for the MOSFET shown in Figure 5.5, the measured drain current, ID, enters the extrinsic drain tap, D', splits into the channel current, IC, and the body current, IB, and exits the device at the extrinsic source tap, S'. Thus $ID = IC + IB$. The intrinsic and extrinsic drain-source voltages are VD and UD respectively, while the intrinsic and extrinsic body-source voltages

are VB and UB respectively. In the subthreshold region, the extrinsic voltages are assumed to be equal to the intrinsic voltages since $IC = 0$.

5.1.2 Subthreshold Expression

In the subthreshold region, it is assumed that the current is dominated by diffusion and that the MOSFET appears as a bipolar transistor where the source is the emitter, the drain is the collector, and the body is the uniformly doped base. These assumptions lead to the following expression for the subthreshold current [24]:

$$IB = \frac{\beta \Gamma Vt^2}{2\sqrt{\phi so - VB}} \exp\left(\frac{\phi so - 2\phi f}{Vt}\right)\left\{1 - \exp\left(-\frac{VD}{Vt}\right)\right\} \tag{5.5}$$

where ϕso is the oxide-silicon equilibrium surface potential at the source, ϕf is the bulk Fermi potential, $Vt = kT/q$, T is the temperature, k is the Boltzmann constant, $\Gamma = \sqrt{2\epsilon s \times qN}/Co$, ϵs is the silicon dielectric constant, N is the body dopant density, $\beta = KP \times WE/LE$, $KP = \mu o \times Co$, μo is the channel mobility, $Co = \epsilon o/Xo$ is the gate-oxide capacitance/area, ϵo is the oxide dielectric constant, Xo is the oxide thickness, $WE = W - \Delta W$ is the effective channel width, W is the as-drawn channel width, ΔW is the two-sided channel width shrinkage, $LE = L - \Delta L$ is the effective channel length, L is the as-drawn channel length, and ΔL is the two-sided channel length shrinkage.

In order to evaluate the above expression, ϕso must be related to VG. The following expressions were derived for an n-channel MOSFET where the charge density, electric field, and electric potential relationships are as shown in Figure 5.6. From charge balance considerations at the oxide-silicon interface the charge density (in charge/area) is

$$Qg + Qot = -(Qc + Qb) \tag{5.6}$$

where Qg is the positive gate charge density, Qot is the positive oxide trapped charge density, Qc is the negative channel charge density, and Qb is the negative bulk charge density.

The gate-oxide charge density, Qg, is given by:

$$Qg = Co\psi o = Co(VGB - \psi s) \tag{5.7}$$

where ψo is the oxide potential drop, $VGB = VGS + VSB$ is the gate-body potential drop, $\psi s = \phi s + VCS + VSB$, VGS is the gate-source surface potential drop, VSB is the source-body potential drop, VCS is the channel-source

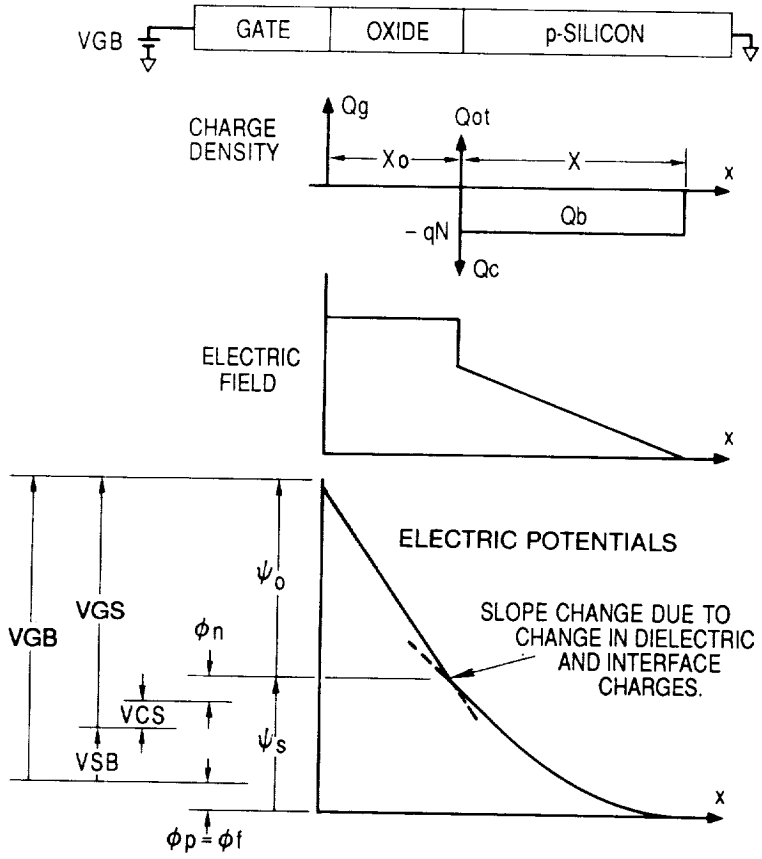

Figure 5.6: Charge density, electric field, and electric potentials for a uniformly doped n-MOSFET.

potential drop, and $\phi s = \phi n + \phi p$ is the equilibrium surface potential. In this derivation $\phi p = \phi f$, where ϕf is the bulk Fermi potential in the bulk region; also ϕn is the Fermi potential at the oxide-silicon interface.

The oxide trapped-charge density, Qot, is due to the as-fabricated oxide charge and other effects which can be represented as a fixed oxide charge. These include the gate-silicon work function and the charge due to ion-implanted dopants which are assumed to be a delta function of dopant located at the oxide-silicon interface. Although this charge is shown located at the oxide-silicon interface, it is evaluated in terms of an equivalent positive charge located on the gate. Thus Qot is expressed in terms of the gate voltage, Vot, and Co:

$$Qot = CoVot \tag{5.8}$$

The channel charge density, Qc, is composed of the channel electrons and the interface trapped charge density, Qit. In the subthreshold region, the channel electron density is zero so the channel charge is made up of interface traps with density Nit. For an n-MOSFET, the Fermi level traverses only the upper half of the band gap where the interface traps are assumed to be negatively charged acceptors. For this case the incremental interface trap density is [25]:

$$qDit = -\frac{dQit}{d\phi s} \tag{5.9}$$

where Dit has units of $1/(\text{Volts} \times \text{cm}^2)$. For simplicity, the acceptor trap density is assumed to be uniformly distributed over the upper half of the band gap. Thus for a given ϕs, the interface charge density is found by integrating Dit from the mid-gap potential, ϕf to ϕs:

$$Qit = -q\int_{\phi f}^{\phi s} Dit\, d\phi s = -qDit(\phi s - \phi f) \tag{5.10}$$

By reasoning similar to that given for Qot, Qit is expressed in terms of an equivalent gate voltage, Vit, and Co as $Qit = CoVit$. The value of Vit is determined for $VG = VT$ or $\phi s = 2\phi f$. Thus $Vit = (qDit/Co)\phi f$. The substitution of this expression into Equation 5.10 yields:

$$Qc = Qit = -CoVit\frac{\phi s - \phi f}{\phi f} \tag{5.11}$$

The total interface trap density over the upper half of the band gap is $Nit = Dit \times \phi f$ with units of $1/\text{cm}^2$. Thus $Nit = CoVit/q$.

The bulk charge density, Qb, represents the depleted bulk acceptor dopants and, for a uniformly doped bulk, is given by [24]

$$Qb = -\Gamma Co\sqrt{\psi s} = -\Gamma Co\sqrt{\phi s + VCS + VSB} \tag{5.12}$$

By combining Equations 5.7, 5.8, 5.11, and 5.12 with Equation 5.6 evaluated at the source where $VCS = 0$, with $VGB = VGS + VSB$, $VG = VGS$, and $VB = -VSB$ we get:

$$VG(\phi so, VB) = \phi so - Vot + \Gamma\sqrt{\phi so - VB} + Vit\frac{\phi so - \phi f}{\phi f} \tag{5.13}$$

where ϕso is ϕs evaluated at the source. This expression is simplified by expanding VG in the variable ϕso and evaluating at the channel inversion point, $\phi so = 2\phi f$. This approach follows Swanson and Meindl [26]; however Fichtner and Potzl [24] expanded VG about $\phi so = 1.5\phi f$ which is halfway between mid gap and channel inversion. In the following expression, we used the first two terms from the Taylor series: $VG(\phi so) = VG(2\phi f) + \{dVG(2\phi f)/d\phi so\}(\phi so - 2\phi f)$. This leads to an expression for the gate-source voltage, VG, in the subthreshold region ($VG \leq VT$):

$$VG = VT + Mi(\phi so - 2\phi f) \tag{5.14}$$

where the n-MOSFET threshold voltage is:

$$VT = VG(2\phi f) = 2\phi f - Vot + Vit + \Gamma\sqrt{2\phi f - VB} \tag{5.15}$$

and where an intermediate value for M is

$$Mi = 1 + \frac{\Gamma}{2\sqrt{2\phi f - VB}} + \frac{Vit}{\phi f} \tag{5.16}$$

Note that Equation 5.15 is identical to Equation 5.1. The above VG expression, Equation 5.14, yields:

$$\phi so = 2\phi f + \frac{VG - VT}{Mi} \tag{5.17}$$

which shows how ϕso depends on VG and VB which is embedded in VT and Mi.

Now we are ready to evaluate the subthreshold current expression, IB, given in Equation 5.5. The $\ln IB$ Taylor series expansion about $VG = VT$ for VD and VB constant is

$$\ln IB = \ln IB\,|_{\phi so=2\phi f} + \frac{d\ln IB}{dVG}\,|_{\phi so=2\phi f}\,(VG - VT) \tag{5.18}$$

The logarithmic form of Equation 5.5 is

$$\ln IB = \ln\left(\frac{\beta\Gamma Vt^2}{2}\{1-\exp\left(-\frac{VD}{Vt}\right)\}\right) - \frac{1}{2}\ln\left(\phi so - VB\right) + \frac{\phi so - 2\phi f}{Vt} \quad (5.19)$$

and thus the terms in the Taylor series approximation are:

$$\ln IB\,|_{\phi so=2\phi f} = \ln\left(\frac{\beta\Gamma Vt^2}{2\sqrt{2\phi f - VB}}\right)\{1-\exp\left(-\frac{VD}{Vt}\right)\} \quad (5.20)$$

$$\frac{d\ln IB}{dVG}\,|_{\phi so=2\phi f} = \frac{1}{Mi\,Vt}\left(1-\frac{Vt}{2(2\phi f - VB)}\right) \quad (5.21)$$

where $d\phi so/dVG = 1/Mi$ was obtained from Equation 5.17. Thus

$$IB = IB0\exp\left(\frac{VG-VT}{M\times Vt}\right)\{1-\exp\left(-\frac{VD}{Vt}\right)\} \quad (5.22)$$

where

$$IB0 = \frac{\beta\Gamma Vt^2}{2\sqrt{2\phi f - VB}} \quad (5.23)$$

and where

$$M = \frac{Mi}{1-\frac{Vt}{2(2\phi f - VB)}} \quad (5.24)$$

The above expression for IB holds only for $VG \leq VT$. For $VG > VT$, IB, given by Equation 5.22, far exceeds the current drawn by the MOSFET in its active region. Thus the IB function must be terminated slightly inside the active region or a new function developed. In SPICE [27], IB is terminated for $VG \geq Von$. This ensures the continuity of current between the subthreshold and saturation regions but not the slope of the current-voltage curve. Other workers have suggested a new formula for IB which allows for continuity in the derivatives across the subthreshold-saturation region boundary. Antognetti et. al. [28] and Fung [29] suggest formulations that are equivalent to the following:

$$IB = \frac{F\times IB0(1-\exp\left(-\frac{VD}{Vt}\right))}{1+F\exp\left(\frac{-(VG-VT)}{M\times Vt}\right)} \quad (5.25)$$

where F is a factor that is either a fitting parameter [28] or estimated [29]. This function is very attractive. For $VG < VT$, IB is identical to Equation 5.22. For $VD > Vt$ and for $VG = VT$, $IB = (F\times IB0/(1+F))$. For $VD > Vt$ and for $VG > VT$, $IB = F\times IB0$. It is seen that for $VG > VT$ that $IB = F\times IB0$

when VG exceeds VT by a few Vt or 50 mV at room temperature. A difficulty arises when attempting to evaluate F. Numerous approaches were attempted with the most successful being one in which F was determined from an offset current found in the saturation region. However, the extraction procedure was not considered robust enough. Thus we have chosen to let $F = 1$ in the above equation and formulated the subthreshold current for all values of VG [30] as:

$$IB = \frac{IB0(1 - \exp(-\frac{VD}{Vt}))}{1 + \exp(\frac{-(VG-VT)}{M \times Vt})} \tag{5.26}$$

5.1.3 Parameter Extraction Algorithms

The expression for the subthreshold current given in Equation 5.22 is easily linearized by expressing it in logarithmic form:

$$\ln(\frac{IB}{1 - \exp(-\frac{VD}{Vt})}) = [\ln IB0] + [\frac{1}{M}]\frac{VG - VT}{Vt} \tag{5.27}$$

where the extracted parameters, $IB0$ and M, are shown inside the brackets.

In order to extract Vit, IB is measured at two values of VB, that is $VB = 0$ and -2.5 V. From Equations 5.16 and 5.24 the M-factor is expressed as:

$$M\{1 - \frac{1}{2}(\frac{Vt}{2\phi f - VB})\} = [M0] + \frac{[\Gamma m]}{2\sqrt{2\phi f - VB}} \tag{5.28}$$

where $M0 = 1 + Vit/\phi f$ so that

$$Vit = (M0 - 1)\phi f \tag{5.29}$$

In the above expression Γm has the same meaning as Γ derived from the active region analysis of a MOSFET. The "m" denotes that Γm is derived from the subthreshold region M factor. In practice, the values extracted for Γm are close to those extracted for Γ.

The extraction of Vot follows from Equation 5.2; that is, for an n-MOSFET:

$$Vot = 2\phi f + Vit - VTo \tag{5.30}$$

where Vit comes from Equation 5.29 and VTo comes from the active region threshold voltage.

For p-MOSFETs, Vot is derived from Equation 5.3; that is

$$Vot = VTo - 2\phi f - Vit \tag{5.31}$$

where again Vit comes from the subthreshold region and VTo from the active region threshold voltage.

Finally, the extraction of $\Gamma 0$ follows from the fitting of Equation 5.23:

$$IB0 = [\Gamma 0]\frac{\beta Vt^2}{2\sqrt{2\phi f - VB}} \tag{5.32}$$

where $\Gamma 0$ has the same physical meaning as the active region Γ. The "0" denotes that $\Gamma 0$ is derived from the $IB0$ expression. In practice, it is found that $\Gamma 0$ values differ significantly from Γ values. This is because $\Gamma 0$ was derived by approximating the width of the base of the bipolar transistor. Thus $\Gamma 0$ reflects the uncertainties in this approximation. In addition $\Gamma 0$ depends on the extraction of $IB0$ which in turn depends on the value of the threshold voltage extracted from the active region. Thus $\Gamma 0$ should be interpreted as a fitting factor with little physical significance.

5.1.4 Results

The results of fitting a set of four different sizes of MOSFETs are listed in Tables 5.1 to 5.3. These results were obtained using the JFETFIT parameter extractor [30] where the L and W dimensions for the MOSFETs are given in the L and W columns. In this extraction process the threshold voltages determined from the saturation region were used.

The parameters used to fit each MOSFET on an individual basis are listed in Table 5.1. These parameters are to be compared with the individual parameters listed in Table 5.2 which were determined from the global fit parameters listed in Table 5.3. By comparing the values in Tables 5.1 and 5.2, it is seen that the major parameters (e.g., VT and β) agree extremely well. In addition, the correlation coefficients, CC, indicate a tolerable degradation from the individual to the global fits. The three subthreshold parameters, Vit, Γm, and $\Gamma 0$, are listed in Table 5.3. Notice that $\Gamma m = 0.850\sqrt{V}$ agrees closely with $\Gamma = 0.831\sqrt{V}$ but as discussed earlier $\Gamma 0 = 11.13\sqrt{V}$ differs significantly from Γ. The density of interface states can be calculated from the equation given above as: $Nit = VitCo/q$. For $Co = \epsilon o/Xo$ where $Xo = 50\,\text{mn}$, and $\epsilon o = 3.9 \times 8.86 \times 10^{-14}\,\text{F/cm}$, $Nit = 8.2 \times 10^9\,(1/\text{cm}^2)$. The conversion formula is: $Nit\,(1/\text{cm}^2) = 2.16 \times 10^{13} \times Vit\,(V)/Xo\,(\text{nm})$.

The parameters for the MOSFET with $W(\mu\text{m})/L(\mu\text{m}) = 9/3$, listed in Table 5.1, were placed in the JFETFIT MOSFET model and used to examine the continuity of the derivatives of the drain current curves. The result is shown in Figures 5.7 and 5.8 where $IB0 = 1.067\,\mu\text{A}$, $VT = 0.700\,\text{V}$, and

Table 5.1: Individual MOSFET parameters based on individually fitting four MOSFETs. In this case, $2\phi f = 0.6\,\mathrm{V}$, $VTo = 0.075\,\mathrm{V}$, and $\Theta = 0.041$.

XT	L	W	VB	β	VT	δ	ϵ	λ	η	τ	R	CC
1	3	9	0.0	2.46×10^{-4}	0.701	0.38	0.335	0.038	1.58	0.070	78	0.9994
2	9	9	0.0	5.38×10^{-5}	0.706	0.49	0.014	0.011	0.49	0.050	78	0.9998
3	9	6	0.0	3.35×10^{-5}	0.699	0.48	0.012	0.011	0.44	0.047	125	0.9998
4	3	6	0.0	1.44×10^{-4}	0.700	0.40	0.288	0.035	1.39	0.065	125	0.9995
5	3	9	-2.5	2.46×10^{-4}	1.445	0.10	0.391	0.042	1.62	0.082	78	0.9993
6	9	9	-2.5	5.38×10^{-5}	1.518	0.26	0.053	0.011	0.62	0.046	78	0.9997
7	9	6	-2.5	3.35×10^{-5}	1.520	0.26	0.051	0.011	0.60	0.042	125	0.9997
8	3	6	-2.5	1.44×10^{-4}	1.461	0.15	0.336	0.038	1.51	0.074	125	0.9994

XT	L	W	VB	ν	IB0	M	Temp
1	3	9	0.0	-0.014	7.782×10^{-7}	1.770	300
2	9	9	0.0	-0.042	1.457×10^{-7}	1.796	300
3	9	6	0.0	-0.037	8.004×10^{-8}	1.857	300
4	3	6	0.0	-0.017	4.664×10^{-7}	1.797	300
5	3	9	-2.5	-0.012	4.593×10^{-7}	1.447	300
6	9	9	-2.5	-0.054	9.069×10^{-8}	1.539	300
7	9	6	-2.5	-0.048	7.730×10^{-8}	1.512	300
8	3	6	-2.5	-0.022	3.064×10^{-7}	1.473	300

Table 5.2: Individual MOSFET parameters derived from the global FET parameters given in Table 5.3. In this case, $2\phi f = 0.6\,\mathrm{V}$ and $VTo = 0.075\,\mathrm{V}$.

XT	L	W	VB	β	VT	δ	ϵ	λ	η	τ	R	CC
1	3	9	0.0	2.39×10^{-4}	0.702	0.37	0.338	0.039	1.52	0.067	50	0.9994
2	9	9	0.0	5.39×10^{-5}	0.704	0.48	0.032	0.012	0.54	0.049	50	0.9995
3	9	6	0.0	3.35×10^{-5}	0.700	0.51	0.032	0.010	0.54	0.049	81	0.9980
4	3	6	0.0	1.48×10^{-4}	0.698	0.40	0.338	0.038	1.52	0.067	81	0.9993
5	3	9	-2.5	2.39×10^{-4}	1.449	0.11	0.338	0.039	1.52	0.067	50	0.9990
6	9	9	-2.5	5.39×10^{-5}	1.514	0.22	0.032	0.012	0.54	0.049	50	0.9966
7	9	6	-2.5	3.35×10^{-5}	1.523	0.26	0.032	0.010	0.54	0.049	81	0.9990
8	3	6	-2.5	1.48×10^{-4}	1.457	0.15	0.338	0.038	1.52	0.067	81	0.9980

XT	L	W	VB	ν	IB0	M	Temp
1	3	9	0.0	-0.014	8.011×10^{-7}	1.766	300
2	9	9	0.0	-0.042	1.810×10^{-7}	1.766	300
3	9	6	0.0	-0.037	1.124×10^{-7}	1.766	300
4	3	6	0.0	-0.017	4.974×10^{-7}	1.766	300
5	3	9	-2.5	-0.012	3.524×10^{-7}	1.487	300
6	9	9	-2.5	-0.054	7.961×10^{-8}	1.487	300
7	9	6	-2.5	-0.048	4.943×10^{-8}	1.487	300
8	3	6	-2.5	-0.022	2.188×10^{-7}	1.487	300

Table 5.3: Global MOSFET parameters. The parameters which are indented are calculated; all other parameters are measured.

Transistor Parameter		Value	Standard ± Deviation ±	%
BETA:	KP($\mu A/V^2$)=μoCo	=	52.790 ± 1.668	(3.16%)
	ΔW(μm)	=	1.086 ± 0.211	(19.38%)
	ΔL(μm)	=	1.249 ± 0.071	(5.71%)
THRESHOLD:	VTf0(V)	=	0.711 ± 0.028	(3.89%)
	Vot(V)	=	0.604 ± 0.027	(4.39%)
	VTo(V)	=	0.077 ± 0.024	(31.35%)
	$\Gamma(\sqrt{V})$	=	0.819 ± 0.018	(2.16%)
	KLG(V × μm)	=	0.005 ± 0.012	(260.24%)
	KLGB(μm)	=	0.057 ± 0.007	(11.77%)
	KWG(V × μm)	=	-0.051 ± 0.068	(-134.17%)
	KWGB(V × μm)	=	0.065 ± 0.039	(59.42%)
DELTA:	D0($\sqrt{V}$)	=	0.355 ± 0.022	(6.09%)
	KLD(μm)	=	0.248 ± 0.039	(15.54%)
	KWD(μm)	=	0.422 ± 0.138	(32.75%)
TAU:	Θ(1/V)	=	0.043 ± 0.003	(6.25%)
	KLT(μm/V)	=	0.042 ± 0.007	(15.34%)
	RW(Ω × μm)	=	401.965 ± 62.943	(15.66%)
ETA:	H0(1/V)	=	0.251 ± 0.062	(24.68%)
	KLH(μm/V)	=	2.227 ± 0.150	(6.72%)
EPSILON:	E0(1/V)	=	0.057 ± 0.022	(39.38%)
	KLE(μm/V)	=	0.690 ± 0.054	(7.83%)
LAMBDA:	L0(1/V)	=	0.006 ± 0.003	(47.28%)
	KLL(μm/V)	=	0.062 ± 0.003	(4.52%)
	KWL(μm/V)	=	0.020 ± 0.016	(80.63%)
M:	M0(unitless)	=	1.267 ± 0.037	(2.94%)
	Vit(V)	=	0.080 ± 0.011	(13.94%)
	Γm($\sqrt{V}$)	=	0.772 ± 0.075	(9.68%)
IB0:	Γ0($\sqrt{V}$)	=	7.788 ± 0.424	(5.44%)

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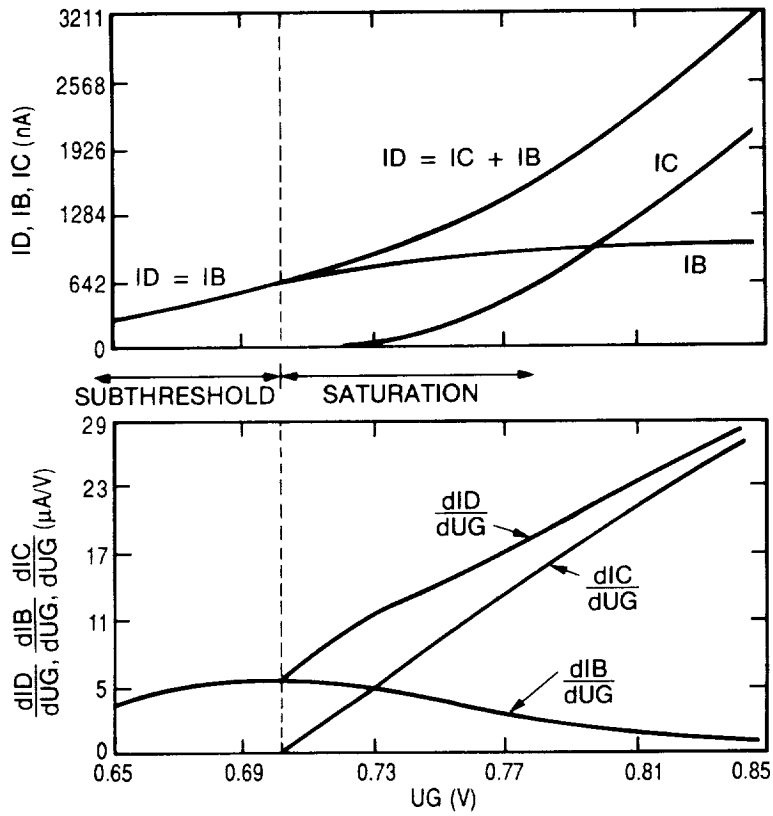


Figure 5.7: MOSFET drain characteristics for $VDS = 5\,\mathrm{V}$. This graph shows that the slope is continuous at the subthreshold-saturation boundary at $VGS = VT = 0.700\,\mathrm{V}$.

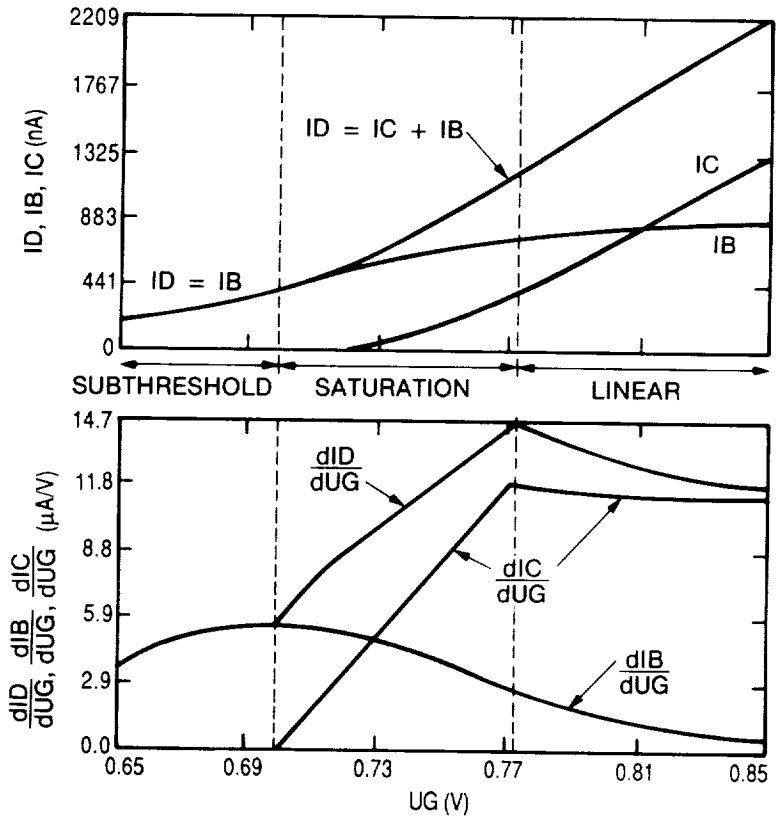


Figure 5.8: MOSFET drain characteristics for $VDS = 0.05$ V. This graph shows that the slope is continuous at the subthreshold-saturation and saturation-linear boundaries.

$ID = IB + IC$. As seen in Figure 5.7, where $VDS = 5\,\mathrm{V}$, the derivatives are continuous across the subthreshold-saturation boundary at $VT = 0.700\,\mathrm{V}$. As seen in Figure 5.8, where $VDS = 0.050\,\mathrm{V}$, the derivatives are continuous not only at the subthreshold-saturation boundary but also at the saturation-linear boundary. This shows that the JFETFIT MOSFET model maintains continuity in the derivatives at both the subthreshold-saturation and saturation-linear boundaries.

5.1.5 Conclusions

Simple expressions are presented for the extraction of the subthreshold current from MOSFETs. The expressions are derived from a bipolar model of the MOSFET operating in the subthreshold region. This region is characterized by the three parameters: Vit, Γm, and $\Gamma 0$. Using the interface trap potential, Vit and the oxide threshold voltage, VTo, derived from the active region allows the extraction of Vot, the oxide trap potential. An expression suitable for inclusion in SPICE-like simulations was given and it was shown that the derivatives of this function are continuous at the threshold voltage. Experimental data indicates that Γm values are close to Γ values but $\Gamma 0$ values differ significantly from Γ values where Γ is derived from the active region. Thus, Γm values serve as a double check of Γ and $\Gamma 0$ serves as a subthreshold fitting parameter.

5.2 Integrated Circuit Simulation on the Hypercube

5.2.1 Objectives

The objectives of this task were:

1. To determine the feasibility of transporting the SPICE circuit simulator (University of California, Berkeley) to the hypercube concurrent computers being constructed at JPL, rewriting code as necessary, to exploit concurrency in computation.

2. To understand the simulator and its algorithms, to gain insight into the distribution and decomposition of SPICE onto the JPL computers, and generally to acquire the expertise required to deal with the problem.

3. To begin development of a simulator providing easily incorporated device models, transistor-level simulation, and a programmable fault environment (for the introduction of simulated faults) using the SPICE transport as a starting point.

4. To execute benchmarks upon the new code for both correctness and speed.

The specific goals were:

1. To implement a subset of SPICE able to compute transient analyses for transistors, resistors, capacitors, and programmable current and voltage sources.

2. If succeeding in this, to begin to enhance the code with the other features.

5.2.2 Progress and Results

The subset of SPICE (mentioned in Section 5.2.1) has been completely implemented. To achieve this, the decomposition problem has been adequately solved, and programs written to accept standard SPICE decks, perform load balancing and communication routings, generate tables for downloading into the hypercube, and format output results for display. These ancillary codes are complete. The SPICE subset itself, executing on the cube, accepts these tables properly and is able to produce correct numerical results.

This effort terminated just as the benchmarking of large circuits commenced. At the end of the effort an unexplained fault caused simulations to "hang" randomly and, for this reason, no useful timing results could be acquired.

5.2.3 Significance of the Results

The transport of SPICE onto the hypercube was successful. Increase of memory resources, and identification of the unexplained fault, which is either an uninitialized memory error or an intermittent communication failure, should remove all remaining obstacles. The code has been sufficiently understood, as manifested in part by our modifying of SPICE 3 to execute a new MOSFET model, and in part by the successful transport to the cube. The decomposition and exploitation-of-concurrency issues are well understood, and we await only the appropriate machine resources to commence simulation and timing experiments on large circuits.

The most important result is that we have learned how to decompose the problem onto a hypercube of any dimension: the codes already written support any cube from 32 nodes to 1024 nodes.

The future development of SPICE on the hypercube (by inclusion of a programmable fault facility) is expected to assist in the modeling of single-event upsets of Random Access Memories (RAMs). The modeling of the memory response to heavy ion hits requires repetitive simulations in order to determine the upset point (critical charge). SPICE on the hypercube should speed up the process of both evaluating existing RAMs and designing new RAM cells that are more resistant to heavy ion upset.

To make this program a viable laboratory utility, the importance of ease of access between the laboratory's VAX computers (which generate the SPICE tables) and the hypercube (which executes the tables) cannot be understated. A form of the JPL MARK II batch scheduler and file server for the JPL MARK III cubes would be highly desirable for this application.

5.2.4 Personnel

We are grateful to the following members of the community at the California Institute of Technology: Sven Mattison and Charles Seitz (Computer Science) for foundational work on the problem, Geoffrey Fox and colleagues (Physics) for their assistance in the decomposition and load-balancing issues, Alain Martin (Computer Science) for assistance with the resulting intractable optimization problem, and James Okamoto (Physics) for SPICE code benchmarking.

5.2.5 Publications

The complete report, including computer codes, is being compiled as SPICE ON THE HYPERCUBE, JPL Internal Report, December 1986.

Chapter 6

A Test Chip Case Study

6.1 Introduction

This case study is an application of the methodology developed in the Product Assurance Technology Program for the qualification circuits fabricated at a silicon foundry. The study consists of an analysis of 3-μm, CMOS/bulk, p-Well, single metal, single poly wafers from a foundry run for the CRRES Chip project. The CRRES Chip geometry (CIF) files were submitted to VLSI Technology Inc. (VTI) for fabrication. Four wafers from Lot Number 4236-0000C4, Run A366 were returned to JPL for testing and qualification, and were code-named "VTI-2." These wafers were numbered 1 (broken on left), 4, 5, and 10.

Over 110 CRRES chips were fabricated on each wafer in a grid 13 chips wide at the diameter of the wafer. The wafer is shown in Figures 6.1 and 6.2. The chips on these wafers are identified by 13 rows and 13 columns, where location row 1, column 1 is at the lower left-hand corner of the wafer. Each chip is 7130 (horizontal) by 7025 (vertical) micrometers, measured center to center on the uncut wafers. In wafer number 1, columns 1 and 2 are missing.

Two test vehicles were included on this run: the first, a Test Strip containing a small number of selected test structures, was placed on each of the CRRES chips (over 100 sites). The second, a Test Chip of the same area as the CRRES chip and containing a large number of test structures, was placed in a regular 3×3 matrix within the "prime site," i.e., the central section, of each wafer. Each Test Chip was separated from the others by 3 wafer sites.

The purpose was to compare results obtained from measurements of Test Strips with those of Test Chips to determine the area required for test structures on a wafer. It was expected that Test Chips might be adequate to characterize the wafer for certain parameters but Test Strips, which provide much more wafer coverage, might be necessary for other parameters.

Section 6.11 contains a full set of wafer maps from wafer #10.

6.2 Areas of Investigation

Each wafer contained over 100 production chips, each bearing a Test Strip. At the same time there were 9 dedicated Test Chips on each wafer. Among the issues explored during the preparation of the Test Chips and Strips, and during the data acquisition and its subsequent analysis, were the following:

1. The first issue was to determine how frequently a parameter needed to be sampled across a wafer. Comparisons between data from the Test Chips

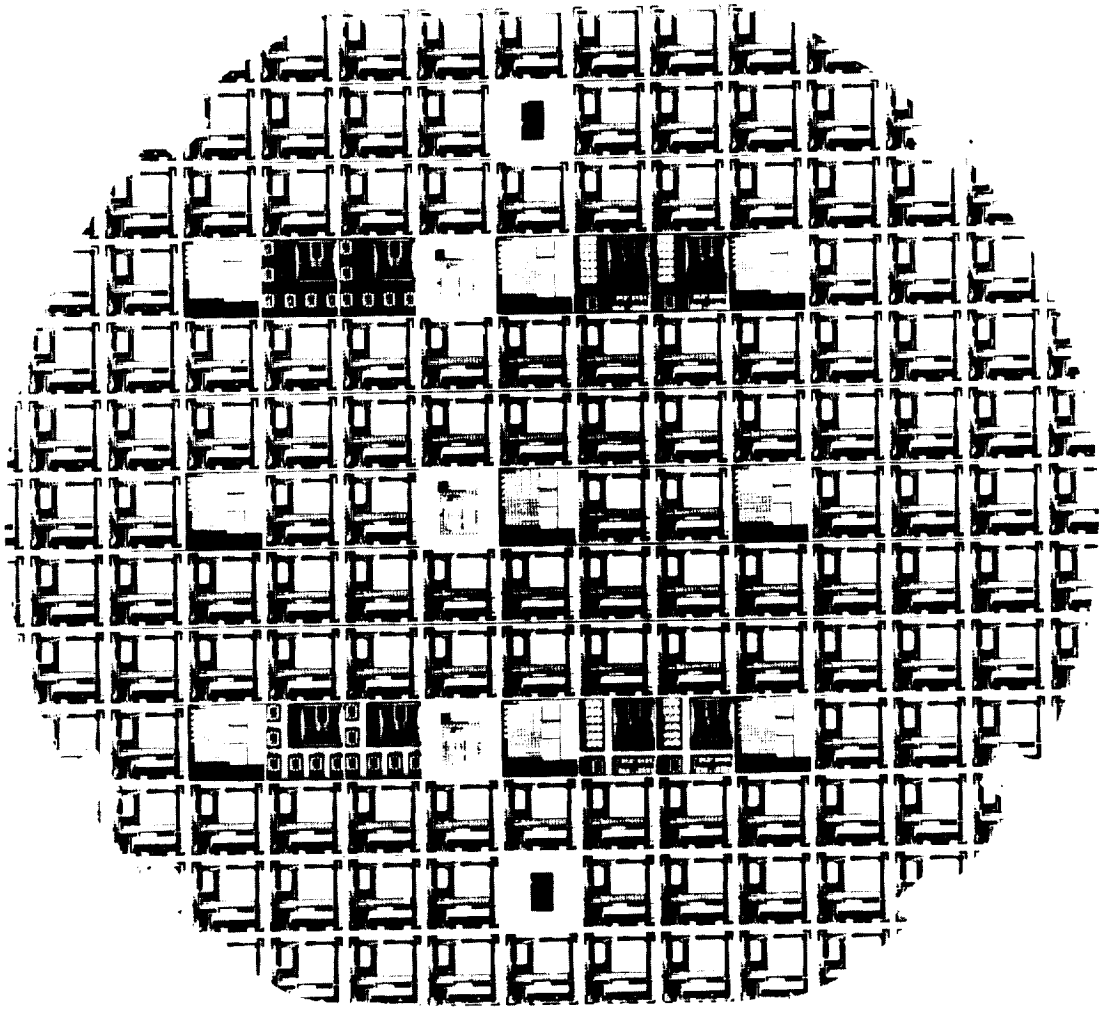
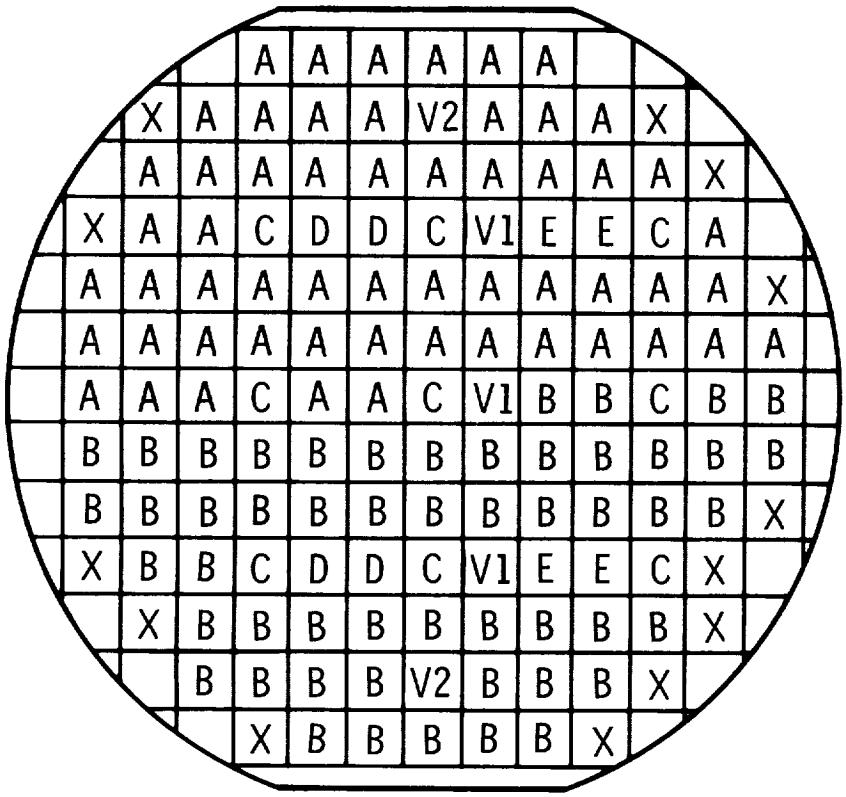


Figure 6.1: Four-inch diameter silicon wafer from run VTI-2.



CHIPS INCLUDED	LOCATION
CRRES CHIP - 1K RAM	A
CRRES CHIP - 1K RAM (SPECIAL)	B
JPL DROP-IN CM5111/STS 102	C
KELVIN TAPPED TRANSISTOR ARRAY (N-TYPE)	D
KELVIN TAPPED TRANSISTOR ARRAY (P-TYPE)	E
4007 TYPE CHIP	(D, E)
PAD TEST CHIPS (3)	(D)
VENDOR DROP IN	V1, V2
INCOMPLETE DIE	X

Figure 6.2: Map of the VTI-2 wafer shown in Figure 6.1 where the different types of chips are indicated in the key.

and Test Strips for different parameters helped to determine the degree of wafer coverage required.

2. A second issue was whether the nine sites were sufficient to fit a surface which conveyed "sufficient" detail (wafer mapping), and if so, for which parameters. Therefore, a quantitative comparison was made between the surface fitted from the many Test Strips and the surface fitted from the nine Test Chips.

3. The issue of determining which points were statistical outliers, and how to identify them, was also approached using two different techniques:

   (a) The first technique was applied to the Test Strip data and involved two passes over the data: the first pass combined corresponding data from all wafers to plot global histograms (for this procedure to be accurate, the wafers must be similar enough to be considered samplings from the same population and no wafer can depart pathologically from the population). From these global histograms, the criteria for exclusions (identification and elimination of outliers) for the second pass were determined. The second pass applied these exclusion windows to the individual wafers.

   (b) The second exclusion technique was applied to the Test Chip data. In this case, exclusions were made to data from each wafer independently. The resulting distributions were used to create the lot summary data using no further exclusions. In effect, decisions on exclusions were made on each wafer in isolation from the others, and the results were subsequently combined. We were curious to know if the results would be realistic, and what clues would become manifest when this method was inadequate. This involved a comparison of the summary results for the two methods. The reason for seeking the validity of the latter technique is due to the severe data management problems of the first technique.

4. The final issue concerned correlations between test structure data and certain functional circuits on the production chips. Examples of the test structure data are transistor thresholds, KP, etc., compared with the results of functional circuits such as a RAM or the timing sampler described elsewhere (Chapter 7) in this report.

6.3 Test Chip and Test Strip Design

As used in this report, the nine Test Chips are chips fully dedicated to test structures; therefore, only a few Test Chips can be included on a production wafer. The Test Chips on this run consumed about 8 percent of the available chip positions, and occupied nine "prime sites" on the wafer.

Test Strips have much smaller dimensions than Test Chips, limiting the number of test structures that can be placed on each strip. However, the Test Strip is replicated on every site on the wafer that contains a production chip. In this run, the Test Strip consumes approximately 5 percent of the area of the production chip and thus about 5 percent of the total area of the wafer.

Test structures for the Test Chips were selected from the following categories:

1. Process parameter extraction.
2. Device parameter extraction.
3. Circuit parameter extraction.
4. Layout rule checking.
5. Yield analysis.

The size of the Test Chip allows structures from all categories to be included; the smaller size of the Test Strip allows selected structures from only the first three categories to be included.

To satisfy the requirements of parameter extraction routines for circuit simulators, transistors of various sizes are included on the Test Chips. Dimensions for both n- and p-channel transistors included on this run, along with the calculated KP for each size, are shown in Table 6.1. These values were derived from the maximum slope, β, of the ID versus VG curve for $VD = 50$ mV using $KP = \beta L/W$ where L and W are the as-drawn channel length and width dimensions, respectively. The KP values shown in Table 6.1 are not corrected for ΔL and ΔW.

6.4 Geometry and Test Program Generation

Once the decisions on the contents of the Test Chip and the Test Strip had been made, the JPL Test Chip Assembler (TCA) was used to generate the geometry. The Test Chips were identified as CM5111, and the Test Strips as ST5102. The

Table 6.1: Transistor Geometries for both n- and p-channel transistors from Run VTI-2, 3-μm CMOS/Bulk p-well, W vs. L, showing KP in $\mu A/V^2$ ($mean \pm \sigma$ at $VBS = 0$) for each Device. The data shown is from wafers 1, 4, 5, and 10.

		As-Drawn Length (μm)					
		2.0	3.0	6.0	9.0	12.0	15.0
n-Channel	15.0		56.7	49.0	46.5	45.2	44.7
Transistors			±2.7	±1.5	±1.4	±1.1	±0.8
	12.0		55.7				
As-Drawn			±3.3				
Width	9.0	103.	54.6		44.5		
(μm)		±12.	±3.5		±0.9		
	6.0		49.9		44.4		
			±3.4		±1.1		
	4.5	81.7	47.6	43.8	41.6		40.6
		±9.2	±3.3	±1.3	±1.3		±1.3
	3.0	77.2	44.6		38.4		
		±8.7	±2.6		±1.9		
p-Channel	15.0		−.809	−.827	−.831	−.837	−.836
Transistors			±.027	±.018	±.017	±.022	±.024
	12.0		−.807				
As-Drawn			±.023				
Width	9.0	−.637	−.811		−.846		−.844
(μm)		±.028	±.025		±.023		±.017
	6.0		−.829		−.858		
			±.021		±.019		
	4.5	−.688	−.836	−.860	−.866		−.872
		±.029	±.020	±.019	±.019		±.016
	3.0	−.717	−.854		−.888		
		±.026	±.021		±.017		

two projects were laid out independently. Using a text input file containing gross-level specifications of the required structures and placement, the TCA generated all detailed geometry automatically. The result was an output file in Caltech Intermediate Form (CIF) which was sent directly to the foundry for fabrication (in the case of the Test Chip CM5111), or else merged into the geometry for the CRRES Chip project (in the case of the Test Strip ST5102).

In addition to producing geometry files in CIF, the TCA produced description files which state the exact locations of the structures in the project, the type of structure, and the essential parameters of each structure. These files were routed to the Test Program Generator, which automatically prepared a test program to be executed by the prober and the test instrumentation. The compilation of a test program on a VAX 11/780 takes about ten minutes. Two separate wafer probing programs were generated: one to test the Test Strips and one to test the Test Chips.

6.5 Wafer Probing and Disposition of Data

The VTI-2 wafers were probed using JPL's test system which, at the time, was built around an LSI-11 computer. Since this system has been replaced by a microVAX-II system, no machine-dependent details of the test software will be given. The test system was designed to execute test programs generated for it following the steps outlined above. Thus, the electrical test and the position of the wafer prober were automatically programmed by the earlier steps.

This study used four wafers, numbered 1, 4, 5, and 10. Wafer 1 had the leftmost two columns (of the 13×13 grid) missing.

The output from the wafer probing was a binary, sequential file which was moved to a VAX 11/780 computer for final formatting. On the VAX, the file was processed by a program called the Test Data Preprocessor, to organize the raw data into labeled, archival, data files. Once this is complete, the binary file is discarded.

The result is a series of small ASCII files written in a format called CRUNCH reference files. Each CRUNCH file, which contains all data from all chips for one particular structure, has an identifier incorporated into its name which is uniquely assigned to this structure by the Test Compiler. For example, had there been a transistor (of given dimensions), called "349" by the test compiler, drawn into the Test Chip, then one CRUNCH file for each wafer would have been generated, each with the characters "349" as part of its filename. Since the Test Chip appears nine times on each wafer, then one such CRUNCH file

would contain nine points. Each of the nine points is labeled in such a way that the exact coordinates of each site, on the wafer, are known. Thus, one CRUNCH file contains enough data to fit a surface for a wafer map.

The test data preprocessor, furthermore, labels the data in each CRUNCH file with information it obtains from the "description file" output of the TCA. Therefore, the labeling of the output data, and the construction of the CRUNCH files, is fully automatic.

Each CRUNCH filename incorporates information to identify the wafer number and whether it was taken from the Test Strip or Test Chip. This filename structure allowed algorithmic file construction and automated access to files. This is essential to automating the analysis of the (formatted but as-measured) data in the CRUNCH files, by the main analysis tool, a program called STMJPL which was derived from the National Bureau of Standards statistical analysis program STATII [31].

6.6 Test Strip Wafer Map Preliminary Results

The STMJPL program generates wafer maps of the important parameters and structures on the Test Strips. The exclusions applied to the data were determined by studying the global histograms to decide which points would be considered "outliers." In this case, the histogram data was normally distributed, indicating to a first approximation that no one wafer was significantly different from the others. Two histograms from this run are shown: the first is the distribution of contact resistance for metal to n+poly (Table 6.2), an example of normally distributed data, and the second is the sheet resistance of the metal layer (Table 6.3), showing a skewed distribution. Wafer maps were generated for individual wafers. A map of contact resistance to n+poly is shown, once in "full" mode (Table 6.4) and the second time in "avenue" mode (Table 6.5).

6.7 Parametric Test Structure Probing: Initial Qualitative Results Test Strip ST5102

From the entire series of wafer maps and the statistics printed with each plot, a preliminary summary was prepared. This is not the result of a full statistical analysis on the data, but rather a tabulation of information obtained from the wafer maps. The data referred to in this section is listed in Table 6.6.

1. Sheet Resistance from Split-Cross-Bridge Resistors:

Table 6.2: Histogram of the normal distribution of contact resistance for metal to n+poly on the Test Strips of Run VTI2, Wafer #1. Mean = 2.11 Ω; Stdev = 0.43Ω; % Stdev = 20.69; Median = 2.15 Ω; Minimum = 0.73 Ω; Maximum = 3.23 Ω.

INTERVAL MIDPOINT (OHMS)		NO. OBS.	NUMBER OF OBSERVATIONS 0 10 20 30 40
0.767		1	*
0.841		2	**
0.915		2	**
0.988		0	
1.06		4	****
1.14		3	***
1.21		2	**
1.28		8	********
1.36		8	********
1.43		6	******
1.51		8	********
1.58		7	*******
1.65	-	13	*************
1.73		16	****************
1.80		14	**************
1.87		21	*********************
1.95		26	**************************
2.02		31	*******************************
2.10	>	32	********************************
2.17		29	*****************************
2.24		34	**********************************
2.32		30	******************************
2.39		22	**********************
2.46		26	**************************
2.54	+	14	**************
2.61		14	**************
2.69		15	***************
2.76		10	**********
2.83		6	******
2.91		5	*****
2.98		5	*****
3.06		2	**
3.13		1	*
3.20		1	*

INCLUDED = 418; EXCLUDED = 0
LOWER BOUND = 0.73; UPPER BOUND = 3.23; BIN COUNT = 34
POINTS BELOW BIN 1 = 0; POINTS ABOVE BIN 34 = 0; BIN WIDTH = 0.0738

Table 6.3: Histogram of the skewed distribution of sheet resistance of the metal layer from the Split-Cross-Bridge Resistor on the Test Strips of Run VTI2, Wafer #1. Mean = 0.033Ω/□; Stdev = 10^{-3}Ω/□; % Stdev = 3.15; Median = 0.0316Ω/□; Minimum = 0.0305Ω/□; Maximum = 0.0357Ω/□.

INTERVAL MIDPOINT (RSHEET)		NO. OBS.	NUMBER OF OBSERVATIONS 0 10 20 30 40
0.0306		3	***
0.0307		9	*********
0.0309	-	18	******************
0.0310		34	**********************************
0.0312		41	***
0.0314		39	**************************************
0.0315		47	**
0.0317		43	***
0.0318		31	*******************************
0.0320	>	23	************************
0.0321		17	*****************
0.0323		8	********
0.0324		7	*******
0.0326		11	***********
0.0328		2	**
0.0329	+	9	*********
0.0331		9	*********
0.0332		9	*********
0.0334		4	****
0.0335		9	*********
0.0337		3	***
0.0339		6	******
0.0340		3	***
0.0342		5	*****
0.0343		4	****
0.0345		4	****
0.0346		1	*
0.0348		0	
0.0349		4	****
0.0351		0	
0.0353		2	**
0.0354		0	
0.0356		1	*
0.0357		2	**

INCLUDED = 408; EXCLUDED = 10
LOWER BOUND = 0.0305; UPPER BOUND = 0.0358; BIN COUNT = 34
POINTS BELOW BIN 1 = 0; POINTS ABOVE BIN 34 = 0; BIN WIDTH = 1.56×10^{-4}

Table 6.4: "Full" Wafer Map of Contact Resistance to n+Poly Wafer #1. Mean = 2.40 Ω, Stdev = 0.318 Ω, % Stdev = 13.3, Median = 2.36 Ω, Minimum = 1.69 Ω, Maximum = 3.24 Ω.

```
VTI200860.C01 CMOS VTI2: VTI DEV.4236-0000C4 RUN A366 3U CMOS/BULK
(VTI2 )( 1)(ST5102)860,870,880,0
21-JUN-1986 22:56:18.00 - ST5102: TEST STRIP - CONTACT RESISTOR

          INCLUDED= 95 EXCLUDED= 0 NON-POINTS= 13 N= 1.00
           >< >< >< >< >< >< >< >< >< >< >< ><
                    78998887776668899
13   v             87#77#88#87#76#67#77653
                  ++875667788887766666554332                  ^
12   v           ++#87#56#78#88777#66#65#44322
                 +9888877777888887777777665544333             ^
11   v          +988#88#88#88#88#88#88#76#55#5556
                +++99888899899988888877765666555566           ^
10   v         ++9988#8778999999988887554566666#666
               12345566676788899988877654456666665555         ^
 9   v        -123455#66#67#77#77#77#76#56#66#65#5555
               455566667777666666666667776656666555544        ^
 8   v        2345566#77#76#55#55#56#67#76#56#55#44#4
               ----13456676655555545666777655555555443        ^
 7   v        ---0134#66666#56#5555677#66#54455#44#3
               88777777778765577766666665555433454433         ^
 6   v        +++9987#77#76#56#77#66#66#55#54#45#44#3
               +++9888776666556677776566666665545555433       ^
 5   v        9988877#65#55#56#67#76#56#76#65#55#4332
               55566666655566666788755677777655543 32         ^
 4   v          55666#677667788767776677788765443 32
                666677787778888777777777777544332             ^
 3   v            666#77#77#78#88#77#66#66#65#432
                  66666667778888888875555655443               ^
 2   v             6#66#66#67#88888#76#55#5554
                     55544556666666556555555                  ^
 1                      33#44#55#55#55#55
                >< >< >< >< >< >< >< >< >< >< >< ><
               1    3    5    7    9   11   13
                 2    4    6    8   10   12
```

-: less than 0.73 3: 1.48 to 1.73 7: 2.49 to 2.74
0: 0.73 to 0.98 4: 1.73 to 1.99 8: 2.74 to 2.99
1: 0.98 to 1.23 5: 1.99 to 2.24 9: 2.99 to 3.24
2: 1.23 to 1.48 6: 2.24 to 2.49 +: 3.24 or greater

Table 6.5: "Avenue" Wafer Map of contact resistance to n+Poly for Wafer #1. Mean = 2.40 Ω, Stdev = 0.318 Ω, % Stdev = 13.3 Ω, Median = 2.36 Ω, Minimum = 1.69 Ω, Maximum = 3.24 Ω.

VTI200860.C01 CMOS VTI2: VTI DEV.4236-0000C4 RUN A366 3U CMOS/BULK
(VTI2)(1)(ST5102)860,870,880,0
21-JUN-1986 22:56:18.00 - ST5102: TEST STRIP - CONTACT RESISTOR
Array = OHMS CP C n+POLY 3.00000

INCLUDED= 95 EXCLUDED= 0 NON-POINTS= 13 N= 1.00

```
                  >< >< >< >< >< >< >< >< >< >< >< >< >< 
                              .8..888...66688..
13          v                   8....88888...666....6..
                              ..8..66..8888..666666..4..2
12          v                 ...8.6.66.8888...66666..44.22
                              ..8888.....88888......66..44...
11          v                ..88888888.888888888888.66......6
                              .....8888..8...888888...6.666....66
10          v                ....8888..8.......8888...4.666666.666
                             .2.4..666.6.888...888..6.44.666666.....
9           v                ..2.4..66666............6..666666......
                             4...6666....666666666666...66.666....44
8           v                2.4..666..8.6........666...6..66...4444
                              ......4.66.66......4.666...6........44.
7           v                ...0..4.66666..66....66...66..44...444.
                             88........8.6.....6666666.....4..4.44..
6           v                .....8......6..6...666666.....444..44..
                              ....888..6666..66....6.666666..4....4..
5           v                ..888...6......666.8.6..6..666.....4..2
                              ...666666...66666.88...6.....6...4..2
4           v                  ..66666..66..88.6...66...88.6.44..2
                              6666...8...8888.............44..2
3           v                   6666.......8888....6666666.44.2
                               6666666...88888888.....6..44.
2           v                    666666666..88888..6.......4
                                   ...44..6666666..6......
1                                  ...44.......4.....
                             >< >< >< >< >< >< >< >< >< >< >< >< >< 
                            1     3     5     7     9     11    13
                               2     4     6     8     10    12
```

-: less than 0.73 3: 1.48 to 1.73 7: 2.49 to 2.74
0: 0.73 to 0.98 4: 1.73 to 1.99 8: 2.74 to 2.99
1: 0.98 to 1.23 5: 1.99 to 2.24 9: 2.99 to 3.24
2: 1.23 to 1.48 6: 2.24 to 2.49 +: 3.24 or greater

(a) $R_{sp,DIFF}$ (p+diffusion): Combining all points (415) from all wafers, the mean is $87.2 \pm 1.9\,\Omega/\square$. Individual wafer statistics match combined statistics very closely. On all wafers the sheet resistance increased linearly from the bottom to the top of the wafer.

(b) $R_{sn,POLY}$ (n+poly): Combining all points (419) from all wafers, the mean is $22.5 \pm 0.67\,\Omega/\square$. Individual wafer statistics match combined statistics very closely; only wafer #5 shows slightly higher ($0.2\,\Omega/\square$) sheet resistance overall. All wafer maps show uniform sheet resistance except on the periphery of the wafer, where, for a very short distance (1 to 2 chips) from the edges, higher sheet resistance is found. In column 13 it is about $2\,\Omega/\square$ higher than on the rest of the wafer.

(c) $R_{sn,DIFF}$ (n+diffusion): First, it should be noted that the n+diffusion layer showed a bimodal distribution in sheet resistance. For all four wafers, row 13 had sheet resistance greater than the rest of the wafer by $20 - 25\,\Omega/\square$. The effect is very abrupt, affecting all chips on only that row. Therefore, the top row was excluded from the analysis and contains chips that probably should not be used. A corresponding effect also appeared in the n-channel transistor and the inverter maps; all n-channel transistors and inverters on the top row were excluded as outliers. Combining all points (395) from all wafers, the mean is $21.8 \pm 1.3\,\Omega/\square$. The distribution is skewed downwards, that is, the "tail" is toward low resistance values. The mode appears to be at about $23\,\Omega$. Individual wafers have statistics which match the combined statistics very closely, with no wafer-to-wafer shifts, and the skewed behavior appearing in all four wafers. The wafer maps all show fairly uniform sheet resistance except on the periphery of the wafer. On all four wafers there is a crescent-shaped region centered to the right along the periphery where the resistance is lower than on the rest of the wafer. The crescent at its thickest is about 2 chips distance across. The effect appears on all four wafers. The area not part of the crescent, which is a circular area within the crescent with its center point to the left of the wafer center, has very uniform sheet resistance at the mode value (approx. $23\,\Omega/\square$).

(d) $R_{s,METAL}$ (Metal): Combining all points (408), from all wafers, the mean is $0.0320 \pm 0.0010\,\Omega/\square$. The distribution is skewed upwards, that is, the "tail" is toward high resistance values. The mode appears to be at about $0.0315\,\Omega/\square$. Statistics from individual wafers match the combined statistics very closely, the skewed behavior appearing

in all four wafers. All four wafer maps show fairly uniform sheet resistance except on the periphery of the wafer, where higher sheet resistance is found. The area of higher resistance is an annulus about 1 chip across.

2. Contact resistance:

   (a) $R_{\text{cmn,POLY}}$ (Metal to n+poly): Combining all points (418) from all wafers, the mean value is $2.12 \pm 0.44\,\Omega$. The distribution is normal. Individual wafers have similar statistics, with wafer #1 slightly higher (mean about $2.38\,\Omega$) and wafer #4 slightly lower (mean about $1.72\,\Omega$). There was no common trend in the individual wafer maps except for a pattern of the rightmost side of each wafer, one or two chips wide, having the lower contact resistances on each wafer.

   (b) $R_{\text{cmp,DIFF}}$ (Metal to p+diffusion): Combining all points (399) from all wafers, the mean value is $15.0 \pm 3.4\,\Omega$. The distribution is normal. Individual wafers have similar statistics, with wafer #1 slightly higher (mean about $16.6\,\Omega$) and wafer #4 slightly lower (mean about $13.2\,\Omega$). This follows the pattern for metal-n+poly contacts stated above. All four wafers showed the common trend of having the lowest contact resistances on the right side of the wafer, and increasing linearly as one moves left across the wafer. The effect is much more prominent than for the metal to n+poly contacts listed above.

   (c) $R_{\text{cmn,DIFF}}$ (Metal to n+diffusion): Combining all points (392) from all wafers, the mean value is $5.13 \pm 1.3\,\Omega$. The distribution is normal. Individual wafers have similar statistics, with wafer #4 lower (mean about $4.78\,\Omega$). All four wafers showed the common trend of having the lowest contact resistances on the right side of the wafer, in a crescent pattern the width of two chips at its thickest point. The remaining circular region (with its center left of wafer center) has, within itself, resistances going linearly from intermediate to high values as one moves across that circular region from right to left.

   (d) General comments on all contact wafer maps: The surfaces were consistently irregular, except for the overall trends noted above. High values tended to form a mesh of ridges while relatively lower values formed valleys. As seen from the standard deviation figures above, the difference in resistance moving from a ridge into a valley could be several ohms. Valleys were about three or four chips in diameter.

Table 6.6: Test Strip ST5102 results. Parametric data was taken from four 4-inch diameter CMOS/bulk wafers each containing 108 Test Strips and 9 drop-in Test Chips. The parameters from the Test Strips and Test Chips were fitted to over 3700 pixels and compared pixel by pixel to compute the parameter percent difference using 100 × (Chip − Strip)/(Strip). The data mean and standard deviations were computed after outlier exclusion.

DATA KEY: (# STRIPS VS # CHIPS)
(MEAN %DIF +- ST DEV. %DIF)
(STRIP MEAN +- STRIP STDEV)
(CHIP MEAN +- CHIP STDEV)

TEST STRUCTURE PARAMETER	WAFER 1	WAFER 4	WAFER 5	WAFER 10	LOT SUMMARY
BRIDGE R	89 vs 8	102 vs 7	102 vs 7	102 vs 8	395 vs 30
SHEET R	3.69 +- 7.52	4.01 +- 6.92	3.41 +- 7.03	4.26 +- 6.79	NOT APPLICABLE
Rsn DIFF	21.8 +- 1.40	21.8 +- 1.31	21.9 +- 1.32	21.9 +- 1.36	21.8 +- 1.34
(ohm/sq)	22.5 +- 0.80	22.5 +- 0.81	22.4 +- 0.79	22.5 +- 0.75	22.5 +- 0.75
BRIDGE R	89 vs 7	101 vs 6	102 vs 6	102 vs 7	394 vs 26
LINEWIDTH	-0.34 +- 1.87	-0.42 +- 1.34	-0.24 +- 1.76	-0.80 +- 1.80	NOT APPLICABLE
Wn DIFF	4.59 +- 0.07	4.78 +- 0.08	4.60 +- 0.05	4.58 +- 0.05	4.64 +- 0.11
(um)	4.57 +- 0.04	4.78 +- 0.05	4.60 +- 0.02	4.56 +- 0.02	4.62 +- 0.09
BRIDGE R	94 vs 8	107 vs 7	107 vs 8	107 vs 8	415 vs 31
SHEET R	-0.38 +- 0.69	-0.10 +- 1.00	-0.91 +- 1.64	-0.40 +- 0.81	NOT APPLICABLE
Rsp DIFF	87.3 +- 1.91	86.9 +- 1.86	87.2 +- 1.87	87.2 +- 2.02	87.2 +- 1.92
(ohm/sq)	86.7 +- 1.49	86.6 +- 1.68	86.1 +- 2.18	86.7 +- 1.52	86.6 +- 1.67
BRIDGE R	94 vs 7	104 vs 7	107 vs 5	107 vs 8	412 vs 27
LINEWIDTH	-0.25 +- 1.76	-0.67 +- 2.52	0.05 +- 2.16	-1.20 +- 1.97	NOT APPLICABLE
Wp DIFF	4.33 +- 0.10	4.49 +- 0.09	4.31 +- 0.07	4.28 +- 0.08	4.35 +- 0.12
(um)	4.31 +- 0.03	4.47 +- 0.04	4.30 +- 0.03	4.23 +- 0.03	4.33 +- 0.10
BRIDGE R	95 vs 8	108 vs 7	108 vs 7	108 vs 9	419 vs 31
SHEET R	-0.74 +- 6.41	1.08 +- 2.93	0.72 +- 3.32	-2.07 +- 3.52	NOT APPLICABLE
Rsn POLY	22.3 +- 0.68	22.5 +- 0.69	22.8 +- 0.65	22.4 +- 0.06	22.5 +- 0.67
(ohm/sq)	22.0 +- 0.36	22.4 +- 0.78	22.7 +- 0.60	21.8 +- 0.55	22.2 +- 0.65
BRIDGE R	94 vs 6	107 vs 7	108 vs 6	108 vs 7	416 vs 26
LINEWIDTH	4.73 +- 19.9	4.17 +- 5.14	4.86 +- 6.43	1.41 +- 4.22	NOT APPLICABLE
Wn POLY	2.62 +- 0.17	2.54 +- 0.11	2.54 +- 0.10	2.63 +- 0.10	2.59 +- 0.18
(um)	2.68 +- 0.06	2.60 +- 0.10	2.63 +- 0.05	2.65 +- 0.08	2.64 +- 0.08
BRIDGE R	95 vs 8	97 vs 7	108 vs 7	108 vs 8	408 vs 30
SHEET R	-1.77 +- 3.70	-2.37 +- 4.10	-2.88 +- 3.59	-2.68 +- 4.03	NOT APPLICABLE
Rs METAL	31.9 +- 1.05	31.9 +- 1.08	32.0 +- 1.00	32.0 +- 1.00	31.9 +- 1.01
(mohm/sq)	31.6 +- 1.00	31.4 +- 1.00	31.3 +- 1.00	31.5 +- 1.00	31.5 +- 1.00
BRIDGE R	94 vs 7	97 vs 7	108 vs 6	108 vs 7	407 vs 27
LINEWIDTH	-0.64 +- 2.58	-2.28 +- 3.13	-1.17 +- 3.28	-1.96 +- 3.47	NOT APPLICABLE
W METAL	3.79 +- 0.15	3.72 +- 0.13	3.75 +- 0.12	3.87 +- 0.19	3.78 +- 0.16
(um)	3.73 +- 0.10	3.64 +- 0.10	3.68 +- 0.15	3.80 +- 0.15	3.71 +- 0.14
CONTACT R	89 vs 9	99 vs 8	102 vs 9	102 vs 9	392 vs 35
CONTACT R	5.46 +- 26.6	13.1 +- 31.0	13.5 +- 30.3	15.6 +- 43.9	NOT APPLICABLE
Rcmn DIFF	5.30 +- 1.12	4.78 +- 1.19	5.24 +- 1.19	5.19 +- 1.43	5.13 +- 1.25
(ohm)	5.67 +- 1.25	4.94 +- 1.26	5.27 +- 1.03	5.41 +- 1.44	5.33 +- 1.22

Table 6.6: Test Strip ST5102 results (Continued).

TEST STRUCTURE PARAMETER	WAFER 1	WAFER 4	WAFER 5	WAFER 10	LOT SUMMARY
CONTACT R	94 vs 8	91 vs 8	107 vs 8	107 vs 9	399 vs 33
CONTACT R	-0.97 +- 14.7	-0.91 +- 14.9	0.41 +- 9.76	0.78 +- 16.4	NOT APPLICABLE
Rcmp DIFF	16.7 +- 3.41	13.2 +- 3.03	15.2 +- 2.59	14.8 +- 3.74	15.0 +- 3.42
(ohm)	16.4 +- 3.16	12.7 +- 2.71	15.0 +- 2.83	14.0 +- 3.49	14.5 +- 3.24
CONTACT R	95 vs 7	107 vs 9	108 vs 9	108 vs 9	418 vs 34
CONTACT R	-4.16 +- 13.9	6.14 +- 31.0	15.3 +- 23.4	7.35 +- 18.0	NOT APPLICABLE
Rcmn POLY	2.40 +- 0.32	1.73 +- 0.41	2.16 +- 0.28	2.22 +- 0.43	2.12 +- 0.44
(ohm)	2.31 +- 0.32	1.70 +- 0.34	2.27 +- 0.26	2.25 +- 0.42	2.12 +- 0.42
N-MOSFET	89 vs 8	102 vs 8	102 vs 9	102 vs 9	395 vs 34
THRESHOLD	-1.18 +- 1.59	-0.60 +- 1.18	-.094 +- 2.51	-0.41 +- 1.61	NOT APPLICABLE
VTOn	0.674 +- 0.008	0.655 +- 0.012	0.668 +- 0.013	0.680 +- 0.009	0.669 +- 0.014
(V)	0.670 +- 0.011	0.653 +- 0.007	0.670 +- 0.008	0.678 +- .007	0.668 +- 0.012
N-MOSFET	89 vs 8	102 vs 8	102 vs 9	102 vs 9	395 vs 34
CONDUCTANCE	1.36 +- 5.06	-0.05 +- 6.41	-2.52 +- 6.82	1.61 +- 5.52	NOT APPLICABLE
KPn=uCo	53.2 +- 2.43	58.0 +- 3.38	55.6 +- 3.39	52.9 +- 2.83	55.0 +- 3.68
(uA/V^2)	53.5 +- 1.93	57.2 +- 4.06	54.0 +- 3.33	53.8 +- 3.49	54.6 +- 3.48
P-MOSFET	94 vs 8	108 vs 9	107 vs 9	108 vs 9	413 vs 35
THRESHOLD	1.50 +- 1.45	0.91 +- 2.34	-3.55 +- 4.62	0.87 +- 1.49	NOT APPLICABLE
VTOp	-0.801 +- 0.010	-0.832 +- 0.016	-0.807 +- 0.011	-0.810 +- 0.012	-0.813 +- 0.017
(V)	-0.786 +- 0.005	-0.827 +- 0.024	-0.822 +- 0.028	-0.805 +- 0.015	-0.811 +- 0.025
P-MOSFET	94 vs 8	108 vs 9	107 vs 9	108 vs 9	413 vs 35
CONDUCTANCE	-1.60 +- 3.80	3.38 +- 6.05	2.19 +- 4.91	-0.34 +- 5.75	NOT APPLICABLE
KPp=uCo	20.0 +- .860	20.6 +- 1.17	19.8 +- .669	19.5 +- 1.20	20.0 +- 1.07
(uA/V^2)	19.8 +- .645	21.1 +- .715	20.2 +- .851	19.5 +- .660	20.1 +- .944
INVERTER	88 vs 9	102 vs 9	102 vs 9	102 vs 9	394 vs 36
THRESHOLD	-2.08 +- 0.68	-1.90 +- 0.84	-2.49 +- 0.95	-2.33 +- 0.88	NOT APPLICABLE
VINV	2.21 +- 0.014	2.17 +- 0.015	2.20 +- 0.011	2.19 +- 0.013	2.19 +- 0.022
(V)	2.17 +- 0.015	2.12 +- 0.010	2.15 +- 0.017	2.14 +- 0.008	2.15 +- 0.020
INVERTER	88 vs 9	102 vs 9	102 vs 9	102 vs 9	394 vs 36
GAIN	-1.30 +- 5.11	-0.13 +- 4.34	-3.12 +- 6.01	-2.19 +- 5.04	NOT APPLICABLE
(unitless)	-15.0 +- 0.59	-14.8 +- 0.79	-14.6 +- 0.67	-15.7 +- 0.71	-15.0 +- 0.82
	-15.3 +- 0.37	-14.9 +- 0.46	-14.9 +- 0.33	-15.9 +- 0.80	-15.2 +- 0.64

Transistor dimensions: Length = 3 um, Width = 9 um for both n- and p- channel.
Inverter Dimensions: Ln = 3.0, Wn = 4.5, Lp = 3.0, Wp = 6.0 (um, strips).
Ln = 3.0, Wn = 4.5, Lp = 3.0, Wp = 5.6 (um, chips).
Contact Dimensions: 3.0 um square, all layers.

This was manifest for all layers. The surfaces were never smooth or continuous, nevertheless the irregularities were not so closely spaced that the fitting algorithm could be suspected of working at too fine a resolution. Again, the features were three to four chips in diameter, so the fitted surfaces (using roughly a hundred points) were received with justifiable confidence.

3. Transistors: The following tables contain values for the threshold voltage, $VT0$, and KP derived from the maximum slope of the ID versus VG curve measured at $VD = 50$ mV. The KP values were calculated using the as-drawn channel width and length dimensions.

   (a) Threshold voltage, $VT0$ (V) at $VBS = 0$:

Transistor Dimensions (μm)	All Wafers Combined	Wafer # 1	Wafer # 4	Wafer # 5	Wafer # 10
n-channel	0.669	0.674	0.655	0.668	0.680
length=3	±0.014	±0.008	±0.012	±0.013	±0.009
width=6	395 pts.	89 pts.	102 pts.	102 pts.	102 pts.
n-channel	0.672	0.676	0.658	0.669	0.683
length=3	±0.015	±0.009	±0.015	±0.013	±0.009
width=9	394 pts.	89 pts.	101 pts.	102 pts.	102 pts.
n-channel	0.709	0.713	0.696	0.709	0.719
length=9	±0.012	±0.006	±0.011	±0.010	±0.007
width=6	394 pts.	89 pts.	102 pts.	101 pts.	102 pts.
n-channel	0.685	0.688	0.673	0.684	0.693
length=9	±0.012	±0.007	±0.009	±0.011	±0.008
width=9	391 pts.	89 pts.	99 pts.	101 pts.	102 pts.
p-channel	-.835	-.821	-.849	-.833	-.834
length=3	±0.016	±0.012	±0.013	±0.011	±0.012
width=6	415 pts.	94 pts.	107 pts.	107 pts.	107 pts.
p-channel	-.813	-.801	-.832	-.807	-.809
length=3	±0.017	±0.010	±0.016	±0.011	±0.012
width=9	413 pts.	94 pts.	106 pts.	107 pts.	106 pts.

Transistor Dimensions (μm)	All Wafers Combined	Wafer # 1	Wafer # 4	Wafer # 5	Wafer # 10
p-channel	-.860	-.845	-.875	-.860	-.856
length=9	±0.014	±0.008	±0.011	±0.011	±0.009
width=6	414 pts.	94 pts.	106 pts.	107 pts.	107 pts.
p-channel	-.846	-.833	-.861	-.845	-.845
length=9	±0.013	±0.009	±0.011	±0.009	±0.009
width=9	414 pts.	94 pts.	106 pts.	107 pts.	107 pts.

(b) $KP = \mu_o C_o$ at $VBS = 0$. Figures shown are KP (μA/V^2):

Transistor Dimensions (μm)	All Wafers Combined	Wafer # 1	Wafer # 4	Wafer # 5	Wafer # 10
n-channel	50.1	48.5	53.4	50.6	47.8
length=3	±3.64	±2.19	±3.33	±3.27	±2.53
width=6	394 pts.	89 pts.	101 pts.	102 pts.	102 pts.
n-channel	55.0	53.2	58.0	55.6	52.9
length=3	±3.68	±2.43	±3.38	±3.39	±2.83
width=9	395 pts.	89 pts.	102 pts.	102 pts.	102 pts.
n-channel	44.6	44.0	46.5	44.2	43.7
length=9	±1.51	±0.74	±0.93	±1.29	±0.88
width=6	394 pts.	89 pts.	102 pts.	101 pts.	102 pts.
n-channel	44.6	44.0	46.0	44.3	43.6
length=9	±1.24	±0.66	±0.72	±1.29	±0.84
width=9	391 pts.	89 pts.	99 pts.	101 pts.	102 pts.
p-channel	19.2	19.2	20.0	19.1	18.6
length=3	±1.06	±0.62	±1.06	±0.76	±1.12
width=6	415 pts.	94 pts.	107 pts.	107 pts.	107 pts.
p-channel	20.0	20.0	20.6	19.8	19.3
length=3	±1.07	±0.86	±1.17	±0.67	±1.20
width=9	413 pts.	94 pts.	106 pts.	107 pts.	106 pts.

Transistor Dimensions (μm)	All Wafers Combined	Wafer # 1	Wafer # 4	Wafer # 5	Wafer # 10
p-channel	15.5	15.7	16.0	15.0	15.3
length=9	±0.54	±0.30	±0.26	±0.43	±0.52
width=6	414 pts.	94 pts.	106 pts.	107 pts.	107 pts.
p-channel	16.3	16.5	16.5	15.9	16.2
length=9	±0.45	±0.23	±0.30	±0.37	±0.52
width=9	414 pts.	94 pts.	106 pts.	107 pts.	107 pts.

(c) General Comments about Transistor Maps: $VT0$ values were very uniformly distributed over all wafers with the standard deviation ranging from 12 - 17 mV. KP values for $L = 3$ μm show more variability than for $L = 9$ μm. This is due in part to variations in the channel length.

4. Inverters (Pulldown $L = 3, W = 4.5$; Pullup $L = 3, W = 6$):

   (a) VINV ($VDD = 5V$): After all final exclusions, the mean value is $2.192 \pm 0.022\,V$. The distributions were quite uniform over all four wafers (394 points). There was a slight tendency for the distribution to be lower at the perimeter (1 chip from the edge) with this effect most pronounced for wafer #5.

   (b) Gain: With all final exclusions, the mean value is -15.01 ± 0.82 (394 points). This parameter is uniformly distributed, except at the perimeter, about 2 chips from the edge.

6.8 Wafer Map Comparison of Test Strip and Test Chip Data

The surface fitting technique used is a Bivariate Interpolation and Smooth Surface Fit Algorithm [32,33]. We have found that the mean and standard deviations are generally well-preserved after interpolation. Surfaces were constructed using data from the Test Chips (termed the chip surface) and the Test Strips (termed the strip surface). Results for wafers 1, 4, 5, and 10 are listed in Table 6.6.

The chip surface is constructed from nine sites located in a 3×3 array found in the plane. Due to the limited number of points, exclusions of outliers

disrupt the surface fitting algorithm, which produces less reliable results due to the fewer number of seed points.

The strip surface is constructed from over a hundred points well dispersed over the plane. In general, the internal parts of surfaces constructed from so many points is trustworthy, but extrapolations on the perimeter can "explode" more quickly than if the number of seed points is small.

The chip and strip surfaces were generated by letting 25 interpolated points (each point is called a pixel) located in a 5×5 array represent each chip position. Then, the difference surface was formed by subtracting each strip pixel from the corresponding chip pixel, dividing this value by the absolute value of the strip pixel, and multiplying the result by 100. This surface represents the mean percent difference from which the standard deviation can be calculated to allow a simple comparison of the two wafer maps.

The difference map, with percent difference computed for each pixel position, and the histogram of these percent difference pixels were plotted. This gives an instant visual statement of the quality of the fidelity between the two fitted surfaces. To our knowledge, this is the first time such a comparison has been carried out. The results are listed in Table 6.6.

Briefly, the following general trends were found for this VTI-2 run:

1. VINV: The mean was -2 percent (the effect was systematic, due to the inverters on the strips differing slightly in structure from those on the chips), the standard deviation was 0.8 percent, and the difference surface was very uniform.

2. Gain: The mean was 2 percent (except for wafer #5 being 3 percent) and the standard deviation was 4 to 6 percent. For the gain, the surfaces were not as uniform as for VINV. In some interior regions the surfaces differed by over 5 percent and there was extensive variation in the periphery.

Differences between contact resistance maps were the most pronounced. The reasons are hinted at above where it is indicated that the surface generated from the Test Strips is a very "rugged" surface. In fact, the surface is sufficiently irregular that one would not expect the surface constructed from the chips (with eight or nine sites) to be comparable to the strip surface. However, the surface constructed from eight or nine chip sites, although a smooth surface relative to that constructed from the strip data, was an excellent "average" surface through the mountainous terrain. The pixel difference "mode" value was generally within five percent. The difference "mean" values were from 4 to 15 percent on the n+poly and n+diffusion contacts, but within one percent for the p+diffusion

contacts. However, because we have an average surface through a mountainous terrain, the standard deviations of the percent differences were high. The best fit was just less than ten percent while the worst fit (n+diffusion on wafer ten) was almost 44 percent. This effect was due largely to the effects of extrapolation external to the data points located on the periphery of the fitted surfaces. Therefore in this particular process, the nine Test Chips did not provide high fidelity in constructing the detail of the surface for contact resistance. The chip data did succeed in reconstructing the "average" surface with surprising statistical uniformity over the interior of the surfaces. This is evidenced by the relatively low mean value for percent difference.

Sheet resistance values, measured using the split-cross-bridge resistors, were in very close agreement between strips and chips. For p+diffusion, the mean difference was always less than one percent, with the standard deviation less than one percent; i.e., the surfaces agreed almost exactly. The means for n+diffusion were within four percent, with standard deviations less than seven percent. The surfaces for n+poly had mean differences of about one percent (except for wafer #10 where it was two percent) and standard deviations of about three percent. The surfaces when plotted, however, are more rugged than (for example) for p+diffusion, and the histograms are wider, as the larger standard deviations would indicate. The metal sheet resistance difference maps suffered only on the periphery; the means were about two percent and standard deviations about four percent.

Transistor parameters were studied for the case of gate length = 3 μm and gate width = 9 μm. Here, the mean value of the n-channel threshold voltage (for $VBS = 0$) difference maps was less than one percent and standard deviations were less than two percent. However, the n-channel KP values had means within two percent and standard deviations of about six percent. The p-channel transistor values were similar except for wafer #5, which had a mean of four percent for $VT0$. The standard deviation for $VT0$ was slightly less for n-channel and differed by almost two percent. Means for KP were within three percent but standard deviations were as high as six percent. It has not yet been determined whether these trends applied to other transistor dimensions.

In general, the agreement between the Test Strip and the Test Chip surfaces was surprisingly good except for the case of contact resistance.

In addition, we note that should any one of the nine sites be excluded for statistical reasons, the surface would have to be reconstructed with the excluded positions "filled" by extrapolations from the other sites. We propose that if structures are included on the Test Chips with the intent of characterizing a surface, those structures be redundantly constructed on each chip. This sug-

gested that 18 sites be used instead of 9. Thus, excluded data could be replaced by data acquired from a spare site.

6.9 Mean Value Comparison of Test Strip and Test Chip Data

The information to be presented below has been compiled from the statistical information which is produced for every run. While to this point, the analysis has been based on qualitative analyses, the software proceeds to generate true statistical analyses of the data. In the distillation which follows, we have suppressed the standard deviation and percent standard deviation, minimum, maximum, and population size information; we have also suppressed the wafer-by-wafer statistics, and the comparisons of the individual wafers to the lot summary statistics. In addition, many of the parameters obtained for transistors have also been suppressed. Shown below are the mean values for the entire lot only. From a study of the histograms for the Test Strips, and from a statistical analysis of the parameter means, it was found that no significant differences existed between the wafers. Thus, all wafers could be considered as drawing their values from a single normally distributed population. The same conclusion was applied to the Test Chips since their values are drawn from the same populations.

6.10 Mean Value Comparisons: Summary Results

Process: 3-μm CMOS/Bulk p-Well Single Metal Single Poly
Lot Number: JPL "VTI2", VTI Dev.4236-0000C4 Run A366
Wafer Numbers: 1, 4, 5, and 10
Date Compiled: August 1, 1986

In each data set below the three numeric columns are:

1. Mean from Test Strips on all wafers.
2. Mean from Test Chips on all wafers.
3. % difference, Test Strips to Test Chips.

1. Contact Resistors

Layer	Contact Size (μm)	Units	Strips	Chips	%
n+Diff	3.000	Ohms	5.13	5.33	3.9
n+Poly	3.000	Ohms	2.12	2.12	0.0
p+Diff	3.000	Ohms	15.0	14.5	-3.3

2. Inverters

Pulldown W/L (μm)	Pullup W/L (μm)	Parameter	Strips	Chips	%
4.50/3.00	5.60/3.00	VHIGH	5.00	4.99	-0.2
		VLOW	.041	.049	19.7
		VINV	2.19	2.15	-1.8
		GAIN	-15.0	-15.2	1.3

3. Split-Cross-Bridge Resistors

Layer	Bridge Width (μm)	Line Width (μm)	Parameter	Strips	Chips	%
Metal	13.5	4.5	RSHEET	.032	.032	-1.3
			WIDTHB	12.7	12.6	-0.8
			WIDTHS	3.78	3.38	-10.6
			SPACE	5.12	5.88	14.8
			PITCH	8.90	9.26	4.0
			ERRPITCH	-.011	.029	—
n+Diff	13.5	4.5	RSHEET	21.8	22.5	3.2
			WIDTHB	13.7	13.7	0.0
			WIDTHS	4.64	4.46	-3.9
			SPACE	4.40	4.75	8.0
			PITCH	9.04	9.21	1.9
			ERRPITCH	.0046	.023	401
n+Poly	9.0	3.0	RSHEET	22.5	22.2	-1.3
			WIDTHB	8.58	8.42	-1.9
			WIDTHS	2.59	2.49	-3.9
			SPACE	3.41	3.43	0.6
			PITCH	5.99	5.92	-1.2
			ERRPITCH	-.0011	-.013	—

Layer	Bridge Width (μm)	Line Width (μm)	Parameter	Strips	Chips	%
p+Diff	13.5	4.5	RSHEET	87.2	86.6	-0.7
			WIDTHB	13.3	13.1	-1.5
			WIDTHS	4.35	4.22	-3.0
			SPACE	4.59	4.61	0.4
			PITCH	8.94	8.84	-1.1
			ERRPITCH	-.0069	-.018	164

4. Transistors

Type	Wid/Len (μm)	Parameter	Strips	Chips	%
n-MOSFET	6.00/3.00	VT0	.672	.674	0.3
		VT1	1.06	1.06	0.0
		VT5	1.95	1.95	0.0
		KPRIME0	50.1	49.9	-0.4
		GAMMA01	.833	.833	0.0
		GAMMA15	.818	.819	0.1
		DRLEAK	20.2	26.3	30.2
		ISAT0	508.	505.	-0.6
		ISAT1	458.	455.	-0.7
		ISAT5	327.	325.	-0.6
	6.00/9.00	VT0	.709	.708	-0.1
		VT1	1.12	1.12	0.0
		VT5	2.09	2.09	0.0
		KPRIME0	44.6	44.4	-0.4
		GAMMA01	.870	.871	0.1
		GAMMA15	.899	.899	0.0
		DRLEAK	21.1	17.3	-18.0
		ISAT0	174.	173.	-0.6
		ISAT1	150.	150.	0.0
		ISAT5	91.6	91.1	-0.5
	9.00/3.00	VT0	.669	.668	-0.1
		VT1	1.06	1.06	0.0
		VT5	1.93	1.93	0.0
		KPRIME0	55.0	54.6	-0.7
		GAMMA01	.829	.832	0.4

Type	Wid/Len (μm)	Parameter	Strips	Chips	%
n-MOSFET	9.00/3.00	GAMMA15	.802	.806	0.5
		DRLEAK	14.3	19.9	39.2
		ISAT0	819.	812.	-0.9
		ISAT1	742.	735.	-0.9
		ISAT5	544.	538.	-1.1
	9.00/9.00	VT0	.685	.683	-0.3
		VT1	1.09	1.09	0.0
		VT5	2.05	2.05	0.0
		KPRIME0	44.6	44.5	-0.2
		GAMMA01	.867	.868	0.1
		GAMMA15	.886	.884	-0.2
		DRLEAK	20.9	12.8	-38.8
		ISAT0	274.	274.	0.0
		ISAT1	238.	237.	-0.4
		ISAT5	148.	147.	-0.7
p-MOSFET	6.00/3.00	VT0	-.835	-.829	-0.7
		VT1	-1.01	-1.01	0.0
		VT5	-1.37	-1.37	0.0
		KPRIME0	19.2	19.4	1.0
		GAMMA01	-.385	-.386	0.3
		GAMMA15	-.331	-.329	-0.6
		DRLEAK	-20.9	-19.2	-8.1
		ISAT0	-223.	-225.	0.9
		ISAT1	-210.	-212.	1.0
		ISAT5	-177.	-179.	1.1
	6.00/9.00	VT0	-.860	-.858	-0.2
		VT1	-1.07	-1.07	0.0
		VT5	-1.56	-1.56	0.0
		KPRIME0	15.5	15.3	-1.3
		GAMMA01	-.460	-.460	0.0
		GAMMA15	-.446	-.448	0.4
		DRLEAK	-22.8	-25.0	9.6
		ISAT0	-60.7	-60.3	-0.7
		ISAT1	-55.1	-54.8	-0.5
		ISAT5	-41.9	-41.6	-0.7
	9.00/3.00	VT0	-.813	-.811	-0.2
		VT1	-.984	-.981	-0.3

Type	Wid/Len (μm)	Parameter	Strips	Chips	%
p-MOSFET	9.00/3.00	VT5	-1.32	-1.32	0.0
		KPRIME0	20.0	20.1	0.5
		GAMMA01	-.367	-.366	-0.3
		GAMMA15	-.310	-.309	-0.3
		DRLEAK	-13.4	-28.1	109.7
		ISAT0	-356.	-358.	0.6
		ISAT1	-337.	-340.	0.9
		ISAT5	-290.	-293.	1.0
	9.00/9.00	VT0	-.846	-.846	0.0
		VT1	-1.05	-1.06	1.0
		VT5	-1.52	-1.52	0.0
		KPRIME0	16.3	16.1	-1.2
		GAMMA01	-.446	-.454	1.8
		GAMMA15	-.426	-.428	0.5
		DRLEAK	-22.6	-13.3	-41.2
		ISAT0	-95.3	-95.0	-0.3
		ISAT1	-87.1	-86.8	-0.3
		ISAT5	-67.5	-67.2	-0.4

Notes: $KPRIME = \mu_o C_o \times 10^6$
DRLEAK in picoamps
$ISAT$ @ VGS=5V, VDS = 5.0V in microamps
$VTx, ISATx$ where x = value of VBS in volts

The agreement between Test Strips and Test Chips is generally within three percent. In the cases of metal sheet resistance and transistor leakage the differences are due to highly skewed populations, indicating the need for a more effective method of identifying outliers.

6.11 Wafer Maps

The following pages contain selected Test Strip wafer maps from Wafer #10. The data is presented as avenue wafer maps where dots indicate the location of the data points on the four-inch diameter CMOS wafer. The surfaces were fitted to the data using a Bivariate Interpolation and Smooth Fit Algorithm[32,33].

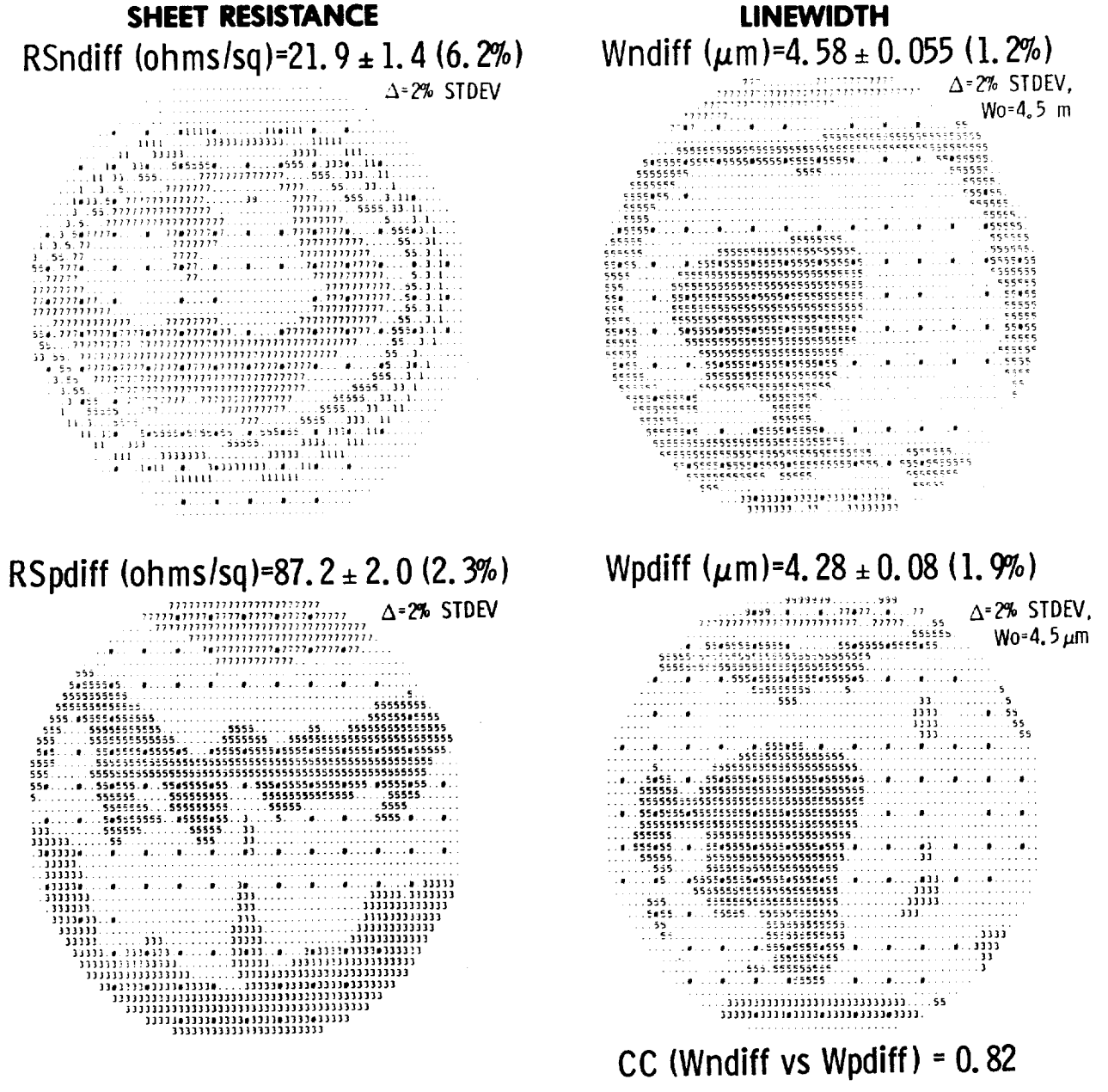


Figure 6.3: Test Chip wafer maps for the sheet resistance and linewidths of the n+diffusion (top) and p+diffusion (bottom) from VTI 2, Wafer #10.

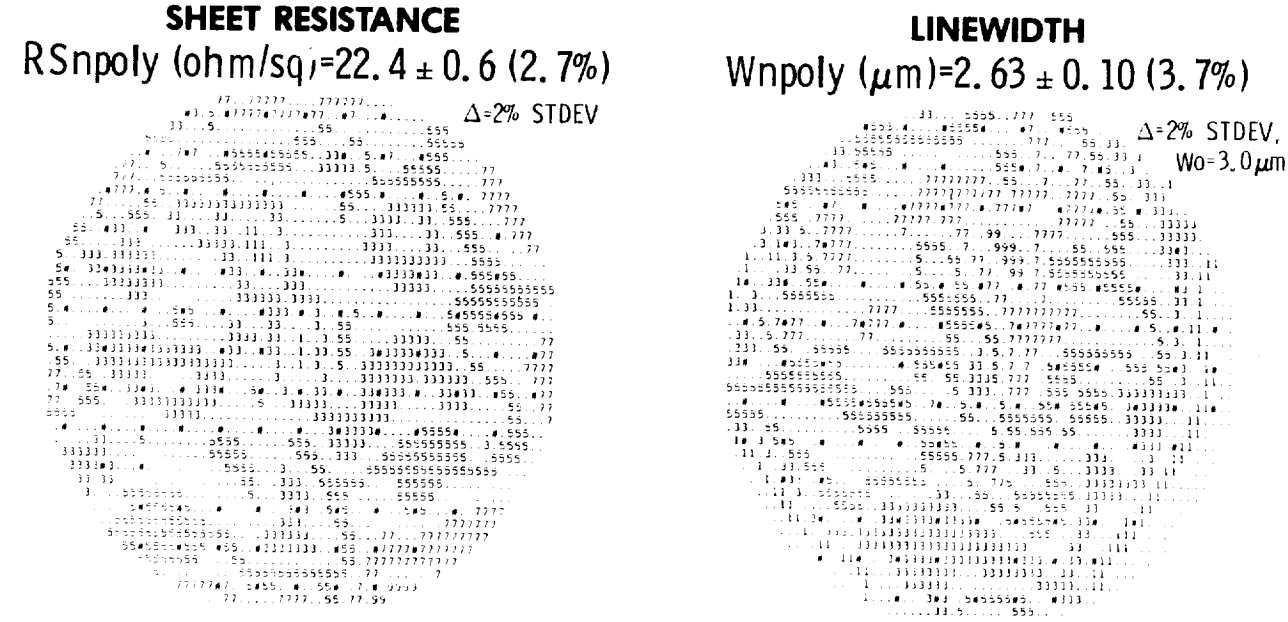
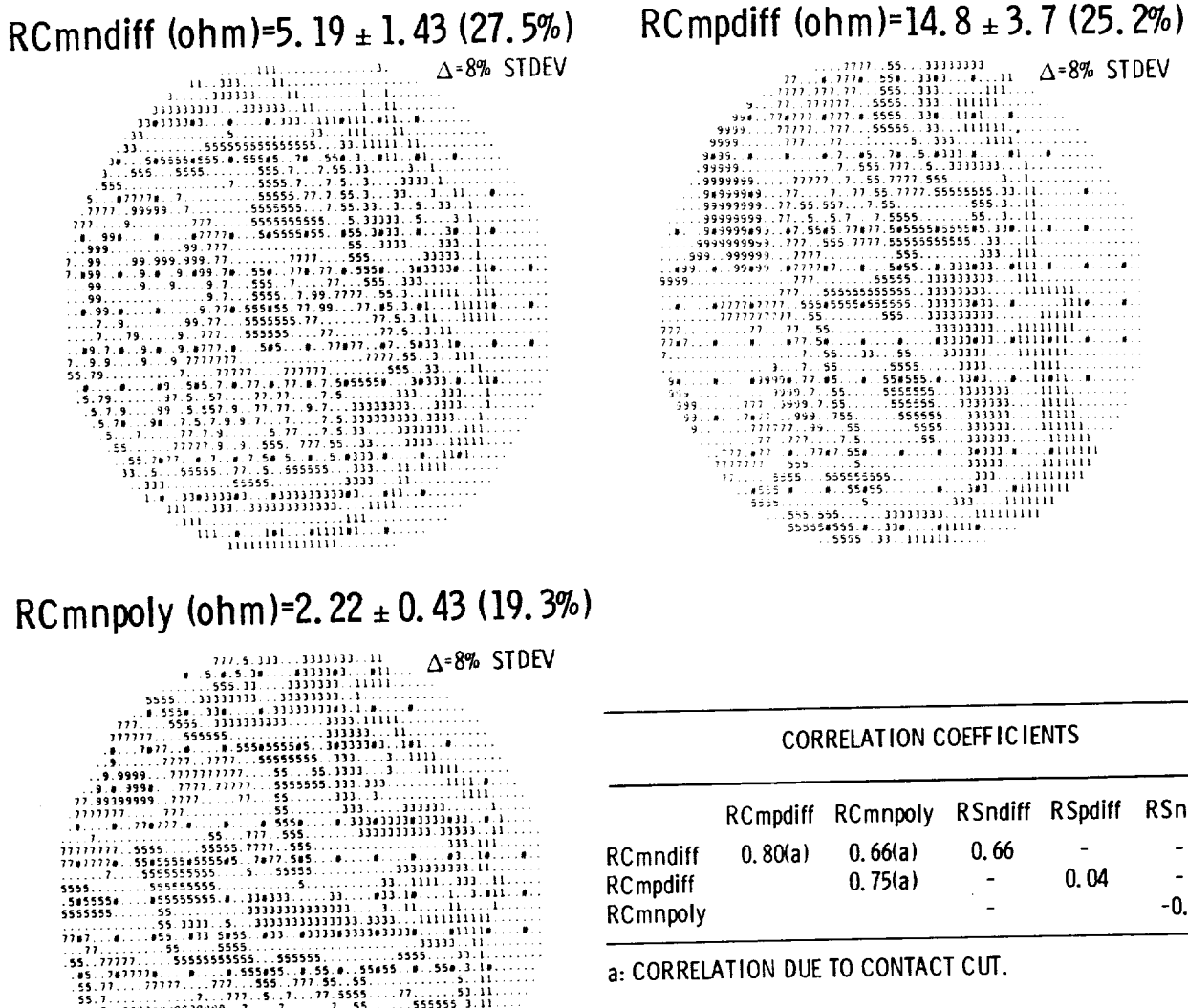


Figure 6.4: Test Chip wafer maps for the sheet resistance and linewidths of the n+poly (top) and metal (bottom) from VTI 2, Wafer #10.



CORRELATION COEFFICIENTS

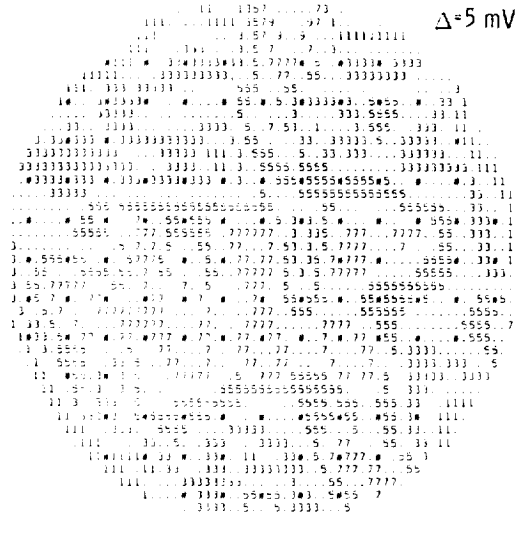
	RCmpdiff	RCmnpoly	RSndiff	RSpdiff	RSnpoly
RCmndiff	0.80(a)	0.66(a)	0.66	-	-
RCmpdiff		0.75(a)	-	0.04	-
RCmnpoly			-		-0.19

a: CORRELATION DUE TO CONTACT CUT.

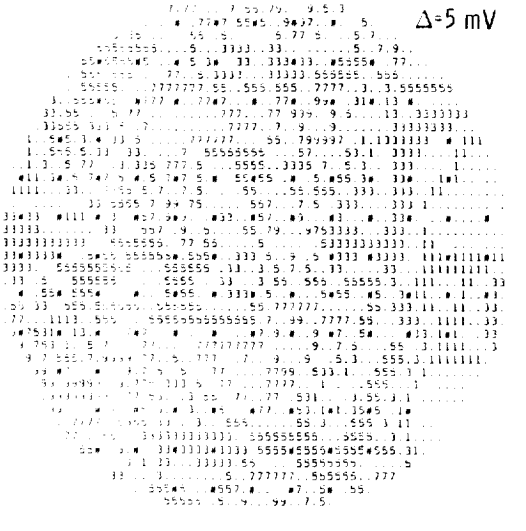
Figure 6.5: Test Chip wafer maps for the contact resistances of metal to (1) n+diffusion (top, left) (2) p+diffusion (top, right), and (3) n+poly (bottom, left) from VTI 2, Wafer #10. In the lower right hand corner is a matrix showing the correlations between the different contact resistance wafer maps and between the contact resistance and related sheet resistance maps.

THRESHOLD VOLTAGE

VTOn (V)=0.680 ± 0.009 (1.3%)

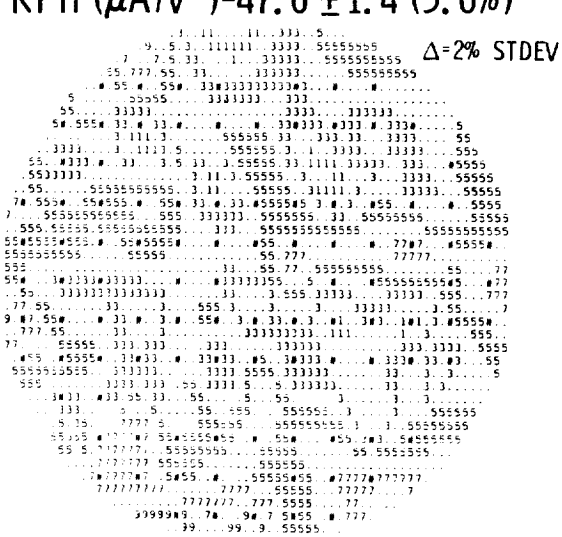


VTOp (V)=0.810 ± 0.012 (1.5%)



CONDUCTION FACTOR

KPn ($\mu A/V^2$)=47.6 ± 1.4 (3.0%)



KPp ($\mu A/V^2$)=17.6 ± 0.9 (5.1%)

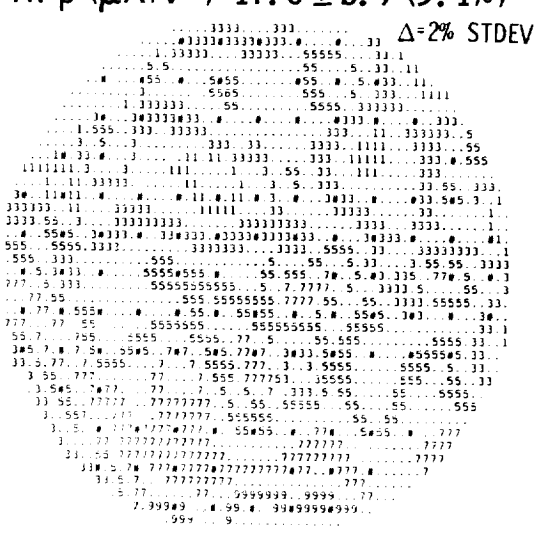
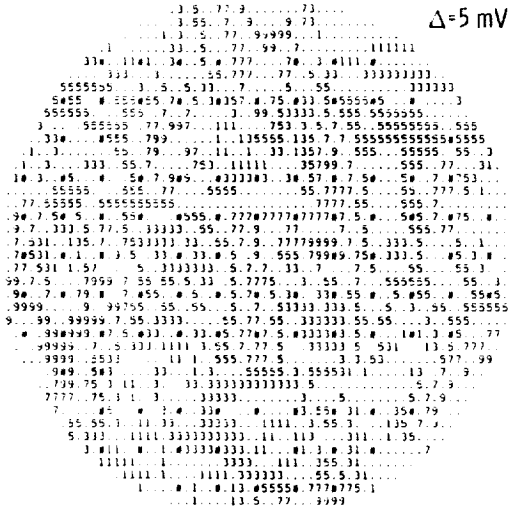


Figure 6.6: Test Chip wafer maps for the transistor threshold voltage, $VT0$, (top) and conduction factor, KP, (bottom) for n-channel MOSFETs (top) and p-channel MOSFETs (bottom).

INVERTER THRESHOLD VOLTAGE

VINV (V)=2.19±0.013 (0.6%)

Δ=5 mV



INVERTER GAIN

|GAIN| =15.7±0.7 (4.5%)

Δ=2% STDEV

CC(VINV vs VTOdiff) = -0.17
VTOdiff = VTOn− |VTOp|
THIS CORRELATION EXPECTED BUT NOT OBSERVED BECAUSE VTO's EXTREMELY TIGHT.

CC (|GAIN| vs Wnpoly) = 0.82
CC (|GAIN| vs VTOsum) = 0.54
VTOsum = VTOn + |VTOp|

Figure 6.7: Test Chip wafer maps for the inverter parameters VINV (left) and Gain (right).

Chapter 7

CRRES Project

7.1 Introduction

The JPL CRRES Chip is a full custom test circuit designed for inclusion in the Microelectronics Package (MEP) of the Combined Release and Radiation Effects Satellite (CRRES). The JPL CRRES chip consists of three operational test circuits for space radiation testing: a Static Random Access Memory for evaluating single event upset rates, a Timing Sampler circuit for evaluating radiation-induced timing degradation, and a-32 cell Transistor Matrix for evaluating the radiation degradation of SPICE-like transistor parameters.

The chip was fabricated at a CMOS foundry and parts for the MEP were delivered to the CRRES program in March 1986. Parts were also supplied to the NASA/JPL ground test segment of the CRRES program.

7.2 Purpose

The purpose of the JPL CRRES chip is:

1. To demonstrate the viability of using custom VLSI circuits in a spacecraft.
2. To validate the JPL microcircuit product assurance technology approach, based on the use of a family of test chips, for procuring custom ICs.
3. To provide a transistor-level understanding of the radiation response of VLSI circuits fabricated at a radiation-soft silicon foundry.
4. To correlate the space radiation response of CRRES chip parameters with ground radiation tests and to provide worst-case circuit design guidelines.
5. To evaluate Single Event Upset (SEU) and total ionizing dose (TID) radiation effects.

7.3 Description of CRRES Chip and Foundry Runs During Reporting Period

The JPL CRRES chip shown in Figure 7.1 is a 3-μm CMOS/Bulk p-well space radiation test chip containing three unique experimental structures: a transistor matrix for parameter extraction, a static random access memory (SRAM) for single-event-upset (SEU) detection, and a timing sampler for measuring radiation-induced timing degradation. The JPL CRRES chip is included in the

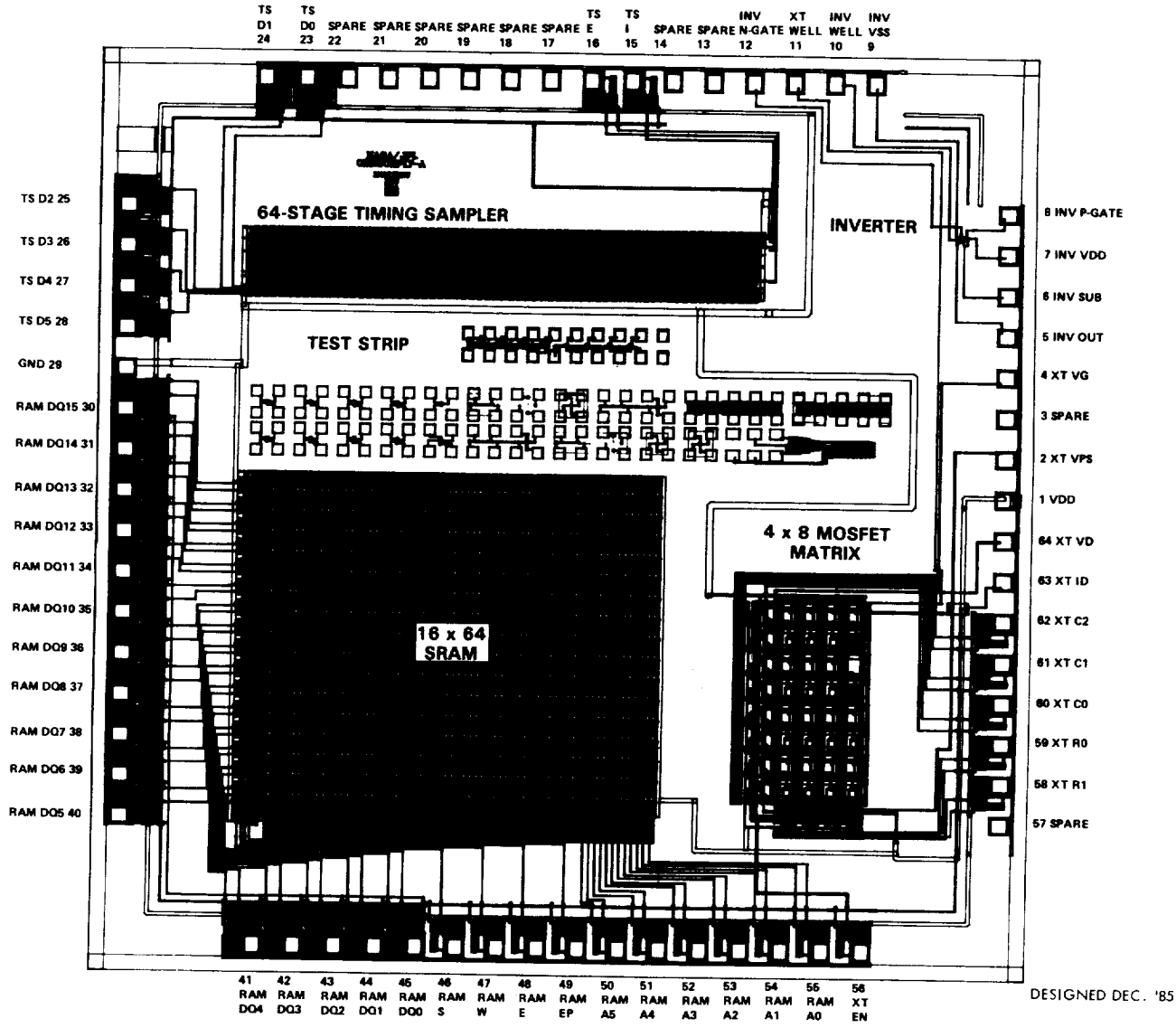


Figure 7.1: The JPL CRRES Chip which is 6.9 mm $\times$ 6.8 mm.

Microelectronics Package (MEP) of the CRRES satellite (Figure 7.2), presently scheduled to be launched in the early 1990's. The CRRES chip also contains several circuits for ground test: a stand-alone six-terminal inverter, JPL parametric test strips for process/fabrication assurance, and (on early versions) a ring oscillator for obtaining timing data to confirm timing sampler results.

This section provides a brief description of the design and function of the JPL CRRES chip and a description of results obtained during the report period. Pin-outs and timing requirements for testing the chip can be found in Section 7.10. The JPL CRRES chip design and function are described in the "Product Assurance Technology for Custom LSI/VLSI Electronics" report for the period October 1982-September 1984 (JPL Publication No. 85-76).

The 1 kbit Static Random Access Memory (SRAM) is organized into 64 16-bit words. The SRAM utilizes either a symmetrical or an asymmetrical six-transistor SRAM cell. These different cells allow investigation of changes in upset rate due to geometry and are described in Section 7.4. The read/write circuitry (Figure 7.3) allows full static operation; all timing data is for minimum execution times for given operations. This design is expected to be the least susceptible to radiation-induced timing changes affecting SEU results.

The transistor matrix (Figure 7.4) is a 32-element, Kelvin tapped, low-leakage circuit for extraction of SPICE-like parameters. The device under test is powered by a separate supply, allowing sub-threshold (pA) measurement. The matrix has 8 columns of 4 locations with either n- or p-channel transistors (Figure 7.5): 29 of these locations contain normal gate oxide transistors of one of four sizes (Figure 7.6). Two locations contain n-channel field oxide transistors (one poly and one metal gate), and one location remains blank for measuring total leakage when all transistors are off.

The timing sampler (Figure 7.7) is a chain of 64 loaded inverter pairs. It is tested by sending a pulse along the chain for a given time. The number of stages that the pulse passes is presented as a binary number. Thus, in-space measurements are simplified. The timing sampler circuit and test results are also described in Chapter 3.

The chip was fabricated by the MOS Implementation Service of ISI (MOSIS) and by two foundry submissions (Foundry 1 and Foundry 2) to enable comparisons of radiation hardness of different processes and manufacturers. Table 7.1 lists the foundry runs used in the development of this chip. Electrical analysis of Foundry 1 indicated that the 1k SRAM chips were only nominally acceptable. The yield was about 20 percent at the wafer level and the chips were latch-up prone. The dominant failure mode of the remaining 1k SRAM chips was high leakage current (on the order of hundreds of microamperes). The 4k SRAM

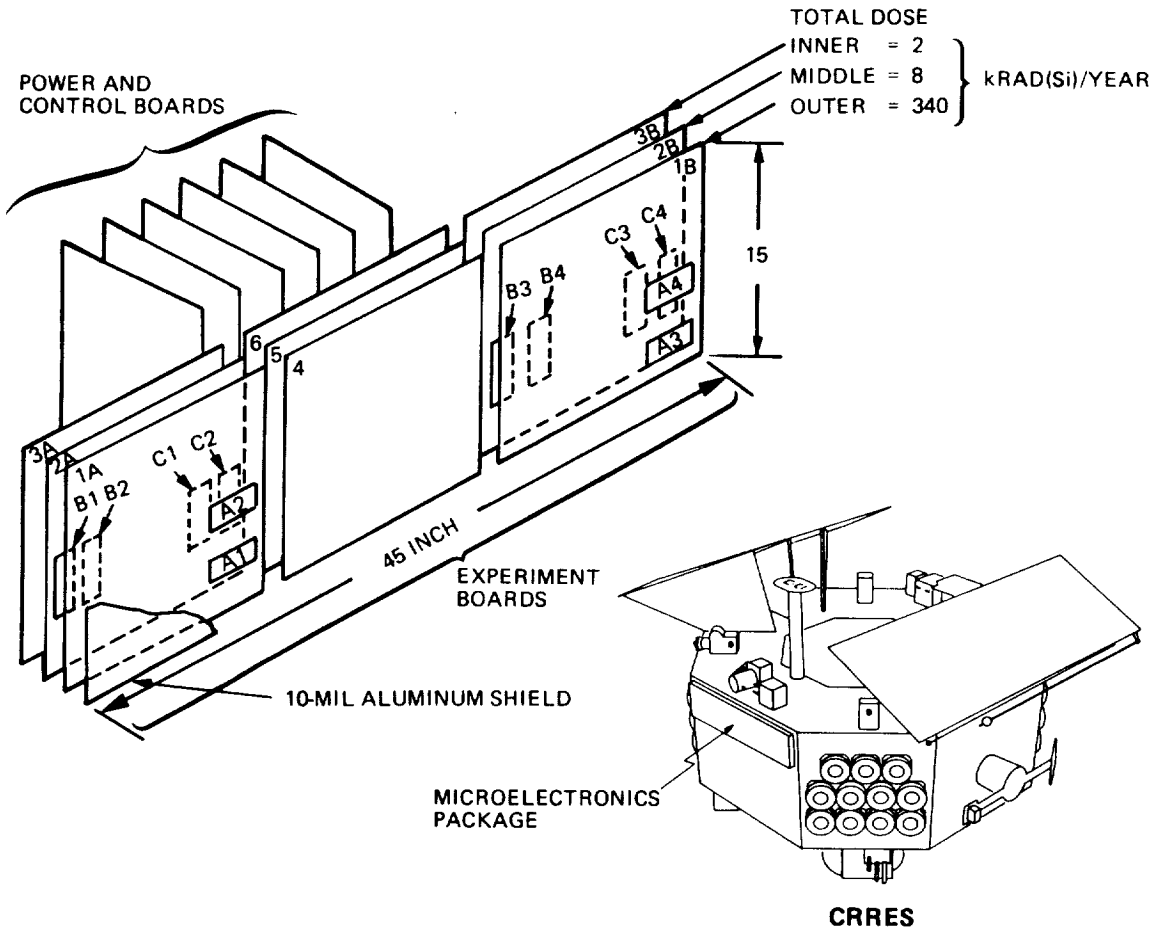


Figure 7.2: The CRRES Satellite showing the location of the Microelectronics Package (MEP), the expected doses for the various experimental boards, and the locations of the 12 JPL CRRES chips denoted by A1-A4, B1-B4, and C1-C4.

Table 7.1: Summary of CRRES/MOSIS Projects as of March, 1987.

PROJECT NAME(S)	MOSIS RUN NUMBER	— DATES — SUBMIT	PKGS OUT	ADDITIONAL RUN(S)
RAM1,RAM1B,RAM1F	M65P	5-20	7-23	
CRESCHP18_B,CRESCHP18_A	M61P	1-8	2-21	
CRESCHP17_B	M5BG	11-22	2-7	
CRESCHP17_A	M5BG	11-22	2-7	
CRESCHP16M	M5BE	11-5	1-29	
PADTEST2	M5BE	10-28	1-29	
PADTEST3	M5BE	10-28	1-29	
PADTEST1	M5BE	10-28	1-29	
CRRES4K9,CRESCHP16	M5BE	10-17	1-29	
CRRES4K8,CRESCHP15	M59A	9-26	1-28	
CR4K7TS,CR4K7R,CR4K7M	—	8-17	*	
CRRES4K7	M56G	5-30	7-23	M57Q
CRRES4K6	M55C	4-24	7-16	M54A
ARRAYN1,ARRAYP1	M53X	3-12	†	M54A,M57Q M58U,M63E
CRRES4K5	M53X	2-15	†	M54A
PADTEST	M53X	2-18	†	M54A
CRESCHP14	M53X	2-6	†	M54A
CRRES4K4	M52S	2-6-85	4-8	
PADTEST	M4CL	11-19	2-5	
CRRES4K3	M4CL	11-19	2-5	M51P-F
CRRES4K2	M4AD	10-17	1-30-85	M4BG-F-M51R-F
2KRAM	M49A	9-13	12-21	M4AD
CRESCHP12,CHIP8284	M48V	8-2	11-30	M49A
CRESCHP11	M46M	6-19	9-13	M47T-F-M48V
CRESCHP10,CRRESCHP8	M45H	5-23	10-10	M46M-M47T-F
CRRESCHP7	M44E	3-30	6-19	M45H
CRRESCHP6	—	2-29	‡	
CRRESCHP5	—	2-28	‡	
CRRESCHP3	M42X	2-1	†	
CRRESCHIP2	M41V	1-16-84	4-11-84	
CRRESCHIP	M3AJ	10-19-83	†	M39D,M39H,M3BM, M3CO,M41V

Notes: CRRESCHPn = 1k SRAM Version CRRES Chip
CRRESCHPnM = 1k SRAM Version CRRES Chip, MOSIS/MIT I/O Pads
CRRES4Kn = 4k SRAM Version CRRES Chip
ARRAYP1, ARRAYN1 = p- or n-Channel Kelvin Tapped Transistors
RAM1, RAM1B, RAM1F = Normal, Asymmetrical, or Faulted SRAM
*DELETE-CIF; †WAFERS FAILED; ‡RUN CANCELLED

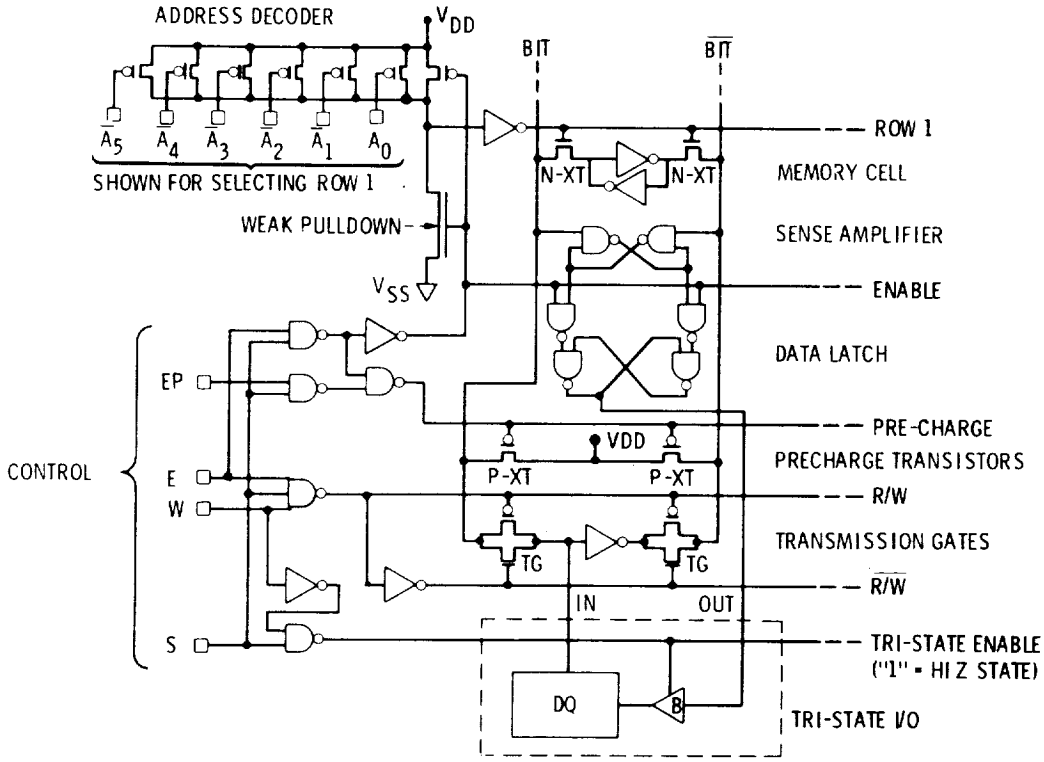


Figure 7.3: JPL CRRES chip SRAM logic diagram.

chips had zero percent yield; the dominant failure was very high leakage current (milliamperes).

The 4k SRAM problem was traced to two design errors (Figure 7.8): the pulldown transistors were not connected to ground in the SRAM cell due to a misplaced p-well ground connection and the p-well and p+diffusion separation in adjoining SRAM cells was too small.

The 1k SRAM chip was submitted for destructive physical analysis at JPL. The problems on this chip were traced to encroachment of the p-well beyond the JPL design rules (Figures 7.9 and 7.10). Such encroachment caused the functional problems described above. The foundry's design rules were examined and found to be more conservative than JPL's on this critical dimension. This analysis also indicated substantial voiding in the field oxide (Figure 7.11). This voiding is not thought to have contributed to any observed yield or functional problems, but could cause long-term reliability problems.

The 1k chip was selected for design modifications and fabrication in order to assure a functional circuit in the remaining single foundry run. At this same

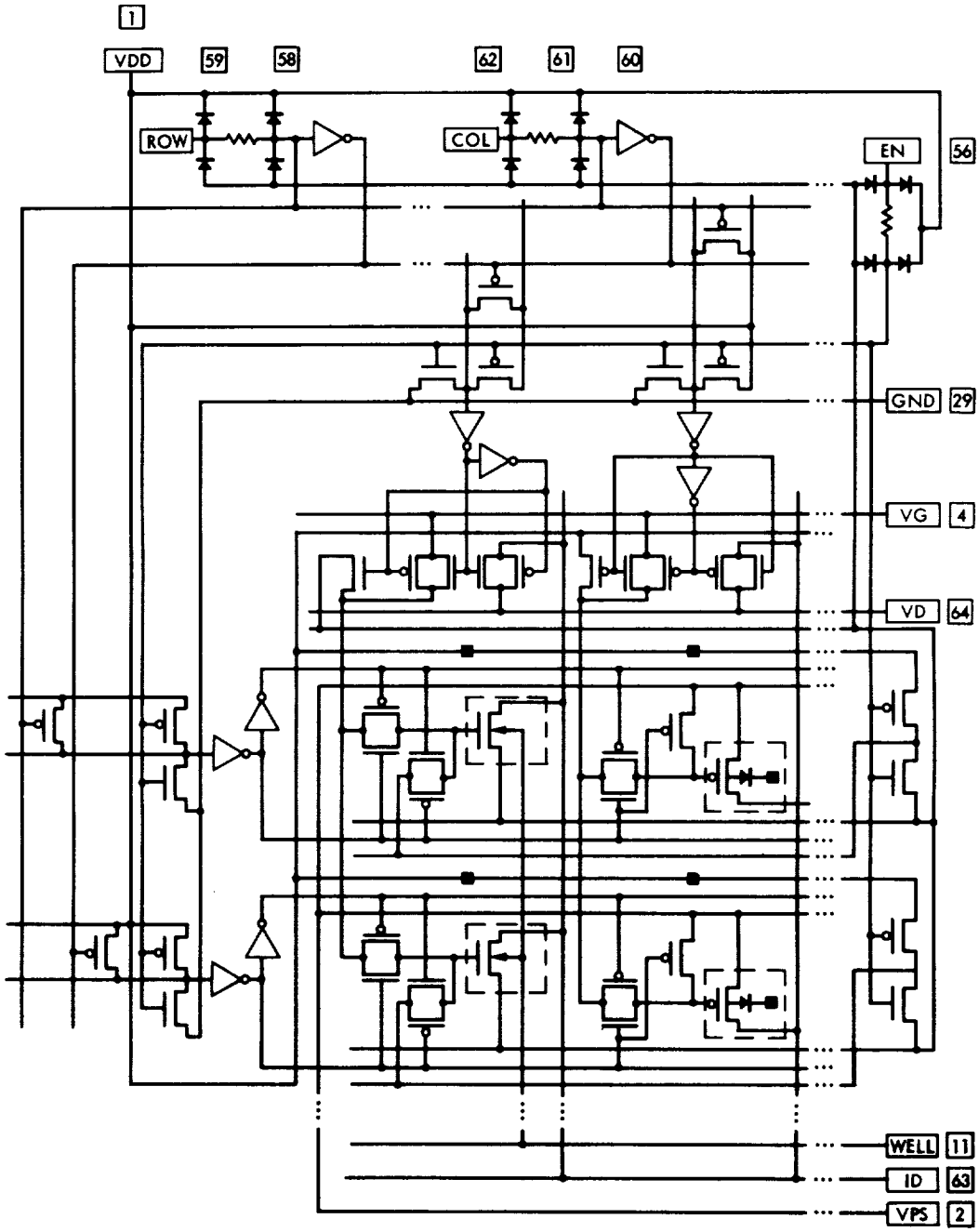


Figure 7.4: The JPL CRRES Chip MOSFET Matrix.

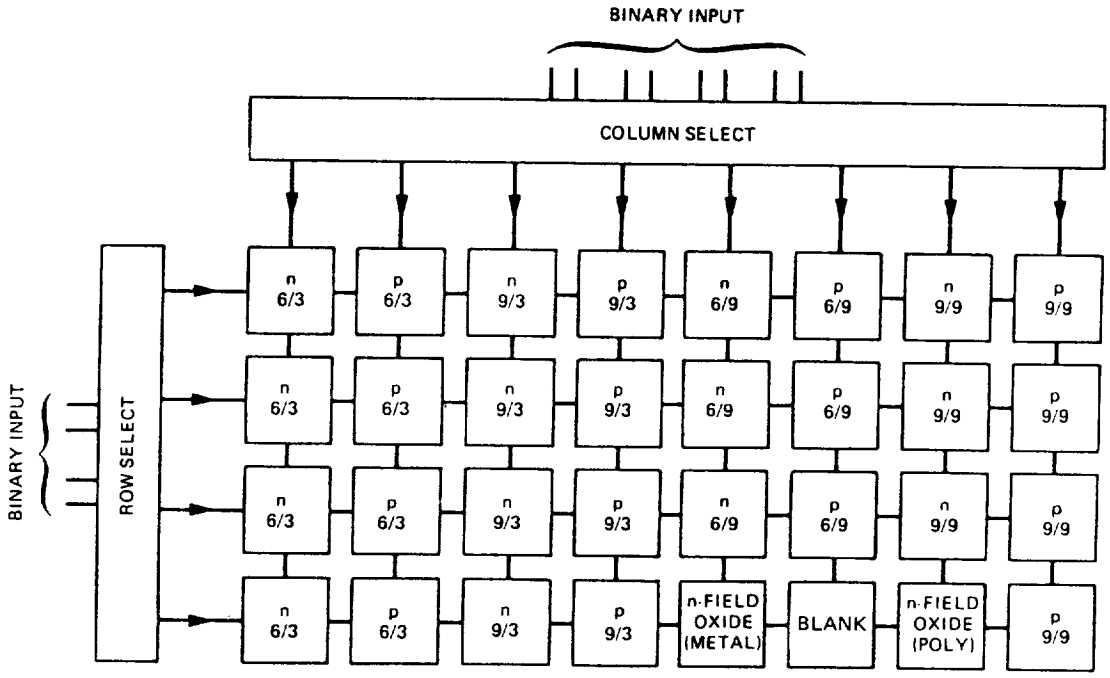


Figure 7.5: Locations of the various transistor sizes in the MOSFET matrix.

time, the ring oscillator was removed from the timing sampler circuit and a new drop-in test strip was placed on the chip.

The Foundry 2 submission was received at the end of February 1986: packaged parts and four wafers were delivered. This run incorporated chips with symmetrical and asymmetrical SRAM cells. About 50 percent of the packaged symmetric cell parts passed all screening tests; this was considerably better than the 20 percent yield resulting from Foundry 1. The asymmetric cell did not pass qualification for the CRRES due to consistently bad I/O lines (DQ1-4).

Chips of the same design as those fabricated at Foundry 2 were also fabricated by MOSIS (MOSIS run M61P). However, the MOSIS run resulted in zero percent electrical yield, compared to 50 percent yield from Foundry 2. The zero percent MOSIS yield was caused by a step coverage problem in the first metal fabrication step and was identified by comparison of results from JPL Fault Chips (Section 2.2) fabricated on each of the two runs.

CRRES Chips from the Foundry 1 and 2 runs were sent to the CRRES program in March of 1986 for integration into the MEP and to serve as spares. A complete listing of all deliveries of JPL CRRES Chips to the CRRES program is shown in Table 7.2 along with the expected total dose before failure for these

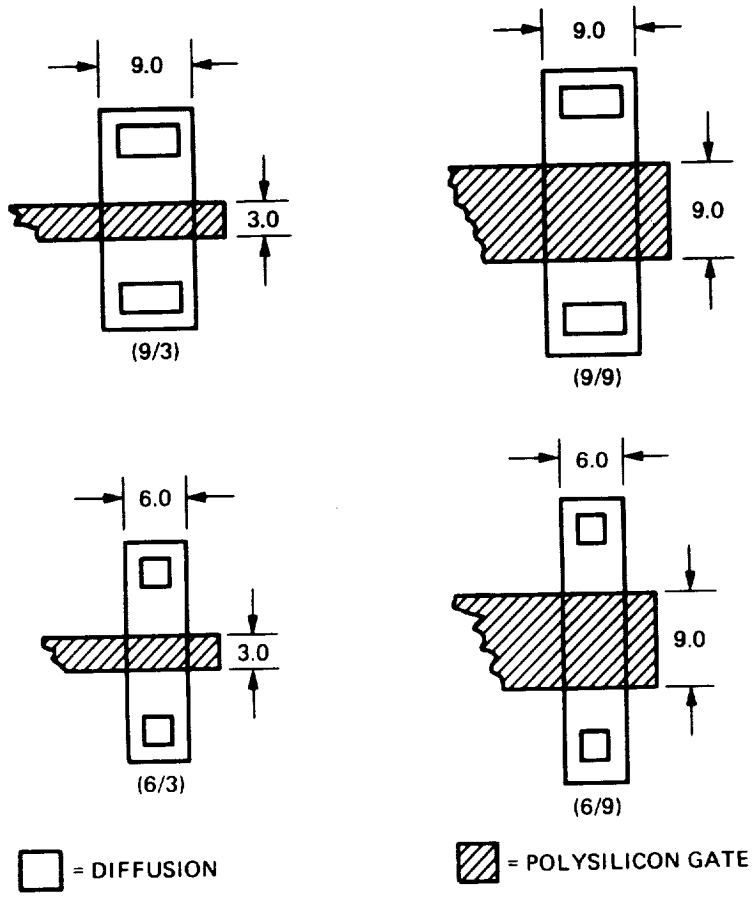


Figure 7.6: Geometry of cells in MOSFET Matrix.

Table 7.2: JPL CRRES Chip deliveries to the CRRES program.

Process	Fail-Dose krad(Si) (De-Lidded)	Breadboard	Flight	Flight (Spare)	SEU JPL	TID AFWL
A (VTI2)	15		4(b)	1(b)	6(c)	10
B (VTI2)	15		4(b)	1(b)		
C (VTI1)	15	9(a)	4(b)	1(b)	4(c)	

(a) = 12-18-85; (b) = 3-11-86; (c) = 3-15-86

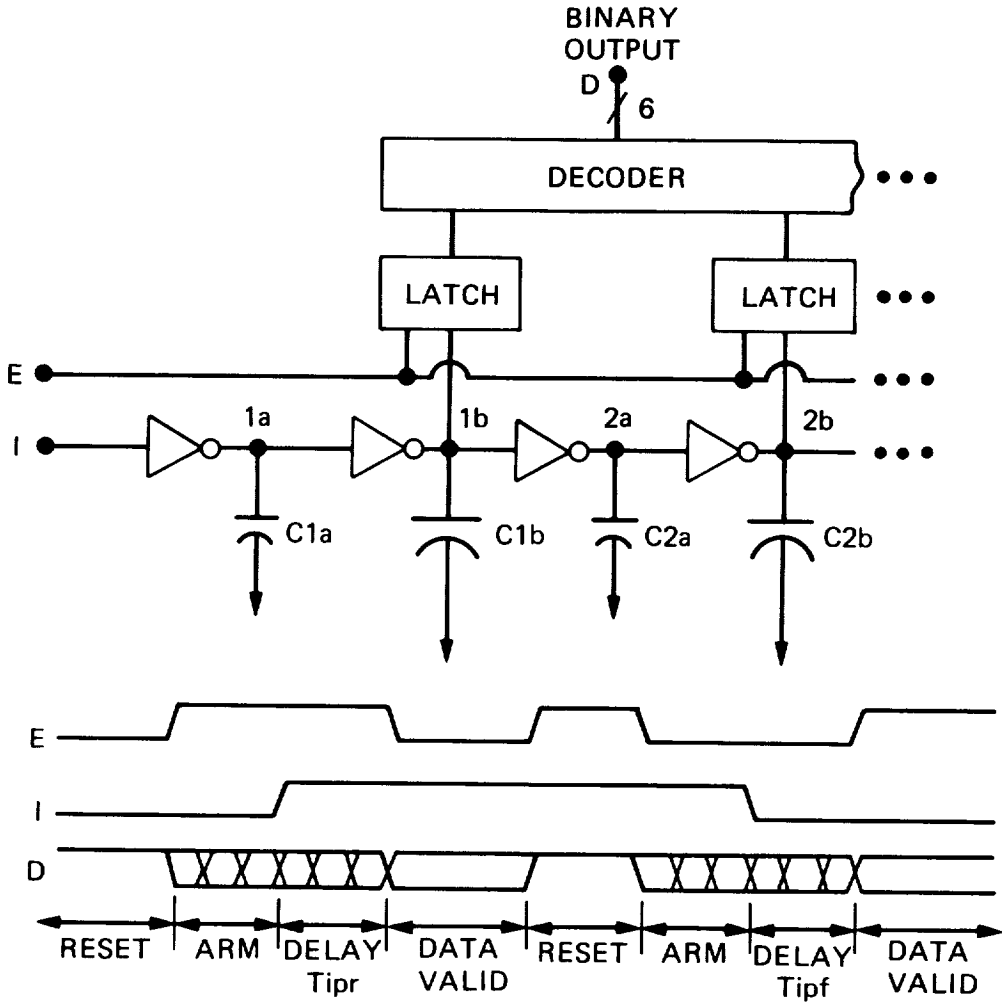


Figure 7.7: JPL CRRES Chip Timing Sampler Circuit.

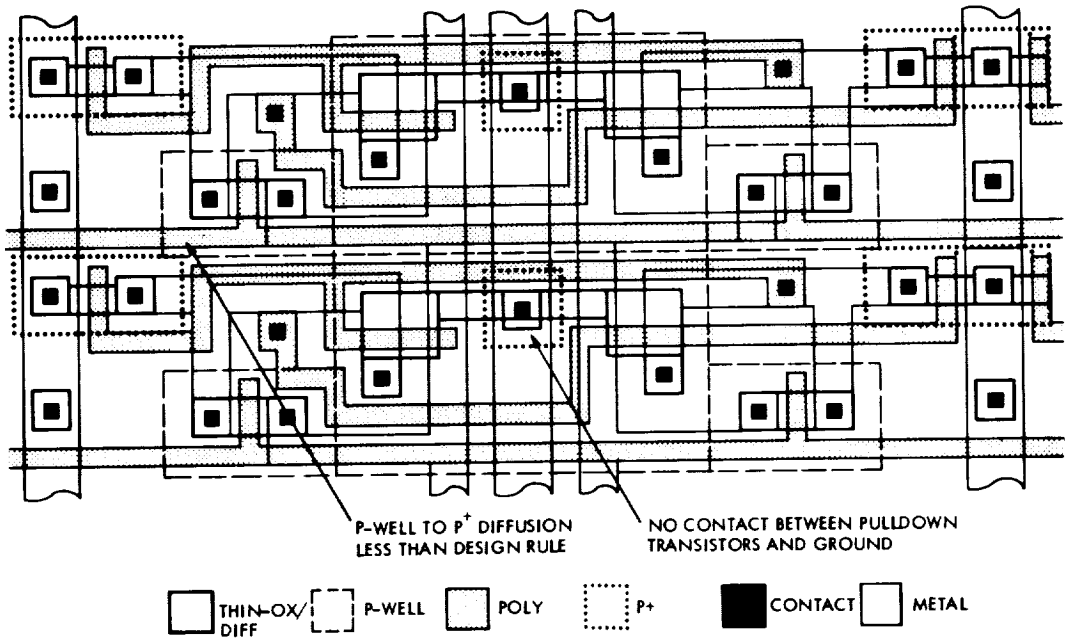


Figure 7.8: Design errors in the 4 kbit SRAM cell.

parts. These parts used the 1 kbit SRAM with symmetrically designed cells. Before the parts intended for the satellite were shipped, they were fully characterized electrically and the data archived at JPL for analysis of test results from space. The location of the chips in the MEP is shown in Figure 7.2 along with the expected dose rate for each board. Table 7.3 shows the chip/board placement and dose rate expected for the JPL CRRES Chips in the MEP.

An analysis of the MEP/JPL CRRES Chip interface was performed in January 1987 and a complete circuit diagram generated, as seen in Figure 7.12. There are several concerns about this interface, indicated on the figure, which may affect the accuracy of measurements made on the JPL CRRES Chips.

7.4 SRAM

The SRAM test circuit (Figure 7.3) is accessed through 64 16-bit words (through tri-state I/O pads), using 4 control lines and 6 address lines. The memory cell is the six-transistor static cell typically used for radiation hard applications.

Functional testing of the SRAM is conducted using a DAS 9100. Standard SRAM patterns of all ones, all zeros, walking ones, and walking zeros are used

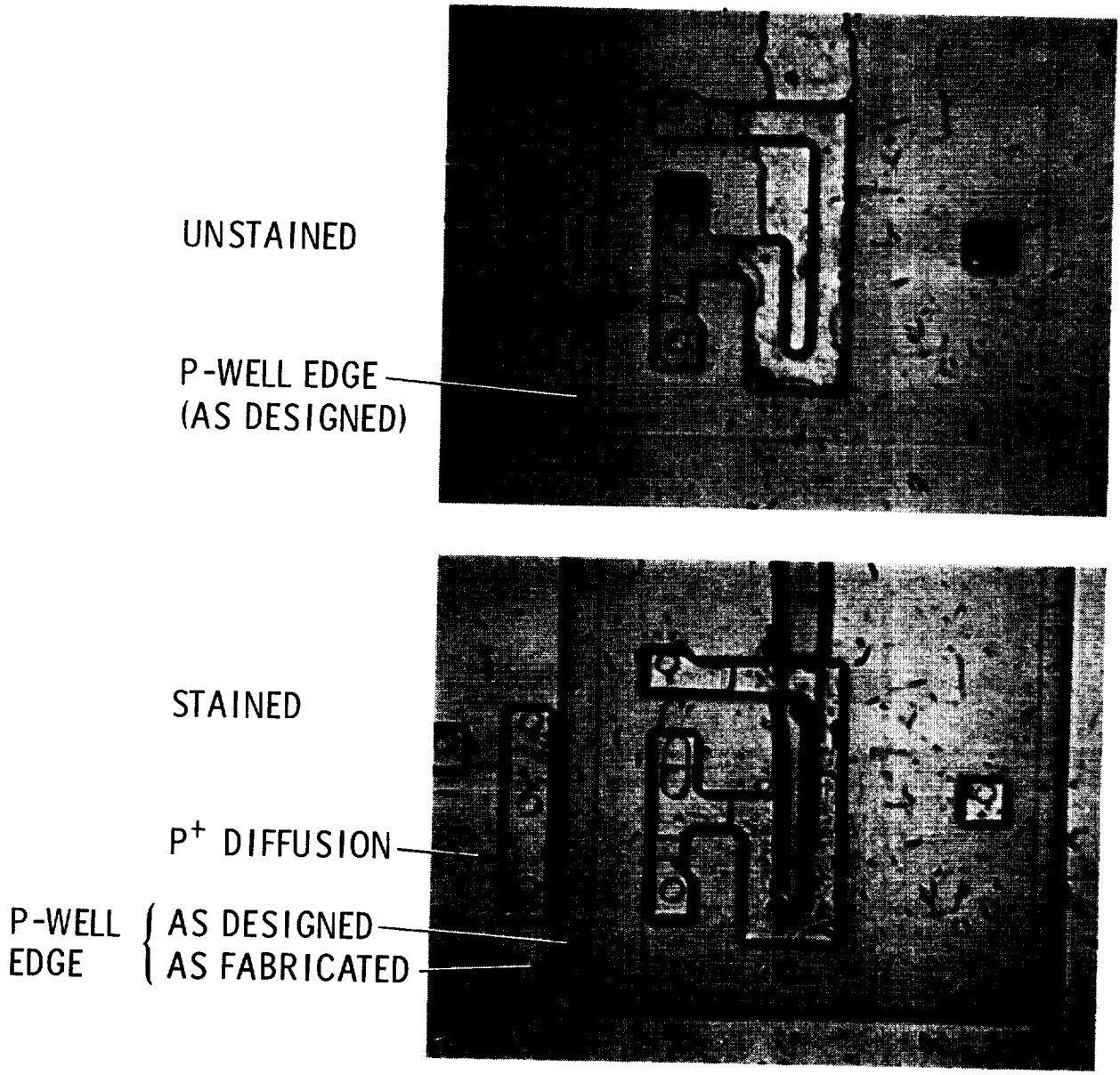


Figure 7.9: Encroachment of the p-well into the p+diffusion in the transistor matrix decoder circuitry.

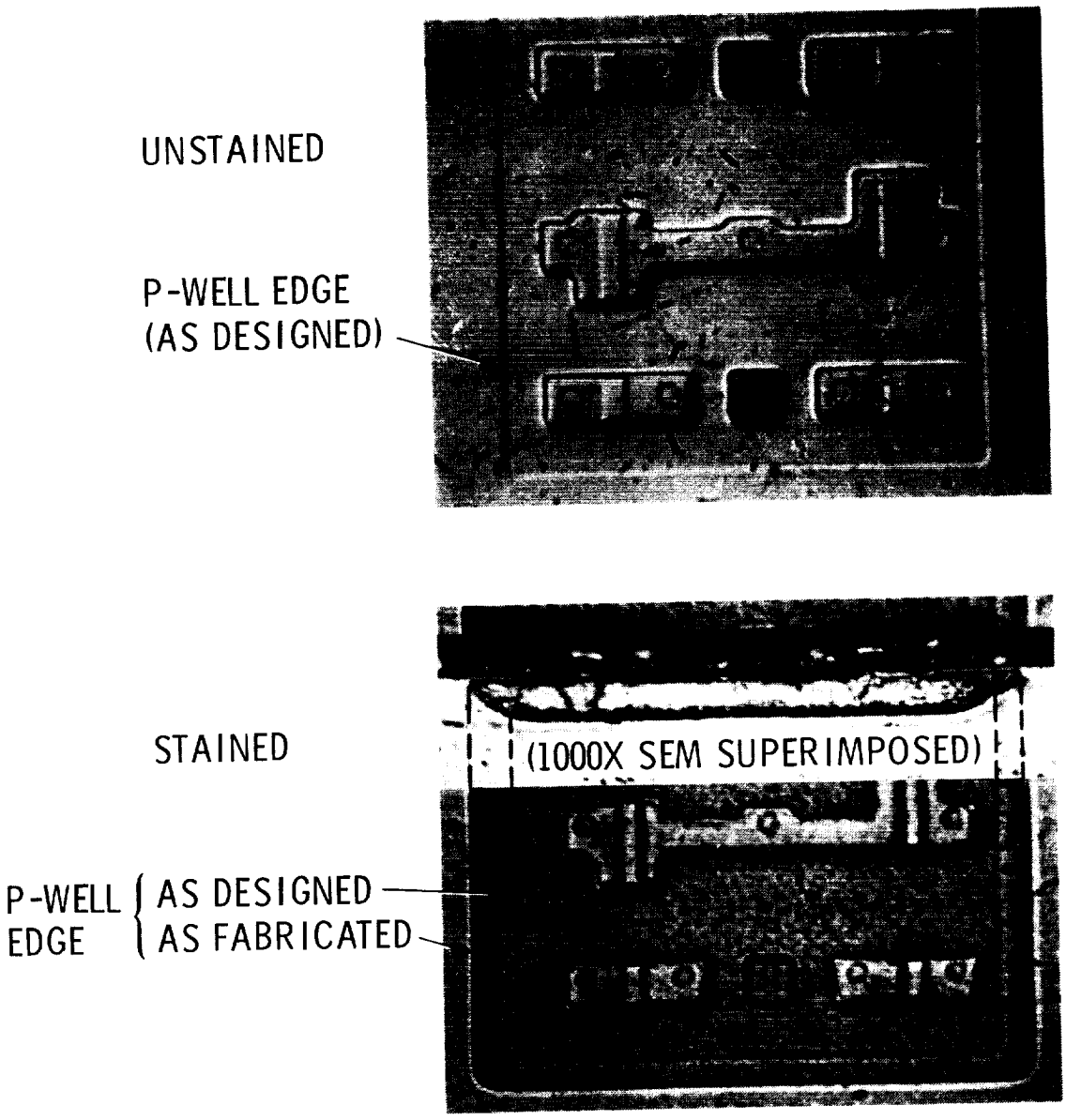
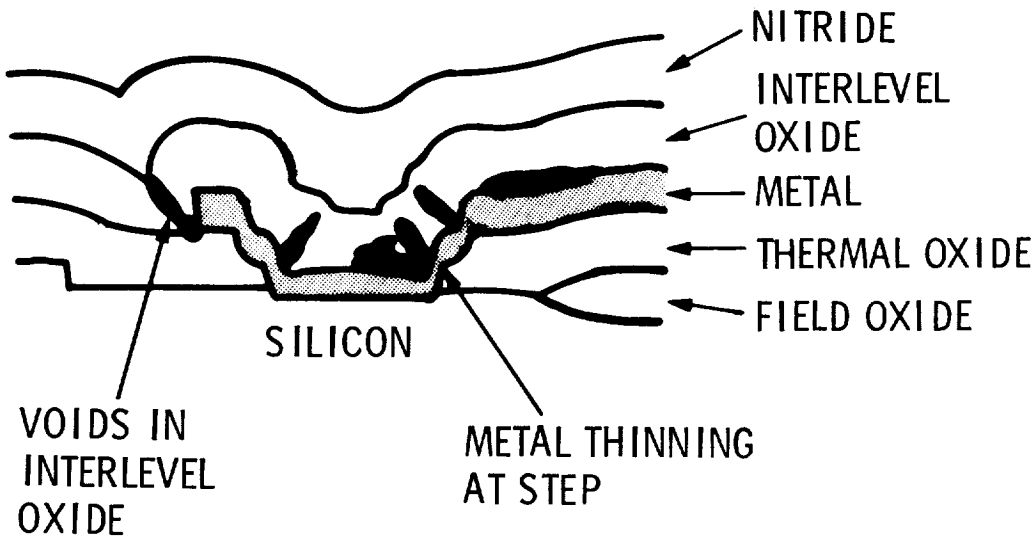
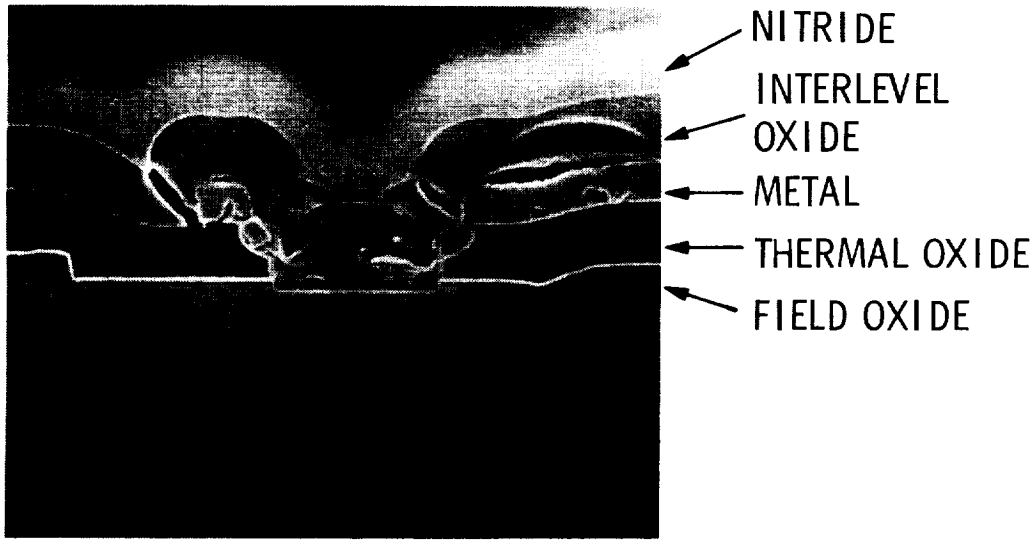


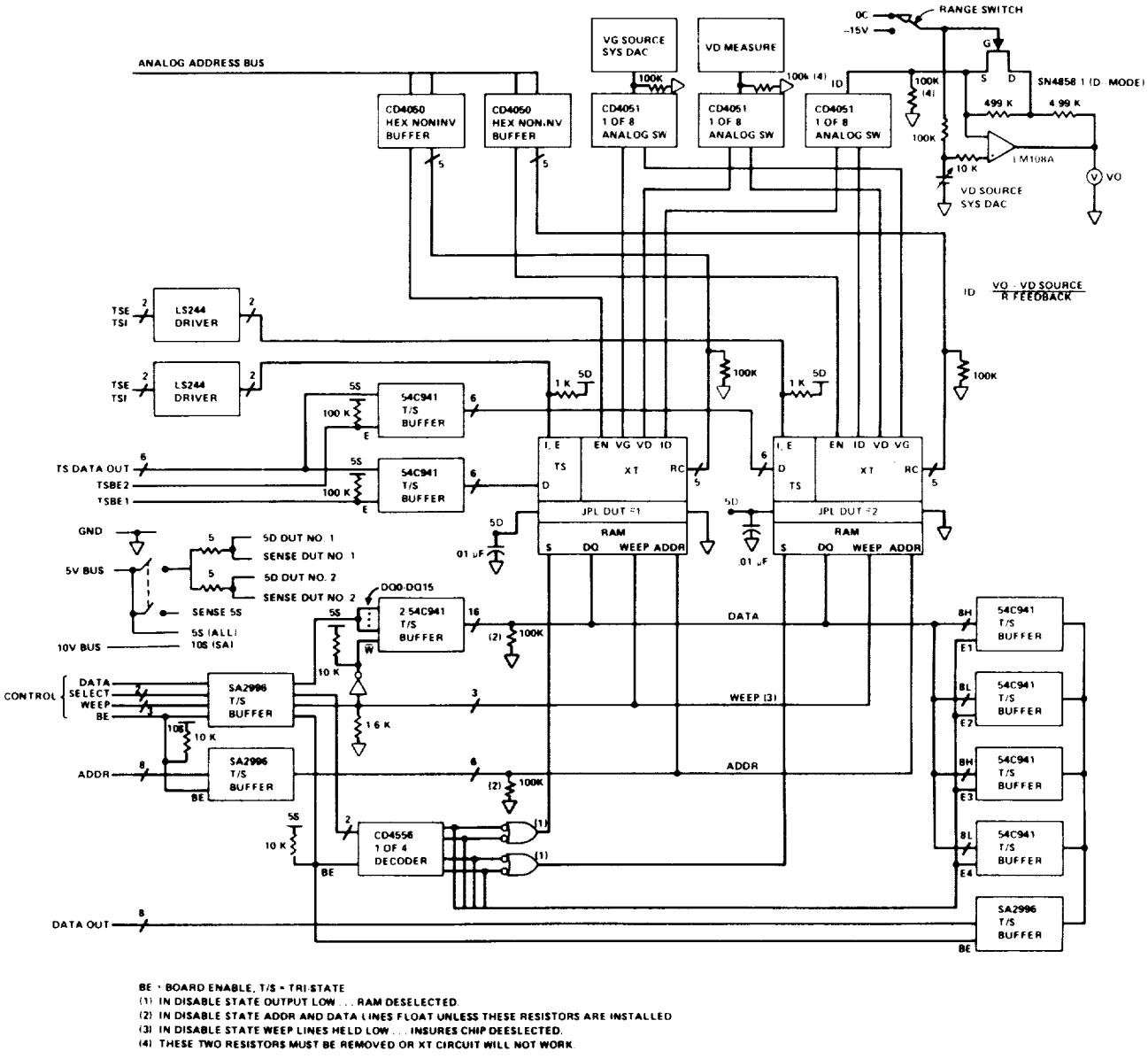
Figure 7.10: Expansion of the p-well around design boundaries in the SRAM cell. Note in the superimposed cross-section on the lower picture that there is more lateral diffusion in this process than depth.





8000X SEM MICROGRAPH
(CROSS SECTION)

Figure 7.11: Voiding in the interlevel oxide. This was not shown to have contributed to any particular failures which were seen on this run, however, it is expected that this could lead to long-term reliability problems.



BE = BOARD ENABLE, T/S = TRI-STATE
(1) IN DISABLE STATE OUTPUT LOW . . . RAM DESELECTED.
(2) IN DISABLE STATE ADDR AND DATA LINES FLOAT UNLESS THESE RESISTORS ARE INSTALLED
(3) IN DISABLE STATE WEEP LINES HELD LOW . . . INSURES CHIP DEESLECTED.
(4) THESE TWO RESISTORS MUST BE REMOVED OR XT CIRCUIT WILL NOT WORK

Figure 7.12: Circuit diagram of one pair of JPL CRRES Chips on the MEP. The notes indicate concerns, as of January, 1987, about the interface between the JPL CRRES Chips and the MEP.

Table 7.3: Chip placement and expected dose rate for the boards of the MEP.

Process	Board Placement	Dose Rate (krad(Si)/year)
A	1A, 1B	340
B, C	2A, 2B	8

and the test is performed at the SRAM's nominal operating rate of 2MHz.

Ground radiation testing was performed by Ted Smith and Don Nichols of JPL's Electronic Parts Reliability Section (Section 514). Such testing is conducted using heavy ions ($Z > 1$) to simulate the effects of primary cosmic rays on semiconductor devices [34]. These effects are Single Event Upset (SEU), a non-destructive change in state of a flip-flop and latch-up, a potentially destructive triggering of the parasitic p-n-p-n device found in all CMOS n- or p-well technologies. This test is performed using a known beam energy and angle of incidence with the ion fluence measured. The device under test is exercised by initially writing a test pattern and then continuously reading and then writing each cell, counting the number of times an upset has occurred. The test fixture used for the CRRES chip writes a pattern of all ones (or zeros) and keeps a total of how many cells have upset. From this data, along with the measured ion fluence, the upset rate and cross section are calculated. A record of specific cell upset locations was not kept in this test.

Tests were also performed at the UC Berkeley 88-inch cyclotron on CRRES chips from the foundry runs that are included in the MEP. Included in these tests were CRRES chips with both balanced and unbalanced cells. The unbalanced cell was developed to find a method for increasing SEU statistics. The data for each of these types of cells is shown in Figures 7.13 and 7.14. Work done on SEU rate modeling, along with the analysis of this data, was published in the proceedings of the 1986 Nuclear and Space Radiation Effects Conference (IEEE Transactions on Nuclear Science, December 1986) and the text of this paper is included in this report as Section 7.5.

The SEU test in the MEP will be similar to the ground test. All ones or all zeros will be written into the SRAM and the number of upsets counted. Dosimetry will be provided by the MEP, which allows for calculation of upset rate and cross section. In addition, the upset location within the SRAM will be stored, except during periods of high upset rates (i.e. solar flares).

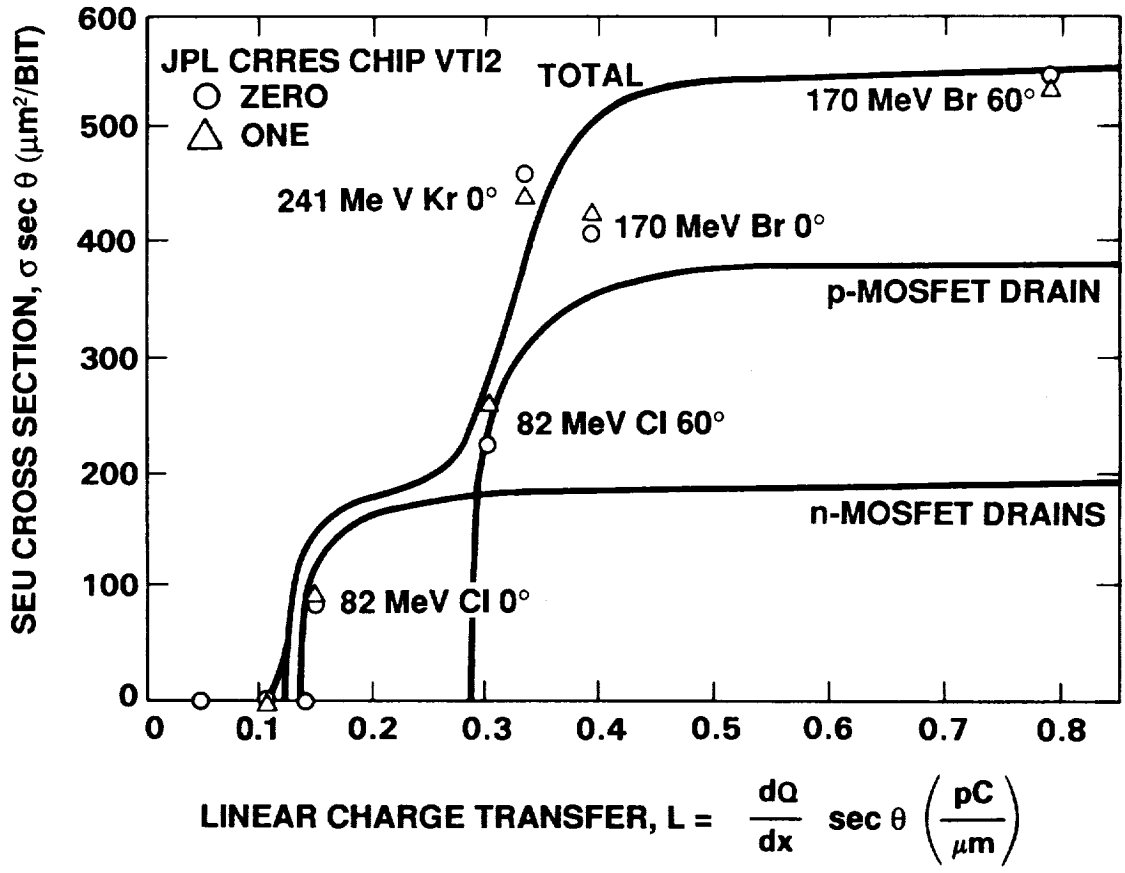


Figure 7.13: Symmetrical cell, 1k SRAM heavy ion upset response.

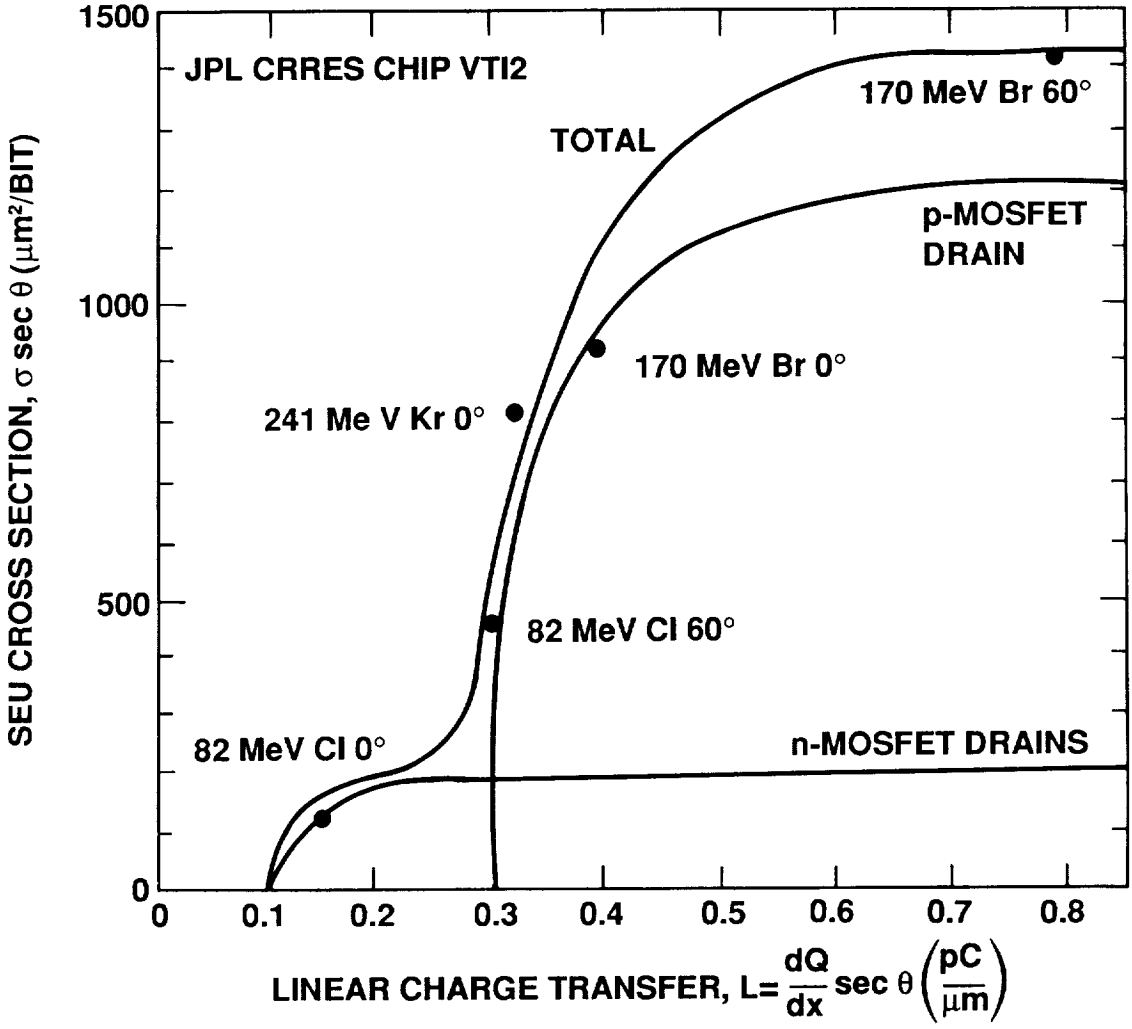


Figure 7.14: Asymmetrical cell, 1k SRAM heavy ion upset response.

7.5 Paper Presented at the 1986 Nuclear and Space Radiation Effects Conference

IEEE Transactions on Nuclear Science, Vol. NS-33, No. 6, December 1986 1637

AN ANALYTICAL METHOD FOR PREDICTING CMOS SRAM UPSETS WITH APPLICATION TO ASYMMETRICAL MEMORY CELLS

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Abstract

An analytical method was developed to predict the heavy-ion-induced upset rate of static random access memory (SRAM) cells. The method was applied to the design of a memory with asymmetrical cells where the goal was to increase the upset rate in order to increase the number of observed upsets in a space environment. The asymmetry is achieved by increasing the drain area of selected transistors in the cell. Results from the analytical model for a space environment indicate the upset rate for the experimental asymmetrical cell (17.2 upsets/1 kbit-year) will be 4.7 times larger than the upset rate for the minimum-geometry balanced cell (3.6 upsets/ 1 kbit-year). The asymmetrical SRAM was designed into a test chip intended for the Combined Release and Radiation Effects Satellite (CRRES).

Introduction

This effort is directed at characterizing the single-event-upset (SEU) rate of a static random access memory (SRAM) cell. Specially designed memory cells with enhanced upset rates are to be included in the JPL test chip[1] as a part of the Microelectronics Package (MEP) of the Combined Release and Radiation Effects Satellite (CRRES). SRAMs are the memory of choice for space flight because they have a very low upset rate, but this makes the detection of upset rates difficult. To increase the upset rate, the six-transistor cell (Fig. 1) was designed with oversize drain regions for both the pull-up Mpa and the pull-down Mnb transistors (Fig. 2). With this design, the maximum upset rate is estimated to increase from 3.6 to 17.2 upsets/1 kbitSRAM-year - an increase of over four times. The modification to the cell requires no additional processing steps.

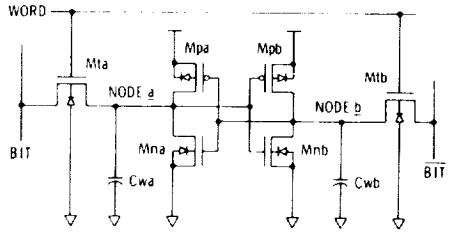

Fig. 1. Six-transistor static memory cell notation.

The upset rates were calculated from a "node set and release" approach and a state-space analysis[2] of the resulting trajectories. As seen in Fig. 3, node b is held at VDD = 5 V while node a is raised to a critical voltage for which the cell upsets. The state-space trajectories shown in Fig. 3 suggest that the critical voltage can be derived from the initial slope of the Va and Vb curves. This approach is in contrast with the usual approach of determining cell upset by injecting a current pulse at a cell node. In such an approach, one must be concerned with the nature of the current pulse.

The authors have recently learned that Jaeger et. al.[3] also derived an analytical expression for calculating the critical charge of "symmetrical" CMOS SRAM cells based on a state-space analysis. They used current pulse to simulate cell upset and their analytical expression follows the SPICE current-pulse analysis reasonably well for large current pulses. The differences between the Jaeger approach and our approach lie in our treatment of critical voltages

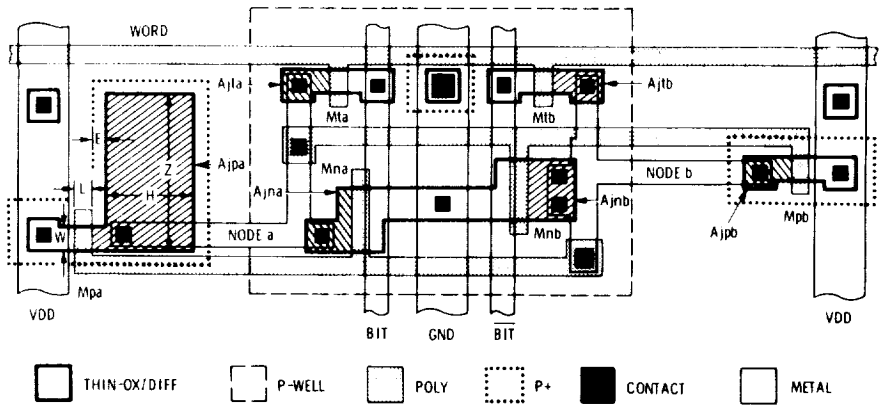

Fig. 2. Asymmetrical experimental memory cell where the SEU sensitive drains are cross-hatched. The dimensions are given in Table 2 except that Zpa = 30 μm, Hpa = 16.5 μm, and Znb = 12 μm.

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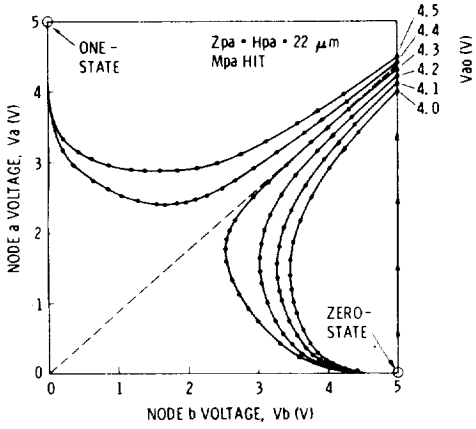

Fig. 3. SPICE derived state-space analysis of an asymmetrical six-transistor static memory cell showing the voltage trajectories after node a is raised to various initial voltages, Vao. From the SPICE analysis, the critical voltage VCpa, is 4.35 V; from the analytic model, the critical voltage, VCpa, is 4.31 V.

using a node set-and-release method rather than a current pulse method, second-order differences in the treatment of the node capacitances, and different simplifications used to create the analytical models. Also in the Jaeger model, the critical voltage includes the forward diode voltage drop, which is needed to model the current pulse. Further, the present paper extends the analysis to the treatment of asymmetrical cells.

Analytical Model

Cell upset is induced by the collision of an energetic heavy ion with a reverse-biased drain diode connected to either node a or node b. Upset occurs when the ion deposits a charge in the vicinity of the depleted diode sufficient to cause the node voltage to reach a critical voltage. When the cell is in the zero-state, defined for node a voltage (Va) low and node b voltage (Vb) high, the drain diodes of transistors Mnb, Mtb, and Mpa are reverse biased and thus are sensitive to a heavy-ion collision. When the cell is in the one-state, defined as Va = high and Vb = low, the drain diodes of transistors Mna, Mta, and Mpb are reverse biased and thus are sensitive to a heavy-ion collision.

With the cell in the zero-state (Va = low and Vb = high), the analytical expression for the critical voltage VCpa for an Mpa heavy-ion hit is derived as follows. Mpa is off and its p⁺n drain diode is reverse biased. An Mpa heavy-ion hit on the drain causes the voltage on node a to increase from its initial zero value. When the voltage increases to a critical value, VCpa, the cell will change state. Since VCpa is usually between VDD - |VTp| and VDD, the power supply bias, and since Vb = VDD, it is safe to assume that both p-channel pull-up transistors Mpa and Mpb are off so that immediately after the hit the initial node a current flows through the n-channel pull-down transistor Mna according to the relation,

$$Inao = -Ca[dVa/dt|o] \quad (1)$$

where Ca is the initial node a capacitance evaluated at Va = VCpa. Likewise the initial node b current flows through the n-channel transistor Mnb according to

$$Inbo = -Cb[dVb/dt|o] \quad (2)$$

where Cb is the initial node capacitance evaluated at Vb = VDD. From the state-space analysis, the ratio of the initial node-voltage time-derivatives for nodes a and b is approximated by

$$(dVa/dt|o)/(dVb/dt|o) = VCpa/VDD. \quad (3)$$

Since the nodal voltages are either at or near VDD, the n-channel currents are given by the saturation region expressions. For Mna,

$$Inao = Bna(VDD - VTna)^2 \quad (4)$$

and for Mnb,

$$Inbo = Bnb(VCpa - VTnb)^2 \quad (5)$$

where VTqi is the threshold voltage, Bqi = KPqWqi/(2Lqi), Wqi is the channel width, Lqi is the channel length, KPq = U0qC0, U0q is the channel mobility, and C0 is the gate-oxide capacitance per unit area. The notation indicates that a q-type diode (q = p for p⁺n diodes and q = n for n⁺p diodes) is connected to the i-th node (i = a or b). Combining the above equations we have the transcendental equation

$$(VCpa - VTnb)^2 = \frac{BnaCbVDD}{BnbCaVCpa}(VDD - VTna)^2. \quad (6)$$

This equation was solved for VCpa using a computer-aided iteration scheme.

The dependence of VCpa on the various parameters can be seen by taking the square root of the above equation. Rearrangment of the resulting expression leads to

$$VCpa = VTnb + (VDD - VTna)\sqrt{\frac{WnaLnbCbVDD}{WnbLnaCaVCpa}}. \quad (7)$$

This expression can be simplified for Wna = Wnb and Lna = Lnb. For VCpa = VDD inside the square root term,

$$VCpa = VTnb + (VDD - VTna)\sqrt{\frac{Cb}{Ca}}. \quad (8)$$

From this expression it can be seen that VCpa depends on the n-channel threshold voltages VTna and VTnb and the nodal capacitances Ca and Cb. For a symmetrically designed cell where Ca = Cb and VTna = VTnb, there is no dependence of VCpa on the threshold voltage or nodal capacitance; however, any imbalance in the cell design or any differential degradation in the threshold voltages will lead to a change in VCpa that will make the cell easier or harder to upset.

With the cell in the zero-state (Va = low and Vb = high), the critical voltage VCnb for an Mnb heavy ion hit is derived in a manner similar to the derivation for VCpa given above. For Va = 0, the critical voltage VCnb is the voltage required to

cause cell upset. From the state-space analysis, the ratio of the initial node-voltage time-derivatives for nodes a and b is approximated by

$$(dVb/dt|o)/(dVa/dt|o) = (VDD - VCnb)/VDD. \quad (9)$$

Since both node voltages are low, the n-channel transistors are off and the p-channel transistors are attempting to pull the nodes high. The initial saturation current through Mpa is

$$Ipao = Ca[dVa/dt|o]$$
$$= Bpa(VDD - VCnb - |VTpa|)^2 \quad (10)$$

and through Mpb is

$$Ipbo = Cb[dVb/dt|o|$$
$$= Bpb(VDD - |VTpb|)^2. \quad (11)$$

Combining the above equations gives for VCnb

$$(VDD - VCnb - |VTpa|)^2 =$$
$$\frac{BpbCaVDD}{BpaCb(VDD - VCnb)} (VDD - |VTpb|)^2 \quad (12)$$

By a similar analysis, the critical voltages for the one-state (Va = high and Vb = low) can be determined. For a heavy-ion hit on Mpb, the critical voltage VCpb is given by

$$(VCpb - VTna)^2 = \frac{BnbCaVDD}{BnaCbVCpb} (VDD - VTnb)^2. \quad (13)$$

For a heavy-ion hit on Mna, the critical voltage VCna is given by

$$(VDD - VCna - |VTpb|)^2 =$$
$$\frac{BpaCbVDD}{BpbCa(VDD - VCna)} (VDD - |VTpa|)^2. \quad (14)$$

In the analytical results presented in this paper, the node a capacitance is given by[4]

$$Ca = CDna + CDta + CDpa + CGnb$$
$$+ CGpb + CWPSa + CWMSa \quad (15)$$

and the node b capacitance is given by

$$Cb = CDnb + CDtb + CDpb + CGna$$
$$+ CGpa + CWPSb + CWMSb \quad (16)$$

where CDqi is the diode capacitance, CGqi is the gate-oxide capacitance, CWPSi is the poly-to-silicon wire capacitance, and CWMSi is the metal-to-silicon wire capacitance. The capacitance of a one-sided step junction[5] is given by

$$CDqi = CJOqAJqi/(1 + Vqi/PBq)^{MJq}$$
$$+ CEOqAEqi/(1 + Vqi/PBq)^{MEq} \quad (17)$$

where CJOq is the planar capacitance per unit area, AJqi is the planar area, MJq is the planar capacitance exponent, CEOq is the edge capacitance per unit length, AEqi is the length of the diode periphery, MEq is the edge capacitance exponent, and PBq is the diode built-in potential barrier. In the above expression, the applied junction bias Vqi for p+n diodes is given by

$$Vni = Vti = VCni \quad (18)$$

and for n+p diodes is given by

$$Vpi = VDD - VCpi \quad (19)$$

where Vqi is positive for reverse-biased diodes and negative for forward-biased diodes. The diode area is given by

$$AJ = W*E + H*Z \quad (20)$$

and the length of the diode edge for Z > W is

$$AE = 2E + 2H + 2Z - W \quad (21)$$

and for Z < W,

$$AE = 2E + 2H - W \quad (22)$$

where the diode dimensional parameters E, H, and Z are shown in Fig. 2. The gate-oxide capacitance has a complex voltage dependence, but in this effort this capacitance is given simply by the fixed value

$$CG = CO*W*L. \quad (23)$$

The poly-to-silicon wire capacitance is given by

$$CWPS = CPS*APS \quad (24)$$

where CPS is the capacitance per area and APS is the capacitor area. The metal-to-silicon wire capacitance is given by

$$CWMS = CMS*AMS \quad (25)$$

where CMS is the capacitance per area and AMS is the capacitor area.

The upset rate was determined from the Petersen equation[6], which is based on a 10-percent worst case differential cosmic-ray spectrum. The upset rate in upsets per bit-day for a heavy-ion hit on a q-type reversed-biased diode on the i-th node is given by

$$Rqi = 5E\text{-}10\ AJqiXCq^2/QCqi^2 \quad (26)$$

where AJ is the diode area in square micrometers and XC is the carrier collection depth in micrometers. For n+p diodes, XC is given by[7]

$$XCn = XCt = (1 + UP/UN)XDn \quad (27)$$

and for p+n diodes by

$$XCp = (1 + UN/UP)XDp \quad (28)$$

where UN and UP are the electron and hole bulk mobilities. In this study the bulk mobility ratio UN/UP was taken as 3. The junction depletion width for a one-sided step junction with full power-supply bias is given by

$$XDq = (EPSILONs/CJOq)\ (1 + VDD/PBq)^{MJq} \quad (29)$$

where the dielectric constant for silicon is EPSILONs = 11.7 x 8.86E-14F/cm. In the above equations the critical charge in picocoulombs is given by

$$QCni = QCti = Ci(VDD - VCni) \quad (30)$$

and

$$QCpi = CiVCpi \tag{31}$$

where Ci is the nodal capacitance in picofarads and VCni and VCpi are the nodal voltages in volts. This expression for the critical charge is based on the incremental charge where dQ = CdV and the VdC term is small and assumed to be zero.

The upset rate for a memory cell in the zero-state is

$$Rzero = Rnbtbpa = Rnb + Rtb + Rpa \tag{32}$$

where the zero-state is defined as node a low and node b high. The upset rate for a memory cell in the one-state is:

$$Rone = Rnatapb = Rna + Rta + Rpb \tag{33}$$

where the one-state is defined as node a high and node b low.

Calculated Results

In these calculations the model parameters given in Table 1 and the cell geometry parameters given in Table 2 were used in the solution of Eqs. (6), (12), (14), and (18). The results for the state-space analysis are listed in Figs. 4 through 7. The drain areas were assumed to be square.

For asymmetrical cells, the Rzero values given in Fig. 4 indicate that the upset rate can vary between 2 and 20 upsets/1 kbitSRAM-year. For the minimum-geometry cell (the square symbol), Rzero = 3.6 upsets/1 kbitSRAM-year, and for the experimental cell (the circle symbol), Rzero = 17.2 upsets/1 kbitSRAm-year. Rone values (Fig. 5) indicate that Rone can vary from 0.7 to 3.6 upsets/1 kbitSRAM-year. The Rzero/Rone ratio (Fig. 6) is always greater than one and for some geometries can be greater than a factor of 10. For the experimental cell, the ratio is 11.3.

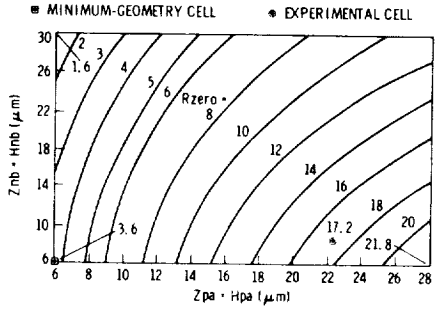

Fig. 4. Calculated geometrical dependence for the zero-state upset rate (in upsets/1 kbitSRAM-year) for an asymmetrical 3-μm CMOS/Bulk SRAM cell with a bias of 5 V, using the Hu collection depth, and based on the 10-percent worst-case differential cosmic-ray spectrum.

For balanced cells, the Rzero = Rone values (Fig. 7) indicate the upset rate can vary between 1 and 9 upsets/1 kbitSRAM-year. Pickel[8] has also shown that the upset rate depends on the relative area of the cell drain diodes. For a four-fold increase in the area, he showed a 40-percent decrease in the upset rate. In essence, his curve emulates the behavior along a vertical line drawn in Fig. 7.

The decrease in upset rate is an important result in consideration of SEU resistance. Clearly the greatest increase in upset rates is achieved with the asymmetrical cell and not the balanced cell.

Experimental Results

Preliminary ground tests have been performed at the 88-inch cyclotron at Berkeley, California, using a 240-MeV krypton beam. For a SRAM with minimum-

Table 1. 3-μm CMOS/Bulk Model Parameters

Parameter (units)	Mn	Mp	Parameter (units)	Value
CJO(fF/μm²)	= 0.3	0.15	VDD(V)	= 5.0
MJ	= 0.5	0.5	CO(fF/μm²)	= 0.69
CEO(fF/μm)	= 0.3	0.2	CPS(fF/μm²)	= 0.04
ME	= 0.25	0.25	CMS(fF/μm²)	= 0.02
PB(V)	= 0.6	0.6		
XD(μm)	= 1.05	2.11		
XC(μm)	= 1.40	8.44		
VTa(V)	= 0.75	-0.75		
VTb(V)	= 0.75	-0.75		
KP=UO*CO(μA/V²)	= 50	20		

Table 2. Minimum Geometry 1-kbitSRAM Transistor Geometries

Transistor	W(μm)	L(μm)	E(μm)	Z(μm)	H(μm)	AJ(μm²)	AE(μm)	AG(μm²)
Mpa	4.5	3.0	3.0	6.0	6.0	49.5	25.5	13.5
Mna	12.0	3.0	3.0	6.0	6.0	72.0	30.0	36.0
Mta	4.5	3.0	3.0	6.0	6.0	49.5	25.5	0.0
Mpb	4.5	3.0	3.0	6.0	6.0	49.5	25.5	13.5
Mnb	12.0	3.0	3.0	6.0	6.0	72.0	30.0	36.0
Mtb	4.5	3.0	3.0	6.0	6.0	49.5	25.5	0.0
APSa(μm²) = 343		AMSa = 272		APSb = 343		AMSb = 272		

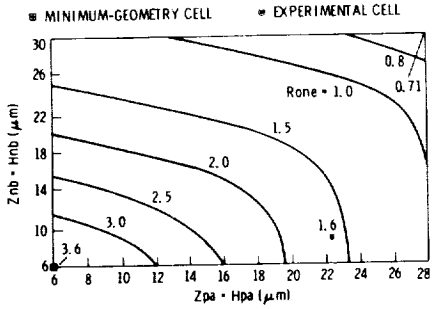

Fig. 5. Calculated geometrical dependence for the one-state upset rate (in upsets/1 kbitSRAM-year) for an asymmetric 3-μm CMOS/Bulk SRAM cell with a bias of 5 V, using the Hu collection depth, and based on the 10-percent worst-case differential cosmic-ray spectrum.

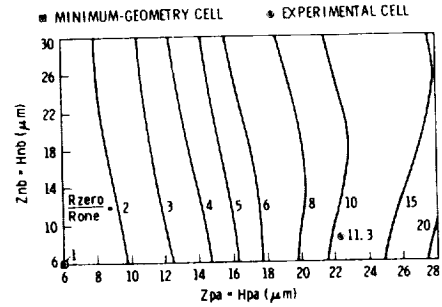

Fig. 6. Calculated geometrical dependence for the ratio of the zero-to-one upset rate for an asymmetrical 3-μm CMOS/Bulk SRAM cell with a bias of 5 V, using the Hu collection depth, and based on the 10-percent worst-case differential cosmic-ray spectrum.

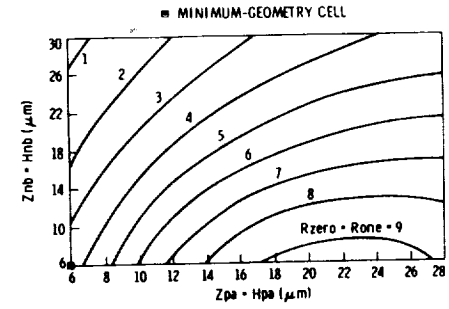

Fig. 7. Calculated geometrical dependence for the upset rate (in upsets/1 kbitSRAM-year) for a symmetrical 3-μm CMOS/Bulk SRAM cell with a bias of 5 V, using the Hu collection depth, and based on the 10-percent worst-case differential cosmic-ray spectrum.

geometry symmetrical cells, an upset rate of about 3200 upsets for 1 million normally incident ions per cm^2 was observed with no difference in upset rate between the zero- and one-states. For the asymmetrical SRAM with the same incident beam, the zero-state showed about 6800 upsets/1,000,000 normally incident ions per cm^2 while the one-state showed about 2400 upsets/1,000,000 normally incident ions per cm^2, giving a Rzero/Rone = 2.8. This result is consistent with the cell area ratio [(Anb + Atb + Apa)/(Ana + Ata + Apb)] = 666/170 = 3.9.

Conclusion

Simple analytical expressions have been developed to guide the design of static RAM cells. The expressions allow a quick exploration of the dependence of upset rate on geometry. For the geometries and technology (3-μm CMOS/Bulk) considered in this effort, the upset rates can be varied from a low of 0.71 to a high of 21.8 upsets/1 kbitSRAM-year.

Acknowledgements

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References

[1] M. G. Buehler, B. T. Moore, and R. H. Nixon, "Parameter Extraction from Spaceborne MOSFETs," IEEE Trans. on Nucl. Sci., NS-32, pp. 4237-4243, December 1985.

[2] L. A. Glasser and D. W. Dobberpuhl, The Design and Analysis of VLSI Circuits, Reading, MA: Addison-Wesley, 1985, Chapter 5.

[3] R. C. Jaeger, R. M. Fox, S. E. Diehl, "Analytical Expressions for the Critical Charge in CMOS Static RAM Cells," IEEE Trans. on Nucl. Sci., Vol. NS-30, pp. 4616-4619, December 1983.

[4] S. M. Kang, "A Design of CMOS Polycells for LSI Circuits," IEEE Trans. on Circuits and Systems, Vol. CAS-28, pp. 838-843, 1981.

[5] A. Vladimirescu and S. Liu, "The Simulation of MOS Integrated Circuits Using SPICE 2," Memorandum UCB/ERL M80/7, Berkeley: Electronics Research Laboratory, University of California, October 1980.

[6] E. L. Petersen, J. B. Langworthy, and S. E. Diehl, "Suggested Single Event Upset Figure of Merit," IEEE Trans. on Nucl. Sci. Vol. NS-30, pp. 4533-4539, December 1983.

[7] C. Hu, "Alpha-Particle-Induced Field and Enhanced Collection of Carriers," IEEE Electron Device Letters, Vol. EDL-3, pp. 31-34, February 1982.

[8] J. C. Pickel, "Single Event Upset Mechanisms and Predictions," Tutorial Short Course, IEEE 1983 Nuclear and Space Radiation Effects Conference, July, 1983.

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7.6 MOSFET Matrix

The MOSFET matrix is used for accurate measurement of individually addressed transistors to allow evaluation of CMOS transistor parameters. Geometry dependence of several of these parameters requires MOSFETs with at least four W/L ratios which, for statistical purposes, are each repeated three or four times in the matrix.

Two distinct modes of matrix operation are controlled by an enable pin (XT EN); see Figure 7.15. When XT EN is low, the matrix is in standby and the transistors are biased in the worst case condition for radiation damage. The gates of all transistors are connected to VDD (VGS for the n-MOSFET is 5.0 V and VGS for the p-MOSFET is 0.0 V) and the drains are floated. This forces radiation-induced positive charge to the silicon dioxide-silicon interface, where it has the maximum effect on threshold voltage shifts. When the matrix is enabled, all devices except the device addressed are in a non-conducting state and transmission gates direct the gate voltage (XT VG) to the transistor under test. Drain current is forced through a common pin (XT ID) and the drain voltage (XT VD) is measured by Kelvin connection via transmission gates. A common p-well connection (XT PWELL) is available for the evaluation of body effect in n-channel transistors, allowing the well of the transistor under test to be biased. A common connection to the sources of all p-MOSFET transistors (XT VPS) is used to evaluate the p-MOSFET body effect. To accomplish this, VDD, which is tied to chip substrate, is raised above 5 V, while the source is held at 5 V during the test.

The measurements require an HP4141B, which has four source/monitor units, two voltage sources, and two voltage monitors; hence the entire measurement can be conducted with one instrument. The matrix addressing circuitry is powered by chip VDD. The pin assignments for the CRRES chip during and between irradiation are shown in Section 7.10. The time required for a complete (ground) test of the matrix is 35 minutes. The measurement configuration in the MEP is simplified (Figure 7.15) due to limitations on the amount of ancillary circuitry that can be flown in space.

During the report period, a sample CRRES chip was irradiated using a Cobalt-60 source. The radiation sequence is shown in Table 7.4. Time between irradiations was less than 60 minutes. Irradiation, electrical testing, and annealing were done at room temperature. The chip was mounted in a 64-pin package; the package lid remained on during irradiation and electrical testing. The electrical data was analyzed with the parameter extraction program, JMOSFIT [35].

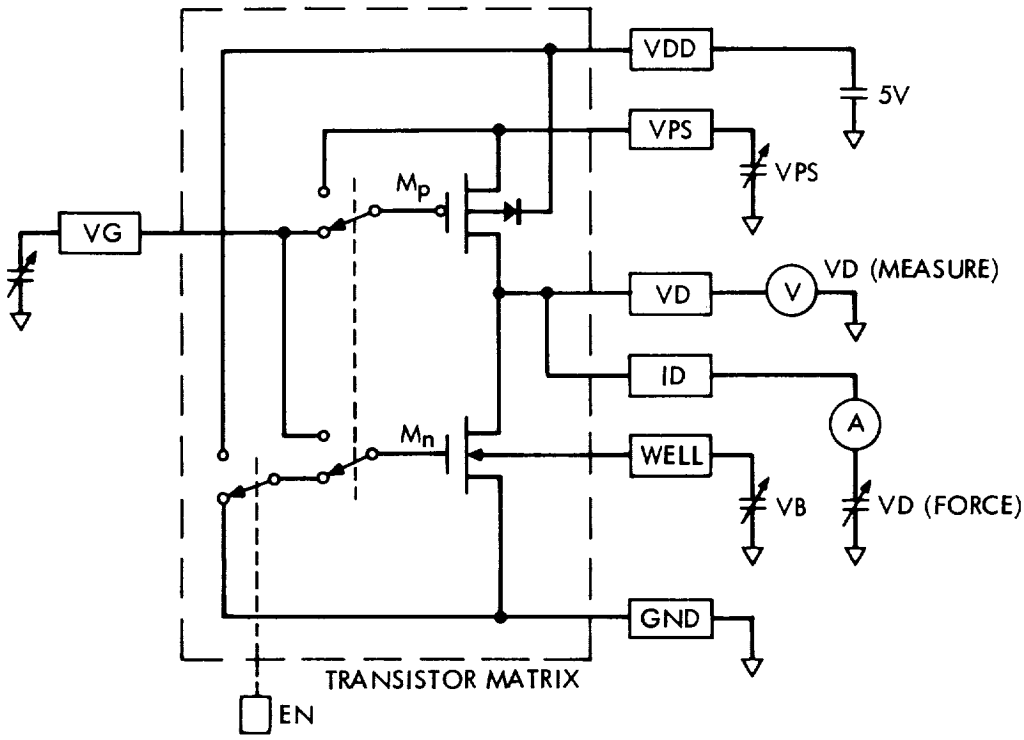


Figure 7.15: Transistor measurement configuration.

Table 7.4: CRRES Chip Cobalt-60 Irradiation.

LEVEL NO.	FLUX (rad/sec)	FLUENCE (krad (Si))	CUMULATIVE FLUENCE (krad (Si))	TIME (min)	DISTANCE (cm)
1	2.5	1	1	6.67	55.7
2	2.5	1	2	6.67	55.7
3	2.5	3	5	20.00	55.7
4	2.5	5	10	33.33	55.7

DEVICE TYPE: CRRES
TEST DATE : 06/10/86

All 32 transistors in the matrix were tested between irradiations, and a total of 252 data points was acquired for each transistor. The gate voltage was stepped from 5.0 to 0.25 V in 0.25 V decrements and then to 0.05 V for the final data point; the drain voltage was stepped from 5.0 to 1.0 V in 0.5 V decrements and then to 0.6, 0.2, and 0.05 V. Four characteristic transistor curves were plotted before and after irradiation for each transistor and are shown in Figure 7.16.

The overall chip leakage current is shown versus total Cobalt-60 dose in Figure 7.17. The leakage current increased from 1 nA at 0 krad(Si) to 8 μA at 10 krad(Si).

Table 7.5 is a row by row comparison of transistors; most parameters are in close agreement between devices. The parameters with the largest percent errors are the geometrical coefficients KWG, KWGB, KWD, KWL, HO, and LO. The primary parameters, such as KP, VTO, and GAMMA agree to within 5 percent.

Tables 7.6 and 7.7 show that the results display the expected behavior for relatively low radiation doses. That is, the change in the threshold voltage, VTO, for both n- and p-MOSFETs, indicates a buildup of positive charge in the oxide. Note that the absolute value of the (negative) threshold voltage is listed in Table 7.7 for the p-MOSFETs. Parameters expected to be insensitive to oxide charge are KP, GAMMA, DO, THETA, KLT, RW, EO, KLE, LO, KLL, and KWL; with the exception of DO and KWL for the n-MOSFETs, this is evidenced in the results.

Threshold voltage for n- and p-MOSFETs for W/L = 6 μm/3 μm are plotted versus total dose in Figure 7.18. The slope and y-intercept were calculated using least-squares fitting.

7.7 Timing Sampler

The CRRES Chip timing sampler [2] provides a substantially improved method for the direct measurement of on-chip circuit delay. The timing sampler is not afflicted with the problem of higher harmonic oscillation modes, as is the ring oscillator, since delays are directly measured using externally generated transitions. This results in repeatable and accurate measurements, and therefore, a high degree of confidence in the results.

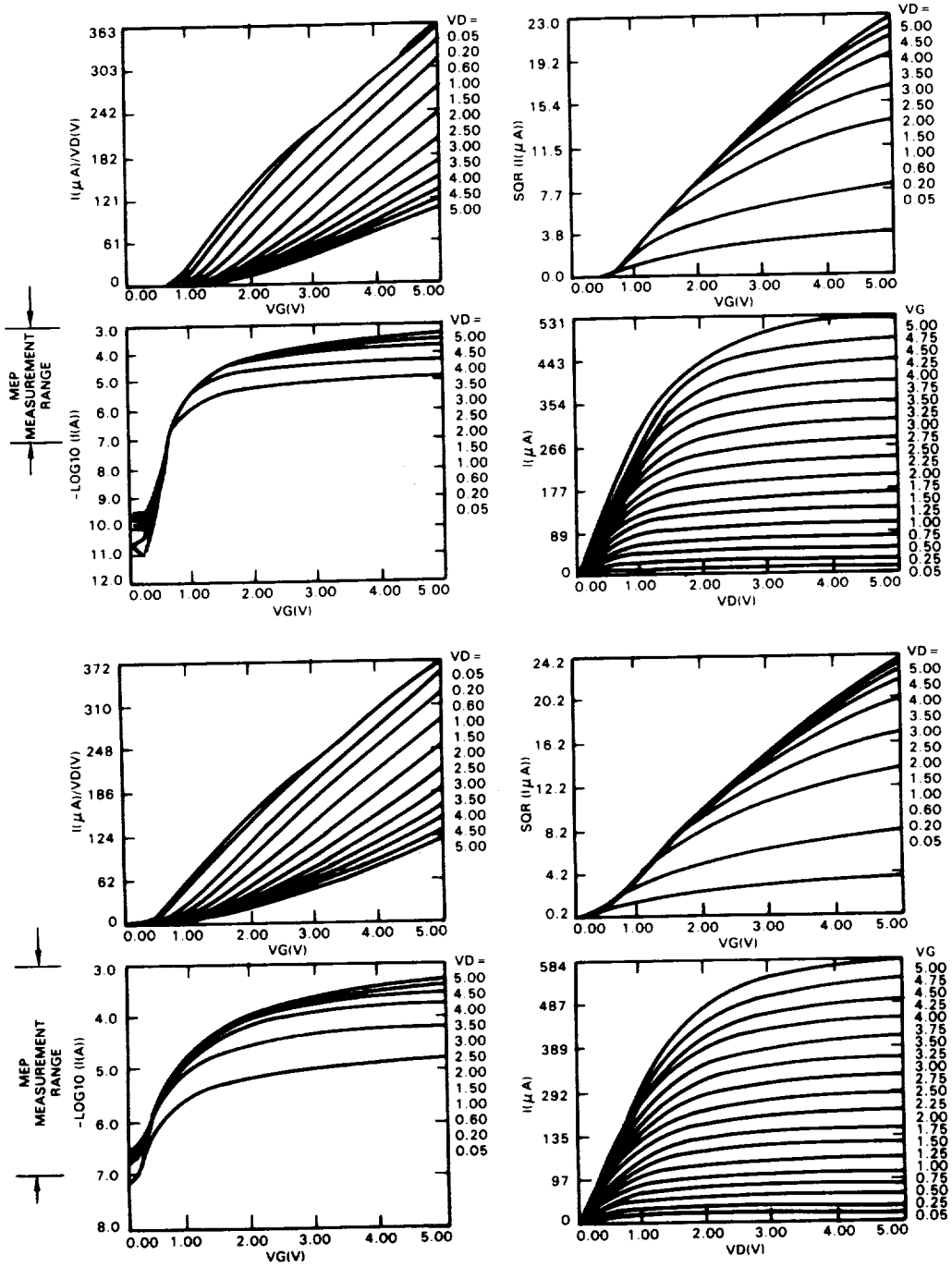


Figure 7.16: n-Channel MOSFET pre-irradiation curves (top) and post-irradiation curves (bottom) after 10 krad(Si) at 2.5 rad(Si)/sec).

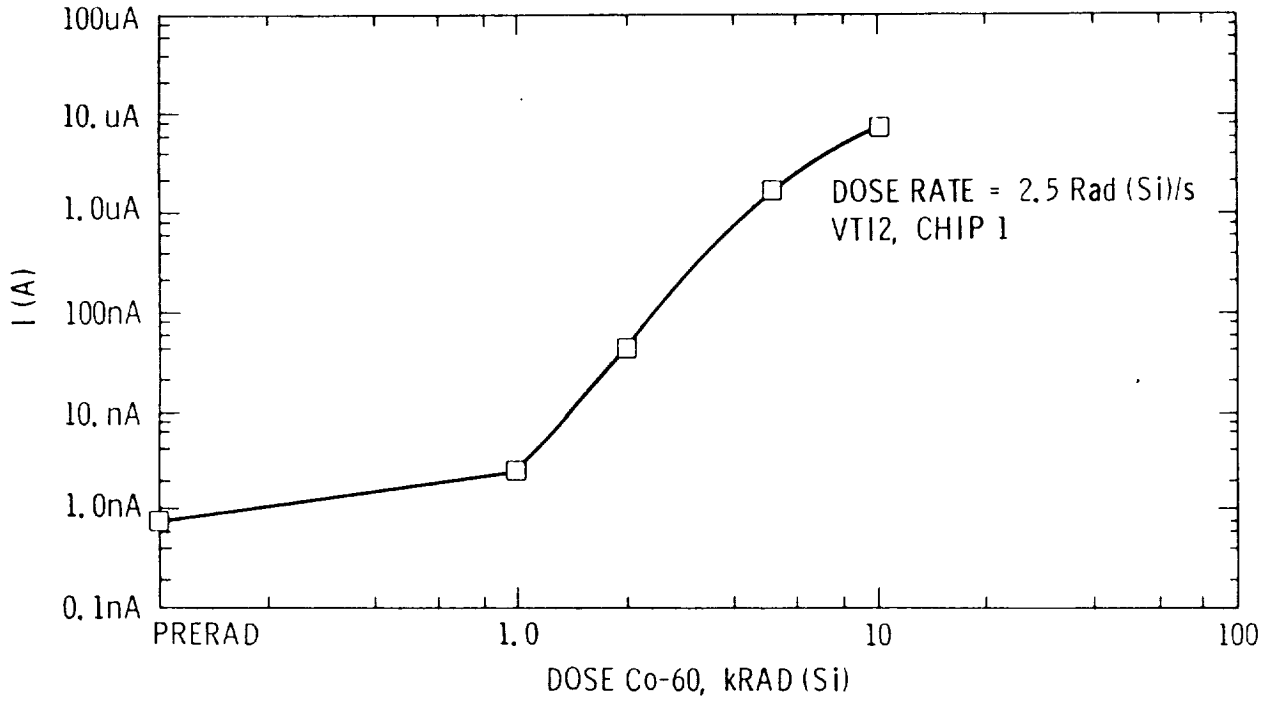


Figure 7.17: CRRES Chip leakage versus total dose.

Table 7.5: Comparison of n-MOSFET Matrix Test Results.

	TRANSISTOR PARAMETER	ROW #2	ROW #3	%	ROW #4	%
BETA:	KP(uA/V^2)	50.84	48.81	4	50.46	1
	$DELTA\,W$(μm)	1.290	0.797	38	1.353	-5
	$DELTA\,L$(μm)	1.018	0.931	9	1.091	-7
THRESHOLD:	$VT0$(V)	0.715	0.679	5	0.719	-1
	PSI(V)	0.069	0.027	61	0.066	4
	$GAMMA$(V$^{0.5}$)	0.834	0.842	-1	0.842	-1
	KLG(V $\times$ μm)	0.053	0.077	-45	0.051	4
	$KLGB$(μm)	0.060	0.06	0	0.074	-23
	KWG(V $\times$ μm)	-.054	0.24	544	-.062	-15
	$KWGB$(μm)	0.104	0.084	-71	0.121	-16
DELTA:	$D0$(V$^{0.5}$)	0.299	0.331	-11	0.315	-5
	KLD(μm)	0.694	0.723	-4	0.636	8
	KWD(μm)	0.272	0.112	59	0.138	49
TAU:	$THETA$(1/V)	0.039	0.049	-26	0.044	-13
	KLT(μm/V)	0.074	0.058	22	0.065	12
	RW(Ω $\times$ μm)	725.41	596.28	18	646.6	11
ETA:	$H0$(1/V)	0.047	0.049	4	0.049	4
	KLH(μm/V)	0.309	0.254	18	0.419	-36
EPSILON:	$E0$(1/V)	0.056	0.056	0	0.057	2
	KLE(μm/V)	0.586	0.592	-1	0.566	3
LAMBDA:	$L0$(1/V)	0.005	0.002	60	0.004	20
	KLL(μm/V)	0.100	0.108	-8	0.099	1
	KWL(μm/V)	0.021	0.001	52	0.017	19

VB = 0, -2.5 V; PHI = 0.6 V

TRANSISTOR GEOMETRIES: W(μm)/L(μm) = 9/3, 9/9, 6/9, 6/3

Table 7.6: n-MOSFET Matrix Cobalt-60 Radiation Test Results.

	TRANSISTOR	TOTAL DOSE (krad (Si))						
	PARAMETER	0k	1k	%	5k	%	10k	%
BETA:	KP(uA/V^2)	50.84	49.54	3	53.40	-5	49.23	3
	$DELTA\,W(\mu m)$	1.290	1.049	19	1.437	-11	1.002	22
	$DELTA\,L(\mu m)$	1.018	1.054	-4	0.998	2	0.996	2
THRESHOLD:	$VT0$(V)	0.715	0.681	5	0.612	14	0.421	41
	PSI(V)	0.069	0.033	52	-.031	145	-.287	516
	$GAMMA$(V$^{0.5}$)	0.834	0.837	-4	0.83	5	0.914	-10
	KLG(V $\times$ μm)	0.053	0.049	8	0.071	-34	-.028	153
	$KLGB(\mu m)$	0.060	0.074	-23	0.067	-12	0.126	-110
	KWG(V $\times$ μm)	-.054	-.045	-17	-.216	300	-.301	457
	$KWGB(\mu m)$	0.104	0.133	-28	0.1	4	0.114	-10
DELTA:	$D0$(V$^{0.5}$)	0.299	0.3	0	0.33	-10	0.426	-43
	$KLD(\mu m)$	0.694	0.635	9	0.744	-7	0.926	-33
	$KWD(\mu m)$	0.272	0.388	-43	0.248	9	0.245	10
TAU:	$THETA$(1/V)	0.039	0.035	10	0.045	-15	0.04	-3
	$KLT(\mu m/V)$	0.074	0.081	-10	0.062	16	0.07	5
	$RW(\Omega \times \mu m)$	725.41	813.2	-12	579.25	20	707.2	3
ETA:	$H0(1/V)$	0.047	0.105	-123	0.106	-126	0.206	-338
	$KLH(\mu m/V)$	0.309	0.528	-71	0.341	-10	0.194	37
EPSILON:	$E0(1/V)$	0.056	0.051	9	0.057	-2	0.058	-4
	$KLE(\mu m/V)$	0.586	0.596	-2	0.593	-1	0.603	-3
LAMBDA:	$L0(1/V)$	0.005	0.003	40	0.005	0	0.005	0
	$KLL(\mu m/V)$	0.100	0.098	2	0.103	-3	0.103	-3
	$KWL(\mu m/V)$	0.021	0.001	52	0.019	10	0.012	43

VB = 0, -2.5 V; PHI = 0.6 V

TRANSISTOR GEOMETRIES: $W(\mu m)/L(\mu m)$ = 9/3, 9/9, 6/9, 6/3

Table 7.7: p-MOSFET Matrix Cobalt-60 Radiation Test Results.

	TRANSISTOR	TOTAL DOSE (krad (Si))						
	PARAMETER	0k	1k	%	2k	%	5k	%
BETA:	KP(uA/V^2)	18.03	18.61	-3	18.41	-2	17.23	4
	$DELTA\ W(\mu m)$	0.527	1.075	-104	0.898	-71	0.835	-58
	$DELTA\ L(\mu m)$	1.112	1.026	8	1.082	3	1.209	-9
THRESHOLD:	$VT0$(V)	0.776	0.809	-4	0.835	-8	0.893	-15
	PSI(V)	0.425	0.462	-9	0.502	-18	0.541	-27
	$GAMMA$(V$^{0.5}$)	0.453	0.448	1	0.431	5	0.455	-0.4
	KLG(V $\times$ μm)	0.081	0.087	-7	0.067	17	0.052	36
	$KLGB(\mu m)$	0.117	0.108	8	0.108	8	0.098	16
	KWG(V $\times$ μm)	0.159	0.163	-3	0.189	-19	0.358	-125
	$KWGB(\mu m)$	0.104	0.094	10	0.122	-17	0.073	30
DELTA:	$D0$(V$^{0.5}$)	0.25	0.204	18	0.230	8	0.201	20
	$KLD(\mu m)$	0.428	0.482	-13	0.414	3	0.215	50
	$KWD(\mu m)$	0.425	0.116	73	0.009	98	-.191	145
TAU:	$THETA$(1/V)	0.099	0.106	-7	0.113	-14	0.103	-4
	$KLT(\mu m/V)$	0.073	0.047	36	0.049	33	0.053	27
	$RW(\Omega \times \mu m)$	2038	1270	38	1323	35	1551	24
ETA:	$H0$(1/V)	0.47	0.198	58	0.258	45	0.1	79
	$KLH(\mu m/V)$	0.845	0.625	26	0.741	12	1.326	-57
EPSILON:	$E0$(1/V)	0.043	0.043	0	0.036	16	0.034	21
	$KLE(\mu m/V)$	0.313	0.283	10	0.268	14	0.273	13
LAMBDA:	$L0$(1/V)	0.018	0.014	22	0.013	28	0.016	11
	$KLL(\mu m/V)$	0.174	0.187	-7	0.184	-6	0.174	0
	$KWL(\mu m/V)$	0.039	0.037	5	0.028	28	0.032	18

VB = 0, 2.5 V; PHI = 0.6 V
TRANSISTOR GEOMETRIES: $W(\mu m)/L(\mu m)$ = 9/3, 9/9, 6/9, 6/3

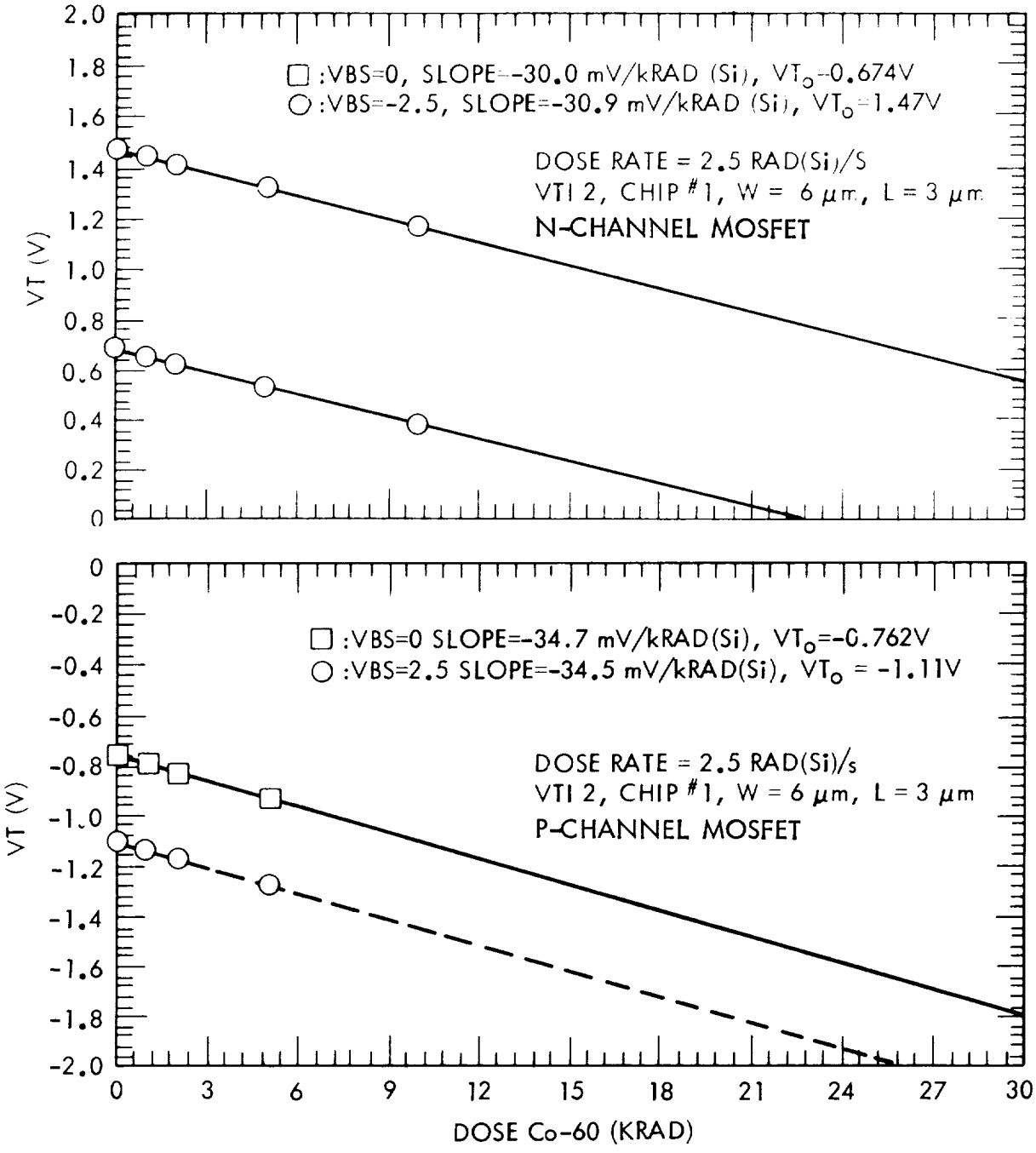


Figure 7.18: Threshold voltage versus dose for n- (top) and p-channel (bottom) MOSFETs. The gate voltage was 5 V during irradiation.

7.7.1 Test Hardware and Measurement Procedure

The CRRES chip timing sampler array consists of a series of 128 identical inverters grouped as 64 inverter-pairs. The output of each inverter-pair is connected to one input of a dynamic Muller-C timing sampler element. The other input of each timing sampler element is connected to the timing sampler array's enable input pad (TSE). The input to the first inverter-pair of the chain is connected to the timing sampler array's delay chain input pad (TSI). As a result of space and weight limitations, the measurement procedure on the CRRES satellite consists of applying a fixed 100 ns delay input (delay between edges on TSI and TSE pins), and then reading the 6-bit binary output word. This output word reflects the number of inverter-pairs the transition has propagated through in the 100 ns period. The timing sampler is essentially a delay-to-digital converter, and therefore results in a possible quantization error in the measured output. This error is minus one least significant bit and results in a worst-case inverter-pair delay error of 100/N percent where N is the number of inverter pairs tripped.

The wafer level measurements performed in the JPL VLSI technology lab employ a more sophisticated technique which eliminates this quantization error and allows the delay to be measured at each of the 64 taps on the inverter-pair chain. The delay from TSI input to tap N on the inverter-pair chain is measured by applying a start transition to input TSI followed by a stop transition on TSE, and then observing the circuit output D0-D5. This sequence is repeated at a 100 kHz rate by a tester that adjusts the delay between start and stop transitions each cycle. The delay is increased when the output from the previous cycle is less than N and decreased when the output is greater than or equal to N. Figure 7.19 illustrates the measurement timing relationships. When the

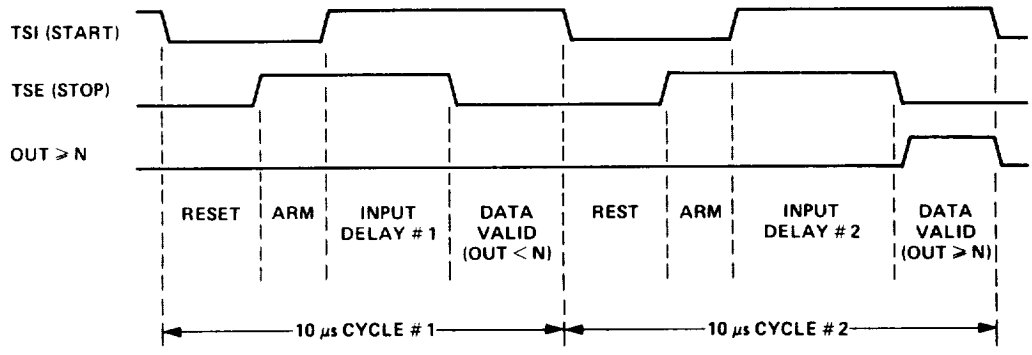


Figure 7.19: Timing analysis for the CRRES chip timing sampler.

feedback loop has stabilized, the start and stop transition inputs are sampled with a counter/timer that employs both pseudo-random time base modulation circuitry and averaging methods to obtain a 0.1 ns resolution on a sample of 100 thousand measurement cycles. Figure 7.20 illustrates the test apparatus. The integrator in the feedback loop integrates the error, which is VCC/2 or -VCC/2, and causes the delay between START and STOP to be adjusted until the loop is stabilized. At this point the delay dithers by a magnitude and rate dependent on the integrator time constant and clock frequency. This dither can be made very small (not observable on a 300MHz oscilloscope) and since the unknown delay is centered in the distribution of delay measurements over many cycles, the counter/timer obtains an accurate reading through averaging. The 12 ns delay line is required because the smallest delay that can be measured with the Tektronix 5009 counter/timer is 10 ns. Since the delay between the START and STOP edges at the first inverter-pair (N = 1) is not precisely known, due to wire and pad delays, the delay reading obtained is used as a baseline for correcting the other delay readings (N = 2 to 64).

7.7.2 Data and Results

Figure 7.21 illustrates the data obtained from a typical CRRES chip timing sampler array. Measurements are made for positive edge delays (X's on plot) and for negative edge delays (O's on plot). The data point at the origin of the plot is an artifact of the baseline reading taken from the first of the 64 inverter-pairs. Since this value is subtracted from all 64 delay readings, there are 63 corrected delay measurements (INVPAIR = 1 through 63 on the plot). By fitting lines through the X's and O's, one obtains effective inverter-pair delays based on 63 inverter-pairs. TDP and TDN are the inverter-pair delays for positive and negative inputs, respectively. By subtracting delays between successive stages, one obtains the individual inverter-pair delays for each of the 63 stages. Figure 7.22 illustrates the positive edge inverter-pair delay data extracted from the X marked points of Figure 7.21. Also illustrated is the distribution of this data. It is evident that there is no obvious trend to this data across the linear dimension of the 2.5 mm array. In other words, a line fitted to this data would have a slope of approximately zero. There is, however, a spread in the inverter-pair data. As can be seen, the data is approximately normally distributed with a mean of 2.54 ns and a standard deviation of 0.36 ns. The lack of trend and tightness of this data explains the high correlation coefficient (greater than 0.9999) obtained by a least squares fit to the data of Figure 7.21.

Table 7.8 summarizes the data from 4 wafers. The average and standard de-

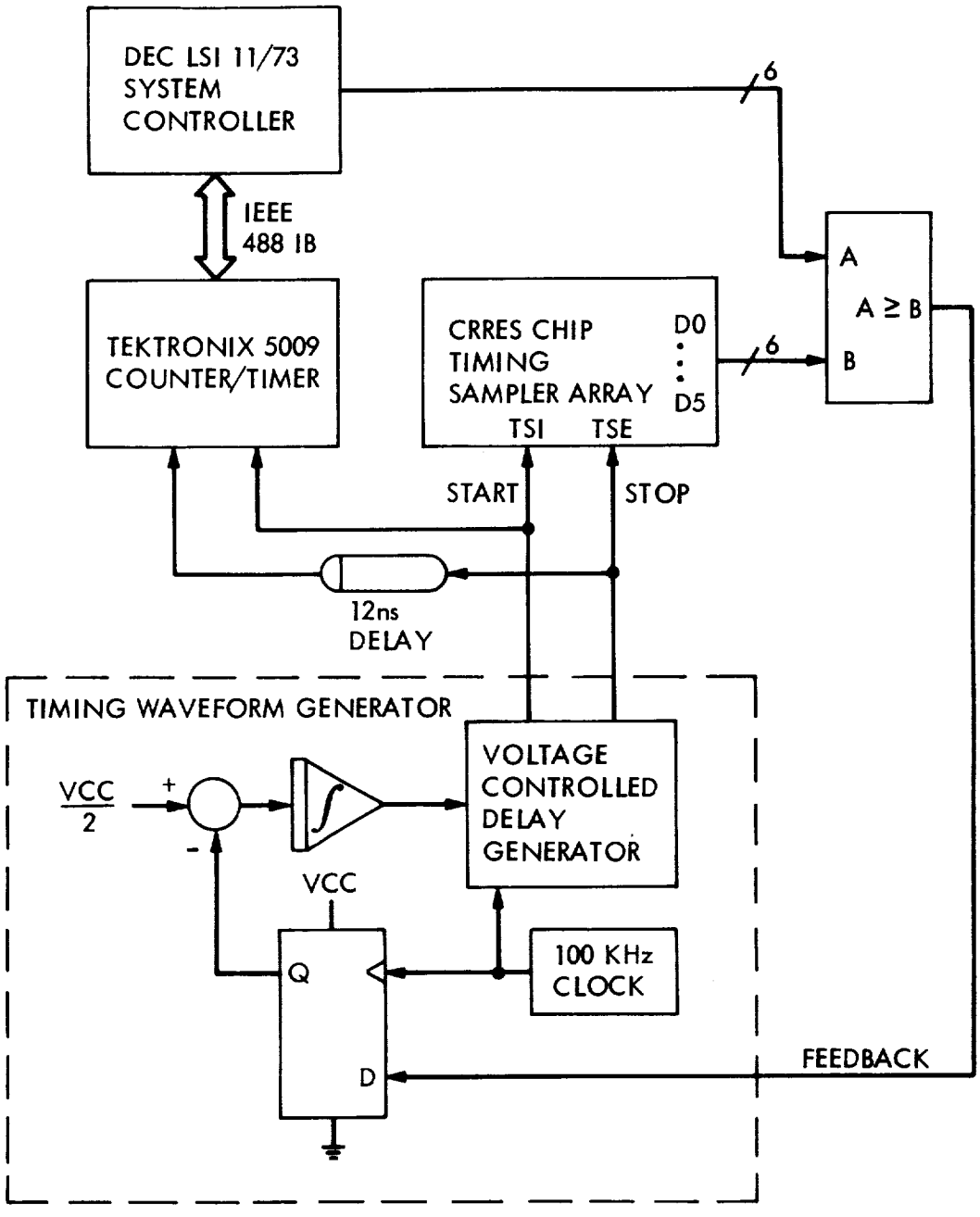


Figure 7.20: Apparatus for measuring JPL CRRES chip timing sampler.

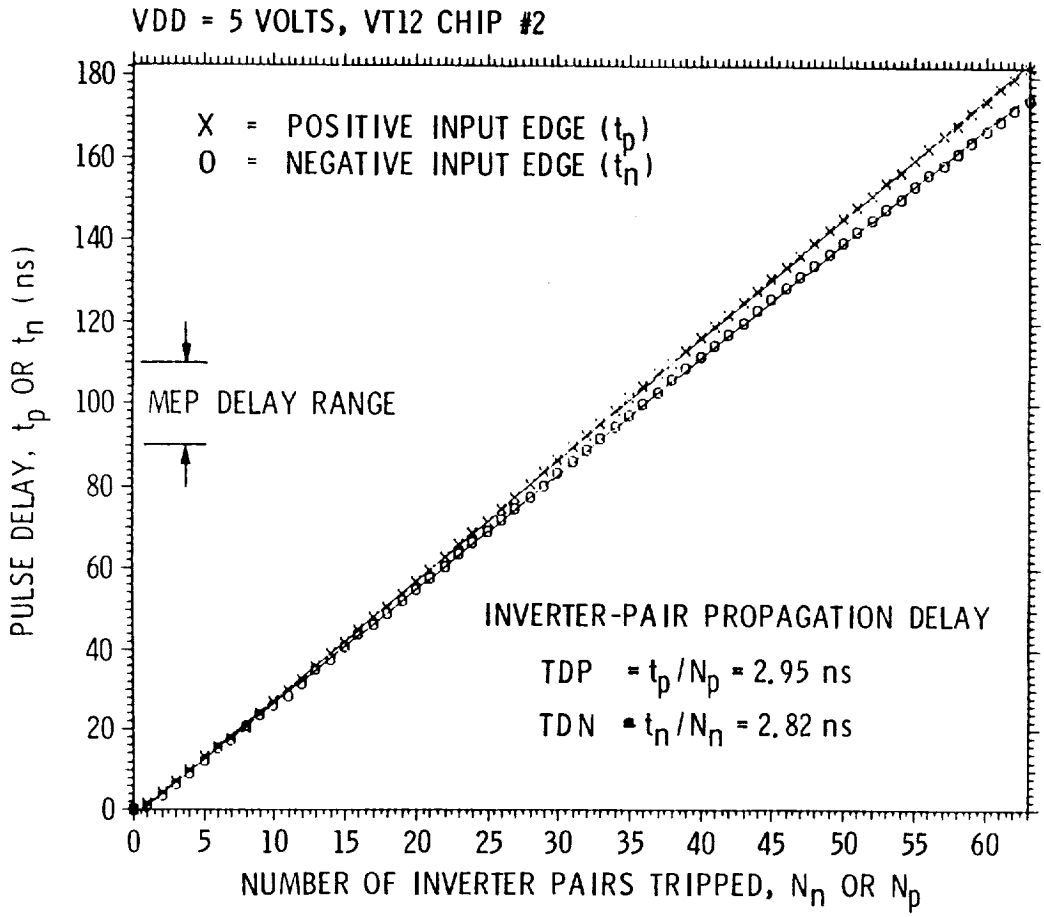
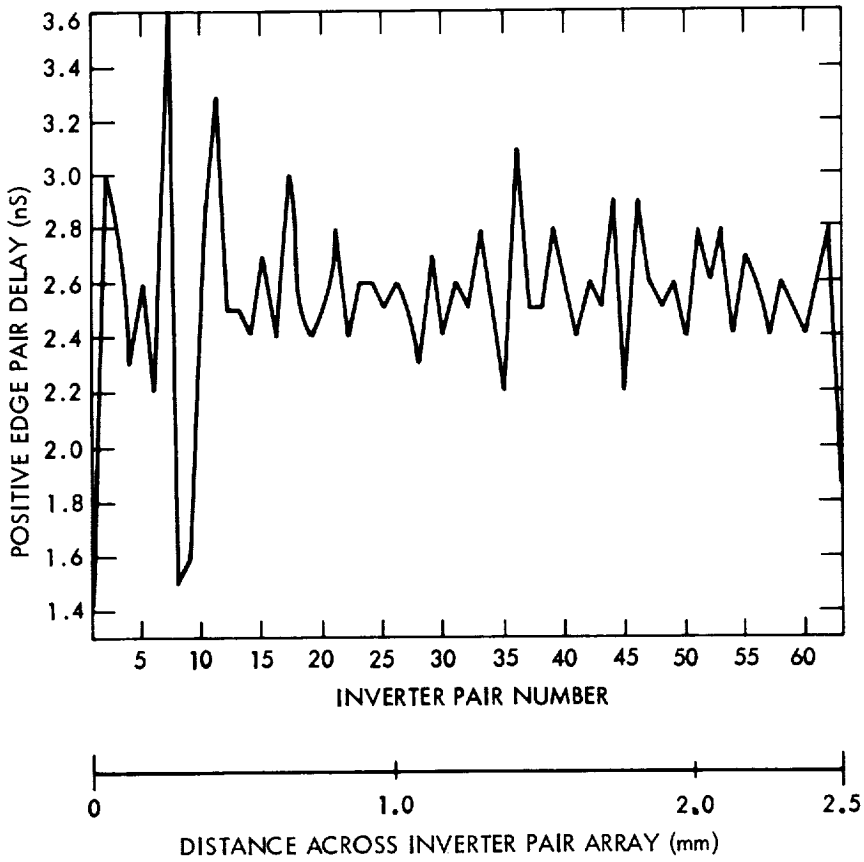


Figure 7.21: Timing sampler inverter-pair array data.



INTERVAL MIDPOINT (ns)		NO. OBS.	NUMBER OF OBSERVATIONS 0 10 20
1.35		1	*
1.47		1	*
1.58		1	*
1.70		0	
1.81		1	*
1.93		0	
2.04		0	
2.16	-	3	***
2.27		2	**
2.39		10	**********
2.50	>	13	*************
2.62		13	*************
2.73		4	****
2.85	+	9	*********
2.96		2	**
3.08		1	*
3.19		0	
3.31		1	*
3.42		0	
3.54		1	*

MEAN	STDEV	% STDEV	MEDIAN	MINIMUM	MAXIMUM
2.53 ns	0.360 ns	14.1	2.50 ns	1.30 ns	3.60 ns

Figure 7.22: Positive edge inverter-pair delta data from one chip.

Table 7.8: Summarized data from the timing samplers on four wafers.

	Wafer #1 (9 sites tested)					
	MEAN	STDEV	% STDEV	MEDIAN	MINIMUM	MAXIMUM
TDP	2.72	0.113	4.16	2.71	2.57	2.86
PR2	0.9998	0	0	0.9999	0.9995	0.9999
TDN	2.57	0.102	3.97	2.58	2.42	2.69
NR2	0.9999	0	0	0.9999	0.9998	0.9999
TDPAVG	2.69	0.107	3.97	2.68	2.54	2.83
TDPSIG	0.27	0.03	11.0	0.28	0.22	0.31
TDNAVG	2.56	0.104	4.05	2.56	2.41	2.68
TDNSIG	0.20	0.03	15.3	0.19	0.15	0.25

	Wafer #4 (41 sites tested)					
	MEAN	STDEV	% STDEV	MEDIAN	MINIMUM	MAXIMUM
TDP	2.61	0.158	6.05	2.61	2.29	2.94
PR2	0.9999	0	0	0.9999	0.9997	0.9999
TDN	2.46	0.134	5.43	2.46	2.18	2.73
NR2	0.9999	0.0006	0.062	0.9999	0.9995	0.9999
TDPAVG	2.58	0.159	6.16	2.59	2.26	2.92
TDPSIG	0.26	0.03	13.3	0.26	0.15	0.32
TDNAVG	2.44	0.135	5.54	2.45	2.14	2.71
TDNSIG	0.20	0.04	20.0	0.20	0.13	0.28

	Wafer #5 (70 sites tested)					
	MEAN	STDEV	% STDEV	MEDIAN	MINIMUM	MAXIMUM
TDP	2.65	0.179	6.76	2.65	2.31	3.64
PR2	0.9999	0	0	0.9999	0.9997	0.9999
TDN	2.48	0.27	11.04	2.51	0.56	3.22
NR2	0.9999	0.0005	0.047	0.9999	0.9993	0.9999
TDPAVG	2.62	0.173	6.59	2.62	2.29	3.54
TDPSIG	0.28	0.05	17.1	0.27	0.22	0.61
TDNAVG	2.49	0.141	5.68	2.50	2.21	3.15
TDNSIG	0.19	0.05	27.6	0.19	0.10	0.56

	Wafer #10 (9 sites tested)					
	MEAN	STDEV	% STDEV	MEDIAN	MINIMUM	MAXIMUM
TDP	2.80	0.131	4.70	2.81	2.56	3.02
PR2	0.9999	0	0	0.9999	0.9998	0.9999
TDN	2.66	0.126	4.75	2.67	2.43	2.87
NR2	0.9999	0	0	0.9999	0.9998	0.9999
TDPAVG	2.76	0.127	4.59	2.76	2.53	2.98
TDPSIG	0.27	0.04	14.8	0.26	0.22	0.34
TDNAVG	2.65	0.119	4.51	2.64	2.43	2.85
TDNSIG	0.18	0.02	10.8	0.19	0.15	0.21

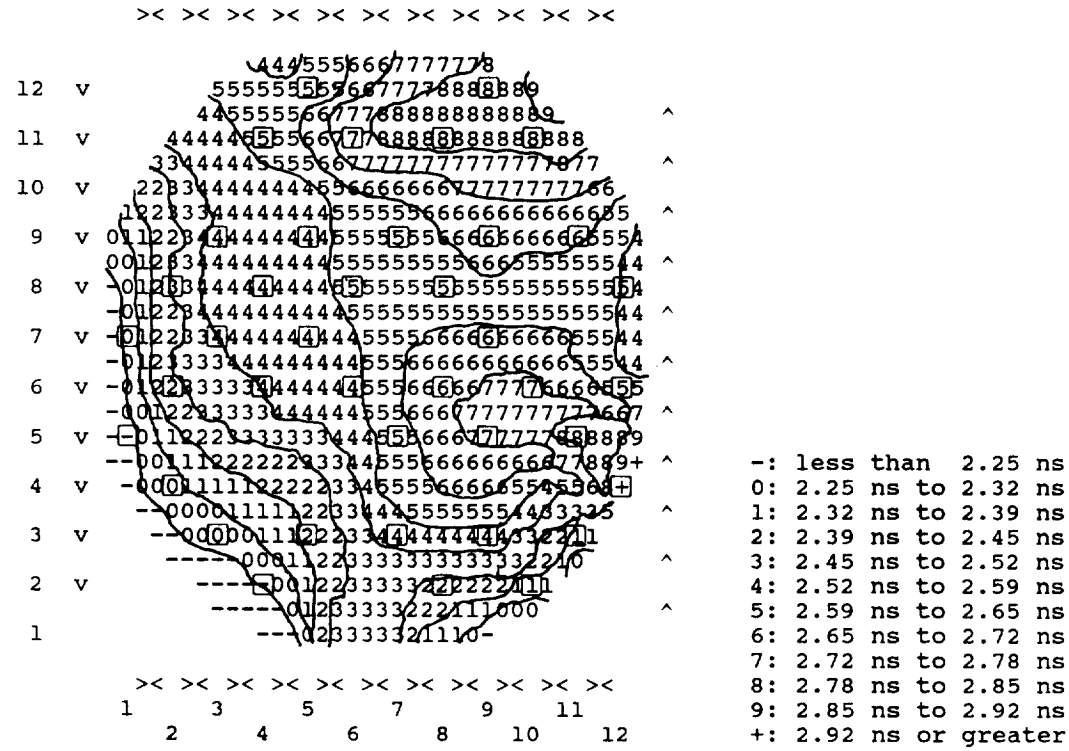
viation computed from the inverter-pair data for positive/negative input transitions is specified by TDPAVG/TDNAVG and TDPSIG/TDNSIG, respectively. PR2/NR2 are the correlation coefficients corresponding to the line fits for the positive/negative transition data. Notice that the average delay variation over a wafer is very small, with a standard deviation of less than 0.2 ns.

The inverter-pair delays for positive and negative transitions on wafer #4 are displayed in Figures 7.23 and 7.24 respectively. The 41 boxed numbers are the actual locations that were measured on this wafer. These maps show that the fastest circuits would be obtained from the lower left side on the wafer. If a microprocessor, whose longest computational delay per clock cycle was 80 gate delays, was fabricated on this run, processors from the lower left portion of the wafer could run at a maximum clock frequency of around 11.5 MHz but processors from the upper right portion of the wafer could run only 9 MHz.

The inverter-pair delay for positive transitions is 5 to 6 percent larger than the inverter-pair delay for negative transitions. This difference is due to the different response times of the n- and p-channel transistors in the inverters. This is due to the timing sampler's design in which the first inverter of each inverter-pair drives a fanout of 1 and the second inverter drives a fanout of 2. So, if the input to the inverter pair is a positive edge, the n-channel transistor in the first inverter drives the output (fanout of 1) while the p-channel transistor in the second inverter drives the output (fanout of 2). If these fanouts were the same, then the positive and negative transition delays would be equal. The magnitude of the delay difference between positive and negative transition delays is a function of the loading imbalance as well as the p-channel and n-channel transistor channel mobility difference and the ratio of the p-channel to n-channel width to length ratio r (r = 5/3 on CRRES chip). This inverter-pair delay can be expressed in terms of intrinsic n-channel and p-channel transistor delays τ_n and τ_p respectively [2].

7.7.3 Conclusions

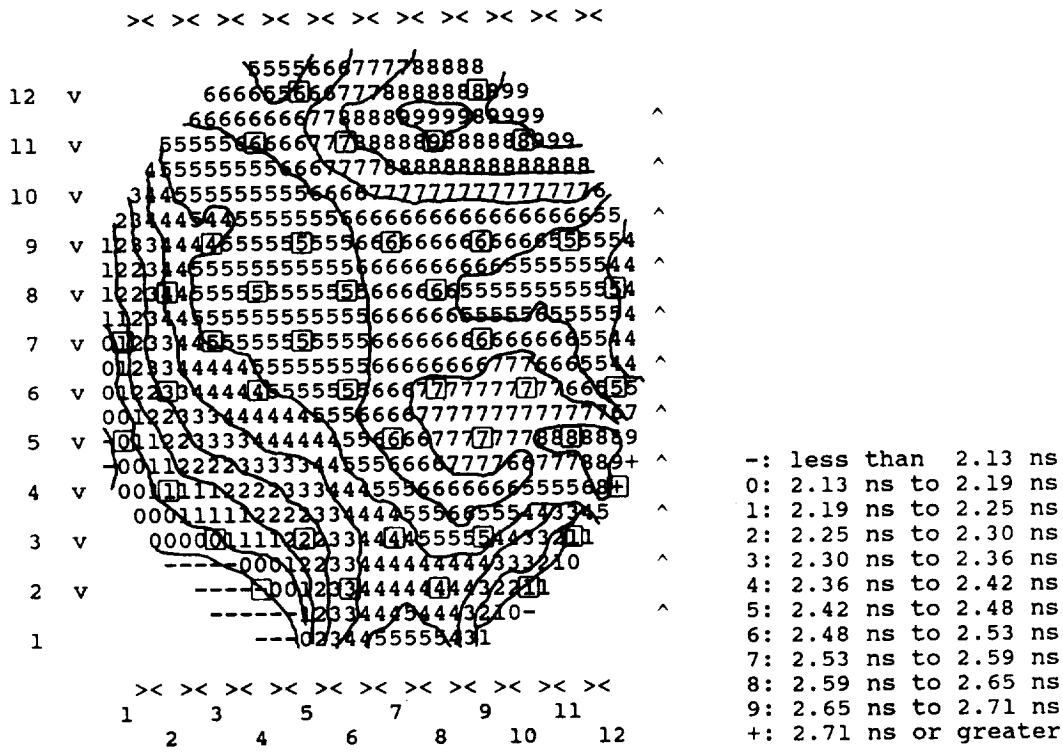
The data obtained from the CRRES chip timing sampler demonstrates this approach to be accurate and robust. This structure provides an easy way to measure inverter delays on a satellite that has power and weight limitations and cannot afford to include standard type lab test equipment such as a frequency counter. Since the delay data obtained from one timing sampler array shows that the inverter pairs all have the same delay ($\pm 0.4ns$), the procedure performed on the satellite (inverter-pair delay = 100 ns/# stages tripped) should give accurate results to within minus one least significant bit.



INTERVAL MIDPOINT (ns)		NO. OBS.	NUMBER OF OBSERVATIONS 0 10 20
2.29		4	****
2.35		1	*
2.42	-	4	****
2.49		3	***
2.55	>	9	*********
2.62		9	*********
2.69		4	****
2.75	+	3	***
2.82		3	***
2.88		1	*

MEAN	STDEV	% STDEV	MEDIAN	MINIMUM	MAXIMUM
2.57 ns	0.159 ns	6.15	2.58 ns	2.25 ns	2.92 ns

Figure 7.23: Wafer map of the average inverter-pair delay for positive edges (Wafer 4).



INTERVAL MIDPOINT (ns)		NO. OBS.	NUMBER OF OBSERVATIONS 0 10 20
2.16		2	**
2.22		3	***
2.27	-	3	***
2.33		2	**
2.39		5	*****
2.45	>	11	**********
2.50		6	******
2.56	+	4	****
2.62		2	**
2.68		3	***

MEAN	STDEV	% STDEV	MEDIAN	MINIMUM	MAXIMUM
2.44 ns	0.135 ns	5.54	2.45 ns	2.13 ns	2.71 ns

Figure 7.24: Wafer map of the average inverter-pair delay for negative edges (Wafer 4).

7.8 Conclusions

The major goal of the JPL CRRES chip project was to provide parts to AFGL for inclusion on the MEP. This was accomplished in March 1986. Additional, parts have been delivered to the ground test part of the CRRES program.

In this report period, the SRAM design was changed in two important ways: design rule violations were eliminated and the asymmetrical SRAM cell design was incorporated to increase the overall probability of seeing SEU. Results from SEU tests of the asymmetrical cell indicate that the upset rate is almost a factor of three greater than that of the balanced cell. Since these tests were performed at energy levels substantially above the minimum energy required to cause upset, the results correspond to the cross-section ratio between the cell geometries.

The transistor matrix design has not changed in the report period except for a slight modification in the ancillary circuitry mandated by foundry-specified minimum design spacings. Results from electrical tests confirm that transistor parameters extracted from transistors in an addressed matrix are a highly successful and preferable alternative to testing individual transistors. Cobalt-60 test results indicate the decoder circuitry does not interfere in any way with transistor measurements until a sufficiently high dose causes the n-channel enhancement mode devices to become depletion mode.

7.9 Future Work

The functions of the CRRES chip will be split into two chips, an SEU Chip and a TID Chip. This is being done since many SRAMs are needed in a satellite experiment in order to get sufficient statistical data on SEUs. For the CRRES chip SRAM cell, we calculate 10 Mbits would be desired. The TID Chip will consist of a MOSFET matrix and timing sampler.

Experimental work is planned to study the radiation effects of the field-oxide devices on MOSFET matrix measurements to establish the specific cause of chip leakage currents. This work is essential to evaluate potential design changes.

Plans for upgrading functional test capabilities are underway. Improved test capabilities will greatly simplify and expedite heavy ion testing of the SRAM and Cobalt 60 testing of the MOSFET matrix and timing sampler.

7.10 CRRES Chip Test Configuration Pin Outs

This section contains pin-outs and connection diagrams to serve as a guide to a user of the JPL CRRES chip.

1. CRRES Chip Leakage Measurement Pin Configuration

PIN	FUNCTION	PIN STATE	PIN	FUNCTION	PIN STATE
1	VDD	VDD	33	SRAM DQ12	GND
2	XT VPS	VDD	34	SRAM DQ11	GND
3	SRAM A7	GND	35	SRAM DQ10	GND
4	XT VG	GND	36	SRAM DQ9	GND
5	INV OUT	NC	37	SRAM DQ8	GND
6	INV SUB	VDD	38	SRAM DQ7	GND
7	INV VDD	VDD	39	SRAM DQ6	GND
8	INV p-GATE	GND	40	SRAM DQ5	GND
9	INV VSS	GND	41	SRAM DQ4	GND
10	INV WELL	GND	42	SRAM DQ3	GND
11	XT WELL	GND	43	SRAM DQ2	GND
12	INV n-GATE	GND	44	SRAM DQ1	GND
13	SPARE	GND	45	SRAM DQ0	GND
14	SPARE	GND	46	SRAM S	GND
15	TS I	GND	47	SRAM W	GND
16	TS E	GND	48	SRAM E	GND
17	SPARE	GND	49	SRAM EP	GND
18	SPARE	GND	50	SRAM A5	GND
19	SPARE	GND	51	SRAM A4	GND
20	SPARE	GND	52	SRAM A3	GND
21	SPARE	GND	53	SRAM A2	GND
22	SPARE	GND	54	SRAM A1	GND
23	TS D0	NC	55	SRAM A0	GND
24	TS D1	NC	56	XT EN	GND
25	TS D2	NC	57	SRAM A6	GND
26	TS D3	NC	58	XT R1	GND
27	TS D4	NC	59	XT R0	GND
28	TS D5	NC	60	XT C0	GND
29	GND	GND	61	XT C1	GND
30	SRAM DQ15	GND	62	XT C2	GND
31	SRAM DQ14	GND	63	XT ID	NC
32	SRAM DQ13	GND	64	XT VD	NC

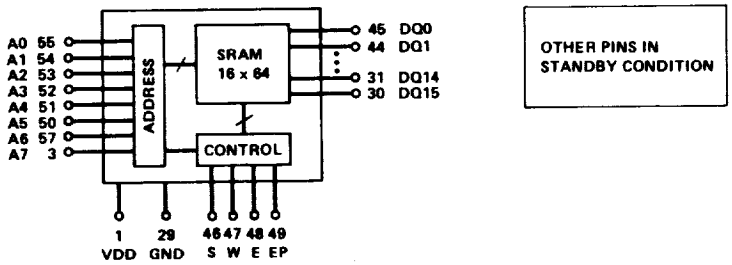
NC = NO CONNECTION
TS = TIMING SAMPLER
XT = TRANSISTOR MATRIX
SRAM = STATIC RANDOM ACCESS MEMORY
INV = INVERTER

2. CRRES Chip Pin Configuration for SRAM Operation. See also Figures 7.1, 7.3, and 7.25.

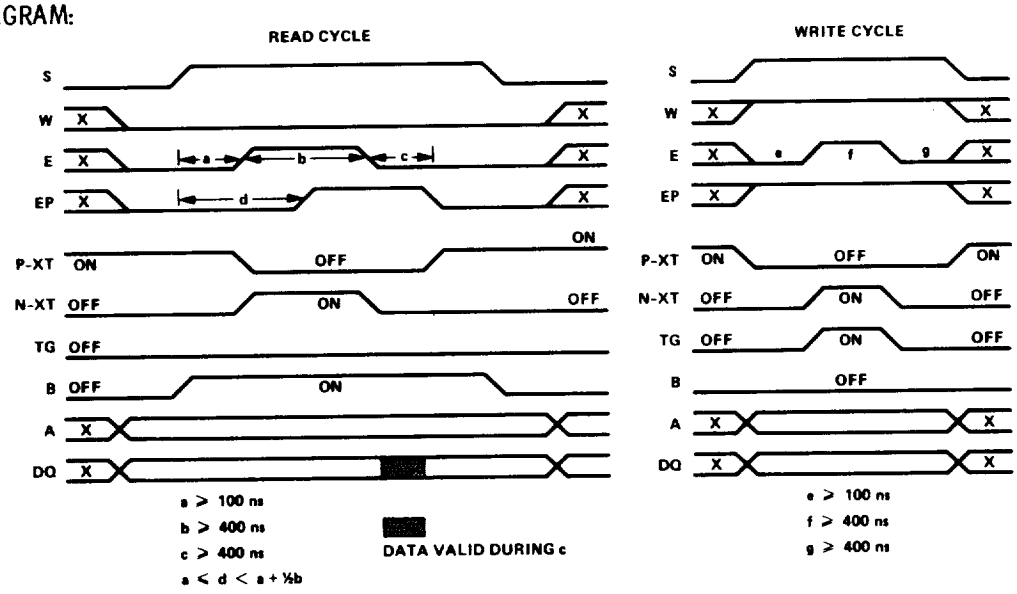
PIN	FUNCTION	PIN STATE	PIN	FUNCTION	PIN STATE
1	VDD	VDD	33	SRAM DQ12	(0,1)
2	XT VPS	VDD	34	SRAM DQ11	(0,1)
3	SPARE	GND	35	SRAM DQ10	(0,1)
4	XT VG	GND	36	SRAM DQ9	(0,1)
5	INV OUT	NC	37	SRAM DQ8	(0,1)
6	INV SUB	VDD	38	SRAM DQ7	(0,1)
7	INV VDD	VDD	39	SRAM DQ6	(0,1)
8	INV p-GATE	GND	40	SRAM DQ5	(0,1)
9	INV VSS	GND	41	SRAM DQ4	(0,1)
10	INV WELL	GND	42	SRAM DQ3	(0,1)
11	XT WELL	GND	43	SRAM DQ2	(0,1)
12	INV n-GATE	GND	44	SRAM DQ1	(0,1)
13	SPARE	GND	45	SRAM DQ0	(0,1)
14	SPARE	GND	*46	SRAM S	*(0,1)
15	TS I	GND	*47	SRAM W	*(0,1)
16	TS E	GND	*48	SRAM E	*(0,1)
17	SPARE	GND	*49	SRAM EP	*(0,1)
18	SPARE	GND	50	SRAM A5	(0,1)
19	SPARE	GND	51	SRAM A4	(0,1)
20	SPARE	GND	52	SRAM A3	(0,1)
21	SPARE	GND	53	SRAM A2	(0,1)
22	SPARE	GND	54	SRAM A1	(0,1)
23	TS D0	NC	55	SRAM A0	(0,1)
24	TS D1	NC	56	XT EN	GND
25	TS D2	NC	57	SPARE	GND
26	TS D3	NC	58	XT R1	GND
27	TS D4	NC	59	XT R0	GND
28	TS D5	NC	60	XT C0	GND
29	GND	GND	61	XT C1	GND
30	SRAM DQ15	(0,1)	62	XT C2	GND
31	SRAM DQ14	(0,1)	63	XT ID	NC
32	SRAM DQ13	(0,1)	64	XT VD	NC

NC = NO CONNECTION
TS = TIMING SAMPLER
XT = TRANSISTOR MATRIX
SRAM = STATIC RANDOM ACCESS MEMORY
INV = INVERTER
*SRAM S, SRAM W, SRAM E, AND SRAM EP, SEE TIMING DIAGRAM

BLOCK DIAGRAM:



TIMING DIAGRAM:



SPECIFICATIONS:

CHIP CURRENT DURING RAM OPERATION = 300 μA

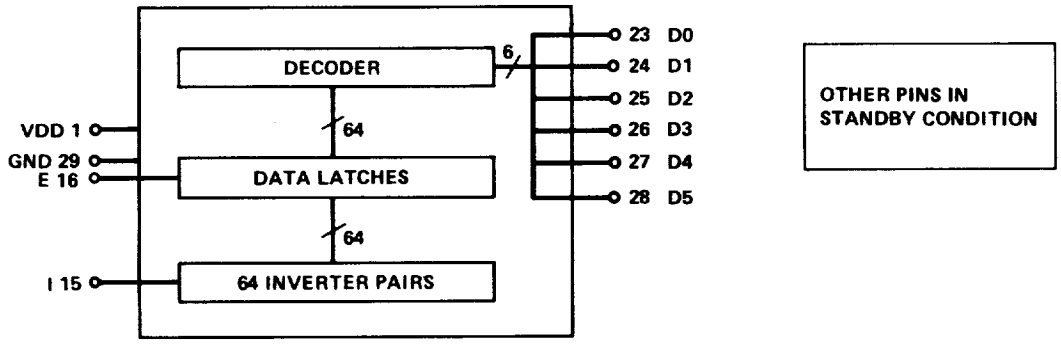
Figure 7.25: Test specifications for the JPL CRRES Chip SRAM.

3. CRRES Chip Pin Configuration for Timing Sampler Operation. See also Figures 7.1, 7.7, and 7.26.

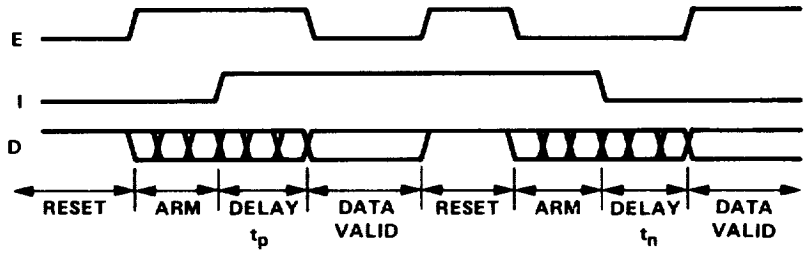
PIN	FUNCTION	PIN STATE	PIN	FUNCTION	PIN STATE
1	VDD	VDD	33	SRAM DQ12	GND
2	XT VPS	VDD	34	SRAM DQ11	GND
3	SPARE	GND	35	SRAM DQ10	GND
4	XT VG	GND	36	SRAM DQ9	GND
5	INV OUT	NC	37	SRAM DQ8	GND
6	INV SUB	VDD	38	SRAM DQ7	GND
7	INV VDD	VDD	39	SRAM DQ6	GND
8	INV p-GATE	GND	40	SRAM DQ5	GND
9	INV VSS	GND	41	SRAM DQ4	GND
10	INV WELL	GND	42	SRAM DQ3	GND
11	XT WELL	GND	43	SRAM DQ2	GND
12	INV n-GATE	GND	44	SRAM DQ1	GND
13	SPARE	GND	45	SRAM DQ0	GND
14	SPARE	GND	46	SRAM S	GND
15	TS I	*(start)	47	SRAM W	GND
16	TS E	*(stop)	48	SRAM E	GND
17	SPARE	GND	49	SRAM EP	GND
18	SPARE	GND	50	SRAM A5	GND
19	SPARE	GND	51	SRAM A4	GND
20	SPARE	GND	52	SRAM A3	GND
21	SPARE	GND	53	SRAM A2	GND
22	SPARE	GND	54	SRAM A1	GND
23	TS D0	(0,1) OUT	55	SRAM A0	GND
24	TS D1	(0,1) OUT	56	XT EN	GND
25	TS D2	(0,1) OUT	57	SPARE	GND
26	TS D3	(0,1) OUT	58	XT R1	GND
27	TS D4	(0,1) OUT	59	XT R0	GND
28	TS D5	(0,1) OUT	60	XT C0	GND
29	GND	GND	61	XT C1	GND
30	SRAM DQ15	GND	62	XT C2	GND
31	SRAM DQ14	GND	63	XT ID	NC
32	SRAM DQ13	GND	64	XT VD	NC

NC = NO CONNECTION
TS = TIMING SAMPLER
XT = TRANSISTOR MATRIX
SRAM = STATIC RANDOM ACCESS MEMORY
INV = INVERTER
*TS I AND TS E, SEE TIMING DIAGRAM

BLOCK DIAGRAM:



TIMING DIAGRAM:



SPECIFICATIONS:

INPUT PULSE DELAY (t_p OR t_n) = 100 nsec +/- 10 nsec REPEATABLE TO ±1 nsec

OUTPUTS = BINARY 6-BIT WORD

Figure 7.26: Test specifications for the JPL CRRES Chip Timing Sampler.

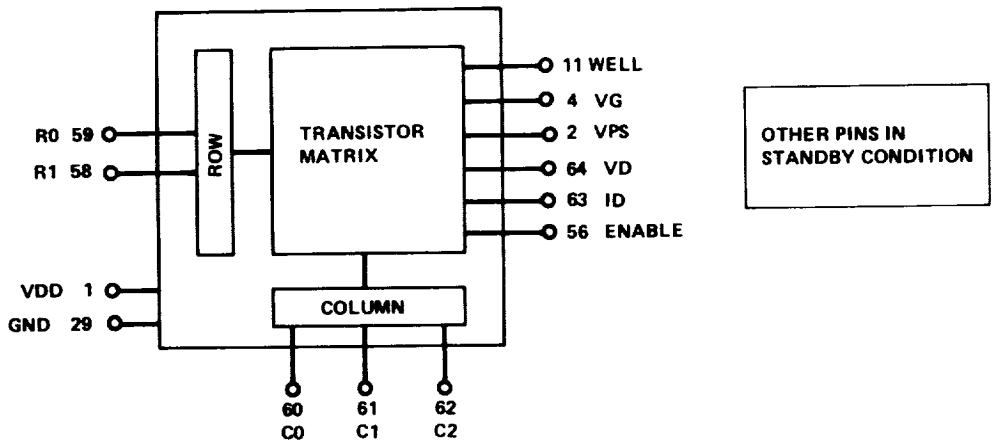
4. CRRES Chip Pin Configuration for MOSFET Matrix Measurement. See also Figures 7.1, 7.4, and 7.27.

PIN	FUNCTION	PIN STATE	PIN	FUNCTION	PIN STATE
1	VDD	VDD	33	SRAM DQ12	GND
2	XT VPS	VDD	34	SRAM DQ11	GND
3	SPARE	GND	35	SRAM DQ10	GND
4	XT VG	VS	36	SRAM DQ9	GND
5	INV OUT	NC	37	SRAM DQ8	GND
6	INV SUB	VDD	38	SRAM DQ7	GND
7	INV VDD	VDD	39	SRAM DQ6	GND
8	INV p-GATE	GND	40	SRAM DQ5	GND
9	INV VSS	GND	41	SRAM DQ4	GND
10	INV WELL	GND	42	SRAM DQ3	GND
11	XT WELL	VS	43	SRAM DQ2	GND
12	INV n-GATE	GND	44	SRAM DQ1	GND
13	SPARE	GND	45	SRAM DQ0	GND
14	SPARE	GND	46	SRAM S	GND
15	TS I	GND	47	SRAM W	GND
16	TS E	GND	48	SRAM E	GND
17	SPARE	GND	49	SRAM EP	GND
18	SPARE	GND	50	SRAM A5	GND
19	SPARE	GND	51	SRAM A4	GND
20	SPARE	GND	52	SRAM A3	GND
21	SPARE	GND	53	SRAM A2	GND
22	SPARE	GND	54	SRAM A1	GND
23	TS D0	NC	55	SRAM A0	GND
24	TS D1	NC	56	XT EN	VDD
25	TS D2	NC	57	SPARE	GND
26	TS D3	NC	58	XT R1	(0,1)
27	TS D4	NC	59	XT R0	(0,1)
28	TS D5	NC	60	XT C0	(0,1)
29	GND	GND	61	XT C1	(0,1)
30	SRAM DQ15	GND	62	XT C2	(0,1)
31	SRAM DQ14	GND	63	XT ID	VS,IM
32	SRAM DQ13	GND	64	XT VD	DVM

NC = NO CONNECTION
TS = TIMING SAMPLER
XT = TRANSISTOR MATRIX
SRAM = STATIC RANDOM ACCESS MEMORY
INV = INVERTER
VS = VOLTAGE SOURCE; IM = CURRENT MEASURE

n-CH XT: COL 0, 2, 4, AND 6; p-CH XT: COL 1, 3, 5, AND 7
XT DIM: Col 1 & 2 $W/L = 6\,\mu m/3\,\mu m$; Col 3 & 4 $W/L = 9\,\mu m/3\,\mu m$,
Col 5 & 6 $W/L = 6\,\mu m/3\,\mu m$; Col 7 & 8 $W/L = 9\,\mu m/3\,\mu m$
LARGE FIELD OXIDE XT: ROW 0, COL 4 AND 6; BLANK: ROW 0, COL 5

BLOCK DIAGRAM:



MEP SPECIFICATION:

IDS MEASURE	100 nA ± 10 nA TO 1 mA ± 0.5 PERCENT
VDS MEASURE	0 TO 5 V ± 1 mV
VDS SUPPLY	0 TO 5 V ± 1 mV
VGS SUPPLY	0 TO 5 V ± 1 mV

IDS = 0.05, 0.2,0.6, 1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5 V — 12 VOLTAGES
VGS = 0.05, 0.5, 1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5 V — 11 VOLTAGES
} TOTAL = 132 DATA POINTS
VBS = 0

PREFERRED MEASUREMENT SPECIFICATION:

VDS = 0.05, 0.2, 0.6,1, 1.5, 2, 3.5, 5 V — 8 VOLTAGES
VGS = 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7,0.8, 0.9 1.0, 1.1, 1.5, 2, 3, 4, 5 V — 16 VOLTAGES
} TOTAL = 128 DATA POINTS
VBS = 0

Figure 7.27: Test specifications for the JPL CRRES Chip MOSFET Matrix.

5. CRRES Chip Leakage Measurement Pin Configuration. Early CRRES Runs Only: Foundry Run 1 (VTI1). This pin-out list is different in that the Ring Oscillator had not yet been removed from the timing sampler circuit

PIN	FUNCTION	PIN STATE	PIN	FUNCTION	PIN STATE
1	VDD	VDD	33	SRAM DQ12	GND
2	XT VPS	VDD	34	SRAM DQ11	GND
3	SRAM A7	GND	35	SRAM DQ10	GND
4	XT VG	GND	36	SRAM DQ9	GND
5	INV OUT	NC	37	SRAM DQ8	GND
6	INV SUB	VDD	38	SRAM DQ7	GND
7	INV VDD	VDD	39	SRAM DQ6	GND
8	INV p-GATE	GND	40	SRAM DQ5	GND
9	INV VSS	GND	41	SRAM DQ4	GND
10	INV WELL	GND	42	SRAM DQ3	GND
11	XT WELL	GND	43	SRAM DQ2	GND
12	INV n-GATE	GND	44	SRAM DQ1	GND
13	SPARE	GND	45	SRAM DQ0	GND
14	SPARE	GND	46	SRAM S	GND
15	TS I	GND	47	SRAM W	GND
16	TS E	GND	48	SRAM E	GND
17	RO ENABLE	GND	49	SRAM EP	GND
18	RO OUTPUT	NC	50	SRAM A5	GND
19	SPARE	GND	51	SRAM A4	GND
20	SPARE	GND	52	SRAM A3	GND
21	SPARE	GND	53	SRAM A2	GND
22	SPARE	GND	54	SRAM A1	GND
23	TS D0	NC	55	SRAM A0	GND
24	TS D1	NC	56	XT EN	GND
25	TS D2	NC	57	SRAM A6	GND
26	TS D3	NC	58	XT R1	GND
27	TS D4	NC	59	XT R0	GND
28	TS D5	NC	60	XT C0	GND
29	GND	GND	61	XT C1	GND
30	SRAM DQ15	GND	62	XT C2	GND
31	SRAM DQ14	GND	63	XT ID	NC
32	SRAM DQ13	GND	64	XT VD	NC

NC = NO CONNECTION
TS = TIMING SAMPLER
XT = TRANSISTOR MATRIX
INV = INVERTER
SRAM = STATIC RANDOM ACCESS MEMORY

Bibliography

[1] M. G. Buehler, T. W. Griswold, C. A. Piña, and C. Timoc, "Test Chips for Custom ICs: Six Kinds of Test Structures," *Circuits Manufacturing*, Vol. 22, pp. 36-42, June 1982.

[2] M. G. Buehler, B. R. Blaes, G. A. Jennings, B. T. Moore, R. H. Nixon, C. A. Piña, H. R. Sayah, M. W. Sievers, and N. F. Stahlberg, "Product Assurance Technology for Custom LSI/VLSI Electronics Report for Period October 1982 - September 1984," JPL Publication 85-76.

[3] M. G. Buehler, B. R. Blaes, C. A. Piña, T. W. Griswold, "Pinhole Array Capacitor for Oxide Integrity Analysis," *Solid State Technology*, Vol. 26, pp. 131-137, November 1983.

[4] E. Kooi, J. G. van Lierop, J. A. Appels, "Formation of Silicon Nitride at an Si-SiO_2 Interface during Local Oxidation of Silicon and during Heat-Treatment of Oxidized Silicon in NH_3 Gas," *J. Electrochem. Soc.*, Vol. 123, pp. 1117-1120, 1976.

[5] O. Nakajima, N. Shiono, S. Musamoto, and C. Hushimoto, "Defects in a Gate Oxide Grown after the LOCOS Process," *Jpn. J. Appl. Phys.*, Vol. 18, pp. 943-951, 1979.

[6] C. A. Goodwin and J. W. Brossman, "MOS Gate Oxide Defects Related to Treatment of Nitride Coated Wafers Prior Local Oxidation," *J. Electrochem. Soc.*, Vol. 129, pp. 1066-1070, 1982.

[7] U. Leineweg and D. Hannaman, "Yield Analysis of Interfacial Contact Resistance Measured on Cross-Contact-Chains," *IEEE VLSI Workshop on Test Structures*, Long Beach, California, February 1986.

[8] J. Shen, W. Maly, and F. Ferguson, Carnegie-Mellon University, "Inductive Fault Analysis of MOS Integrated Circuits," *IEEE Design and Test of Computers*, Vol. 2, pp 13-26, December 1985.

[9] M. Buehler and H. Sayah, "Addressable Inverter Matrix for Process and Device Characterization," *Solid State Technology*, Vol. 28, pp 185-191, May 1985.

[10] Fail-Safe Technology,"Report on Failure Characteristics of the NMOS and PMOS SMARTPAC," 18 July 1986.

[11] H. Iwai and S. Kohyama, "On-Chip Capacitance Measurement Circuits in VLSI Structures," *IEEE Tran. Elec. Dev.*, Vol. ED-29, No. 10, pp. 1622-1626, October 1982.

[12] J. Paulos and D. Antoniadis, "Measurement of Minimum-Geometry MOS Transistor Capacitances," *IEEE Tran. Elec. Dev.*, Vol. ED-32, No. 2, pp. 357-363, February, 1985.

[13] H. Iwai, J. Oristian, J. Walker, and R. Dutton, "A Scalable Technique for the Measurement of Intrinsic MOS Capacitance with Atto-Farad Resolution," *IEEE Tran. Elec. Dev.*, Vol. ED-32, No. 2, pp. 344-356, February, 1985.

[14] M. Furukawa, H. Hatano, and K. Hanihara, "Precision Measurement Technique of Integrated MOS Capacitor Mismatching Using a Simple On-Chip Circuit," *IEEE Tran. Elec. Dev.*, Vol. ED-33, No. 7, pp. 938-944, July, 1986.

[15] T. Chan, A. Wu, P. Ko, and C. Hu, "A Capacitance Method to Determine the Gate-to-Drain/Source Overlap Length of MOSFET's," *IEEE Elec. Dev. Lett.*, Vol. EDL-8, No. 6, pp. 269-271, June, 1987.

[16] P. Richman, *MOS Field-Effect Transistors and Integrated Circuits*, John Wiley & Sons, New York, 1973.

[17] N. Sasaki, "Higher Harmonic Generation in CMOS/SOS Ring Oscillators," *IEEE Trans. Elec. Dev.*, Vol. ED-29, pp. 280-283, 1982.

[18] T. W. Houston, "Comments on 'Higher Harmonic Generation in CMOS/SOS Ring Oscillators,'" *IEEE Trans. Elec. Dev.*, Vol. ED-30, pp. 958-959, 1983.

[19] I. Ohkura, K. Okazaki, and Y. Horiba, "A New Exact Delay Logic Simulation for ED MOS LSI," *Proceedings IEEE Int. Conf. Cir. Comp.*, p. 953, 1980.

[20] E. S. Anolock and L. Y. Chen, "Application of Step Stress to Time Dependent Breakdown," *Proc. 19th Rel. Phys. Symp.*, p. 23, 1981.

[21] E. S. Anolock and L. Y. Chen, "Screening of Time Dependent Dielectric Breakdown," *Proc. 20th Rel. Phys. Symp.*, p. 238, 1982.

[22] A. Berman, "Time-Zero Dielectric Reliability Test by a Ramp Method," *Proc. 19th Rel. Phys. Symp.*, p. 204, 1981.

[23] P. S. Winokur, J. R. Schwank, P. J. McWorter, P. V. Dressendorfer, and D. C. Turpin, "Correlating the Radiation Response of MOS Capacitors and Transistors," *IEEE Trans. on Nucl. Sci.*, Vol. NS-31, pp. 1453-1460, 1984.

[24] W. Fichtner and H. W. Potzl, "MOS Modeling by Analytical Approximations: Subthreshold Current and Threshold Voltage," *Int. J. Elec.*, Vol. 46, pp. 33 - 55, 1979.

[25] S. M. Sze, *Physics of Semiconductor Devices*, John Wiley and Sons, New York, 1969.

[26] R. M. Swanson and J. D. Meindl, "Ion-Implanted CMOS transistors in Low-Voltage Circuits," *IEEE J. Solid-State Circ.*, SC-7, p. 145, 1972.

[27] A. Vladimirescu and S. Liu, "The Simulation of MOS Integrated Circuits Using SPICE2," Memorandum No. UCB/ERL M80/7, February 1980.

[28] P. Antognetti, D. D. Caviglia, and E. Profumo, "CAD Model for Threshold and Subthreshold Conduction in MOSFET's," *IEEE J. Solid-State Circ.*, Vol. SC-17, pp. 454 - 458, 1982.

[29] A. H.-C. Fung, "A Subthreshold Conduction Model for BSIM," Memorandum No. UCB/ERL M85/22, March 1985.

[30] M. G. Buehler and Y.-S. Lin, "Comparison of Results From Simple Expressions for MOSFET Parameter Extraction," *Proc. IEEE Conf. Microelectronic Test Structures*, Vol. 1, pp. 90-96, 1988.

[31] R. L. Mattis, "A FORTRAN Program for Analysis of Data from Microelectronic Text Structures," National Bureau of Standards Special Publication 400-75, July 1983.

[32] H. Akima, *Collected Algorithms from ACM, Algorithm 526*, revised June 6 1977: ACM 1978.

[33] ACM Transactions on Mathematical Software, Vol. 4, No. 2, pp. 160-164, June 1978.

[34] D. K. Nichols, W. E. Price, and C. Malone, "A Guideline for Heavy Ion Radiation Testing for Single Event Upset," JPL Publication 84-22, 1984.

[35] M. G. Buehler, B. T. Moore, and R. H. Nixon. "Parameter Extraction from Spacebourne MOSFETs," *IEEE Trans. Nucl. Sci.*, NS-32, pp. 4237-4243, 1985.

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15. Supplementary Notes

16. Abstract

In this effort, advanced measurement methods that use microelectronic test chips are described. These chips are intended to be used in acquiring the data needed to qualify Application Specific Integrated Circuits (ASICs) for space use. This work represents the collaborative effort of integrated-circuit (IC) parts specialists, device physicists, test-chip engineers, and fault-tolerant-circuit designers. Their efforts were focused on developing the technology for obtaining custom ICs from CMOS/bulk silicon foundries. In pursuit of this goal, a series of test chips has been developed: a Parametric Test Strip, a Fault Chip, a set of Reliability Chips, and the CRRES (Combined Release and Radiation Effects Satellite) Chip, a test curcuit for monitoring space radiation effects.

The technical accomplishments of the effort include: (1) Development of a Fault Chip that contains a set of test structures used to evaluate the density of various process-induced defects; (2) Development of new test structures and testing techniques for measuring gate-oxide capacitance, gate-overlap capacitance, and propagation delay; (3) Development of a set of Reliability Chips that are used to evaluate failure mechanisms in CMOS/Bulk: interconnect and contact electromigration and time-dependent dielectric breakdown; (4) Development of MOSFET parameter extraction procedures for evaluating subthreshold characteristics; (5) Evaluation of Test Chips and Test Strips on the second CRRES wafer run; (6) Two dedicated fabrication runs for the CRRES Chip flight parts; and (7) Publication of two papers: one on the Split-Cross Bridge Resistor and another on Asymmetrical SRAM Cells for Single-Event Upset Analysis.

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