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M.A. Richard and P.C. Claspy
Case Western Reserve University
Cleveland, Ohio

K.B. Bhasin
Lewis Research Center
Cleveland, Ohio

and

M.B. Bendett
Honeywell, Inc.
Bloomington, Minnesota

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M.A. Richard, P.C. Claspy

Case Western Reserve University, Department of Electrical Engineering
Cleveland, OH 44106

K.B. Bhasin

NASA Lewis Research Center
21000 Brookpark Rd., Cleveland, OH 44135

M.P. Bendett

Honeywell, Inc.
Bloomington, MN

E-5434

ABSTRACT

Optical interconnects are being considered for the high speed distribution of multiplexed control signals in GaAs MMIC-based phased array antennas. This paper describes the performance of a hybrid GaAs optoelectronic integrated circuit (OEIC), along with a description of its design and fabrication. The OEIC converts a 16-bit serial optical input to a 16 parallel line electrical output using an on-board 1:16 demultiplexer and operates at data rates as high as 305 Mbps. The performance characteristics as well as potential applications of the device are presented.

INTRODUCTION

The advantages of large directly radiating phased array antennas for rapid beam scanning are well known, but conventional hardware is heavy and bulky, and architectures for implementing these arrays have resulted in cumbersome, topologically complex, and high loss internal distribution systems. GaAs monolithic microwave integrated circuits (MMIC's), which have undergone extensive development and which could be used as array output modules, represent a major step toward improved and light weight arrays[1]. Yet, the interconnection of these devices into a beam formation network (BFN), is still a rather formidable problem. Conventional methods carrier and control signal distribution to the radiating elements suffer from cross talk and electromagnetic interference between elements. To alleviate these problems, several optics-based signal distribution methods have been proposed as solutions. Among the propose methods are those which use fiber optics to interconnect the BFN's[2-5], and those which use optical processing within the BFN's.[6-9]

The work described here is addressed toward the meeting of needs of fiber optic interconnected BFN's. The GaAs MMIC's in a phased array antenna are relatively complex. They include a variable phase shifter and a variable power amplifier which permit the creation of the aperture phase and amplitude distribution that is appropriate to the desired radiated beam configuration. Some proposed architectures also include a local oscillator and a mixer at each antenna element.[10,11] In fiber optic interconnected systems, optical fibers would be used to carry the control signals to the variable phase shifters and amplifiers as well as the signal to be transmitted

and the local oscillator phase locking signal. All control signals for the array including phase shifter and amplifier control signals could be multiplexed onto one optical channel as seen in Fig. 1. Although the actual rate at which a single phase shifter or power amplifier requires data may be low, the large number of elements involved necessitates a high overall data transfer rate, and thus a wide bandwidth channel will be required. Some demonstrations of the use of optical interconnects in phased array applications, using discrete components, have been reported[12], and Crow et. al., have reported a demultiplexing OEIC[13]. In this paper we report on the design and fabrication of a hybrid, high speed GaAs MESFET integrated circuit optical receiver/demultiplexer.

The constructed device is a hybrid optoelectronic integrated circuit (OEIC). Two GaAs circuits, an optical receiver and a demultiplexer, are packaged together in a 34-pin flatpack with a fiber pigtail attached for optical input. The inputs to the OEIC are a 16 bit optical serial data stream at 830 nm, an electrical high-speed clock, and a synchronization signal (FWBO). The outputs are 16 parallel TTL-level electrical outputs and an input clock divided by 16.

DESIGN AND FABRICATION

A PIN photodiode was chosen in place of the conventional MSM photodetector because of its superior noise performance, its speed capability, and its enhanced photosensitivity. It also has the advantage over the MSM or NPN structures commonly used for monolithic integration in that it can be operated in the photovoltaic mode if necessary since it is an asymmetric device. It was implemented using an interdigitated structure (2 μm finger width, 5 μm finger spacing) with an overall size of 40 μm x 60 μm. To achieve high speed and sensitivity a multi-stage differential amplifier is used to boost the signal from the detector up to logic levels. This amplifier consists of a transimpedance input stage followed by two additional capacitively coupled stages, each with a gain of approximately 10 dB. A constant output level is achieved by using a digital amplifier output section. The output from the receiver chip is fed into the 1:16 demultiplexer, that employs direct coupled FET logic (DCFL) circuitry. Although this does not necessarily provide the optimum speed and power dissipation characteristics, it permits circuit construction using established design rules which have been proven during previous development programs. In order to keep the electrical power consumption as low as possible and to reduce the number of high speed circuits, the demultiplexer design incorporated a high speed front end followed by lower speed stages. The outputs of the demultiplexer chip were designed to drive a TTL load and therefore are the major power consumers in the OEIC.

Optical input to the circuit is achieved through the use of a pigtailed optical multimode fiber with a 50 μm core. The fiber is mounted flush on top of the optical receiver wafer. By polishing the end of the fiber at a 58 degree angle, total internal reflection occurs and the light is forced to exit through the side of the fiber. This scheme allows the use of a planar photodiode without the need to bring the fiber in perpendicular to the device. In addition, some focusing of the light is provided by the fiber's curved surface.

All of the circuits were designed using Honeywell GaAs E/D MESFET design and layout rules, and the entire OEIC is amenable to monolithic integration on a single chip. The design was implemented using Honeywell's GaAs Self-Aligned Gate MESFET

process, which is based on selective ion implantation into 3-inch GaAs substrates. Efforts were made initially to fabricate the integrated optical detectors using the standard E/D MESFET implants. In the final fabrication, however, the process was modified to add deep n+ and p+ implants for the PIN detector to permit more efficient collection of carriers that are photogenerated below the wafer surface. The basic process uses 1 μm gate length FET's with V_T's of -0.6 V for Dmode and +0.3 V for Emode devices. Photolithography is accomplished using a projection aligner with die-by-die alignment. (A cross-sectional view of a wafer at various points in the fabrication process is shown in Fig. 2) In this process, Be and Si are implanted through a thin Si_3N_4 implant cap to form the p-buried layer as well as the enhancement and depletion channels, as shown in Fig. 2a. After channel activation the anneal cap is stripped and the refractory metal gate is sputter-deposited and patterned using reactive ion etching. This gate metal then serves as the self-aligned implant mask for the n+ source and drain implants of the FET's, with photoresist masking outside the device areas. (Fig. 2b) Finally, the PIN detector is photolithographically defined and the deep n+ and p+ implants are made, then annealed with a Si_3N_4 cap, using a rapid optical annealer. Ohmic contacts are formed by evaporation using a AuGe-based metal and then lifted off and sintered (Fig. 2c), and interconnect metallization consists of two-level metals defined by a dielectric-assisted liftoff (DAL) technique. This DAL process, together with filled VIA's for interlevel interconnects, permits a complete planarity of the chip topology, which is important in obtaining a high yield for LSI/VLSI fabrication. Both interconnect levels have sheet resistances less than 0.07 ohms per square, which provides for low IR drops and small RC time constants in complex high-speed circuits.

OPERATION

For testing and characterization the completed circuits were packaged in a 34 lead flatpack with a fiber pigtail. These flatpacks were then mounted in a test fixture for an initial performance test. The test fixture is a circuit board with a card edge connecter for the power supply inputs, and coaxial connections for the RF inputs and demultiplexer outputs. A compression clamp connects the flatpack leads to the circuit board tracings. An HP 8080 serial word generator was used to directly modulate an Ortel laser through an HP bias tee, which in turn fed into the optical controller. The word generator was programmed to cycle a 64 bit word output in an NRZ format, and by viewing the demultiplexer outputs on an HP sampling oscilloscope the operation of the device was confirmed. Because of the 1:16 demultiplexer, each output of the controller cycled a 4 bit word. The maximum clock frequency of the controller, limited by the demultiplexer, was found to be 305 MHz. Due to the oscilloscope's 50 Ω inputs, the waveforms were limited to an amplitude of less than 800 mV. Fig. 3 shows three of the 16 output channels along with the data valid line as viewed with a sampling oscilloscope. In this plot the clock frequency was 240 MHz, and the input data was a repeated 64 bit word.

The controller requires less than 200 μW of optical input power. Although tests at Honeywell have demonstrated that powers as low as 1 μW are sufficient, equipment limitations precluded operation of the device at such low optical powers. The electrical power consumption of the controller was found to be always less than 370 mW, and was measured to be as low as 120 mW in some cases. Because most of the power is consumed by the TTL drivers, the terminations of the output leads affected the power consumption greatly.

Initial tests of the device showed that the outputs had uncertainties. A clean output with a definite bit pattern could only be obtained by adjusting the clock frequency to certain values. In addition, the bit pattern sent to a specific output did not necessarily appear on that output. The latter problem was immediately identified as a timing problem in the synchronization (FWBO) signal; the FWBO pulses were not arriving at the proper moment so that the demultiplexer would know which bit was the first. Because the data was input through the laser, fiber and detector/amplifier while the FWBO was input directly into the demultiplexer, the FWBO arrived before the corresponding data. Likewise, the output uncertainty problem was found to be caused largely by the timing of the high speed clock input, which was out of phase with the optically input data because of propagation path length differences. These problems were overcome by using a pulse generator with a variable delay control to regenerate both the clock and FWBO signals shifted in time.

APPLICATIONS

The optical controller described in this paper was developed primarily for use as a phased array antenna controller. As such, the use of the device has been demonstrated in the control of monolithic Ka-Band phase shifter,[14] and in the control of a 30 GHz 8-element phased array antenna.[15] However, many other applications are conceivable as shown in Fig. 4. The built in demultiplexer makes this OEIC suitable for many high data rate transfer applications including neural networks, signal processing interconnections, and integrated modulator/detector arrays.

CONCLUSION

We have described a hybrid MESFET optical controller capable of data rates as high as 300 Mbps. The device uses less than 370 mW of electrical power and requires less than 200 μW of optical power. Because of the on-board demultiplexer, the OEIC has many potential applications beyond its intended phased array antenna application. A fully monolithic version of this device has been fabricated and will be tested in the near future. This device shows that optical and digital technologies are monolithically integratable, and any additional circuitry such as coding or clock recovery that can be fabricated using E/D MESFET design can easily be added to address a specific application.

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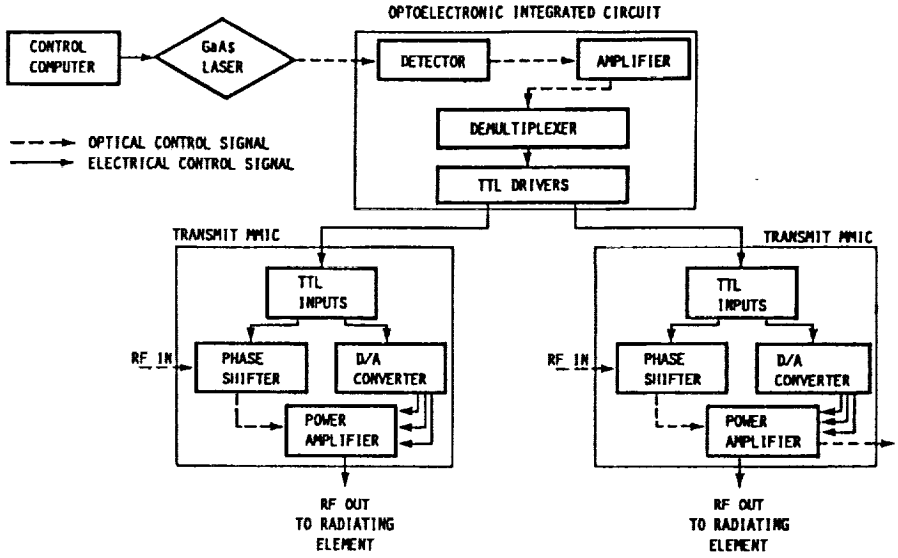

Fig. 1. A possible signal multiplexing scheme.

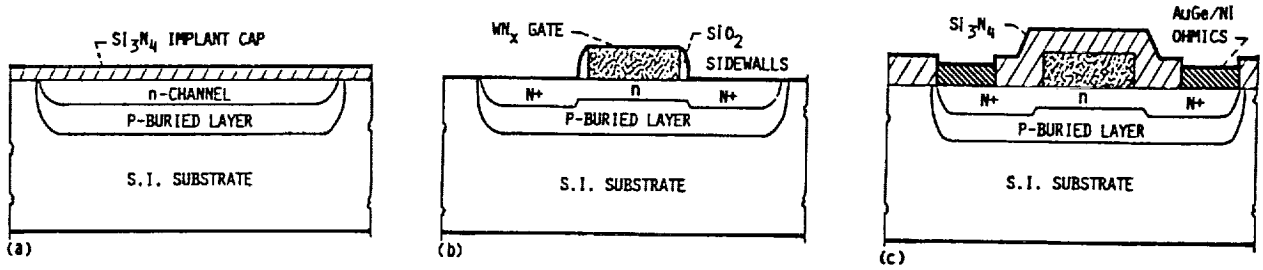

Fig. 2. Fabrication steps: (a) n, n^-, p implantation through Si_3N_4 cap, (b) WN metallization, N^+ implant self-aligned using SiO_2 side-wall spacers, (c) ohmic contact metallization.

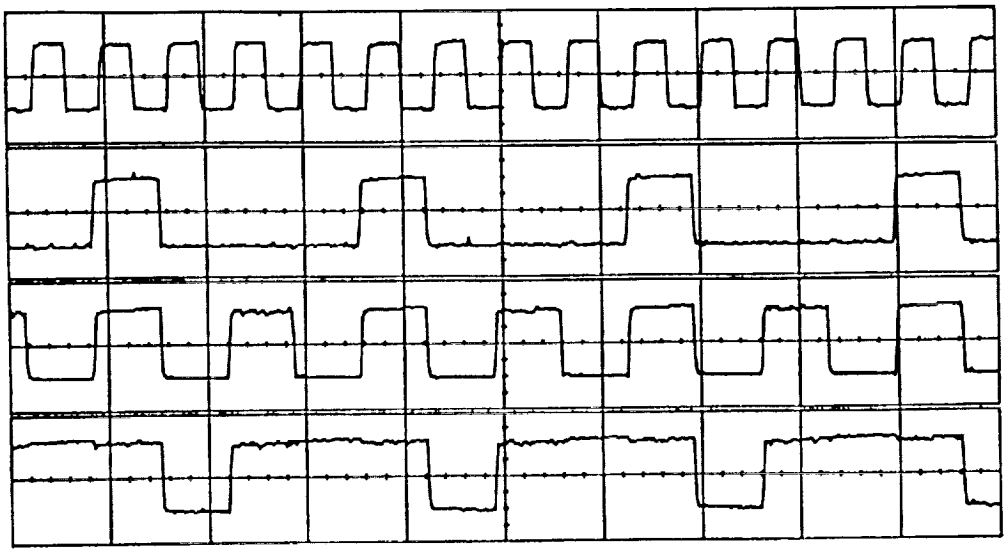

Fig. 3. Outputs of the OEIC. The top trace is the output clock divided by 16 while the lower three traces are data outputs. The input data is a 64 bit repeating word at a clock rate of 240 MHz. The ordinate for each trace is 200 mv/div. while the timebase is 100 ns/div.

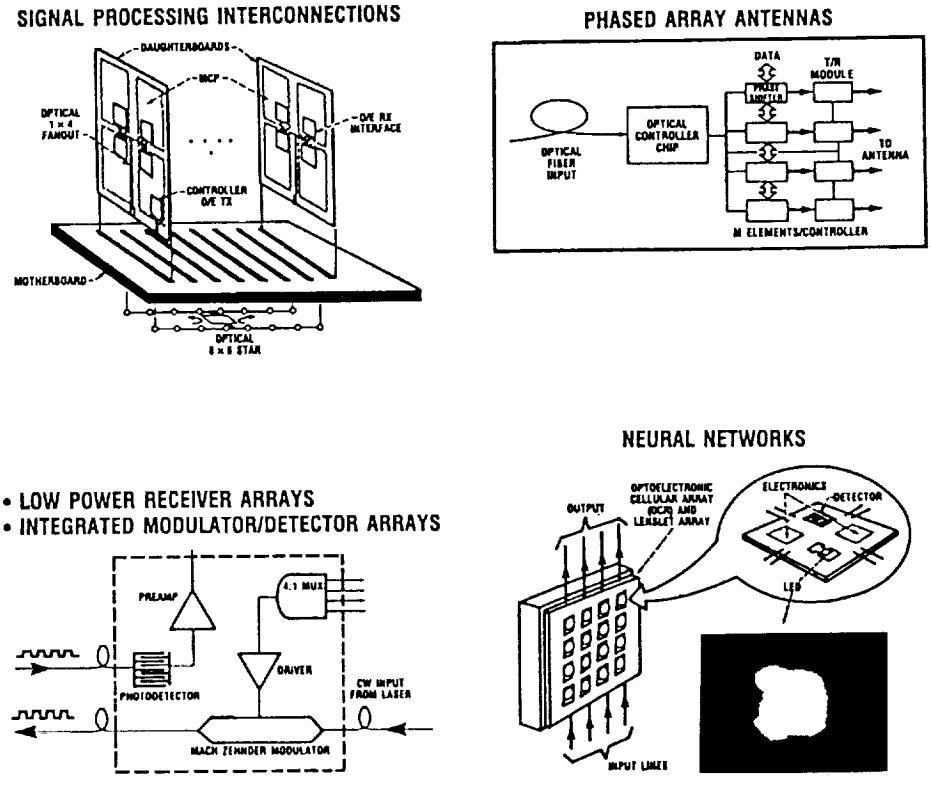

Fig. 4. Potential applications of OEIC include signal processing interconnections, phased array antennas, detector arrays, and neural networks.

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16. Abstract

Optical interconnects are being considered for the high speed distribution of multiplexed control signals in GaAs MMIC-based phased array antennas. This paper describes the performance of a hybrid GaAs optoelectronic integrated circuit (OEIC), along with a description of its design and fabrication. The OEIC converts a 16-bit serial optical input to a 16 parallel line electrical output using an on-board 1:16 demultiplexer and operates at data rates as high as 30b Mbps. The performance characteristics as well as potential applications of the device are presented.

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