VIRGINIA POWER ELECTRONICS CENTER

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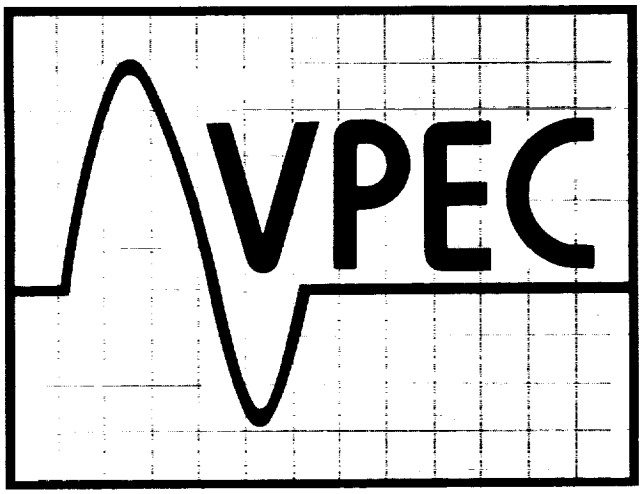
THE BRADLEY DEPARTMENT OF ELECTRICAL ENGINEERING

ANALYSIS AND DESIGN OF A HIGH POWER, DIGITALLY-CONTROLLED SPACECRAFT POWER SYSTEM

SIX MONTH REPORT

PREPARED FOR
NASA/GODDARD SPACE FLIGHT CENTER
GREENBELT, MD 20771
NAG5-1232

PREPARED BY
F.C. LEE AND B.H. CHO



May 16, 1990

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I. SUMMARY

This midterm report describes the progress to date on the Analysis and Design of a High Power, Digitally Controlled Spacecraft Power System. Two quarterly presentations have already been made to NASA Goddard. This report contains the presentation material as well as a summary of the accomplishments to date.

The Statement of Work is divided into two phases.

1. Phase I:

    - Task 1. Battery Discharger Topology Trade-off

2. Phase II:

    - Task 1. ORU Level Modeling and Control
    - Task 2. DC Bus Regulation and Mode Control
    - Task 3.Example Design of Digitally Controlled Spacecraft
    - Task 4.Bus Performance Verification With Model

This report describes the progress on Phase 1, Task 1 and Phase 2 Tasks 1 and 2. The remaining two tasks have just been started.

II. Phase 1, Task 1: Battery Discharger Topology Trade-off

Several battery discharger topologies have been compared for use in the space platform application. The task originally called for a comparison of the following candidate topologies:

1. Boost Converter

2. Tapped-Boost Converter

3. Voltage-Fed Push-Pull with Auto-transformer

4. Current-Fed Push-Pull with Auto-transformer

Updated information has since been provided on the battery voltage specification. Initially it was thought to be in the 30 to 40 V range. It is now specified to be 53 V to 84 V. This eliminated the tapped-boost and the current-fed auto-transformer converters from consideration. After consultations with NASA, it was decided to trade-off the following topologies:

1. Boost Converter

2. Multi-Module, Multi-Phase Boost Converter

3. Voltage-Fed Push-Pull with Auto-transformer

A non-linear design optimization software tool developed by VPEC was employed to facilitate an objective comparison. Non-linear design optimization insures that the best design of each topology is compared.

The results indicate that a four-module, boost converter with each module operating 90 degrees out of phase is the optimum converter for the space platform.

Phase 2, Task 1 : ORU Level Modeling and Control

Large-signal and small-signal models have been generated for the shunt, charger, discharger, battery, and the mode controller. The models were first tested individually according to the space platform power system specifications supplied by NASA. The battery ORU model consists of the battery, charger, and discharger models integrated together. This model was used to investigate issues such as interfacing, control, and paralleling of ORU's.

The effect of battery voltage imbalance on parallel dischargers was investigated with respect to dc and small-signal responses. Similarly, the effects of paralleling dischargers and chargers were also investigated. A solar array and shunt model was included in these simulations. A model for the bus mode controller (power control unit) was also developed to interface the ORU model to the platform power system.

Phase 2, Task 2 : DC Bus Regulation and Mode Control

The small signal models were used to generate the bus impedance plots in the various operating modes. The large signal models were integrated into a system model, and time domain simulations were performed to verify bus regulation during mode transitions. Some changes have subsequently been incorporated into the models. The changes include the use of a four module boost discharger, and a new model for the mode controller, which includes the effects of saturation The new simulations for the boost discharger show the improvement in bus ripple that can be achieved by phase-shifted operation of each of the boost modules.

ANALYSIS AND DESIGN OF A HIGH POWER, DIGITALLY CONTROLLED SPACECRAFT POWER SYSTEM

Quarterly Progress Review

for

NASA Goddard Space Flight Center
Greenbelt, MD

January 31, 1990

Prepared by

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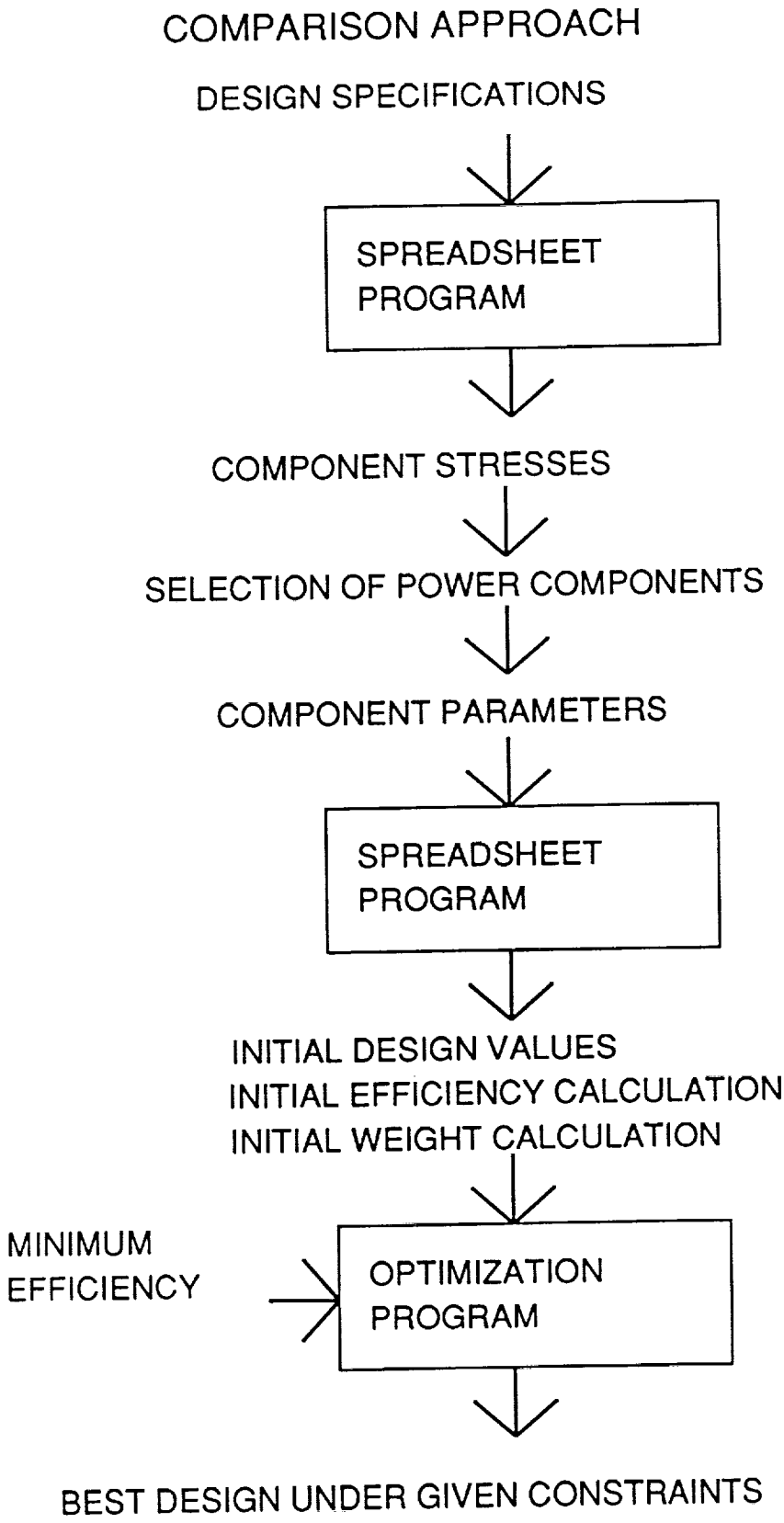
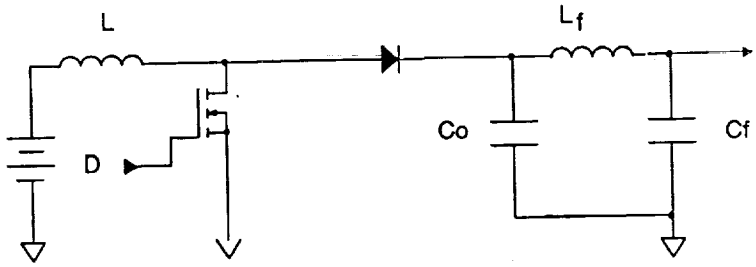
BATTERY DISCHARGER TOPOLOGY TRADEOFF STUDY


COMPARISON APPROACH
DESIGN SPECIFICATIONS
SPREADSHEET PROGRAM
COMPONENT STRESSES
SELECTION OF POWER COMPONENTS
COMPONENT PARAMETERS
SPREADSHEET PROGRAM
INITIAL DESIGN VALUES
INITIAL EFFICIENCY CALCULATION
INITIAL WEIGHT CALCULATION
MINIMUM EFFICIENCY
OPTIMIZATION PROGRAM
BEST DESIGN UNDER GIVEN CONSTRAINTS

BOOST CONVERTER CHARACTERISTICS



Boost Converter with Secondary Filter

SIMPLEST STEP-UP TOPOLOGY

1 SWITCH, 1 DIODE

NO TRANSFORMER

CONTINUOUS INPUT CURRENT

HIGH RMS CURRENT STRESS IN Co

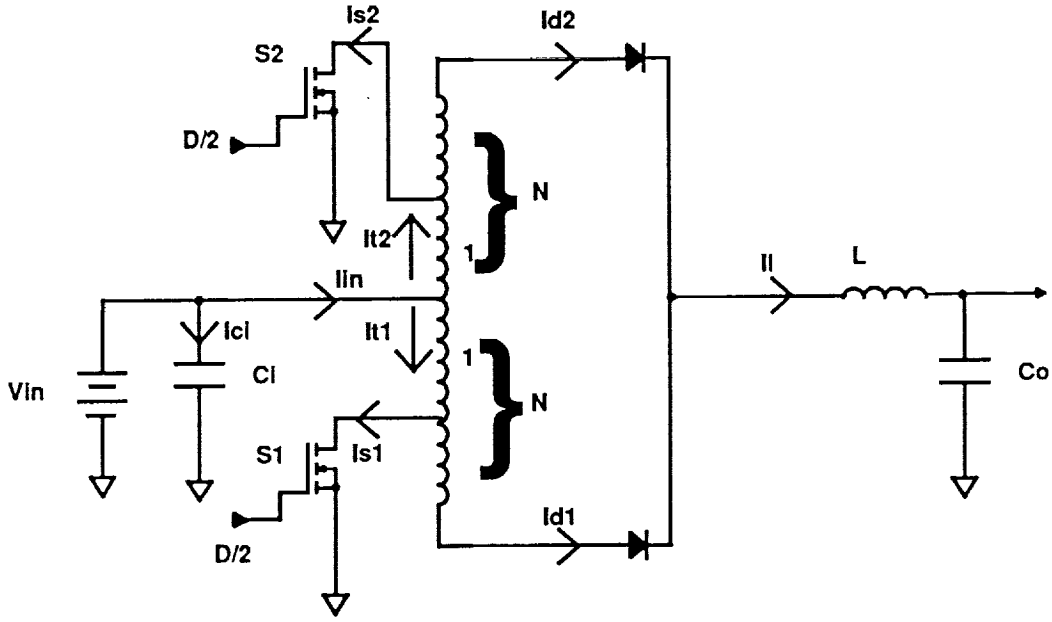
DIFFICULT CONTROL CHARACTERISTICS

MOVING POLES

RIGHT-HALF-PLANE ZERO

CIC NECESSARY TO OBTAIN GOOD PERFORMANCE

VFPPAT CONVERTER CHARACTERISTICS



$Vo/Vi = 1 + ND$

BUCK-TYPE STEP-UP TOPOLOGY
2 SWITCHES, 2 DIODES

CONTINUOUS OUTPUT CURRENT

SEMI-CONTINUOUS INPUT CURRENT

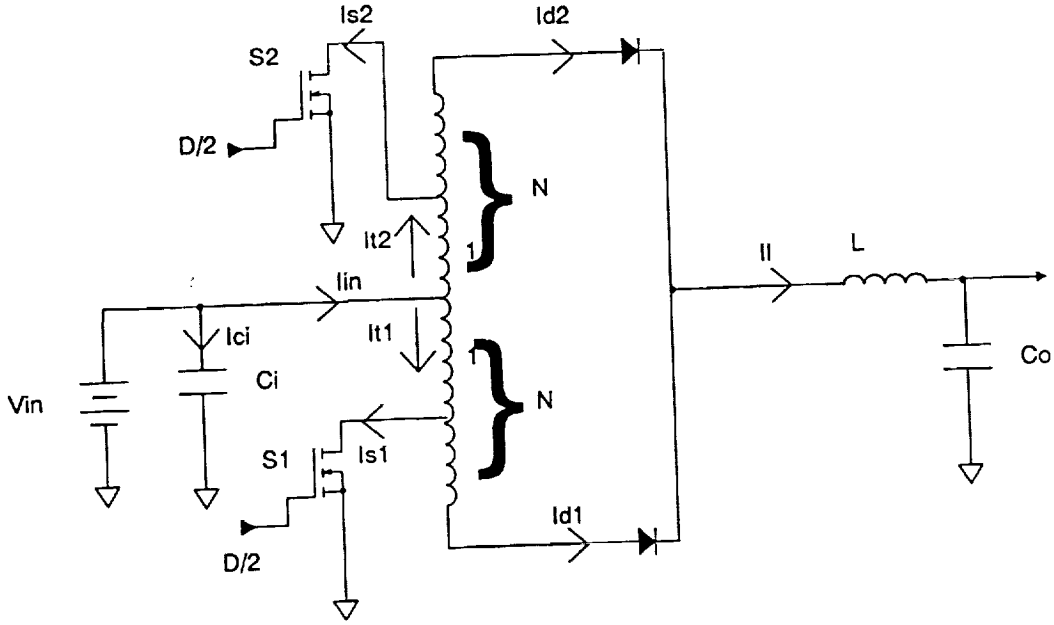
HIGHER SWITCH AND DIODE VOLTAGE STRESS

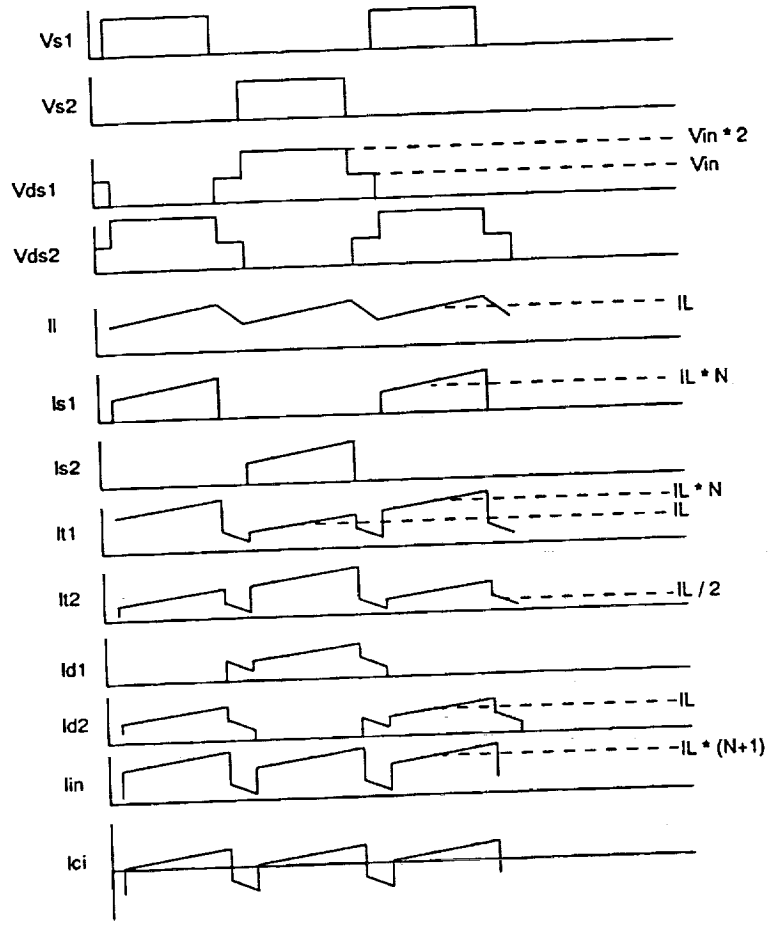
SIMPLER CONTROL CHARACTERISTICS
CIC NECESSARY TO FLUX-BALANCE TRANSFORMER

LOW SWITCHING LOSS

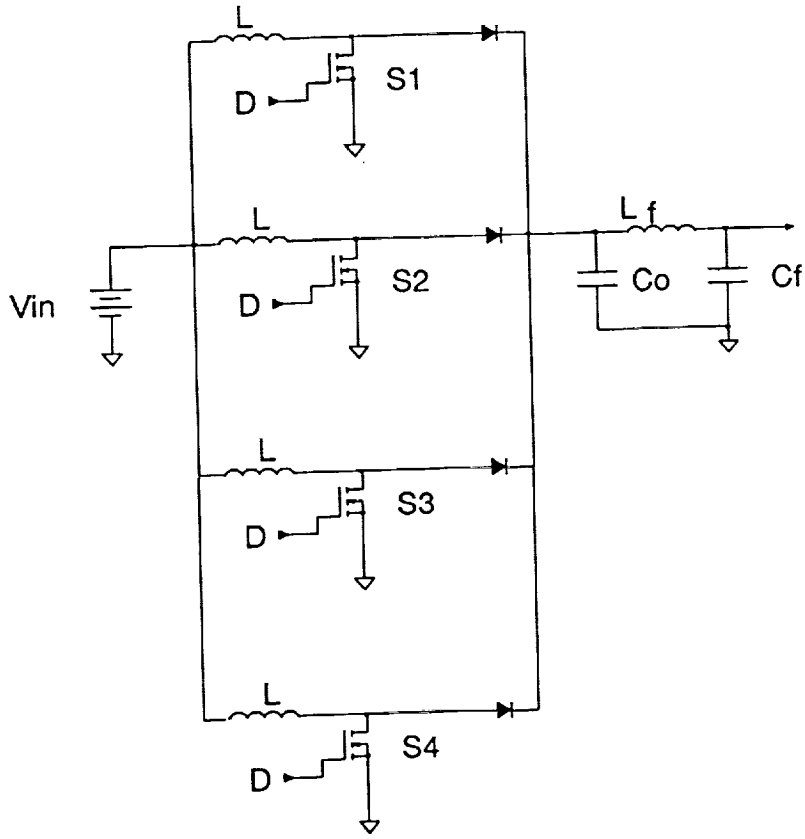
POTENTIALLY HIGH LEAKAGE INDUCTANCE LOSS

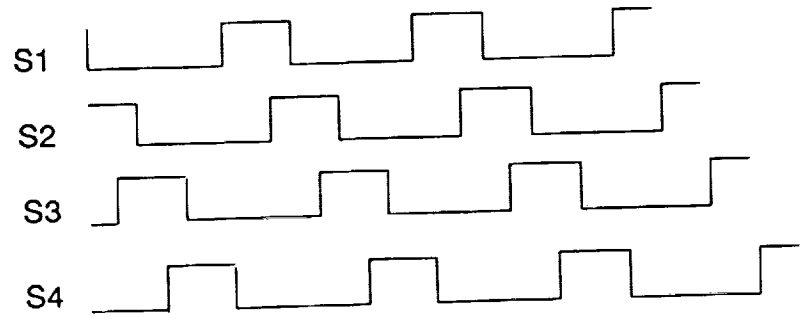
VOLTAGE-FED, PUSH-PULL WITH TAPPED AUTOTRANSFORMER (VFPPAT) CONVERTER





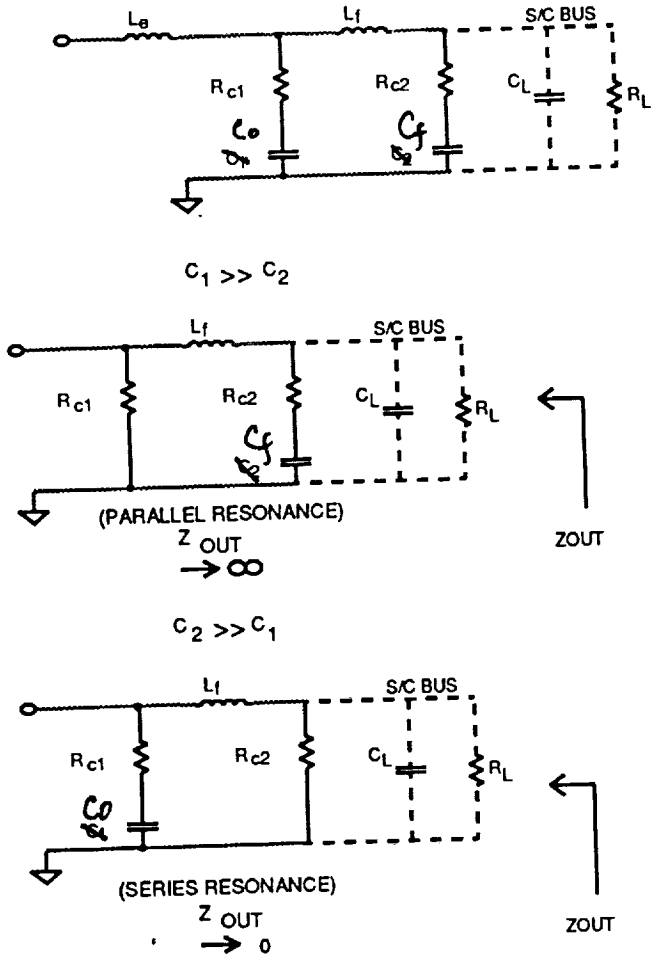
MULTI-MODULE/MULTI-PHASE CONCEPT





DRAMATIC REDUCTION OF OUTPUT CAP. STRESS
BENEFICIAL FOR THE BOOST CONVERTER
MUCH FASTER TRANSIENT RESPONSE POSSIBLE
CAN BE MORE RELIABLE
- CLOSED-LOOP CURRENT SHARING
- N+1 REDUNDENCY

OUTPUT FILTER DESIGN

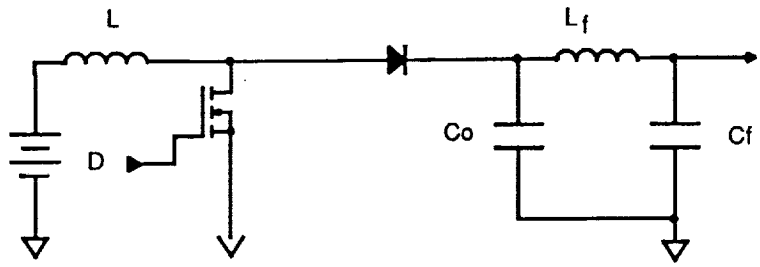


SECOND STAGE CAPACITOR IS BUS CAPACITANCE

DESIGN FOR 1V P-P RIPPLE ON FIRST STAGE

SECONDARY RESONANCE DESIGNED FOR Fs/5

95% EFFICIENT BOOST DESIGN

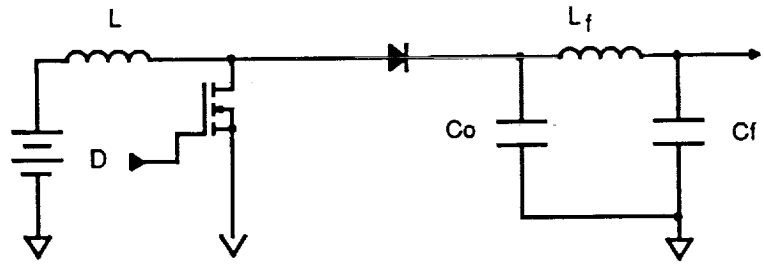


Fs: 110 KHZ
L: 30 uH
C: 70 uF
INDUCTOR TURNS: 11
INDUCTOR CORE WIDTH: 9.5E-3 M
INDUCTOR WINDOW WIDTH: 4.3E-3 M
INDUCTOR AIR GAP: 13 MILS
INDUCTOR WIRE SIZE: 1.03E-6 M^2

LOSS BREAKDOWN
FET CONDUCTION LOSS: 9.5 W
FET SWITCHING LOSSES: 50.0W
DIODE CONDUCTION LOSS: 13.5 W
DIODE SWITCHING LOSSES: 9.4
INDUCTOR COPPER LOSS: 11.4 W
INDUCTOR CORE LOSS: .9 W

WEIGHT BREAKDOWN
INDUCTOR WEIGHT: .02 KG
CAPACITOR WEIGHT .32 KG
TOTAL: .34 KG

97% EFFICIENT BOOST DESIGN

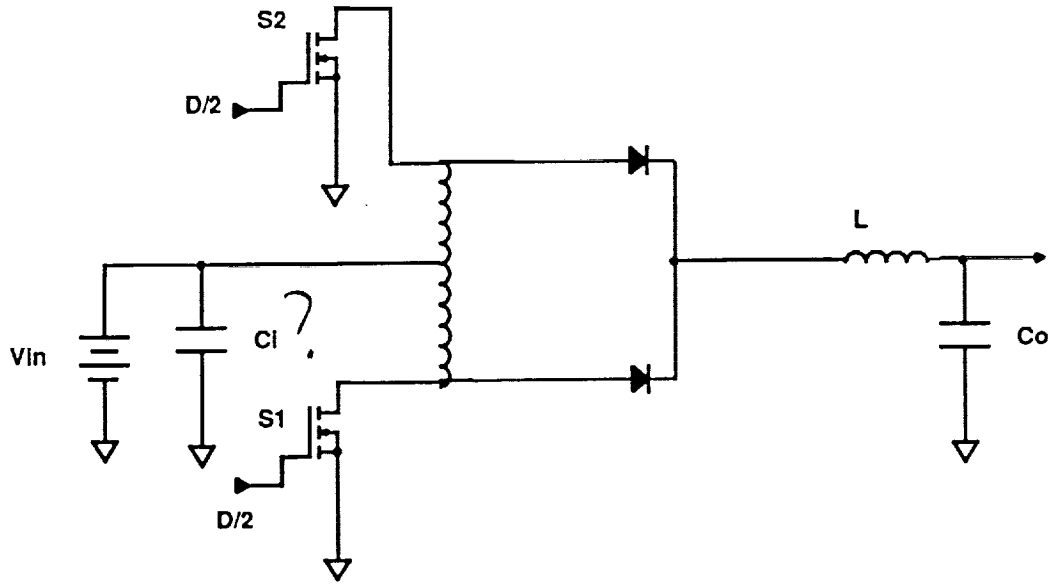


Fs: 45 KHZ
L: 72 uH
C: 180 uF
INDUCTOR TURNS: 22
INDUCTOR CORE WIDTH: 1.1E-2 M
INDUCTOR WINDOW WIDTH: 1.1E-2 M
INDUCTOR AIR GAP: 28 MILS
INDUCTOR WIRE SIZE: 3.2E-6 M^2

LOSS BREAKDOWN
FET CONDUCTION LOSS: 9.1 W
FET SWITCHING LOSSES: 20.3 W
DIODE CONDUCTION LOSS: 13.5 W
DIODE SWITCHING LOSSES: 3.8 W
INDUCTOR COPPER LOSS: 8.1 W
INDUCTOR CORE LOSS: 0.4 W

WEIGHT BREAKDOWN
INDUCTOR WEIGHT: .08 KG
CAPACITOR WEIGHT .74 KG
TOTAL: .82 KG

95% EFFICIENT VFPPAT DESIGN



Fs: 75 KHZ
L: 63 uH
Co: 3 uF
Ci: 25 uF

why do we need to filter the input current
<EMC Concern>

IND. TURNS: 56
IND. CORE WIDTH: 4.1E-3 M
IND. WINDOW WIDTH: 9.3E-3 M
IND. AIR GAP: 32 MILS
IND. WIRE SIZE: 9.3E-7 M^2

XFORMER TURNS: 9
XFROMER CORE WIDTH: 1.3E-2 M
XFORMER WINDOW WIDTH 4.0E-3 M
XFORMER LEAKAGE L: 1.3 uH

LOSS BREAKDOWN

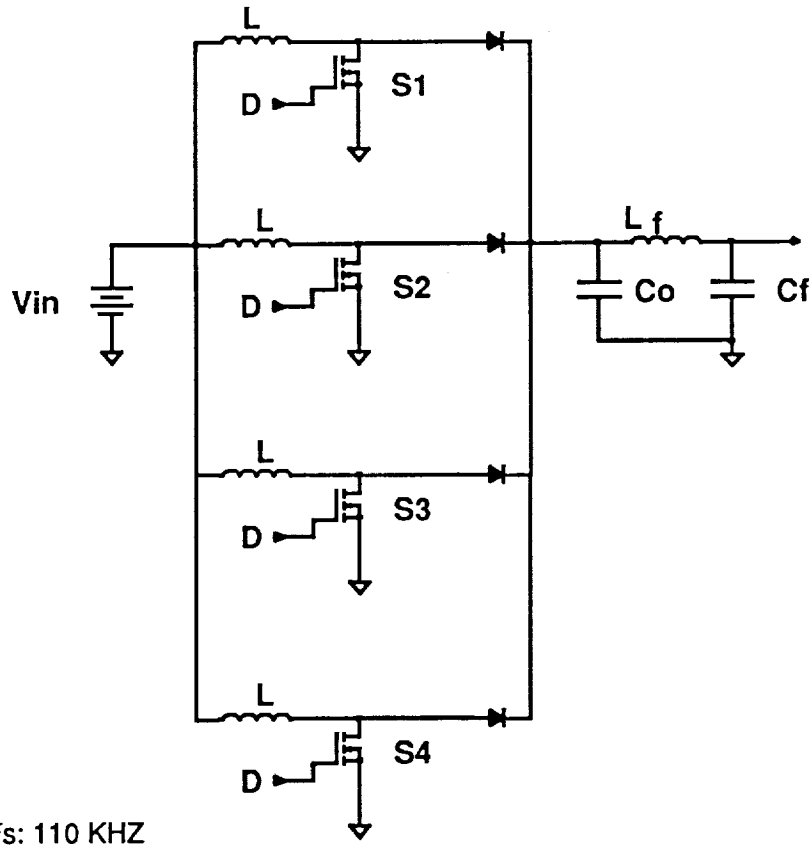
FET CONDUCTION LOSSES: 32.8 W
FET SWITCHING LOSSES: 17.2 W
DIODE CONDUCTION LOSS: 13.5 W
DIODE SWITCHING LOSSES: 7.2
INDUCTOR COPPER LOSS: 7.4 W
INDUCTOR CORE LOSS: 0.0 W

XFORMER COPPER LOSS: 11.0 W
XFORMER CORE LOSS: 1.6 W
XFORMER LEAKAGE LOSS: 5.9 W

WEIGHT BREAKDOWN

INDUCTOR WEIGHT: .01 KG
CAPACITOR WEIGHT .13 KG
XFORMER WEIGHT: .13 KG
TOTAL: 0.27 KG

95% EFFICIENT FOUR MODULE BOOST DESIGN

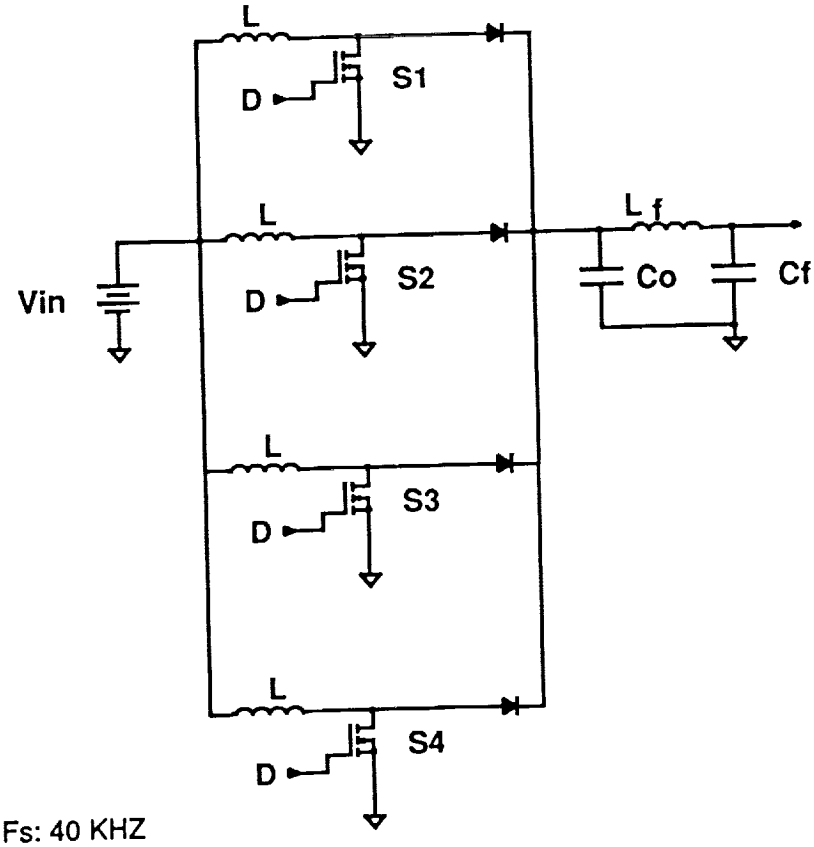


Fs: 110 KHZ
L: 116 uH
C: 25 uF
INDUCTOR TURNS: 13
INDUCTOR CORE WIDTH: 8.7E-3 M
INDUCTOR WINDOW WIDTH: 3.2E-3 M
INDUCTOR AIR GAP: 4 MILS
INDUCTOR WIRE SIZE: 3.6E-7 M^2

LOSS BREAKDOWN
FET CONDUCTION LOSS: 9.6 W
FET SWITCHING LOSSES: 50.0W
DIODE CONDUCTION LOSS: 13.5 W
DIODE SWITCHING LOSSES: 9.4
INDUCTOR COPPER LOSS: 8.7 W
INDUCTOR CORE LOSS: 2.7 W

WEIGHT BREAKDOWN
INDUCTOR WEIGHT: .04 KG
CAPACITOR WEIGHT .11 KG
TOTAL: .15 KG

97% EFFICIENT FOUR MODULE BOOST DESIGN



Fs: 40 KHZ
L: 319 uH
C: 50 uF
INDUCTOR TURNS: 5
INDUCTOR CORE WIDTH: 2.2E-2 M
INDUCTOR WINDOW WIDTH: 1.7E-3 M
INDUCTOR AIR GAP: 2 MILS
INDUCTOR WIRE SIZE: 3.3E-7 M^2

LOSS BREAKDOWN
FET CONDUCTION LOSS: 9.1 W
FET SWITCHING LOSSES: 17.7 W
DIODE CONDUCTION LOSS: 13.5 W
DIODE SWITCHING LOSSES: 3.3 W
INDUCTOR COPPER LOSS: 9.8 W
INDUCTOR CORE LOSS: 5.3 W

WEIGHT BREAKDOWN
INDUCTOR WEIGHT: .23 KG
CAPACITOR WEIGHT .23 KG
TOTAL: .46 KG

CONCLUSIONS

A MULTI-MODULE BOOST CONVERTER OFFERS THE LOWEST WEIGHT BATTERY DISCHARCHER

97% EFFICIENCY IS OBTAINABLE AND PRACTICAL

FLIGHT QUALIFIED PARTS CAN BE USED

BOTH THE VFPPAT AND THE BOOST DESIGNS REQUIRE CIC. VFPPAT FOR FLUX BALANCING, AND THE BOOST FOR DYNAMIC PERFORMANCE AND STABILITY

THE STABILITY MARGIN OF THE BOOST DESIGN CAN BE MADE EQUAL TO THE VFPPAT DESIGN

OUTPUT IMPEDANCE AND LOAD TRANSIENT RESPONSE OF THE BOOST DESIGN CAN BE MADE EQUAL TO OR BETTER THAN THE VFPPAT DESIGN

SPACE PLATFORM ORU-LEVEL MODELING AND CONTROL

SPACE PLATFORM

ORU LEVEL MODELLING AND CONTROL

PHASE II, TASK 1

* BATTERY ORU = BATTERY, CHARGER, & DISCHARGER
  - MODULARITY AND REPLACEMENT
  - REDUNDANCY

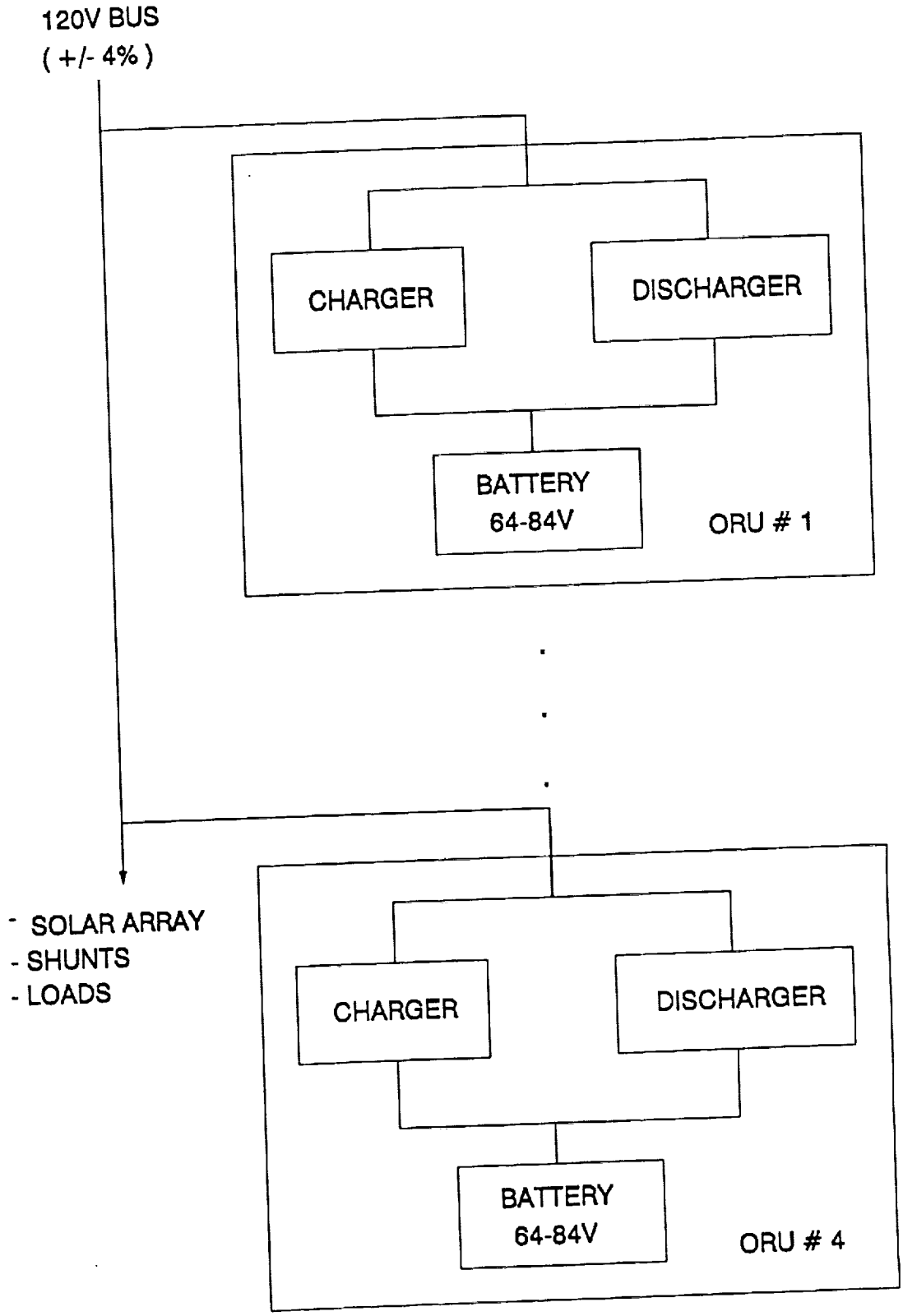
* EASY5 MODEL GENERATION FOR BATTERY ORU
  - USE OF EXISTING COMPONENT MODELS
  - EASE OF PARALLELING

* PARALLELING OF BATTERY ORUs
  -EASY5 SIMULATION
  - ANALYSIS

* BATTERY DISCHARGER PARALLELING

* BATTERY CHARGER PARALLELING
  - CHARGE CURRENT REGULATION
  - BUS VOLTAGE REGULATION

PARALLEL BATTERY ORU MODULES



BATTERY DISCHARGE POWER CONVERTER

* BOOST CONVERTER DESIGN FROM SPREADSHEET

* CONVERTER CHARACTERISTICS
  - Vin = 64 - 84 V
  - Vout = 120 V
  - DUTY RATIO = .30 TO .47
  - EFFICIENCY = 96 %
  - 75 KHz SWITCHING FREQUENCY
  - VOLTAGE RIPPLE < 200mV Pk-Pk
  - OUTPUT POWER = 1500W CONTINUOUS / 1800W PEAK

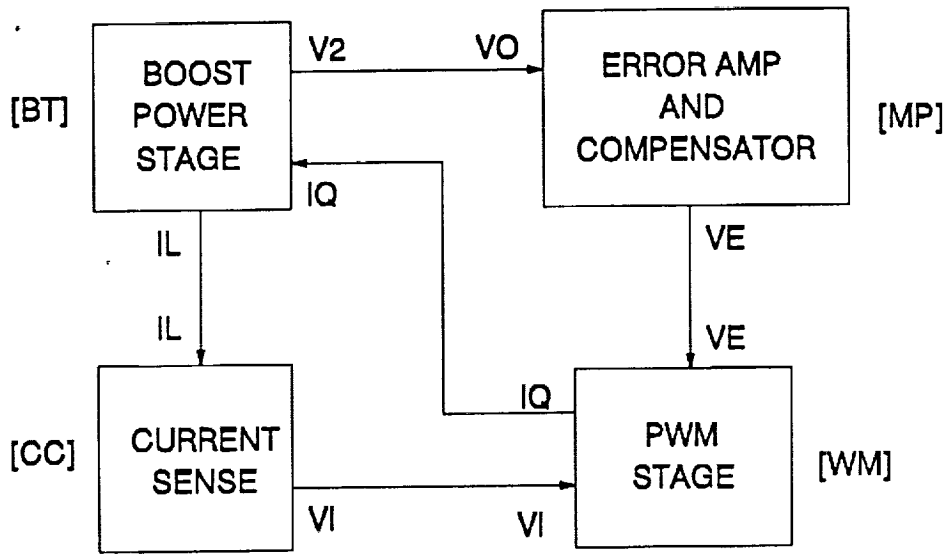
* TWO LOOP CONTROL METHOD
  - SINGLE COMMON VOLTAGE LOOP
  - ONE CURRENT LOOP PER DISCHARGER
  - PRELIMINARY LOOP COMPENSATION

* TWO STAGE FILTERING
  - LOW OUTPUT VOLTAGE RIPPLE
  - LOW OUTPUT IMPEDANCE

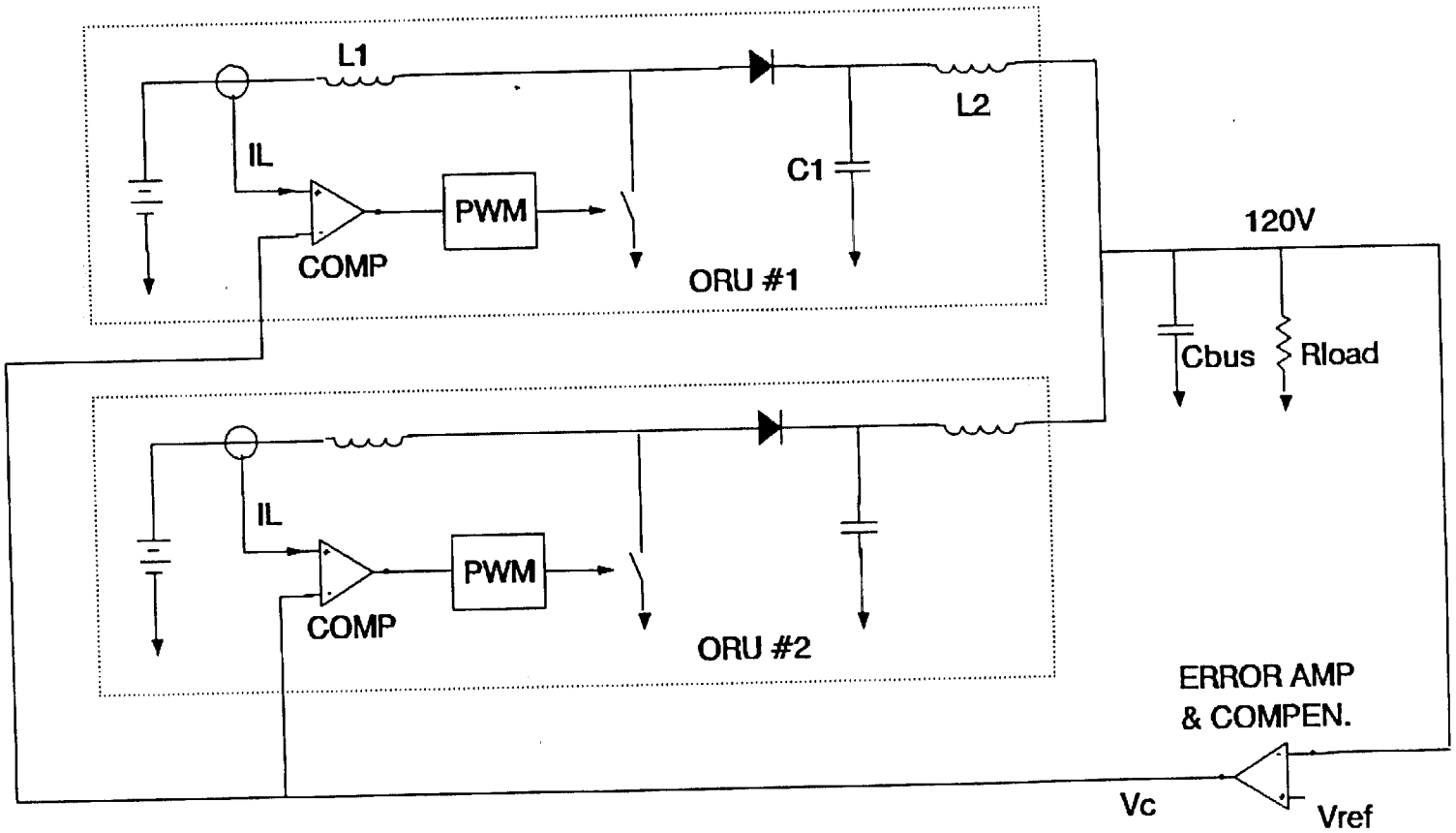
EASY5 DISCHARGE CONVERTER MODEL

* LARGE SIGNAL CHARACTERISTICS

* DISCRETE CIRCUIT EQUATIONS
  - CONTINUOUS CONDUCTION MODE
  - DISCONTINUOUS CONDUCTION MODE



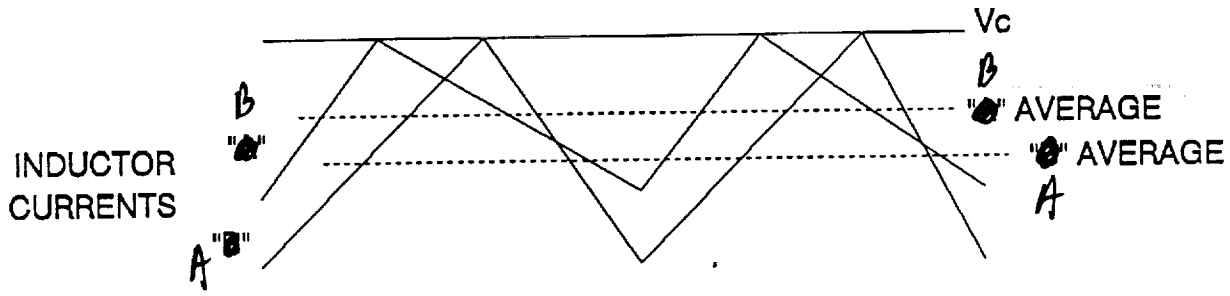
PARALLEL DISCHARGER CONTROL



DC ANALYSIS FOR PARALLEL DISCHARGERS

* BATTERY VOLTAGE IMBALANCE
  - CHARGE IMBALANCE
  - SHORTED CELL

* CURRENT MODE CONTROL : CURRENT SHARING
  - BATTERY CURRENT = INDUCTOR CURRENT
  - PEAK CURRENT DETECTION



$$\frac{dI}{dt} = \frac{dV}{L}$$

BATTERY "B" VOLTAGE > BATTERY "A": VOLTAGE

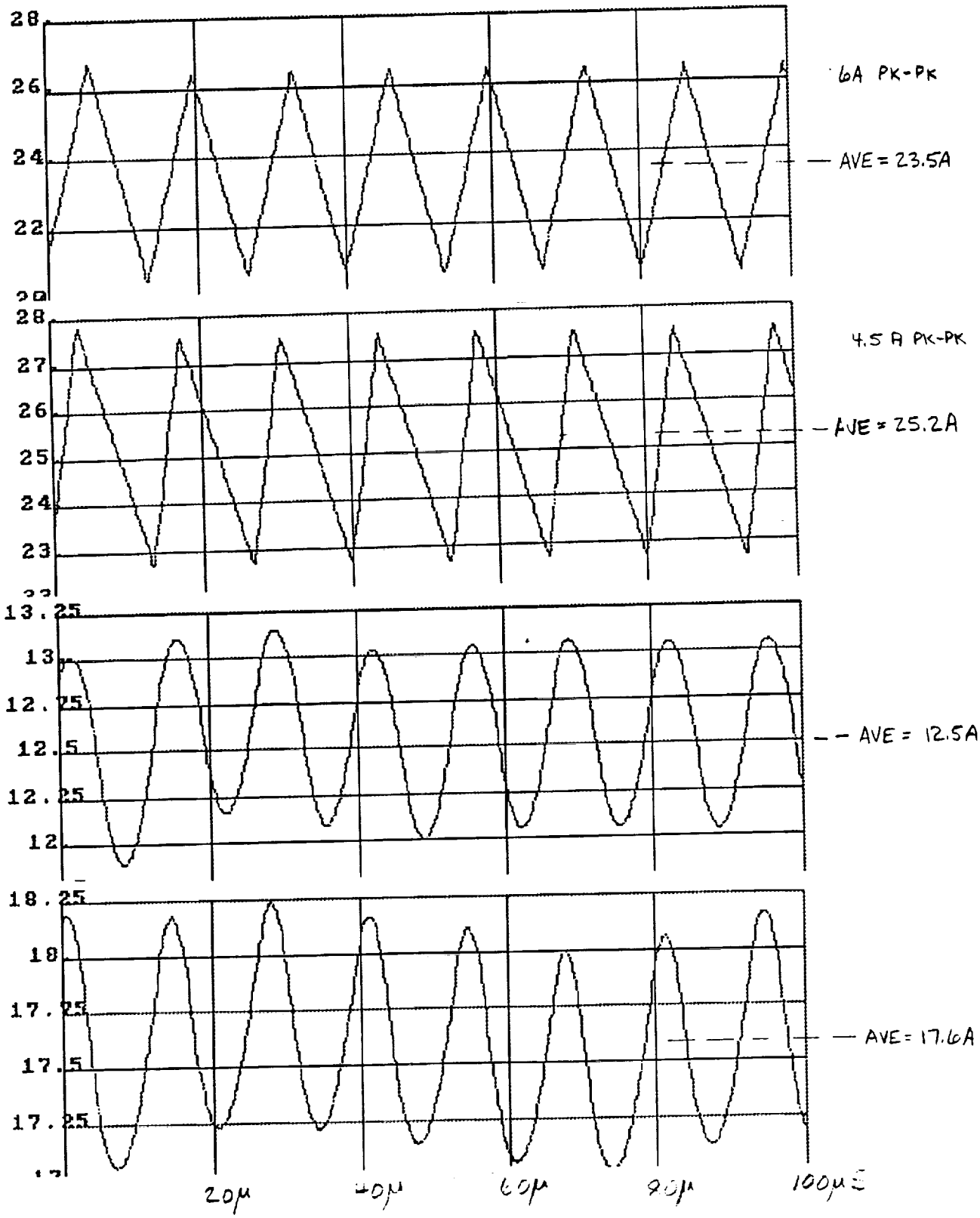
RESULT : BATTERY "B" AVERAGE CHARGE CURRENT IS HIGHER

* Free Running
* Freq. mismatch.

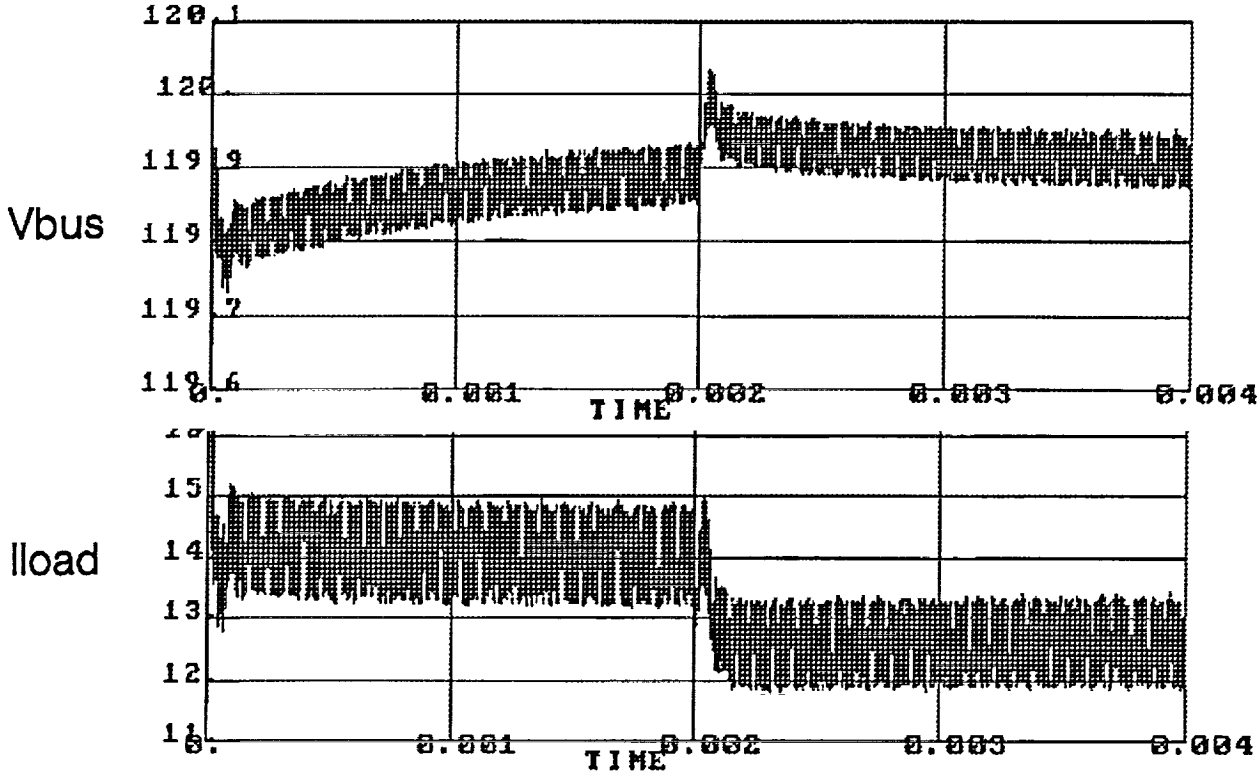
PARALLEL DISCHARGER CURRENTS

BATTERY "A" = 64V , BATTERY "B" = 84V

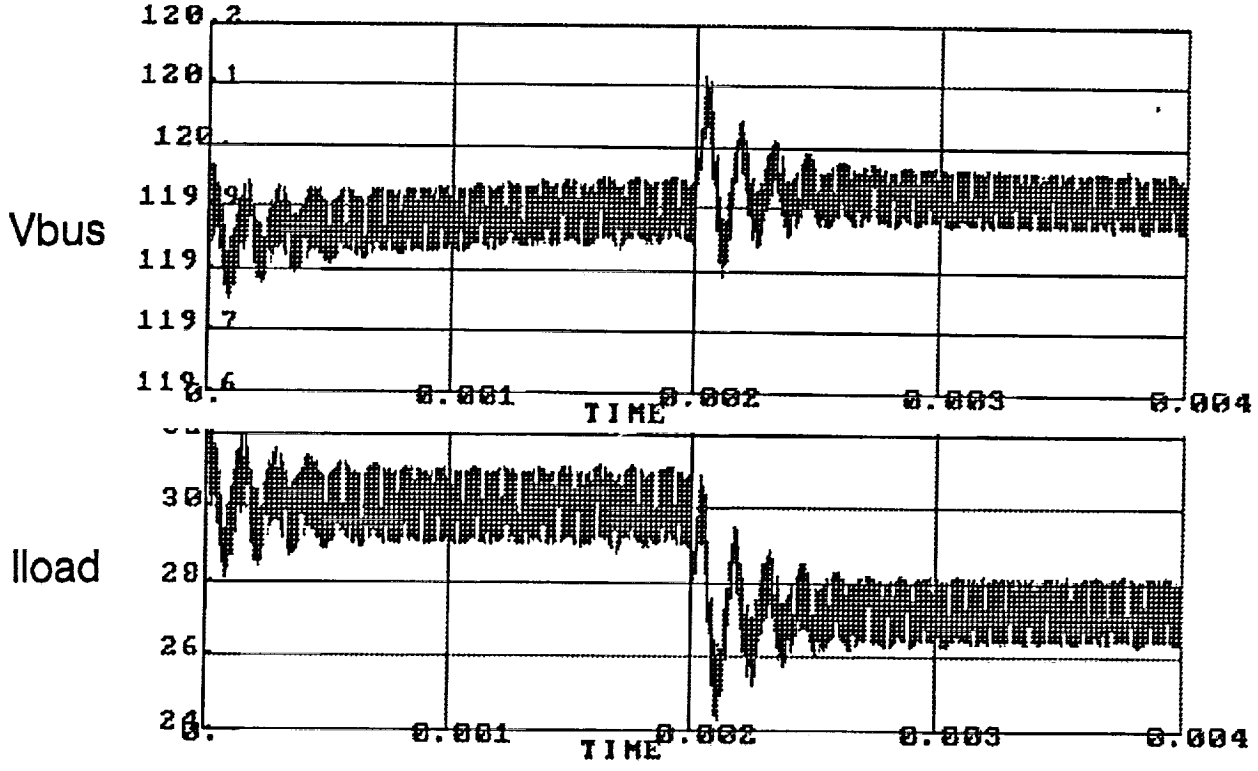
Check peak value



SINGLE DISCHARGER TRANSIENT RESPONSE



PARALLEL DISCHARGER TRANSIENT RESPONSE



SAME COMPENSATION

SMALL SIGNAL ANALYSIS OF PARALLEL DISCHARGERS

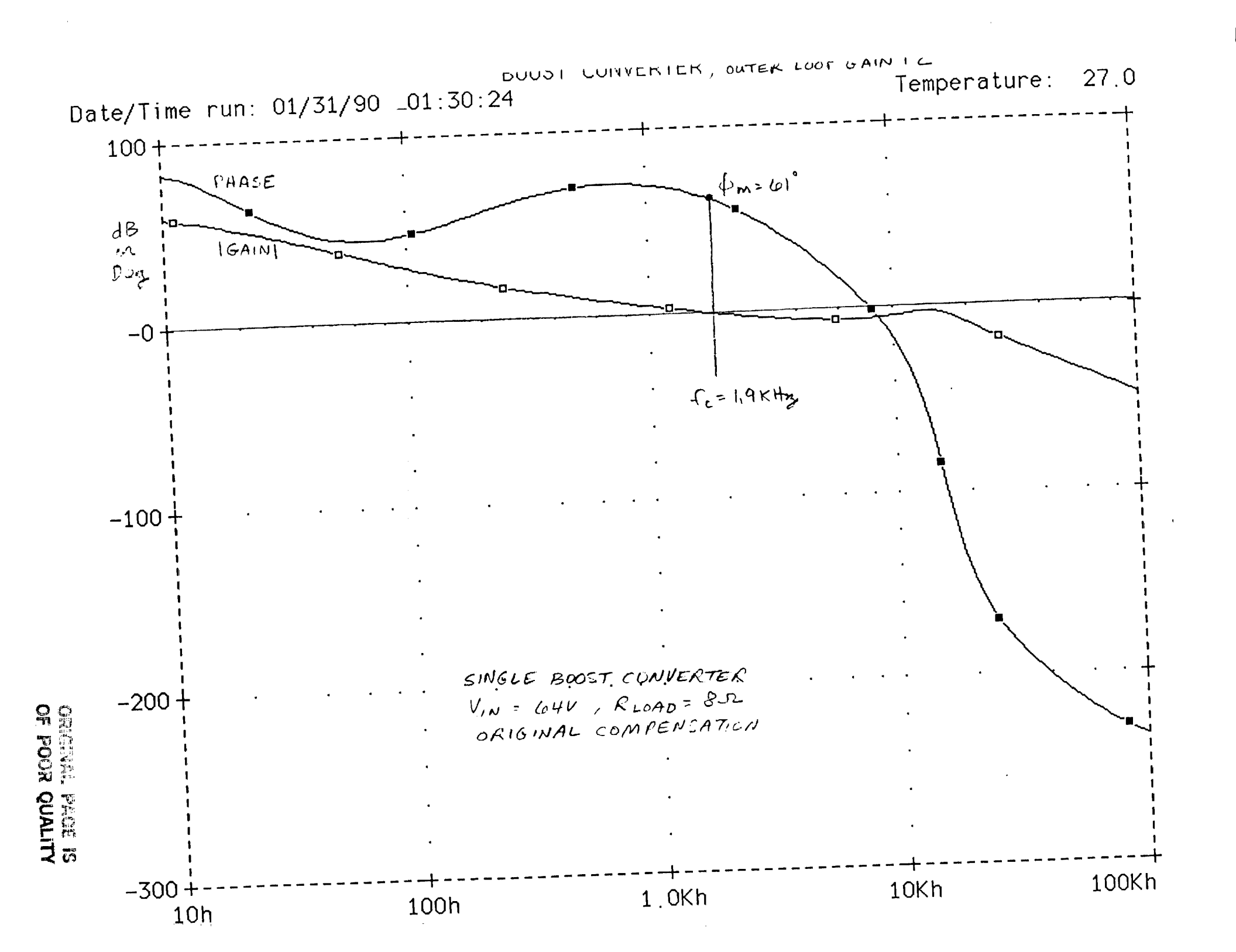
* STABILITY MODIFIED BY ADDING PARALLEL MODULES

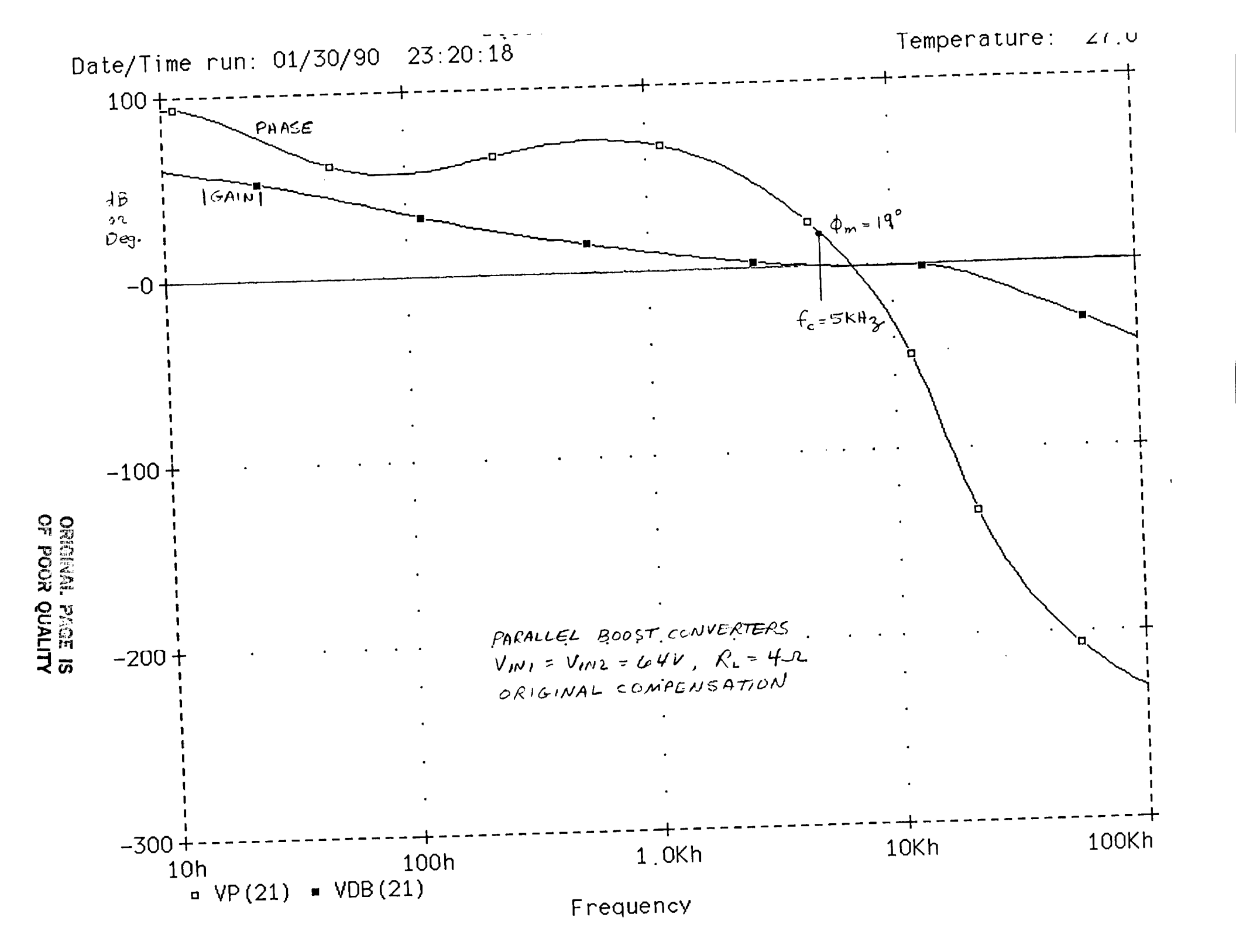
* MODIFICATION OF FILTER CORNER FREQUENCIES
  - FIRST CORNER FREQUENCY = VARIABLE
  - SECOND CORNER FREQUENCY = FIXED

* WORST CASE IS FOUR PARALLEL DISCHARGERS

* LOOP RECOMPENSATION NECESSARY

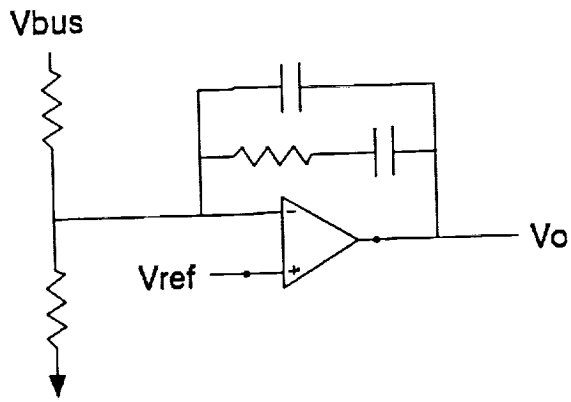
* SPICE MODEL FOR FEEDBACK LOOP ANALYSIS





LOOP RECOMPENSATION FOR PARALLEL DISCHARGERS

* TWO POLE & ONE ZERO COMPENSATOR



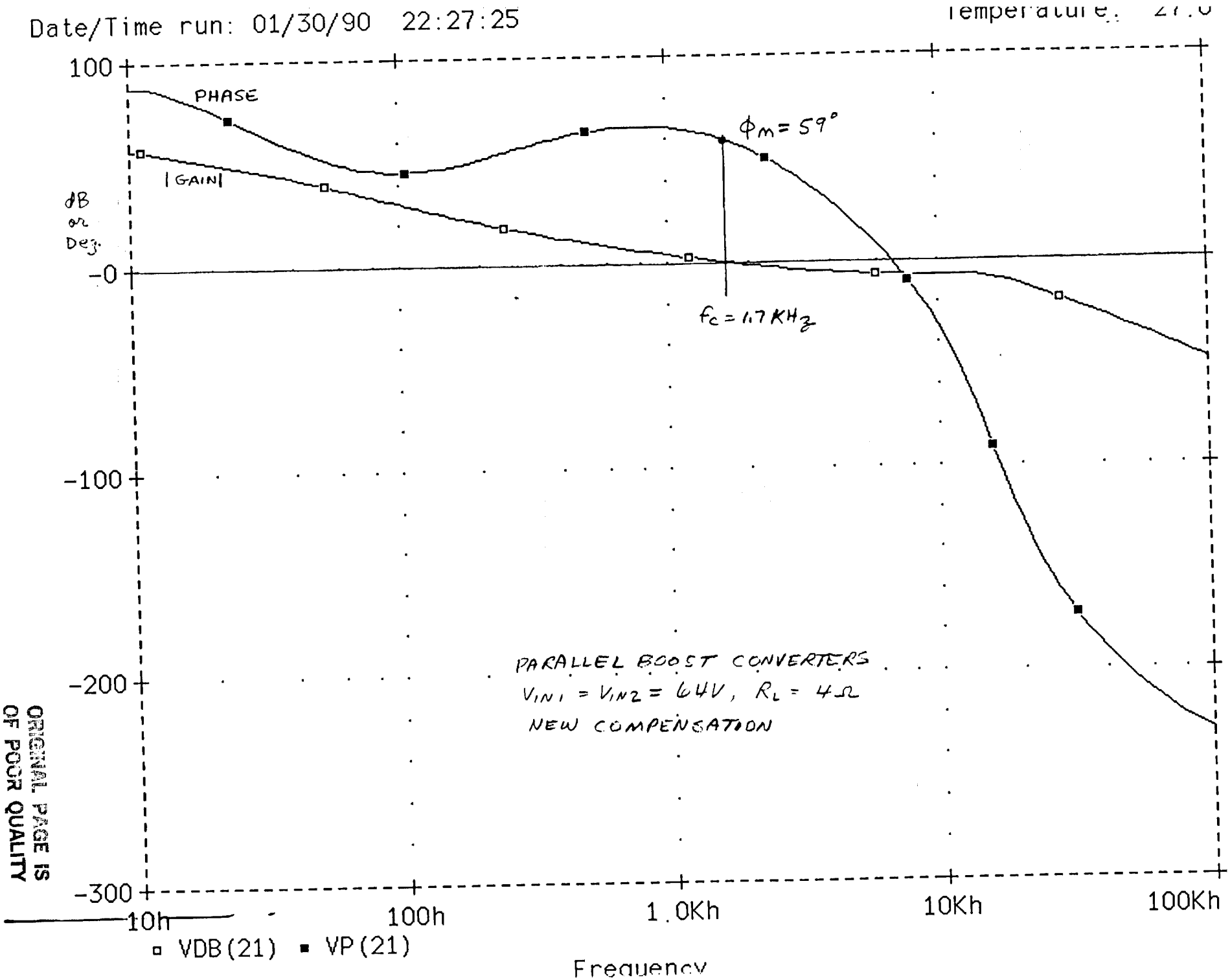
$$\frac{Vo}{Vbus} = \frac{Wm(1 + S/Wz)}{S(1 + S/Wp)}$$

* RECOMPENSATION STRATEGY
  - SHIFT ZERO TO HIGHER FREQUENCY
  - REDUCE DC GAIN

?

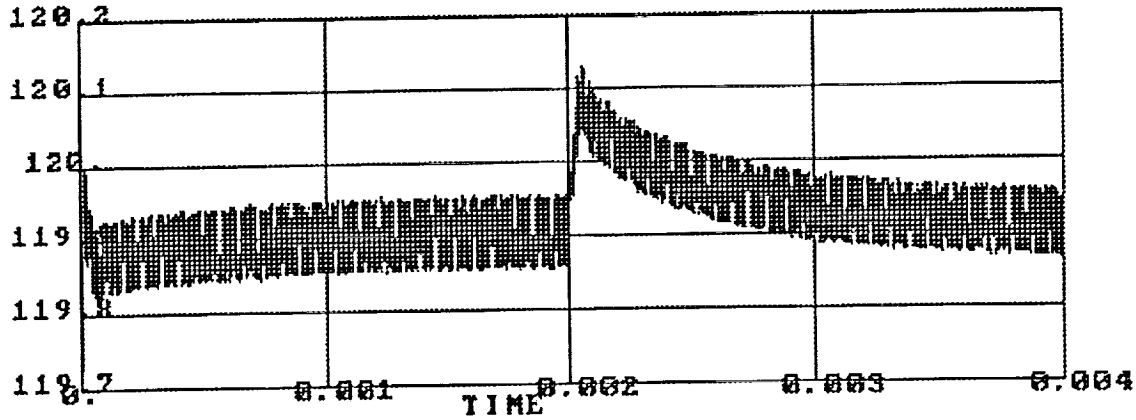
* TRADE-OFF MODULARITY FOR LOOP GAIN & BANDWIDTH

* LOOP GAIN AND PHASE NOT AFFECTED BY BATTERY VOLTAGE IMBALANCE

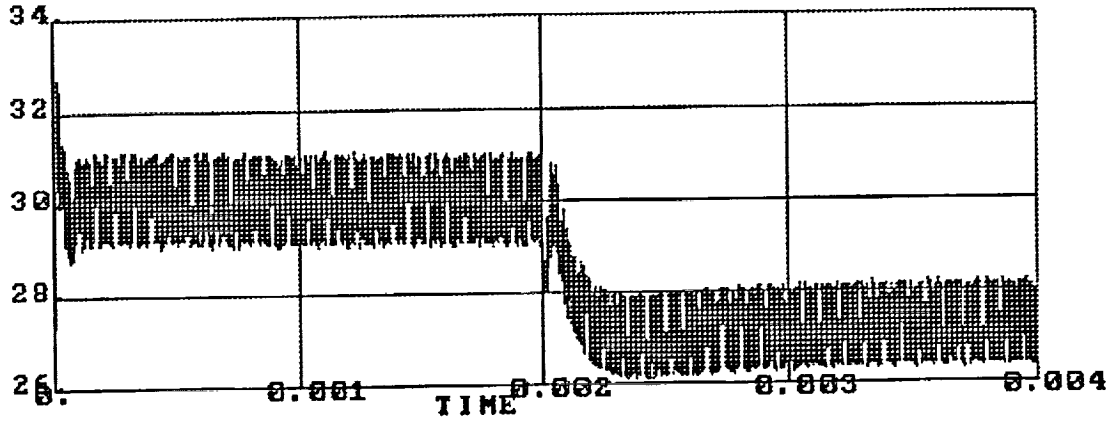


RECOMPENSATED PARALLEL DISCHARGER TRANSIENTS

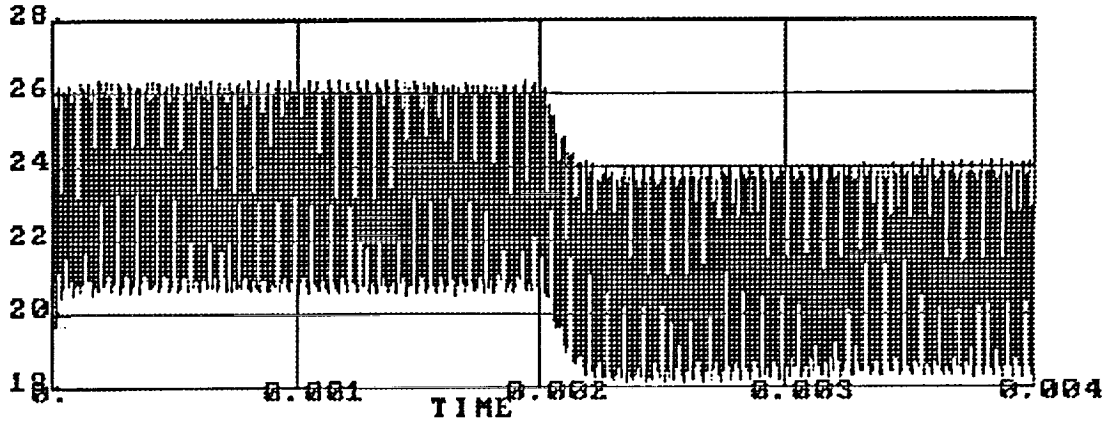
Vbus



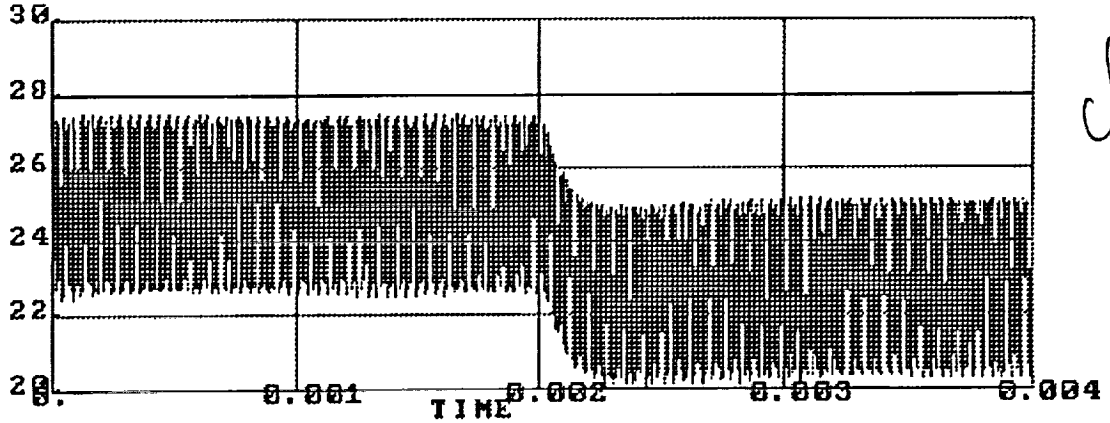
Ibus



IL1
BAT "A"



IL2
BAT "B"



check pea

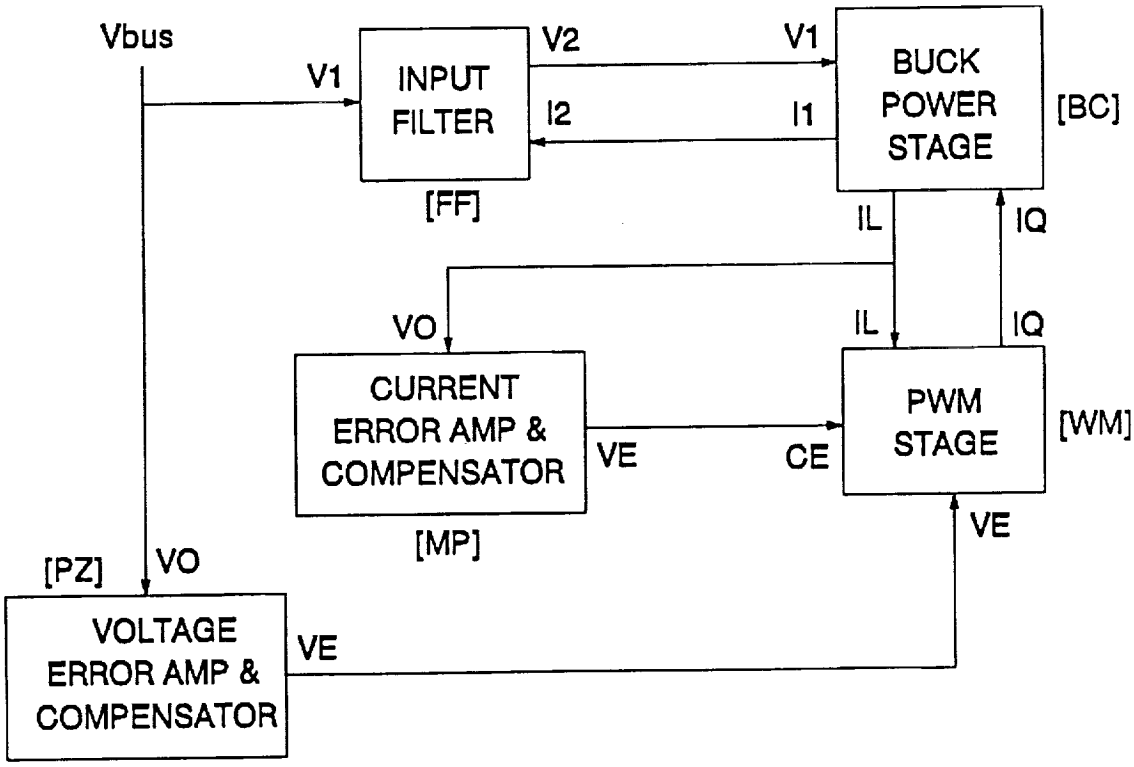
Vbat "A" =64V, Vbat "B" =84V

EASY5 BATTERY CHARGER MODEL

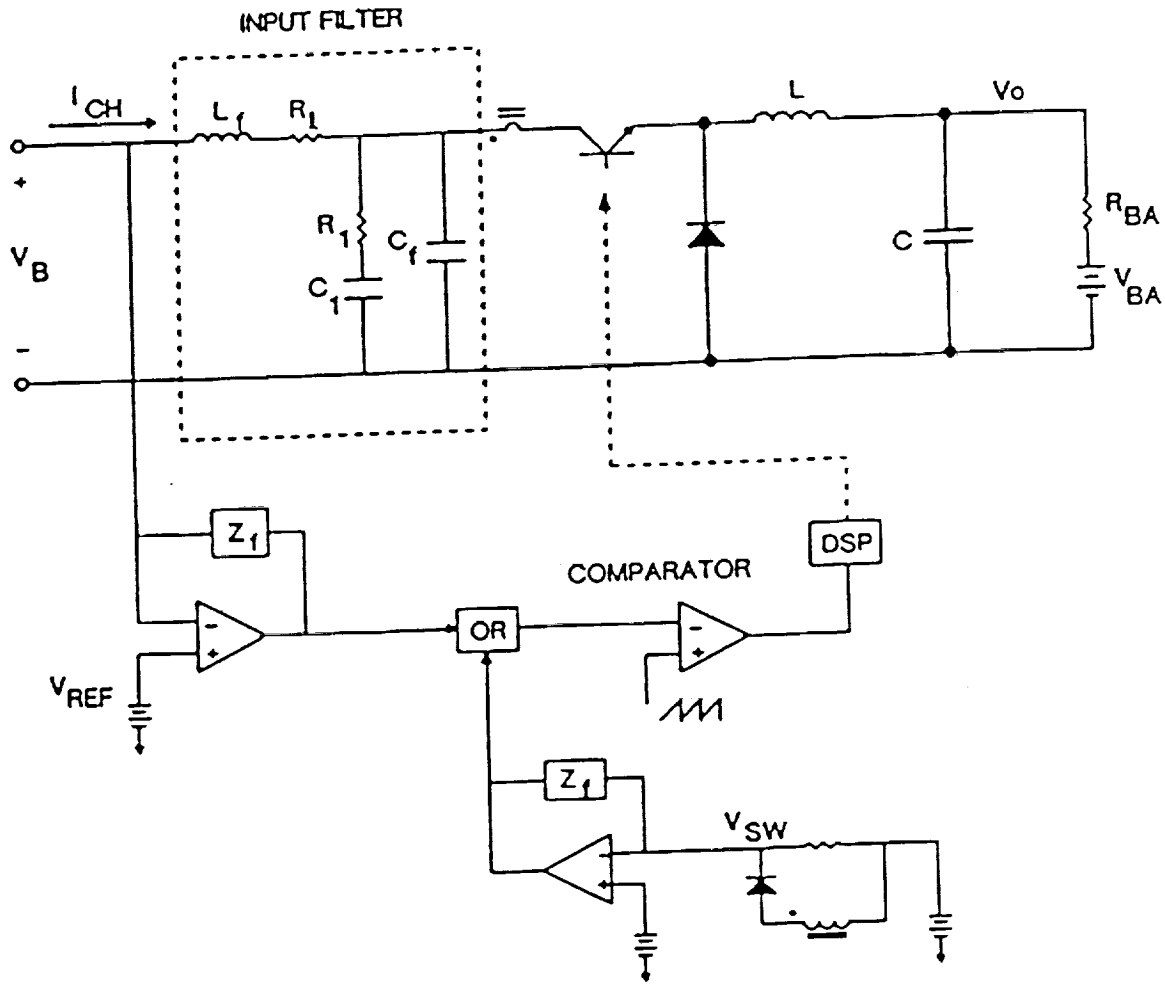
* BUCK CONVERTER EXAMPLE DESIGN FROM FAIRCHILD REPORT

* CHARGE CURRENT REGULATION
  - INDUCTOR CURRENT SENSING & REGULATION
  - CHARGE RATE LIMITING

* BUS VOLTAGE REGULATION
  - CHARGE CURRENT VARIED TO CONTROL BUS VOLTAGE
  - BUCK CONVERTER WITH FEEDFORWARD OF Vbus
    OR
    BOOST CONVERTER WITH FEEDBACK OF Vbus

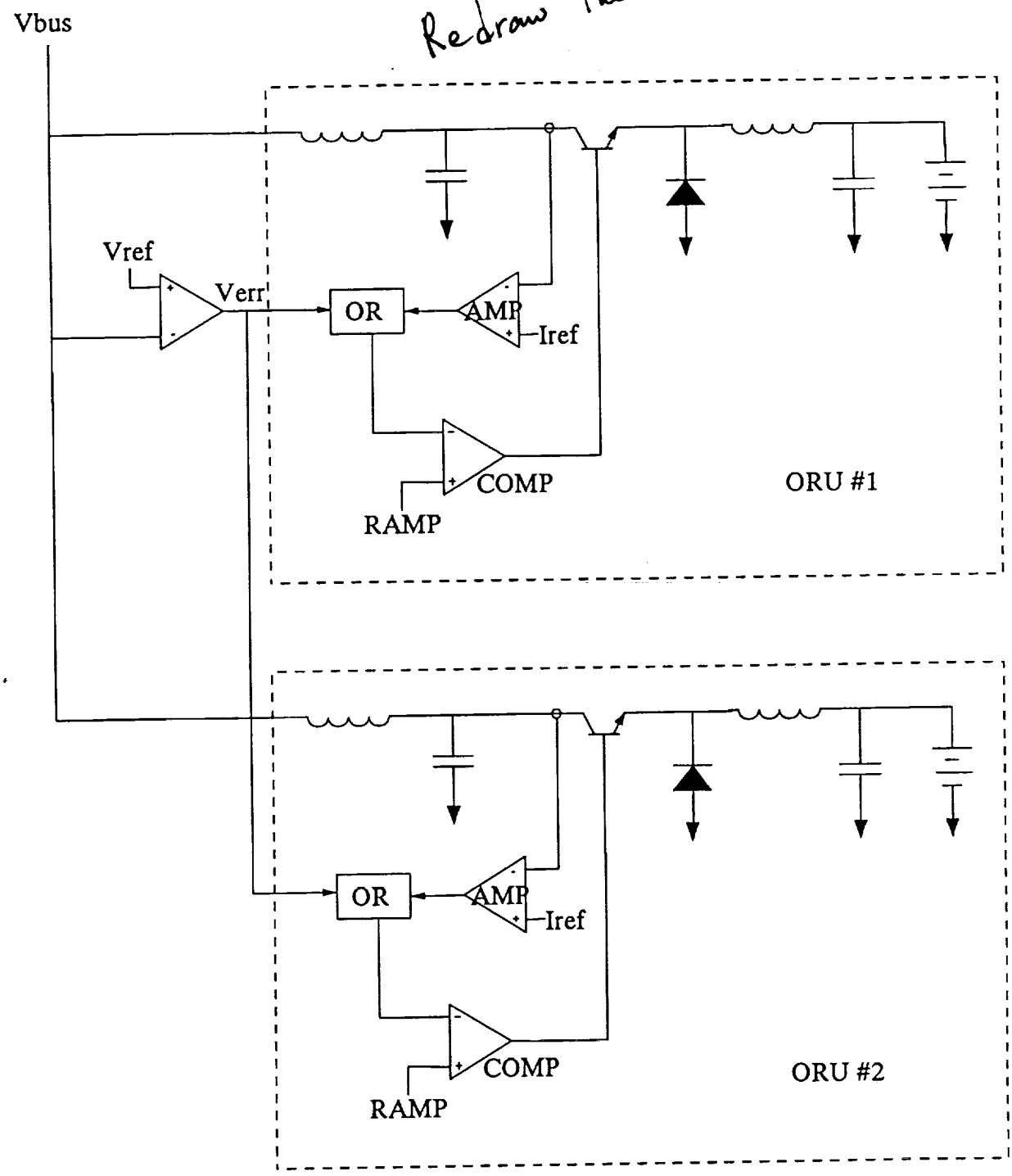


Battery Charger Circuit



PARALLEL CHARGER MODEL

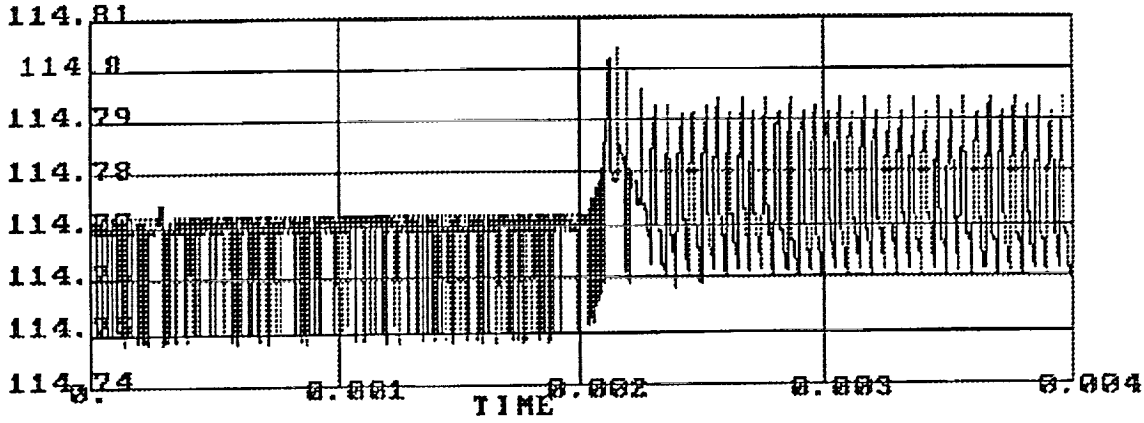
Redraw the block diagram



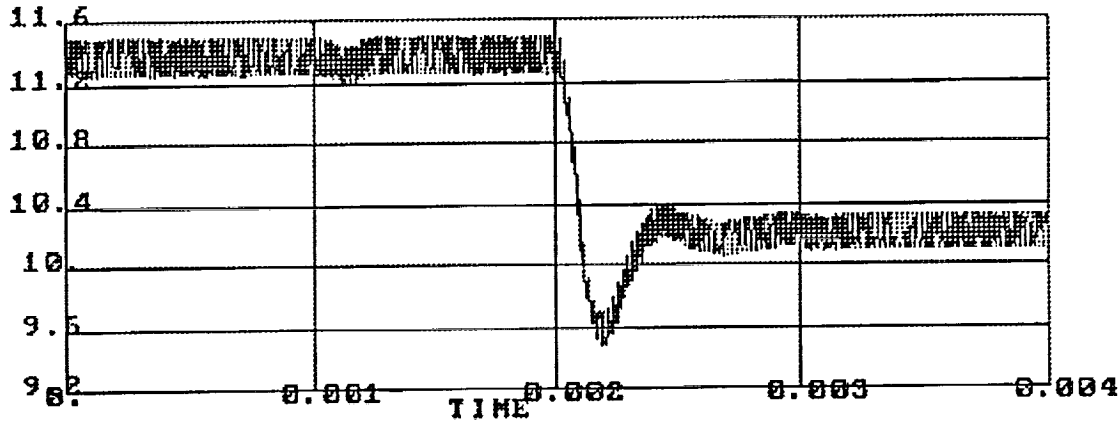
---- CHARGE CURRENT REGULATION MODE ----

SINGLE CHARGER TRANSIENT RESPONSE *

Vbus

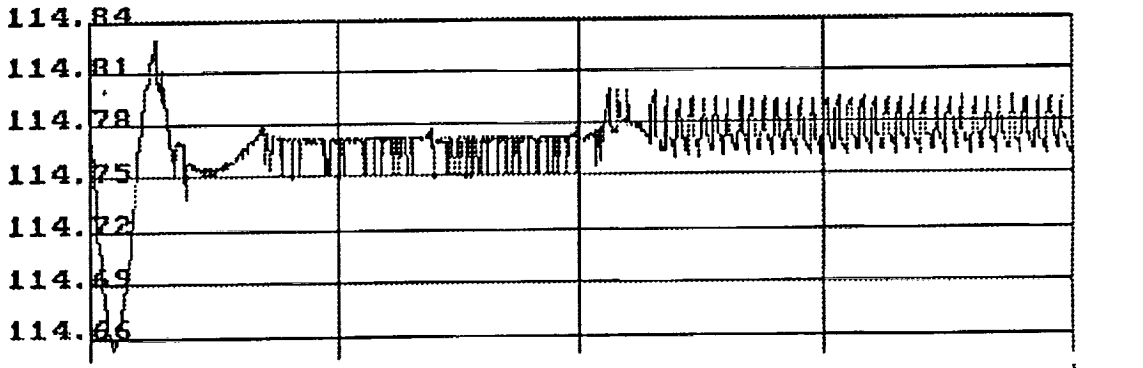


Ichg
FROM BUS



PARALLEL CHARGER TRANSIENT RESPONSE *

Vbus



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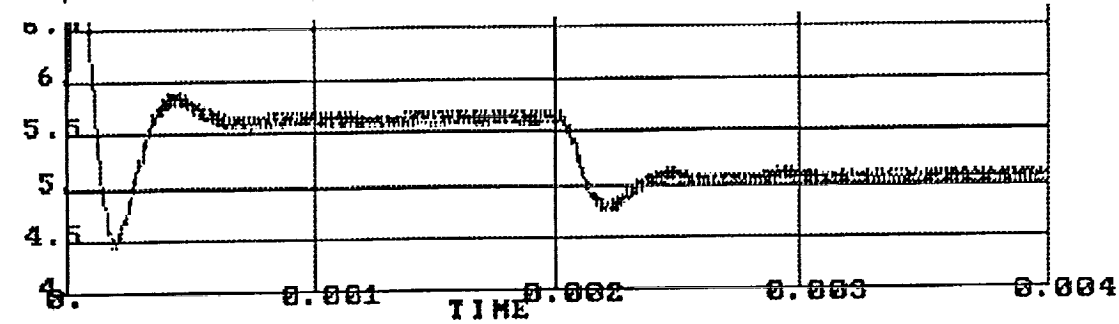
FROM BUS

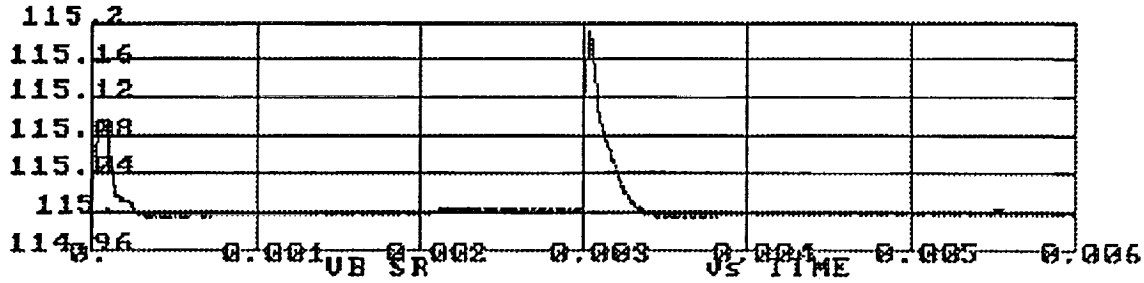


* SAME COMPENSATION FOR EACH CASE

-- BUS VOLTAGE REGULATION MODE --

SINGLE CHARGER TRANSIENT RESPONSE *

Vbus



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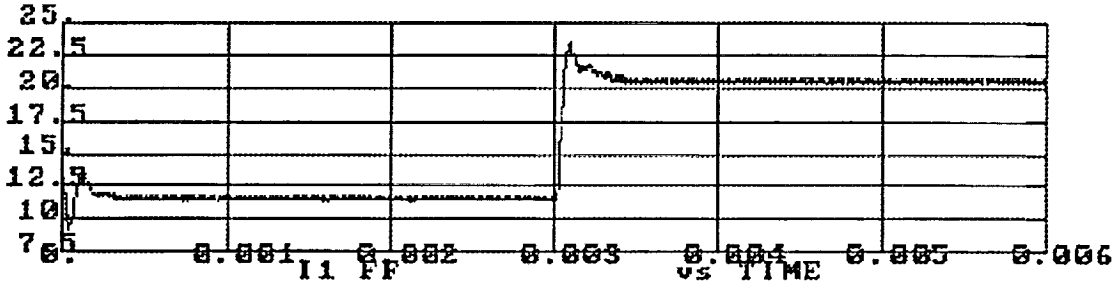
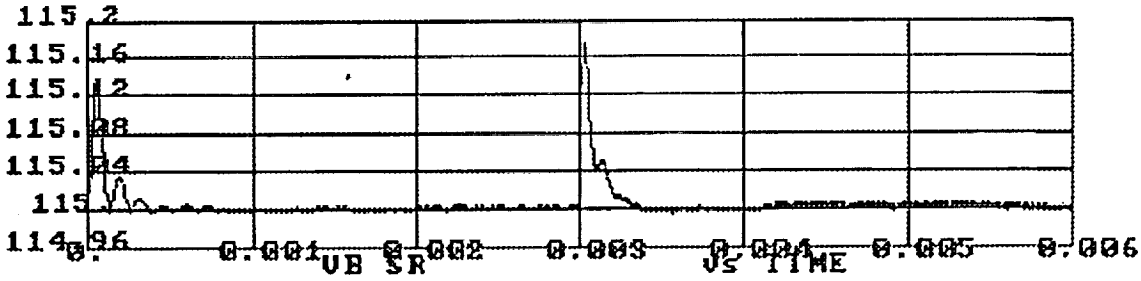
FROM BUS

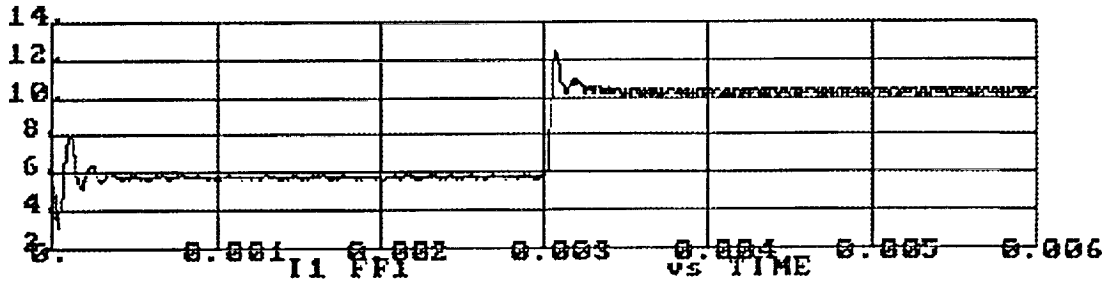


PARALLEL CHARGER TRANSIENT RESPONSE *

Vbus



Ichg
FROM BUS



* BOTH BATTERIES = 64V

SUMMARY OF BATTERY ORU MODELLING

* EASY5 MODELS DEVELOPED FOR BATTERY ORU

* PARALLEL DISCHARGER MODELLING
  - DC CURRENT SHARING
  - RECOMPENSATION FOR PARALLEL MODULES
  - BATTERY VOLTAGE IMBALANCE & LOOP GAIN

* PARALLEL CHARGER MODELLING
  - CHARGE CURRENT REGULATION MODE
  - BUS VOLTAGE REGULATION MODE

REVIEW OF SPACE PLATFORM POWER SYSTEM MODELING

INTRODUCTION

Modeling and simulation :

Large and small signal component models have been developed for the following, using the EASY5 analysis program :

- Solar cells/solar array
- Solar array shunt switching units
- DC-DC converters (buck, boost, flyback, forward)
- Error amplifiers, PWM controllers
- Battery dischargers (boost, tapped-boost) and output filter
- Battery charger (buck) and input filter
- Battery
- Loads
- Mapham inverter
- Spacecraft power system models (for both AC and DC bus)

These models have been used to study

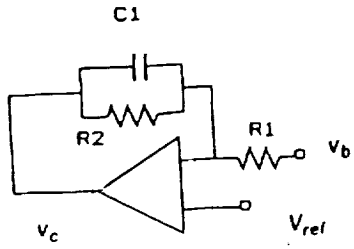
- Transient response to step change of load
- Mode transitions with changes of illumination level
- Paralleling of chargers and dischargers
- Stability study using frequency response plots (small signal models)

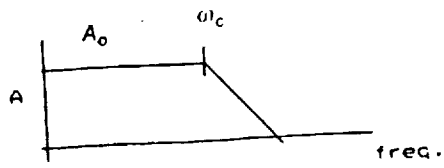
Design and analysis :

- Battery charger design
- Battery discharger topology trade-off study
- Battery discharger design
- Analysis of bus impedance, stability and ripple in the shunt regulation mode
- Analysis of bus impedance in charger and discharger regulated modes

Proposed future work :

- Modeling, analysis, design
- Hardware system testbed



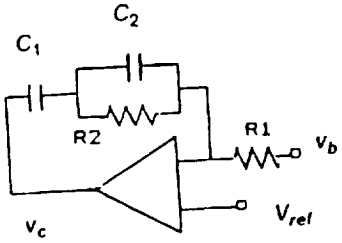


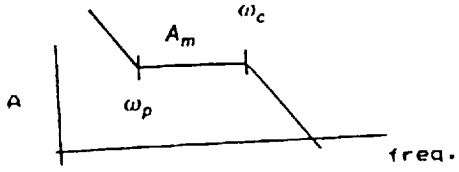
$$A = \frac{v_c}{v_b} = \frac{A_o}{1 + \frac{s}{\omega_c}}$$

$$\omega_c = \frac{1}{C_1 R_2}$$

$$A_o = \frac{R_2}{R_1}$$

Proportional gain compensator (select PG = 1)





$$A = \frac{v_c}{v_b} = \omega_m \frac{(1 + \frac{s}{\omega_p})}{s(1 + \frac{s}{\omega_c})}$$

$$A_m = \frac{R_2}{R_1}(1 + \frac{C_2}{C_1})$$

$$\omega_p = \frac{1}{R_2(C_2 + C_1)} \qquad \omega_c = \frac{1}{C_2 R_2} \qquad \omega_m = \frac{1}{C_1 R_1}$$

Integrator type compensator (select PG = 0)

Fig. 2.1-5 Compensators for [SR] model

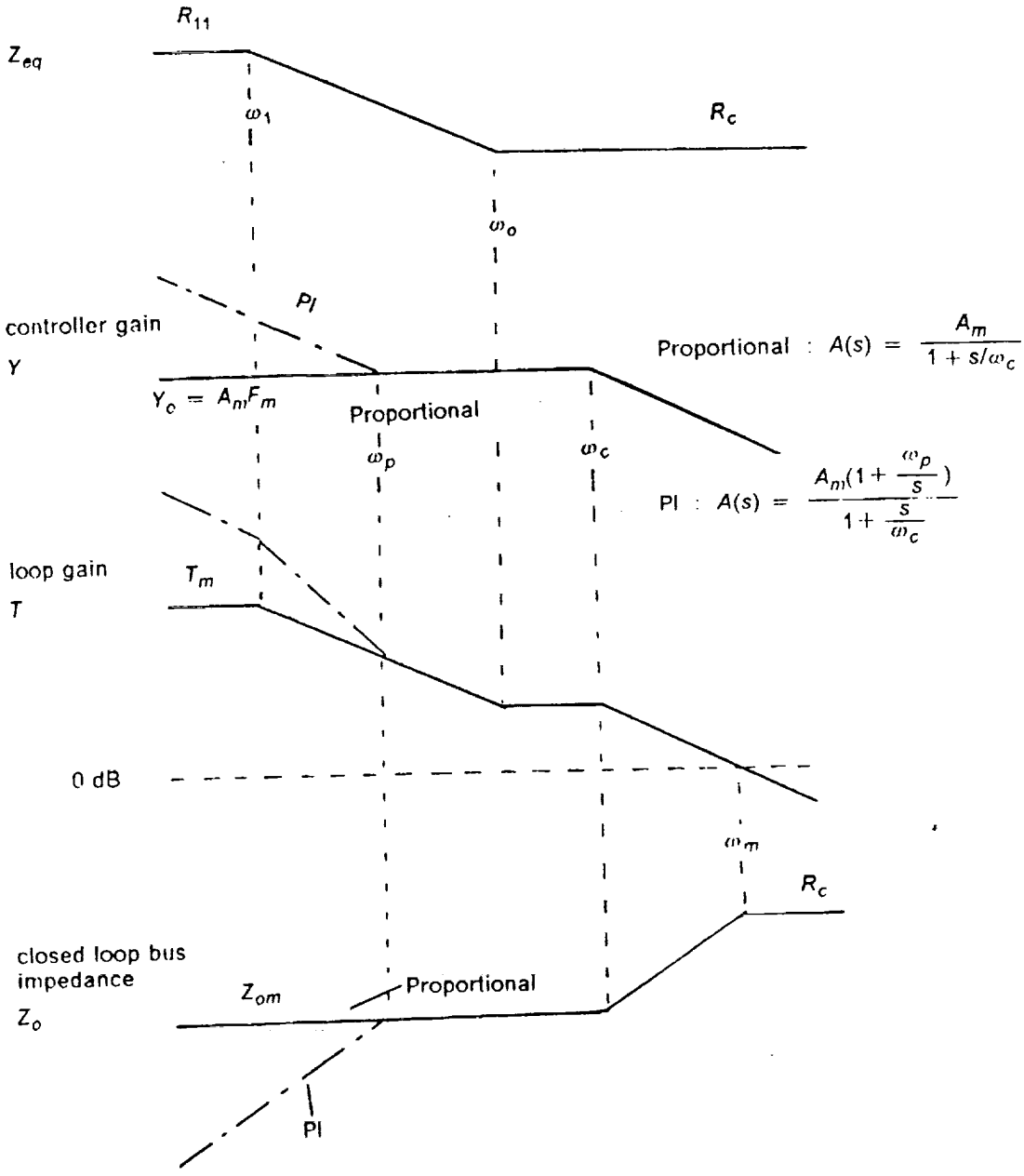


Fig. 4 Loop gain and bus impedance plots

Salient design features for shunt unit and bus capacitor

- For a properly designed system, the peak bus impedance is the ESR of the bus filter capacitor (this determines the overshoot for a step load change)
- A proportional controller has fast transient response but has a load dependant bus voltage error (a voltage "band" requirement)
- An integrator type compensator can decrease the voltage band requirement, but the zero required to reduce phase lag results in a low frequency pole in the bus impedance. This may make the transient response slower.
- The bus ripple depends on the following factors :

  Switching frequency
  Bus capacitor ESR
  Bus capacitance
  Current per parallel switch

$$V_{pp} = I_p R_c + D(1 - D)\frac{T_s I_p}{C}$$

where

D = duty ratio modulation
R_c = bus capacitor ESR
I_p = current from one set of NPS strings
T_s = switching period
C = bus capacitor

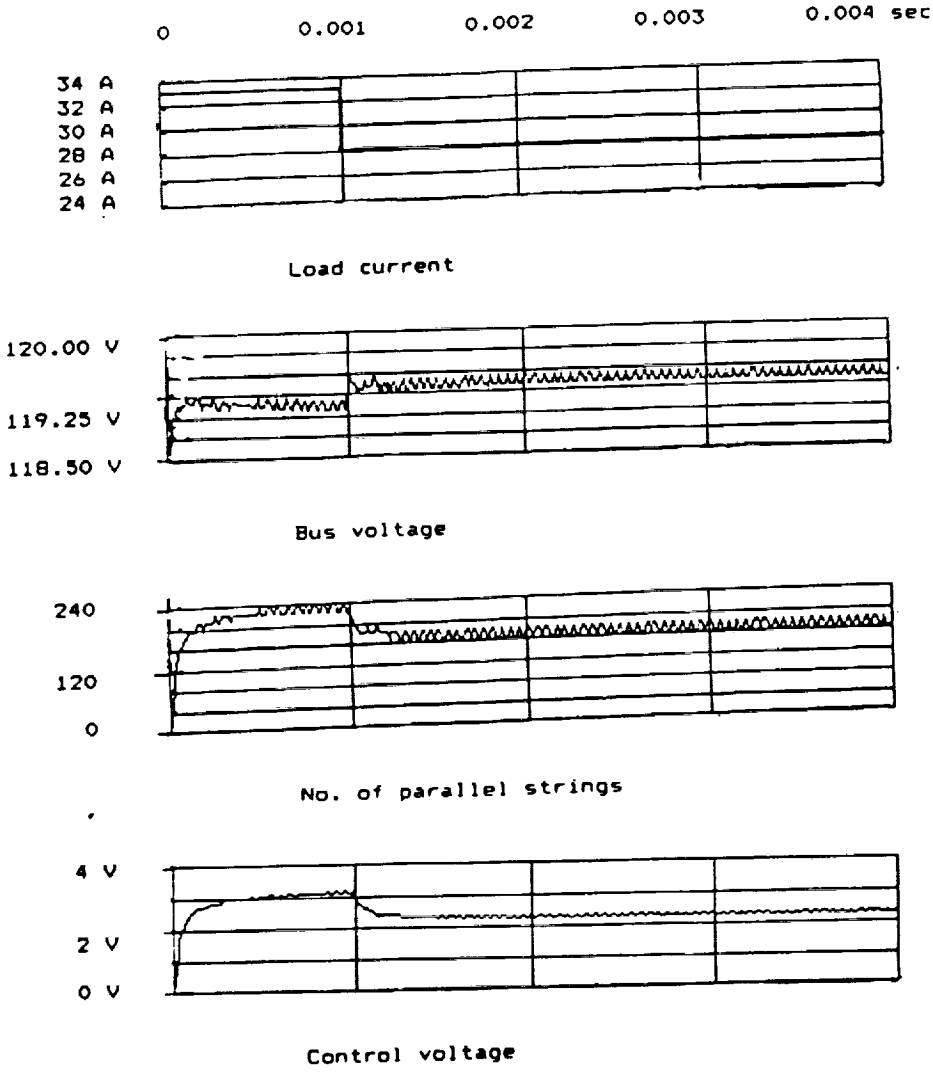


Fig. 5a Simulation for proportional compensator

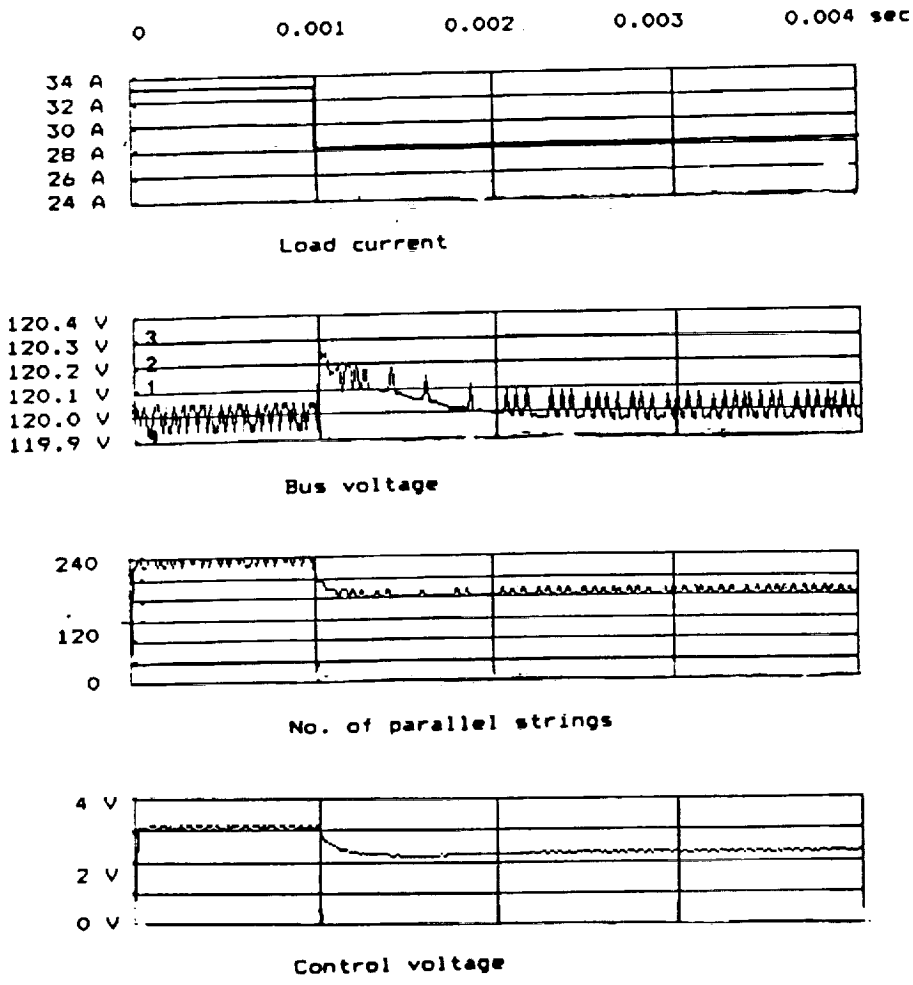
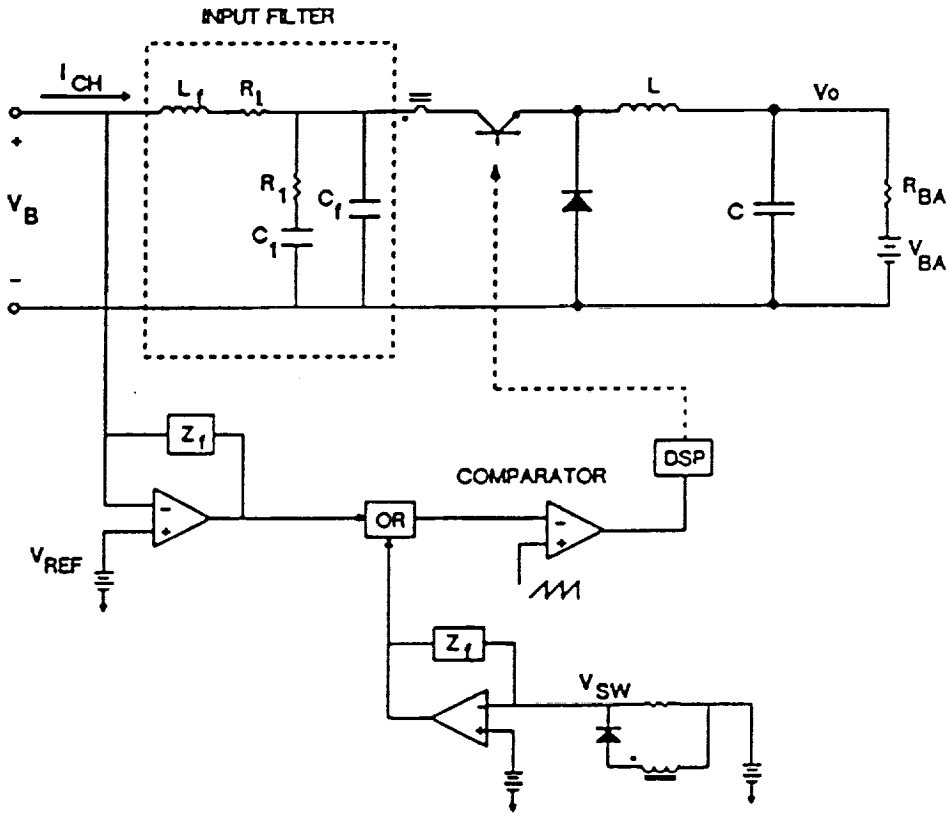


Fig. 5b Simulation for PI compensator

Battery charger circuit (Buck) with input filter



- An input filter is added to smooth the pulsating current drawn by the buck converter
- The circuit can be made to function in two modes.
- In the bus voltage regulation mode, the current is less than the maximum battery charge current and the charger regulates the bus
- When the array has sufficient illumination to provide the maximum charge current, the charger current is limited to this maximum value. The bus voltage rises and the array shunt switching unit regulates the bus

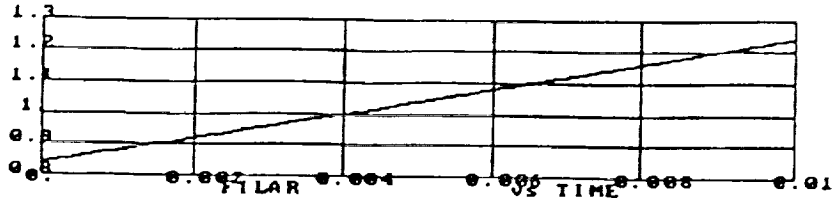
Salient design features for the charger

- Input filter corner frequency is one decade below the switching frequency to lower the ripple to 1% of output side ripple
- An integrator type compensator (2 poles, 2 zeroes) is used.

$$H_v = \frac{w_m}{s} \frac{(1 + s/w_{z1})(1 + s/w_{z2})}{(1 + s/w_p)}$$

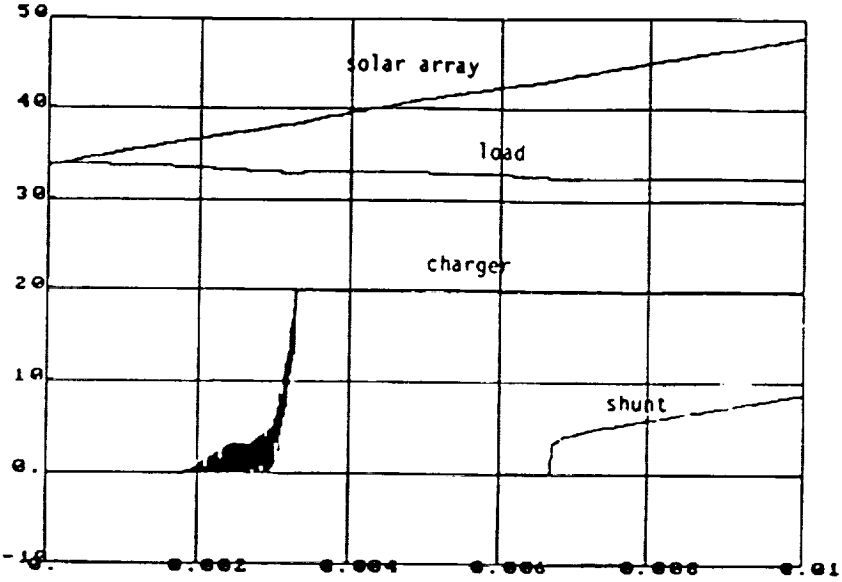
- The low frequency compensator zero is the dominant pole for bus impedance and determines transient response. It is kept as large as possible. However, placing it beyond the low frequency pole of the power stage can cause conditional instability
- The peak overshoot is determined by the ESR of the bus filter capacitor
- The second zero approximately determines the settling speed of the system
- These transient response features have been verified from the step load simulation

Simulation for transient response of charger



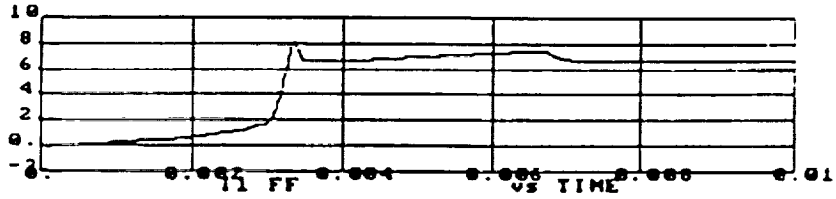
illumination level

[A]



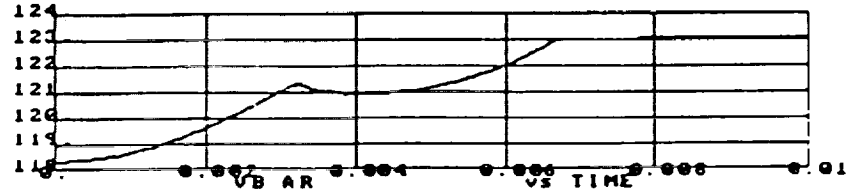
currents

[A]



input filter current

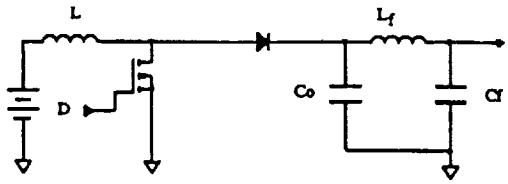
[V]



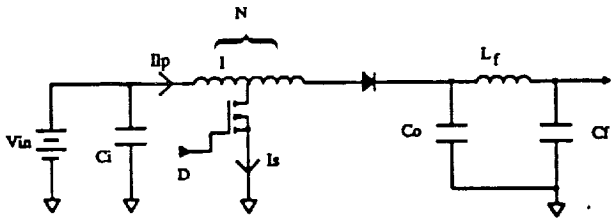
bus voltage

Discharger topology comparison

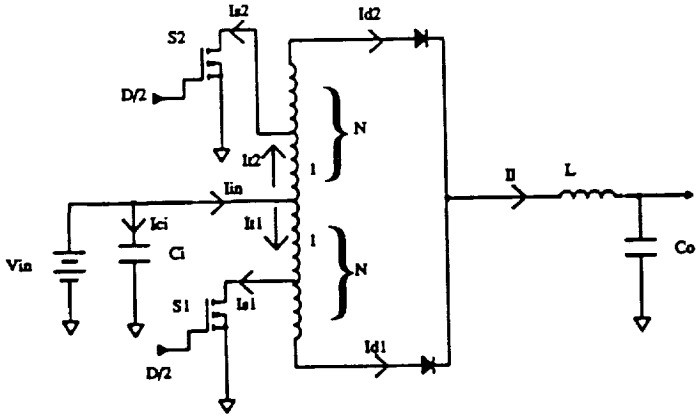
Topologies considered for discharger



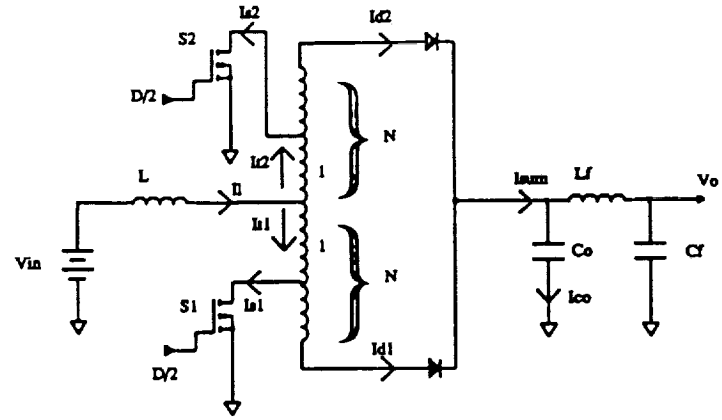
Boost



Tapped boost



Voltage fed push pull with tapped auto transformer (VFPPTAT)



Current fed push pull with tapped auto transformer (CFPPTAT)

	Boost	T-Boost	VFPPTAT	CFPPTAT
Inductor Tap Ratio	1	2	1	1
X-former Tap Ratio	n/a	n/a	3	3
Conversion Frequency	25kHz	25kHz	50kHz	50kHz
Inductance (15% Ripple)	$59\mu H$	$140\mu H$+	$65\mu H$	$5.5\mu H$
Peak Inductor Current	66 A	42.5 A	19.2 A	66 A
Inductor Energy ($\frac{1}{2} LI_p^2$)	.13 W-S	.13 W-S	.010 W-S	.012 W-S
Max. Duty Cycle	73%	56%	41% *	47% *
Peak Q current	66 A	85 A	57.6 A	49.5 A
RMS Q current	49 A	55 A	37 A	30 A
Peak Q Voltage	120 V	82.5 V	90 V	120 V
Peak Diode Current	66 A	42.5 A	19.2 A	33 A
Peak Diode Voltage	120 V	165 V	210 V	180 V
Input Cap RMS Current	0	18.4 A	19.7 A	0
Output Cap RMS Current	26 A	19 A	0	10.3 A
Pri. Leakage L delta I	0	42.5 A	38.4 A	16.5 A

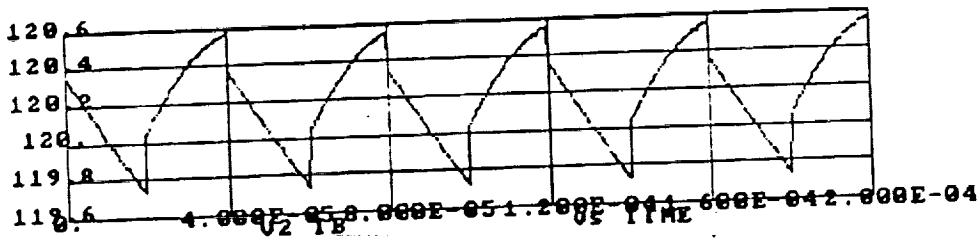
+ This is the whole inductance. The primary inductance is $35\mu H$.

* This is the duty cycle per switch. The duty cycle seen by the inductor is twice.

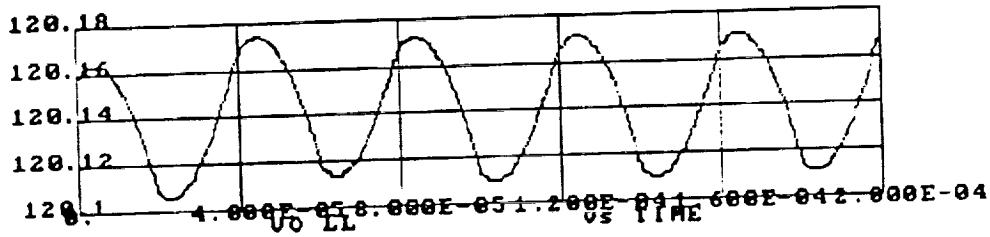
Results of comparison : choice of discharger topology

- the boost converter is simple, has only one switch, one diode and no transformer, and continuous input current
- it however has disadvantages (specially if the step up ratio is high). These are the RHP zero in the control/output voltage transfer function, high output current stress in the output capacitor, and difficulty in control loop design at high transformation ratios (i.e., high duty ratio)
- the tapped boost allows a lower duty ratio for a given voltage step up, the RHP zero is at a higher frequency and more manageable
- the VFPPTAT is buck derived so it provides continuous output current, well behaved control characteristics, and a lower current stress than the boost or tapped boost
- the VFPPTAT however needs two diodes and two switches, and the circuit is sensitive to transformer saturation
- CFPPTAT has many desirable features such as lowest switch current stress.
- the CFPPTAT however needs two switches, and it is expected that that it may not compare favorably with 2 tapped boost converters operating in parallel and out of phase by 180 degrees
- the tapped boost topology was therefore selected for modeling as discharger

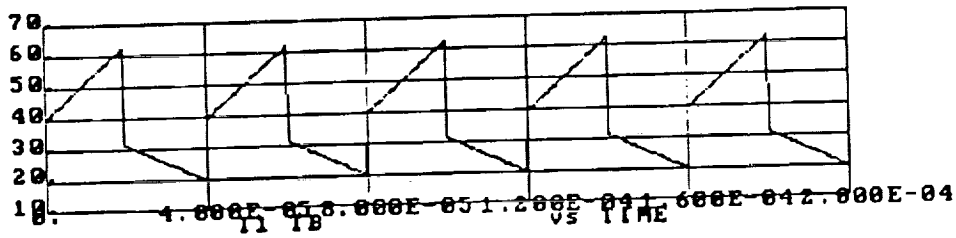
Simulation waveforms for tapped boost discharger model



a) First Stage Capacitor Bank Voltage

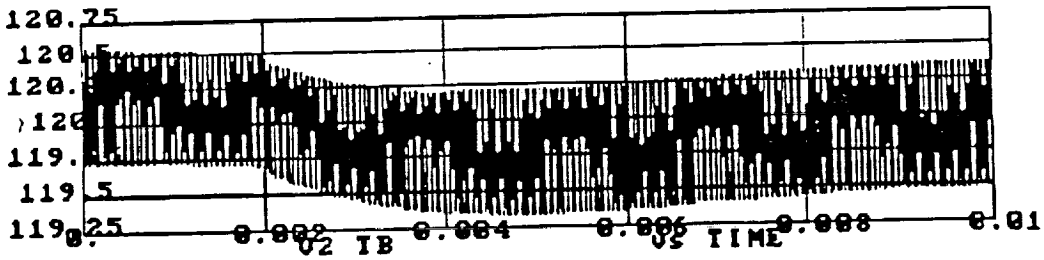


b) Bus Voltage

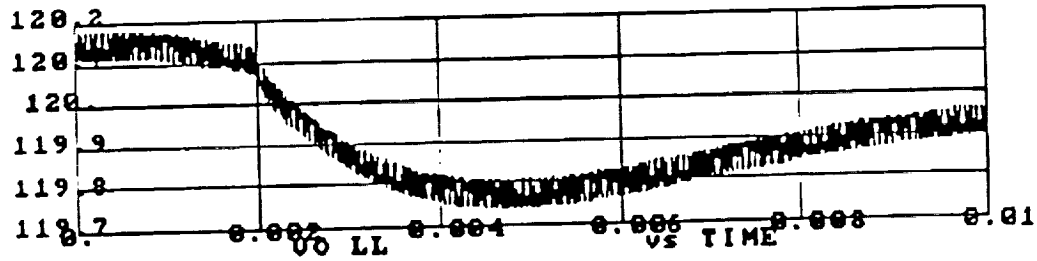


c) Input Current

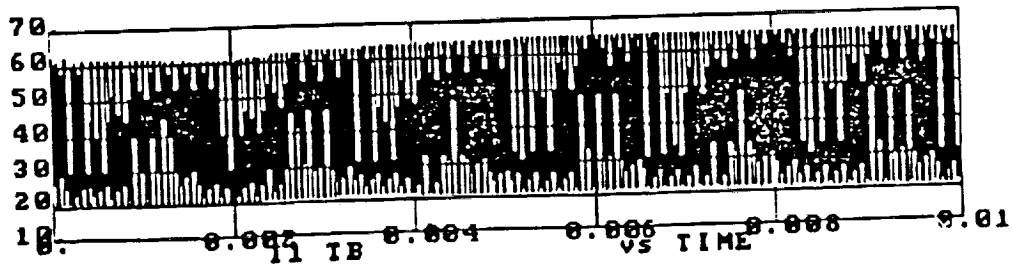
Transient response of discharger to a 1 A step load current change



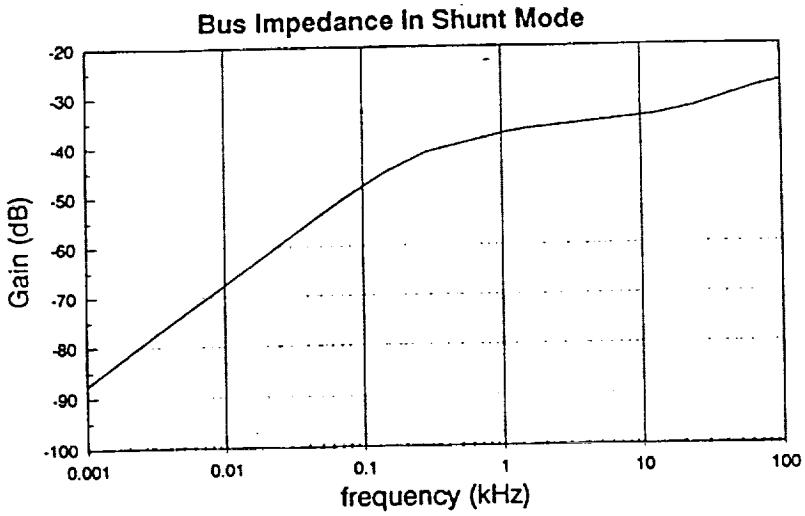
a) First Stage Capacitor Bank Voltage

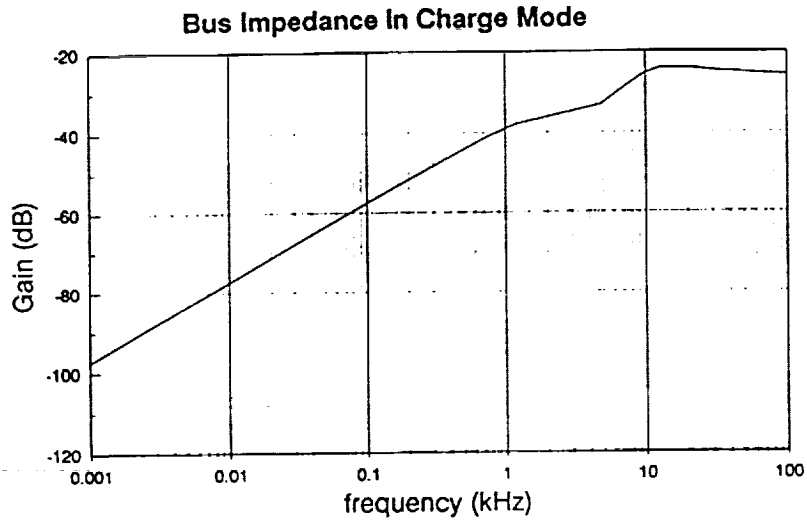


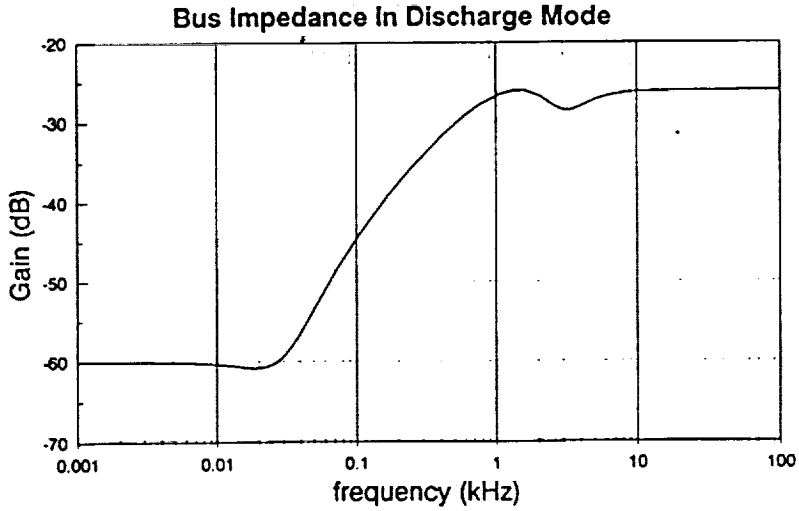
b) Bus Voltage



c) Input Current







Comparison of bus impedances in different modes

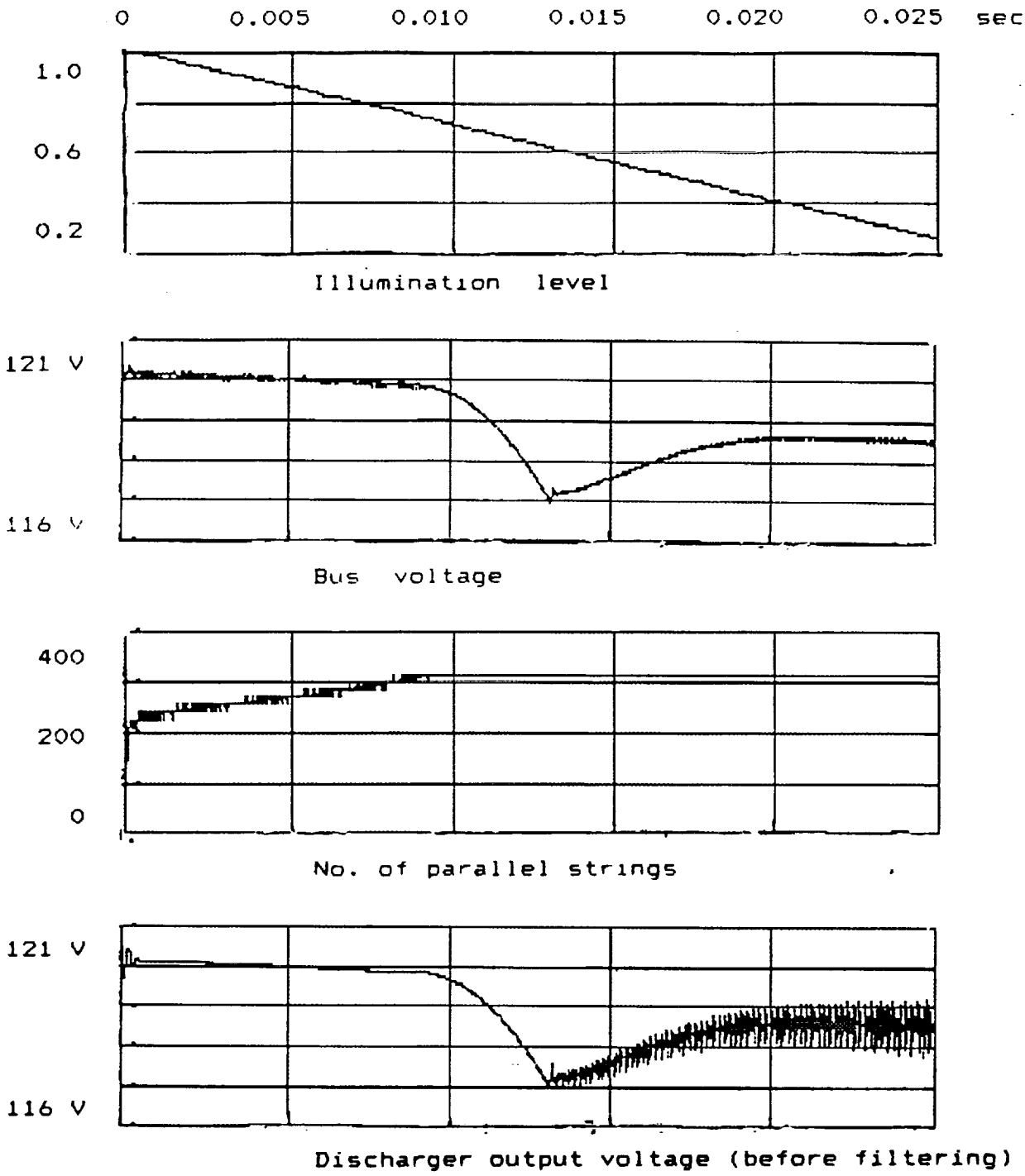


Fig. 4.1-5 Sunlight to eclipse transition

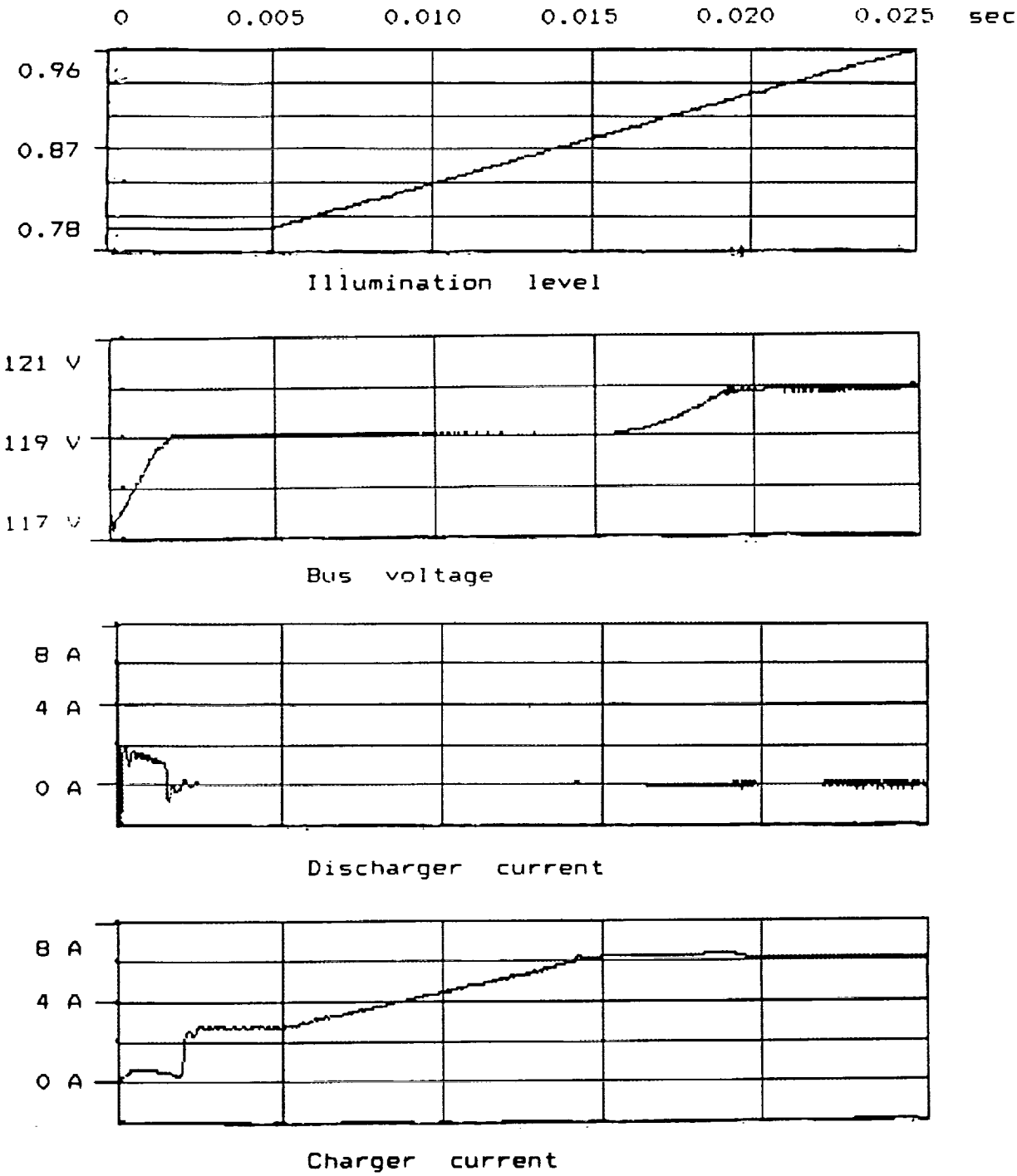


Fig. 4.1-6 Eclipse to sunlight transition

Proposed future work : Hardware system testbed

Objectives :

- To enable verification and improvement of existing EASY5 computer models
- To provide experimental confirmation of analytical design procedures

Proposed hardware work :

The following are to be designed, built and tested. The designs will be optimized by VPEC's power converter optimization (CADO) software.

- battery charger
- battery discharger (boost, and an alternate topology)
- mode controller

These are to be tested with :

- a simple solar array simulator
- battery simulator
- load bank

These will allow verification of simulations for many of the system modes. Future work could incorporate a solar array shunt switching unit for verification of the shunt mode.

References :

[1] J.Lee, S.Kim, B.H. Cho, and F.C. Lee,, "Computer-aided modeling and analysis of power processing systems (CAMAPPS) - Phase II", Final report prepared for NASA/Goddard, VPI&SU, 1987

[2] B.H Cho, J.R. Lee, "Design, analysis and simulation of the main bus dynamics of spacecraft power systems," IECEC Conference proceedings, 1988

[3] J. Lee, "Analysis and simulation of dynamics of spacecraft power systems," (Dissertation), VPI&SU, 1989

[4] A. Patil, S. Kim, D. Sable, B. Cho, F.C. Lee, "Modeling of space platform power distribution," Final report prepared for Fairchild Space Company, VPI&SU, 1989

[5] F.S. Tsai and F.C. Lee, "Computer modeling and simulation of a 20 kHz AC distribution system for the space station," Report prepared for NASA Lewis Research Centre, VPI&SU, 1987

ANALYSIS AND DESIGN OF A HIGH POWER, DIGITALLY CONTROLLED SPACECRAFT POWER SYSTEM

QUARTERLY PROGRESS REVIEW

for

NASA GODDARD SPACE FLIGHT CENTER
GREENBELT, MD

MAY 1, 1990

PREPARED BY

D. SABLE, A. PATIL, T. SIZEMORE, S. DEUTY, B.H. CHO AND F.C. LEE

VIRGINIA POWER ELECTRONICS CENTER
VIRGINIA POLYTECHNIC INSTITUTE
AND STATE UNIVERSITY
BLACKSBURG, VA 24061

PRESENTATION OUTLINES

1. **Space Platform Power System Modeling**

   1.1 Battery discharger analysis & design — **DS**

   1.2 EASY5 modeling for battery ORU — **TS/AP**

   Battery charger/discharger mode control

2. **Space Platform Power System Testbed**

   2.1 Battery discharger design

   2.1.1 Four-module boost — **DS**

   2.1.2 Voltage-fed push-pull autotransformer — **SD**

   2.2 Battery charger design — **TS**

3. **Discussion**

1. SPACE PLATFORM

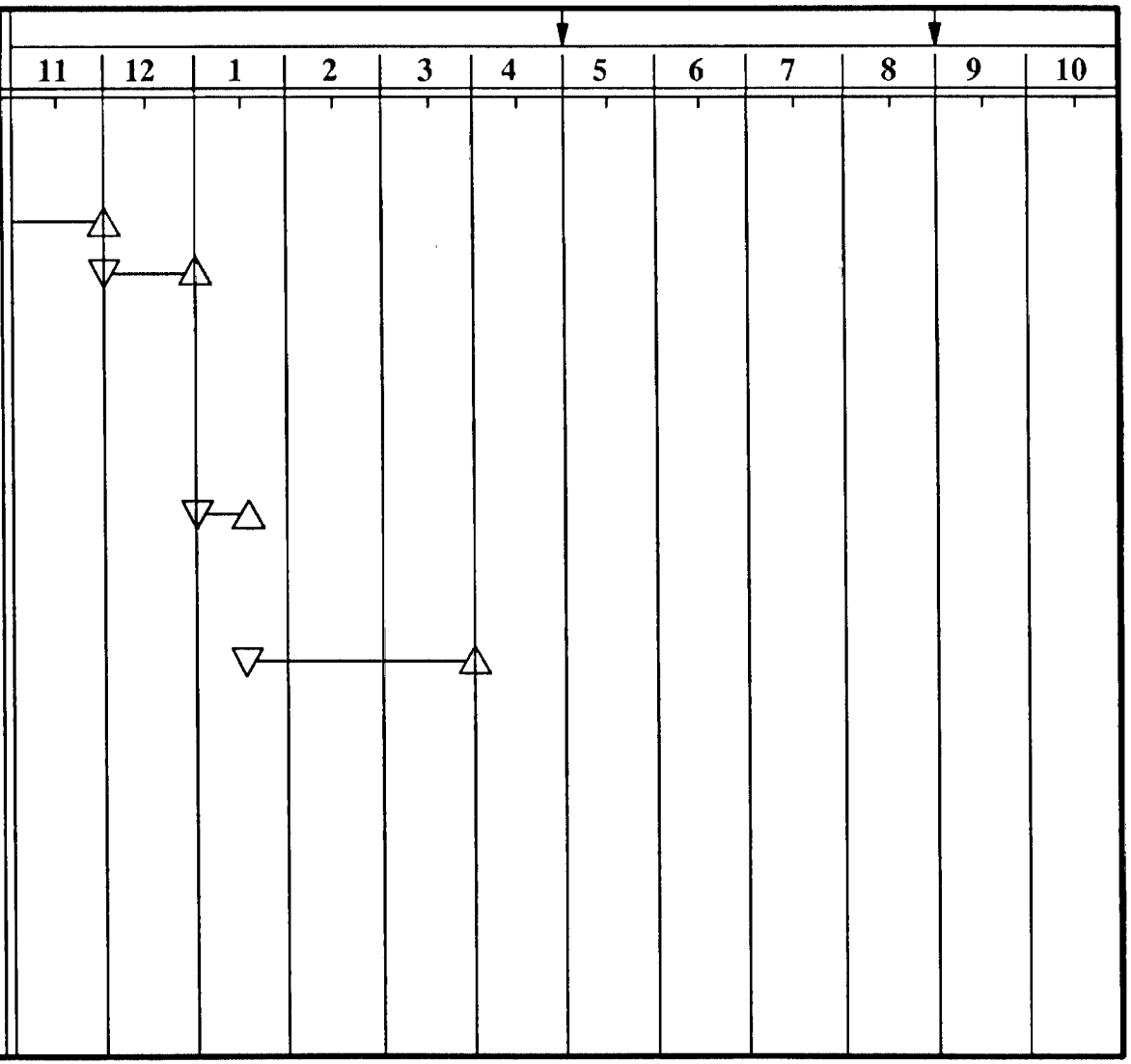
POWER SYSTEM MODELING

△	PLAN
⧋	CHANGE
▲	COMPLETE

NASA/GSFC Space Platform Modeling
Project Schedule
Phase II (Ending 8/31/90)

4/26

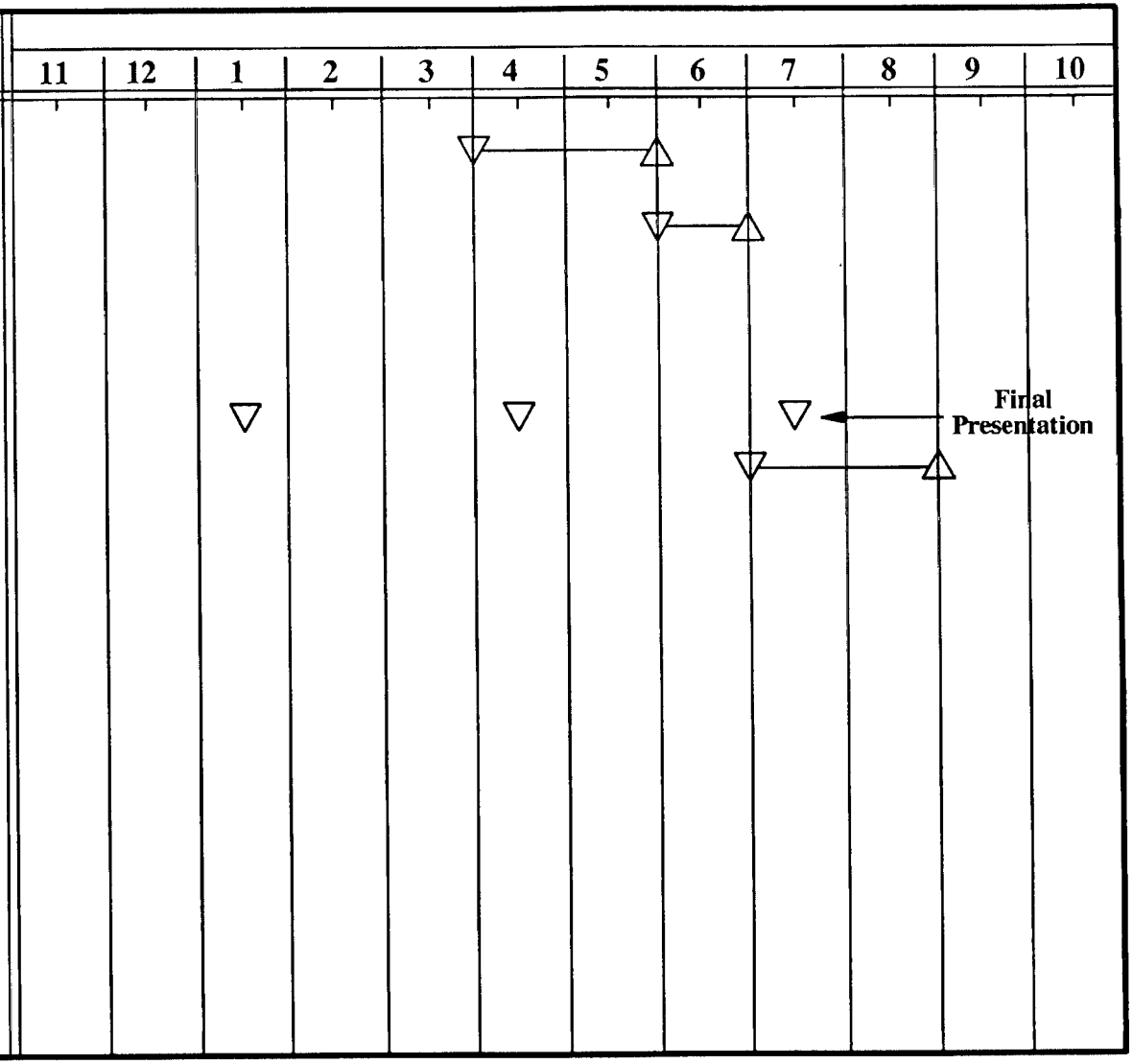
NO	TASK DESCRIPTION
1.	ORU Level Modeling and Control
	• Parallel battery ORU subsystem modeling
	• ORU control and analysis
	- Issues related to paralleling
2.	DC Bus Regulation and Mode Control
	• PV subsystem w/the parallel ORU modeling
	• Design
	• Analysis and Simulation of PV Subsystem
	- Controller Design
	- Band Tolerance and bus regulation
	- Charger, SASU



△	PLAN
⧋	CHANGE
▲	COMPLETE

NASA/GSFC Space Platform Modeling
Project Schedule

NO	TASK DESCRIPTION
3.	Example Design of Integrated System
4.	System Level Simulation
	- Verifications
5.	Report
	• Quality
	• Final Report



BATTERY DISCHARGER ANALYSIS

PROGRESS SINCE LAST MEETING

1) TRADEOFF STUDY HAS BEEN FURTHER REFINED

USE OF POLYPROPYLENE INSTEAD OF POLYCARBONATE CAPS

INDUCTOR CORE LOSS DATA HAS BEEN UPDATED

TWO DIODES IN SERIES EMPLOYED FOR REDUNDENCY

2) MULTI-MODULE BOOST CONVERTER CONTROL LOOP HAS BEEN REFINED

DAMPING PROVIDED FOR SECONDARY OUTPUT FILTER

HIGHER GAIN MARGIN PROVIDED

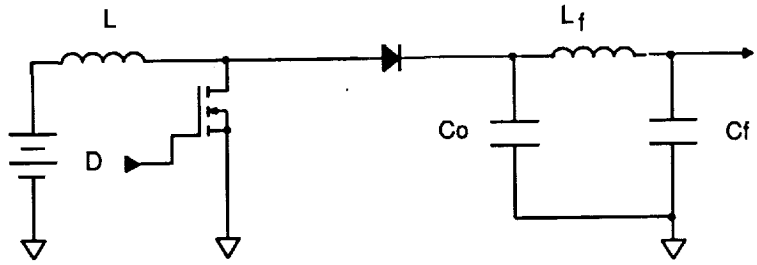
3) DESIGNS HAVE BEEN SELECTED FOR HARDWARE BUILD

45 KHZ, 97% EFFICIENT MULTI-MODULE BOOST CONVERTER

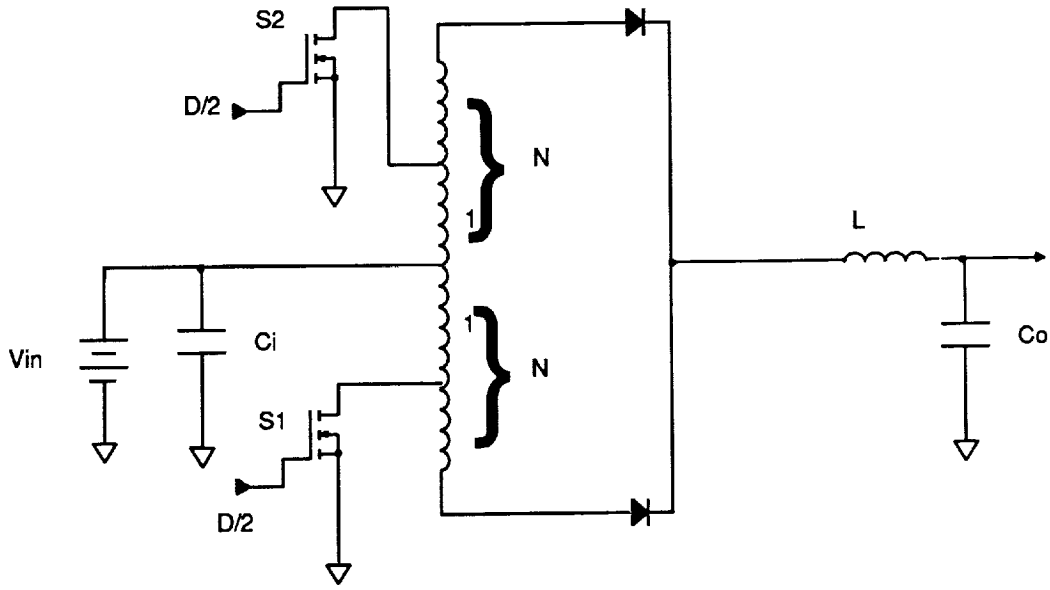
40 KHZ, 96% EFFICIENT VOLTAGE-FED AUTOTRANSFORMER CONVERTER

BATTERY DISCHARGER TRADEOFF STUDY

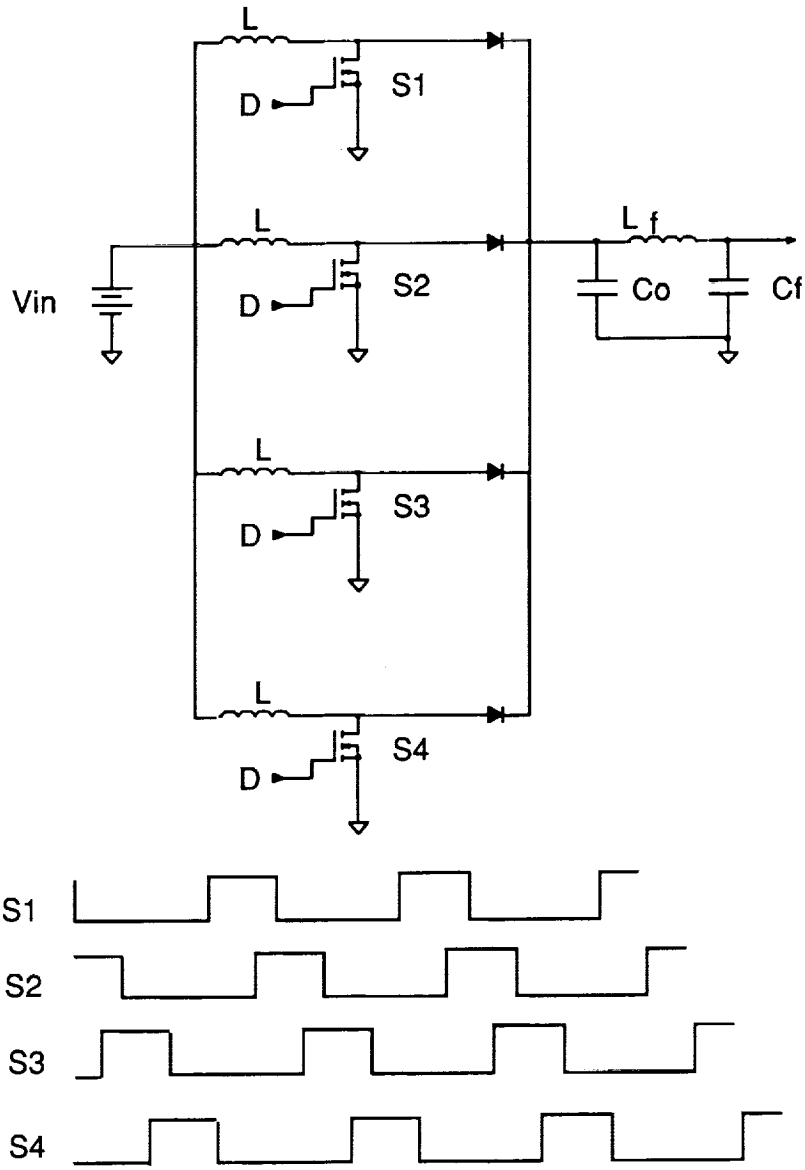
BOOST CONVERTER



VOLTAGE-FED, PUSH-PULL WITH TAPPED AUTOTRANSFORMER (VFPPAT) CONVERTER

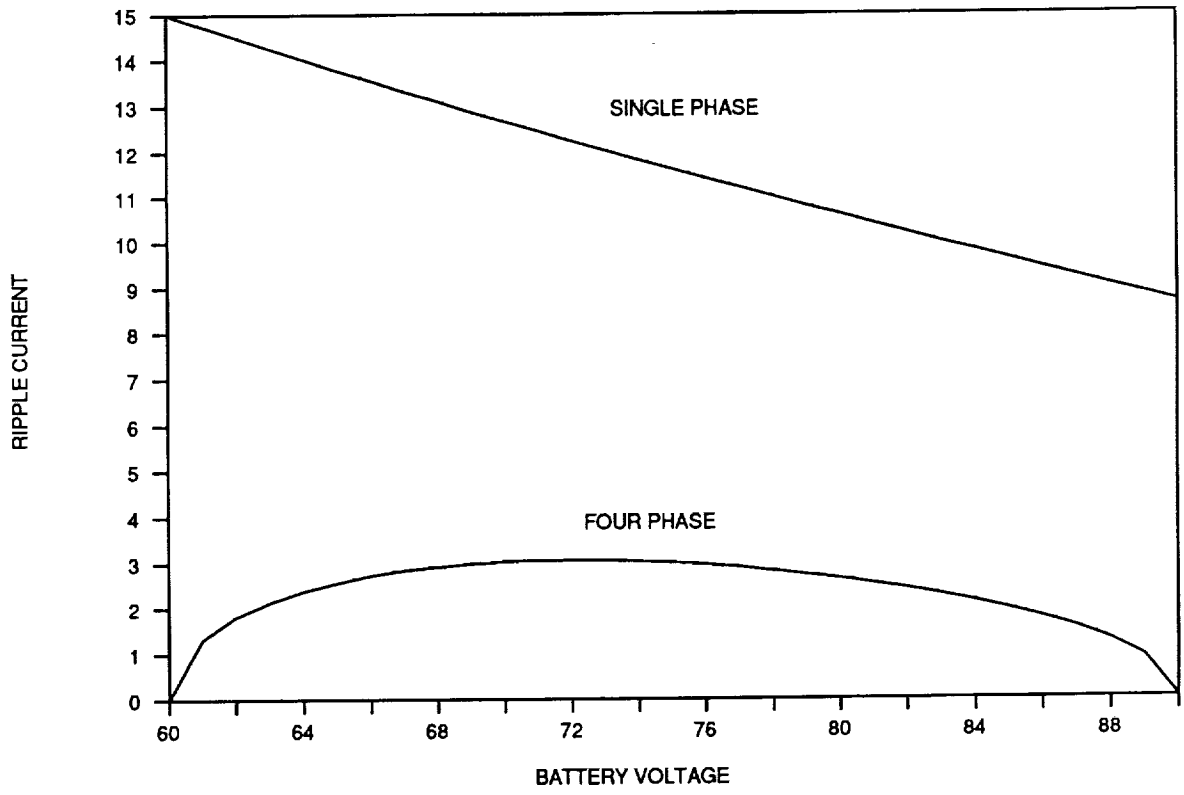


MULTI-MODULE/MULTI-PHASE CONCEPT

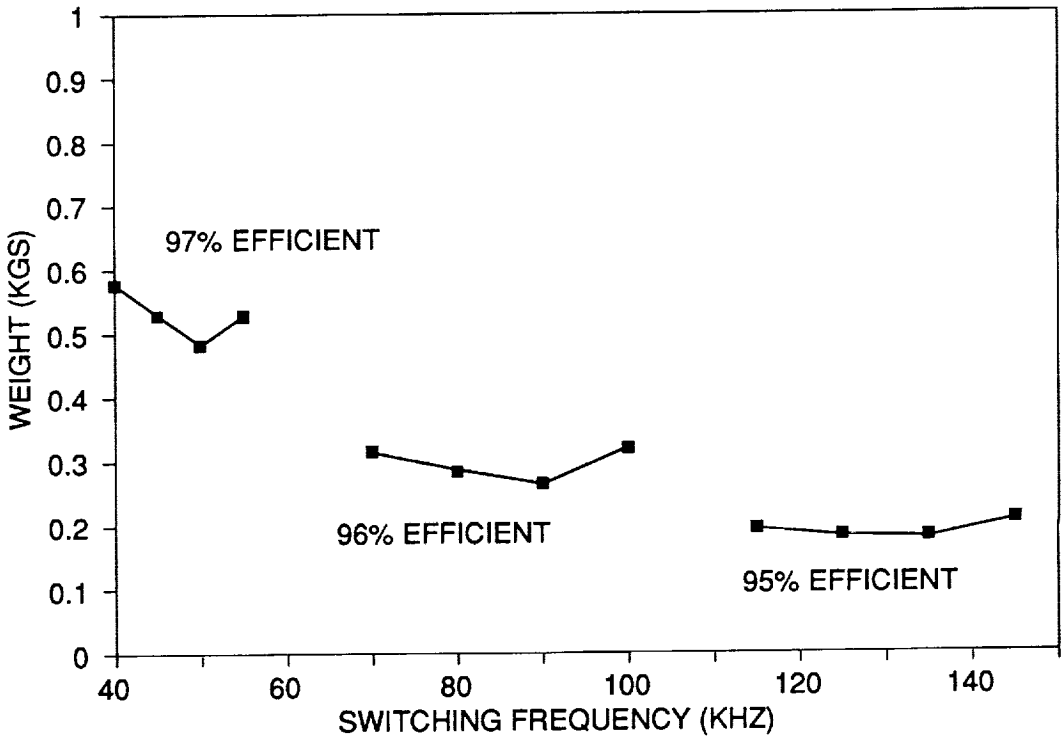


DRAMATIC REDUCTION OF OUTPUT CAP. STRESS
BENEFICIAL FOR THE BOOST CONVERTER
MUCH FASTER TRANSIENT RESPONSE POSSIBLE
CAN BE MORE RELIABLE
- CLOSED-LOOP CURRENT SHARING
- N+1 REDUNDENCY

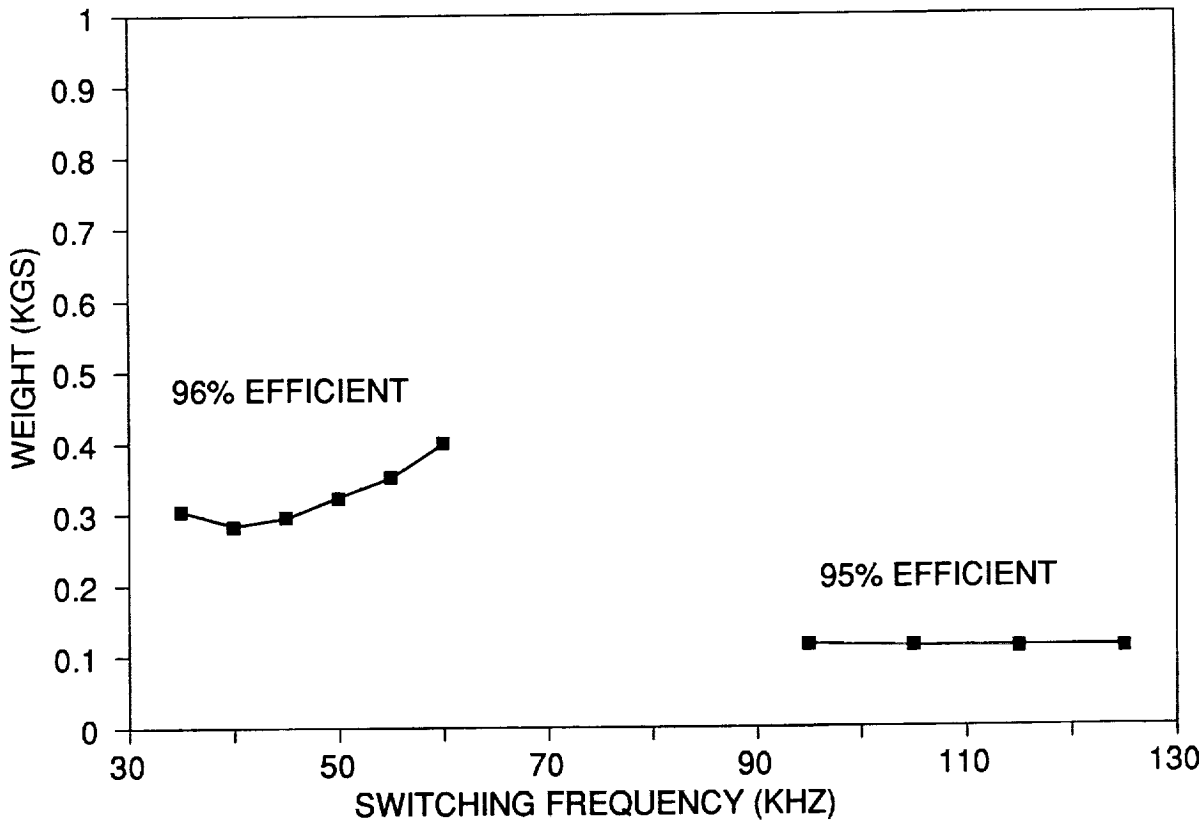
OUTPUT CAPACITOR RIPPLE CURRENT



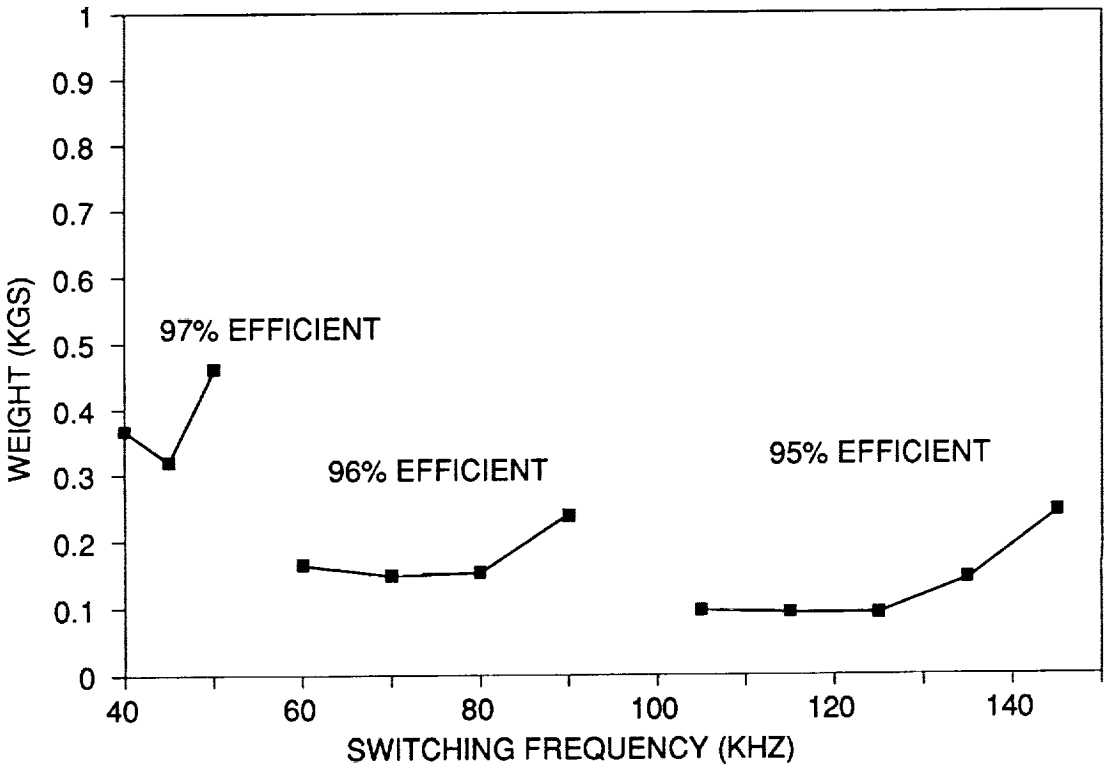
SINGLE-MODULE BOOST DESIGNS



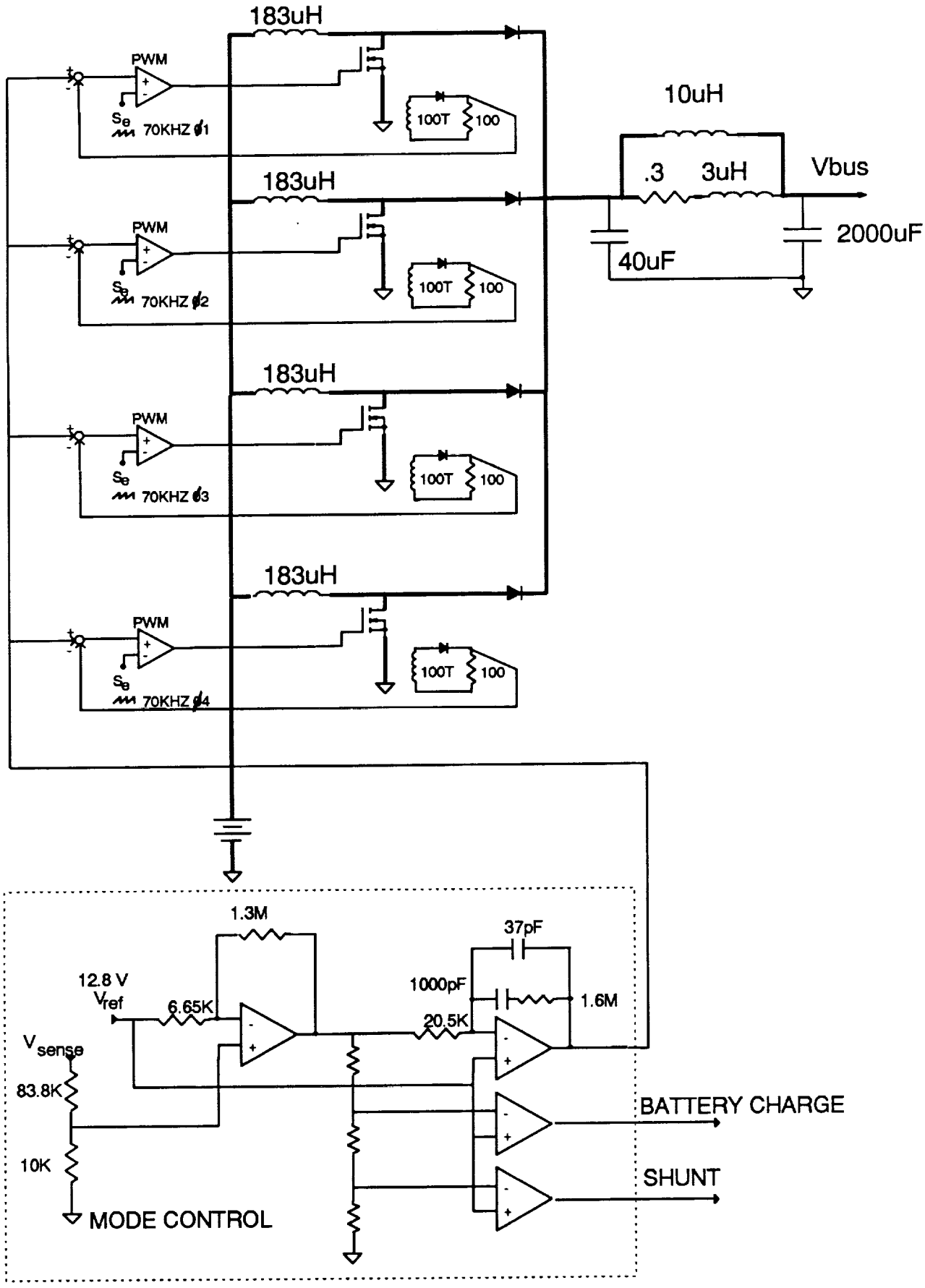
VOLTAGE-FED AUTOTRANSFORMER DESIGNS

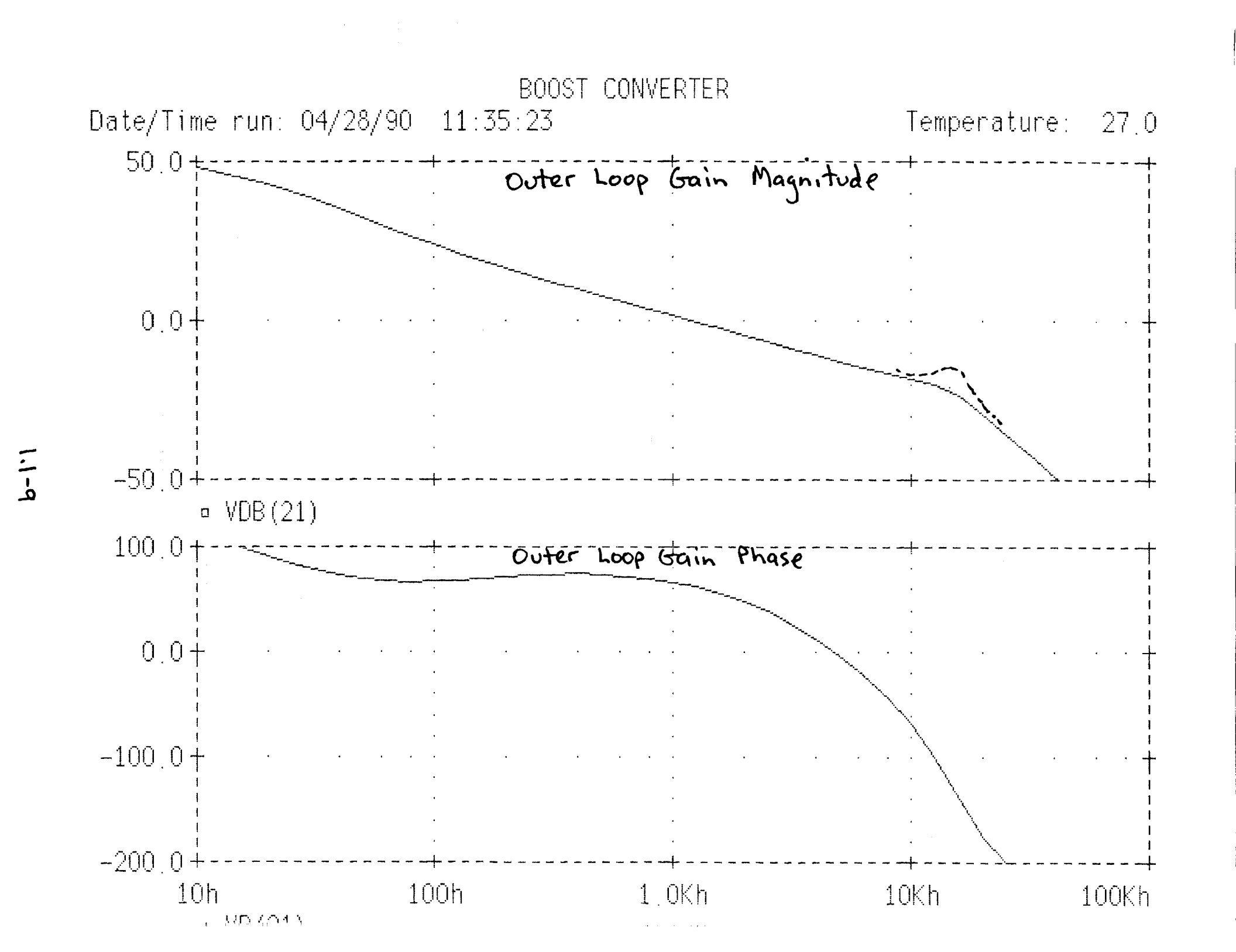


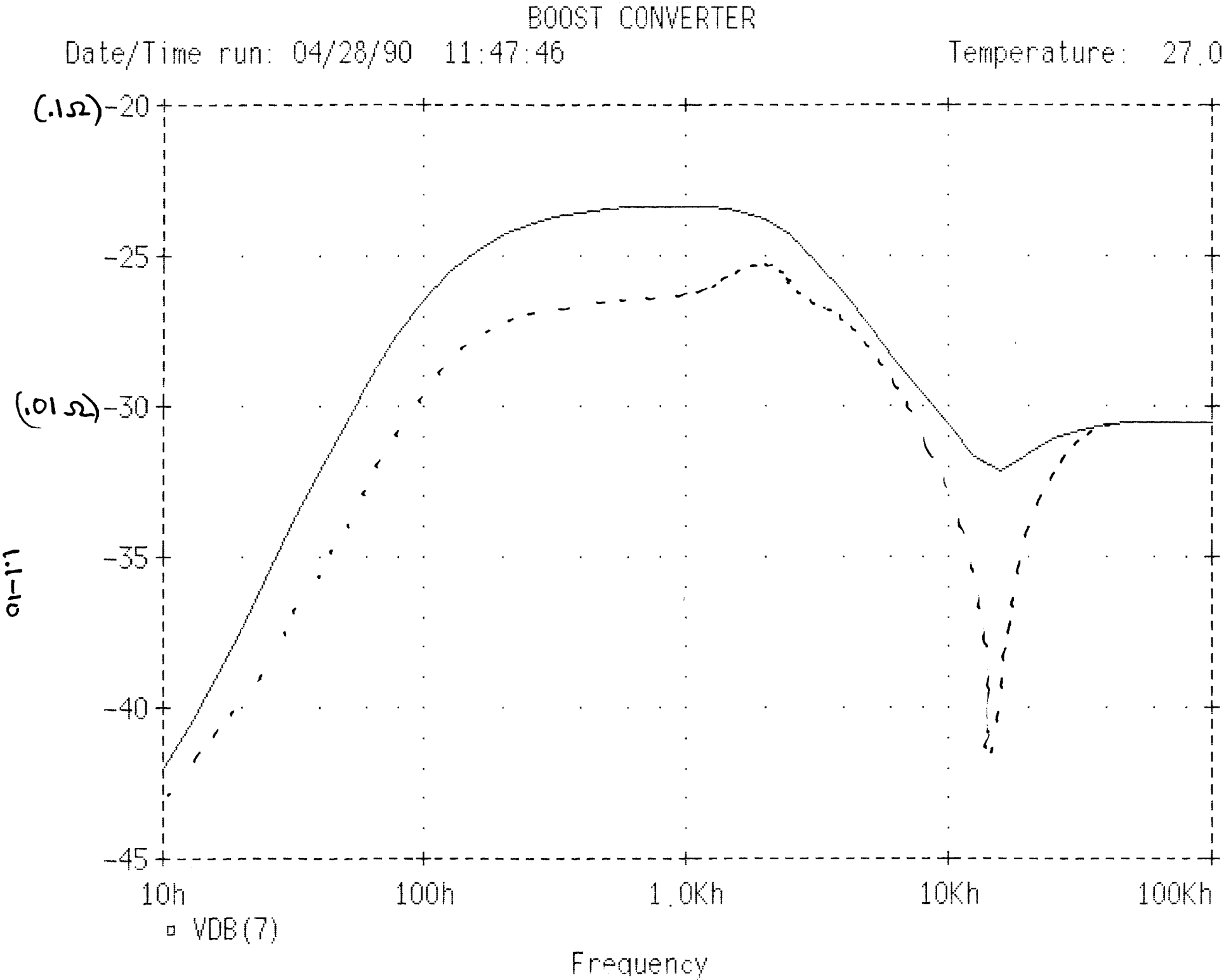
FOUR MODULE BOOST DESIGNS

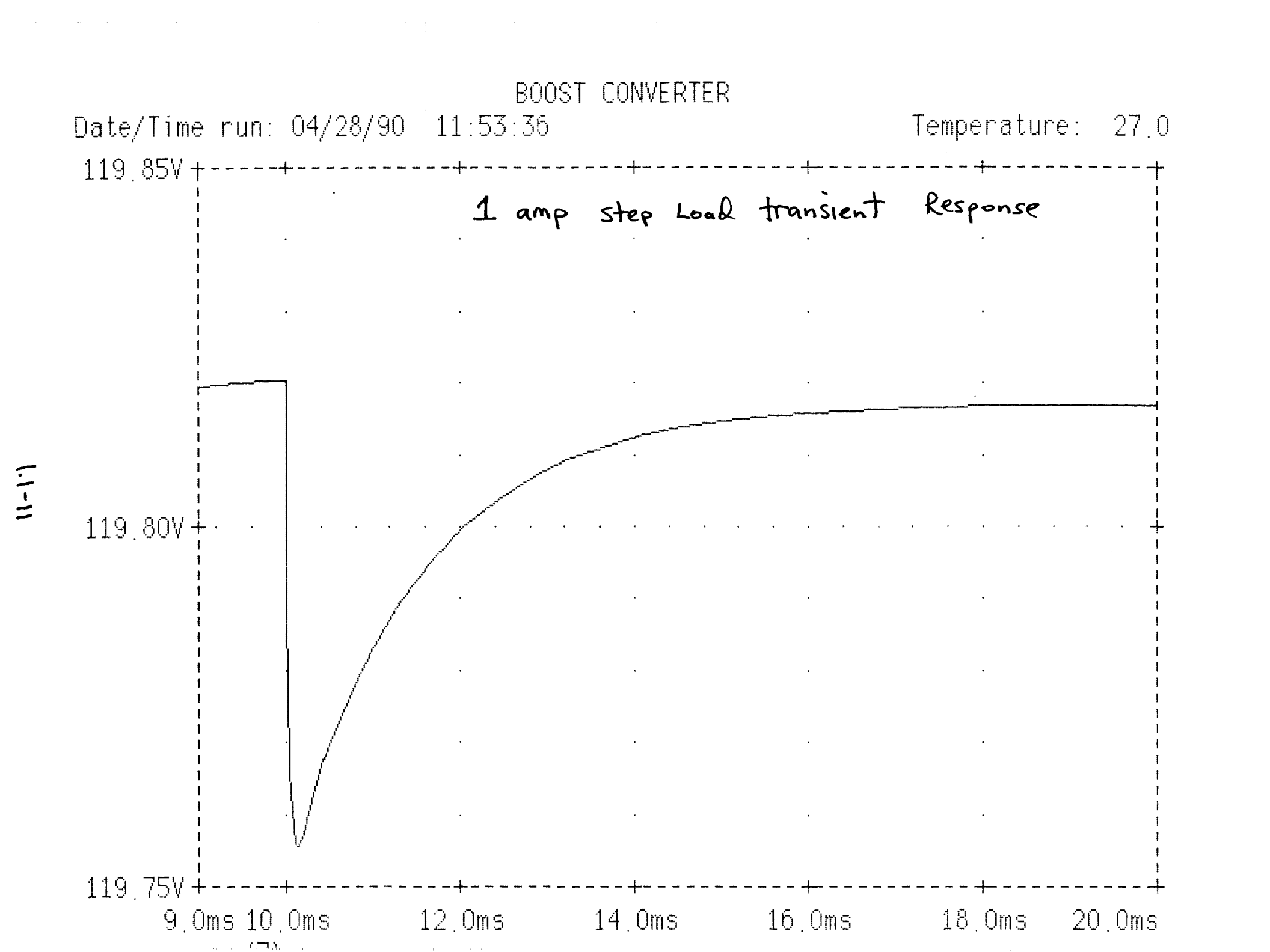


FOUR MODULE BOOST CONTROL CIRCUIT




BOOST CONVERTER
Date/Time run: 04/28/90 11:35:23
Temperature: 27.0
Outer Loop Gain Magnitude
50.0
0.0
-50.0
VDB(21)
Outer Loop Gain Phase
100.0
0.0
-100.0
-200.0
10h
100h
1.0Kh
10Kh
100Kh


BOOST CONVERTER
Date/Time run: 04/28/90 11:47:46
Temperature: 27.0
(.1Ω)
(.01Ω)
-20
-25
-30
-35
-40
-45
dB
10h
100h
1.0Kh
10Kh
100Kh
VDB(7)
Frequency


BOOST CONVERTER
Date/Time run: 04/28/90 11:53:36
Temperature: 27.0
1 amp step Load transient Response
119.85V
119.80V
119.75V
9.0ms
10.0ms
12.0ms
14.0ms
16.0ms
18.0ms
20.0ms

ORU MODELLING WITH EASY5

SUMMARY AND REVIEW

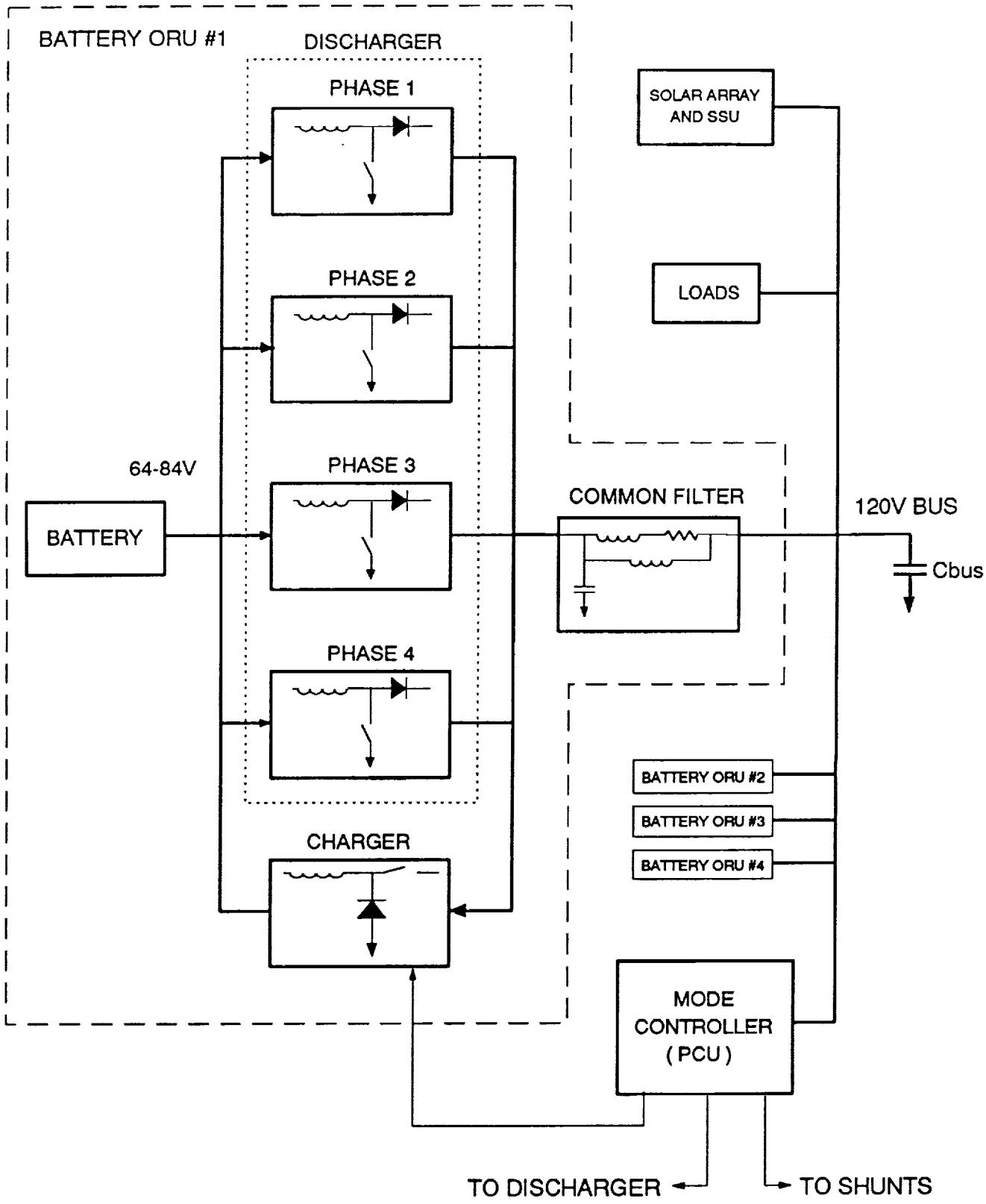
- PARALLEL DISCHARGER CONTROL
  - * BATTERY VOLTAGE IMBALANCE & CURRENT SHARING
  - * 2'nd STAGE LC FILTER
  - * EFFECT OF PARALLELING ON STABILITY
- PARALLEL CHARGER CONTROL

NEW EASY5 MODELS

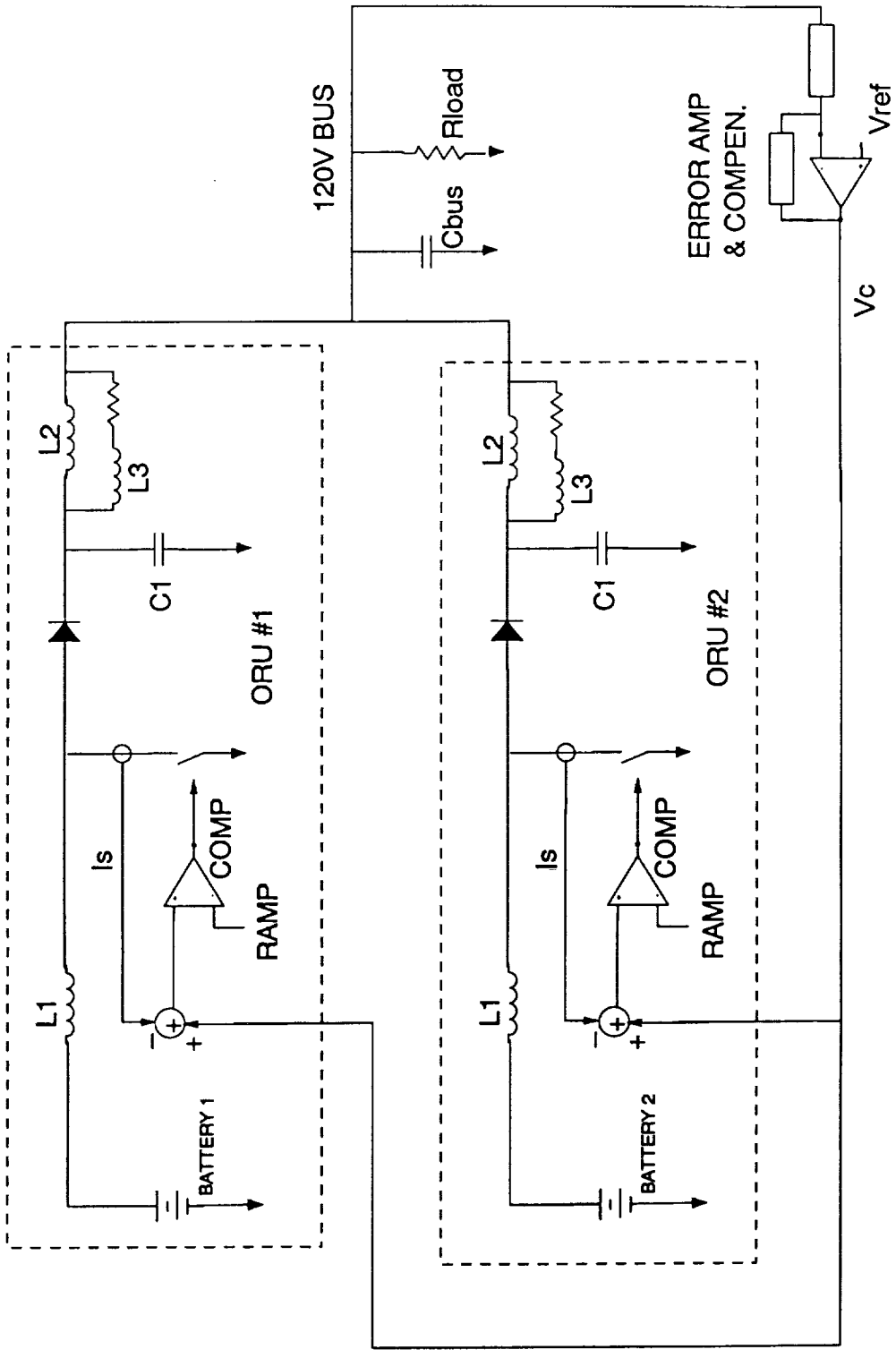
- MODE CONTROLLER (PCU)
- FOUR PHASE MODULATOR

ORU POWER SYSTEM CONTROL

SPACE PLATFORM POWER SYSTEM



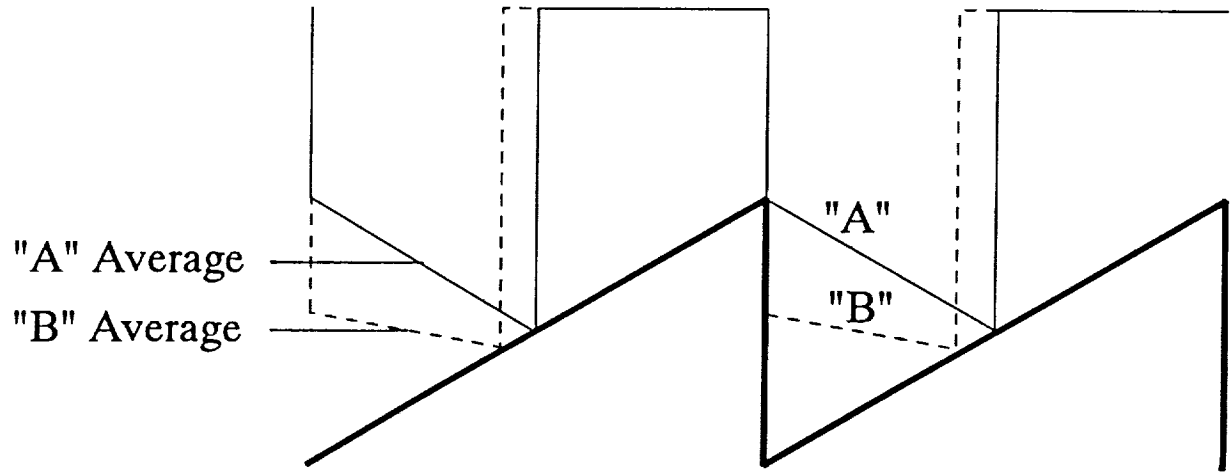
PARALLEL DISCHARGER CONTROL



DC ANALYSIS FOR PARALLEL DISCHARGERS

* BATTERY VOLTAGE IMBALANCE
  - CHARGE IMBALANCE
  - SHORTED CELL

* CURRENT MODE CONTROL : CURRENT SHARING
  - BATTERY CURRENT = INDUCTOR CURRENT
  - PEAK CURRENT DETECTION

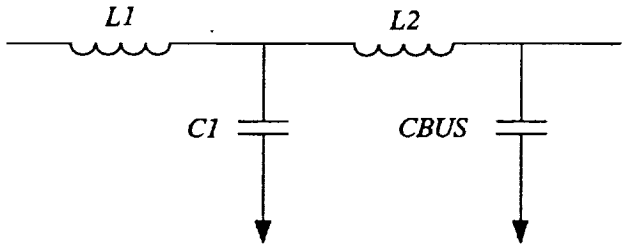


——— Inductor "A" current - - - - - Inductor "B" current

Battery "B" voltage > Battery "A" voltage

Result: Battery "B" average discharge current is higher, voltage imbalance corrected .

TWO STAGE LC FILTER



$L1 >> L2$

$CBUS >> C1$

CHARACTERISTIC EQUATION

(Note: C2 = CBUS)

$$S^4 + S^2\left[\frac{1}{L2\,C1} + \frac{1}{L2\,C2}\right] + \frac{1}{L1\,L2\,C1\,C2} = 0$$

$$\left[S^2 + \frac{1}{L1\,(C1 + C2)}\right]\left[S^2 + \frac{1}{L2\,C1} + \frac{1}{L2\,C2}\right] \approx 0$$

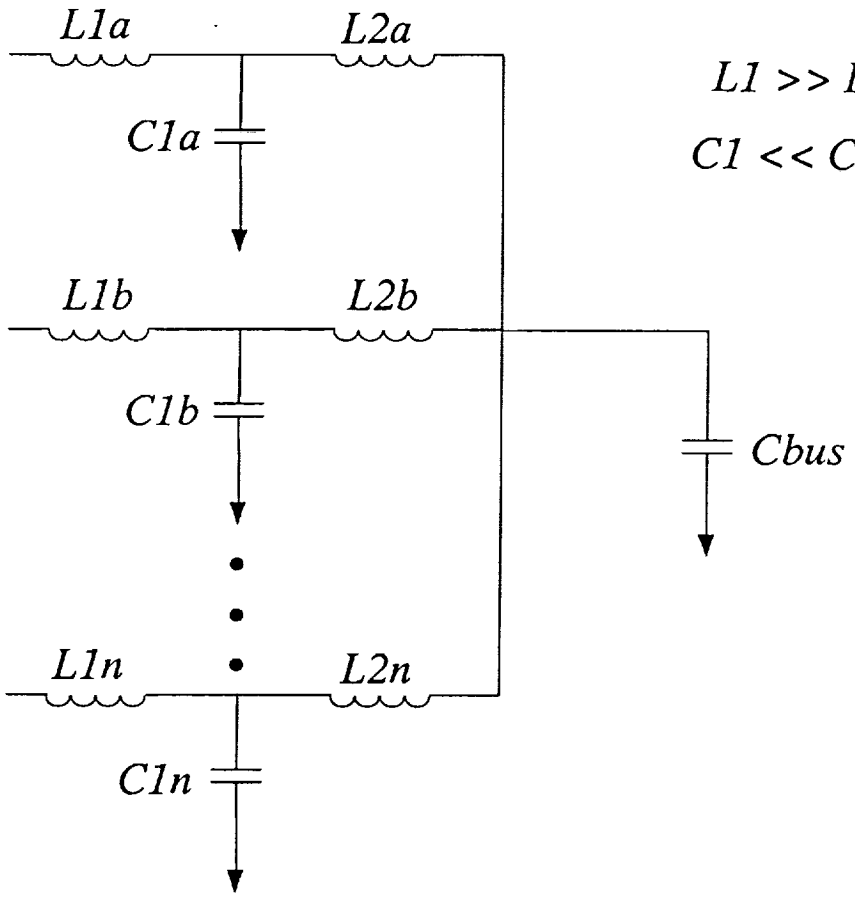
RESONANT FREQUENCIES

$$W_{o1} = \frac{1}{\sqrt{L1\,(C1 + C2)}} \approx \frac{1}{\sqrt{L1\,C2}}$$

$$W_{o2} = \frac{1}{\sqrt{L2\left[\frac{C1\,C2}{C1 + C2}\right]}} \approx \frac{1}{\sqrt{L2\,C1}}$$

PARALLEL CONVERTERS WITH TWO STAGE FILTERS

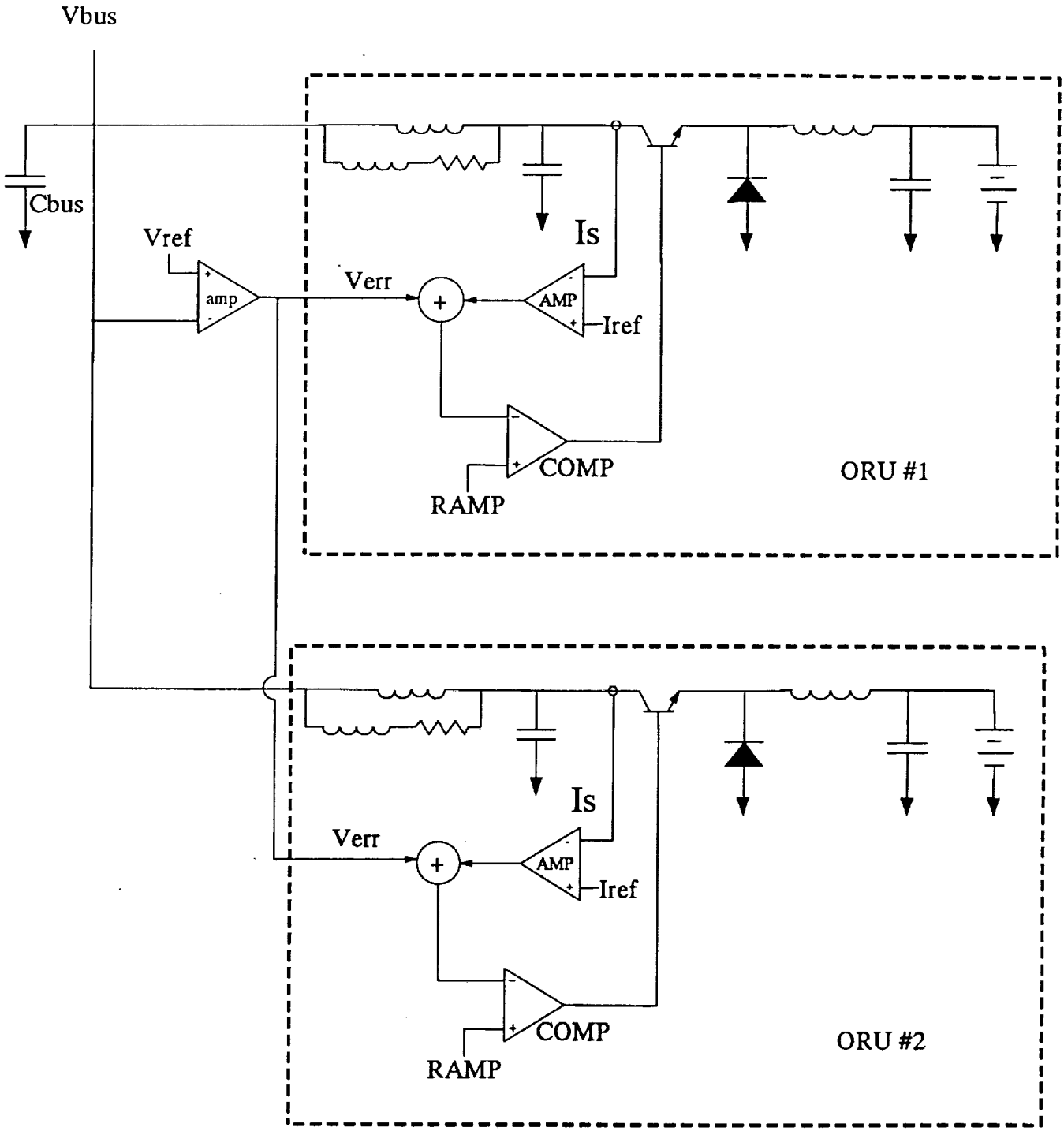
(BUCK OR BOOST EQUIVALENT)



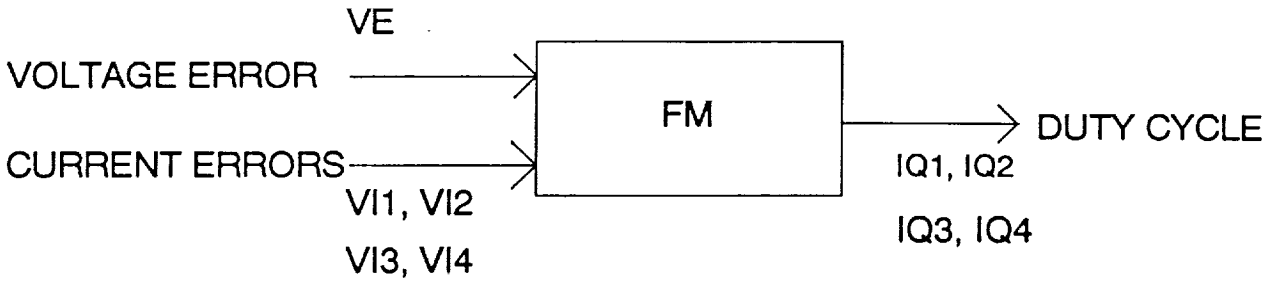
$$W_{o1} = \frac{1}{\sqrt{\frac{L1}{n}(n\,C1 + Cbus)}} \approx \frac{\sqrt{n}}{\sqrt{L1\,Cbus}}$$

$$W_{o2} = \frac{1}{\sqrt{\frac{L2}{n}\left[\frac{n\,C1\,Cbus}{n\,C1 + Cbus}\right]}} \approx \frac{1}{\sqrt{L2\,C1}}$$

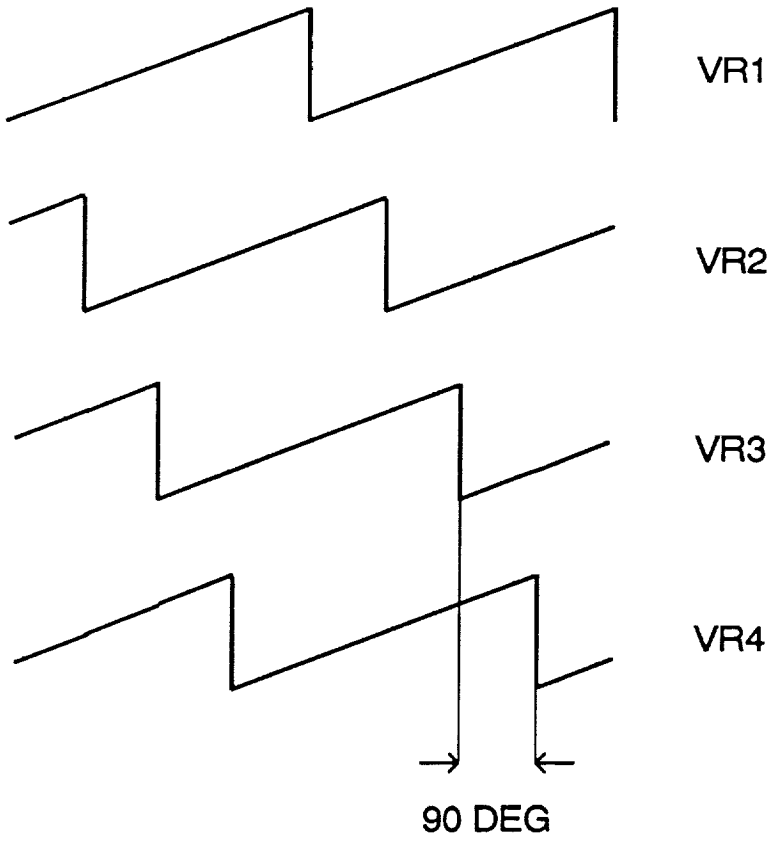
PARALLEL CHARGER MODEL



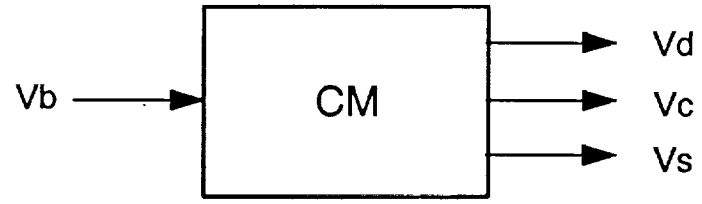
EASY5 FOUR PHASE MODULATOR MODEL

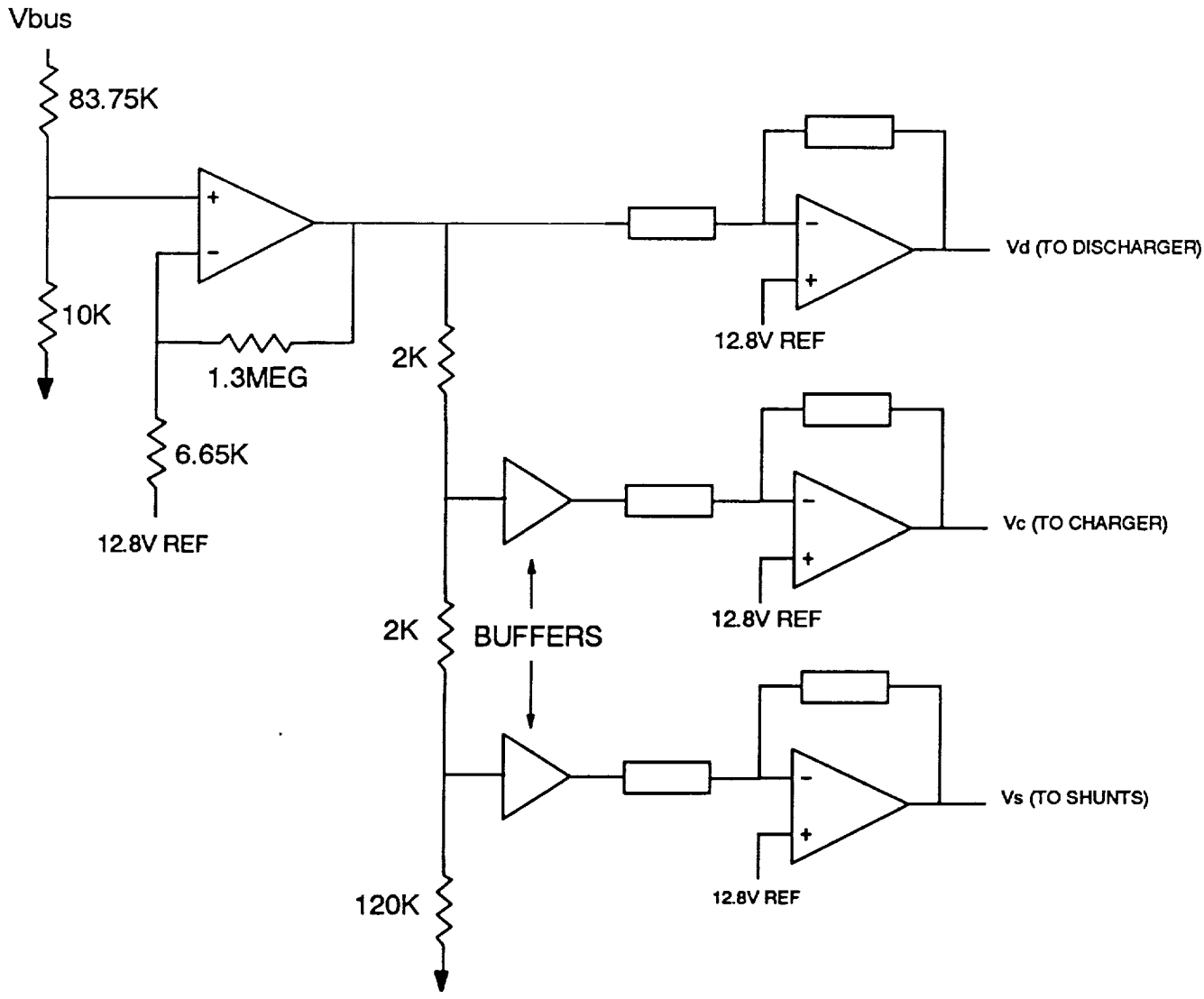


THE FOUR MODULATOR RAMPS ARE ALL SHIFTED BY 90 DEG :



EASY5 MODE CONTROLLER MODEL



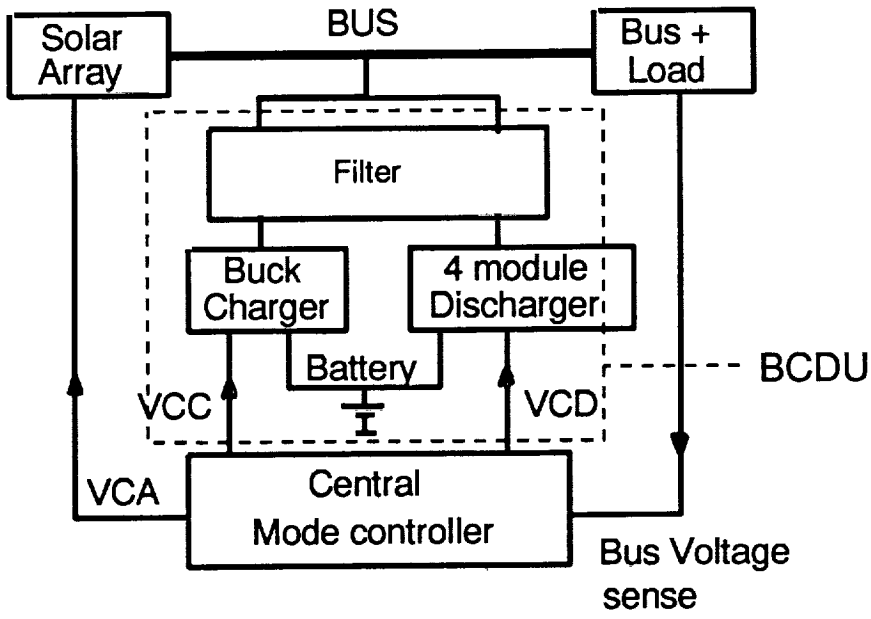


NOTE: ALL OP-AMPS HAVE ONE COMMON 12.8V REFERENCE

MODELING AND SIMULATION OF POWER SYSTEM

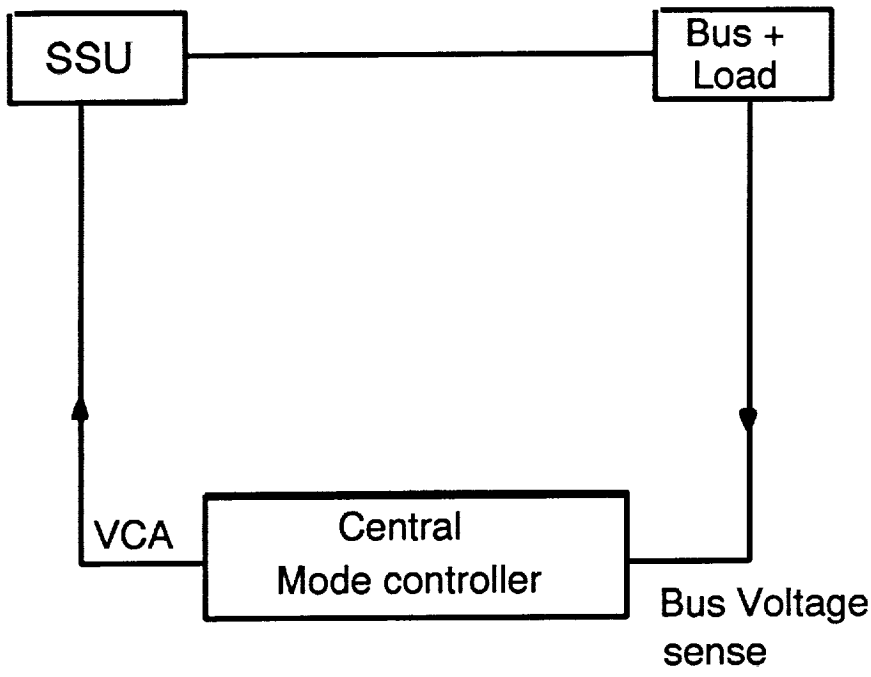
- System block diagram
- Operation of solar array
- Operation of 4-module discharger
- Operation of charger
- Mode transition from array to discharger

SYSTEM BLOCK DIAGRAM



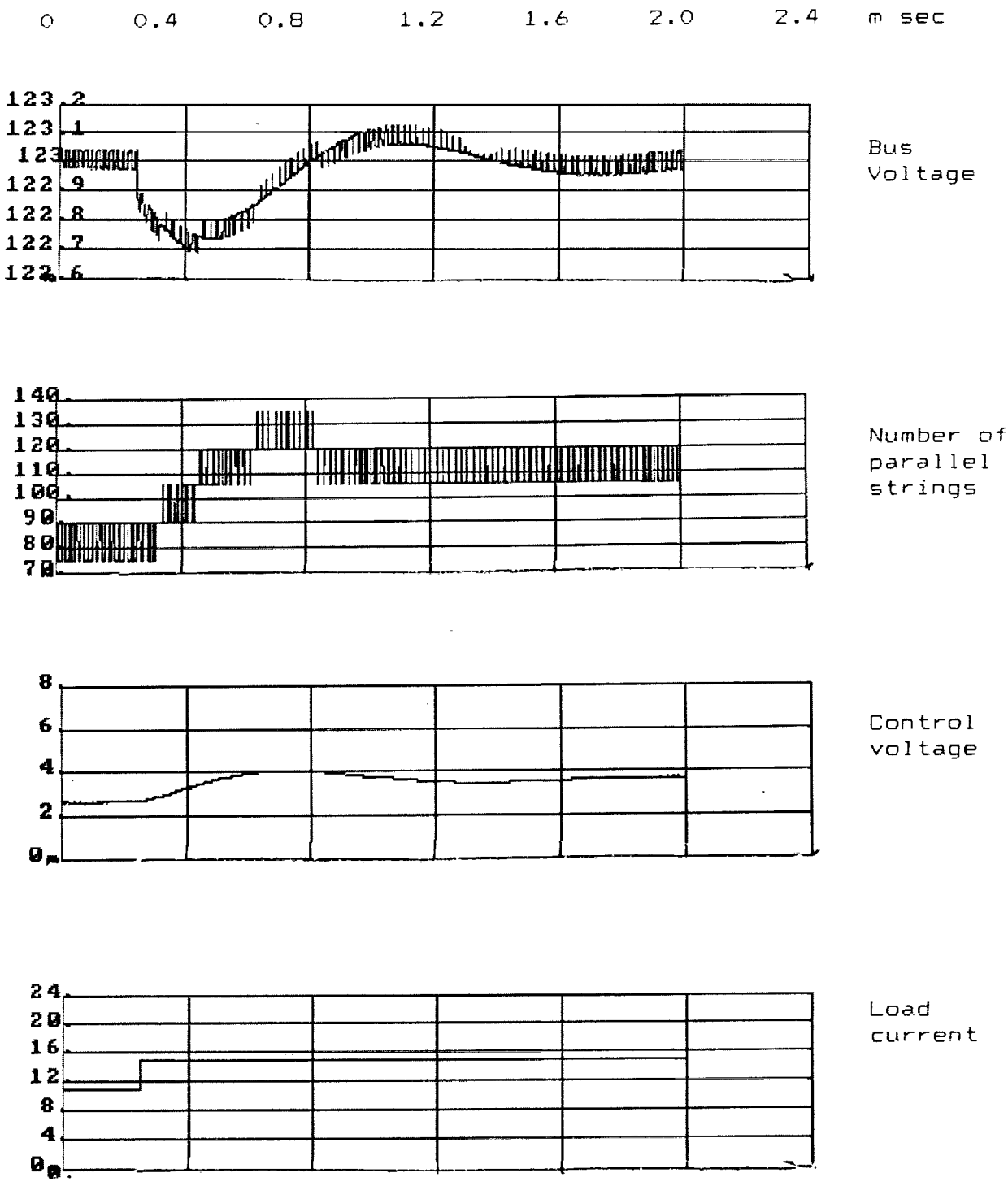
- New models are controlled by a central mode controller
- New discharger is a 4-module boost converter
- Models are set up as per the proposed hardware design
- Details are shown in the subsequent simulations
- Each mode is tested with a step load change
- Mode transition is induced by changing the illumination level

SOLAR ARRAY SWITCHING UNIT OPERATION

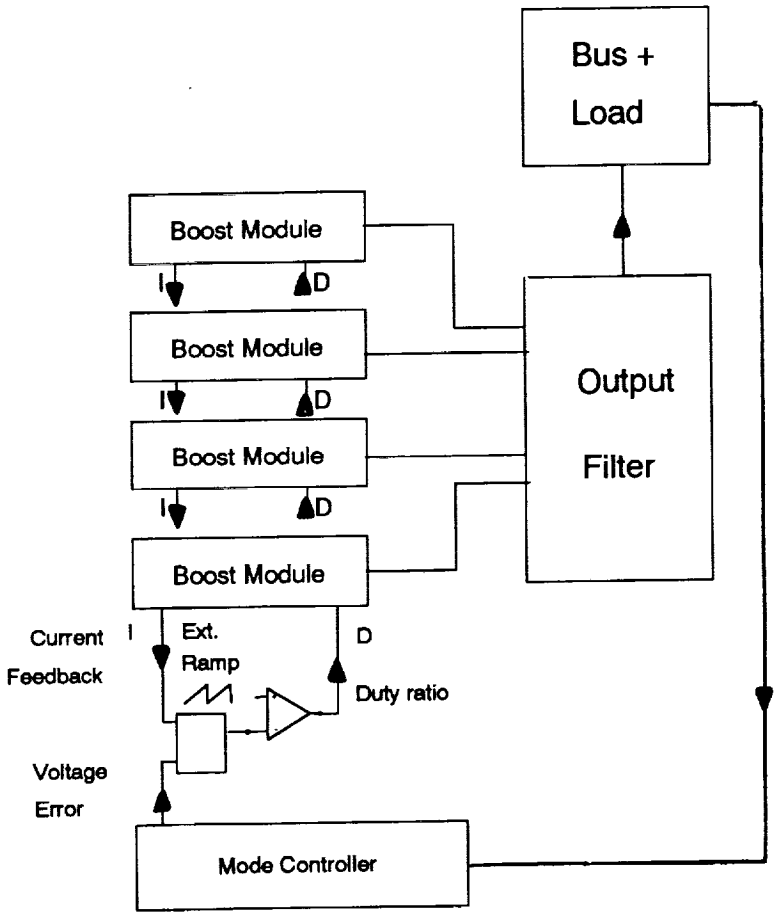


- The solar array is controlled by a central mode controller
- The bus is regulated by the array
- The simulation shows a change in parallel strings with load

SOLAR ARRAY OPERATION FOR LOAD STEP CHANGE

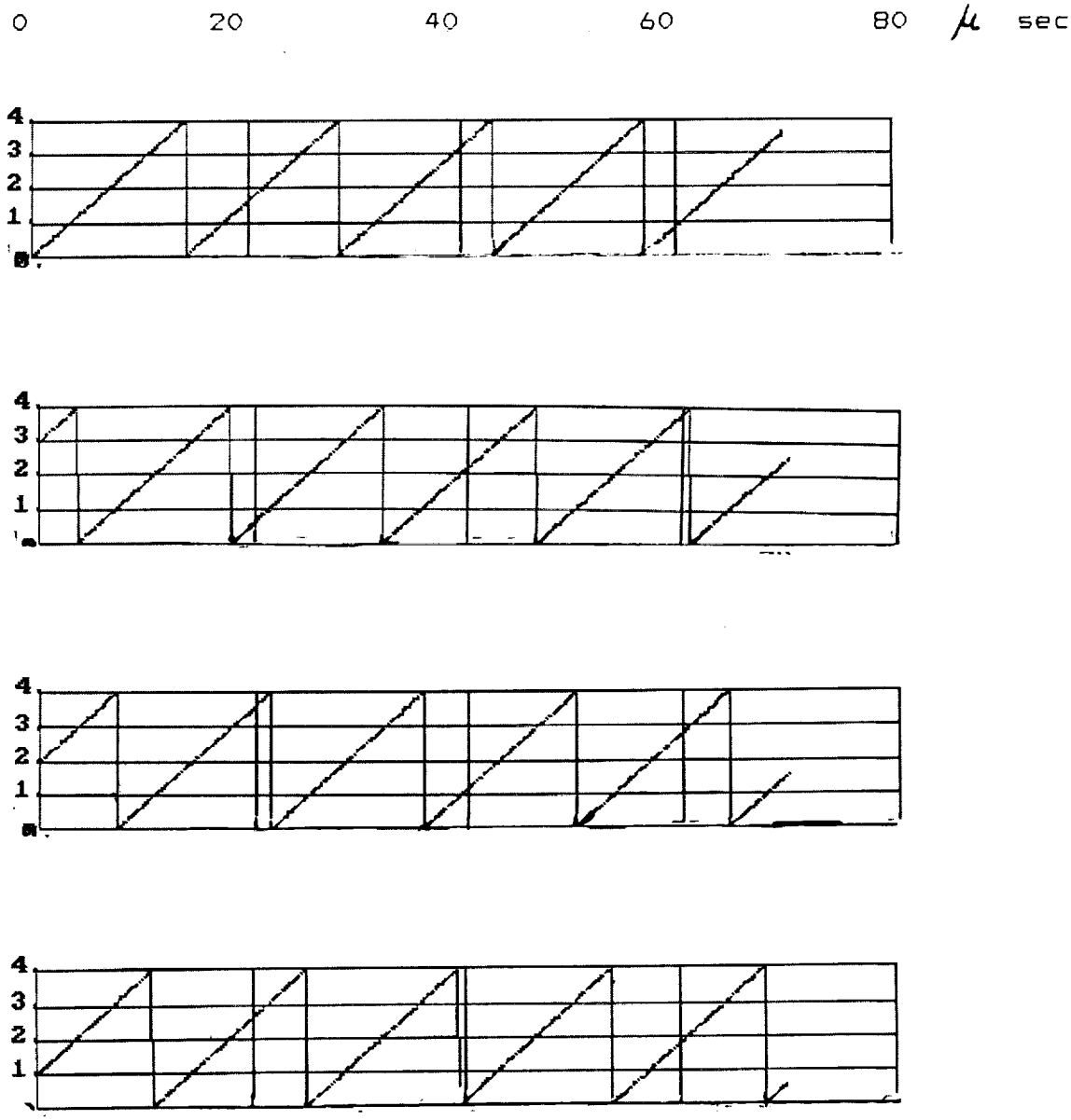


DISCHARGER MODEL TEST SIMULATION

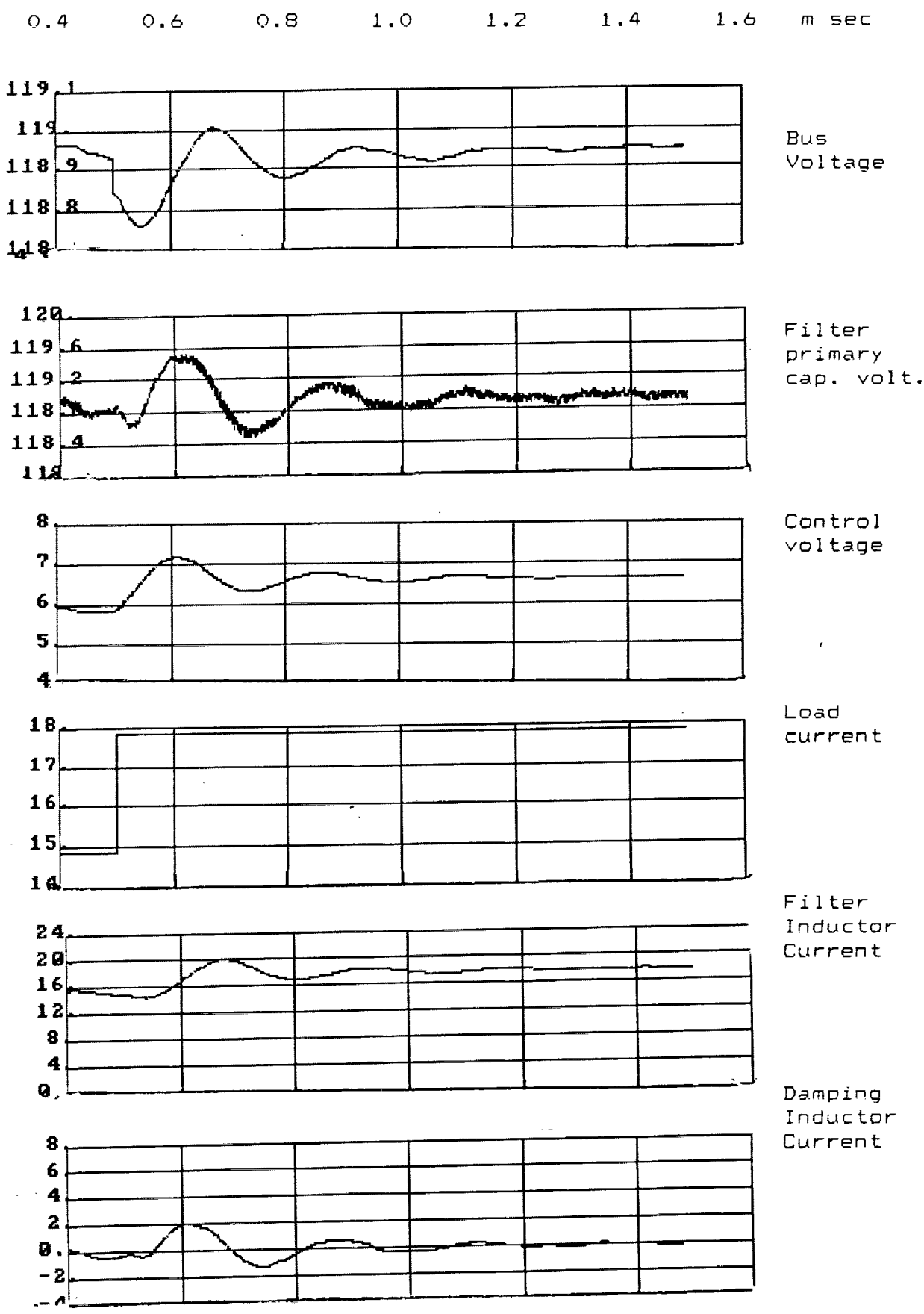


- The voltage error is common to all modules
- Each module has it's own phase shifted PW modulator
- Current feedback is applied separately to each module

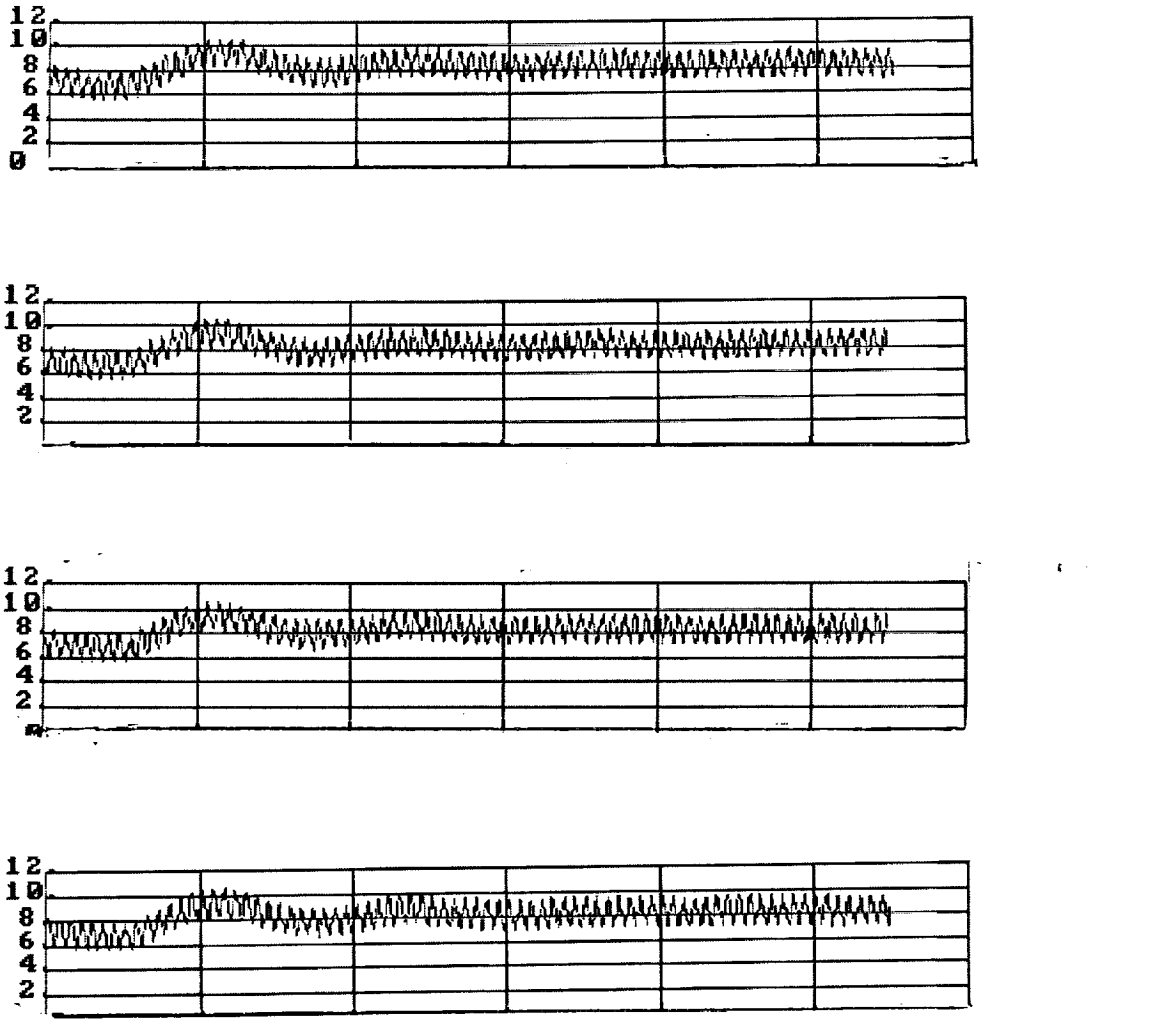
PHASE-SHIFTED RAMPS FOR MULTIMODULE BOOST DISCHARGER



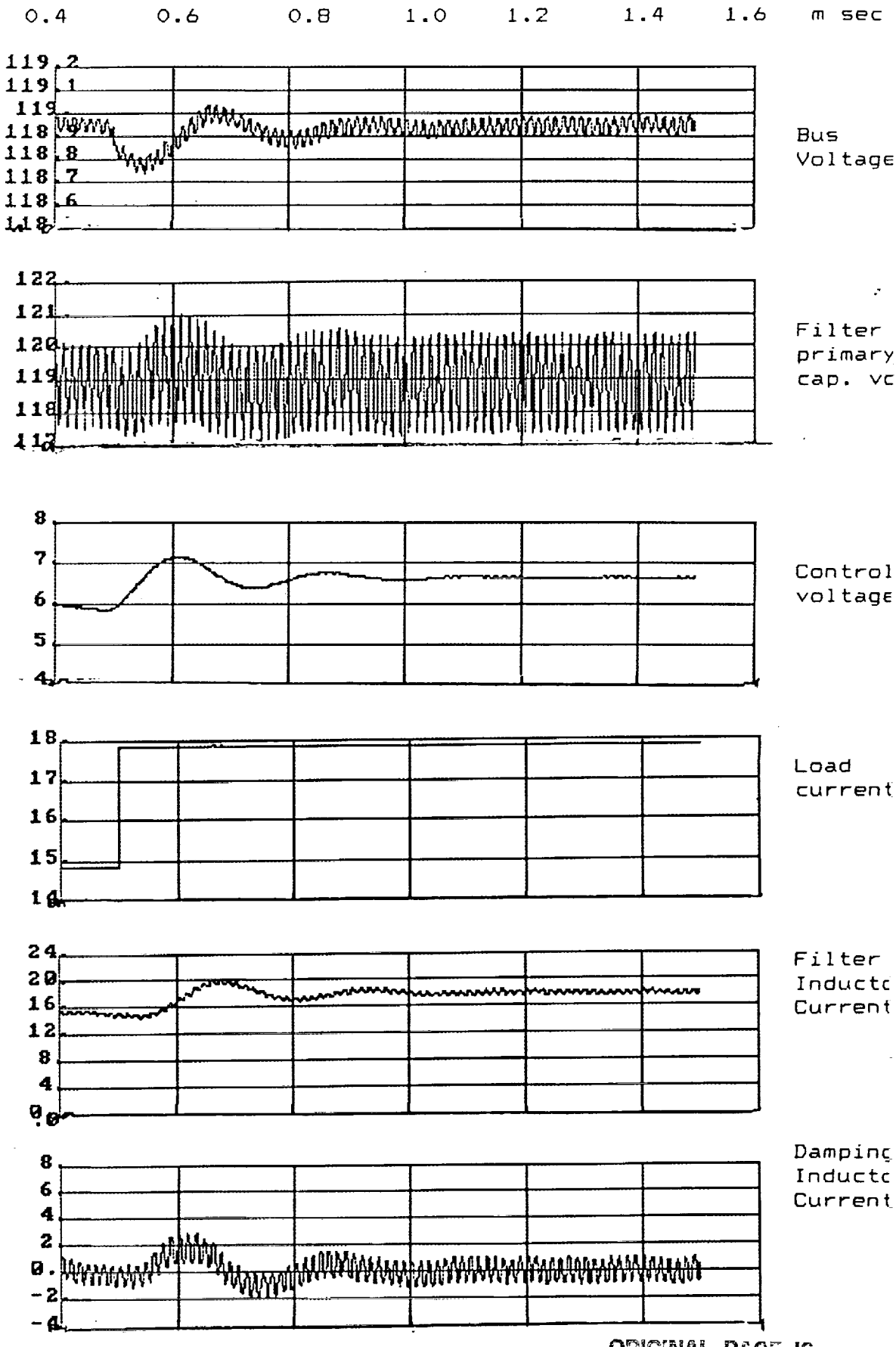
DISCHARGER OPERATION FOR A LOAD STEP CHANGE



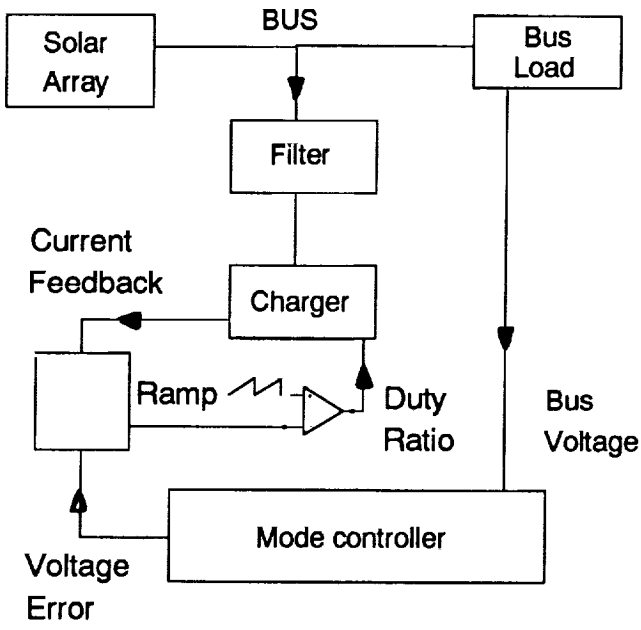
EQUAL SHARING OF CURRENT BY THE FOUR MODULES



DISCHARGER OPERATION WITHOUT PHASE SHIFTED RAMPS

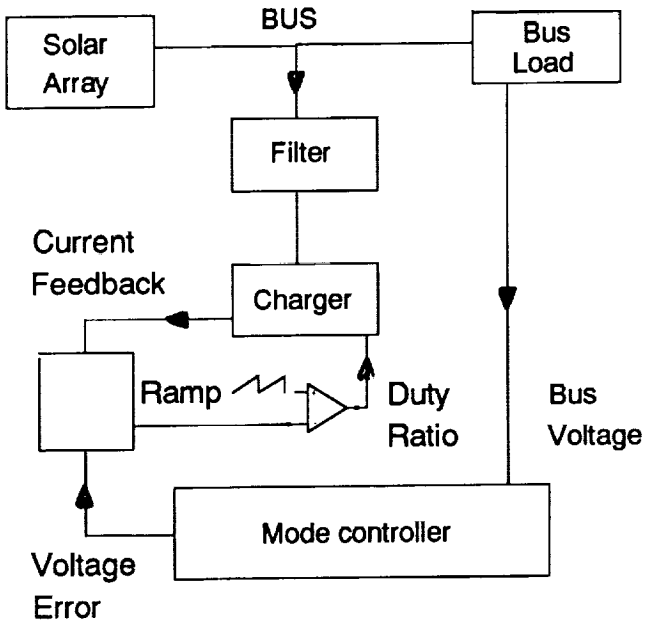


CHARGER MODEL TEST SIMULATION 1



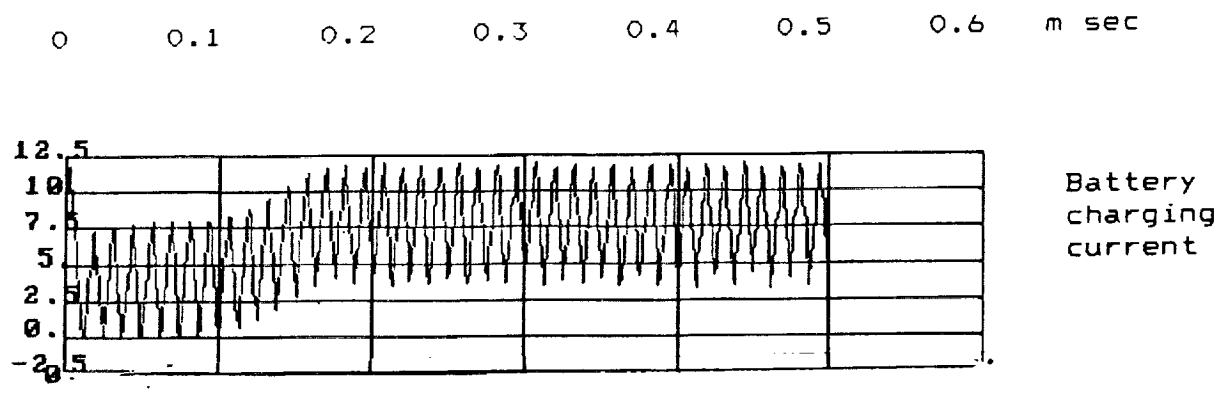
- In the voltage regulation mode, the charger regulates the bus
- The bus is regulated by changing the charging current

CHARGER MODEL TEST SIMULATION 2



- In the current regulation mode, the array regulates the bus
- The charger regulates the charging current at the limiting value

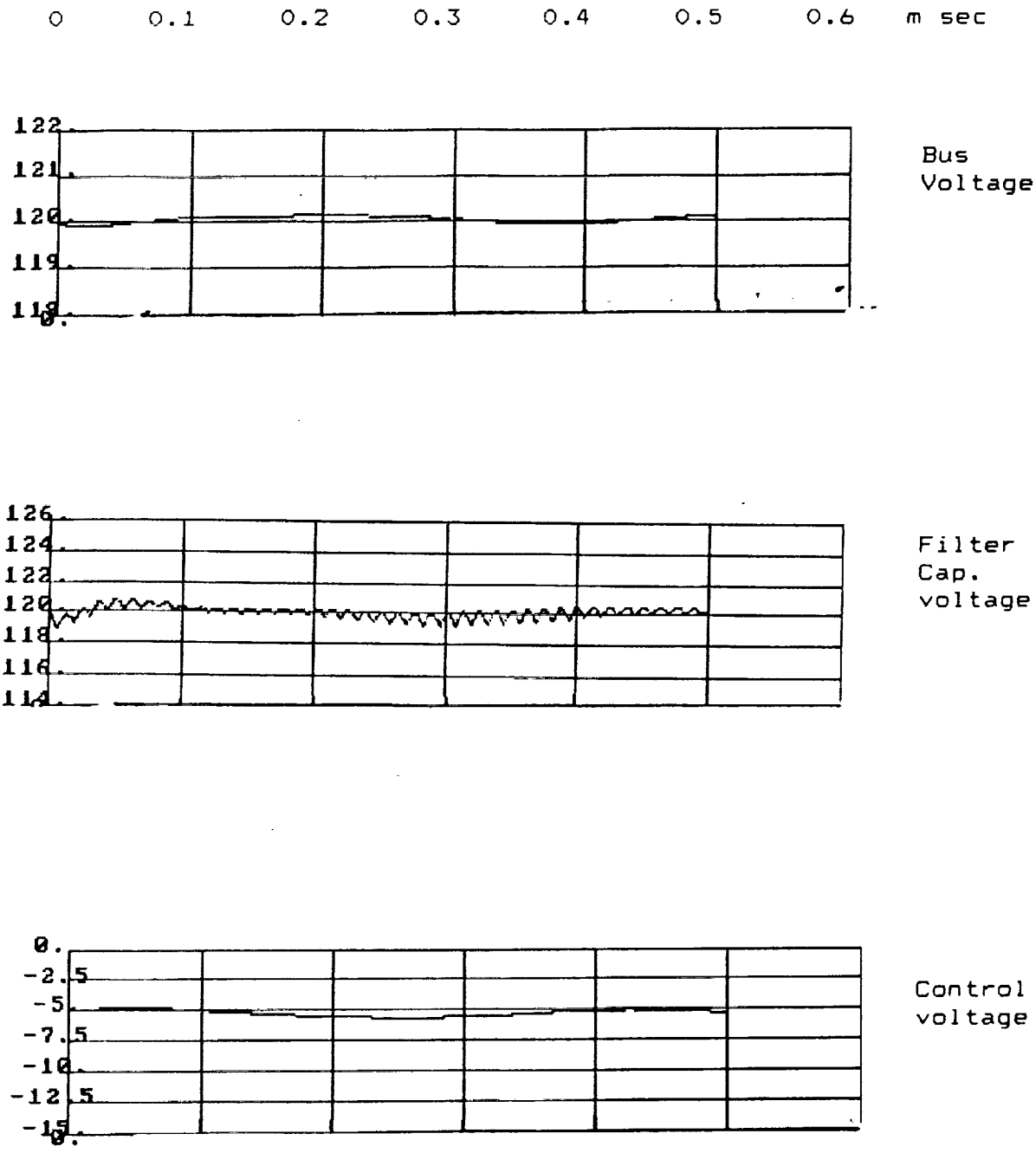
CHARGER IN CURRENT REGULATION MODE



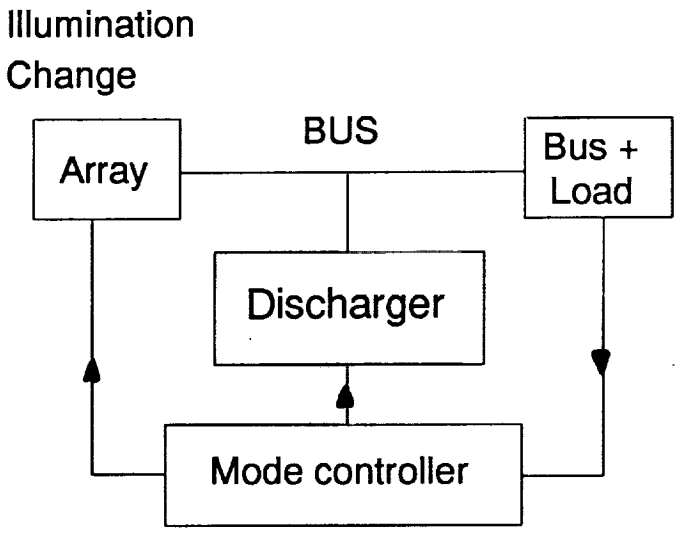
1.2 - 20A

C-2

CHARGER IN VOLTAGE REGULATION MODE

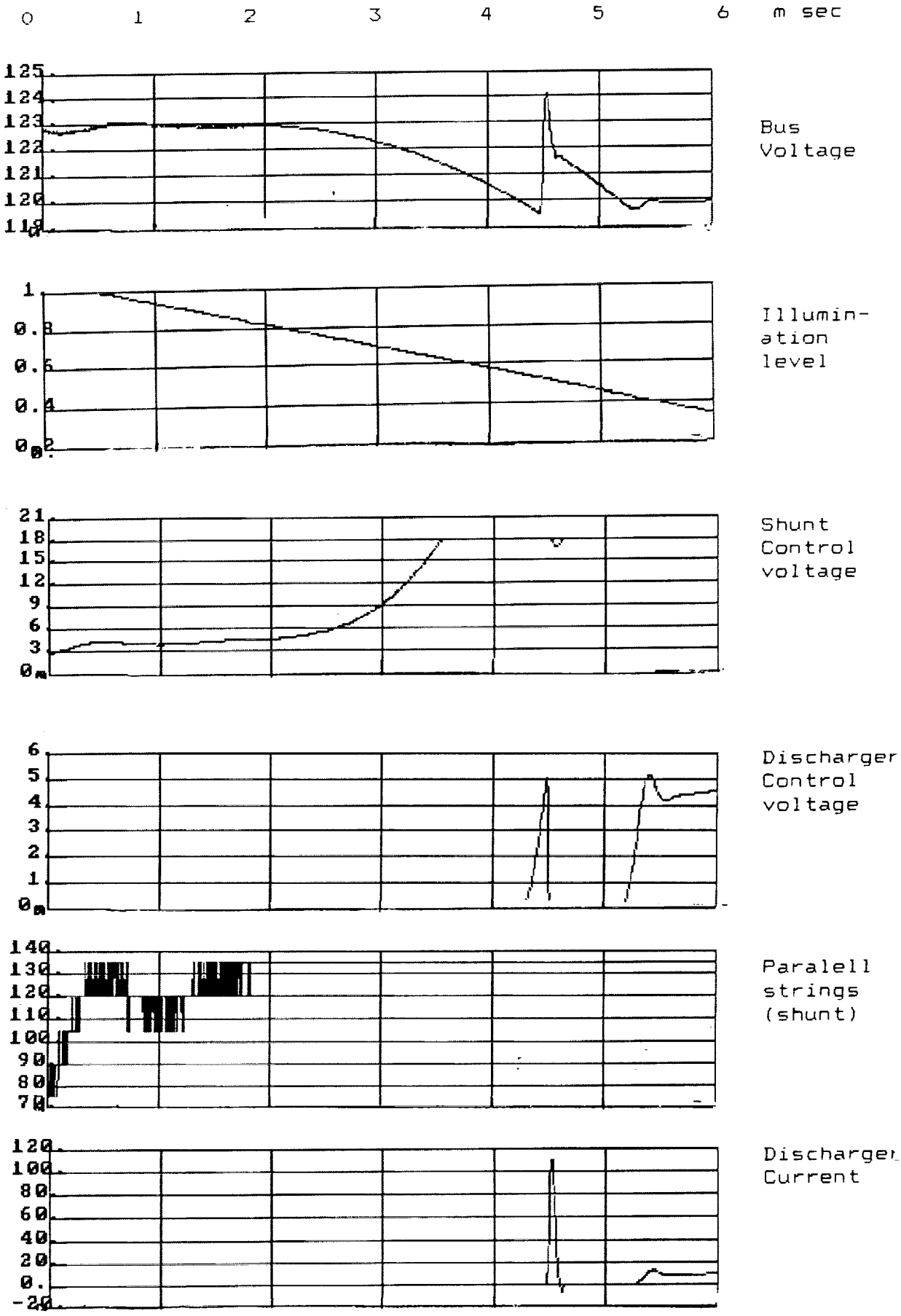


MODE TRANSITION SIMULATION



- Mode transitions are induced by changing the illumination level
- With sufficient illumination, the array regulates the bus
- At low illumination level, the discharger regulates the bus

SIMULATION FOR TRANSITION FROM SUNLIGHT TO ECLIPSE



2. SPACE PLATFORM

POWER SYSTEM TEST BED

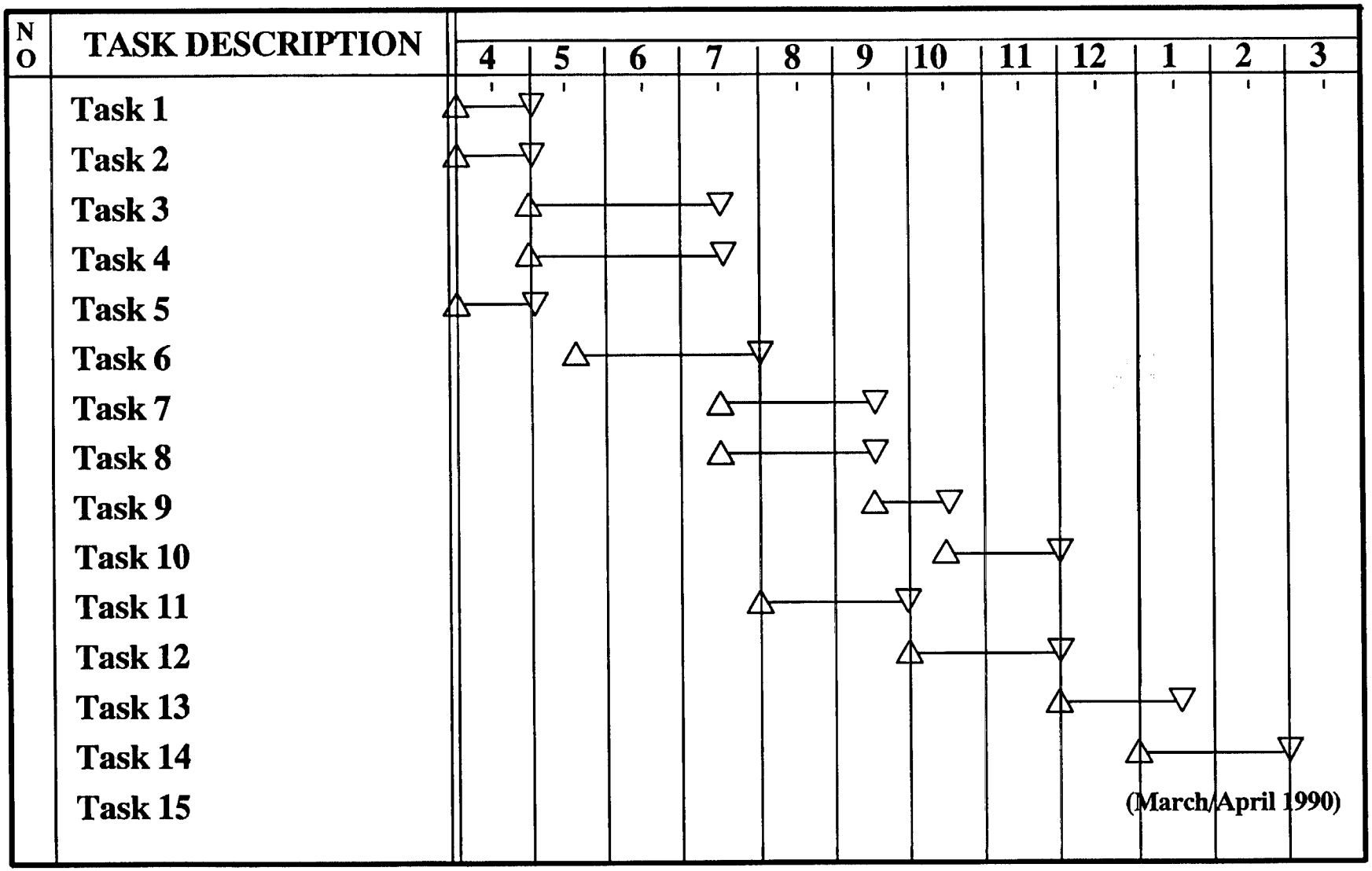
NASA/GSFC Space Platform Testbed

Year 1 Tasks

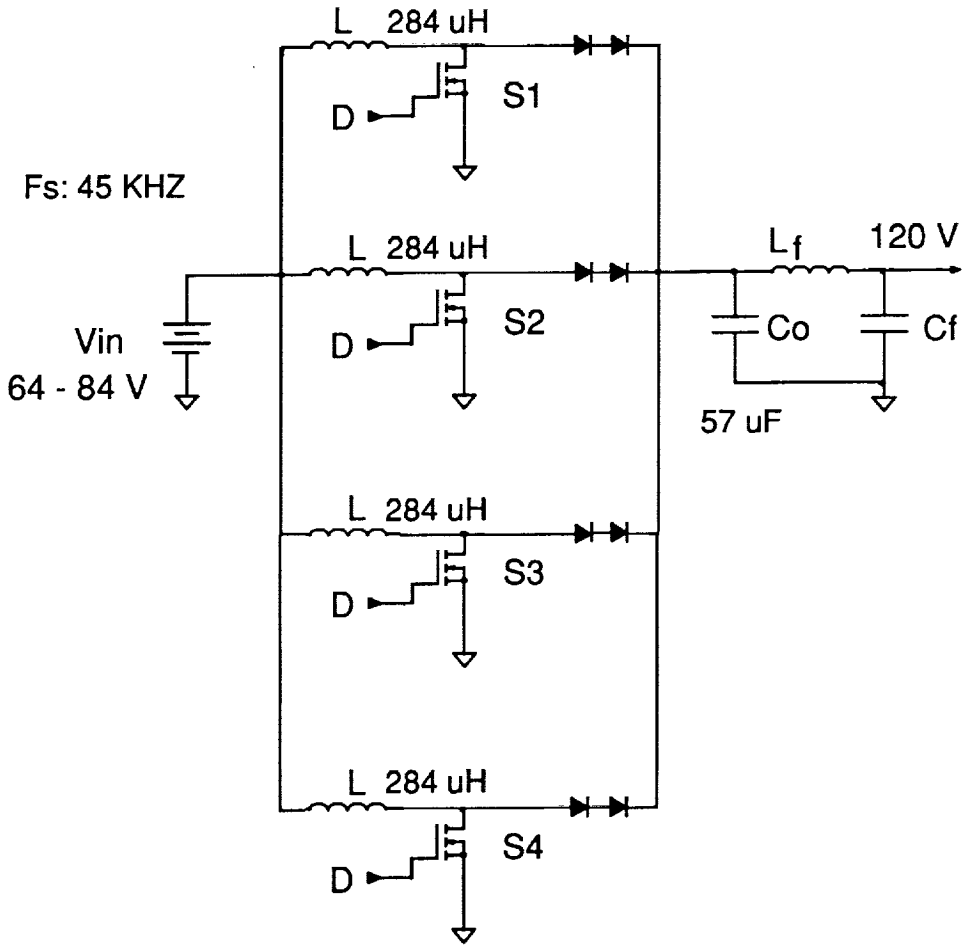
1.	Design Multi-Module Boost Converter	DS
2.	Design VFPPAT Converter	DS
3.	Build Multi-Module Boost Converter	DS
4.	Build VFPPAT Converter	SD
5.	Design Battery Charger	TS
6.	Bild Battery Charger	TS
7.	Test Multi-Module Boost Converter (Open-Loop)	DS/JI
8.	Test VFPPAT Converter	SD
9.	Select Optimum Discharger & Design Control Loop	DS/SI
10.	Build Discharger Controller, Integrate & Tester	DS/SI
11.	Test Batter Charger	TS
12.	Design Charger Controller	TS
13.	Build Charger Controller & Integrate	TS
14.	Integrate Charger & Discharger (W/Mode Controller)	DS
15.	Test ORU System	DS
16.	Investigate Bi-directional Converter	

△	PLAN
⧋	CHANGE
▲	COMPLETE

Space Platform Testbed Schedule



97% EFFICIENT FOUR MODULE BOOST DESIGN



INDUCTOR DESIGN

INDUCTOR TURNS: 31
INDUCTOR CORE WIDTH: 8.6E-3 M
INDUCTOR WINDOW WIDTH: 8.9E-3 M
INDUCTOR AIR GAP: 9 MILS
INDUCTOR WIRE SIZE: 1.54E-6 M^2

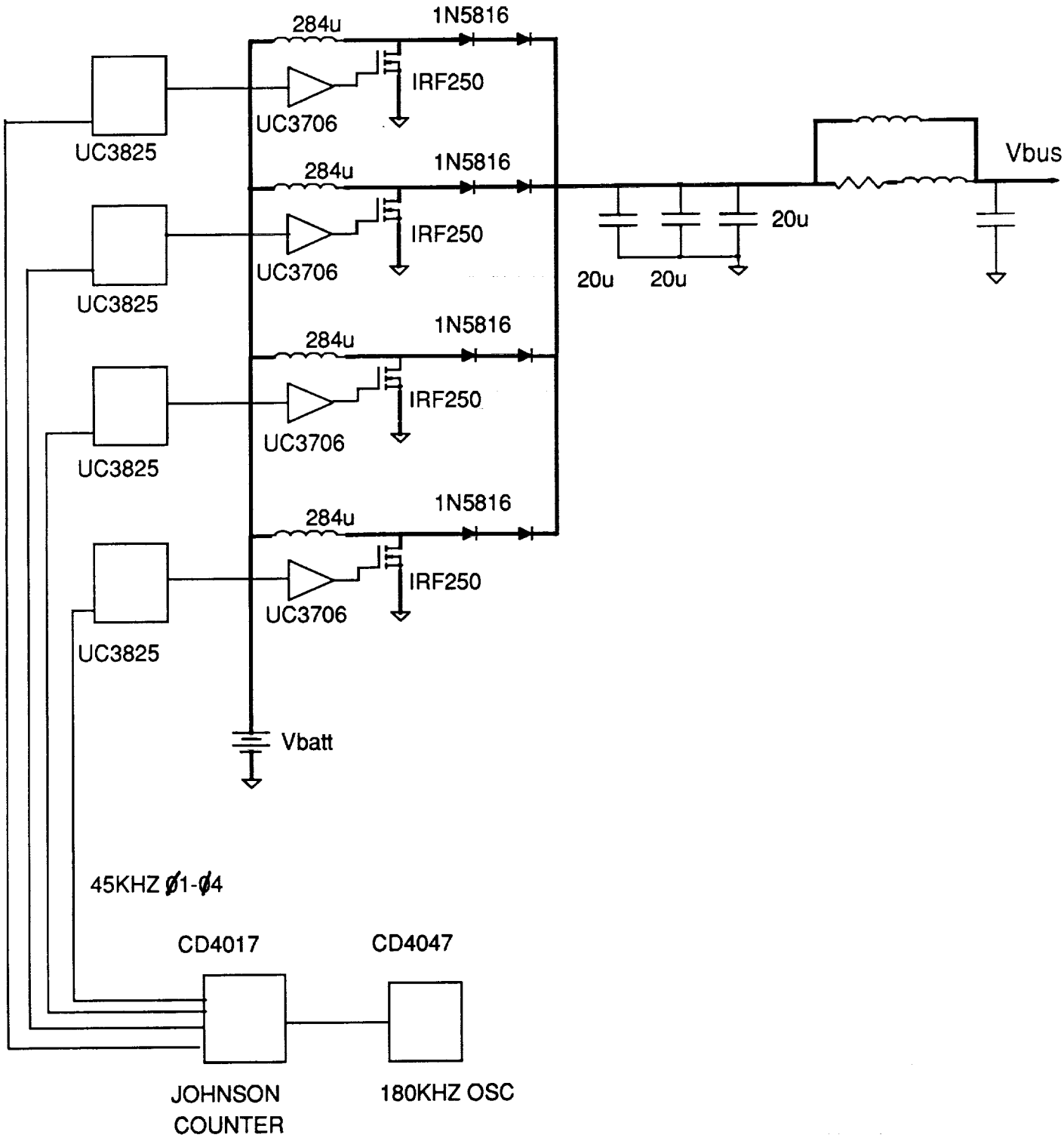
WEIGHT BREAKDOWN

INDUCTOR WEIGHT: 0.16 KG
CAPACITOR WEIGHT: 0.16 KG
TOTAL: 0.32 KG

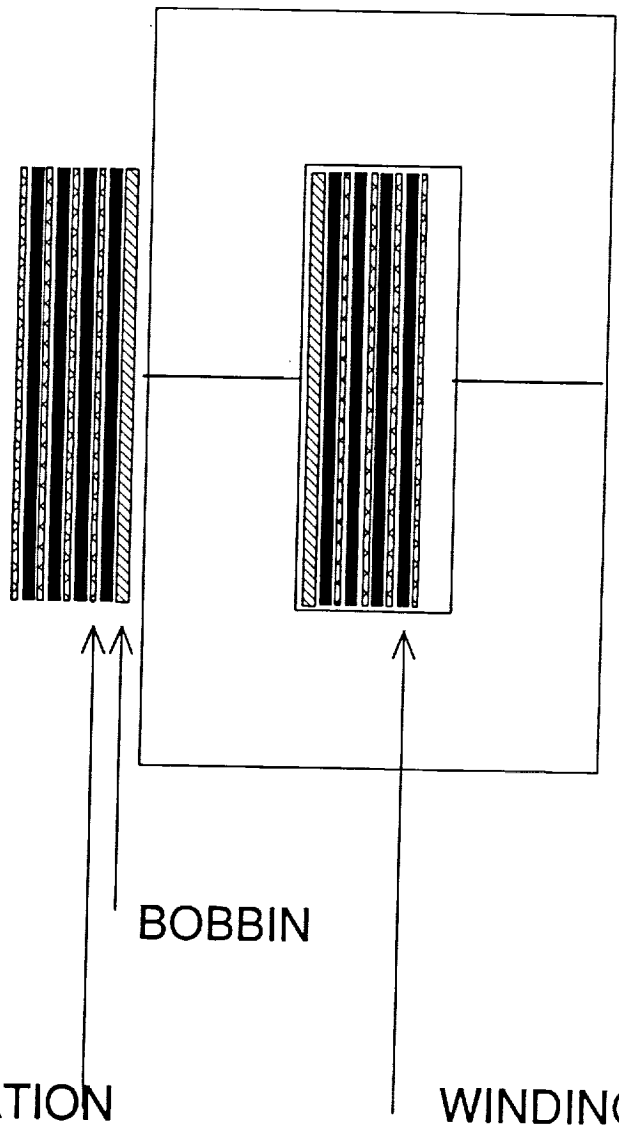
LOSS BREAKDOWN

FET CONDUCTION LOSS: 9.1 W
FET SWITCHING LOSSES: 11.8 W
DIODE CONDUCTION LOSS: 22.5 W
DIODE SWITCHING LOSSES: 3.7 W
INDUCTOR COPPER LOSS: 5.9 W
INDUCTOR CORE LOSS: 4.8 W

MULTI-MODULE BOOST HARDWARE DEVELOPMENT



FOUR MODULE BOOST INDUCTOR



CORE: MC1200-1B (METGLAS)

40 TURNS 4 MIL X 1 INCH COPPER FOIL

13 MIL AIRGAP

FOUR MODULE BOOST CONVERTER
BATTERY DISCHARGER STRESS ANALYSIS

COMPONENT PARAMETER	APPLIED VALUE	RATED VALUE	STRESS RATIO
MOSFET CONTINUOUS DRAIN CURRENT	9 AmpS	33 Amps	27%
PEAK TRANSISTOR DRAIN-TO-SOURCE VOLTAGE	120 Volts	200 Volts	62%
PEAK TRANSISTOR GATE VOLTAGE	10 Volts	±20 Volts	50%
PEAK DIODE CURRENT	9 AmpS	20 Amps	45%
PEAK DIODE REVERSE VOLTAGE	60 Volts	150 Volts	40%
OUTPUT CAPACITOR VOLTAGE	120 Volts	200 Volts	60%
OUTPUT CAPACITOR RMS CURRENT	1.1 Amps	22 Amps	5%

VOLTAGE-FED, PUSH-PULL, AUTOTRANSFORMER, (VFPPAT) BATTERY DISCHARGER

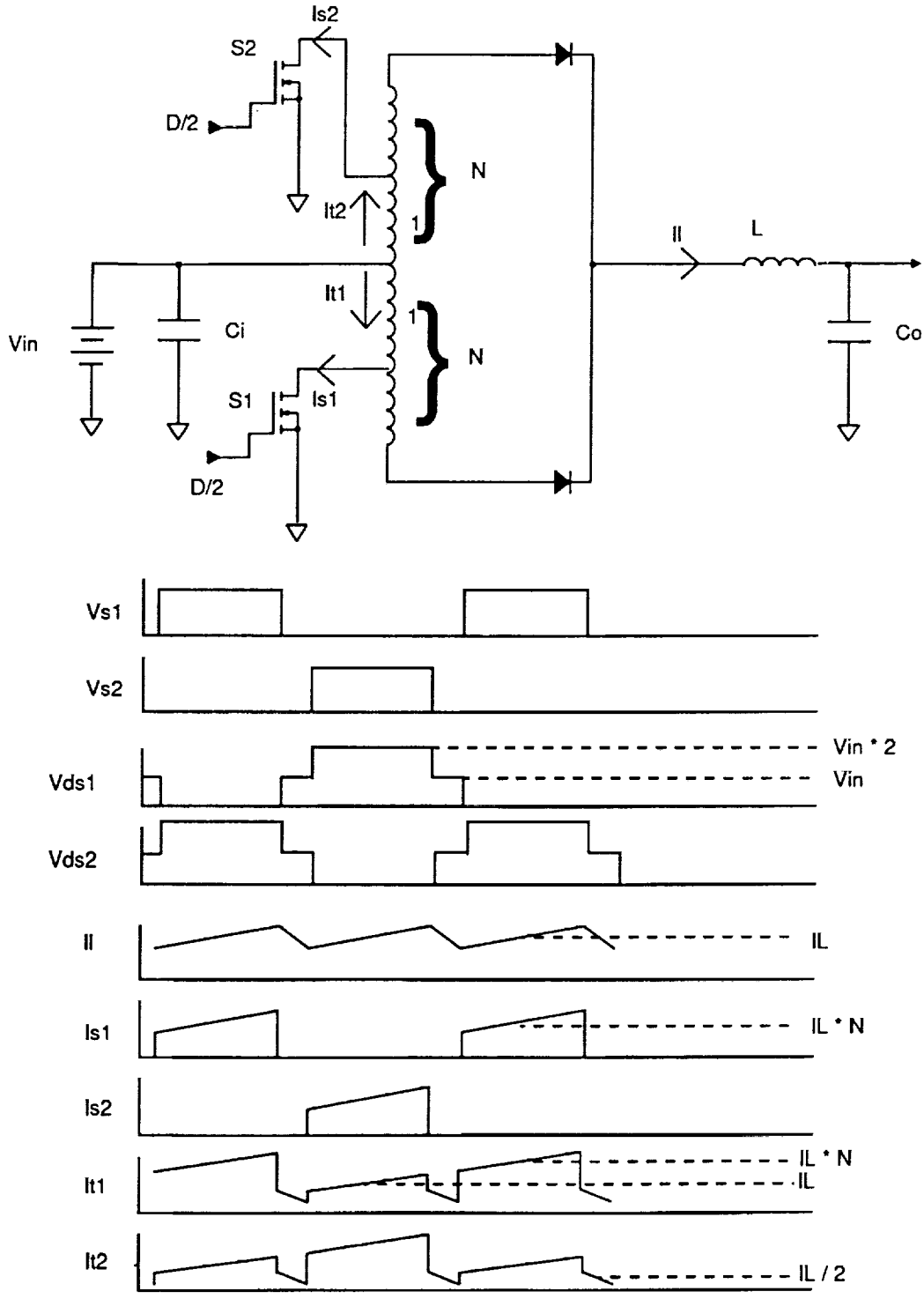
HARDWARE DESIGN TOPIC LIST

VFPPAT

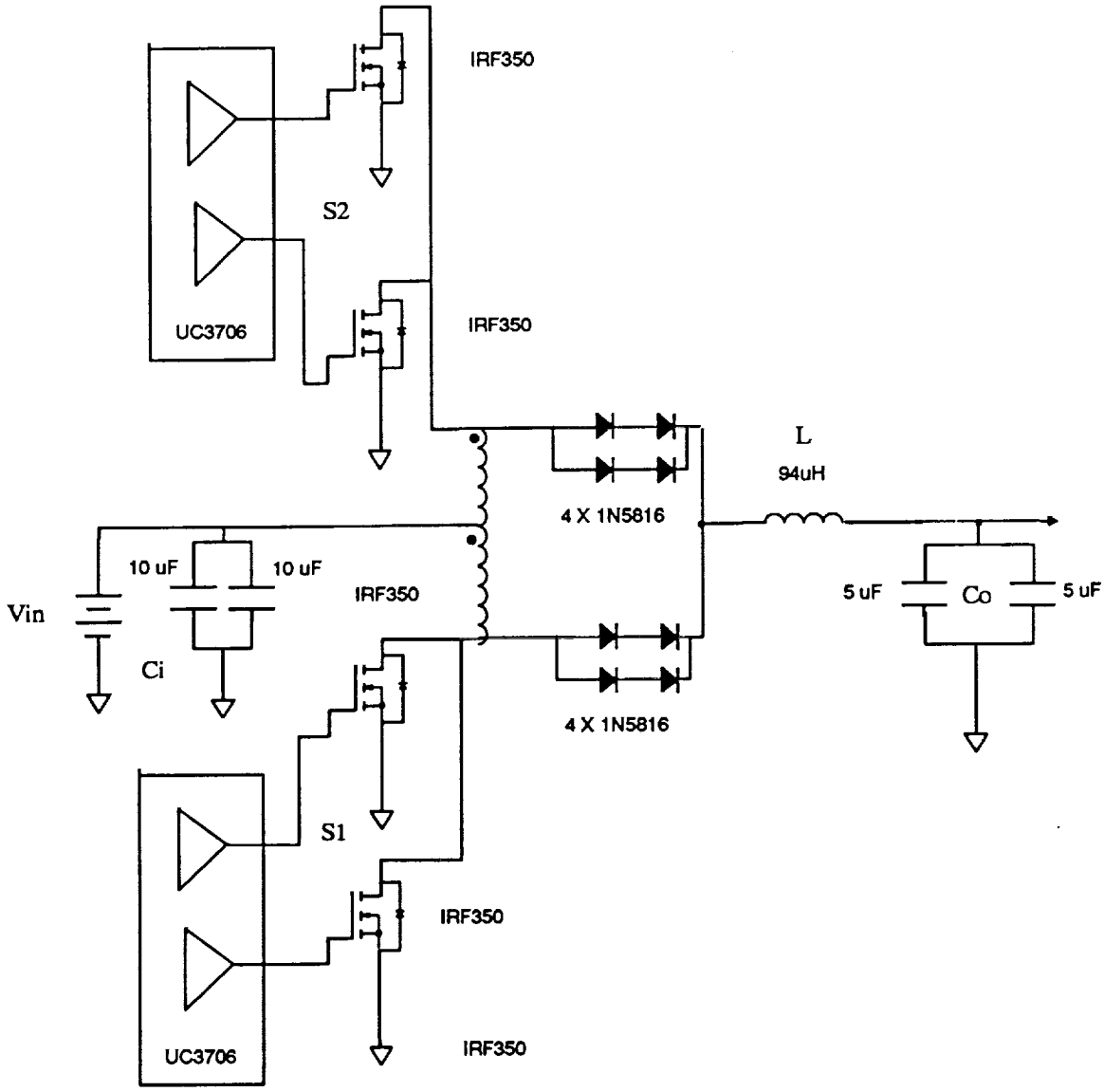
BATTERY DISCHARGER DESIGN SPECIFICATIONS

PARAMETER	SPECIFICATION
INPUT VOLTAGE RANGE	64 VDC to 84 VDC
OUTPUT VOLTAGE RANGE	120 VDC ± 4%
OUTPUT VOLTAGE RIPPLE	200 mV peak to peak
OUTPUT POWER RANGE	0 Watts to 1800 Watts
SWITCHING FREQUENCY	40 kHz
EFFICIENCY GOAL	96%
TRANSIENT PERFORMANCE	
OUTPUT VOLTAGE PEAKING RANGE	115.2 VDC - 124.8 VDC
OUTPUT SETTLING TIME	10 msec

VOLTAGE-FED, PUSH-PULL WITH TAPPED AUTOTRANSFORMER (VFPPAT) CONVERTER



VFPPAT SCHEMATIC WITH ACTUAL COMPONENTS



DISCHARGER POWER STAGE COMPONENTS

POWER SWITCH

- IRF350, INTERNATIONAL RECTIFIER
- TWO IN PARALLEL FOR HIGH EFFICIENCY
- Rdson = 250 mOHM

POWER DIODE

- 1N5816, UNITRODE
- Trr = 35 nS

INDUCTOR

- MC0007 METGLAS CUT C-CORE, MAGNETICS, INC.
- L = 94 uH

INPUT AND OUTPUT CAPACITORS

- POLYPROPYLENE, ELECTRONIC CONCEPTS, INC.
- LOW ESR
- LIGHTWEIGHT

DRIVER IC

- UC3706, DUAL OUTPUT DRIVER, UNITRODE
- PEAK OUTPUT CURRENT = 1.5 A

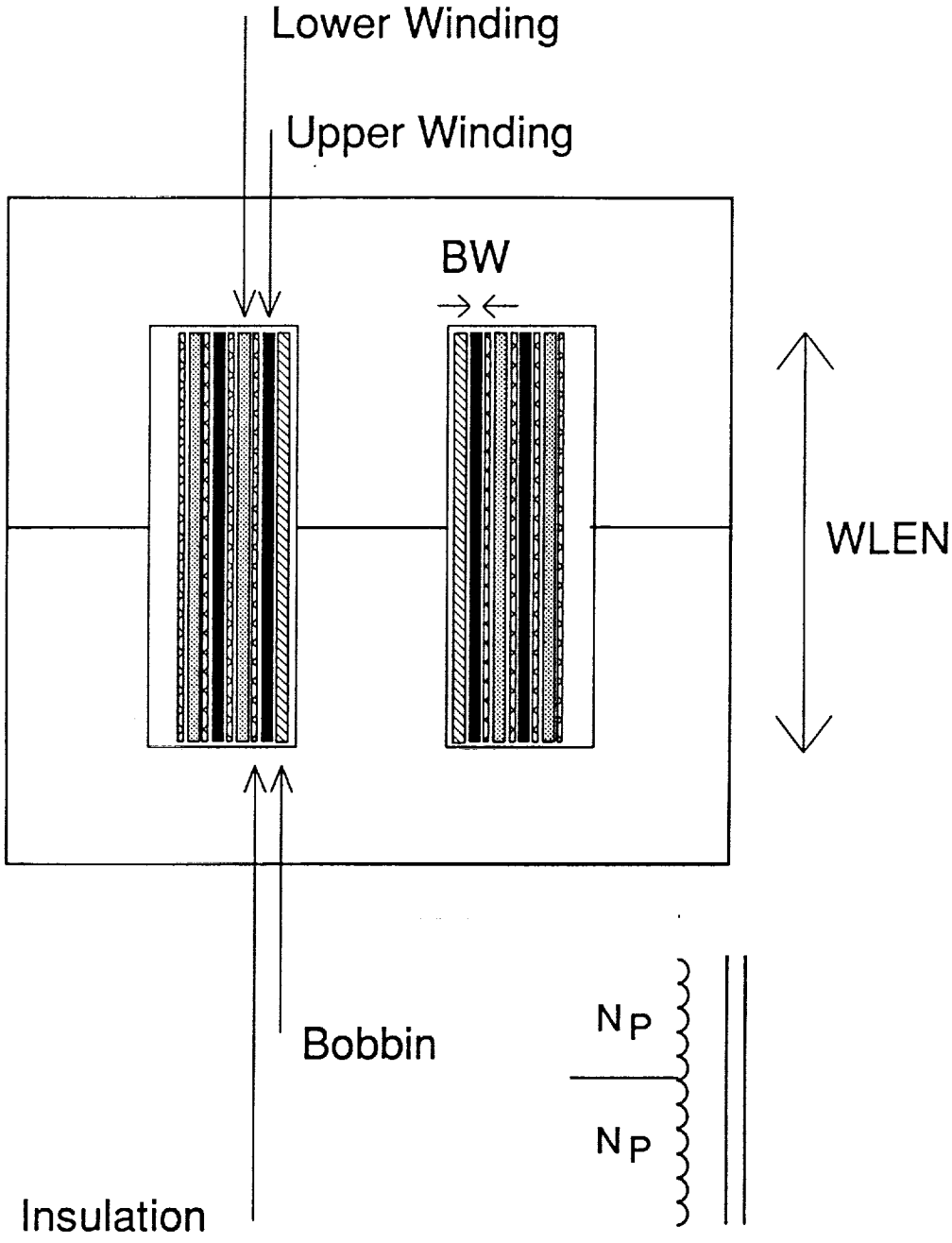
VFPPAT MAXIMUM COMPONENT STRESS EVALUATION

STRESS PARAMETER	** APPLIED VALUE	RATED VALUE	PERCENT USEAGE
PEAK TRANSISTOR DRAIN CURRENT*	8.3 Amps	60 Amps	14%
PEAK TRANSISTOR DRAIN-TO-SOURCE VOLTAGE	168 Volts	400 Volts	42%
PEAK TRANSISTOR GATE VOLTAGE	10 Volts	±20 Volts	50%
PEAK DIODE CURRENT*	8.15 Amps	20 Amps	41%
PEAK DIODE REVERSE VOLTAGE*	82 Volts	150 Volts	55%
OUTPUT CAPACITOR VOLTAGE	120 Volts	200 Volts	60%
OUTPUT RMS CURRENT*	0.4 Amps	22.5 Amps	2%
INPUT CAPACITOR VOLTAGE	84 Volts	200 Volts	42%
INPUT CAPACITOR RMS CURRENT*	3.25 Amps	15 Amps	25%

* 50% DIVISION OF PARAMETER ASSUMED

** APPLIED VALUES PREDICTED USING A SPREAD SHEET PROGRAM

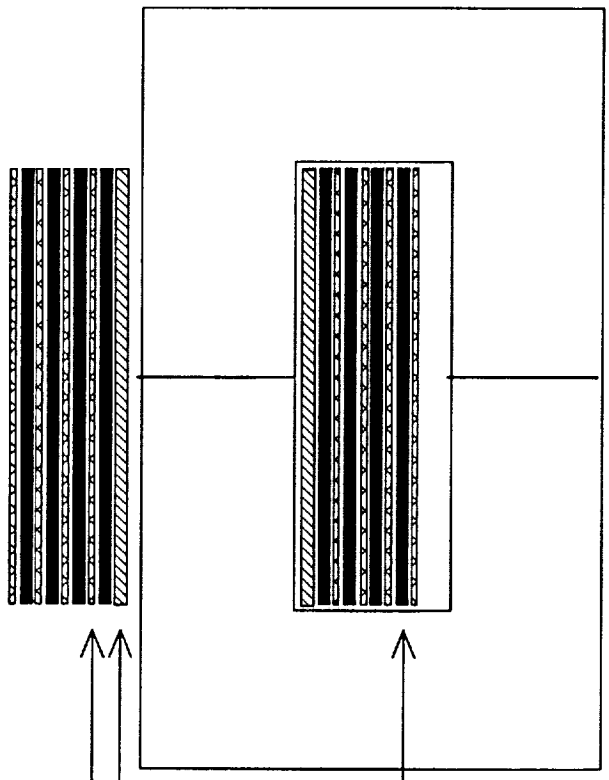
AUTOTRANSFORMER DESIGN



CORE: EE4242/15 TDK H7C1

20 TURNS 3 MIL X 1.1 INCH COPPER FOIL

VFPPAT INDUCTOR DESIGN



CORE: MC0007-1B (METGLAS)

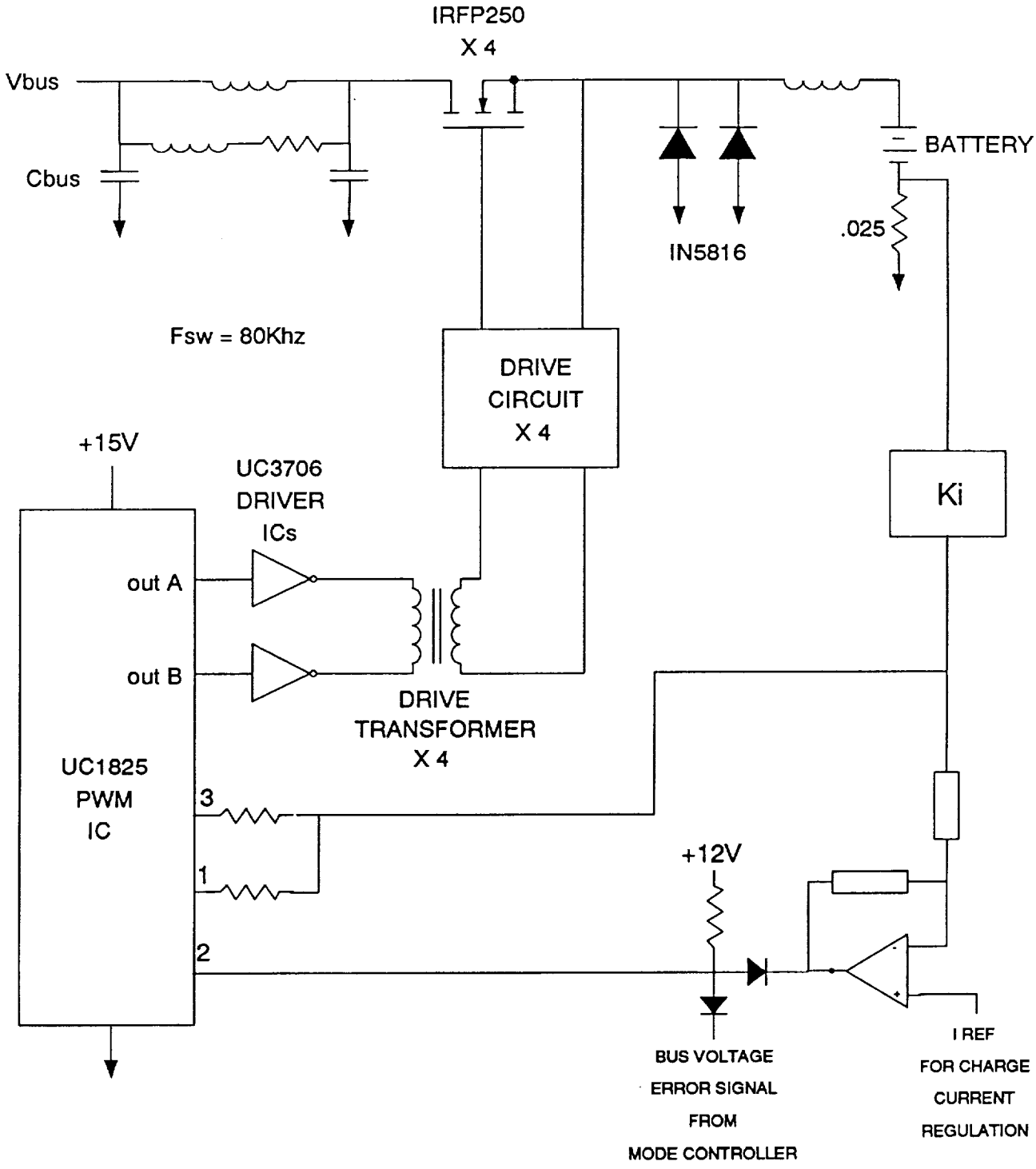
32 TURNS 4 MIL X 1 INCH COPPER FOIL

24 MIL AIRGAP

BATTERY CHARGER DESIGN SPECIFICATIONS

PARAMETER	SPECIFICATION
INPUT VOLTAGE RANGE	120 VOLTS +/- 4%
OUTPUT VOLTAGE RANGE	53 - 84 VOLTS
DUTY RATIO	44% TO 70%
TOPOLOGY	SINGLE PHASE BUCK
CHARGE CURRENT RANGE	1 TO 20 AMPS
SWITCHING FREQUENCY	80 KHz
ESTIMATED EFFICIENCY	95 %
CONTROL	BUS VOLTAGE / CHARGE CURRENT

BATTERY CHARGER SCHEMATIC



CHARGER POWER STAGE COMPONENTS

POWER SWITCH

- IRFP250 MOSFET, INTERNATIONAL RECTIFIER
- FOUR IN PARALLEL FOR HIGH EFFICIENCY
- Rdson = 85 mOHM

POWER DIODE

- 1N5816, UNITRODE
- TWO IN PARALLEL
- Trr = 35 nS

INDUCTOR

- METGLAS CUT C-CORE, MAGNETICS, INC.
- L = 46uH

INPUT CAPACITOR

- POLYPROPYLENE, ELECTRONIC CONCEPTS, INC.
- LOW ESR
- LIGHTWEIGHT

INPUT FILTER

- COMMON TO DISCHARGER

BATTERY CHARGER STRESS ANALYSIS

COMPONENT PARAMETER	APPLIED VALUE	RATED VALUE	STRESS RATIO
MOSFET CONTINUOUS DRAIN CURRENT	5 Amps	33 Amps	15%
PEAK TRANSISTOR DRAIN-TO-SOURCE VOLTAGE	120 Volts	200 Volts	60%
PEAK TRANSISTOR GATE VOLTAGE	+10 Volts	±20 Volts	50%
RMS DIODE CURRENT	7.5 Amps	20 Amps	38%
PEAK DIODE REVERSE VOLTAGE	120 Volts	150 Volts	80%
INPUT CAPACITOR VOLTAGE	120 Volts	200 Volts	60%
INPUT CAPACITOR RMS CURRENT	4.2 Amps	15 Amps	28%

CHARGER POWER INDUCTOR DESIGN

MATERIAL : METGLAS

- HIGH Bsat ALLOWS SMALL INDUCTOR SIZE
- LOW LOSS
  -1 MIL LAMINATION : HIGH RESISTIVITY & LOW EDDY CURRENT LOSS
- HIGH PERMEABILITY
- LOW Bsat DRIFT OVER TEMPERATURE

CONDUCTOR AND INSULATION

- COPPER FOIL : 5 MIL THICKNESS
  * HIGH WINDOW UTILIZATION
  * LOW SKIN EFFECT LOSS
  * LOW PROXIMITY LOSS
- INSULATION : 2 MIL KAPTON TAPE

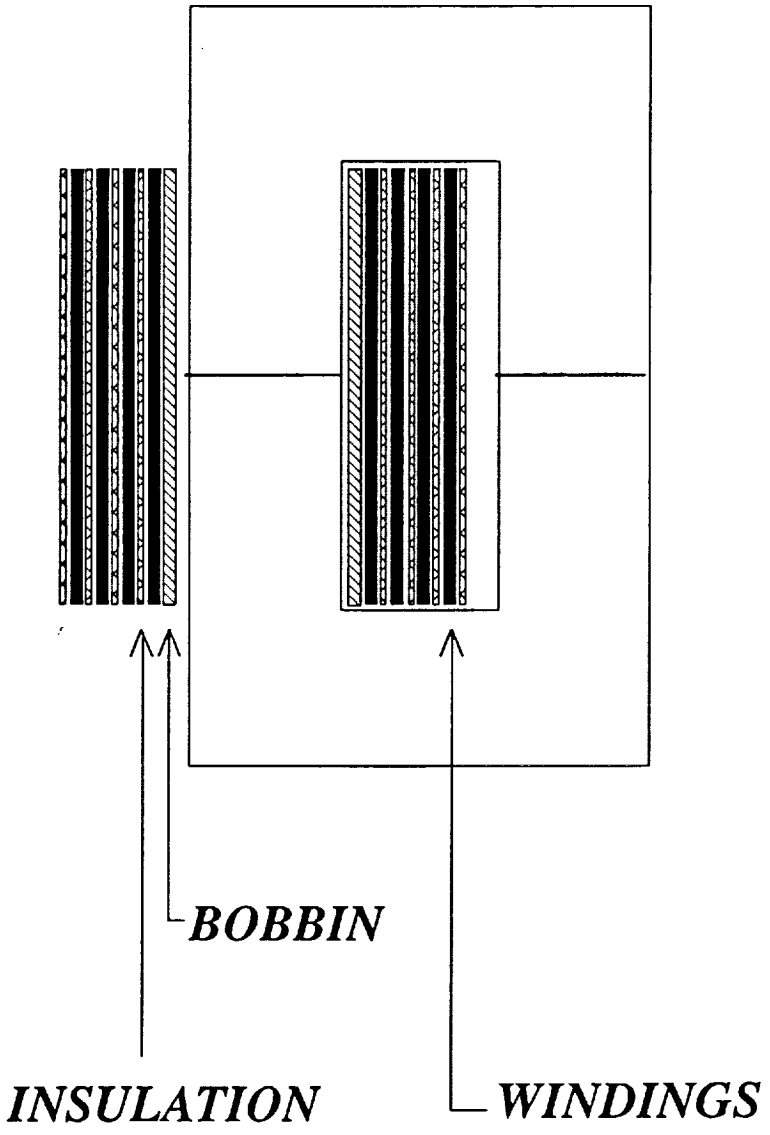
CORE

- MAGNETICS, INC. MC1603 CUT C-CORE
- 14 MIL GAP FOR L = 46 uH
- DISADVANTAGE : GAP LOSS AND PROXIMITY LOSSES

DESIGN

- SPREAD SHEET PROGRAM
- AREA PRODUCT APPROACH
- TRADE-OFFS : LOSSES AND WEIGHT
- CONSIDERATIONS : STANDARD FOIL AND TAPE DIMENSIONS

CHARGER POWER INDUCTOR DESIGN



CORE : MC1603-1B (METGLAS)

21 TURNS COPPER FOIL (5 MIL X 1 INCH)

14 MIL AIR GAP (PER LEG)

CHARGER PWM AND DRIVE CIRCUITS

ISOLATED GATE DRIVE

DRIVE TRANSFORMER

- CORE RESET
- FERRITE TOROID
- 1:1 TURNS RATIO FOR HIGH COUPLING

FOUR SEPARATE DRIVE CIRCUITS

- MOSFET TURN-ON CURRENT SHARING
- ELIMINATING PARASITIC OSCILLATIONS

UNITRODE UC3706 DRIVER CHIPS

- Ipeak = 1.5 AMPS
- SWITCHING SPEED

UNITRODE UC1825 PWM IC

CHARGER REGULATION CIRCUITS

CHARGE CURRENT REGULATION

- RESISTIVE CURRENT SENSING
  - * 25 mOHM IN SERIES WITH THE BATTERY
  - * ADVANTAGE : SIMPLICITY
  - * DISADVANTAGE : LOSSES
    - 10 A CHARGE = 2.5W LOSS
    - 20 A CHARGE = 10W LOSS
- ADJUSTABLE CHARGE CURRENT REFERENCE

BUS VOLTAGE REGULATION

- IMMEDIATELY AFTER ECLIPSE
- DURATION
- ERROR SIGNAL FROM MODE CONTROLLER (PCU)

CURRENT/VOLTAGE MODE SELECTION

- DIODE OR-ING CIRCUIT
- CHARGE CURRENT REFERENCE LEVEL
- MODE CONTROLLER THRESHOLDS

3. DISCUSSION

DISCUSSION

1) BATTERY CHARGING CURRENT
2) SOLAR ARRAY CHARACTERISTICS
3) BATTERY RIPPLE CURRENT SPEC
4) MINIMUM BATTERY VOLTAGE
5) BIDIRECTIONAL CONVERTER ??
6) APPRVED PARTS
7) SOLAR ARRAY SIMULATOR
8) MULTI-MODULE CHARGER ??
9) SERIES DIODES
10) V/T LIMIT