NASA-CR185127
21 August 1989

ADVANCED TECHNOLOGY SATELLITE DEMODULATOR DEVELOPMENT FINAL REPORT

Contract No. NAS3-24578

Prepared for:

NASA Lewis Research Center
21000 Brookpark Road
Cleveland, OH 44135

Prepared by:

Ford Aerospace Corporation
3825 Fabian Way
Palo Alto, CA 94303

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1.0 SUMMARY

Ford Aerospace has developed a proof-of-concept satellite 8PSK modulation and coding system operating in the TDMA mode at a data rate of 200 Mbps using rate 5/6 forward error correction coding. The 80 Msps 8PSK modem was developed in a mostly digital form and is amenable to an ASIC realization in the next phase of development. The codec was developed as a paper design only. The power efficiency goal was to be within 2 dB of theoretical at a BER of 5×10^{-7} while the measured implementation loss was 4.5 dB. The bandwidth efficiency goal was 2 bits/sec/Hz while the realized bandwidth efficiency was 1.8 bits/sec/Hz. The burst format used a preamble of only 40 8PSK symbol times including 32 symbols of all zeros and an eight symbol unique word.

The modem and associated special test equipment (STE) were fabricated mostly on a specially designed stitch-weld board although a few of the highest rate circuits were built on printed circuit cards. All the digital circuits were ECL to support the clock rates of from 80 MHz to 360 MHz. No attempt was made to miniaturize the 3.37 GHz i.f. circuits which were fabricated from commercially available connectorized parts. The complete modem and STE were rack mounted in a single seven foot 19 inch rack.

The transmitter and receiver matched filters were square-root Nyquist bandpass filters realized at the 3.37 GHz i.f. The modem operated as a coherent system although no analog phase locked (PLL) loop was employed. An open loop local oscillator left the modulation constellation spinning at the output of the quadrature detector where it was digitized by an eight bit ADC sampling at one sample per symbol and a digital PLL which acquired the carrier was used to despin the constellation. The instantaneous phase was computed by an arctangent table lookup of the addressing I and Q samples. The clock recovery was affected by phase locking the clock recovery PLL to the output of an envelope detector. No symbol transitions were included in the preamble solely for clock recovery since the clock recovery scheme exploited the phase continuity in the symbol clock to allow phase prediction of the clock phases between bursts.

STE had to be built to generate the burst format, modulate the the carrier with the 8PSK signal, filter the modulator output with the square root Nyquist response, and finally measure the BER on a burst basis. Additional STE generated the additive WGN and the adjacent and co-channel interferences.

The Nyquist filters proved to be the major technological problem in realizing the goal of 2 bits/sec/Hz bandwidth efficiency. The rolloff factor of 0.2 was too difficult to achieve and tests were performed with a rolloff factor of 0.4. We concluded that a SAW filter approach at a center frequency of about 280 MHz may allow achieving the 0.2 rolloff factor.

The excessive degradation from theoretical on long TDMA bursts was attributed to clock jitter and the intersymbol interference caused by the Nyquist filters. The phase predictor in the clock recovery circuit did not perform properly and we believe that this is the cause of the excessive degradation in BER with short TDMA bursts.

Within the budgetary constraints of the program, the Ford Aerospace approach to the demodulator has been proven and is eligible to proceed to the

next phase of development of a satellite demodulator engineering model. This would entail the development of an ASIC version of the digital portion of the demodulator, an MMIC version of the quadrature detector, and SAW Nyquist filters to realize the bandwidth efficiency.

2.0 INTRODUCTION

The objective of this program was to perform advanced modulation technology development (AMTD) which would significantly increase the bandwidth efficiency of TDMA uplink modulation systems while maintaining present system performance levels (i.e., the power and bandwidth efficiencies of QPSK). A proof-of-concept (POC) model of a satellite demodulator which exhibits the potential for low weight and power consumption was to be constructed to: (a) demonstrate technology feasibility, (b) help establish practical bandwidth efficiency limitations, and (c) provide the database for the design and development of engineering model demodulators.

An ultimate version of the POC model would be used in a communication satellite on-board processing payload. The advantages of such payloads over the conventional "bent-pipe" transponder have been well touted in the literature and will not be reexamined here. Only two such payloads are known and both are currently being built: ACTS for NASA and ITALSAT for the Government of Italy. Both of these systems utilize analog satellite demodulators, SMSK with a Viterbi algorithm decoder in a TDMA mode for ACTS and continuous QPSK uncoded for ITALSAT. Neither of these systems has the bandwidth or power efficiencies as high as the design goals for the demodulator reported here nor its degree of digital implementation.

The latter bears on the ability to achieve the ultimate in miniaturization through the use of application specific integrated circuits (ASIC). Only an all or mostly digital mechanization could achieve this which is the main significance of the Ford Aerospace approach to the design of the AMTD demodulator. Ford developed a preliminary concept of the modulation system including a forward error correction (FEC) codec, modem, and the special test equipment (STE). Subsequently, we designed, built, and tested the modem and STE. A single breadboard/POC model was constructed since sequential breadboard and POC model phases were not feasible given the program resources. For the same reason and by prior agreement, the FEC codec was developed only as a paper design.

The Ford POC concept was to employ 8PSK modulation filtered to 1.2 Hz/symbol/sec. In the POC model actually built and tested, it was necessary to relax the filtering to 1.4 Hz/symbol/sec because of the limited resources available for reiterating the Nyquist bandpass filters which had proved to be a significant technological issue. The program proceeded over a span of 40 months during which the POC model was built and tested. Within the budgetary constraints, we have proven the feasibility of the proposed approach and believe, therefore, that the next phase of development of an ASIC version can proceed with significantly lower risk.

To minimize the resources devoted to writing this final report, we have extensively referenced prior reports as well as previously prepared system documentation in which the theory and operation of some of the hardware has been discussed. Similarly, numerous appendices were used to minimize the

time and effort necessary in the compilation of a complete description of the testing. The codec work which was not performed on contract funds is Ford proprietary and is reported under a separate cover entitled "Coding Appendix".

3.0 CONCEPT AND DESIGN OF POC MODEL

In this section the AMTD concept as finally implemented and tested is described. The system requirements which were to be satisfied by the POC model are presented in Appendix A, AMTD MODULATION SYSTEM REQUIREMENTS. These requirements were originally presented in the SOW in the RFP for the AMTD program (reference 1) and were subsequently refined in stages, first in the FAC proposal (reference 2) and later in an independent research and development report(reference 3)

3.1 DESIGN OF MODULATION AND FILTERING

The main requirement, that the bandwidth efficiency of the system be greater than 2 bits/s/Hz leads immediately to a system with the number of modulation states greater than four, namely eight or sixteen. Since the system is specified for bandwidth efficiency, the transmitted waveform must be filtered and cannot be a "wideband" waveform using a rectangular shaped baseband pulse which would lead to an integrate and dump type receiver. Since the power efficiency is specified to be within 2 dB of theoretical, the filtering of the waveform must minimize intersymbol interference (ISI) and, therefore, the modulating pulse must satisfy the Nyquist theorem for vestigial symmetry of the transmittance function. This leads to the use of a family of well known (but unrealizable) raised cosine filter functions characterized by a rolloff factor, α. The rolloff factor ranges from 1 for a bell shaped frequency response with no flat portion to a rolloff of zero for the "brick-wall" function. In an idealized system using Nyquist filtering consisting of perfectly packed adjacent channels with no spectral overlap, the bandwidth occupied per channel, B, is defined by

$$B=(1+\alpha)f_s \tag{3-1}$$

where f_s is the symbol rate emanating from the modulator. For a modulator which accepts binary data at rate R_d from its source and maps this data into M (a power of 2) possible channel waveforms, f_s is then defined as

$$f_s = \frac{R_d}{\log_2 M} \tag{3-2}$$

If the channel data rate, R_d is the result of source encoding a raw data stream at bit rate R_b through an encoder of coding rate R_c, we have that

$$R_d = \frac{R_b}{R_c} \tag{3-3}$$

The bandwidth efficiency, η defined as $\frac{R_b}{B}$ is determined to be

$$\eta = \frac{R_b}{B} = \frac{R_c \log_2 M}{(1+\alpha)} \quad \text{bits/sec/Hz} \qquad (3\text{-}4)$$

by manipulating equations (3-1) through (3-3). Clearly since $\eta>2$, M must be larger than 4, i.e., a higher level modulation than QPSK or 4QAM. It was shown in tradeoffs available in standard references that the required maximum of 1 dB degradation from theoretical with -20 dB CCI would require forward error correction (FEC) coding to be applied to meet that specification. Employing the Tanner rate 5/6 block code with 8PSK was shown by simulation to meet the "less than 1 dB degradation" specification (see Coding Appendix). With R_C = 5/6 in equation (3-4), the bandwidth efficiency specification will be satisfied with α = 0.2. In such a system, the coded data rate is 240 Mbps, the channel symbol rate is 80 Msps and, from (3-1), B = 96 MHz.

The bandwidth efficiency of the POC system with α=0.2 but without coding is calculated from (3.4) to be 2.5 bits/sec/Hz and with coding is 2.05 bits/sec/Hz.

The TDMA burst structure was specified in reference 1. The specification that the "maximum time to acquire synchronization shall be 100 bit times" was taken to be the maximum length of the burst preamble at the maximum data rate of 200 Mbps or 500 ns. Similarly, the specification that "the maximum unique word length used to indicate the start of valid data in real time shall be 20 bit times" (100 ns) is taken to require that the maximum unique word (UW) length is (100 ns)/(12.5 ns/symbol) = 8 symbol times and the balance of the preamble is taken to be an unmodulated carrier burst equal to (400 ns)/(12.5 ns/symbol)= 32 symbols in length which will force acquisition of the carrier recovery loop prior to the arrival of the UW. No clock loop locking pattern (except for the UW) is provided since a running clock phase estimate is updated each burst as well as between bursts such that no significant clock phase error accumulates once a particular access is initially acquired. A test frame and burst structure with two accesses is shown in Figure 3-1.

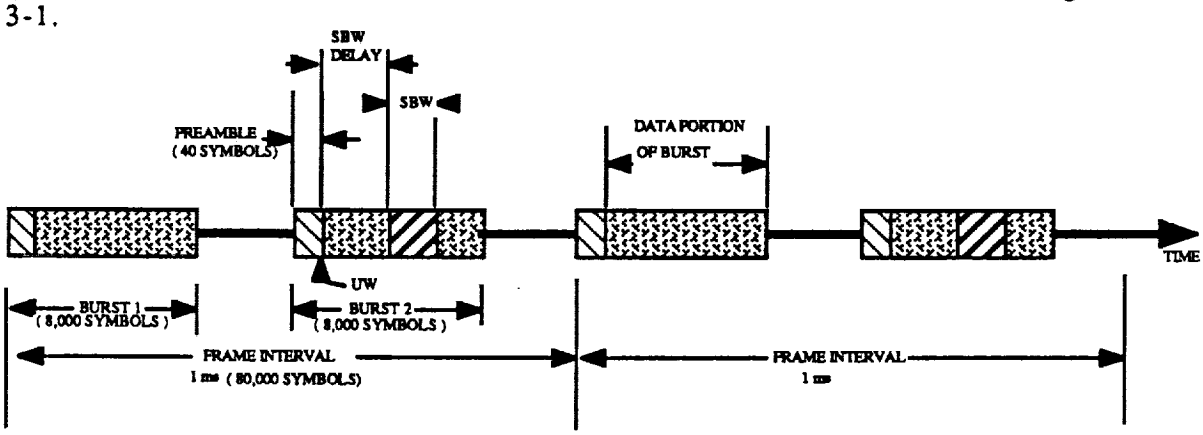


FIGURE 3-1 FRAME AND BURST STRUCTURE

The code used for the UW is discussed in detail in reference 4. It is an eight bit Neuman-Hofman code utilizing BPSK for maximum noise immunity.

3.2 DESIGN OF PROOF-OF-CONCEPT MODEL

The POC model was planned, built, and tested without the FEC codec due to budgetary constraints (reference 5). The system performance with the codec will have to be inferred from the modem performance without coding.

3.2.1 BURST GENERATOR

The burst generator generates serial pseudorandom data at a clock rate of 240 MHz using an 11 stage linear feedback shift register generator (LFSRG). The LFSRG starts up immediately after the burst generator completes the preamble consisting of the 32 "all zeros" symbols and UW code. The serial data stream out of the burst generator is converted to parallel words of 3 bits and applied to the 8PSK modulator shown in Figure 3-2. The operation and specification of the burst generators are covered in detail in reference 6.

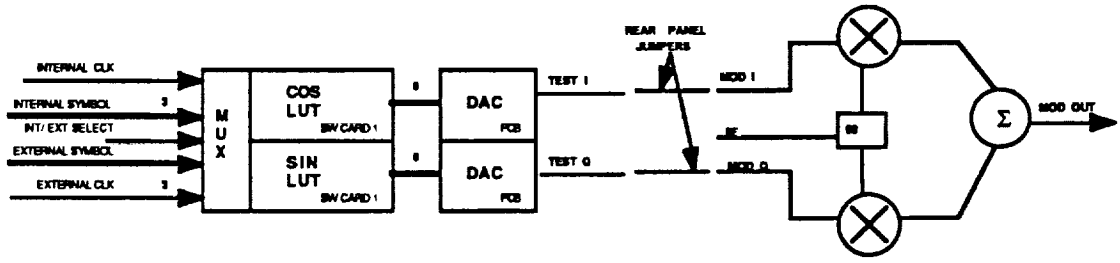


Figure 3-2 8PSK MODULATOR

3.2.2 MODULATOR

For the purposes of testing the system without a codec, the modulation states are mapped as a Gray code from the input data as shown in Figure 3-3. This ensures that when the modulator makes the most probable error (i.e., to a phase adjacent to the correct one) only a single bit error results. The operation and specification of the modulators are covered in detail in reference 7.

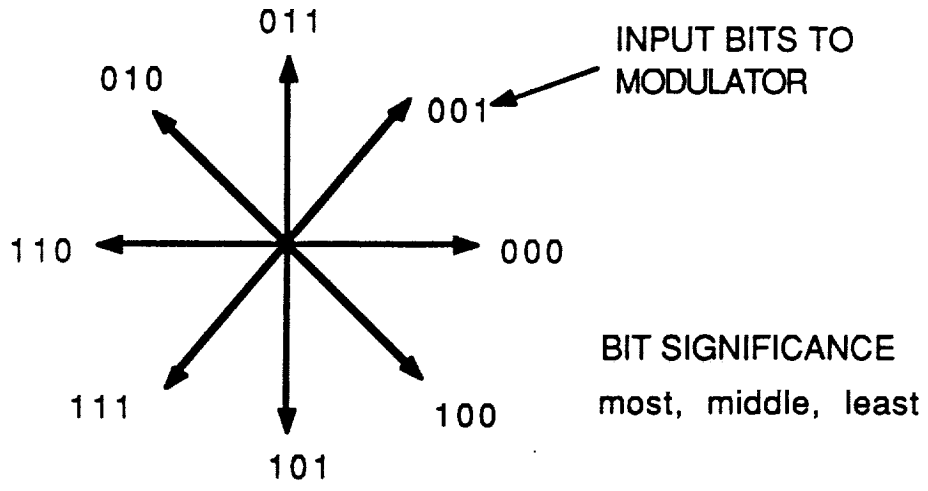


FIGURE 3-3 GRAY CODING ON 8PSK

3.2.3 FILTERING

Following the modulator is the transmitter r.f. filter centered at 3.37 GHz with frequency response of a cascade of a square-root Nyquist with rolloff factor of 0.4 and an inverse sinc equalizer . The transmitter filter is within the Interference and Noise Test Set where noise, and (on a selectable basis) CCI and/or ACI is added to the signal. The traveling wave amplifier input and output connections are located on this unit and the filtered signal can be passed through the TWTA to simulate the ground based transmitter effects of AM/AM and AM/PM conversion. The receiver matched filter is also mounted within the Interference and Noise Generator.

3.2.3.1 FILTER FUNCTIONAL DESIGN

To achieve the matched filter performance, it is well known that the receiver filter must be a "conjugate match" to the transmitted waveform and the received waveform, after passing through the receiver filter, needs to be sampled at the peak of the response. To fulfill the Nyquist ISI free criterion, the overall system response (i.e., the cascade of the transmitter and receiver) must have the "vestigial symmetry" property. One family of filters which has this characteristic is the raised cosine filter with frequency response given by (3-5).

$$H(f) = \begin{cases} 1 & 0 \le f \le \frac{(1-\alpha)}{2T_s} \\ \cos^2\left\{\frac{\pi T_s}{2\alpha}\left(f - \frac{(1-\alpha)}{2T_s}\right)\right\} & \frac{(1-\alpha)}{2T_s} \le f \le \frac{(1+\alpha)}{2T_s} \\ 0 & f \ge \frac{(1+\alpha)}{2T_s} \end{cases} \quad (3\text{-}5)$$

where T_s is the symbol time, and a is the filter rolloff factor. The above filter is of course unrealizable since its bandwidth is limited, Another characteristic of interest is that it has linear phase versus frequency hence no group delay distortion. If we have a modulator which can output delta functions into the transmitter filter, the transmitter and receiver filters will be identical and the frequency responses of each will be given by the square root of equation (3-5). If a modulator were used which inputs a rectangular pulse into the transmitter filter (as almost all modulators do), the mismatch of the resulting waveform with the receiver matched filter would result in an attendant degradation in BER performance. The usual procedure to avoid this loss is to cascade the transmitter filter with an "inverse sinc equalizer" which is a filter having the reciprocal of the $\frac{\sin(x)}{x}$ Fourier transform of the rectangular pulse emanating from the modulator. Applying this equalization to the transmitter filter, $H(f)_{xmt}$, the transmitter and receiver filter transfer functions can be written respectively as

$$H(f)_{xmt} = \begin{cases} \frac{\pi f T_s}{\sin \pi f T_s} & 0 \le f \le \frac{(1-\alpha)}{2T_s} \\ \frac{\pi f T_s}{\sin \pi f T_s} \cos\left\{\frac{\pi T_s}{2\alpha}\left(f - \frac{(1-\alpha)}{2T_s}\right)\right\} & \frac{(1-\alpha)}{2T_s} \le f \le \frac{(1+\alpha)}{2T_s} \\ 0 & f \ge \frac{(1+\alpha)}{2T_s} \end{cases} \quad (3.\text{-}6)$$

and

$$H(f)_{rec} = \begin{cases} 1 & 0 \le f \le \frac{(1-\alpha)}{2T_s} \\ \cos\left\{\frac{\pi T_s}{2\alpha}\left(f - \frac{(1-\alpha)}{2T_s}\right)\right\} & \frac{(1-\alpha)}{2T_s} \le f \le \frac{(1+\alpha)}{2T_s} \\ 0 & f \ge \frac{(1+\alpha)}{2T_s} \end{cases} \quad (3\text{-}7)$$

The transfer functions given by (3-5) through (3-7) are shown in Figure 3-4 below for the case of α=0.4 The curve labeled WO/EQ is equation (3-5) and the curve labeled W/EQ is the cascade of equations (3-6) and (3-7). Note that the for equal amplitude adjacent channel signals spaced by 96 MHz, the spectra will cross over at about -8.5 dB. The ACI performance of this filter cannot approach that of the originally planned filter with α=0.2 which had infinite loss at half the ACI spacing frequency.

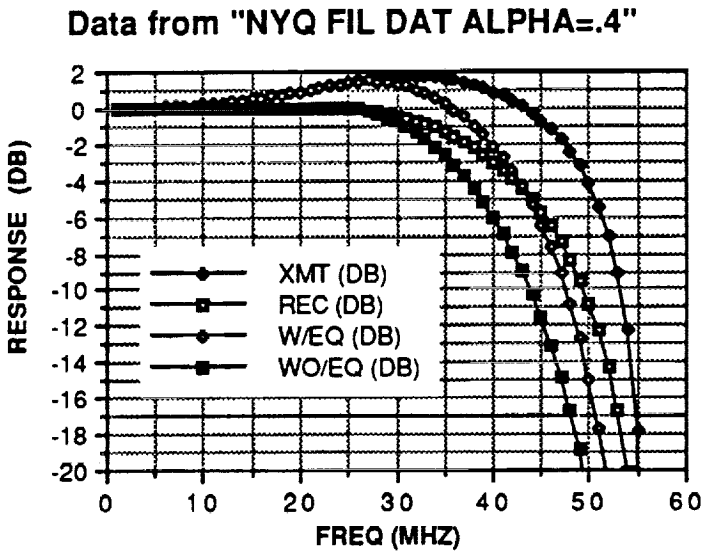


Figure 3-4 Responses of Nyquist Filters for α= 0.4 and T_S=12.5 ns

3.2.3.2 FILTER ELECTRICAL DESIGN

The electrical design of the filters for the AMTD modem is based on the Nyquist criterion for ISI free sampling. Since a perfect brick wall filter is not realizable, a skew symmetric function is added to the filter bandedge as required by Nyquist in order to achieve a finite steepness. A commonly used, and physically realizable shape is based on a raised cosine function, shown above. By varying the function, various filter rolloffs can be obtained, limited only by the frequency spacing between any adjacent channels. In the case of AMTD, the channels are spaced 96 MHz apart. Thus, in order to achieve at least 36 dB adjacent channel rejection , a 20% rolloff filter is needed.

Pole and zero locations for a number of different raised cosine filters have been previously tabulated (reference 8). To translate these into a physically realizable structure, in this case a coupled cavity configuration, a known filter circuit similar to the desired one was optimized to match the desired response precisely. Since there is both a transmit and receive filter, a square root raised cosine filter was used for each in order to achieve a cascaded function equal to the desired full raised cosine response. Figure 3-5 shows the ideal pole zero locations along with the optimized 9 pole M matrix circuit. The M values correspond to normalized mutual inductances between unit series capacitors. M values on the diagonal (i.e. m1,1) have the effect of frequency tuning each individual resonance used to partially compensate for the effect of the lowpass to bandpass mapping (to 3.373056GHz). The filter exhibits 9 poles with 4 finite imaginary zeroes.

Since steeply sloped filters inherently correspond to rapid phase variations, the group delay response of the optimized filter does not meet the requirement for linear phase of the ideal Nyquist filter. As a result, an all pass group delay equalizer is added to the filter. The M matrix for the equalizer was obtained in a similar fashion to that of the filter and is shown in Figure 3-6. The 6 poles required for the equalizer is probably minimal for the 8 PSK signal. The equalizer was split into 2 and 4 pole equalizers for better tunability.

Since the chosen modulation utilizes rectangular pulses, in addition to the filters there is a x/sin(x) equalizer required. This was electrically realized using a 2 pole Chebychev filter with 6.7 dB ripple along with a 2 pole delay equalizer. The M matrices for these two devices are shown in Figure 3-7. This equalizer was added to the transmit filter side.

Figures 3-8 and 3-9 show the magnitude response of the approximated 20% rolloff filters versus the ideal response.

3.2.3.3 FILTER MECHANICAL DESIGN

The mechanical design of the filters use patented, dielectrically loaded cylindrical cavities sized below cutoff. This configuration has been used on several satellite contracts by Ford Aerospace and offers very low size and weight along with high Q factors as compared with conventional microwave filter designs (see reference 9). The hybrid dielectric resonator mode used results in two modes per cavity. Figure 3-10 shows the mechanical configuration of one of the 9 pole filters.

The 9 pole square root Nyquist filters were realized using 5 physical cavities each, 4 using two modes and 1 using a single mode. Isolators were used on both input and output. The delay equalizers were realized using shorted cavities coupled by circulators. The equalizer response is thus determined by its reflected power. The x/sin(x) equalizer was realized in a similar fashion. The overall circuit is shown in Figure 3-11 Each rectangular cavity represents a cavity loaded with a dielectric resonator disc.

3.2.3.4 FILTER TUNING AND TESTING

The filters were tuned by empirically adjusting the resonator sizes and iris dimensions. A proprietary method allowed simple characterization of the iris bandwidths. The filters, due to their shaped amplitude responses, proved difficult to tune. Normally, filters are tuned by their return loss, so that when all the poles are visible and the return loss is adequate the tuning is completed. However, the 9 pole filters had to be tuned for a particular shape by degrading the return loss. Eventually a response reasonably similar to that desired was obtained. The delay equalizers and the x/sin(x) equalizer was relatively straightforward, although the delay requirements were quite stringent.

A particular problem with this type of design is that the delay equalizer amplitude response tends to be somewhat unpredictable due to the imperfect nature of the circulators. As a result, unwanted amplitude ripples often appear, especially if the equalizer order is high. Figures 3-12a through 3-13c show the amplitude and group delay performance of the 20% rolloff filters.

3.2.3.5 ALTERNATE 40% ROLLOFF FILTERS

The 20 % rolloff filters proved to be troublesome in practice due to mechanical difficulties and produced what was perceived to be high ISI when tested in the demodulator. Of particular trouble was temperature instability of the delay equalizers. As a result, alternate filters were built exhibiting a 40% rolloff characteristic. Simplifications resulting from this change included use of 8 pole filters (especially important due to symmetry) and 4 pole delay equalizers. Figures 3-14 through 3-16 shows the M matrices for the new filters. Figures 3-17 and 3-18 show the approximated 40% rolloff response versus the ideal response. In addition, some small mechanical changes improved the sensitivity of the filter to temperature and vibration. It should be noted that these filters were constructed from off the shelf parts; if manufactured for a spacecraft they typically have excellent mechanical characteristics. Figures 3-19a through 3-20b show the amplitude and group delay performance of the 40% rolloff filters. The 40% filters were those used in the delivered POC Model.

Design Data for 20% Square Root Raised Cosine Rolloff Filter

Pole Locations

Real	Imaginary
-0.5119	0
-0.4104	±.5007
-0.1984	±.8855
-0.111	±1.0738
-0.0291	±1.1677

Zero Locations

Real	Imaginary
0	±1.2052
0	±1.2990

Coupled Cavity Matrix BW=80 MHZ

Cavity	1	2	3	4	5	6	7	8	9
1	0.01493	1.1113	0	0	0	0	0	0	0
2	1.1113	0.01493	0.71619	0	-0.3138	0	0	0	0
3	0	0.71619	0.01493	0.85246	0	0	0	0	0
4	0	0	0.85246	0.01493	0.40262	0	-0.0021	0	0
5	0	-0.3138	0	0.40262	0.01493	0.51138	0	0	0
6	0	0	0	0	0.51138	0.01493	0.46741	0	-0.3796
7	0	0	0	-0.0021	0	0.46741	0.01493	0.90547	0
8	0	0	0	0	0	0	0.90547	0.01493	0.83368
9	0	0	0	0	0	-0.3796	0	0.83368	0.01493

Input Transformer 1.24879
Output Transformer 1.1707

Figure 3-5 Pole, Zero Locations and Circuit Matrix for 20% Rolloff Filter

Design Data for 20% Square Root Raised Cosine Rolloff Equalizer

Pole Locations

Real	Imaginary
±.3387	±.1640
±.3490	±.4881
±.3226	±.7629

Realized Using 4 pole and 2 pole Equalizers

Coupled Cavity Matrix BW=80 MHZ

4 Pole Equalizer

Cavity	1	2	3	4
1	0	0.7942	0	0
2	0.7942	0	0.4115	0
3	0	0.4115	0	0.2639
4	0	0	0.2639	0

Input Transformer 1.2363

2 Pole Equalizer

Cavity	1	2
1	0	0.8175
2	0.8175	0

Input Transformer 0.6328

Figure 3-6 Pole Locations and Circuit Matrices for 20% Rolloff Equalizer

Design Data for 20% Sinc Equalizer

Realized Using 2 Pole Filter and 2 Pole Equalizer

Coupled Cavity Matrix BW=80 MHZ

2 Pole Filter

Cavity	1	2
1	0	0.3519
2	0.3519	0

Input Transformer 0.07782

2 Pole Equalizer

Cavity	1	2
1	0	0.2849
2	0.2849	0

Input Transformer 0.4977

Figure 3-7 Circuit Matrices for 20% Rolloff Sinc Equalizer

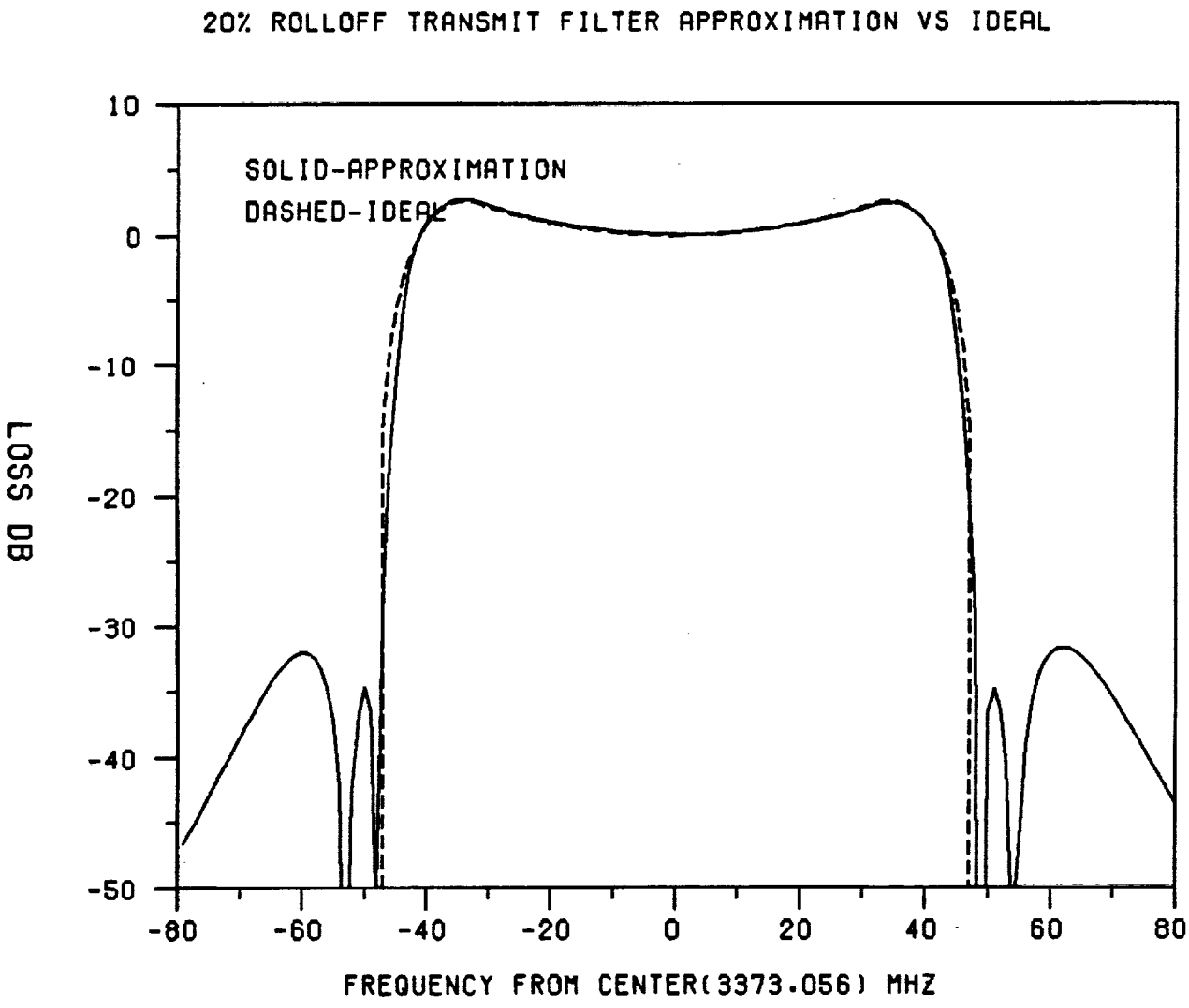


Figure 3-8 Comparison of 20% Rolloff Transmit Filter Approximation vs Ideal Responses

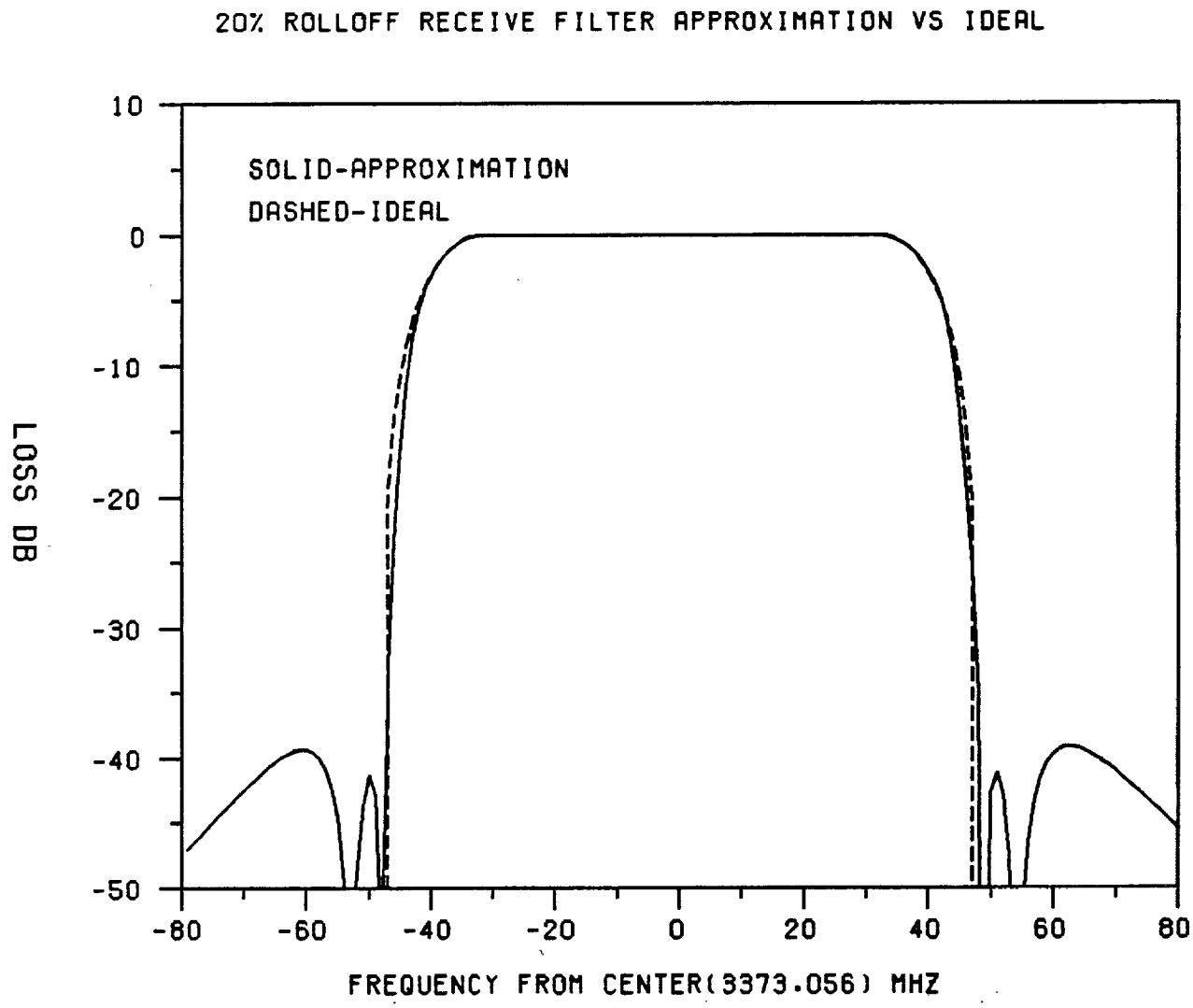


Figure 3-9 Comparison of 20% Rolloff Receive Filter Approximation vs Ideal Responses

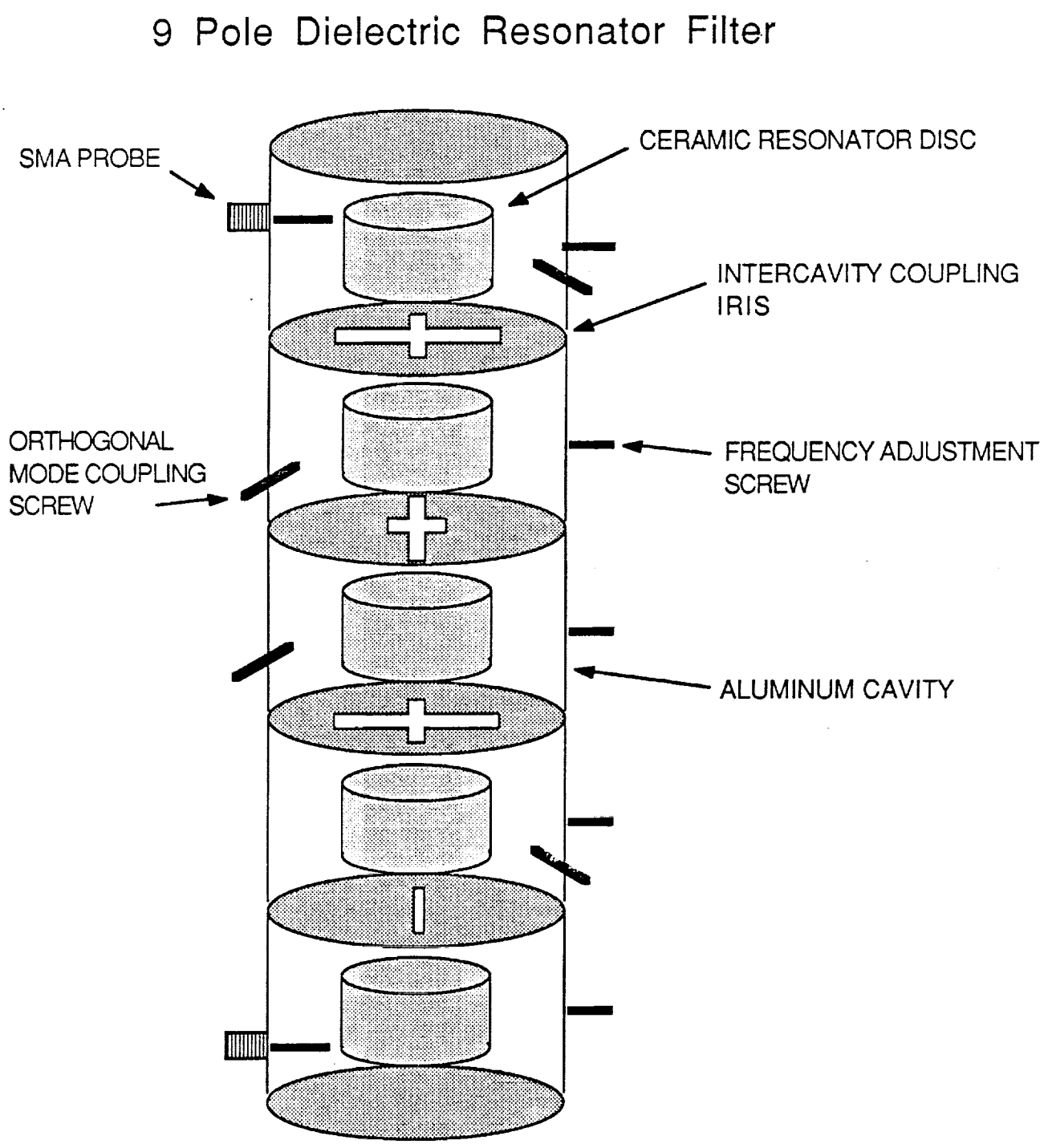


Figure 3-10 Mechanical Configuration of 20% Rolloff 9 Pole Filter

Block Diagram of 20% Rolloff Filter

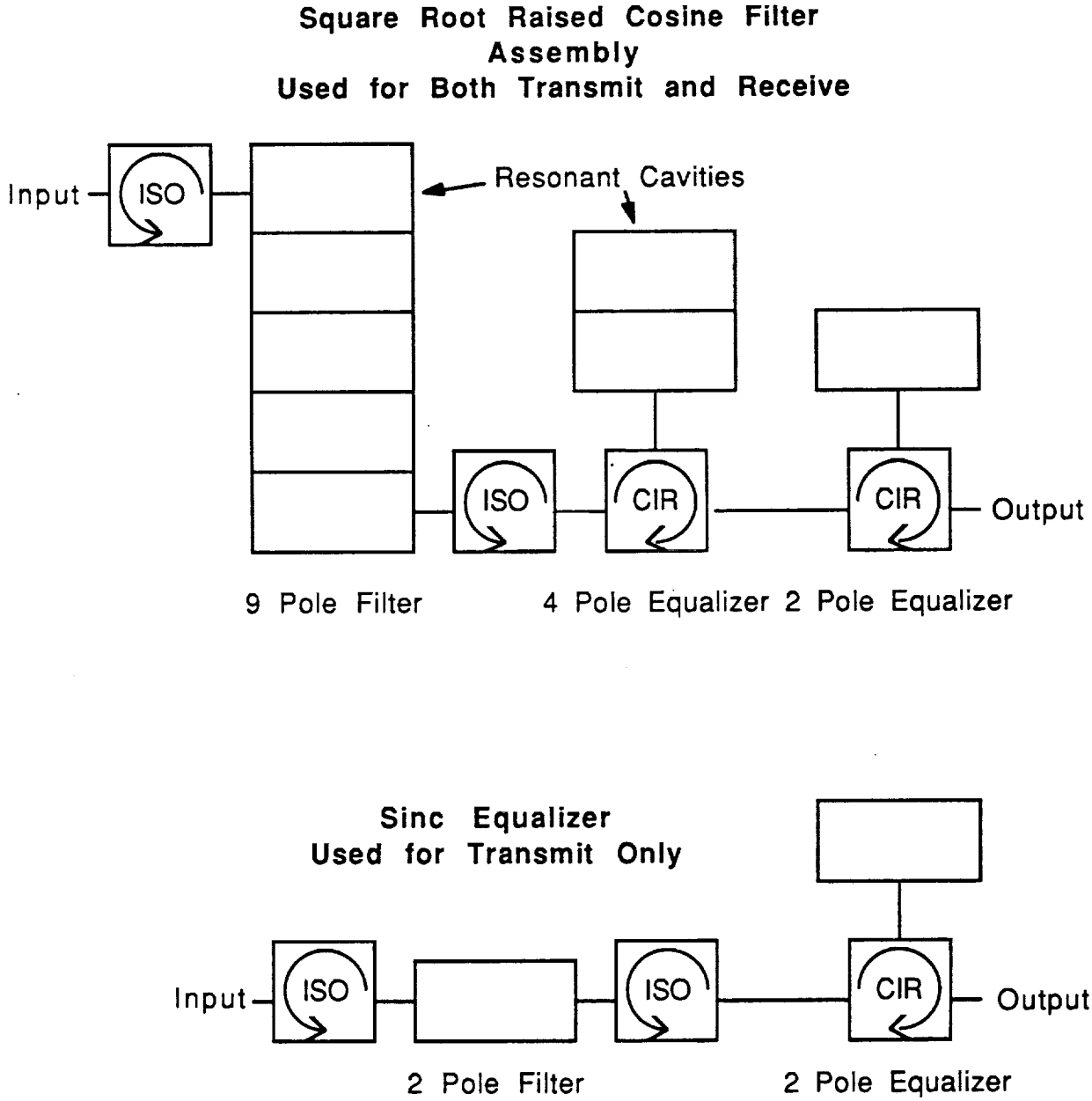


Figure 3-11 Overall 20% Rolloff Circuit

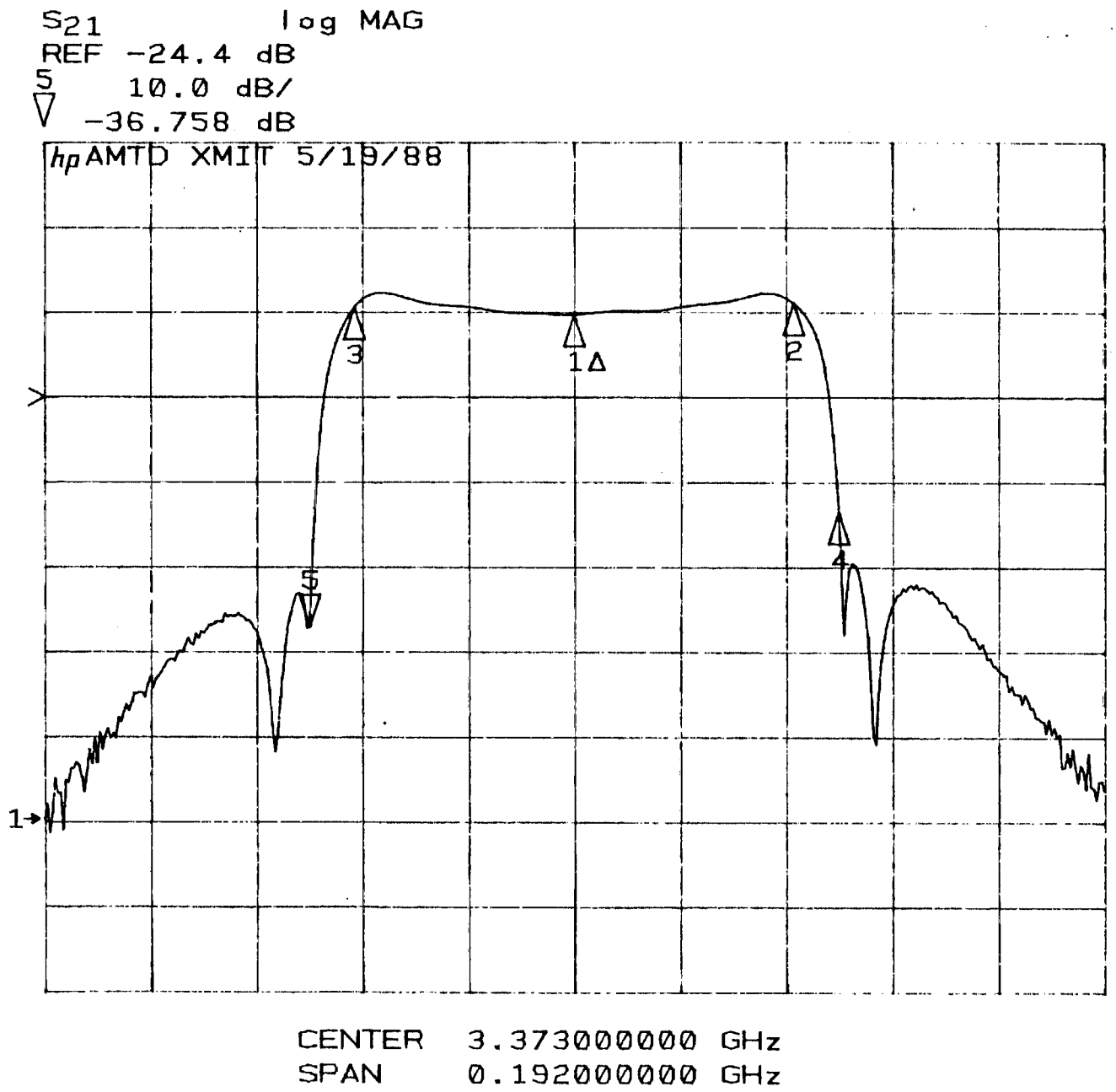


Figure 3-12a Wideband Magnitude Response of 20% Rolloff Transmit Filter

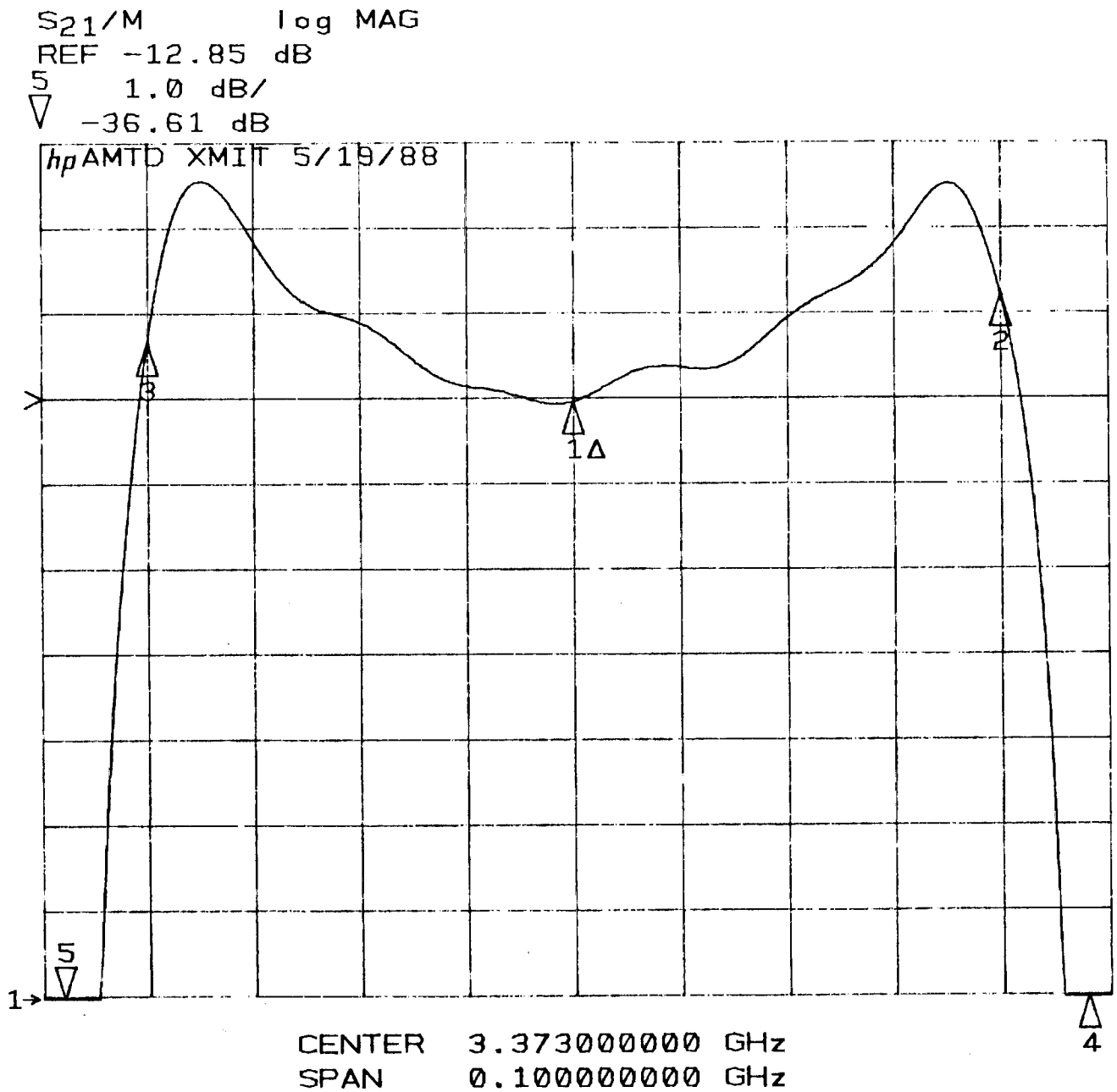


Figure 3-12b Narrowband Magnitude Response of 20% Rolloff Transmit

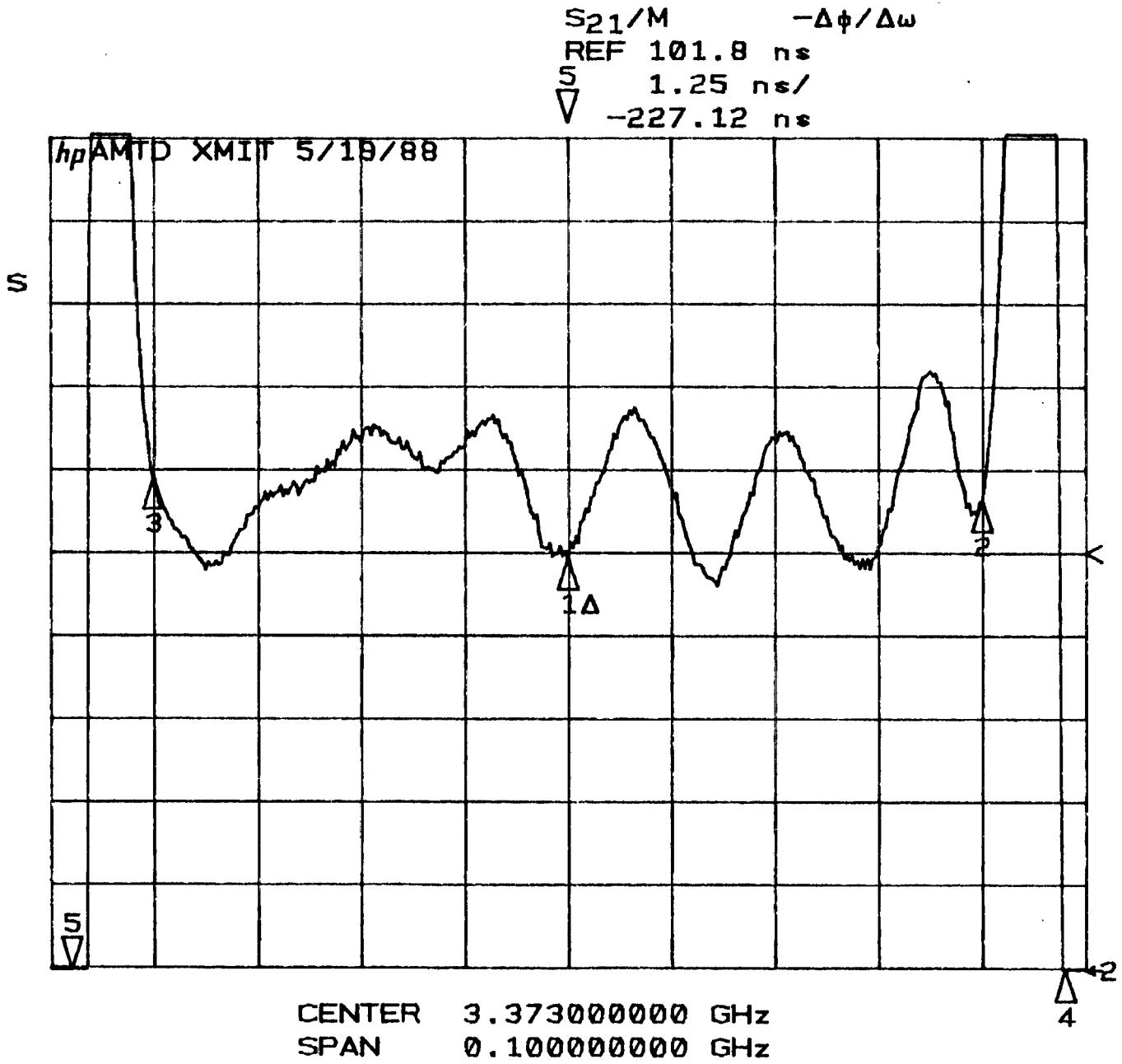


Figure 3-12c Narrowband Group Delay Response of 20% Rolloff Transmit Filter

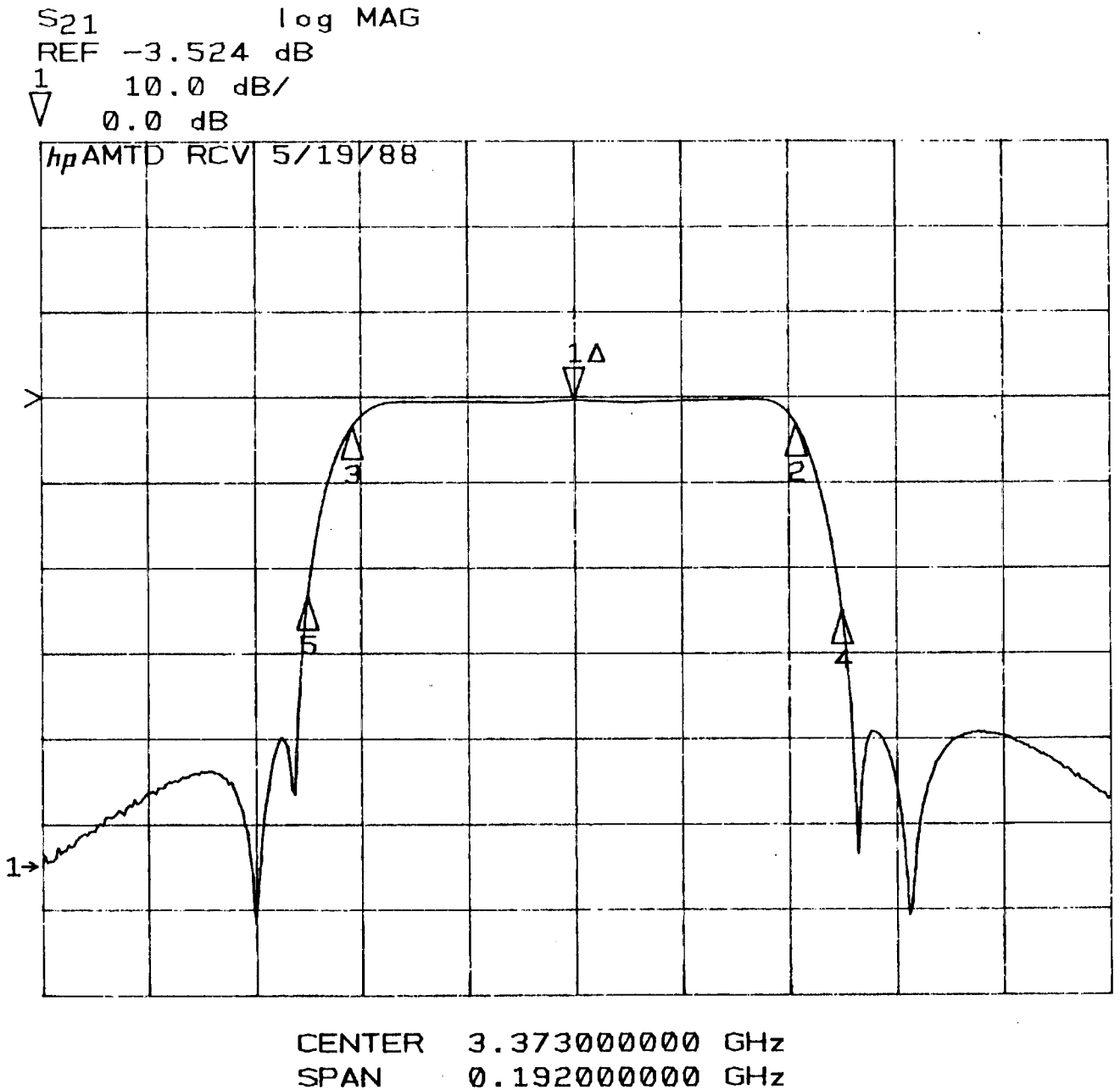


Figure 3-13a Wideband Magnitude Response of 20% Rolloff Receive Filter

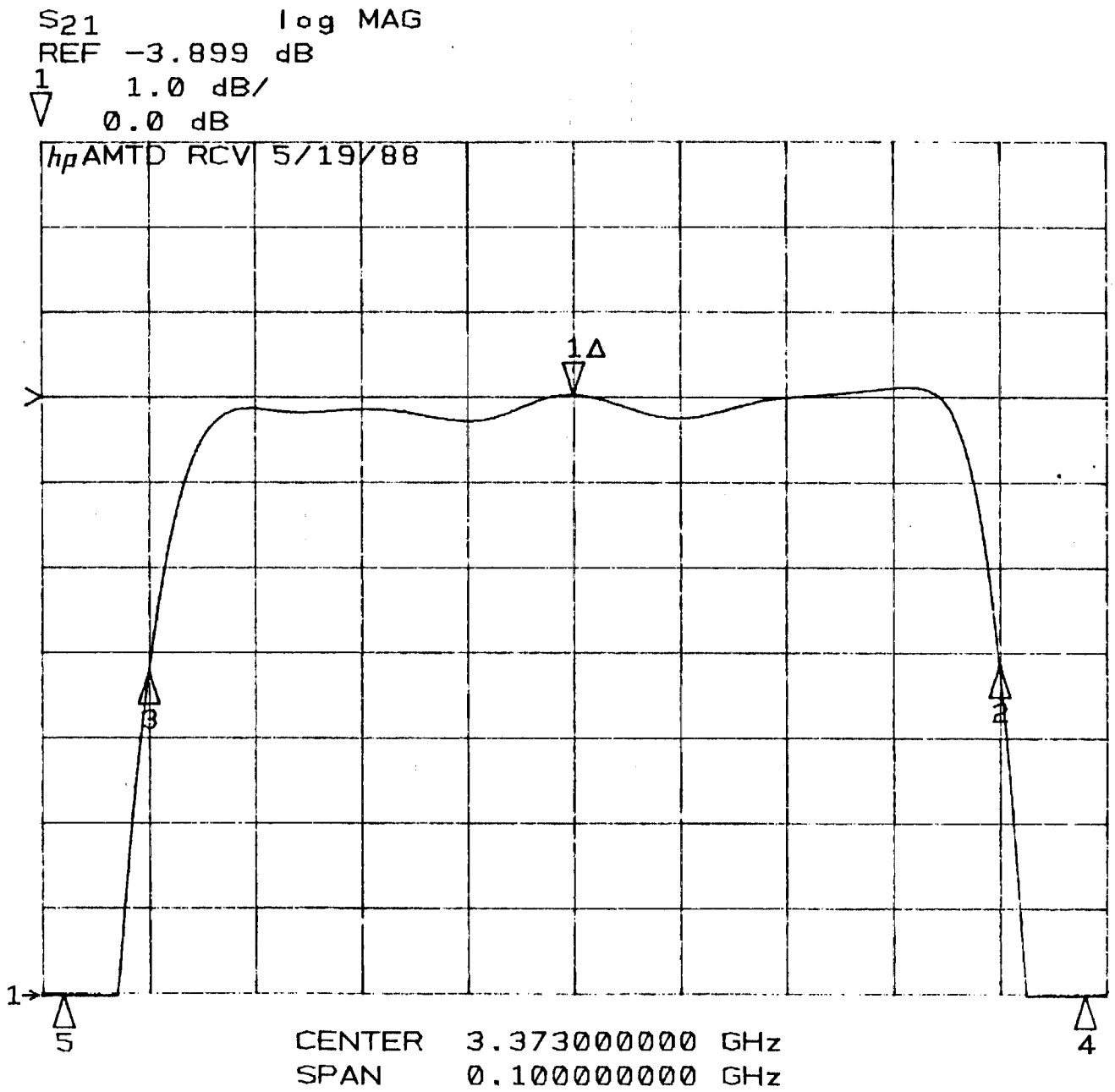


Figure 3-13b Narrowband Magnitude Response of 20% Rolloff Receive

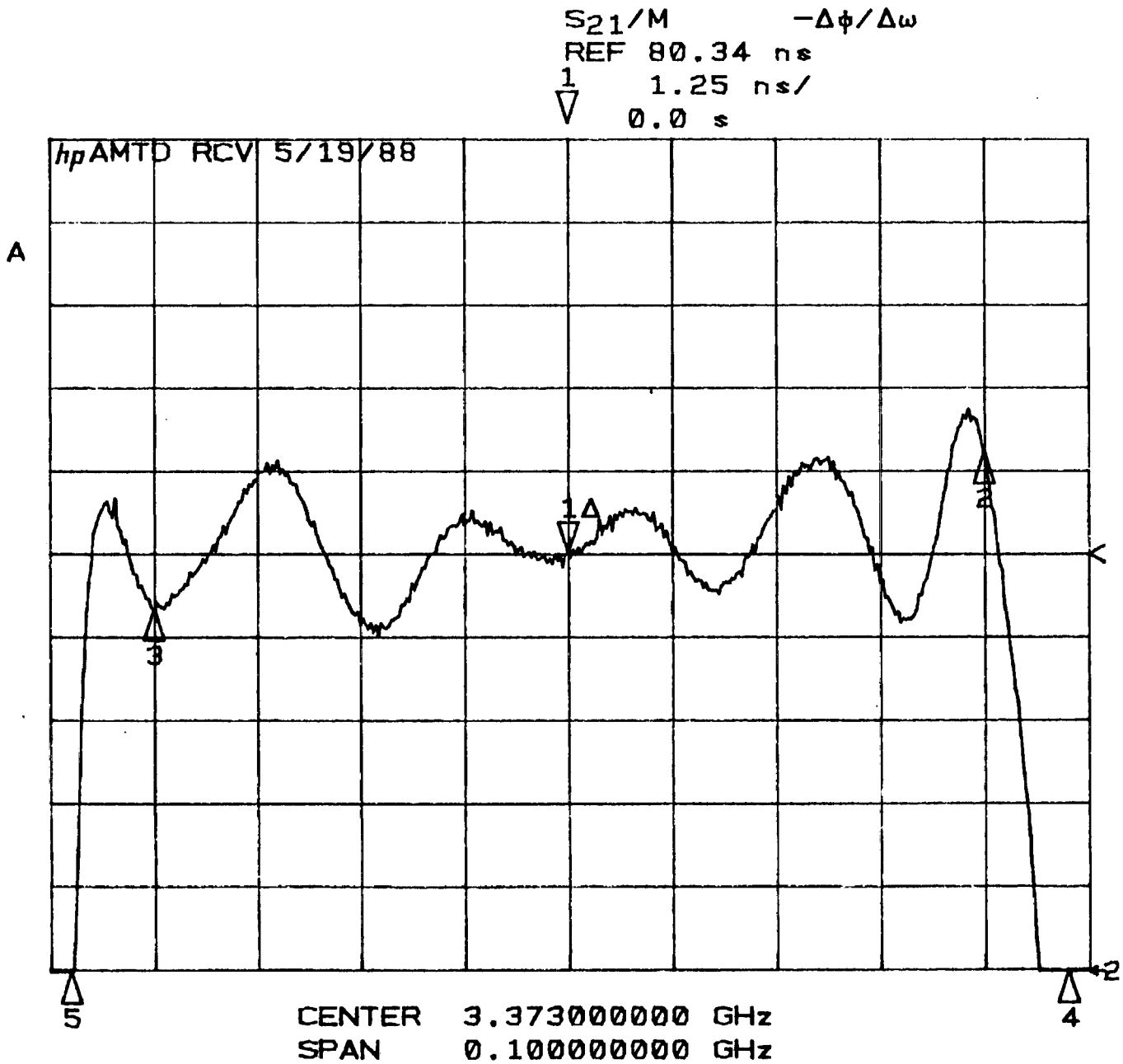


Figure 3-13c Narrowband Group Delay Response of 20% Rolloff Receive

Design Data for 40% Square Root Raised Cosine Rolloff Filter

Pole Locations

Real	Imaginary
-0.5118	±.3326
-0.3095	±.8394
-0.1687	±1.1806
-0.0438	±1.3479

Zero Locations

Real	Imaginary
0	±1.4100
0	±1.5692

Coupled Cavity Matrix BW=80 MHZ

Cavity	1	2	3	4	5	6	7	8
1	0.0176	1.0828	0	-0.4089	0	0	0	0
2	1.0828	0.0176	1.0563	0	0	0	0	0
3	0	1.0563	0.0176	0.4444	0	-0.0073	0	0
4	-0.4089	0	0.4444	0.0176	0.5083	0	0	0
5	0	0	0	0.5083	0.0176	0.4444	0	-0.4089
6	0	0	-0.0073	0	0.4444	0.0176	1.0563	0
7	0	0	0	0	0	1.0563	0.0176	1.0828
8	0	0	0	0	-0.4089	0	1.0828	0.0176

Input Transformer 1.556:1
Output Transformer 1.556:1

Figure 3-14 Pole, Zero Locations and Circuit Matrix for 40% Rolloff Filter

Design Data for 40% Square Root Raised Cosine Rolloff Equalizer

Pole Locations for Required Delay

Real	Imaginary
±.5507	0
±.5334	±.5885

4 Pole Equalizer Used to Improve Delay Performance

Coupled Cavity Matrix BW=80 MHZ

Cavity	1	2	3	4
1	0	1.2134	0	0
2	1.2134	0	0.6211	0
3	0	0.6211	0	0.4004
4	0	0	0.4004	0

Input Transformer 1.9145

Figure 3-15 Pole Locations and Circuit Matrices for 40% Rolloff Equalizer

Design Data for 40% Sinc Equalizer

Realized Using 2 Pole Filter and 2 Pole Equalizer

Coupled Cavity Matrix BW=80 MHZ

2 Pole Filter

Cavity	1	2
1	0	0.3276
2	0.3276	0

Input Transformer= 0.05317

2 Pole Equalizer

Cavity	1	2
1	0	0.2404
2	0.2404	0

Input Transformer= 0.4233

Figure 3-16 Circuit Matrices for 40% Rolloff Sinc Equalizer

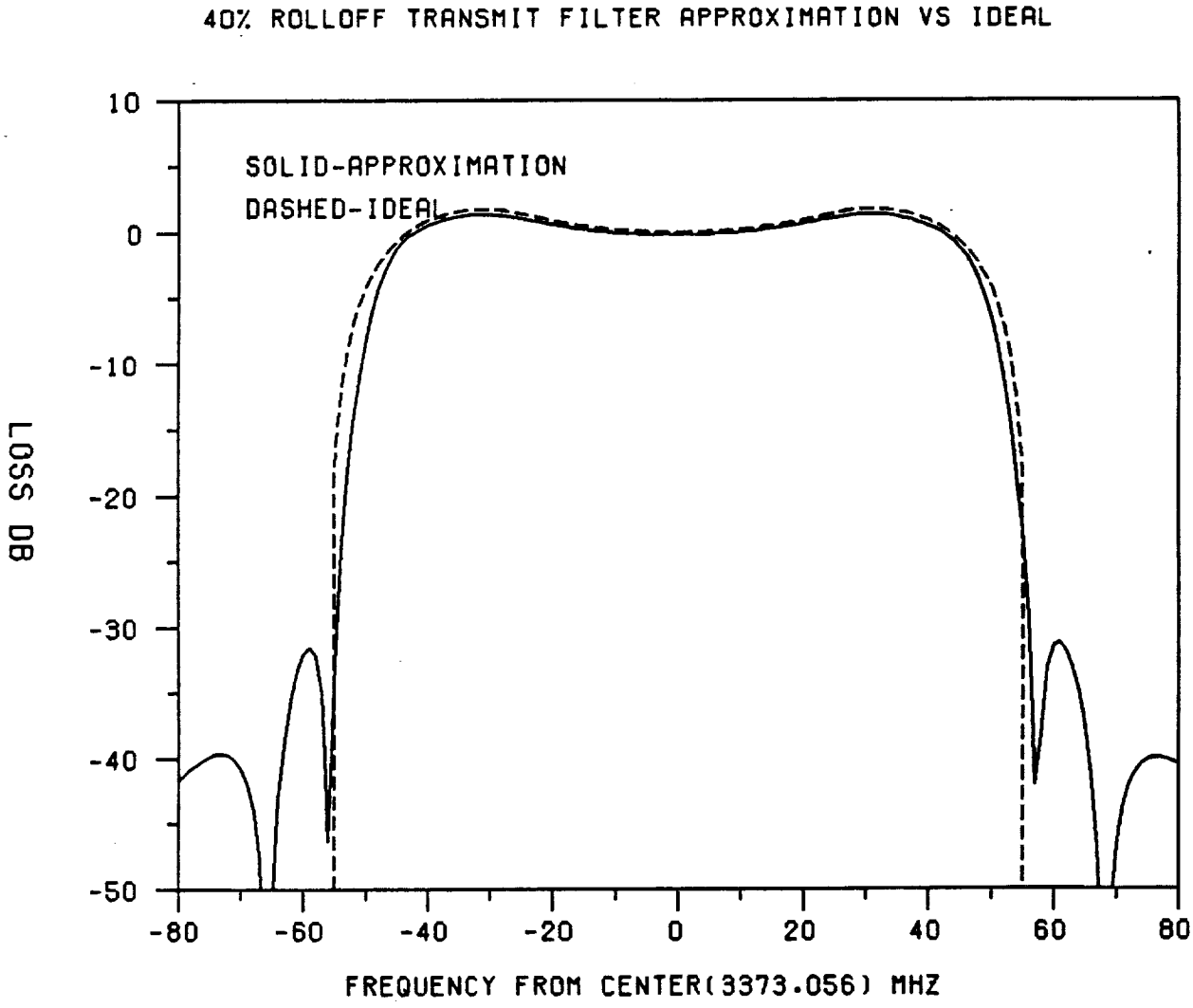


Figure 3-17 Comparison of 40% Rolloff Transmit Filter Approximation vs Ideal Responses

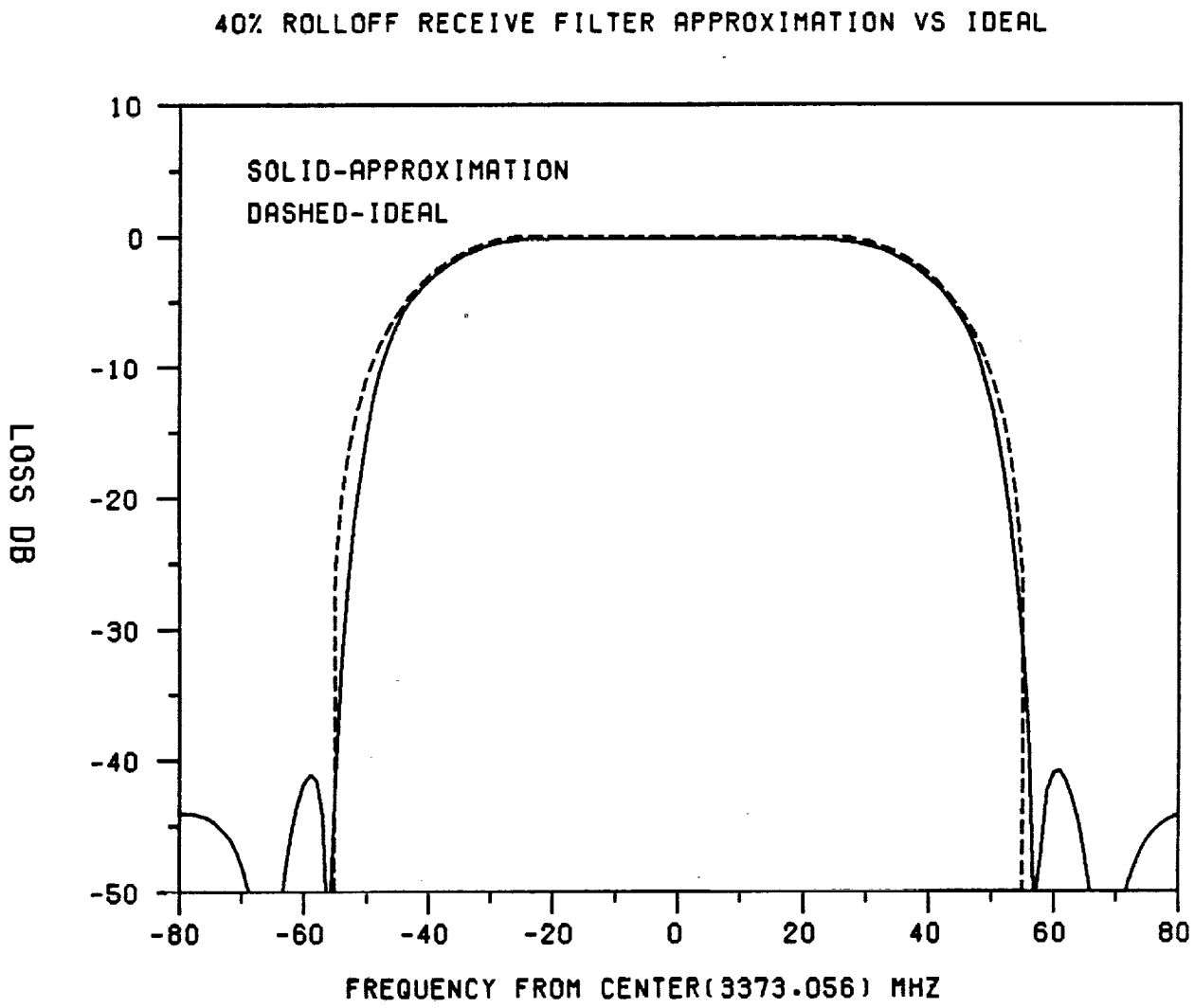


Figure 3-18 Comparison of 40% Rolloff Receive Filter Approximation vs Ideal Responses

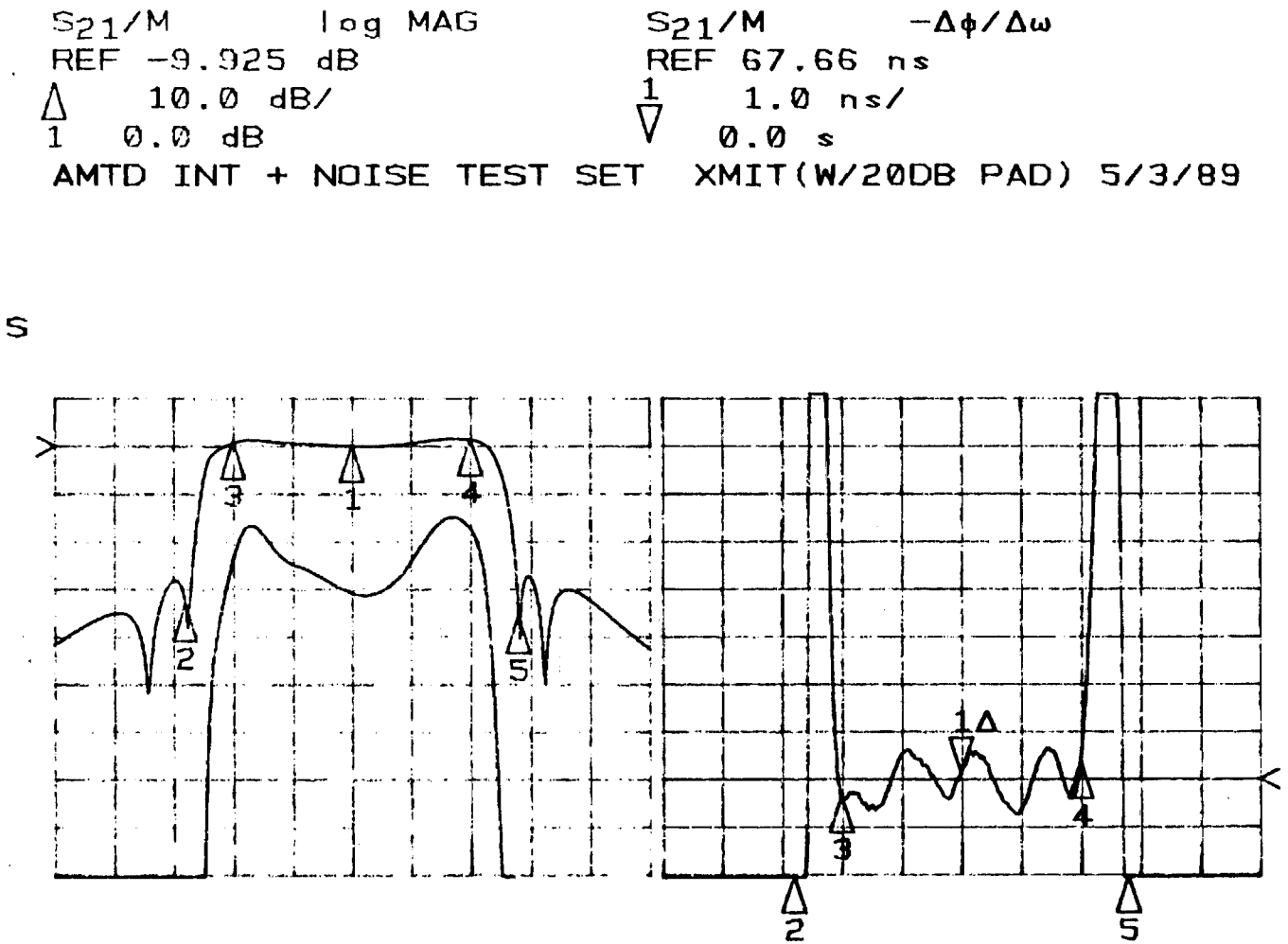


Figure 3-19a Wideband Magnitude Response of 40% Rolloff Transmit Filter

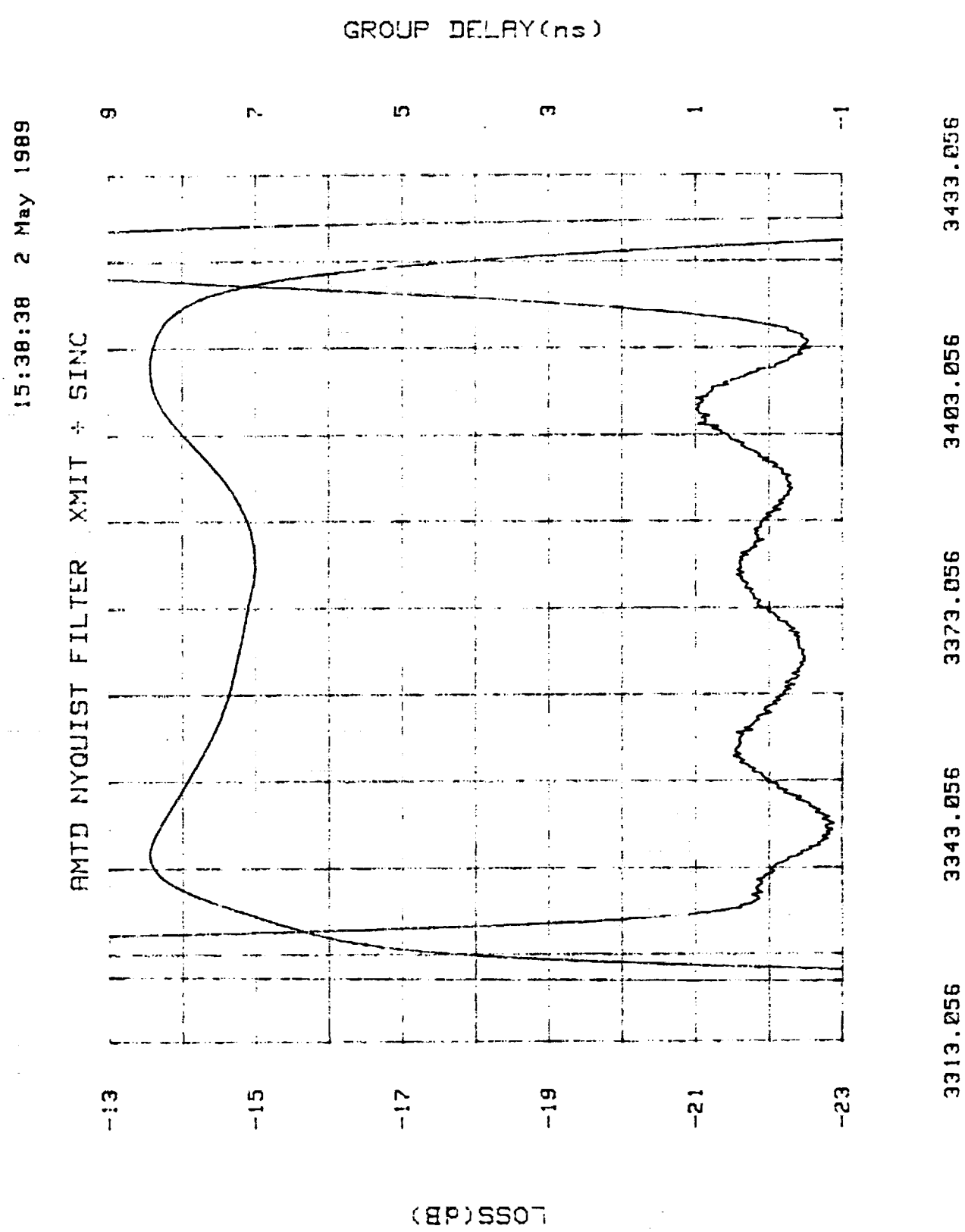


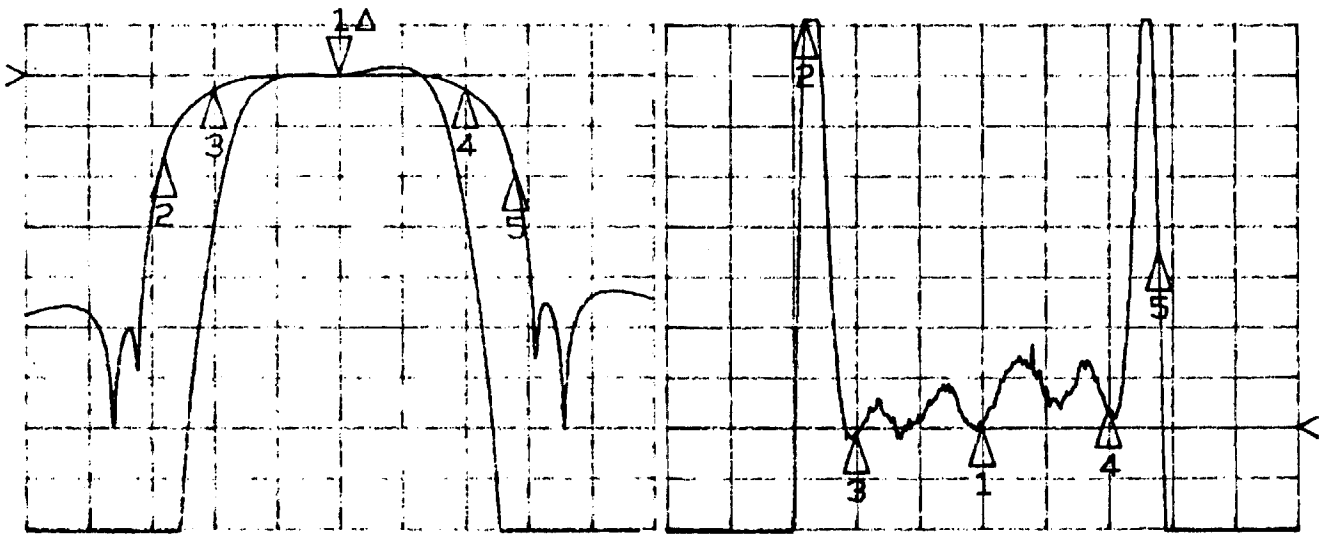
Figure 3-19b Narrowband Magnitude and Group Delay Response of 40% Rolloff Transmit Filter

S21/M log MAG
REF -2.675 dB
1 10.0 dB/
0.0 dB

S21/M -Δφ/Δω
REF 50.88 ns
Δ 1.0 ns/
1 0.0 s

AMTD INT + NOISE TEST SET RECEIVE SECTION 5/3/89

A



CENTER 3.373056000 GHz
SPAN 0.200000000 GHz

Figure 3-20a Wideband Magnitude Response of 40% Rolloff Receive Filter

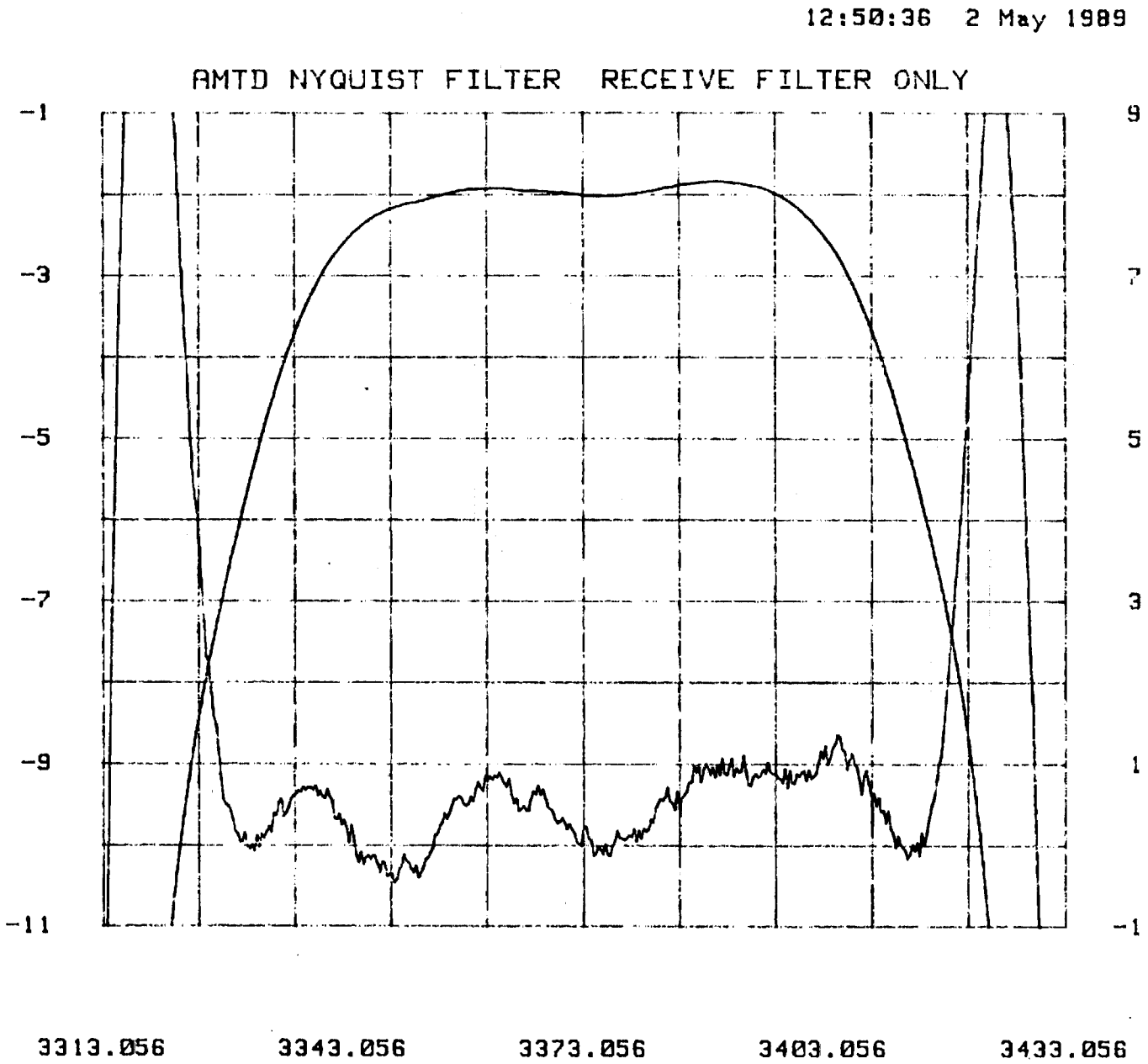


Figure 3-20b Narrowband Magnitude and Group Delay Response of 40% Rolloff Receive Filter

3.2.4 DEMODULATOR

The demodulator includes the analog quadrature detector and three levels of synchronization implemented digitally as follows:

- carrier acquisition and tracking
- symbol clock acquisition and tracking
- start of frame and UW detection and tracking

The carrier acquisition and tracking circuits also include the symbol decision function.

3.2.4.1 QUADRATURE DETECTOR

The output of the Interference and Noise Test Set is input to the demodulator shown in block diagram form on the D-size sheet. The input is equally divided between the demodulator and the amplitude detector used for clock synchronization. The latter detects the AM on the received signal due to the effect of band limiting of the initially constant amplitude 8PSK signal. The detected signal has a mean fluctuation frequency equal to the symbol frequency. This noisy signal is amplified, limited, and then filtered in the "baud acquisition" digital PLL. The signal to the demodulator is input to a quadrature detector fed by a 3.37 GHz reference oscillator. Under normal operation, the reference oscillator is not coherent with the received carrier (although it can be made so by a front panel switch for special testing). Assuming the received uplink carrier at 30 GHz were perfectly stable and that the maximum satellite oscillator instability was $\pm\ 5\times10^{-8}$, the maximum difference between the received carrier and reference oscillator is ± 1.5 KHz. The quadrature detector is discussed in detail in reference 10.

3.2.4.2 CARRIER TRACKING PLL AND BAUD DECISION

The digital phase locked loop used for acquiring and tracking the phase of the carrier burst is shown in block diagram form in the size-D foldout in the panel labeled "BAUD CALCULATOR". A first order PLL was selected because of its simplicity in requiring only a single accumulator (pole) and because, after the loop is synchronized during the preamble of each burst, the maximum accumulated phase error possible before the next synchronization burst is sufficiently small by virtue of the high stabilities of the oscillators. The two eight bit ADCs sample the I and Q outputs of the quadrature detector at an 80 MHz rate synchronized to the recovered symbol clock (averaged over many bursts). The timing of the sampling is carefully adjusted to the maximum opening in the eye-patterns of the I and Q waveforms. The carrier PLL is provided 12 bit digital words from the phase lookup table (RAM LUT) which are values of the arctangent of the instantaneous phase calculated from the pairs of I and Q samples. The 12 bit accumulator phase is subtracted from the input phase and yields an 11 bit difference which is latched and input to a block labeled "scalar". A multiplexer reduces the gain of the PLL after acquisition by a right shift. The maximum gain, 1/8, is used during acquisition and the minimum gain, 1/32, is switched in following the 32 symbol carrier sync portion of the preamble and used while tracking the modulated carrier throughout the rest of the burst where it averages the phase error modulo $\pi/4$. The lock-range for such a PLL using a linear phase detector is given by

$$LR_{linear}=\frac{\alpha}{2T} \qquad (3\text{-}8)$$

which for $\alpha=1/32$, $T^{-1}=40$ MHz, and applying another gain factor of 1/8 (due to the modulo $\pi/4$ operation) obtains a lock range of ±78 kHz. The measured lock range was about ±60 kHz.

A generic block diagram of a first order digital PLL is shown in Figure 3-21. The phase detector can either be a sinusoidal one as used in the symbol clock PLL or linear as used in the carrier PLL.

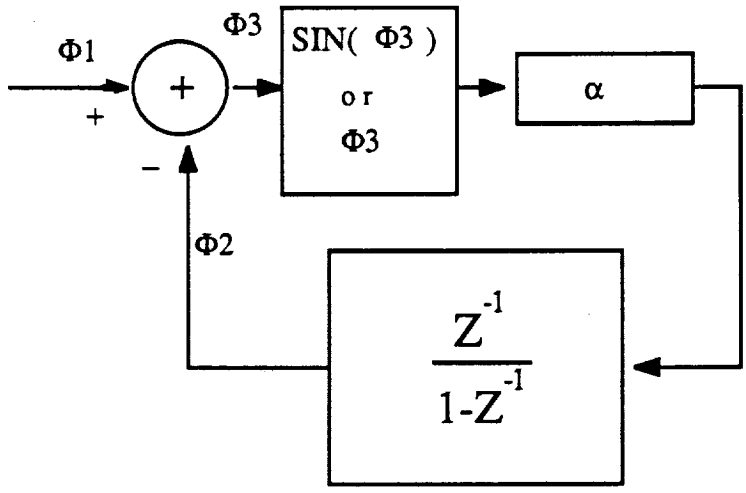


FIGURE 3-21 GENERIC FIRST ORDER DIGITAL PLL

The transfer function of the PLL for the case of a small phase error in the sinusoidal phase detector or in a linear phase detector is

$$\frac{\Phi 2(z)}{\Phi 1(z)} = \frac{\alpha}{z-(1-\alpha)} \qquad \text{for } \alpha \leq 1 \qquad (3\text{-}9)$$

For a step in frequency (i.e., a ramp in phase),

$$\Phi 1(n) = n\Omega T U(n) \qquad (3\text{-}10)$$

where U(n) is the unit sampled step function such that U(n) = 1 for $n \geq 0$, and zero for $n<0$.

$$\Phi 1(z) = \Omega T \frac{z}{(z-1)^2} \qquad (3\text{-}11)$$

$$\text{Then, } \Phi 2(z) = \frac{\alpha \Omega T z}{(z-(1-\alpha))(z-1)^2} \qquad (3\text{-}12)$$

$$\Phi 2(n) = Z^{-1}[\Phi 2(z)] = \frac{\Omega T}{\alpha}\left[(1-\alpha)^n - 1 + \alpha n\right] U(n-1) \qquad (3\text{-}13)$$

The error is obtained by subtracting (3-13) from (3-10) to obtain

$$\Phi 3(n) = \frac{\Omega T}{\alpha}\left\{\alpha n U(n) - \left[(1-\alpha)^n - 1 + \alpha n\right] U(n-1)\right\}$$
$$= \frac{\Omega T}{\alpha}\left\{1-(1-\alpha)^n\right\} \qquad \text{for } n>1 \qquad (3\text{-}14)$$

The final value of the error is obtained as

$$\lim_{n \to \infty} \Phi 3(n) = \frac{\Omega T}{\alpha} \qquad (3\text{-}15)$$

With a value of α = 1/8 and assuming the maximum initial frequency error between the LO and signal of ±1.5 KHz, evaluating (3-15) yields a final value of phase error of 0.03^{o}. Evaluating the quantity in (3-14) within the braces, for n = 32 symbols obtains the result that the phase has settled to within 99% of the final value by the end of the carrier portion of the preamble.

3.2.4.3 SYMBOL CLOCK PLL

The symbol clock recovery loop is shown in the panel labeled BAUD ACQUISITION in the size-D drawing and in Figure 3.-22. There are separate first order phase locked loops for each of the two independent bursts used in testing the POC. In addition to the usual PLL, linear predictive correction is used to extrapolate the expected phase of the clocks between bursts.

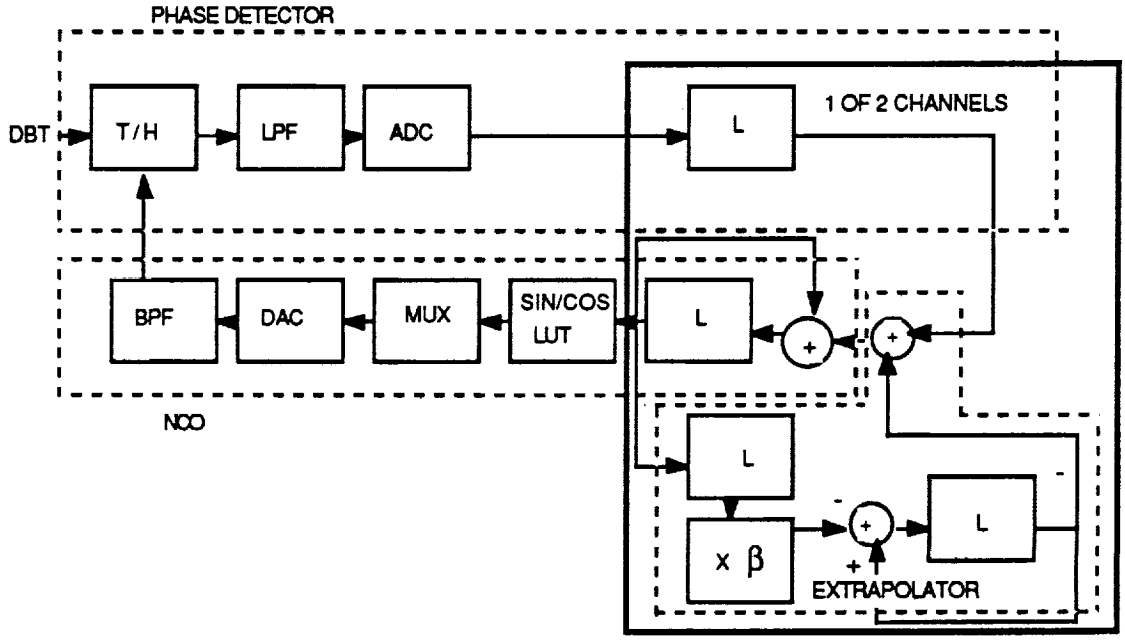


FIGURE 3-22 SYMBOL CLOCK RECOVERY LOOP

The symbol burst stability is specified as $\pm 5 \times 10^{-7}$ which for 80 Msps is ±40 Hz. This is also the required minimum lock-range of the symbol recovery first order PLL. The lock-range and bandwidth of a first order PLL are equal and, for a digital PLL, the lock-range, LR in Hz for a PLL with a sinusoidal phase detector is given by

$$LR_{sine} = \frac{\alpha}{2\pi T} \text{ Hz} \qquad (3\text{-}16)$$

For T^{-1}=80 MHz, and $\alpha = 2^{-17}$, LR=±97 Hz. The average lock range as actually measured was approximately ±140 Hz. The loop noise bandwidth for a first order PLL is the bandwidth multiplied by $\pi/2$ which is 152 Hz for our loop. This information alone is not of much use except as one parameter in an equation

relating the phase jitter to the input signal-to-noise ratio and Nyquist filter rolloff. Unfortunately, obtaining such a relationship mathematically is formidable and a published result has not been found in the literature for the case of extracting symbol sync from the 8PSK waveform.

3.2.4.4 UW START OF FRAME DETECTOR

The operation of the UW and start of frame circuits are discussed in reference 11. A mathematical analysis of the UW operation is given in Appendix F.

3.3 POC MODEL SPECIFICATION AND TESTING

3.3.1 SPECIFICATIONS AND TEST PROCEDURES

The specifications for the POC model are given in Table 3.3.1-1. While it was originally planned to measure the POC Model according to seven test specifications, the lack of feasible tests and test equipment for a number of the parameters forced their abandonment within the constraints of budget and schedule. Thus, the only measurements carried out were BER tests in the presence of AWGN, ACI, and CCI.

TABLE 3.3.1-1 Specification of the POC Model

PARAMETER	VALUE	TEST SPEC. NO. OR METHOD OF DETERMINING COMPLIANCE
Bandwidth Efficiency	> 2 Bits/sec/Hz	1
Bit Rate	240 Mbps	by design
Channel Spacing	96 MHz	by design
Transmission Mode	TDMA	by design
Frame Length	1 ms	by design
Preamble (CW portion) (UW portion)	32 symbols 8 symbols	by design
Receive Frequency	3.373056 GHz±1.5KHz	by design
Input level at receiver filter	-30 dBm±0.5 dB	by design
BER at Es/No=21 dB	$< 5 \times 10^{-7}$	2
Degradation Due to +20 dB ACI	< 1 dB	3
Degradation Due to -20 dB CCI	< 1 dB	3
Probability of bit error due to missing unique word	$< 1 \times 10^{-7}$ at Es/No =13 dB	by computation (4)
Probability of Carrier Cycle Slip	< TBD at Es/No= TBD dB	5
Bit-timing Jitter	< 125 ps RMS	6
Probability of Clock Cycle Slip	< TBD at Es/No=TBD dB	7
Minimum Guard Time Between Bursts		25 ns by design of STE

3.3.2 SPECIAL TEST EQUIPMENT

The special test equipment used to measure the performance of the POC model was the Interference/Noise Generator and the bit error rate tester (BERT). These equipments are discussed in detail in reference 12 and 7 respectively.

4.0 DISCUSSION OF TEST RESULTS

4.1 ANALOG TESTS

The spectrum output of the 8PSK modulator before filtering by the transmitter filter is shown in Figure 4.1-1. The power spectrum is the characteristic $[\sin(x)/x]^2$ of a rectangular pulsed modulator. A small amount of 80 MHz clock leakage is evident but will be almost completely suppressed by the filters. The spectrum of the modulator subjected to the square-root Nyquist transmitter filter (all the rolloff factors shown in this section are for α=0.4) and inverse sinc equalizer plus the delay equalizer is shown in Figure 4.1-2. The "bandwidth efficient " spectrum is quite evident from this picture. The output of the receiver square-root Nyquist and its associated equalizer is shown in Figure 4.1-3. Since this is the cascaded spectrum of two square-root Nyquist filters, the characteristic shape is the full Nyquist response where the 6 dB bandwidth is the 80 MHz symbol rate. Some slight in-band ripple is evident which probably contributes to the ISI loss of the system. The constellation as displayed at the output of the quadrature detector on the HP 8980A is shown in Figure 4.1-4. To obtain the despun display, an LO coherent with the transmitter was injected at the quadrature detector. The dispersion of the constellation "clouds" is due to ISI. The smallest dispersion is obtained when the ADC clock is optimized for mid-baud sampling at precisely the maximum eye opening. The I and Q eye-patterns shown in Figures 4.1-5 and 4.1-6 respectively were produced under the same test conditions as the constellation display. The constellation display can be thought of as a "cut" across the time axis which runs perpendicular to the plane of the constellation display. Thus the eye-patterns can be obtained from the constellation display by rotating it first about the I-axis to get the I eye-pattern and then around the Q-axis to get the Q eye-pattern. The constellation corresponds to the maximum eye opening while the rest of the eye-patterns are traced out by moving the sampling point in time to early and late positions (i.e., into and out of the paper of the constellation display).

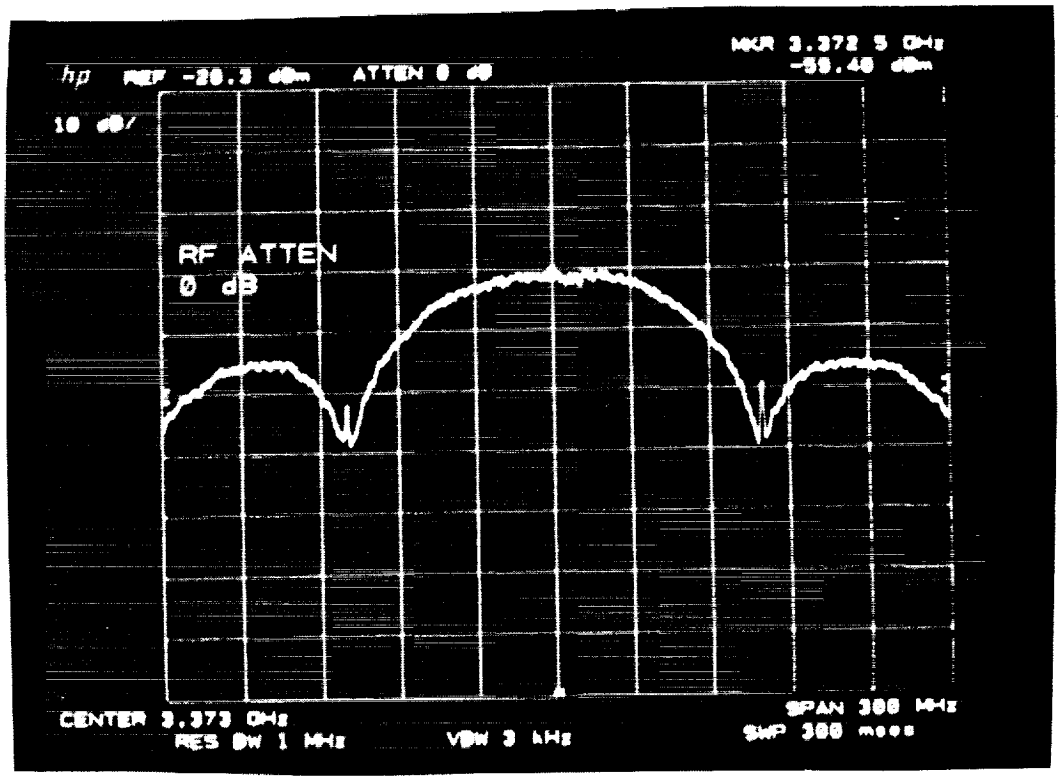


Figure 4.1-1 Power spectrum at output of 8PSK modulator

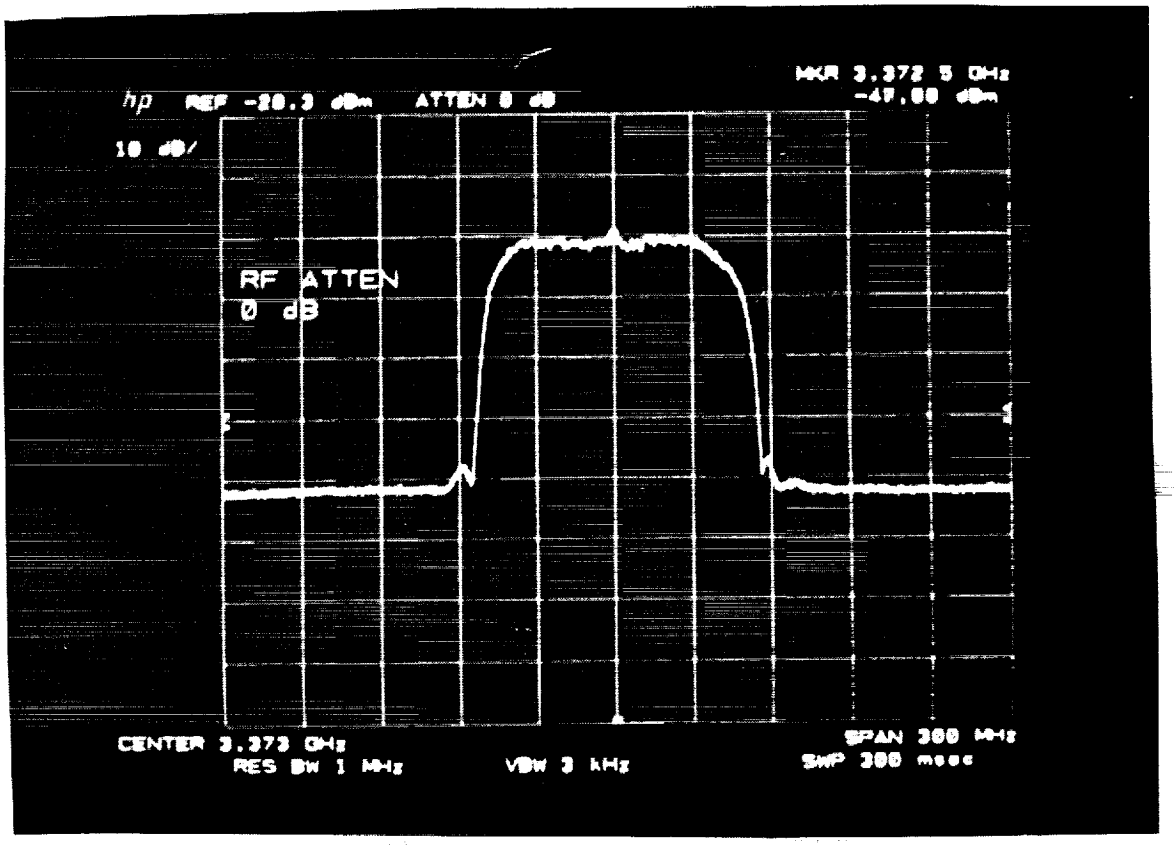


Figure 4.1-2 Power spectrum at output of transmitter. Includes effects of square-root Nyquist filter, inverse sinc equalizer, and group delay equalizer.

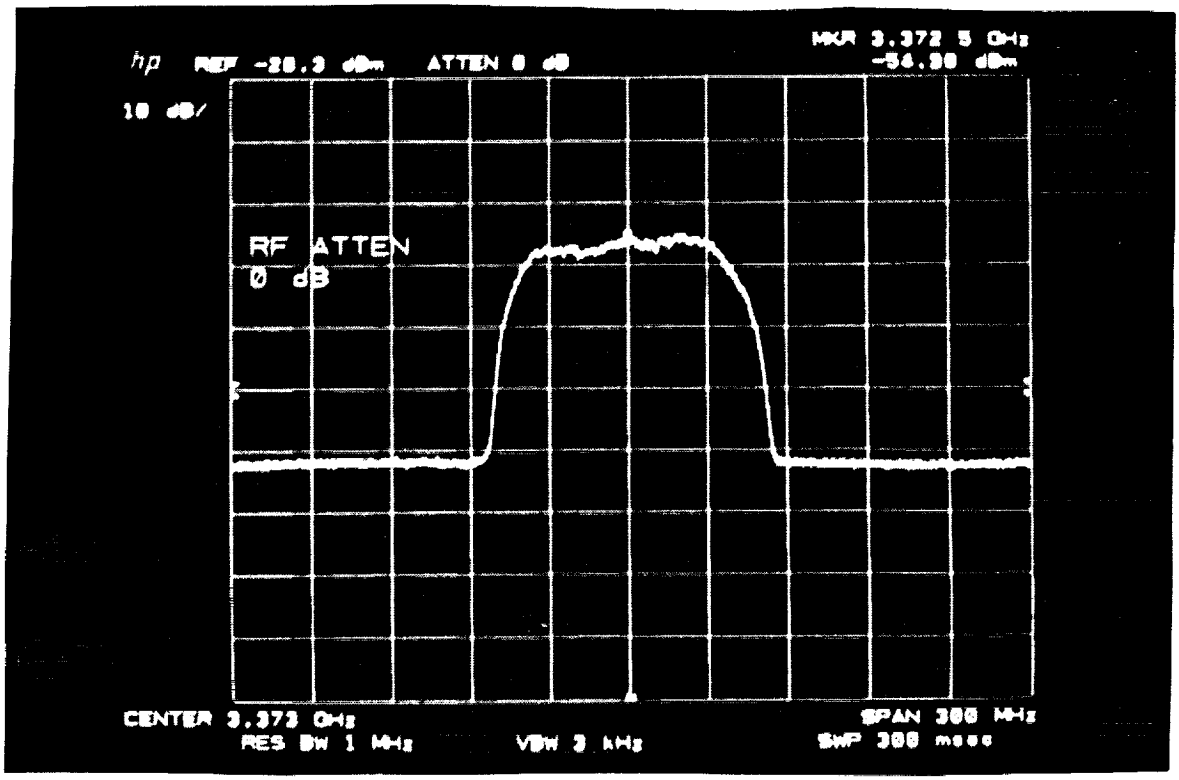


Figure 4.1-3 Power spectrum at output of receiver filter. Shows full Nyquist response due to cascade of transmitter and receiver filters and modulator spectrum

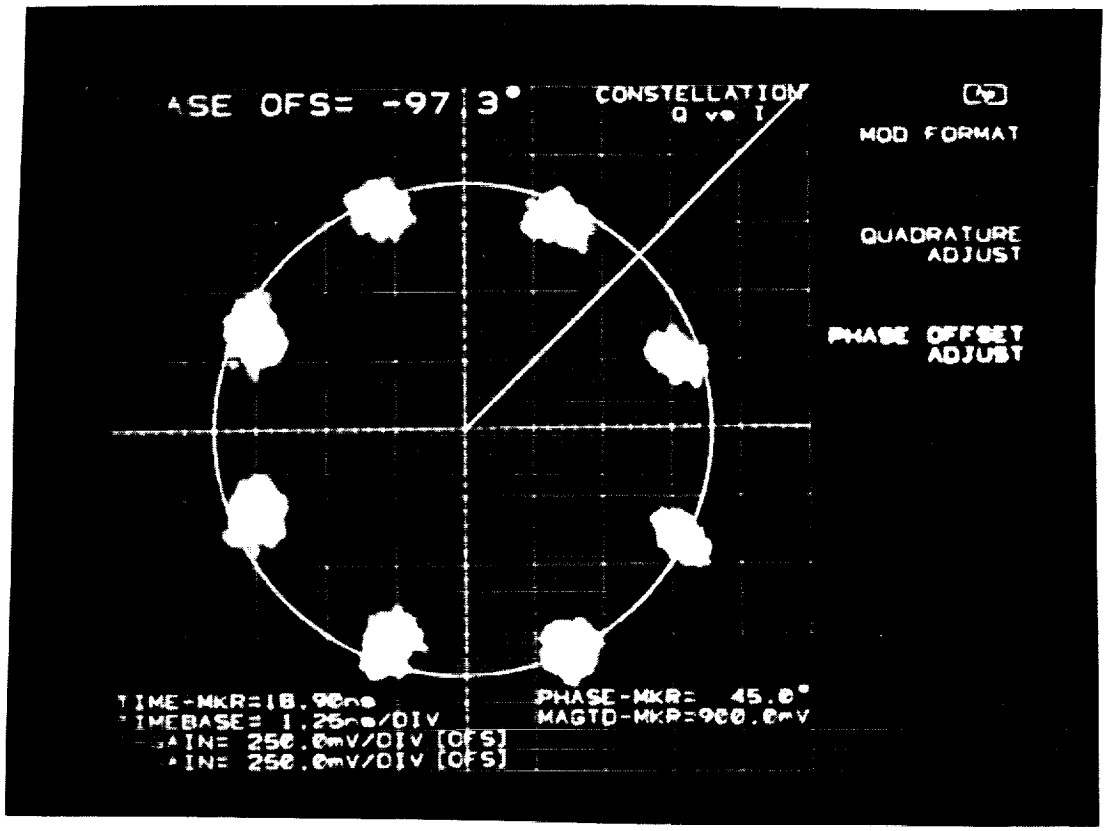


Figure 4.1-4 8PSK Constellation as displayed on HP 8980A

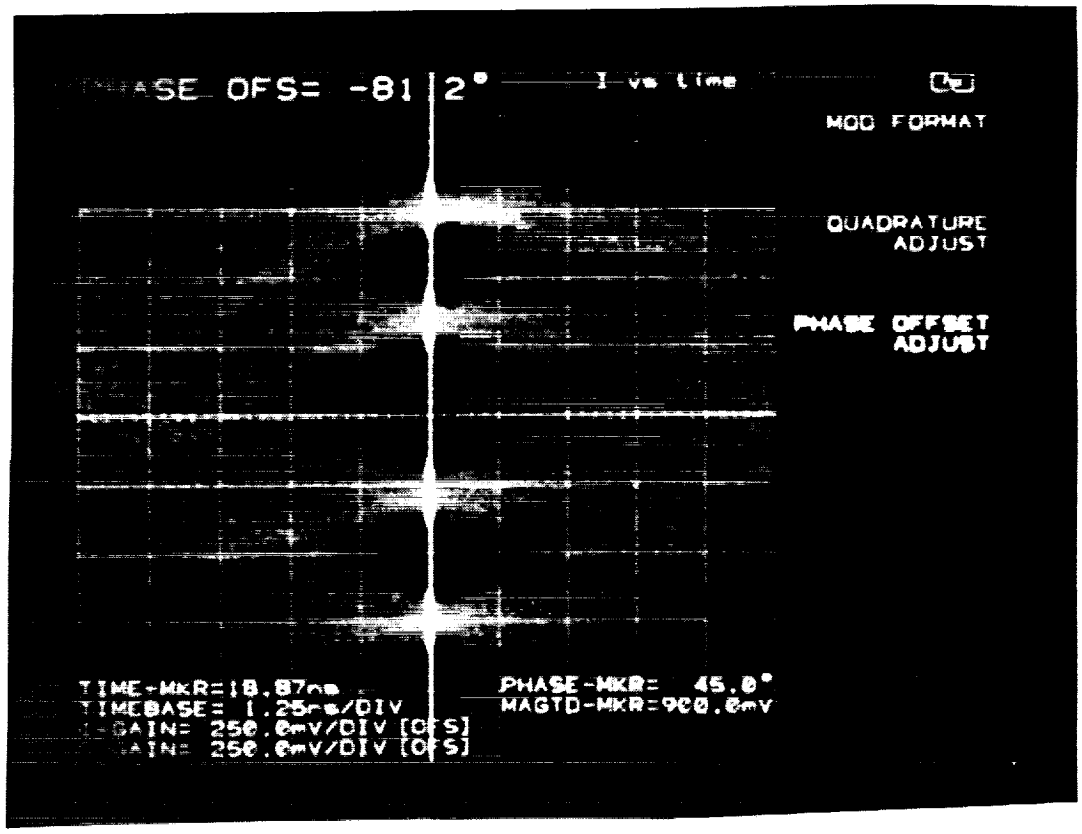


Figure 4.1-5 Eye pattern on I side at output of quadrature detector

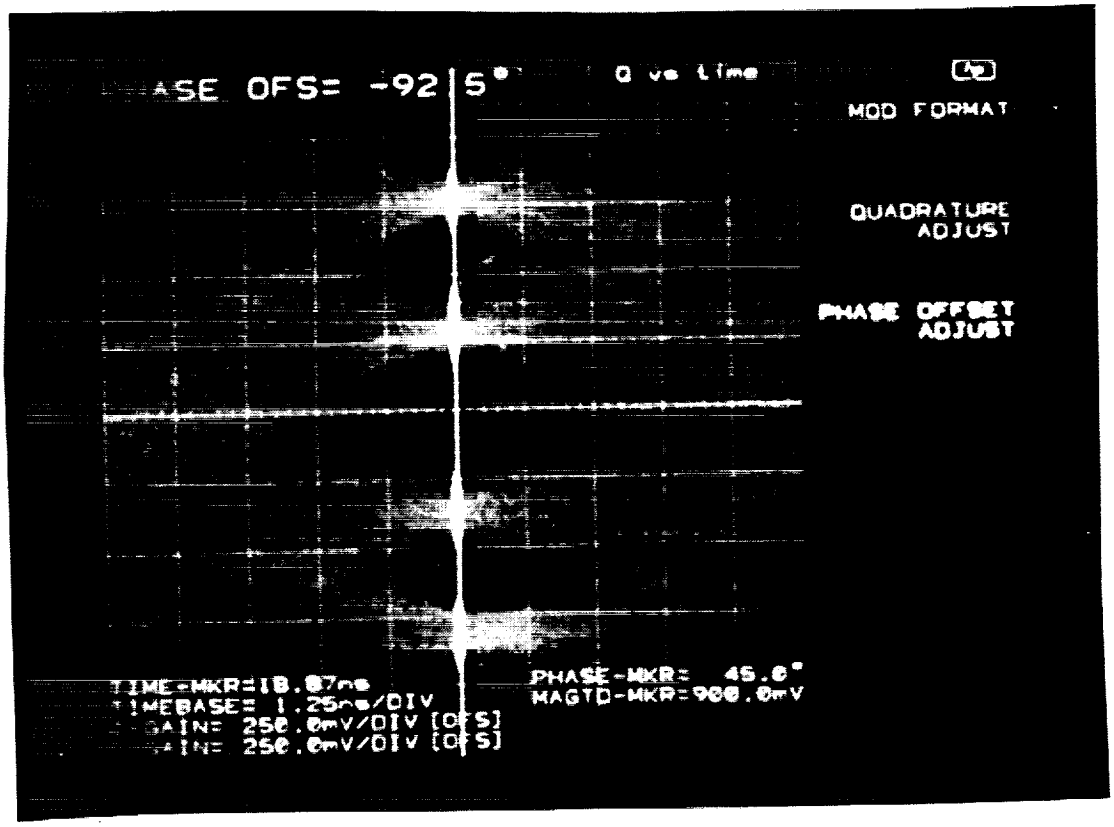


Figure 4.1-6 Eye pattern on Q side at output of quadrature detector

The correct adjacent channel spacing for the ACI measurement with α=0.4 is 112 MHz. The spectrum before the receiving square-root Nyquist filter in the Interference/Noise test set is shown in Figure 4.1-7 for 112 MHz spacing and +10 dB ACI to desired signal ratio. The deep cusps in the display indicate that there is little leakage from the ACI to the desired channel. Similarly, even with +20 dB ACI as shown in Figure 4.1-8 the deep cusps indicate low interference. Repeating the same tests with the spacing of 96 MHz (this is the spacing appropriate to the α=0.2 filters) the cusps in the spectra no longer exist as shown for +10 dB and +20 dB ACI in Figures 4.1-9 and 4.1-10 respectively. The absence of the cusps indicate leakage of interference power from the ACI into the desired channel and, as will be shown in the next section, predictably cause serious degradation of the BER performance.

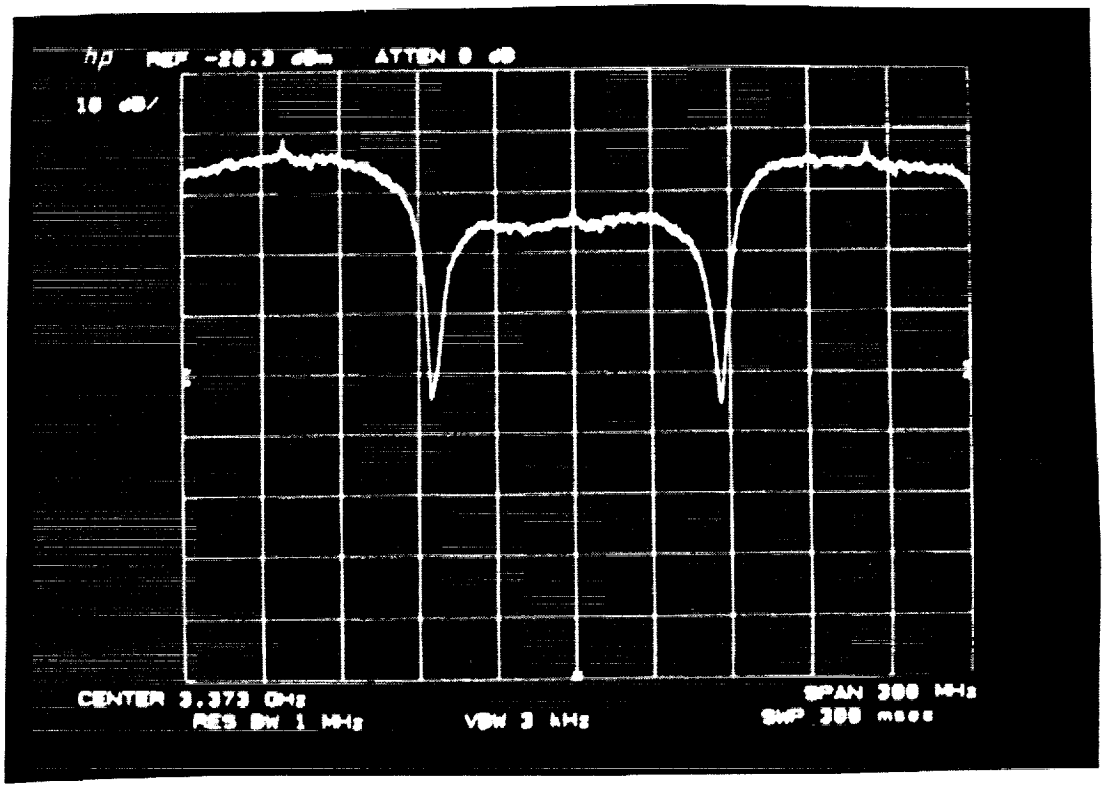


Figure 4.1-7 Spectral display of +10dB ACI for 112 MHz separation between channels

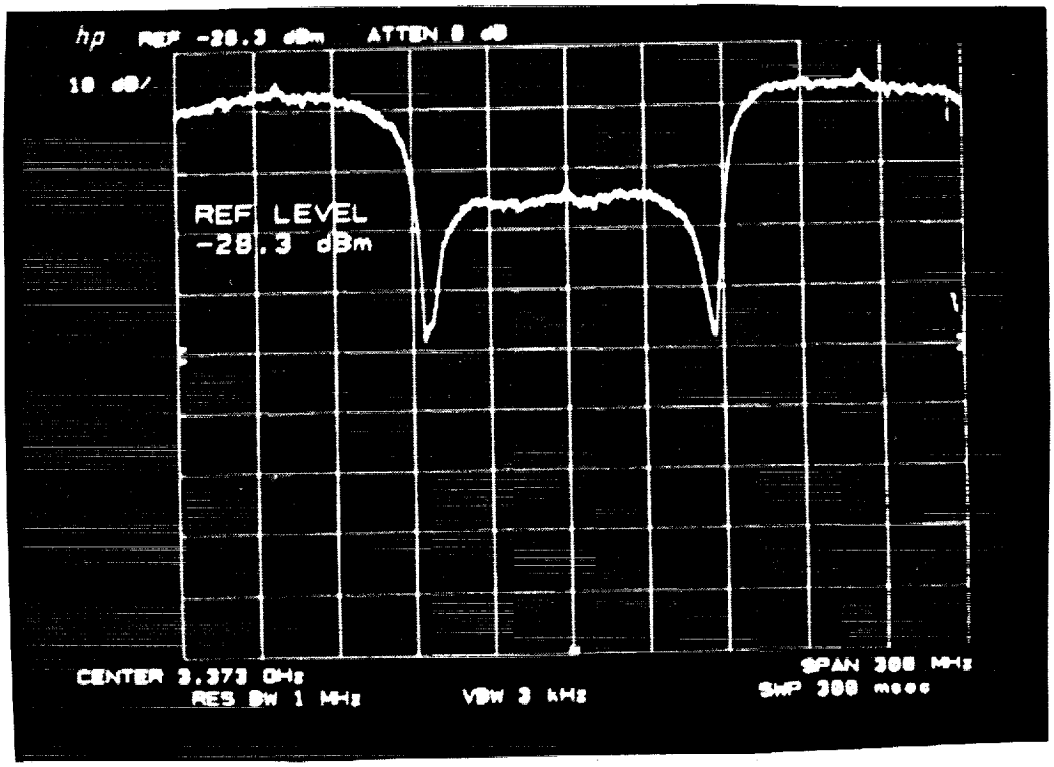


Figure 4.1-8 Spectral display of +20dB ACI for 112 MHz separation between channels

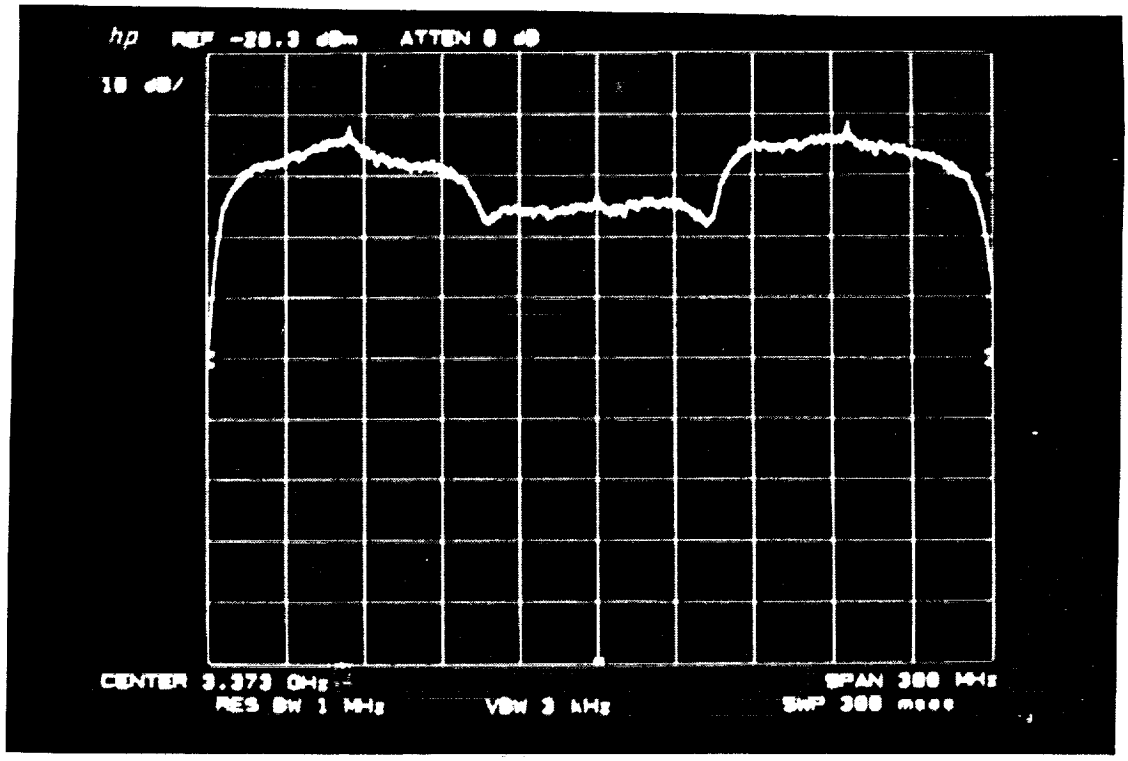


Figure 4.1-9 Spectral display of +10dB ACI for 96 MHz separation between channels

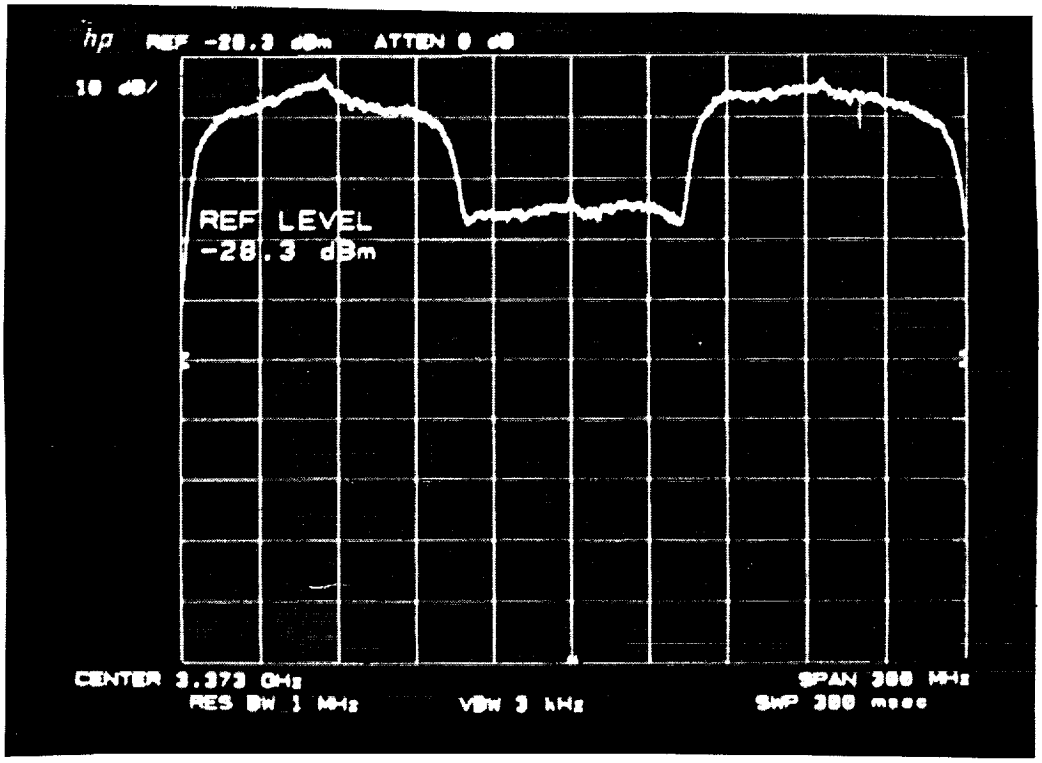


Figure 4.1-10 Spectral display of +20dB ACI for 96 MHz separation between channels

4.2 BER TESTS

The function of a demodulator is to take the input modulated r.f or i.f. signal in its noisy and distorted environment, extract the modulated information bits from it with the fewest possible errors, and pass the bits in a serial stream to the output. Hence, the most fundamental test of the demodulator is the BER versus symbol energy-to-noise-density ratio (Es/No). The theoretical curve and test results for the POC Model are shown in Figure 4.2-1 which displays the results for a long burst occupying almost the entire frame as well as a "short" burst occupying 46% of the frame. At the specified performance point of 5×10^{-7}, the long burst BER is about 4.5 dB from theoretical. The short burst BER curve diverges rapidly from theoretical. (In Figure 4.2-1 the clock offset frequency is 8 Hz.)

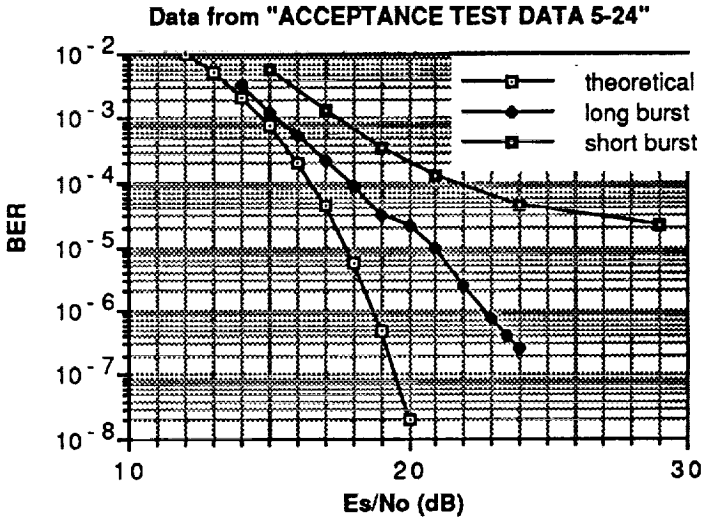


FIGURE 4.2-1 BER versus Es/No for Long and Short Bursts

The effect of burst length on BER is displayed in Figure 4.2-2 as BER versus burst length as a percentage of the frame length at Es/No=24 dB. (In Figure 4.2-2, the clock offset is 2 Hz.) We conclude that the degradation in BER as the burst length decreases is due to the poor performance of the clock phase extrapolation circuit which fails to accurately predict the phase ramp from the end of one burst (of an access) to the beginning of the next burst (of the same access). As illustrated by comparing Figures 4.2-1 and 4.2-2, the greater the frequency offset the the greater the degradation due to the error in predicting the clock phase.

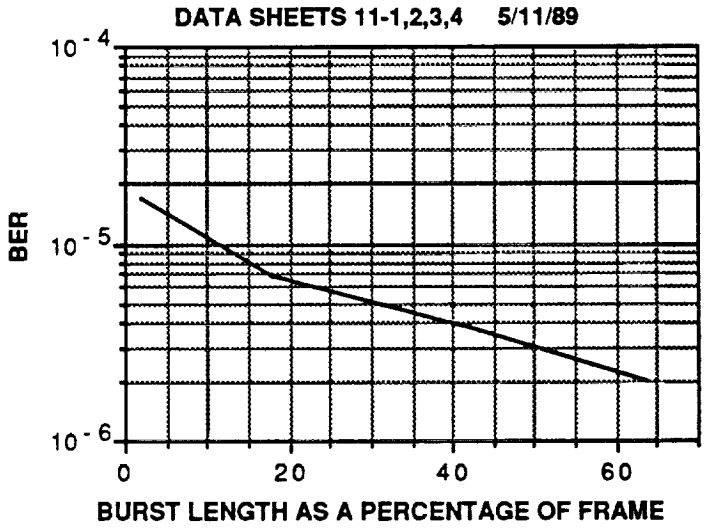


FIGURE 4.2-2 BER versus Burst Length as a Percentage of Frame Length

Figure 4.2-3 depicts the degradation of BER versus the offset between the LO and the input carrier frequencies for several values of Es/No. In a first order PLL, the static phase error is directly proportional to the offset frequency and a rapid degradation in the BER performance occurs as the static phase error builds up. As can be seen from the figure, the rate of BER degradation is greater at high values of Es/No than at lower ones.

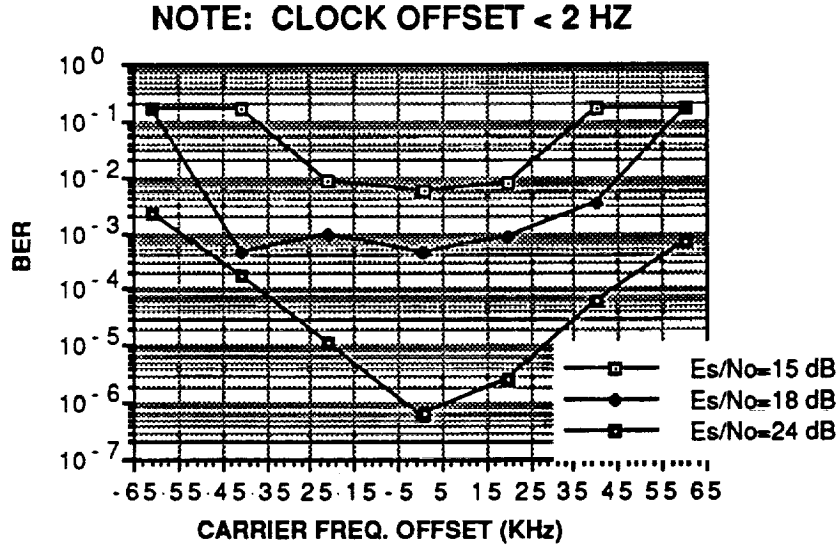


FIGURE 4.2-3 BER versus Carrier Offset Frequency

Figure 4.2-4 depicts the degradation in BER versus the offset between the demodulator baud clock crystal LO and the true received baud rate. The reason

for the asymmetry of this curve is due to the fact that the cables which adjust the sampling pulse into the ADCs for optimality were cut for a phase-shift corresponding to an offset frequency of about 40 Hz. Again, the BER degradation steepness is higher for higher values of Es/No.

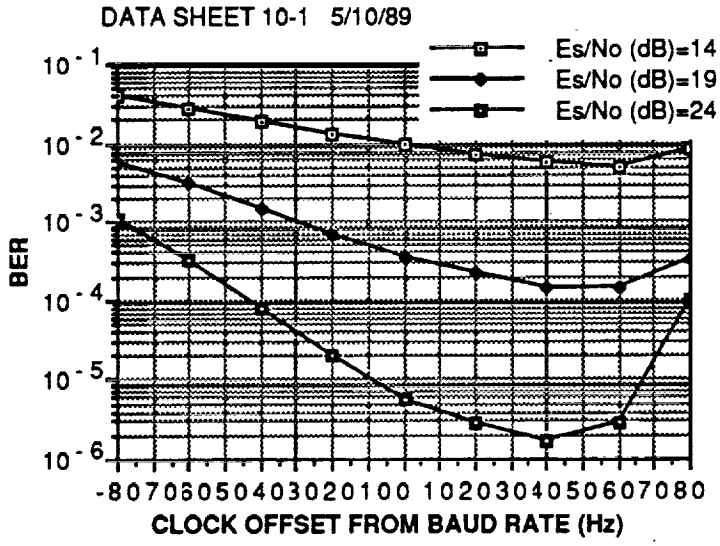


FIGURE 4.2-4 BER versus Clock Offset Frequency

The graph of Figure 4.2-5 shows the effect of CCI at two levels, -20 dB and -25 dB relative to the desired signal. The CCI causes less than the expected degradation of 2 dB due to the fact that the demodulator implementation loss dominates the BER performance even in the presence of small values of CCI.

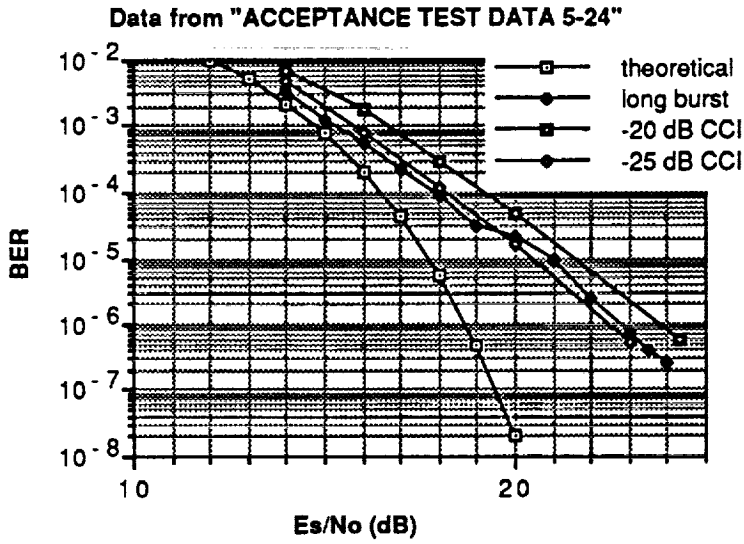


FIGURE 4.2-5 BER versus Es/No for several values of CCI

Figure 4.2-6 displays the effects of ACI of various levels on the BER for ACI channels spaced at ±112 MHz (which is the spacing given by equation 3-1 for α=0.4). The indicated "long burst" data is in AWGN only. It is noted that no sig-

nificant degradation is observed until the ACI is increased to +15 dB relative to the desired signal. This should be compared to the data in Figure 4.2-7 which shows the effects of ACI spaced by 96 MHz, the adjacent channel spacing originally planned for the filters having α=0.2. In this case, because the Nyquist rolloff factor is 0.4, even ACI of -10 dB relative to the desired signal causes significant BER degradation.

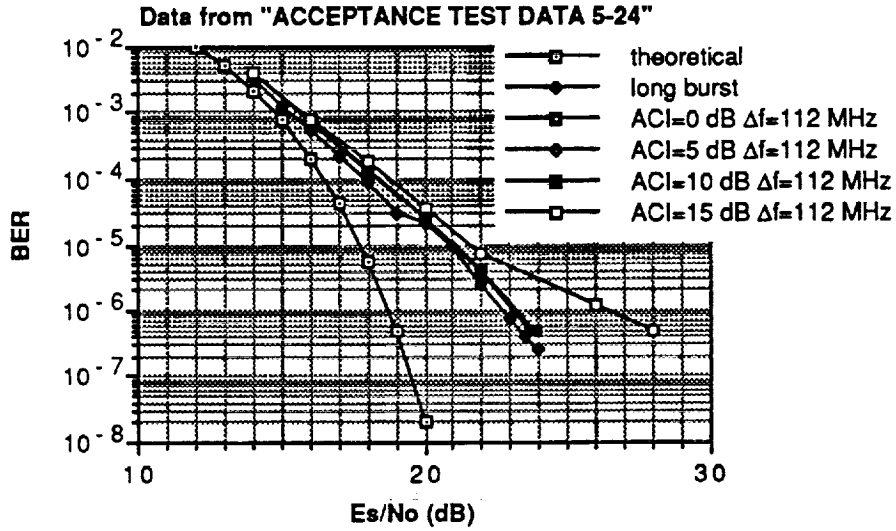


FIGURE 4.2-6 BER versus Es/No for ACI at 112 MHz

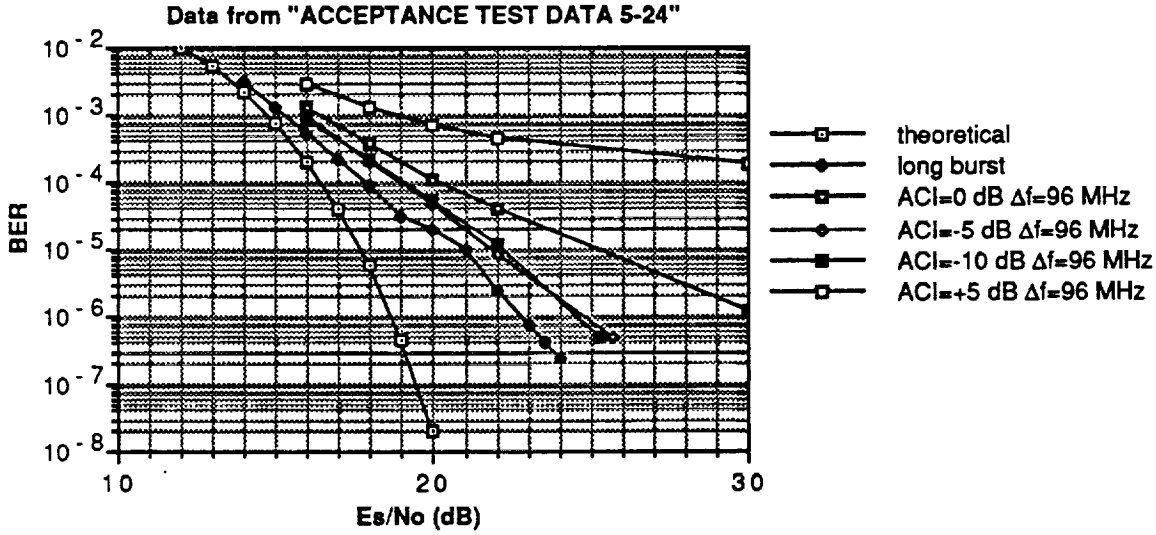


FIGURE 4.2-7 BER versus Es/No for ACI at ±96 MHz

4.3 CAUSES OF IMPLEMENTATION LOSS

It is believed that the sources of degradation in AWGN for long bursts are due to the following:

- intersymbol interference in the Nyquist filters

- jitter in the recovered clock causing non-optimum sampling of the baseband signals at the I and Q ADCs

- jitter in the recovered clock causing false error indications out of the BERT
  (i.e., the true BER may be better than we measure due to false errors in the BERT)

In the case of short bursts, it seems likely that the increased degradation when reducing the burst length is due to the poor extrapolation of phase from the end of one burst to the following burst from the same access.

The ISI is due to the fact that the Nyquist filters at the receiver and transmitter are neither ideal in their shape, matched to the input symbol rate, or perfectly linear in delay. Neither are they matched to each other. Similarly, the inverse sinc equalization in the transmitter is nonideal thereby also contributing some ISI loss.

Jitter in the recovered clock may be the greatest cause of degradation in the BER. No analytical or simulation results were found in the literature for 8PSK thus there is very little information on which to base an optimal design. The clock recovery is based on the fact that if an MPSK waveform which is passed through a band-limiting filter is applied to a generalized amplitude detector, the detector output will consist of a DC component with pattern noise as well as harmonics of the symbol frequency surrounded by pattern noise caused by the random data. The clock recovery is effected by envelope detecting the output of the receiver bandpass filter, amplifying the detector output in a wideband video amplifier, thresholding in a Schmidt trigger, and finally filtering in a very narrow digital PLL which tracks the 80 MHz component while rejecting the pattern noise. The design of both the detector and its preceding bandpass filter needs to be optimized to minimize the effects of jitter.

The cause of the very poor performance in ACI with 96 MHz channel spacing is clearly the use of the filters with α=0.4 instead of the originally proposed rolloff factor of 0.2.

5.0 SUMMARY OF RESULTS AND CONCLUSIONS

1. The basic Ford concept for the 8PSK demodulator was proven to be valid although a better method of symbol clock estimation will need to be devised to avoid degradation on short bursts. This can be achieved in one of two ways:

   a. Improve the means of extrapolating the phase from the end of one burst to the arrival of the next burst

   b. Independently acquire the phase of the symbol clock on each burst as is done for the carrier. This would likely require lengthening the preamble by adding a clock acquisition section.

2. To achieve the specified bandwidth efficiency of better than 2 bits/sec/Hz, with 8PSK, the Nyquist filter rolloff factor will need to be no larger than 0.2. Ford originally proposed and tried to use a set of SAW filters for this purpose

but this approach was frustrated due to the following factors:

a.The modulator and quadrature detector, which were almost completed when the contract started, were built at about 4 GHz. NASA then specified the interfacing IF frequency to be 3.37 GHz. For budgetary reasons it was decided to use the already developed units.

b. SAW filters cannot be built at 4 GHz and the ones ordered were centered at 280 MHz requiring four stages of up and down conversions in order to use the existing modulator and quadrature detector. The conversions proved to be not feasible due to attendant distortion and extra complexity they introduced.

3. The microwave Nyquist filter with α=0.2 proved to have excessive ISI causing a very large implementation loss and were, therefore, replaced with a similar design with α=0.4. The implementation loss using the α=0.4 filter was lower than that with the α=0.2 filter but, as shown by the results above, the ACI goal with 96 MHz channel spacing, hence the bandwidth efficiency target of 2 bits/sec/Hz, cannot be realized. Ford believes that if the modulator and quadrature detector were built at 280 MHz, the SAW filter approach would be the most feasible even for α=0.2. This would necessitate an up and down converter pair to operate at the NASA specified 3.73 GHz IF.

An estimate of the logic gates has been made for the various sections of the digital portions of the demodulator and is reported in Appendix G. It has been concluded that the entire digital portion could be built on two ECL gate arrays although external memory parts might be required for the lookup table. The quadrature detector including the local oscillators could be integrated onto a small hybrid device along with the SAW filter. The goal would be a complete demdodulator on a card of about 5 by 7 inches and weighing only a few ounces. Power dissipation would be about 10 to 15 watts.

6.0 REFERENCES

1. Advanced Modulation Technology Development for Satellite Demodulator Applications, RFP3-650502 11/06/84, NASA Lewis Research Center, Cleveland, Ohio

2. Advanced Modulation Technology Development for Satellite Demodulator Applications, Volume II-Technical Proposal Ford Aerospace & Communications Corp., Palo Alto, CA 15 Jan. 1985

3. Advanced Modulation Technology Development , IR&D Report, Feb. 1986

4. S. Ames "BER Due to Unique Word Errors in AMTD", Project Memo, June 27,1988.

5. Letter to NASA LeRC from FACC, Sept. 2, 1985 ref. 3E2620-85-SEC-2472 (FEC breadboard not included)

6. AMTD POC Demodulator System Documentation: Burst Generator Operation/Specification

7. AMTD POC Demodulator System Documentation: Modulator/BERT Operation/Specification

8. J. J. Poklemba, "Pole-zero approximations for the raised cosine filter family", COMSAT Technical Review, Vol. 17, No. 1, Spring 1987

9. S.J. Fiedziuszko, "Dual Mode Dielectric Resonator Loaded Cavity Filter," IEEE Trans. Microwave Theory Tech., Vol. MTT-30, pp 1311-1316, September 1982.

10. AMTD POC Demodulator System Documentation: Quadrature Detector Operation Manual May 24, 1989

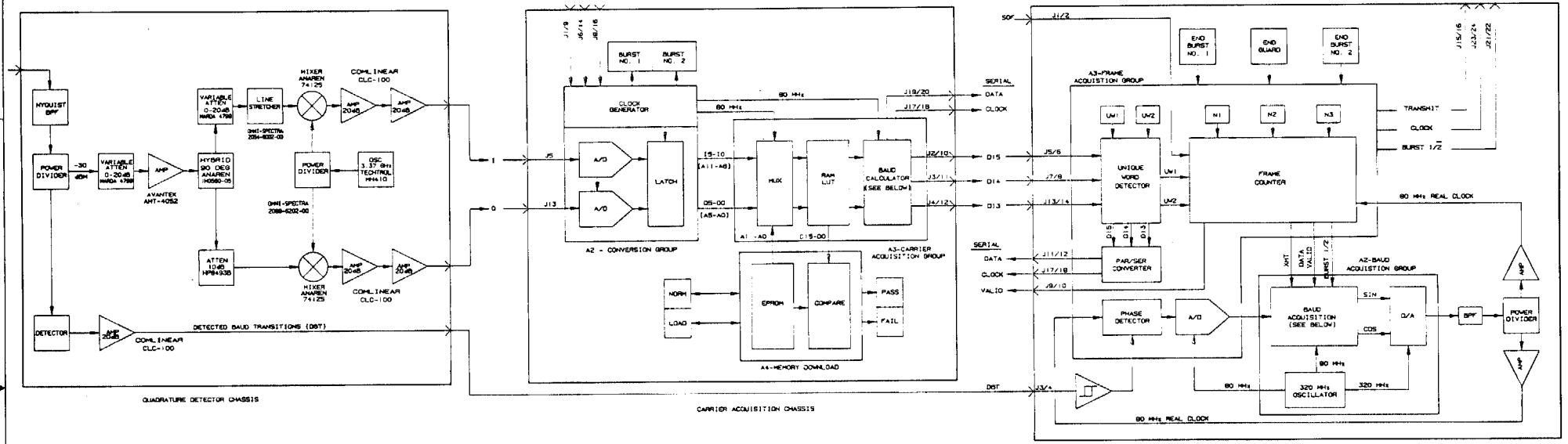
11. AMTD POC Demodulator System Documentation: Carrier Acquisition/Baud Acquisition Specification

12. AMTD Special Test Equipment System Documentation Interference/Noise Generator Operation Manual May 24, 1989

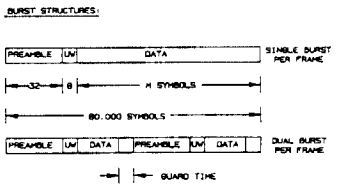
NOTES (UNLESS OTHERWISE SPECIFIED):

REVISIONS

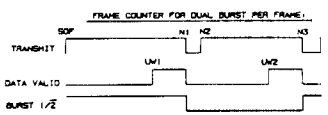
REV	DESCRIPTION	DATE	APPROVED

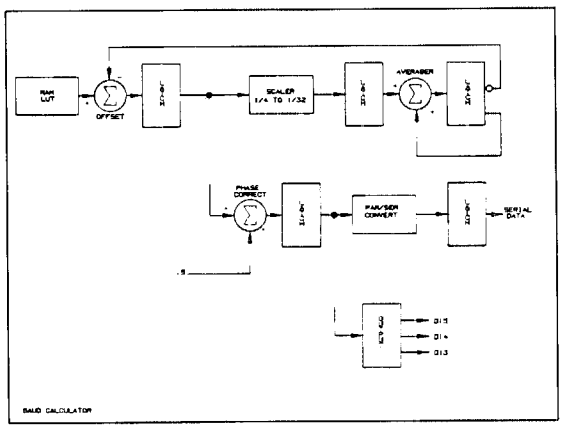


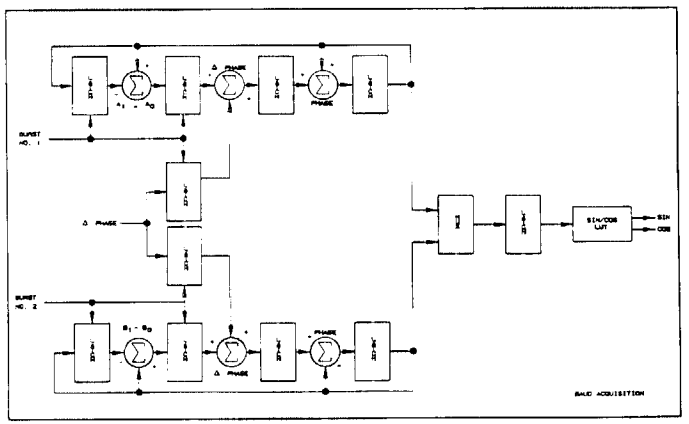
BURST STRUCTURES:



FRAME COUNTER FOR DUAL BURST PER FRAME:







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D	11530	DEMODULATOR	

SCALE SHEET

APPENDICES:

A Modulation/ Demodulation System Requirements

B Test Procedure and Data Sheet #1---Bandwidth Efficiency

C. Test Procedure and Data Sheet #2-- Bit Error Rate Test

D. Test Procedure and Data Sheet #3--ACI and CCI Test

E. Test Procedure and Data Sheet #6--Bit Timing Jitter

F. BER Due to Unique Word Errors in AMTD

G. AMTD ASIC

TITLE: AMTD MODULATION/DEMODULATION SYSTEM SPECIFICATION

1.0 Scope

This document defines the design, performance, and operating requirements for the AMTD Proof-of-Concept (POC) modulation/demodulation system.

2.0 Applicable Documents

The following documents and their amendments form a part of this specification:

AMTD Statement of work NAS3-24678
Preliminary Design Review 17 June 1986
Workmanship Standard Mil Std 454, Req. 9
Drawings Standard DOD-D1000B, Level 1,
Development Design Drawings

3.0 Requirements

3.1 Modulation System Requirements

The modulation system shall include the following elements: encoder, burst formatter, modulator, interference and noise test set, demodulator, and decoder. The block diagram in figure 1 shows the arrangement of these elements in the modulation system.

The actual equipment produced during the program will be governed by the following agreements with the government:

1) The POC model with respect to the requirements below will consist of the encoder, modulator, demodulator, and decoder.

2) The encoder and decoder will be produced as a paper design only. The coded system performance will be inferred from the uncoded performance as measured without encoder and decoder as shown in Figure 1.

3) The demodulator is the only deliverable hardware unit.

4) The modulator and special test equipment including the burst formatter and interference and noise test set which will be built during the program will be loaned to the government on an indefinite basis.

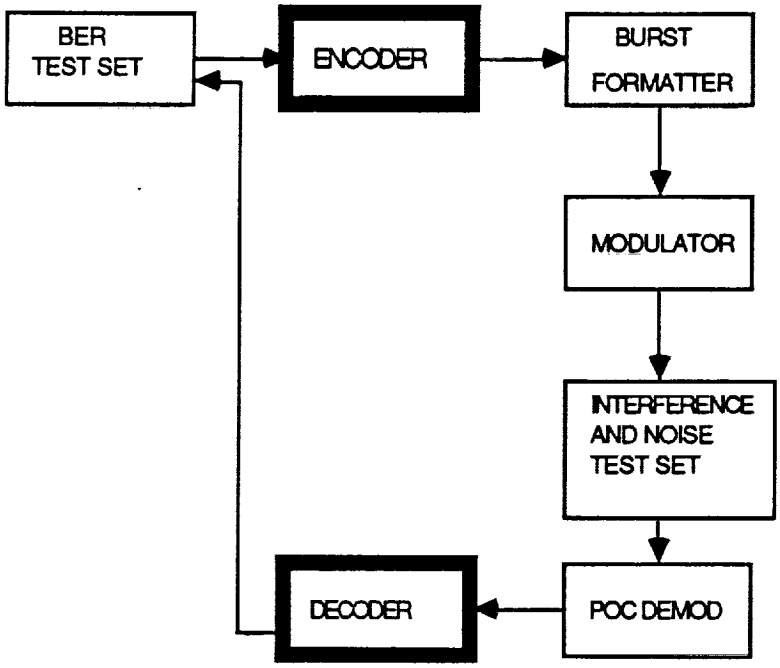


FIGURE 1. ARRANGEMENT OF MODULATION SYSTEM ELEMENTS FOR TESTING

3.1.1 General Requirements

(a) The uplink modulation system shall operate in a multiple channel environment with satellite TDMA and a single modulator and transmitter per channel. (e.g. FDM/TDMA uplink) The transmitter shall exhibit nonlinear transfer characteristics as specified in Figure 3.8.3 of the S.O.W.

(b) The modulation system shall support the full range of baseband information throughputs from 100 kbps up to and including 200 Mbps per demodulator with a burst rate of greater than 200 Mbps. The modulation system will be tested only at the maximum burst rate of 240 Mbps.

(c) The modulation system shall be designed for a significant advancement in bandwidth efficiency while preserving state-of-the-art system performance and minimizing power requirements.

(d) The modulation system shall use IF carrier demodulation at 3.373056 GHz.

(e) For the purpose of determining the usable bandwidth, assume adjacent channels are equal to the desired channel in bandwidth and burst rate and meets the adjacent channel interference specified in 3.2.2 e.

3.1.2 Modulation Scheme and System Hardware Goals

(a) The modulation scheme developed for the uplink modulation system shall be optimized for bandwidth efficiency within the constraints imposed by the uplink system and POC model requirements.

(b) The demodulator hardware design shall possess the potential for small size and low weight and power consumption for flight application.

(c) The demodulator hardware design shall incorporate advancements in component technologies, where possible, while maintaining a high probability of successful implementation.

3.2 POC Model Requirements

3.2.1 General Requirements

(a) The POC model shall adhere to the general modulation system requirements of section 3.1

(b) The POC model of the advanced technology satellite demodulator shall be capable of verifying though a combination of tests and analyses the modulation system concepts and designs developed in Tasks I and II and provide an information base for future design development of EM demodulators including potential MMIC and LSI implementations. The POC model shall be functionally equivalent to, but need not represent the form or fit of a final flight-qualifiable demodulator. The design shall consist of all drawings and specifications generated for the POC model and any LSI implementation recommendations which are derived from the test results for the POC model.

(c) The POC model shall consist of those devices necessary to recover the original baseband data from received bursts of a modulated carrier following uplink degradations.

(d) The POC model shall demodulate successive bursts independently.

(e) The POC model shall provide an indication of the start of valid data in real time.

(f) The POC model shall be implemented with advanced technology components which will be available within the time period of this contract. A technology possessing a potential improvement in performance, reliability, size, weight and/or power consumption is to be preferred to using an existing technology.

(g) Space-qualifiable components and materials shall be utilized in the POC model satellite demodulator design. Commercial equivalent parts may be used in the POC model hardware.

(h) The POC model shall be compatible with off-the-shelf

interface components at TTL and ECL logic levels.

(i) The POC model shall be separable and distinct from any test equipment so that the demodulator can be independently evaluated as a part of a larger transponder system.

3.2.2 Electrical and Performance Requirements

The POC model shall be designed to meet or exceed the following electrical and performance requirements:

(a) The minimum bandwidth efficiency shall be 2 bits/second/Hz.

(b) The maximum average symbol-energy to noise-power-density ratio (Es/No) for the specific modulation scheme used shall be within 2 dB of the required (Es/No) for the ideal theoretical case at a bit error probability of $5x10^{-7}$.

(c) The maximum time to acquire synchronization shall be 100 information bit times with a maximum probability of acquisition failure of 10^{-8}.

(d) The maximum unique word length used to indicate the start of valid data in real time shall be 20 bit times.

(e) Channel filtering and guard bands shall be selected to assure less than 1 dB of performance degradation due to adjacent channel interference when the adjacent channel power level is 20 dB higher than the desired channel.

(f) The POC model shall exhibit less than 1 dB of degradation in the bit error rate performance of 3.2.2 (b) when measured with a maximum ratio of desired signal to co-channel interferer of 20dB over the usable bandwidth.

(g) The minimum guard time between successive bursts from independent sources shall be 10 nsec.

(h) The minimum burst duty cycle shall be 1 burst/msec.

(i) The maximum burst rate instability shall be $\pm 5x10^{-7}$.

(j) The minimum mean time to cycle slip shall be four order of magnitude greater than the preamble duration when (Es/No) is 3-dB less than the operating (Es/No) specified in 3.2.2(b).

(k) The minimum data portion of a burst shall be equal in length to the preamble portion of a burst.

3.2.3 Electrical And Performance Parameters

POC model performance goals shall be established for the following electrical and performance parameters:

(a) bandwidth efficiency
(b) bit error rate performance

(c) time to acquire synchronization
(d) input signal power spectrum
(e) input noise power density
(f) channel nonlinearities
(g) frame efficiency
(h) envelope deviation
(i) probability of missed unique word detection
(j) burst-to-burst frequency variation
(k) power consumption

3.2.4 Environmental Design Objective

The POC model shall be designed for operation in a laboratory environment with an extended temperature range of 0^{o} to 50^{o}C. Any custom LSI or MMIC for direct application in the POC model or potential application in the engineering models shall be designed and tested in accordance with the Contractor's flight environment and qualification specifications.

3.5 Product Assurance Requirements

The following shall be performed by the development engineers and technicians in the normal course of their duties in the development of the POC model and not by Quality assurance staff.

3.5.1

An equipment log and continuous history of the fabrication, inspection, test, assembly and storage of the POC model shall be delivered with the hardware.

3.5.2

The Contractor shall inspect and document those characteristics that materially influence the integrity and performance of the POC model. Critical raw materials and parts shall be inspected and tested to determine conformance to applicable specifications and drawings. Reports of actual test results shall be kept in the equipment log.

3.5.3

Equipment and tools used in the acquisition of data shall be calibrated, maintained, and controlled to ensure their accuracy and reliability. Records on data acquisition equipment shall be kept in the equipment log.

3.5.4

The Contractor shall assemble the POC model using workmanship in accordance with Mil-Std 454, Requirement 9.

3.5.5

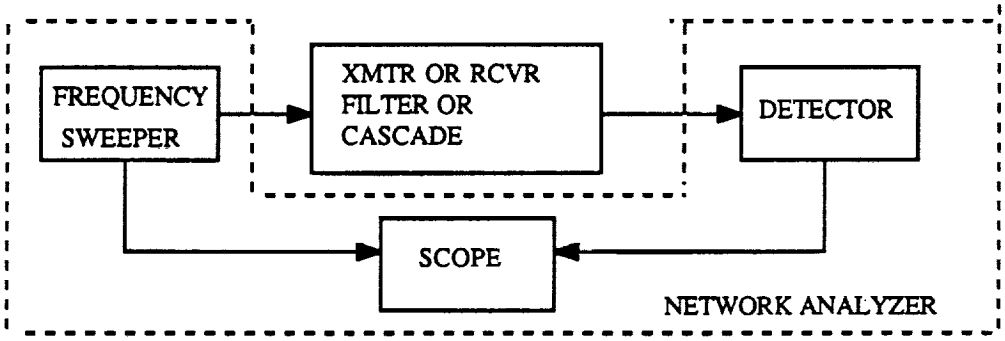
The Contractor shall prepare drawings for the POC model in accordance with the basic requirements of DOD-DI000B, Level 1 - Development design drawings.

3.5.6

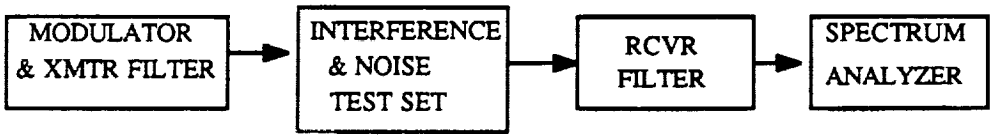
The Contractor shall prepare discrepancy documentation (report, analysis, corrective action and concurrence) for the POC model. Records on discrepancy documentation shall be kept in the equipment log.

PURPOSE:

The purpose of this test is to supply the data necessary to compute the bandwidth efficiency and verify that it exceeds the specification of 2 bits/sec/Hz. In addition, by direct measurement with the modulator and noise source the input signal power spectrum and noise spectral densities are recorded. The test setups are shown in Figure 1.



a. FREQUENCY RESPONSE OF XMTR AND RCV FILTERS



b. DETERMINATION OF SIGNAL AND NOISE SPECTRA

FIGURE 1. TEST SETUP FOR MEASURING FILTER RESPONSES AND SIGNAL AND NOISE SPECTRA

BANDWIDTH EFFICIENCY CALCULATION:

Define the following quantities:

raw data rate=200 Mbps

R=code rate=5/6

code symbol rate=raw data rate/R= 240 Msps

Fs=channel symbol rate=code symbol rate/(code symbols/channel symbol)=240 Msps/3=80 Msps

α=Nyquist filter rolloff constant=0.2

B=total RF bandwidth occupied by the signal=$(1+\alpha)$*Fs=1.2*80 MHz=96 MHz

Finally, using the required raw data rate and B, the bandwidth efficiency, η, can be computed as

η=raw data rate/ total required transmission bandwidth =200/96 = 2.08 bits/sec/Hz

The codec is not provided as part of the proof-of-concept hardware but is assumed to be present thereby raising the data rate from 200 to 240 Mbps yielding an 8PSK channel symbol rate of 80 Msps. Thus, the bandwidth efficiency goal can be said to be met provided that the BER performance is met and that the filter charactersistic is shown to approximately exhibit the Nyquist filter characteristic with α=0.2.

Ideally, the overall channel response for zero intersymbol interference (ISI) should exhibit the Nyquist raised cosine response with 6 dB bandwidth equal to the noise-bandwidth, B as shown in Figure 2. (Nyquist filters have linear phase.) In order for the transmitted waveform to be matched in the receiver and have the overall waveform exhibit the Nyquist characteristic, the transmitter and receiver filter impulse responses could both be made equal to the square-root of the raised-cosine overall characteristic if the transmissions were impulses. However, when the transmitter modulator waveform is a rectangular pulse rather than impulsive, it is necessary to include an inverse sinc function equalizing filter in the transmitter to maintain the waveform matching. The required responses of the receiver and transmitter filters for the rectangular pulse modulator are shown in Figure 3.

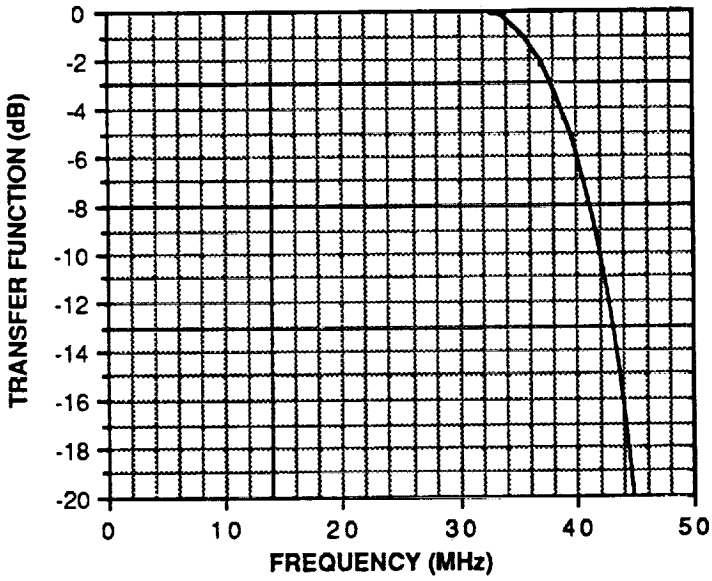


FIG.2 NYQUIST TRANSFER FUNCTION ALPHA=.2

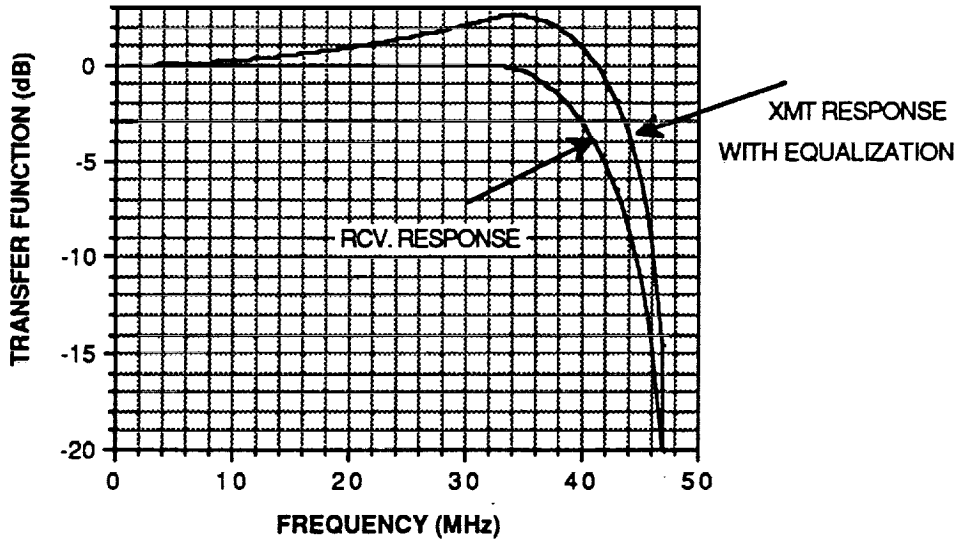


FIG. 3 NYQUIST FILTER RESPONSES ALPHA=.2

TEST PROCEDURE:

A. NYQUIST FILTER CHARACTERISTICS.

1. Connect the test equipment and filter under test as shown in Figure 1 (a). Place markers at the center of the band (fo=3.37056 GHz), at the nominal Nyquist cutoff points (fo+/-40 MHz), at the nominal "infinite" attenuation points (fo+/-48 MHz), and at the adjacent channel center frequencies (fo+/-96 MHz). Sweep out the amplitude characteristics over the nominal Nyquist cutoff bandwidth with 1 dB/ sensitivity and photgraph the trace. Increase the sweep to include fo+/-96 MHz with 5 dB/ sensitivity and photograph the trace. Perform this step for both the transmitter and receiver filters seperately.

2. With the markers set as indicated in step 1, photograph the group delay characteristics of each filter using appropriate scale sensitivities of ns/.

3. Repeat 1. and 2. with both filters connected in cascade.

B.SIGNAL AND NOISE SPECTRA

1. Connect the equipment as shown in Figure 1 (b). With the signal turned off and the noise turned on at the maximum level, record the noise power spectral density over the band of interest (fo+/-48 MHz). It should approximate the receiver response shown in Figure3.

2. With the noise turned off and the modulated signal turned on, record the signal power spectral density over the band of interest (fo+/-48 MHz). It should approximate the transfer function shown in Figure 2.

AMTD TEST PROCEDURE AND DATA SHEET # 2 BIT ERROR RATE TEST June 29, 1989

PURPOSE:

The purpose of this test is to verify the bit error rate (BER) performance of the modulation system in additive white Gaussian noise (AWGN). This is the basic test to demonstrate the complete functionality of the modulation system as well as demonstrate that its performance compared to theoretical is within the specified maximum degradation. It will measure the combined effects of AWGN, L.O. frequency error, and determine the effects of BER as a function of position within the TDMA burst and length of the averaging interval within the burst.

TEST SETUP AND EQUIPMENT REQUIRED:

The test setup and required equipment is shown in the block diagram of Figure 1.

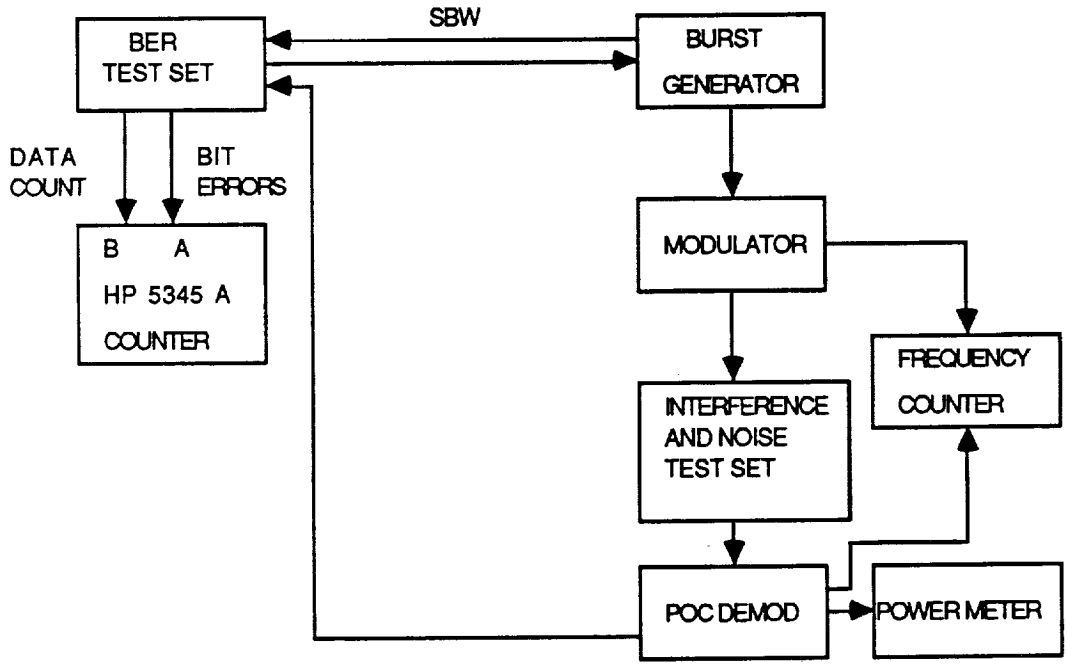


FIGURE 1. ARRANGEMENT OF MODULATION SYSTEM ELEMENTS FOR TESTING

TEST PROCEDURE:

1. Connect the system as shown in Figure 1. Adjust the frequency error between the modulator signal generator and the Demod L.O. to be less than +/- 1.5 kHz.

2. Set the BER Test Set for a burst length equal to a full 1ms frame.

3. With the adjacent channel interferers and AWGN sources turned off, adjust the signal power as measured at the output of the POC Demod bandpass filter to the nominal input level required to operate the Demod, -30 dBm.

4. Turn the signal source off and turn on the noise source. Adjust the noise power as measured on the power meter to the a level 10 dB below the nominal signal power set in step 3. Record the values of the variable attenuators in the noise path in the Interference and Noise Test Set.

5. Operate the modulation system in the normal burst mode format as shown in Figure 2 with the burst length of 8000 8PSK symbol times. With the sub-burst window (SBW) opened for 512 symbol times, set the HP 5345A gate time to be as shown in Table 1.

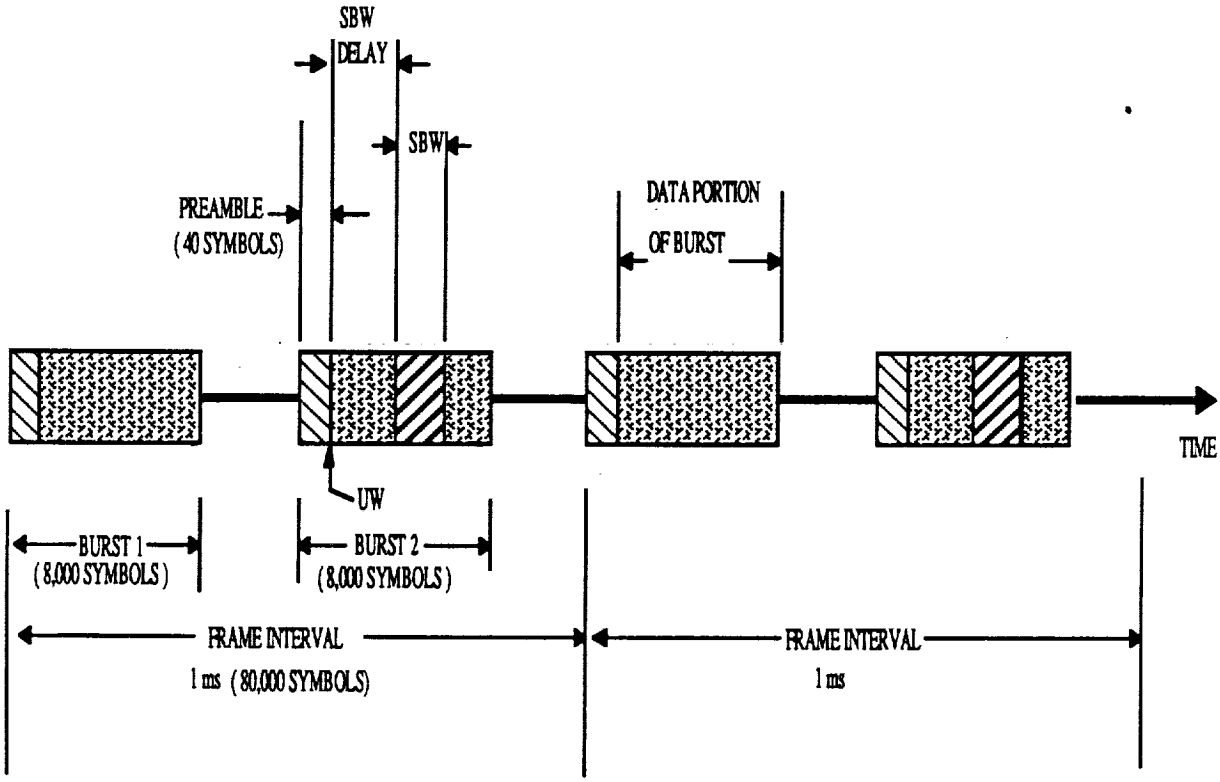


FIGURE 2 FRAME AND BURST STRUCTURE

6. Channel B of the computing counter accumulates the total data counts while channel A accumulates three times the error counts occurring during the SBW. The counter will display the ratio of the frequency in channel B (FB) to that in channel A (FA). The BER to a confidence of 99% of being between BER/2 and 2*BER is the reciprocal of 3*(FB/FA). Record FB/FA and the computed value of BER on the TEST DATA SHEET.

7. Increase the noise attenuator in 1 dB steps and repeat steps 5 and 6 until the point Es/No=20 dB has been measured.

8. Repeat steps 5, 6, and 7 for the SBW widths of 5,120 and 51,200.

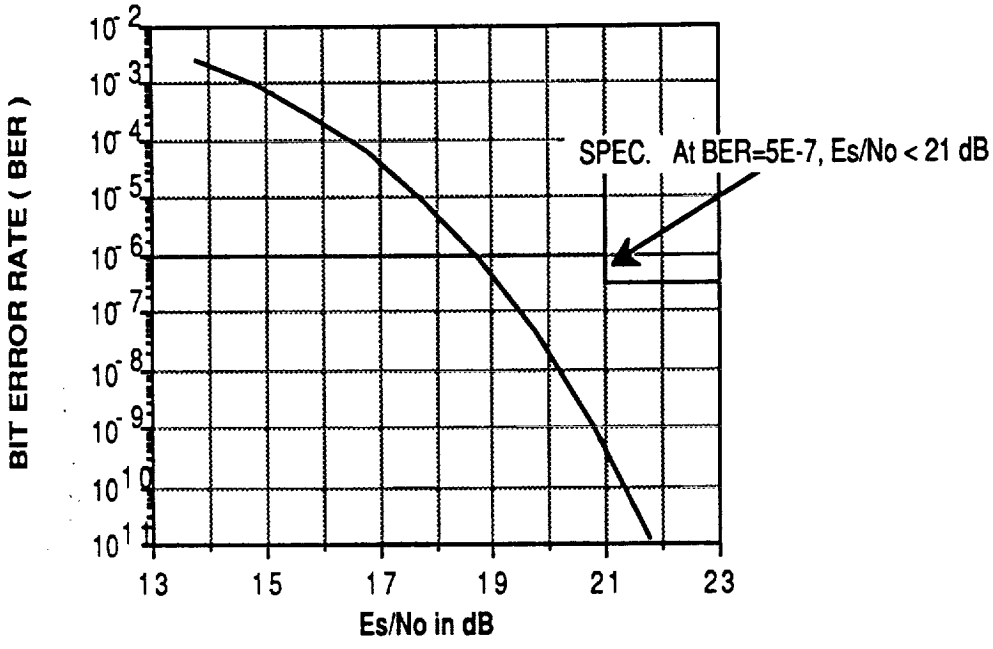
9. Repeat steps 5 through 8 for the following values of frequency error between the modulator signal generator and Demod L.O.: +/- 5 kHz, +/- 10 kHz, and +/- 20 kHz.

10. Plot recorded data on the curve in Figure 3.

Es/No (dB)	THEORET-ICAL BER	SBW=512 GATE TIME ON HP 5345	SBW=512 MEASURE-MENT TIME	SBW=5,120 GATE TIME ON HP 5345	SBW=5,120 MEASURE-MENT TIME	SBW=51,200 GATE TIME ON HP 5345	SBW=51,200 MEASURE-MENT TIME
10	2.9×10^{-2}	10 ms	3.2 s	1 ms	326 ms	100 us	33 ms
11	1.8×10^{-2}	10 ms	3.2 s	1 ms	326 ms	100 us	33 ms
12	1.0×10^{-2}	10 ms	3.2 s	1 ms	326 ms	100 us	33 ms
13	5.3×10^{-3}	100 ms	32 s	10 ms	3.2 s	1 ms	326 ms
14	2.2×10^{-3}	100 ms	32 s	10 ms	3.2 s	1 ms	326 ms
15	7.7×10^{-4}	100 ms	32 s	10 ms	3.2 s	1 ms	326 ms
16	2.1×10^{-4}	1 s	320 s	100 ms	32 s	10 ms	3.2 s
17	4.3×10^{-5}	10 s	3200 s (54 min)	1 s	320 s	100 ms	32 s
18	5.7×10^{-6}	100 s	9 hrs	10 s	54 min	1 s	320 s
19	4.7×10^{-7}	1000 s	90 hrs	100 s	9 hrs	10 s	54 min
20	2.1×10^{-8}						

TABLE 1 THEORETICAL BER AND REQUIRED GATE AND MEASUREMENT TIMES AT THEORETICAL PERFORMANCE FOR TEST RANGE OF Es/No AND THREE LENGTHS OF SBW
(In general, for BER greater than theoretical, measurement times will be less than indicated.)

Figure 3 Theoretical BER vs. Es/No



AMTD TEST PROCEDURE DATA SHEET VER 1.2 7/21/88

SHEET #:_____ DATA: __ / __ / 1988

NAME:_____ TIME: __ : __

TEST SETUP

QUADRATURE DEMODULATION: COHERENT / NON-COHERENT

ZERO TRACKING: ENABLED / DISABLED

FREQUENCY ERROR (XMTR AND QUAD DEMOD LO): _____KHz

BAUD CLOCK: HARDWIRED / RECOVERED

DATA SOURCE: MOD/BERT / TAU-TRON

DATA PN LENGTH: $2^{11}-1$ / $2^{7}-1$ / $2^{15}-1$ / $2^{20}-1$ / $2^{23}-1$

MODE: CONTINUOUS / BURST

SBW (RELATIVE) STARTING POSITION: _____HEX

MODULATION: 8-PSK / QPSK / BPSK

NOTES:_____

Es/No (dB)	THEORETICAL BER	SBW LENGTH B/A	SBW LENGTH BER	SBW LENGTH B/A	SBW LENGTH BER	SBW LENGTH B/A	SBW LENGTH BER
12	1.0×10^{-2}						
13	5.3×10^{-3}						
14	2.2×10^{-3}						
15	7.7×10^{-4}						
16	2.1×10^{-4}						
17	4.3×10^{-5}						
18	5.7×10^{-6}						
19	4.7×10^{-7}						
20	2.1×10^{-8}						
21							

PURPOSE:

This test has the following two purposes:

1. To verify that the degradation of the BER is less than 1 dB in the presence of adjacent channel interference (ACI) which is stronger than the desired signal by more than 20 dB.

2. To verify that the degradation of the BER is less than 1 dB in the presence of co-channel interference (CCI) which is weaker than the desired by less than 20.

TEST SETUP AND EQUIPMENT REQUIRED:

The test setup and required equipment is shown in the block diagram of Figure 1.

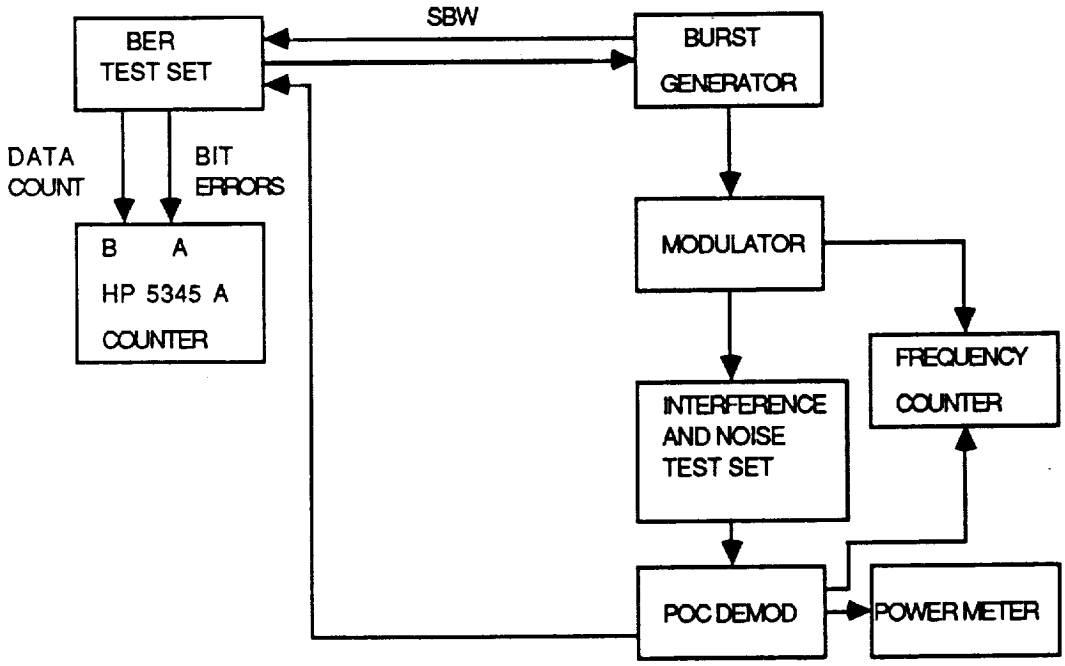


FIGURE 1. ARRANGEMENT OF MODULATION SYSTEM ELEMENTS FOR TESTING

TEST PROCEDURE:

1. Connect the system as shown in Figure 1. Adjust the frequency error between the modulator signal generator and the Demod L.O. to be less than +/- 1.5 kHz.

2. Set the BER Test Set for a burst length equal to 1 millisecond.

3. With the adjacent channel interferers and AWGN sources turned off, adjust the signal power as measured at the

output of the POC Demod bandpass filter to the nominal input level required to operate the Demod, -30 dBm.

4. Turn off the signal and noise and turn on the two ACI interferers. Adjust the center frequency of the interferers to be at fo +/- 96 MHz using the HP 8601A . Adjust the levels of the ACI into the power meter such that the total power measures 23 dB above the nominal signal power when the two interferers are equal. The spectral relationship between the desired and ACI will be as shown in Figure 2.

5. Repeat the BER test performed in the BIT ERROR RATE TEST and record the data on the data sheet.

6. Turn off the ACI, noise, and the signal.

7. Turn on the CCI and adjust its level on the power meter to be 20 dB below the nominal signal value. The spectral relationship between the signal and CCI is as shown in Figure 2 where the spectral overlap is not shown.

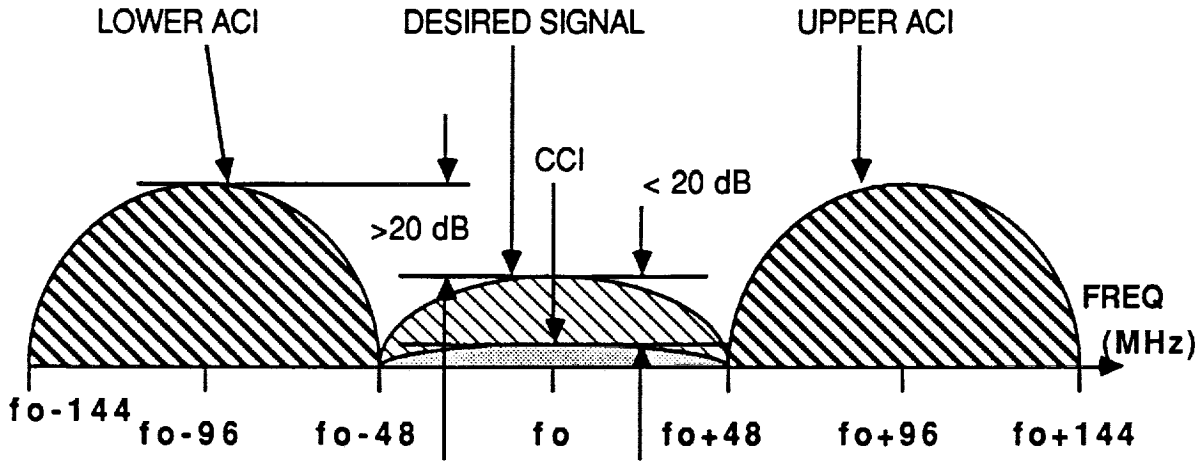


FIGURE 2. Relationship of power spectra of desired signals and interferers. fo=3373.056 MHz

11. Repeat the BER test performed in the BIT ERROR RATE TEST and record the data on the data sheet.

12. Plot the BER versus E_S/N_O for the data taken with CCI and ACI on Figures 3 and 4 respectively after superimposing the measured data of BER versus E_S/N_O with noise alone on both figures.

13. The degradation due to interference is determined by subtracting the value of E_S/N_O with noise plus interference from the value of E_S/N_O with noise alone at a BER of 5×10^{-7}.

		SBW=512		SBW=5,120		SBW=51,200	
Es/No (dB)	THEORET-ICAL BER	GATE TIME ON HP 5345	MEASURE-MENT TIME	GATE TIME ON HP 5345	MEASURE-MENT TIME	GATE TIME ON HP 5345	MEASURE-MENT TIME
10	2.9×10^{-2}	10 ms	3.2 s	1 ms	326 ms	100 us	33 ms
11	1.8×10^{-2}	10 ms	3.2 s	1 ms	326 ms	100 us	33 ms
12	1.0×10^{-2}	10 ms	3.2 s	1 ms	326 ms	100 us	33 ms
13	5.3×10^{-3}	100 ms	32 s	10 ms	3.2 s	1 ms	326 ms
14	2.2×10^{-3}	100 ms	32 s	10 ms	3.2 s	1 ms	326 ms
15	7.7×10^{-4}	100 ms	32 s	10 ms	3.2 s	1 ms	326 ms
16	2.1×10^{-4}	1 s	320 s	100 ms	32 s	10 ms	3.2 s
17	4.3×10^{-5}	10 s	3200 s (54 min)	1 s	320 s	100 ms	32 s
18	5.7×10^{-6}	100 s	9 hrs	10 s	54 min	1 s	320 s
19	4.7×10^{-7}	1000 s	90 hrs	100 s	9 hrs	10 s	54 min
20	2.1×10^{-8}						

TABLE 1 THEORETICAL BER AND REQUIRED GATE AND MEASUREMENT TIMES AT THEORETICAL PERFORMANCE FOR TEST RANGE OF Es/No AND THREE LENGTHS OF SBW
(In general, for BER greater than theoretical, measurement times will be less than indicated.)

CCI TEST DATA

DEGRADATION DUE TO CCI: E_S/N_O AT BER= 5 X 10^{-7} WITH NOISE PLUS CCI ..... dB (a)

E_S/N_O AT BER=5 X 10^{-7} WITH NOISE ALONE ..... dB (b)

DEGRADATION (a) minus (b) ..... dB

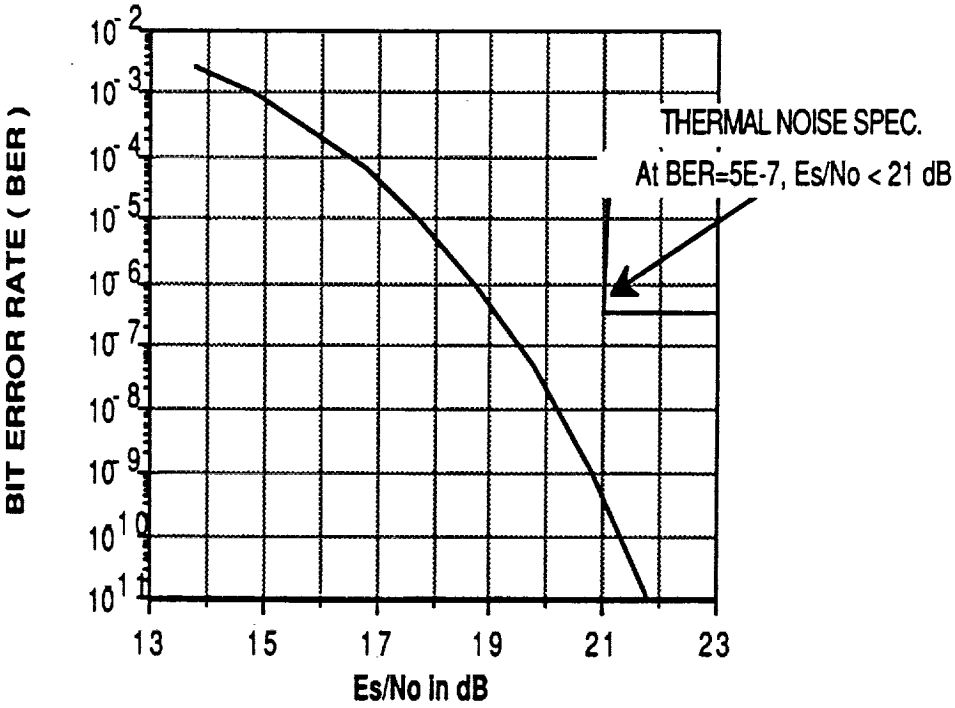


FIGURE 3. Theoretical BER versus E_S/N_O. Superimpose test data for both noise alone and for noise plus 20 dB CCI.

ACI TEST DATA

DEGRADATION DUE TO ACI: E_S/N_O AT BER= 5 X 10^{-7} WITH NOISE PLUS ACI ..... dB(a)

E_S/N_O AT BER=5 X 10^{-7} WITH NOISE ALONE ..... dB(b)

DEGRADATION (a) minus (b) ..... dB

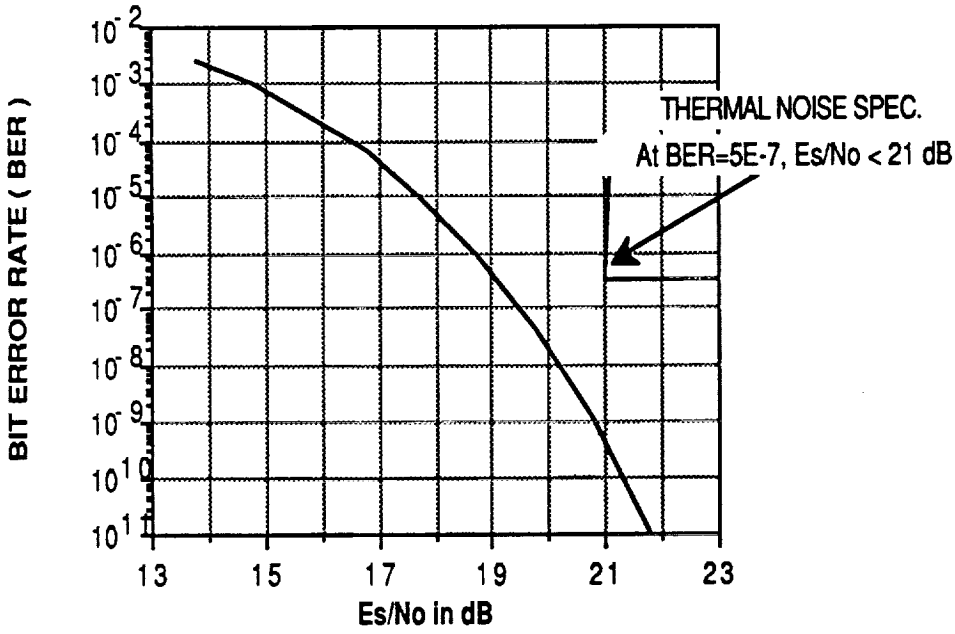


FIGURE 4. Theoretical BER versus E_S/N_O. Superimpose test data for both noise alone and for noise plus -20 dB ACI.

APPENDIX E

AMTD TEST PROCEDURE AND DATA SHEET #6 BIT TIMING JITTER TEST June 29, 1989

PURPOSE:

The purpose of this test is to verify that the jitter on the recovered symbol clock is less than the maximum specified value. The jitter on the recovered clock is due to a combination of factors including additive white Gaussian noise (AWGN), quantizing errors, and the pattern noise inherent in the random nature of the detected baud transitions (DBT). The DBT is the "signal" from which the 80 MHz clock must be recovered.

TEST SETUP AND EQUIPMENT REQUIRED:

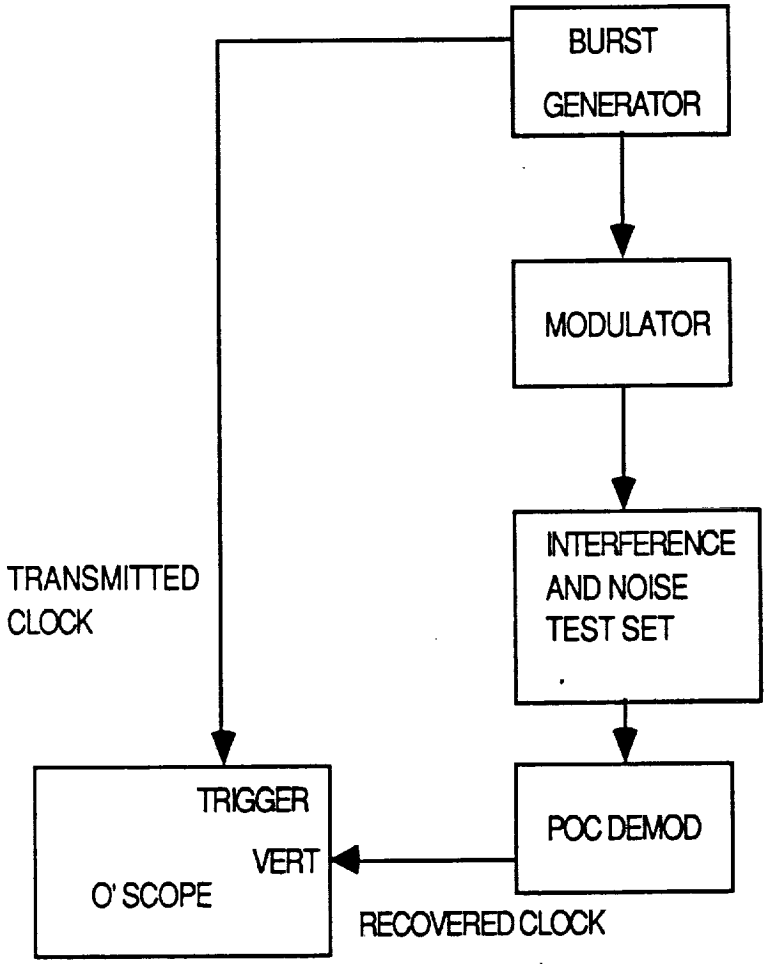


FIGURE 1. ARRANGEMENT OF MODULATION

SYSTEM ELEMENTS FOR TESTING

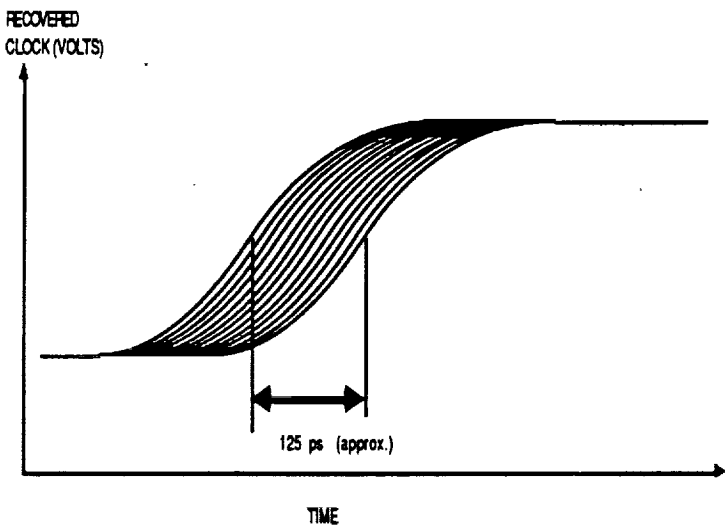


FIGURE 2 OSCILLOSCOPE DISPLAY OF RISING EDGE OF RECOVERED CLOCK

TEST PROCEDURE:

1. Connect the system as shown in Figure 1.

2. Turn the signal source on with the data in the continuous mode.

3. Adjust the Es/No to 10 dB as described in the BIT ERROR RATE TEST procedure.

4. Observe the oscilloscope trace of the leading edge of the reconstructed clock as shown in Figure 2 as the trace is being triggered externally by the transmitter 80 MHz clock. Measure the width of the trace at the half-height point and record on the test data sheet.

5. Repeat the measurement in step 4 for values of Es/No in 2 dB increments up to and including 22 dB.

Es/No (dB)	WIDTH OF TRACE (ps)
10	.....
12	.....
14	.....
16	.....
18	.....
20	.....
22	.....

BER Due to Unique Word Errors in AMTD

S. Ames

June 27, 1988

The original AMTD concept embodied a distributed unique word (UW) where only a portion of the UW would be transmitted in each burst. If N is the number of bits in the UW, it would require N bursts to transmit the complete word. The purported advantage of this scheme was that a more efficient TDMA frame would result since the overhead bits allocated to the UW in each burst would be reduced. Data timing in the TDMA frame is related to the UW correlation peak which must be detected in a particular baud slot. This being the case, each bit of a distributed word would need to be gated into the UW correlator at a precise time which effectively requires a complete UW in each burst. The original AMTD proposal also suggested using the UW for a signaling function whereby three UW bits could be transmitted in each burst to signal that the ground station was about to retard or advance the burst within the frame but this function can be performed better by other means.

The original AMTD spec as it appears in the SOW allocates eight baud slots to the UW and it has been decided to implement the non-distributed UW in the POC model. Thus, the full UW will appear in each burst in the eight slots immediately following the 32 all zeros symbols. The UW symbols will be clocked out of the demodulator into a digital correlator which consists of a tapped shift register with a modulo-2 adder on each stage. The second input to the mod-2 adder is the bit of the UW word code. To reduce the probability of a missed detection, a number of errors, E, are allowed in the correlator output. Thus its output is applied to a threshold which requires at least (N-E) of the UW bits to be correct before declaring the UW as present. Also, to prevent the spurious generation of UW correlations due to random data, the arrival of a UW is windowed by a gate which spans the expected location of the correlation peak to within plus or minus one or more baud slots. The span of the windowing gate is W slots. The concept of the UW and its detector is shown in Figure 1.

The analysis of the UW probability of missed detection and false alarm is given in reference 1. For a probability of an individual bit error equal P, the reference gives the probability of UW missed detection, Q, and the probability of false alarm, F, as

$$Q = \sum_{I=E+1}^{N} C_I^N P^I (1-P)^{N-I} = I_p(E+1, N-E) \quad (1)$$

$$F = \sum_{I=0}^{E} C_I^{N/2} P^{N/2+I} (1-P)^{N/2-I} = P^{N/2}\left(1 - I_p(E+1, N/2-E)\right) \quad (2)$$

where $I_p(a,b)$ is the incomplete beta function. The approximation for the probability of a false alarm of the windowed UW is given in ref. 1 as $F \cdot W$. If the UW is missed the entire burst is lost. Similarly, if a UW false alarm occurs the TDMA expansion buffer is filled with garbled data. The effect on the overall bit error rate (BER) from both events is the same and is expressed as

BER = $(Q + F \cdot W) \cdot$ (ave. no. of bits per burst)$\cdot$ (ave. no. of bursts per frame)$\cdot$ 0.5/(ave. no. of bits per frame)$=(Q + F \cdot W) \cdot 0.5$ (3)

The BER was computed using equations 1-3 with the results given in Figure 2. It is known that the minimum value of $\frac{E_s}{N_0}$ that the AMTD will see is about 12.6 dB (reference 2). Although the data modulation is 8-PSK, the modulation of the UW may be QPSK, or BPSK. These candidate modulations have a probability of bit error, P, corresponding to $\frac{E_s}{N_0}$

=12.6 dB of 7.7×10^{-10} for BPSK and 1.0×10^{-5} for QPSK.

The bit error rate, P, is that due to the effects of noise on individual bits as distinguished from the BER which results from UW errors. It is desirable that the BER due to UW errors be small compared to P so that there is very small degradation of the system performance due to the former. Since the specified bit error rate of AMTD is 5×10^{-7} and the contribution due to UW errors is thus set to a maximum of 1×10^{-7}.

When evaluating equation (3), the component Q and $F \cdot W$ were evaluated separately and it was noted that for values of E, N, and W of interest, the miss probabilty, Q, dominated the false alarm probability, $F \cdot W$ by at least several to many orders of magnitude. Thus Figure 2 is essentially the BER due to Q alone. By inspecting the graphs, we conclude that for the values of P no larger than 1.0×10^{-5}, the codes of length 8 or 16 with even one error allowed are sufficient to guarantee a low enough BER contribution due to a UW miss.

The UW codes which will be used are Neuman-Hofman sequences selected from Table 14-4, Reference 3, P.451.

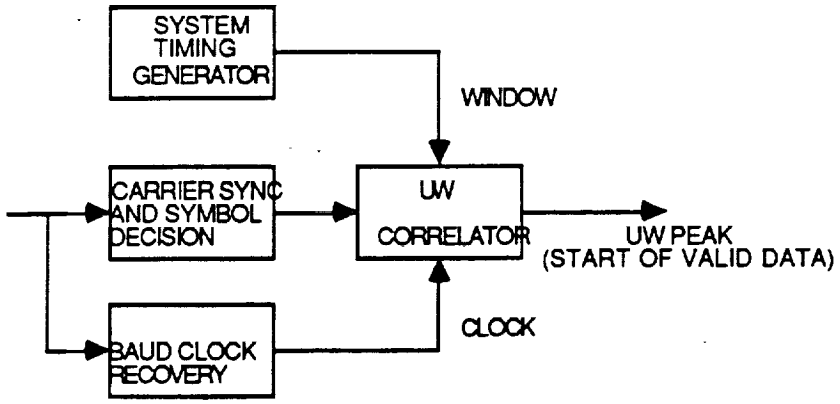
EIGHT BIT CODES: 00001101 or 00011101
SIXTEEN BIT CODES: 0000011001101011 or

0000111011101101

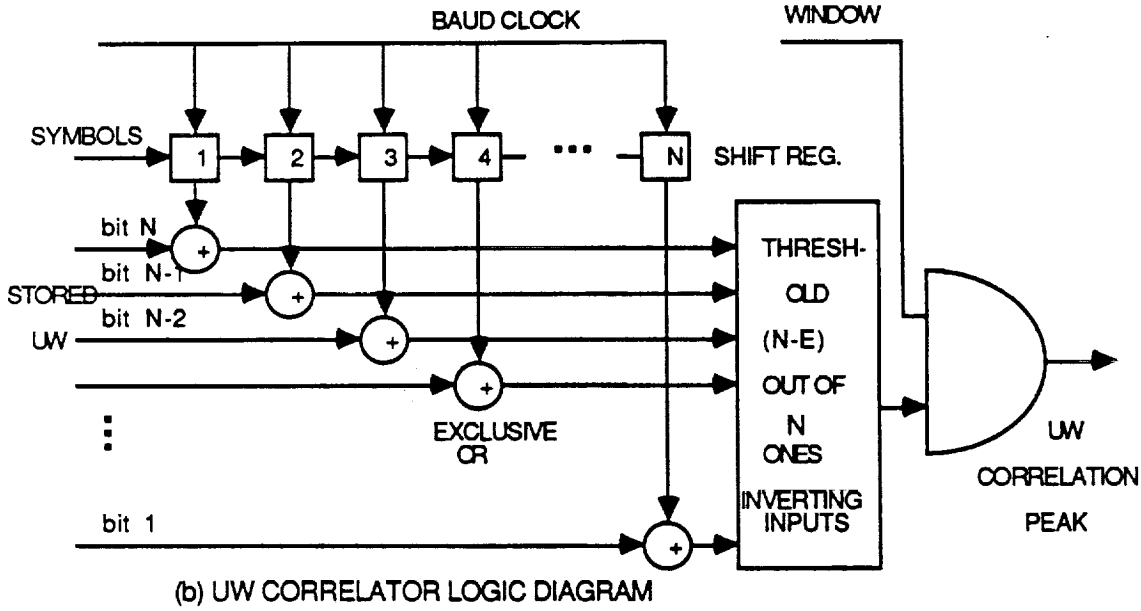
1. Feher, K., Digital Communications: Satellite/Earth Station Engineering, Prentice-Hall 1983, pp.375-384

2. "Advanced Modulation Technology Development", Independent Research and Development Report, 5 Feb. 1986.

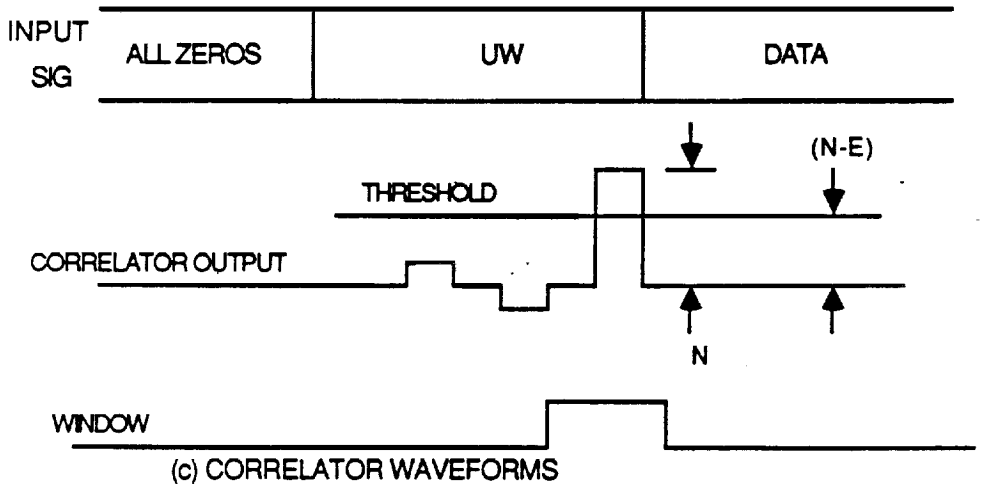
3. Spilker, J. J., Digital Communications by Satellite, Prentice-Hall 1977 pp. 450-452.



(a) TDMA DEMOD BLOCK DIAGRAM



(b) UW CORRELATOR LOGIC DIAGRAM



(c) CORRELATOR WAVEFORMS

FIGURE 1 UW CORRELATOR CONCEPT

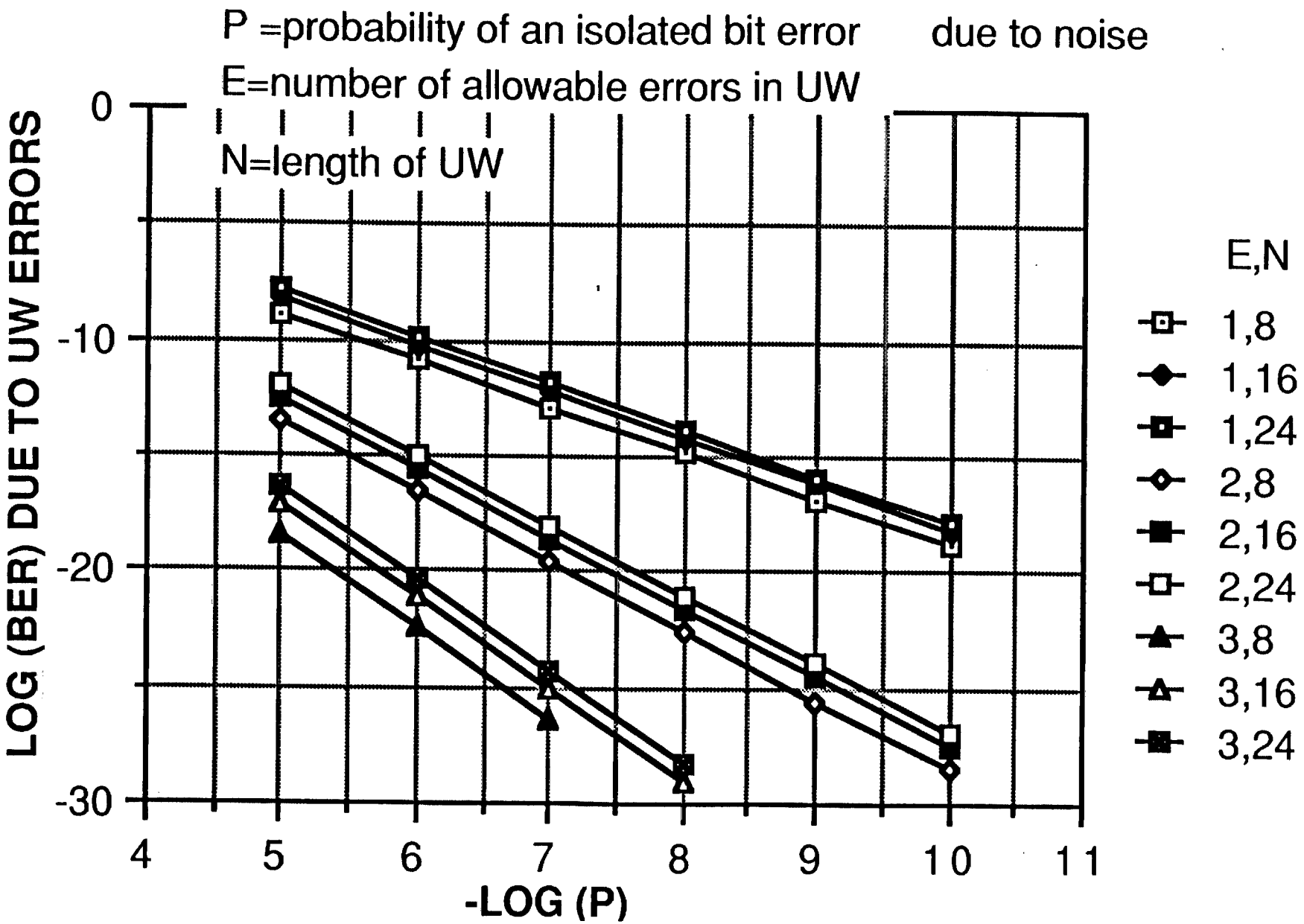


Figure 2 BER DUE TO UW ERRORS VS. P

APPENDIX G

AMTD ASIC

by R. Govea

A large part of the circuitry comprising the AMTD Demodulator is implemented in discrete integrated circuits from the 100K ECL family. For purposes of size, weight, and power reduction it is desirable to seek a higher level of integration for these circuits; the most cost-effective technology to accomplish this end is the high-speed gate array. This format allows reasonable integration of digital functions coupled with the low cost inherent to standard gate array offerings.

To gauge the scope of such an effort, a simple translation from discrete to gate array formats has been performed in Table 1. The Raytheon ECL gate array line was chosen as a target. To develop an equivalence, each of the ECL integrated circuits used in the AMTD POC Model was analyzed and converted to the Raytheon MAPS complexity measure. MAPS (Minimum Addressable Placement Sites) nomenclature is roughly equivalent to gate count in a CMOS ASIC; Raytheon currently offers arrays with 7696 and 4620 MAPS capacity, and will soon release a new array of around 14,000 MAPS capacity.

Having developed the MAPS equivalent to the 100K ECL family members, it is a simple matter to count the POC IC counts and convert to MAPS. The results, however, must be evaluated in light of several caveats. First, the 100K to MAPS conversion is only approximate, based on Raytheon-supplied macro functions. Second, the MAPS equivalents have limited internal fanouts and may not interconnect as easily as the 100K parts. Third, the topology of the Raytheon array, coupled with the specific AMTD circuitry, may not make optimum use of the array. Although these and other factors cannot be resolved without extensive design efforts, even a doubling of the MAPS complexity would still permit the AMTD digital circuits to be integrated on two ASIC chips (at a rough cost of $100K/chip for the Raytheon foundry effort).

Another consideration is that the use of a gate array implementation brings a new set of design options not available in 100K logic family standard parts. Using a gate array, new and more efficient circuit implementations may be applicable to the system architecture, a process which probably will reduce MAPS count, reduce power, and increase reliability. While it was convenient to scope the conversion of discrete to ASIC by translating the existing IC-based design, a gate array development program should include some time to optimize the circuit design approach and evaluate alternate implementations which fully exploit the capabilities of an all-integrated solution.

Several areas of investigation are already evident. The first lies in the Lookup Table (LUT), currently a cumbersome and power consuming 4Kx16 RAM. It may be possible to implement a combined memory/interpolator within one ASIC chip; use of a hardware interpolator reduces the memory requirement to a level easily implemented in a gate array. The second lies in the Clock Recovery circuitry, where alternate implementation approaches may reduce the burst-to-burst tracking requirement (easing ground stability tolerances) while maintaining performance levels.

In summary, the path to upgrade the AMTD Digital Demodulator is both clear and unobstructed. Estimates indicate that the existing circuit elements will readily fit into commercially available gate arrays, and provide performance exceeding the discrete design. There is an opportunity to improve on the current design with low risk. Finally, there is every expectation that a gate array design would satisfy a number of short- and long-term questions about the reliability, size, power, cost, and producability of digital demodulator designs.

Table 1 AMTD Gate Equivalence

6/29/89

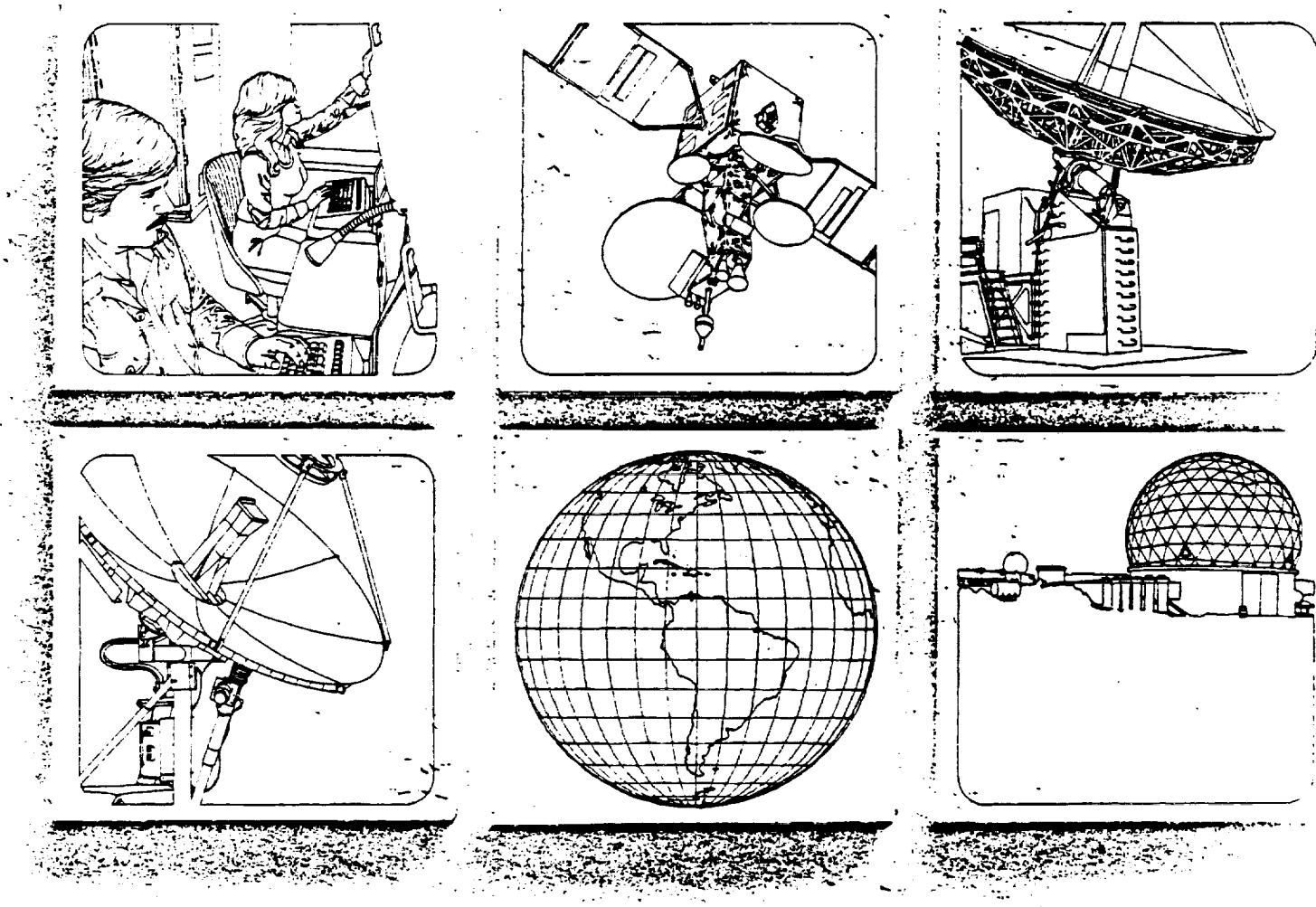
		Clock Gen		Input Mux		Baud Calc		Frame Count		Baud Acq	
ECL Part	MAP Equiv	IC Count	MAP Equiv	IC Count	MAP Equiv	IC Count	MAP Equiv	IC Count	MAP Equiv	IC Count	MAP Equiv
101	15		0		0		0	2	30		0
102	15	2	30		0	7	105	3	45	1	15
107	15		0		0	1	15	3	45		0
113	20	4	80	1	20	1	20	3	60		0
114	30	1	30	3	90	4	120	1	30	3	90
122	27	3	81	2	54	3	81	1	27	7	189
131	21		0		0		0	5	105	1	21
136	80	2	160		0		0	7	560		0
141	96		0		0		0	4	384		0
151	42		0	3	126	16	672	3	126	25	1050
155	24		0	3	72		0	4	96	6	144
166	35		0		0		0	8	280		0
170	20		0	1	20		0		0		0
171	24		0		0	6	144	1	24		0
180	80		0		0	8	640		0	14	1120
182	56		0		0		0	1	56		0
			381		382		1797		1868		2629

AMTD

POC DEMODULATOR

SYSTEM DOCUMENTATION

BURST GENERATOR
OPERATIONS / SPECIFICATION



Ford Aerospace/Space Systems Division

AMTD

POC DEMODULATOR

SYSTEM DOCUMENTATION

BURST GENERATOR
OPERATIONS / SPECIFICATION

SEPTEMBER 13, 1988

VER 5.2
8-24-88

OPERATIONS MANUAL

BURST GENERATOR

(AMTD)

TABLE OF CONTENTS

1. GENERAL DESCRIPTION

The Burst Generator's function is to take a serial data stream operating at 240 MBPS (Mega-bits per second) and format it into a burst of data with an appropriate preamble at 80 MSPS (Mega-symbols per second).

The Burst generator will produce a frame which is 1mS in duration and may contain either one or two bursts depending on the configuration. Each burst is completely flexible in its construction of preamble, including number of zeros and definition as well as existence of a unique word. The number of data symbols sent for each burst is also programmable.

The Burst Generator requires at least one 240 MHz data/clock source in order to operate. The Burst Generator will multiplex the source internally in order to produce two separate but coherent bursts. If two non-coherent burst are desired then two independent 240 MHz data/clock sources must be provided.

The Burst Generator may also be placed in a continuous mode to facilitate system baseline testing. This may be accomplished from a front panel control switch. The user may select continuous data from Data 1 or Data 2. This choice is irrelevant if only a single data/clock source is being utilized.

2. FRONT PANEL

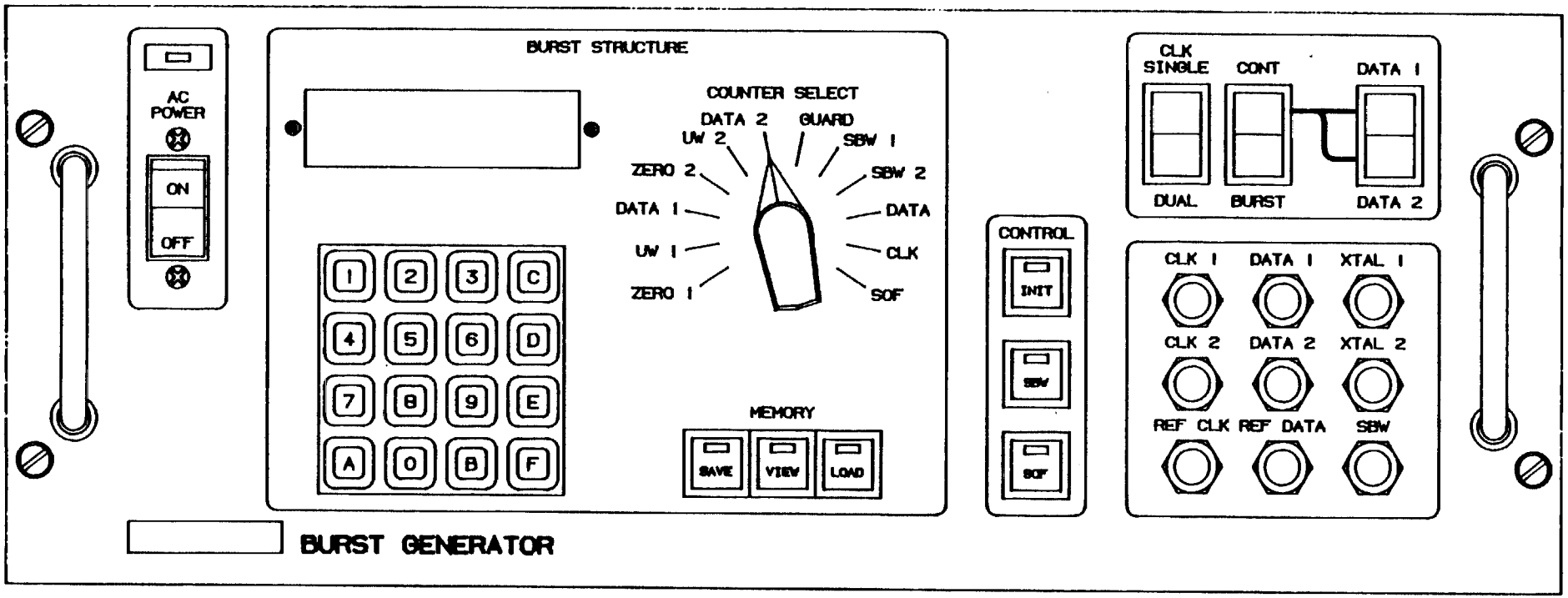
The front panel, shown in Figure 1, consists of five main functional groups: AC power, Burst Structure, Control, Configuration, and Connecter interface.

2.1. AC POWER The AC power group consists of the circuit breaker and the "power on" LED indicator.

2.2. BURST STRUCTURE The Burst structure group consists of the LED display, Hexadecimal keypad, Counter Select switch and Memory control. (See Figure 2).

2.2.1. LED Display - Five digit hexadecimal display.

2.2.2. Hexadecimal Keypad - Used to enter values into the various counters / registers. Because of the way the counter logic was implemented all values loaded into the counters are effectively incremented by one by the counter hardware. This should be taken into account by the user when



A00022
AMTD
LEVEL 50

FIGURE 1

BURST GENERATOR
FRONT PANEL

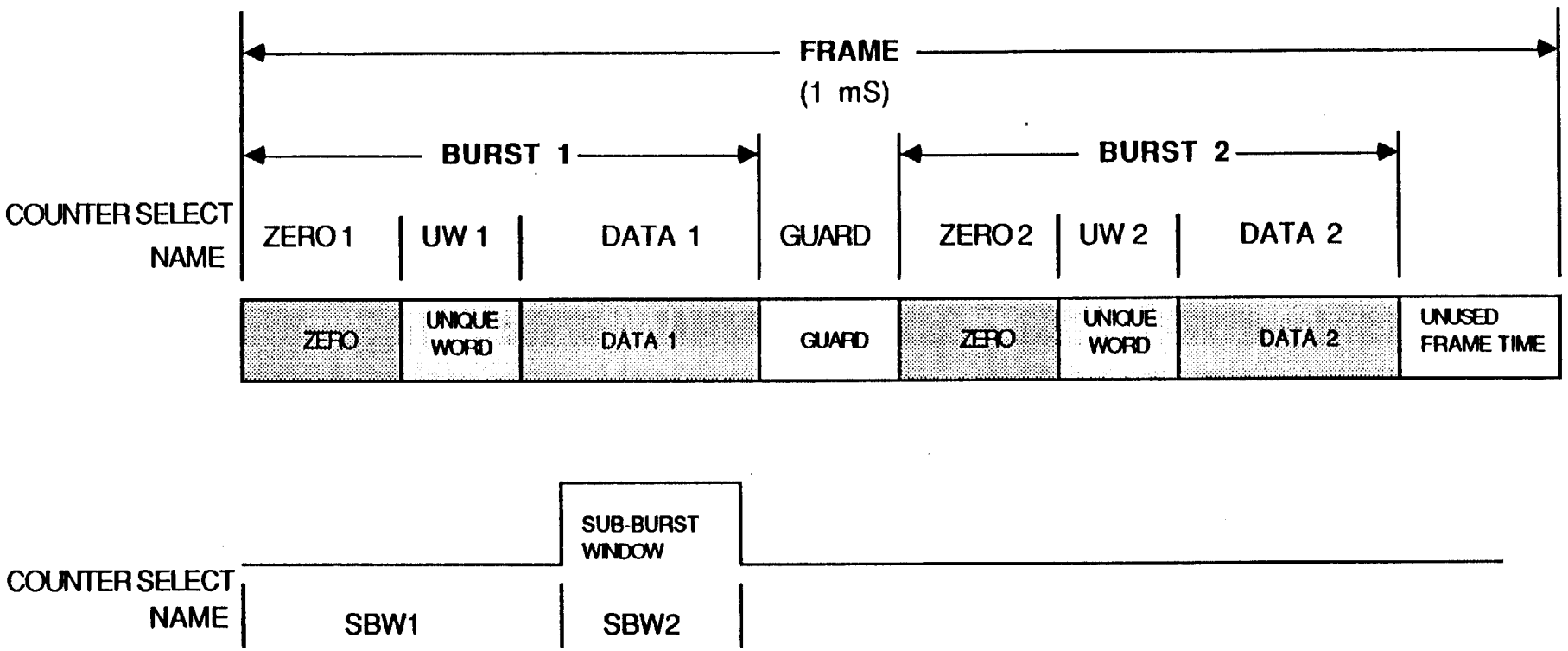


FIGURE 2

BURST STRUCTURE

loading values into the counters.

Example: Fred would like Burst 1 to contain 32 zero symbols in its preamble. In order to do this he would need to load 1FH (31) into the ZERO 1 counter. The Burst 1 zero counter logic would "add" an extra count to the 1FH (31) to give the desired 20H (32) number of zeros.

2.2.3. Counter Select - Allows the user to select one of twelve counters (See Table 2.2.3):

ZERO 1 - Burst 1 zero counter. ZERO 1 controls the number of zero symbols transmitted at the beginning of Burst 1.

Min Value: 1H
Max Value: FFH

UW 1 - Burst 1 Unique Word counter. UW 1 determines whether a unique word will be transmitted. If UW 1 is set to 7H then an eight symbol unique word will be sent following the Burst 1 zero symbols. If UW 1 is set to 0H then a unique word will not be transmitted. Values between 0H and 7H should be avoided since they will cause partial unique words to be transmitted.

Min Value: 0H
Max Value: 7H

DATA 1 - Burst 1 Data counter. DATA 1 controls the number of data symbols transmitted following the Burst 1 preamble. Because the data counter logic contains a 20 bit counter it is possible to load values greater than 13880H (80,000) into the counter. If this should occur the "excess" data symbol counts are ignored and the 1 mS / 80,000 symbol frame structure is kept intact.

Min Value: 0H
Max Value: 13880H - (ZERO 1 + UW 1 + 2)

ZERO 2 - Burst 2 zero counter. ZERO 2 controls the number of zero symbols transmitted at the beginning of Burst 2.

Min Value: 1H
Max Value: FFH or 13880 - (ZERO 1 + UW 1 + DATA 1 + GUARD + 4)
(Whichever is smaller)

UW 2 - Burst 2 Unique Word counter. UW 2 determines whether a unique word will be transmitted. If UW 2 is set to 7H then an eight symbol unique word will be sent following the Burst 2 zero symbols. If UW 2 is set to 0H then a unique word will not be transmitted. Values between 0H and 7H should be avoided since they will cause partial unique words to be transmitted.

Min Value: 0H
Max Value: 7H

DATA 2 - Burst 2 Data counter. DATA 2 controls the number of data symbols transmitted following the Burst 2 preamble. Because the data counter logic contains a 20 bit counter it is possible to load values greater than 13880H (80,000) into the counter. If this should occur the "excess" data symbol counts are ignored and the 1 mS / 80,000 symbol frame structure is kept intact.

Min Value: 0H
Max Value: 13880H - (ZERO 1 + UW 1 + DATA 1 + GUARD + ZERO 2 + UW 2 + 6)

GUARD - Guard time counter. Guard controls the amount of time between the end of Burst 1 and the beginning of Burst 2. The Guard time is selected in 12.5 nS increments. If Burst 1 and Burst 2 are non-coherent the exact Guard time between the bursts will vary.

Min Value: 1H
Max Value: 1FH

SBW1 - Start Sub-burst Window counter. The Sub-burst Window enable signal is controlled by two twenty bit counters. The first counter, SBW1, controls when the Sub-burst window will be asserted. It is based on the symbol (80MHz) clock and is timed from the beginning of the frame. When positioning the Sub-Burst Window enable signal within the burst for BERT testing it must be kept in mind that SBW1 is referenced from the start of frame in the Burst Generator and not the beginning of the frame as it arrives at the BERT. The difference between these two events is the delay in the system which includes the Modulator, Filters, Interference and Noise Generator, and the Demodulator.

Min Value: 1H

Max Value: 13880H

SBW2 - Duration of Sub-burst Window counter. SBW2 controls the length of time that the Sub-burst Window signal is asserted. SBW2 is based on the symbol (80MHz) clock and is timed from the end of SBW1.

Min Value: 1H
Max Value: 13880H - (SBW1 + 1)

EXAMPLE: Fred Nasa wants to count errors for a 512 symbol time period 50 symbols after Burst 1's unique word. Fred currently has the counters loaded with the following values:

Counter	Hex	Decimal
ZERO 1	1F	31
UW 1	07	7
DATA 1	1F40	8,000
GUARD	5	5
ZERO 2	1F	31
UW 2	07	7
DATA 2	1F40	8,000

In order to calculate the correct value for SBW1 Fred will have to determine the system delay time and convert it to symbol time periods (see Figure 3). Fred finds out from Steve Ford that the system delay is 223 nS. Fred uses the following formula to calculate the contents of SBW1:

SBW1 = Frame offset + Delay

where

Frame offset = total number of symbols from start of frame to the position where error counting is to begin.

Delay = RND(system delay / 12.5 nS)

In Freds case:

Frame offset = ZERO 1 + UW 1 + 50 + 2

where the 50 represents the position in the data portion of Burst 1 that Fred wants to begin error testing and the 2 compensates for the extra count that occurs in ZERO 1 and UW 1. (see 2.2.2)

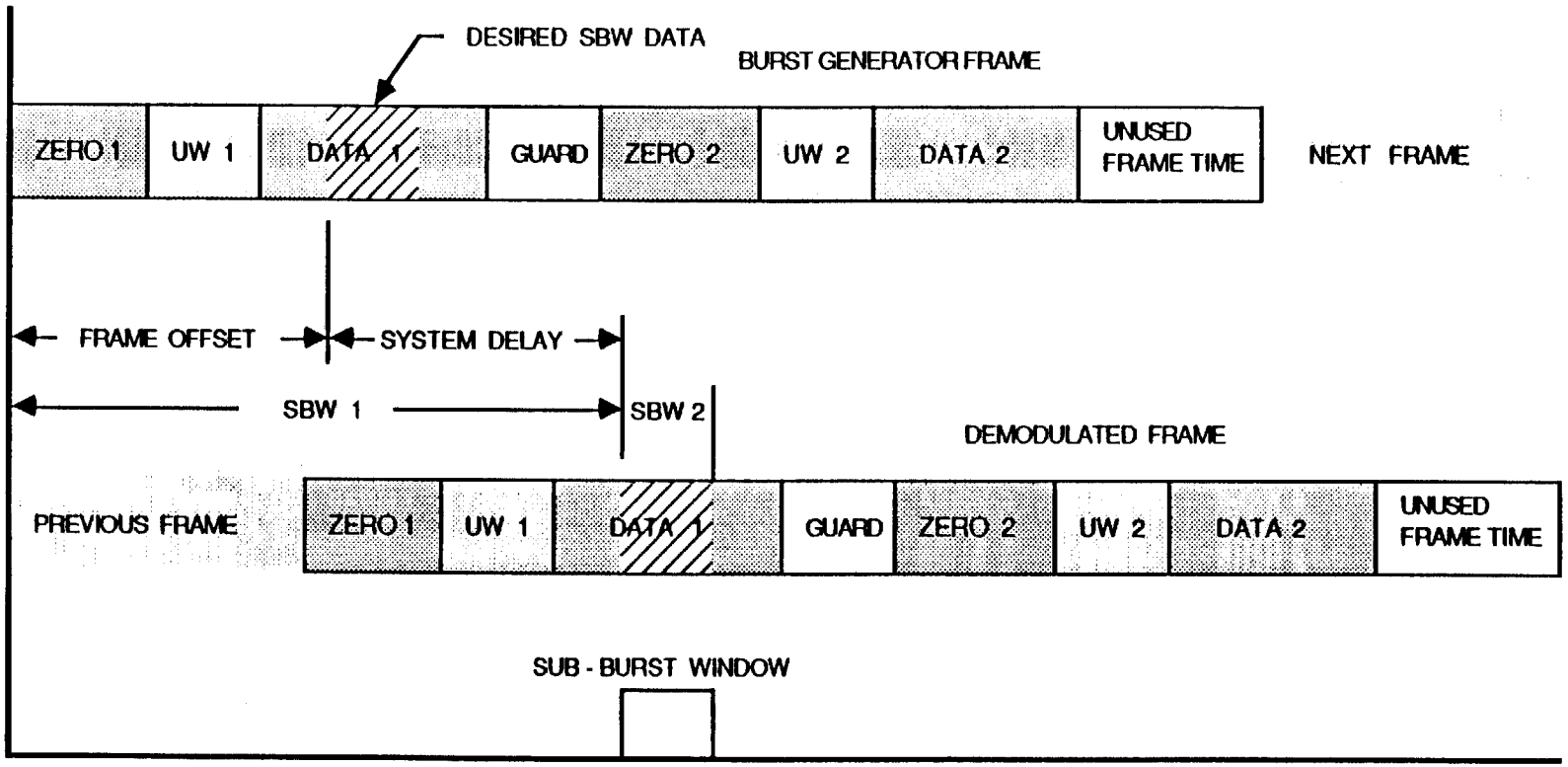


FIGURE 3
SUB-BURST WINDOW
CALCULATION

Frame offset = 31 + 7 + 50 + 2 = 90

Delay = RND(223 nS / 12.5 nS) = 18

and

SBW1 = 90 + 18 = 108

So Fred would need to load SBW1 with 6CH and SBW2 with 200H in order to perform error counting on Burst 1 starting with the 50th data symbol following unique word 1 and lasting for 512 data symbols.

TABLE 2.2.3

COUNTER	MINIMUM	MAXIMUM	TYPICAL
ZERO 1	1	FF	1F
UW 1	0	07	07
DATA 1	0	13880	1F40
GUARD	1	1F	02
ZERO 2	0	FF	1F
UW 2	0	07	07
DATA 2	0	13880	1F40
SBW1	1	13880	0300
SBW2	1	13880	0200

DATA - Delay Reference Data register. DATA controls the digital delay used to delay the reference data. The Reference Data may be delayed in 4 nS steps from approximately 0 nS to 128 nS.

Min Value: 0H
Max Value: 1FH

CLK - Delay Digital Modulator Clock register. CLK controls the programmable delay used to adjusted the 80 MHz symbol clock that is utilized by the digital modulator. This allows the user to align the clock and data at the modulator input latch. The delay is adjustable in 0.75 nS steps with a maximum delay of approximately 165 nS.

Min Value: 0H
Max Value: FFH

SOF - Delay Start of Frame register. SOF controls the programmable delay used to delay the Start of Frame signal that is transmitted to the Demodulator. This adjustable delay is used to align the Start of Frame signal with the arrival of the I and Q data at the demodulator and thus compensate for the delay caused by the modulator and Quadrature detector. SOF delay is identical to the CLK delay in function and implementation.

2.2.4. MEMORY CONTROL - The Burst Generator contains the Intel 2001 1K Non-Volatile Random Access Memory (see Figure 4). The Intel 2001 actually contains 1K of RAM which is mirrored by 1K of EEPROM. Each time the user performs an operation with one of the counters or registers a copy of the data is written to the RAM. Before power down the user may choose to permanently save these values in the EEPROM. The 2001 has a 10,000 Non-Volatile Store life cycle. The Memory control allows the user to perform the following functions:

SAVE - When the SAVE switch is asserted the current contents of the Intel 2001 RAM are stored in the non-volatile Intel 2001 EEPROM.

VIEW - Allows the user to view the current value in a counter or register. Each time a value is loaded into a counter / register it is also written to the Intel 2001 RAM. When VIEW is asserted the value in the scratch RAM is displayed to the user and is reloaded in the ECL hardware to insure that the user is actually viewing what is in the counter / register. On power up it is necessary to initialize all the counters and registers. At power up the contents of the Intel 2001 EEPROM is automatically loaded into the RAM. If the user wants to use the values from the EEPROM, the user may simple "VIEW" each counter/register, which will cause the value for that counter/register to be transferred from the NVRAM into the counter/register and to the LED display.

LOAD - Allows the user to load a value from the hexadecimal keypad into a counter/register selected by the Counter Select switch. A copy of the value is also loaded into the scratch RAM for use by the SAVE and VIEW commands.

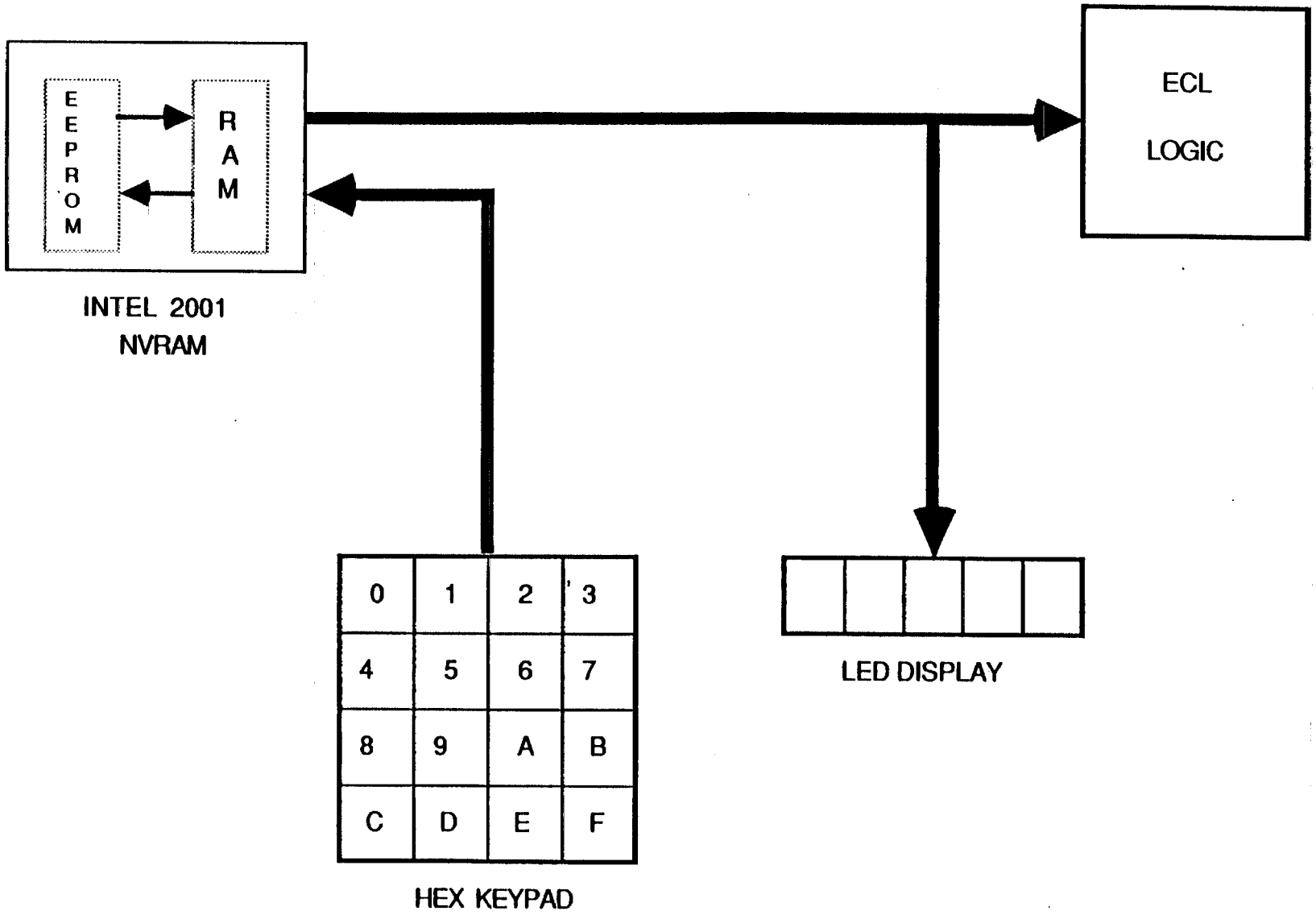


FIGURE 4

DATA INTERFACE

2.3. CONTROL Allows the user to control the operation of the Burst Generator in the following manner:

INIT - Allows the user to suppress the symbol (80MHz) clock to the counters while they are being loaded. INIT is asserted at power up and must be deasserted in order for the Burst Generator to operate. It is possible to load the various counters and registers without placing the Burst Generator in the INIT mode, but the user runs a small risk of obtaining unpredictable results during the one frame when the new value is entered. When the INIT LED is on, INIT is asserted.

SBW - Sub-Burst Window allows the user to count errors during a specific time period within the frame. When SBW is asserted an error enable signal is generated based on the information loaded into SBW1 and SBW2. When the SBW LED is on, SBW is asserted.

SOF - Start of Fame allows the user to send a Start of Frame signal to the demodulator. When SOF is asserted a signal that marks the beginning of Burst 1 is generated. When the SOF LED is on, SOF is asserted.

2.4. CONFIGURATION - Allows the user to determine the configuration and content of the frame that the Burst Generator produces. The frame may be configured in the following manner:

CLK SINGLE/DUAL - Allows the user to select a single clock source (and thus produce coherent bursts) or dual clock sources (which would provide a separate source for each burst and cause them to be non-coherent).

CONT/BURST - The Continuous switch allows the user to send a continuous stream of data symbols which may used for system baseline testing. If the Burst mode is selected the Burst Generator will produce a 1 mS frame which will have a structure based on the contents of the various counters outlined in section 2.2.3.

DATA 1/DATA 2 - If the Burst Generator is in the continuous mode the user may send data from either data source 1 (which would be used to produce Burst 1) or from data source 2 (which would be used to produce Burst 2). If the CLK SINGLE/DUAL switch is in the SINGLE position then it is irrelevant which position the DATA 1/DATA 2 switch is in since only a single source is being utilized for both Bursts.

2.5. CONNECTER INTERFACE

2.5.1. INPUTS

CLK 1 — 240 MHz ECL coupled clock input used to generate Burst 1.

DATA 1 — 240 MBPS ECL coupled data input used to generate Burst 1 data symbols.

CLK 2 — 240 MHz ECL coupled clock input used to generate Burst 2.

DATA 2 — 240 MBPS ECL coupled data input used to generate Burst 2 data symbols.

2.5.2. OUTPUTS

XTAL 1 — 240 MHz crystal output to be used to drive a PN data source for DATA 1/CLK 1.

XTAL 2 — 240 MHz crystal output to be used to drive a PN data source for DATA 2/CLK 2. If only a single source is to be utilized, XTAL 2 would not be used.

REF CLK — 240 MHz data clock derived from Xtal 1.

REF DATA — 240 MBPS serial frame data to be used for baseline testing.

SBW — Sub-burst Window ECL coupled signal.

3. REAR PANEL

The Burst Generator rear panel interface connectors, shown in Figure 5, may be separated into two general categories: Modulator and Demodulator.

3.1. MODULATOR The Modulator interface consists of five single ended ECL output signals. They are:

S0 — Least significant symbol bit

S1 — Middle significant symbol bit

S2 — Most significant symbol bit

$\overline{\text{XMIT}}$ — Transmit enable which is asserted during the transmission of all bursts and is used to enable the carrier in the modulator.

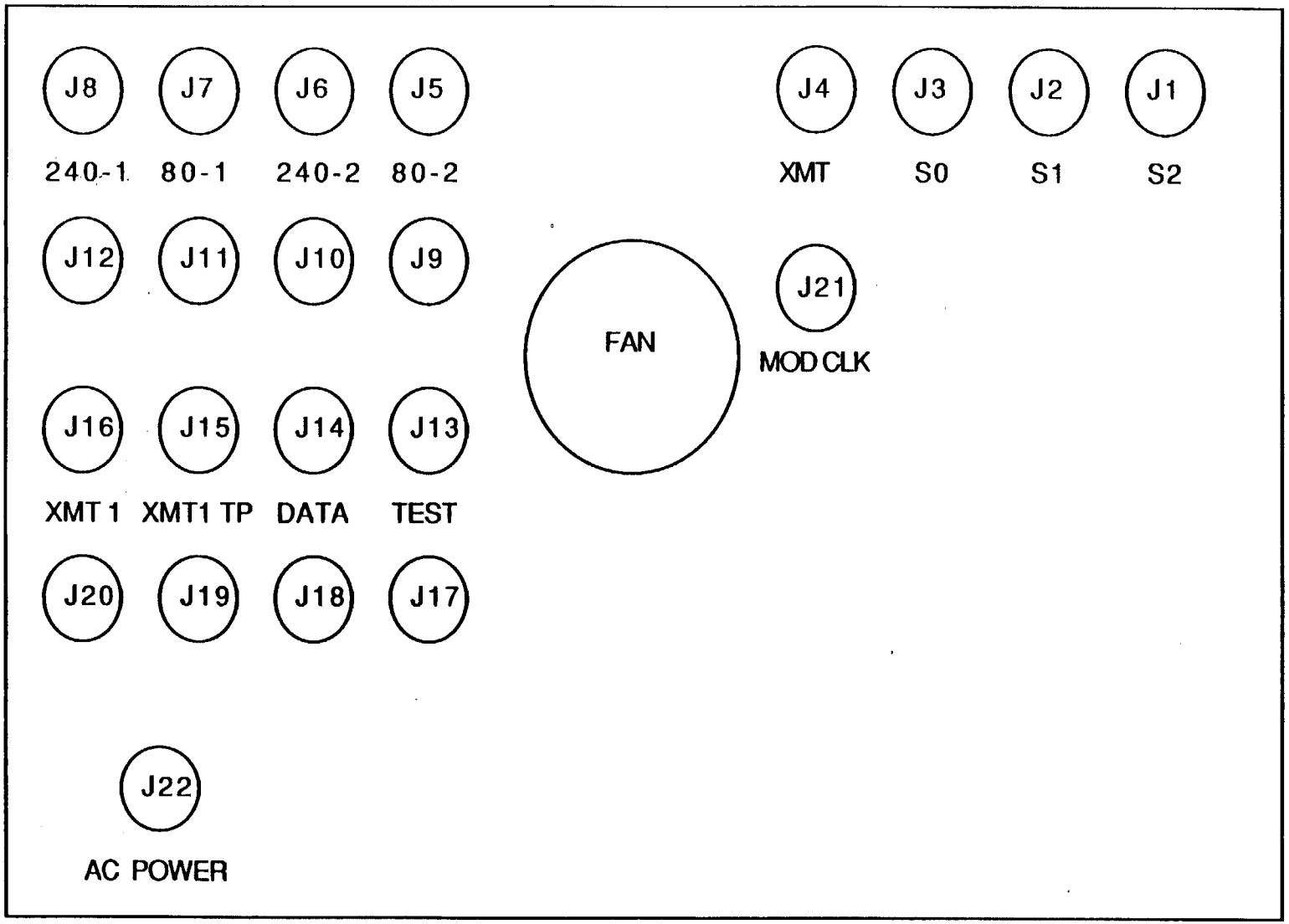


FIGURE 5
BURST GENERATOR
REAR PANEL

MOD CLK The Modulator Clock output is utilized by the digital modulator. Mod Clk is the multiplexed output of the Burst 1 and Burst 2 symbol clocks. The exact alignment of each symbol clock with it's respective data is accomplished using the CLK Delay register (See section 2.2.3).

3.2. DEMODULATOR The Demodulator interface consist of ten differential ECL outputs, two differential ECL test points, and one AC coupled test point. Depending on the configuration of the system, many of the Demodulator interface outputs will not be utilized. Most of the output signals were provided for Phase one testing which did not consist of clock recovery.

3.2.1. OUTPUTS The following signals are ECL coupled, differential outputs:

240-1 Burst 1 240 MHz clock

80-1 Burst 1 80 MHz clock

240-2 Burst 2 240 MHz clock

80-2 Burst 2 80 MHz clock

XMIT1 Burst 1 transmit enable (Start of frame marker)

3.2.2. TEST POINTS The following test points are available:

TEST DATA Serial 240 MBPS differential ECL output from Burst 1 and Burst 2.

XMIT1 TP Start of frame test point which has been AC coupled and is suitable for use with an oscilloscope.

4. OPERATION

The operation of the Burst Generator may be separated into four general areas: Power on procedures, Burst Configuration, and Sub-burst window configuration.

4.1. POWER ON After power on the Burst Generator will be in the INITIALIZE mode (INIT asserted), Start of Frame will be enabled (SOF asserted), and Sub-burst Window will be inactive (SBW deasserted). The first operation that must be performed is the initialization of all counters and registers. This may be

accomplished by two different methods depending on whether the user would like to use previously stored values or enter new values.

4.1.1. **VIEW** IF previously stored values from the NVRAM are to be used the user would:

1. Turn on Burst Generator

2 Select a counter/register using the Counter Select switch in the Burst Structure group.

3. Press the VIEW button. The value, which was stored in the NVRAM, for the selected counter / register will be displayed on the LED display and will be loaded into the ECL logic.

4. Repeat steps 2 and 3 until all counters / registers have been initialized.

5. Place CONT/BURST rocker switch in the BURST position.

6. Place CLK SINGLE/DUAL in correct position for the number of data/clock sources that are being utilized.

7. Exit initialization mode by pressing the INIT switch (INIT LED should be off).

4.1.2. **LOAD** If new values are to be utilized the user would:

1. Turn on Burst Generator

2. Select the desired counter/register using the Counter Select dial.

3. Enter the desired value using the hexadecimal keypad. (Remember to subtract one from the actual desired count to compensate for the counter implementation. See section 2.2.2.)

4. Press the LOAD switch.

5. To load more counters repeat steps 2-4.

6. Place CONT/BURST rocker switch in the BURST position.

7. Place CLK SINGLE/DUAL in correct position for the number of data/clock sources that are being utilized.

8. Exit initialization mode by pressing the INIT switch (INIT LED should be off).

In general a counter / register may be altered at any time (not just at power on) by either of the above procedures.

4.2. BURST CONFIGURATION The Burst Generator can be operated in either the burst or continuous mode. To operate the Burst Generator in the burst mode :

1. Load the counters with the desired values using one of the methods outlined in section 4.1.

2. Place the CONT/BURST rocker switch in the BURST position.

When the Burst Generator is in continuous mode the symbol clock which runs the Frame and burst counters is disabled and the data is allowed to "free run". When in continuous mode the user may select whether Data 1 or Data 2 will be used. To place the Burst Generator in the continuous mode:

1. Place the CONT/BURST rocker switch in the CONT position.

4.3. SUB-BURST WINDOW CONFIGURATION The Sub-Burst Window feature allows the user to perform error testing over selected portions of the frame. This is accomplished by providing the BERT with an "error enable" signal which allows the BERT to count errors only when the SBW signal is asserted. The Sub-burst window signal may be programmed by performing the following steps:

1. Determine the value for SBW1 using the following formula (see the SBW calculation example in section 2.2.3.):

   SBW1 = Frame offset + Delay

   where

   Frame offset = total number of symbols from

the start of the frame to the position where error counting is to begin.

Delay = RND (system delay / 12.5 nS)

2. Determine the value for SBW2 using one of the following formulas:

SBW2 = ERROR COUNT TIME / SYMBOL TIME

where

ERROR COUNT TIME = Total real time error counting is to take place.

SYMBOL TIME = 12.5 nS

or

SBW2 = SERIAL BIT COUNT / SYMBOL BITS

where

SERIAL BIT COUNT = Total number of serial data bits during which the user wants to count errors.

SYMBOL BITS = 3

or

SBW2 = SYMBOL COUNT

where

SYMBOL COUNT = The number of symbols during which the user wants to count errors.

3. Load SBW1 and SBW2 with the calculated values using the procedure outlined in section 4.1.2.

4. Enable SBW by pressing the SBW switch until the SBW LED is on.

PROOF - OF - CONCEPT

BURST GENERATOR CHASSIS

(AMTD)

TABLE OF CONTENTS

LIST OF FIGURES/TABLE

1.0 SCOPE

This specification establishes the performance, design, test manufacture requirements for the Burst Generator Chassis for the Advanced Modulation Technology Development (AMTD) system.

2.0 APPLICABLE DOCUMENTS

The latest issues of the following documents are a part of this specification:

(a)	NAS3-24678	Advanced Technology Satellite Demodulator Development, Statement of Work.
(b)	17 June 1986	Preliminary Design Review Package
(c)		AMTD System Specification

3.0 DESIGN REQUIREMENTS

3.1 Functional Description

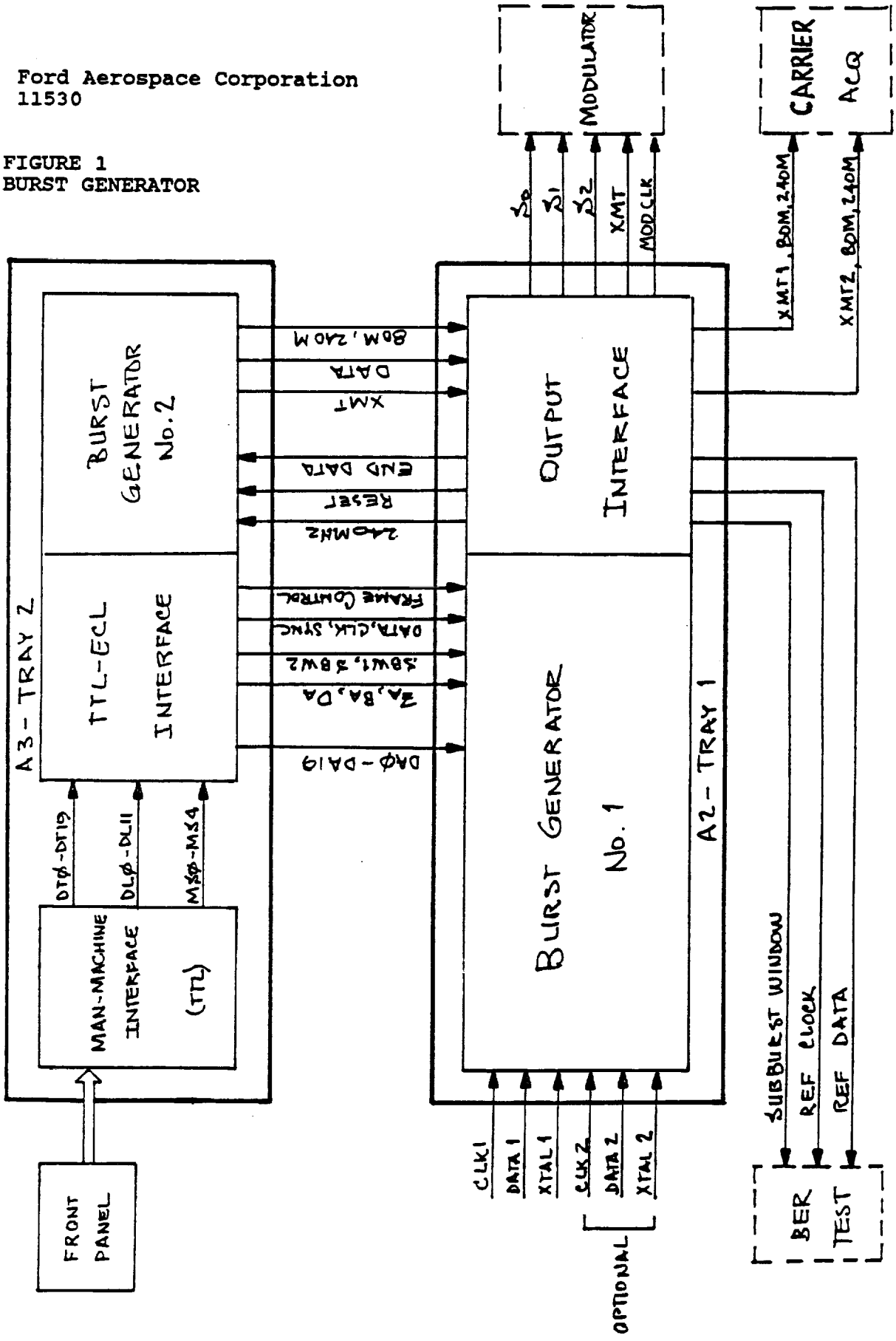
The Burst Generator, as shown in Figure 1, accepts continuous data and clock from a test source, at a rate of 240 MHz. The operator can select various formats for the frame. The generator then generates the data for one or two bursts in the frame and provides this data in 3-bit symbols, in parallel format, at a rate of 80 MSPS to the modulator.

The Burst Generator provides the 3-bit symbols also in serial format, at a rate of 240 MBPS with the associated 240 MHz clock, so that a BER Tester can perform error rate measurements. The Burst Generator also provides a Sub-Burst Window (SBW) control signal to indicate when BER testing shall take place.

For testing of the Carrier Acquisition chassis the Burst Generator also provides the transmit No. 1 and transmit No. 2 control signals, with their associated continuous 80 and 240 MHz clocks, to identify the burst No. 1 and burst No. 2 data in the frame.

Ford Aerospace Corporation
11530

FIGURE 1
BURST GENERATOR



3.2 Physical Description

The Burst Generator Chassis is rack mountable on slides. The front panel (7 inches high) and rear panel layouts are shown in Figures 2 and 3 respectively.

All front panel controls, with the exception of AC power on/off are activated by solid state switches. Front panel status is displayed by LED indicators.

3.3 PERFORMANCE SPECIFICATIONS

3.3.1 Configuration

The Burst Generator has three major parts: the man-machine interface (A3), Burst 1 (A2), and Burst 2 (A3).

3.3.1.1 Man-Machine Interface (A3)

The Burst Generator structures a frame of data as shown in Figure 4. A frame can have one or two bursts of data, but the frame is limited to 1 mS (80,000 symbols) total. Each burst has three segments: zeros, unique word, and data. A number of guard symbols separate the two bursts.

The operator can view the length of each segment on the front panel; he can also change these lengths from the keypad.

A TTL card on the second tray (A3), as shown in Figure 5, accepts data from the front panel. The card displays the incoming data on the front panel. The card combines the two inputs into data and control lines for the high-speed ECL cards. The data lines contain the number of bits to be loaded into the counter which controls the selected segment, while the control lines determine which segment has been selected. Section 3.3.2 gives a complete a complete description of all front panel controls.

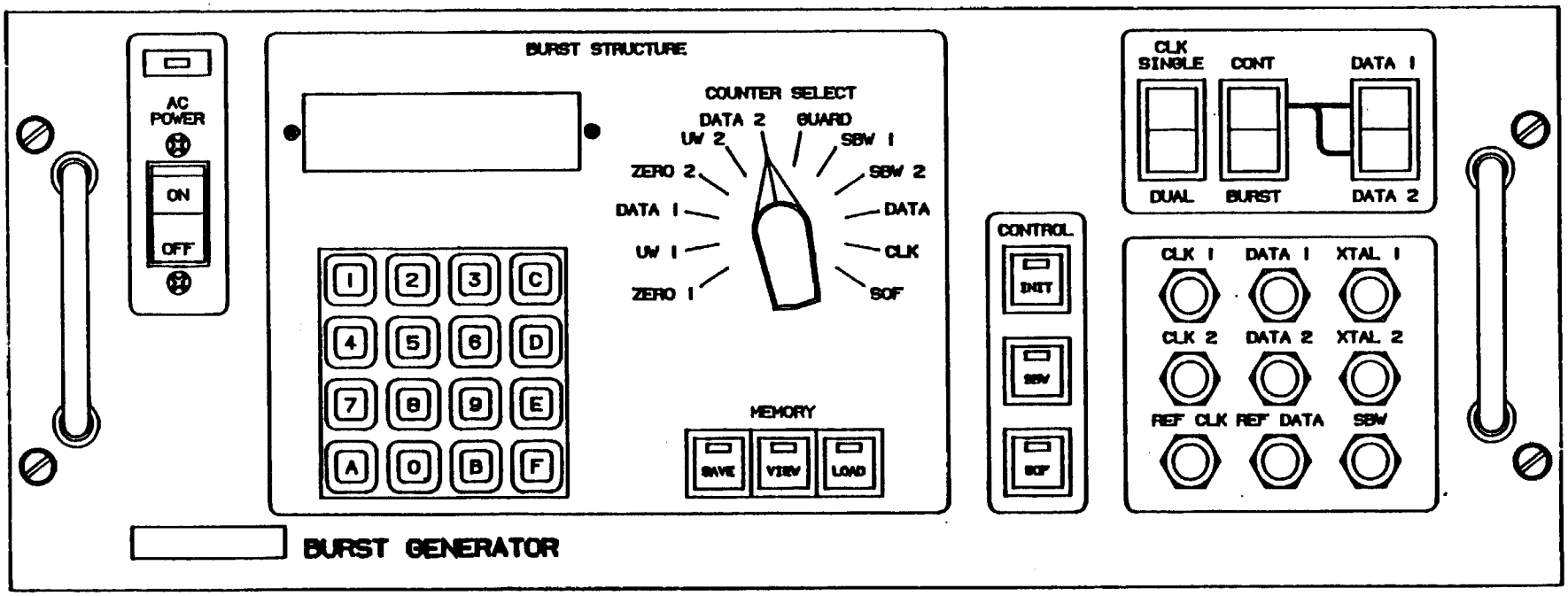


FIGURE 2

BURST GENERATOR
FRONT PANEL

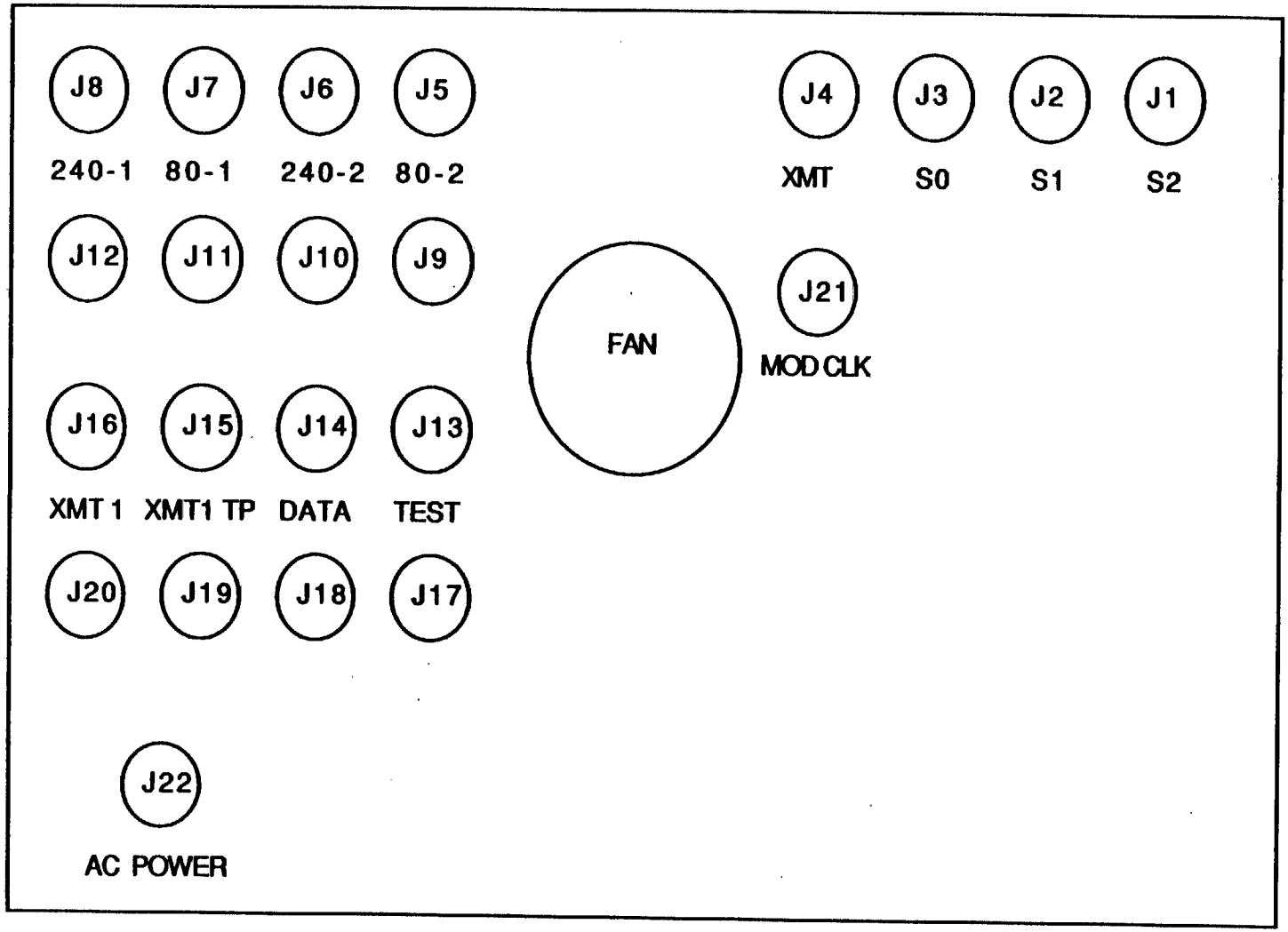


FIGURE 3
BURST GENERATOR
REAR PANEL

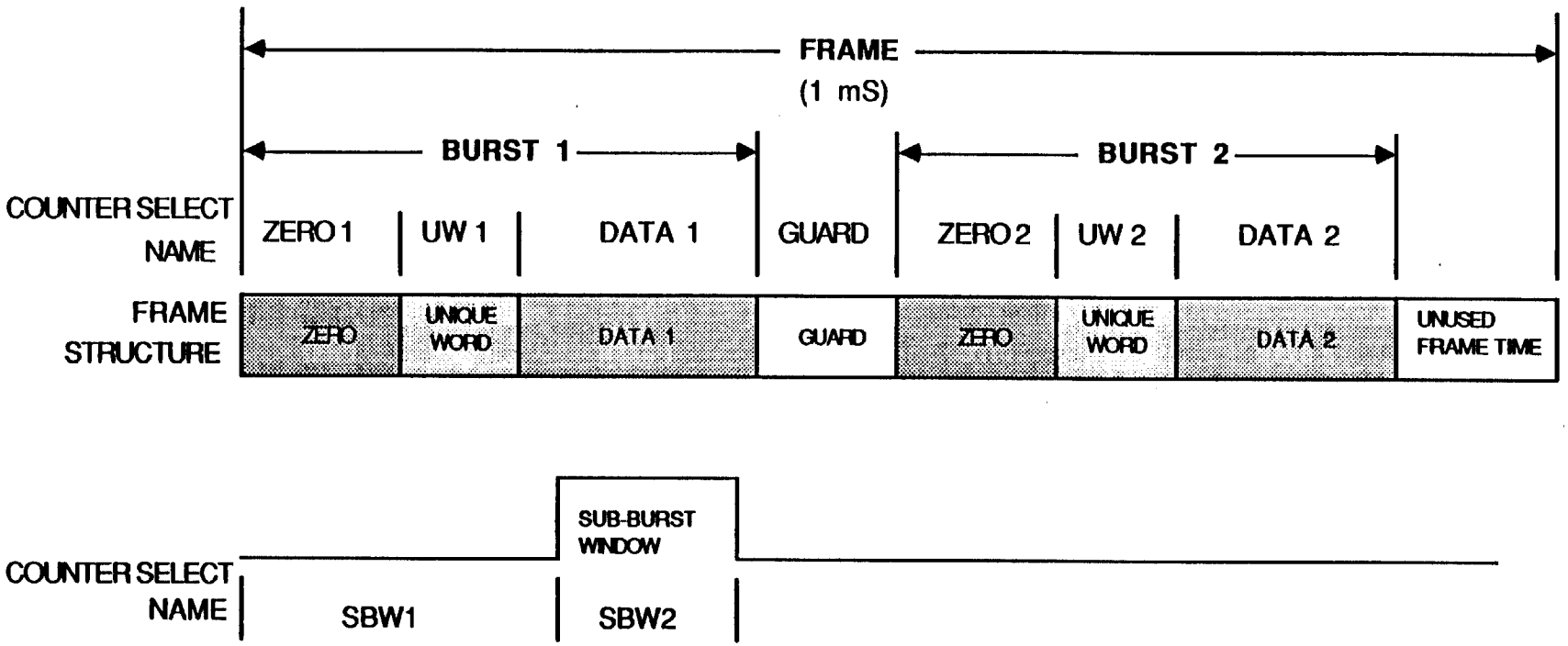


FIGURE 4

FRAME STRUCTURE

3.3.1.2 TTL-ECL Interface (A3)

This interface, located on the ECL card of the second tray, receives the following control lines from the TTL card (See Figure 1):

- o DT0-DT19 — 5-digit data for segment length
- o DL0-DL11 — Segment selection from "Counter Select"
- o MS0-MS4 — Frame control, such as: mode (continuous - burst), one burst - two bursts, clock (single-dual).

The interface logic translates the TTL signals into ECL signals and generates the following control lines for the Burst Generators:

- o DA0-DA19 — 5-digit data bus for Burst 1
- o DB0-DB19 — 5-digit data bus for Burst 2
- o ZA,BA,DA — Burst 1 zero, unique word, data segment select
- o ZA,BB,DB — Burst 2 zero, unique word, data segment select
- o G — Guard Segment select
- o SBW1, SBW2 — Sub-Burst window segment select
- o Data, Clk, SOF — Delay for test data, clock and start of frame

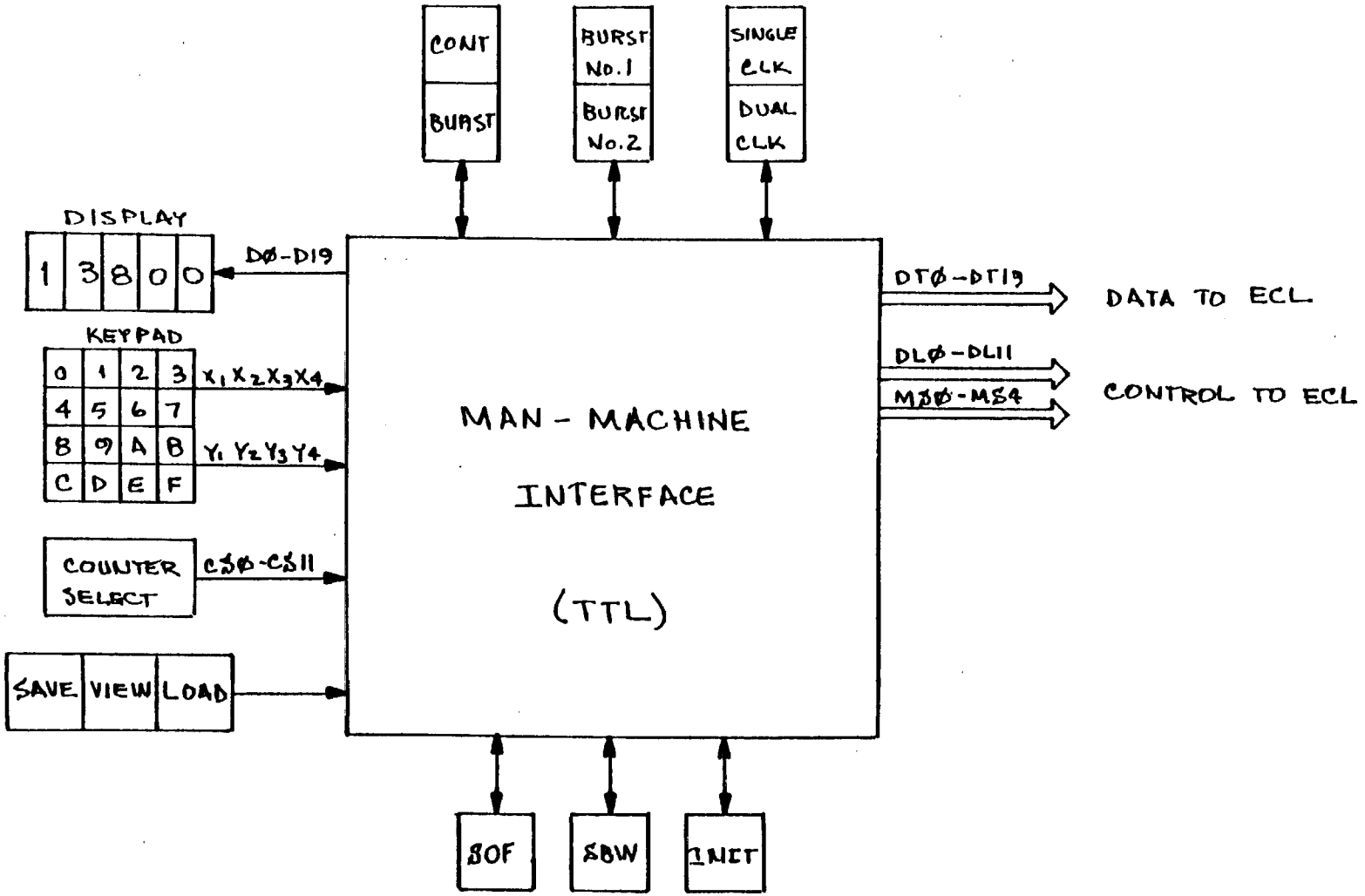
3.3.1.3 Burst 1 (A2)

Burst 1 hardware, shown in Figure 6, receives the 240 MHz clock and 240 MBPS data from one test source. For a "single clock" command both bursts (Burst 1 and Burst 2) operate from the clock 1/data 1 inputs. For a "dual clock" command Burst 1 utilizes clock 1/data 1 inputs, and Burst 2 uses clock 2/data 2 inputs.

Burst 1 has the frame counter. The continuous mode

FIGURE 5

MAN-MACHINE INTERFACE



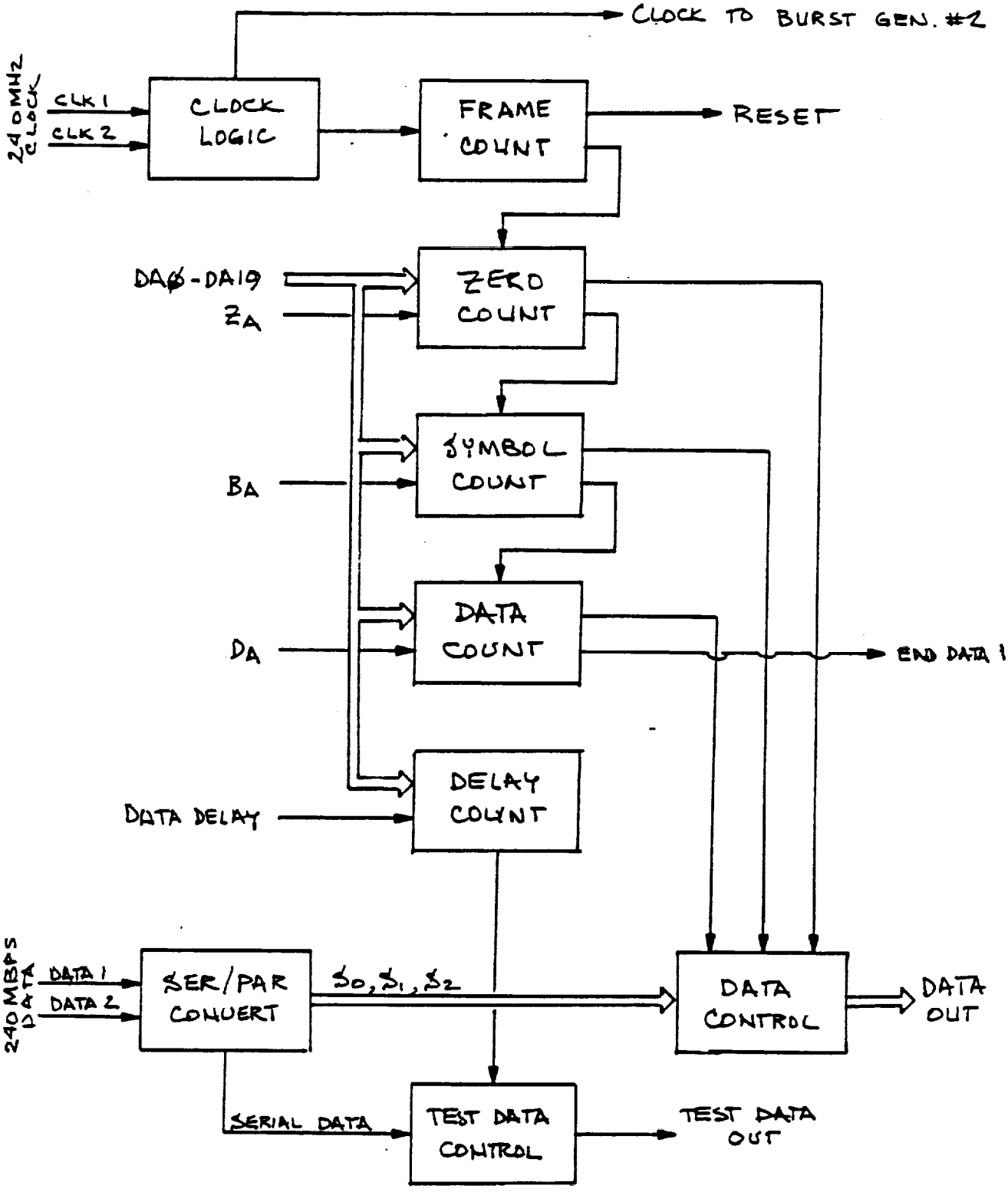


FIGURE 6

BURST 1
BLOCK DIAGRAM

disables this counter, but in burst mode it counts to 80,000 to mark the start of each frame.

The lengths of Burst 1 segments are stored in the logic for zero count, symbol count, and data count. These logic counters are sequentially activated, so they can control the output data in the generation of Burst 1.

This data goes via a modulator and demodulator to a BER tester. If this tester requires reference data, then this data may have to be delayed to compensate for the delay in the mod/demod path. The operator selects this delay on the front panel and this delay is stored in the "delay count". Then this logic delays the serial data stream by a number of 80 MHz clock pulses equivalent to the number stored in the delay count.

3.3.1.4 Burst 2 (A3)

Burst 2 hardware, shown in Figure 7, receives the data and clock from the first Burst Generator or from its own source if in Dual Clock Mode. The lengths of Burst 2 segments are stored in the logic for guard count, zero count, symbol count, and data count. These logic counters are sequentially activated at the end of Burst 1, so they can control the output data in the generation of Burst 2.

"Delay count" performs the same function on Burst 2 data, as its counterpart in Burst 1.

3.3.1.5 Output Interface (A2)

The Output Interface, shown in Figure 8, converts the gray data words into a binary code to accommodate 8-PSK modulation. This interface also has provisions to align the transmit control signals and the 80 MHz clocks with the outgoing data bits, so that all signals are in phase at the rear of the demodulator.

The operator programs the delay on the front panel and the information is stored in the clock delay and SOF (Start of Frame) delay respectively. Programmable adjustable delay lines perform the actual task.

This interface also contains the sub-burst window count logic. The sub-burst window provides an "error count enable" signal for a programmable (from the front

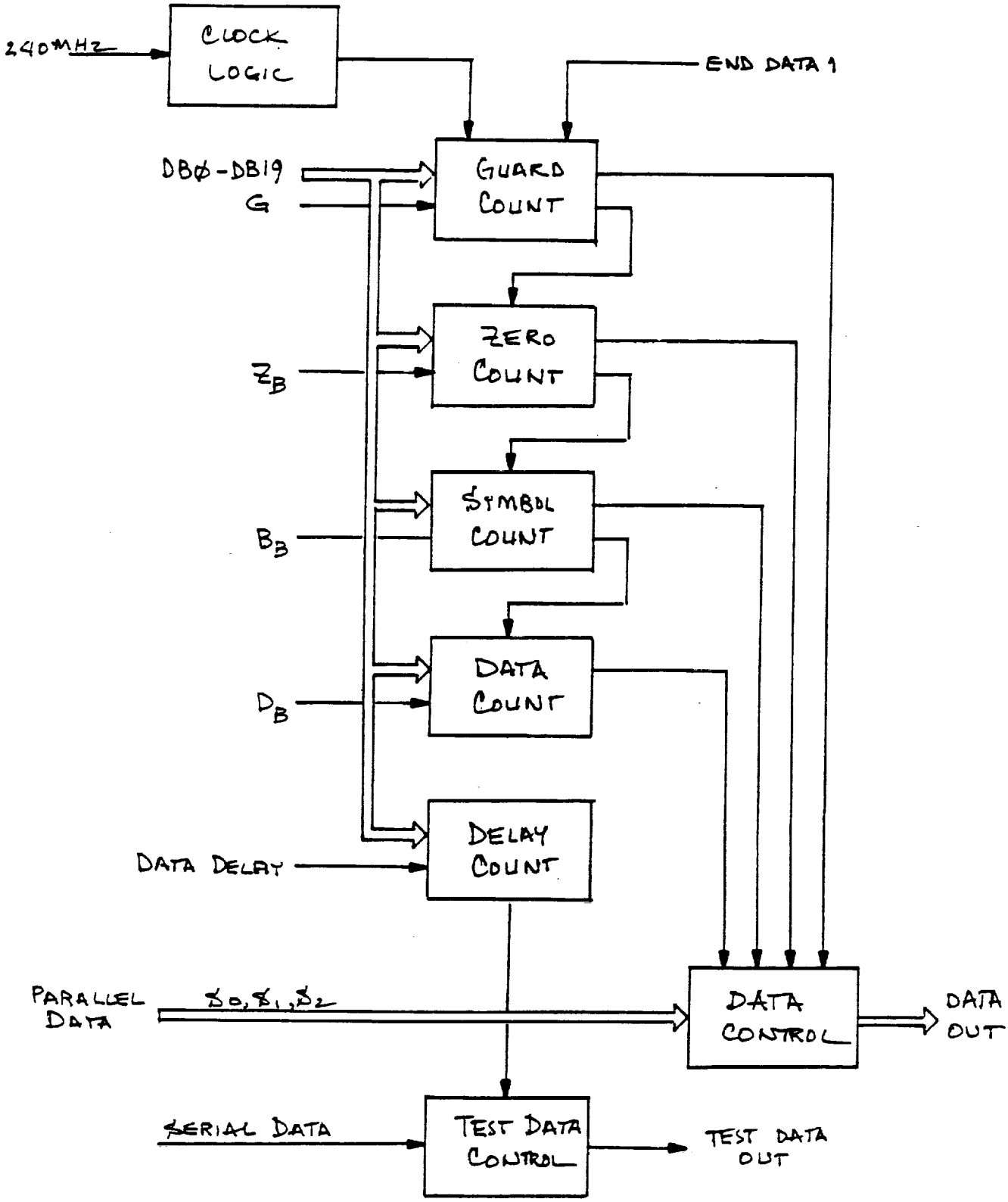


FIGURE 7

BURST 2
BLOCK DIAGRAM

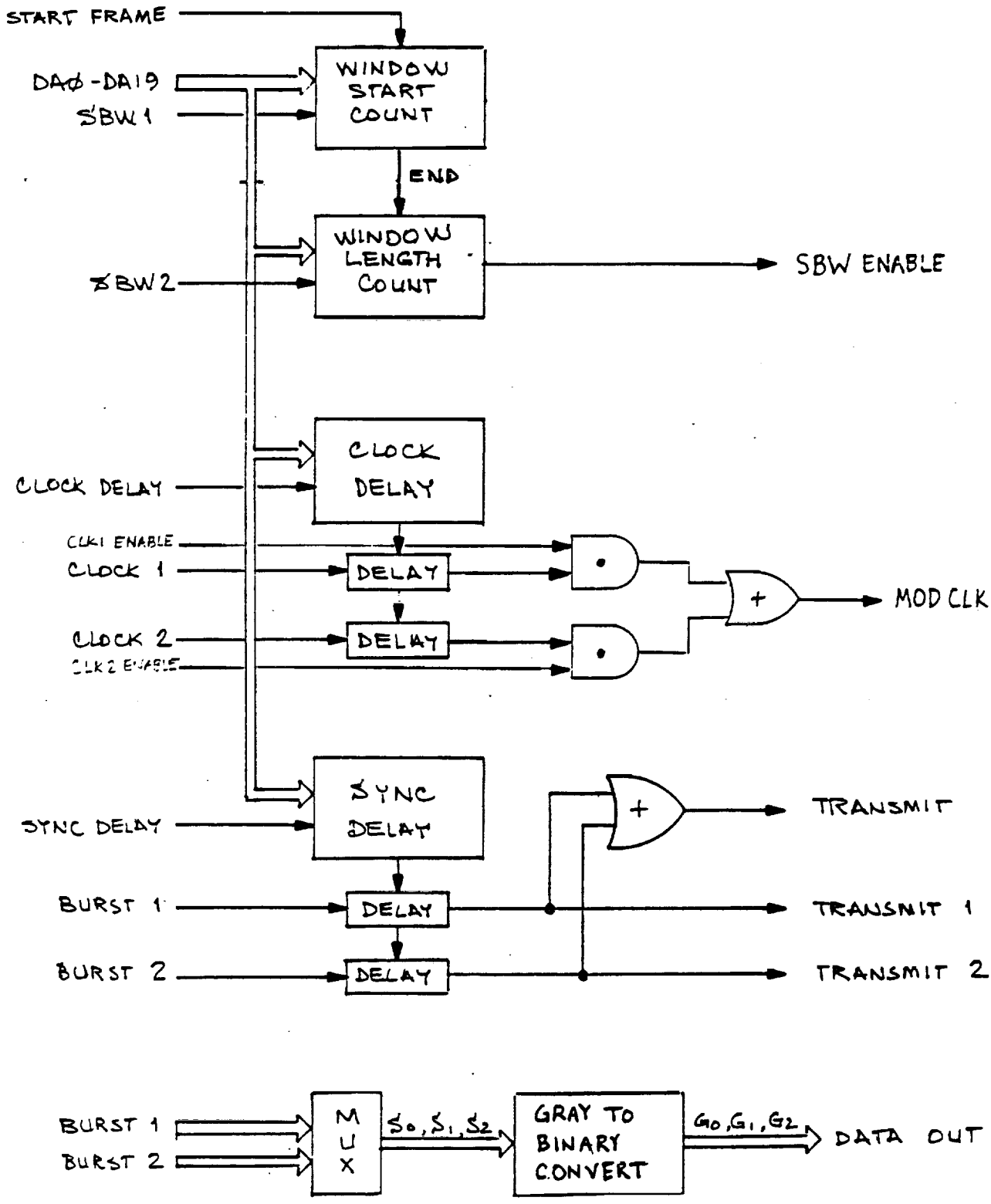


FIGURE 8

OUTPUT INTERFACE
BLOCK DIAGRAM

panel) portion of the data in either Burst 1 or Burst 2, as illustrated in Figure 4 for Burst 1.

3.3.2 CONTROL AND STATUS SPECIFICATIONS

Switches on the front panel control the operation of the Burst Generator as specified in Section 3.3.2.1.

The Burst Generator monitors the status of its operation for display on the front panel as specified in Section 3.3.2.2.

3.3.2.1 Controls

The Burst Formatter provides the following switches for local control of the chassis' operation:

- o POWER ON/OFF — This switch controls the main power to the supplies in the chassis.
- o SOF — This switch controls the transmission of a start of frame signal to the Baud Acquisition Chassis. In the ON mode (LED ON) a SOF signal is transmitted at the start of each frame. In the OFF mode (LED OFF) the SOF signal is not transmitted.
- o SBW — This switch enables the sub-burst windows in the ON position.
- o INIT — The logic in the chassis is reset by activating this switch.
- o CONT/BURST — This switch controls the frame format. In CONT mode the generator transmit one zero section, one unique word and then data on a continuous basis. In BURST mode the generator transmits 1 mS frames.
- o DATA 1/DATA 2 — This switch controls the data in continuous mode only. The generator

transmits data from Burst 1 when DATA 1 is selected; and from Burst 2 when DATA 2 is selected.

- o CLOCK SINGLE/ DUAL — Burst 1 and Burst 2 have the same clock/data when in SINGLE mode. Burst 1 and Burst 2 have individual clocks/data when in DUAL mode.

- o KEYPAD — The operator enters the number of symbols for any burst segment through the keypad. Enter each number in a 5-digit HEX format, the number is displayed on the LEDs above the keypad.

- o COUNTER SELECT — On this switch the operator selects where the number of the keypad shall be entered:

  ZERO 1 - Zeros in Burst 1
  UW1 - Unique word in Burst 1
  DATA 1 - Data in Burst 1

  ZERO 2 - Zeros in Burst 2
  UW 2 - Unique word in Burst 2
  DATA 2 - Data in Burst 2
  GUARD - Gap between Bursts 1 and Burst 2

  SBW1 - Start of Sub-Burst window, referenced from the start of frame.
  SBW2 - Length of Sub-Burst window

  DATA - Test data delay in 12.5 ns steps
  CLK - Clock/data alignment delay
  SOF - SOF/data alignment delay

- o SAVE — This switch stores all of the current frame segment and delay register values in NVRAM (Non-volatile RAM.)

- o VIEW — This switch displays the working number of the location selected by the COUNTER select switch.

- o LOAD — This switch loads the displayed keypad number into the working location, selected by the COUNTER select switch.

3.3.2.2 Status

The Burst Formatter provides the following displays for monitoring of the chassis' operation:

- o POWER — Indicates the presence AC power.
- o SOF — LED ON: SOF signal transmitted. LED OFF: SOF signal suppressed.
- o SBW — LED ON: The Sub-Burst window control signal is active. LED OFF: Sub-Burst window control signal is suppressed.
- o CONT/BURST — The top LED is ON in the continuous mode. The bottom LED is ON in the burst mode.
- o DATA 1/DATA 2 — The top LED is ON, when the generator selects Data 1 source in continuous mode. The bottom LED is ON, when the generator selects Data 2 source in continuous mode.
- o CLOCK — The TOP LED is On, when Burst 1 and 2 have the same clock. The BOTTOM LED is ON, when Burst 1 and 2 have individual clocks.
- o DISPLAY — Displays the number as indicated in section 3.3.2.1.

3.3.2.3 Monitoring Points

The front panel of the Burst Generator has the following inputs:

- o CLK 1 — Clock for Burst 1 at 240 MHz

- o DATA 1 — Data for Burst 1 at 240 MBPS
- o CLK 2 — Clock for Burst 2 at 240 MHz
- o DATA 2 — Data for Burst 2 at 240 MBPS

The front panel of the Burst Generator has the following outputs:

- o REF CLK — Serialized frame clock at 240 MHz
- o REF DATA — Serialized frame data at 240 MBPS
- o SBW — Sub-burst window signal to be used with the bit error rate test set.
- o XTAL 1 — 240 MHz XTAL output - for Burst 1 data source
- o XTAL 2 — 240 MHz XTAL output - for Burst 2 data source

3.4 INTERFACE SPECIFICATIONS

This section describes the external interfaces. These interfaces are via the rear panel. Table 3.4 lists the connector assignment.

3.4.1 Modulator Interface

The Burst Generator transmits the following signals to the modulator:

3.4.1.1 Frame Symbol Words

These words contain three bits: S2 (MSB), S1 and SO (LSB). Each Bit represent a binary "1", when the output level is -10V $\pm$0.1V; and a binary "0" when the output level is -1.7 V $\pm$0.1 V.

These bit signals are ECL driven and DC coupled as shown in Figure

3.4.1.2 Transmit Control Signal

This signal indicates valid data on the bit lines, when it is at the binary "0" level (-1.7V $\pm$0.1V). The transmit control signal indicates non-valid data on

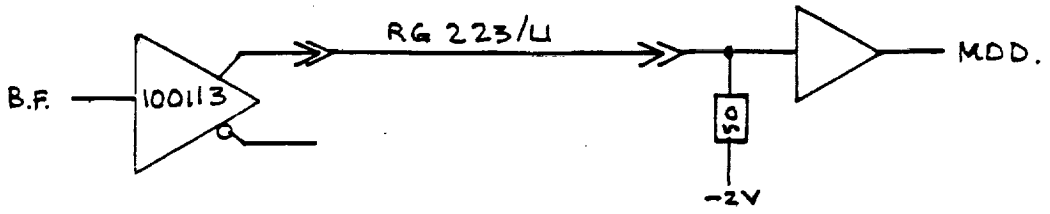


FIGURE 9

BURST GENERATOR - MODULATOR INTERFACE

the bit lines, when it is at the binary "1" level (-1.0V ±0.1V). This control signal is ECL driven and DC coupled as shown in Figure 9.

3.4.1.3 Modulator Clock Signal

This signal is used by the Digital Modulator to latch the symbol data. It is the multiplexed 80 MHz symbol clock derived from Burst 1 and Burst 2. The clock is ECL driven and DC coupled as shown in figure 9.

3.4.2 Carrier Acquisition Interface

The Burst Generator transmits the following signals to the carrier acquisition chassis:

3.4.2.1 Clock Signals

The Burst Generator provides four clock signals to the carrier acquisition chassis: 80 MHz and 240 MHz associated with Burst 1 data; and 80 MHz and 240 MHz associated with Burst 2 data.

The 80 MHz ±.01% clock signals have a 66 percent duty cycle, and they are DC coupled as shown in Figure 10.

CONN.	SIGNAL	INTERFACE
J1	Frame Symbol Bit - S2	Modulator
J2	Frame Symbol Bit - S1	Modulator
J3	Frame Symbol Bit - S0	Modulator
J4	Transmit Control Signal	Modulator
J5	80 MHz - Burst 2	Demod.
J6	240 MHz - Burst 2	Demod.
J7	80 MHz - Burst 1	Demod.
J8	240 MHz - Burst 1	Demod.
J9	80 MHz - Burst 2 - Inv	Demod.
J10	240 MHz - Burst 2 - Inv	Demod.
J11	80 MHz - Burst 1 - Inv	Demod.
J12	240 MHz - Burst 1 - Inv	Demod.
J13	Serial Test Data Out	BERT
J14	Serial Data In	Demod.
J15	Transmit Burst	Test Point
J16	Transmit Burst 1	Demod
J17	Serial Test Data Out - Inv	BERT
J18	Serial Data In - Inv	Demod
J19	Spare	
J20	Transmit Burst 1 - Inv	Demod
J21	Digital Modulator Clock Out	Modulator
J22	Power 115 VAC - 60Hz	

TABLE 3.4

INTERFACE CONNECTORS

as shown in Figure 10.

The 240 MHz ±.01% clock signals have a 50/50 percent duty cycle, and they are also DC coupled as shown in Figure 10.

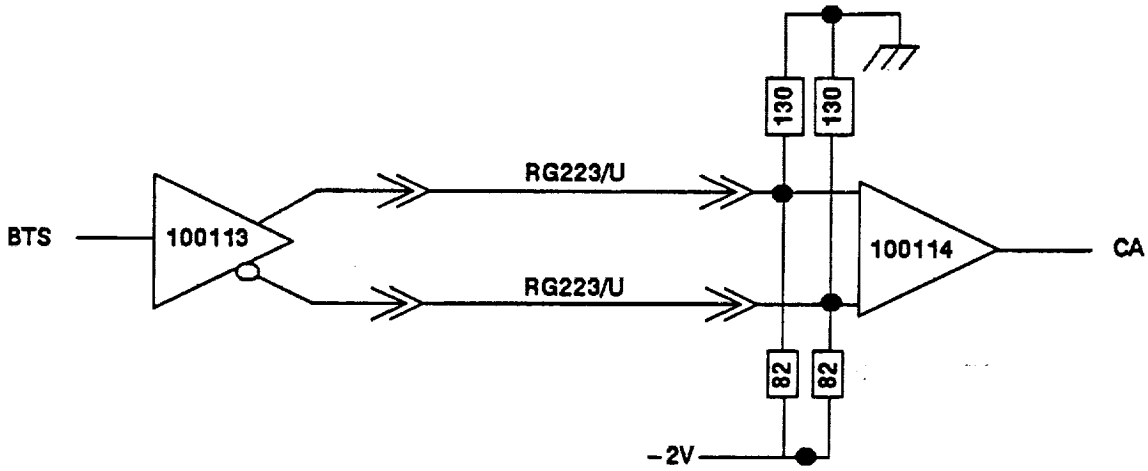


FIGURE 10

CLOCK INTERFACE CIRCUIT

3.4.2.2 Transmit Control Signal

Transmit Control No. 1 indicates the start of a frame when the (+) output is more positive than the (INV) output.

This control signal is ECL driven and shall be DC coupled as shown in Figure 11.

3.4.3 Baud Acquisition Interface

The Burst Generator receives the following signal from the baud acquisition chassis:

3.4.3.1 Serial Data Signal

The Burst Generator accepts the three most significant bits of the reconstructed valid data words, in gray code and in serial format, at a rate of 240 MBPS ±2%, most significant bit first.

This data signal shall be ECL driven and DC coupled as shown in Figure 11.

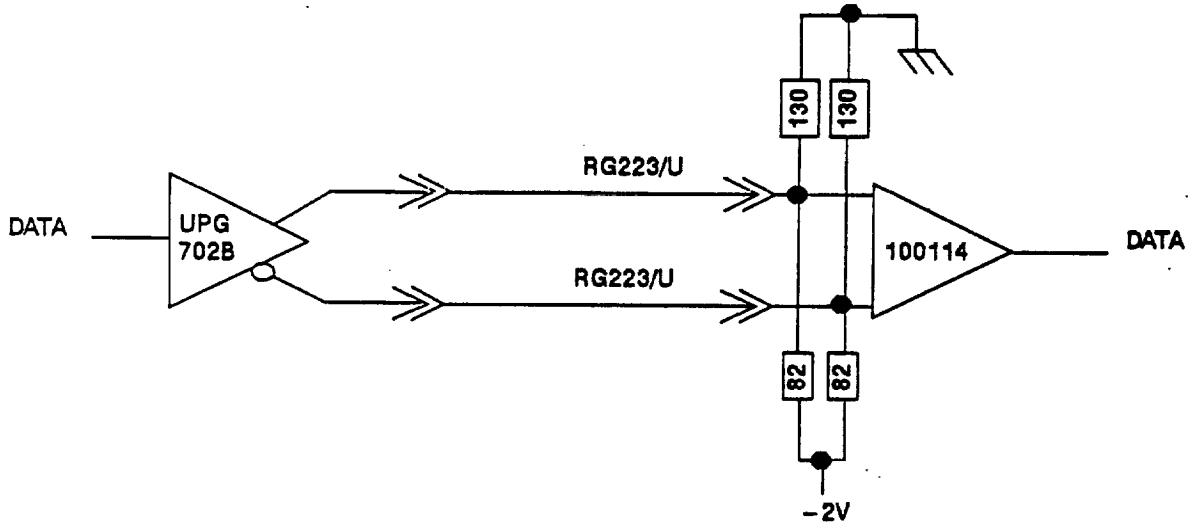


FIGURE 11

SERIAL INPUT INTERFACE

3.4.4 Test Output

The Burst Generator provides the serialized frame symbols as reference test signals. These symbols, representing Burst 1 and Burst 2 data, are serialized in binary code, at a rate of 240 MBPS ±2%, most significant bit first.

This signal is ECL driven and shall be coupled as shown in Figure 12.

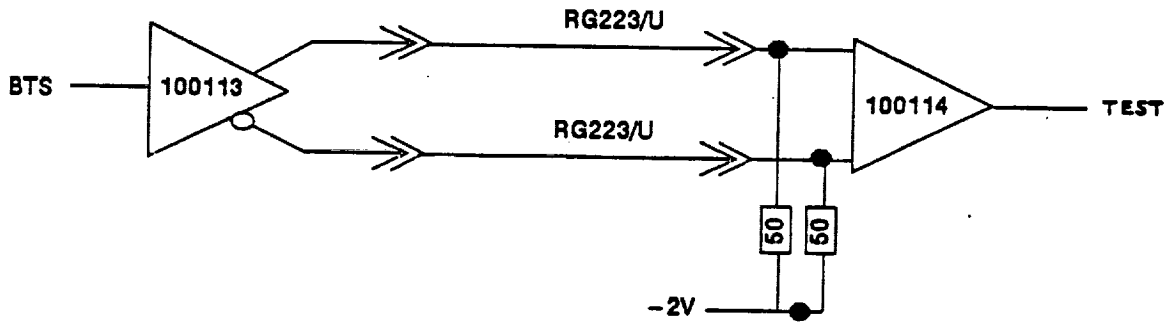


FIGURE 12

TEST OUTPUT INTERFACE

3.4.5 AC Power

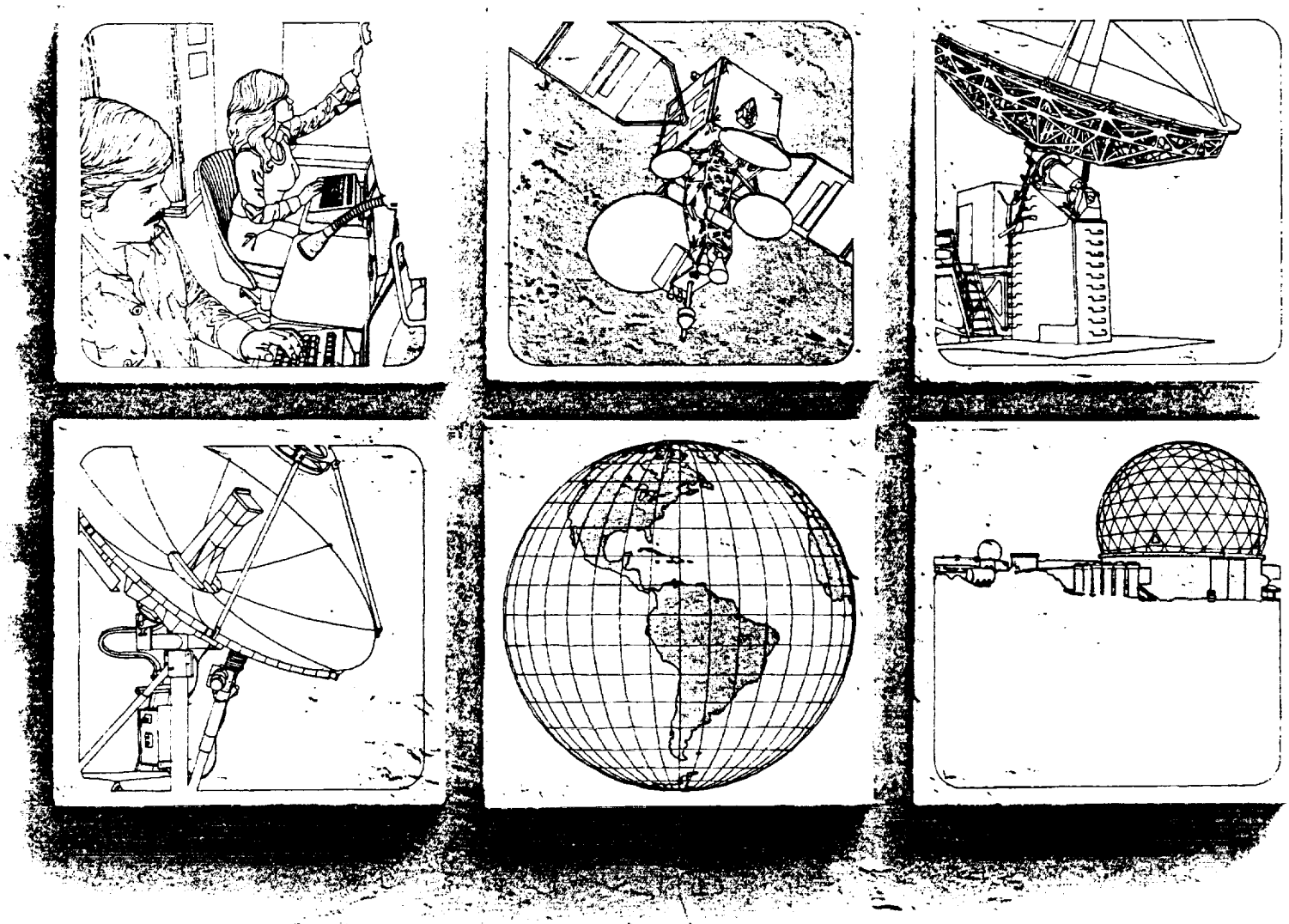
The Burst Generator chassis operate on 120 Volts AC ±10% and 60 Hz ±5%. The maximum current is 3 AMPS.

AMTD

POC DEMODULATOR

SYSTEM DOCUMENTATION

MODULATOR / BERT
OPERATIONS / SPECIFICATION



Ford Aerospace/Space Systems Division

AMTD

POC DEMODULATOR

SYSTEM DOCUMENTATION

MODULATOR / BERT
OPERATIONS / SPECIFICATION

SEPTEMBER 13, 1988

VER 2.0
8-24-88

OPERATIONS MANUAL

MODULATOR / BERT

(AMTD)

TABLE OF CONTENTS

1. GENERAL DESCRIPTION

The Modulator / BERT may be separated into two main functions: digital modulator and bit error rate test set, as shown in Figure 1.

1.1. BERT The term Bit Error Rate Test set is a misleading title if one wishes to accurately describe the complete function of all the digital hardware that is not associated with the modulator portion of the chassis. The BERT portion of the chassis actually performs three major functions:

- o Pseudo-random data and clock source (for use with the Burst Generator)
- o AMTD hardware simulator (for use with the Baud and Clock Acquisition chassis integration)
- o Bit Error Rate Test logic

Throughout this document the term **BERT** will be used to describe the collection of functions outlined above, while the term **Modulator** will be used to describe the hardware in the chassis associated with the modulation function. Thus the chassis may be referred to as the "BERT" or the "Modulator" when in actuality its complete title is the Modulator / BERT, which is cumbersome to type and to read. Because the BERT portion of the chassis does encompass three major functions it will also be convenient to refer to them directly as the **PN data generator**, **Simulator**, and **BERT logic**, when referring to the pseudorandom data and clock source hardware, the AMTD hardware simulator, and the actual bit error rate test logic.

1.1.1. PN / CLOCK SOURCE The PN data generator consist of two separate data / clock sources which produce two individual, non-coherent 240 MBPS serial data streams with their associated 240 MHz clocks. Each PN generator produces a sequence with a period of $2^{11}-1$ bits and requires a 240 MHz clock source in order to operate.

1.1.2. HARDWARE SIMULATOR The Simulator portion of the BERT allows several portions of the AMTD system to be eliminated for testing purposes. When in "simulation" mode the BERT chassis will produce all of the signals necessary to replace the Burst Generator, Modulator, Quadrature Detector, and either the Baud Acquisition or Carrier Acquisition chassis. The different possible test configurations are shown in Figure 2.

The simulator facilities smooth system integration by

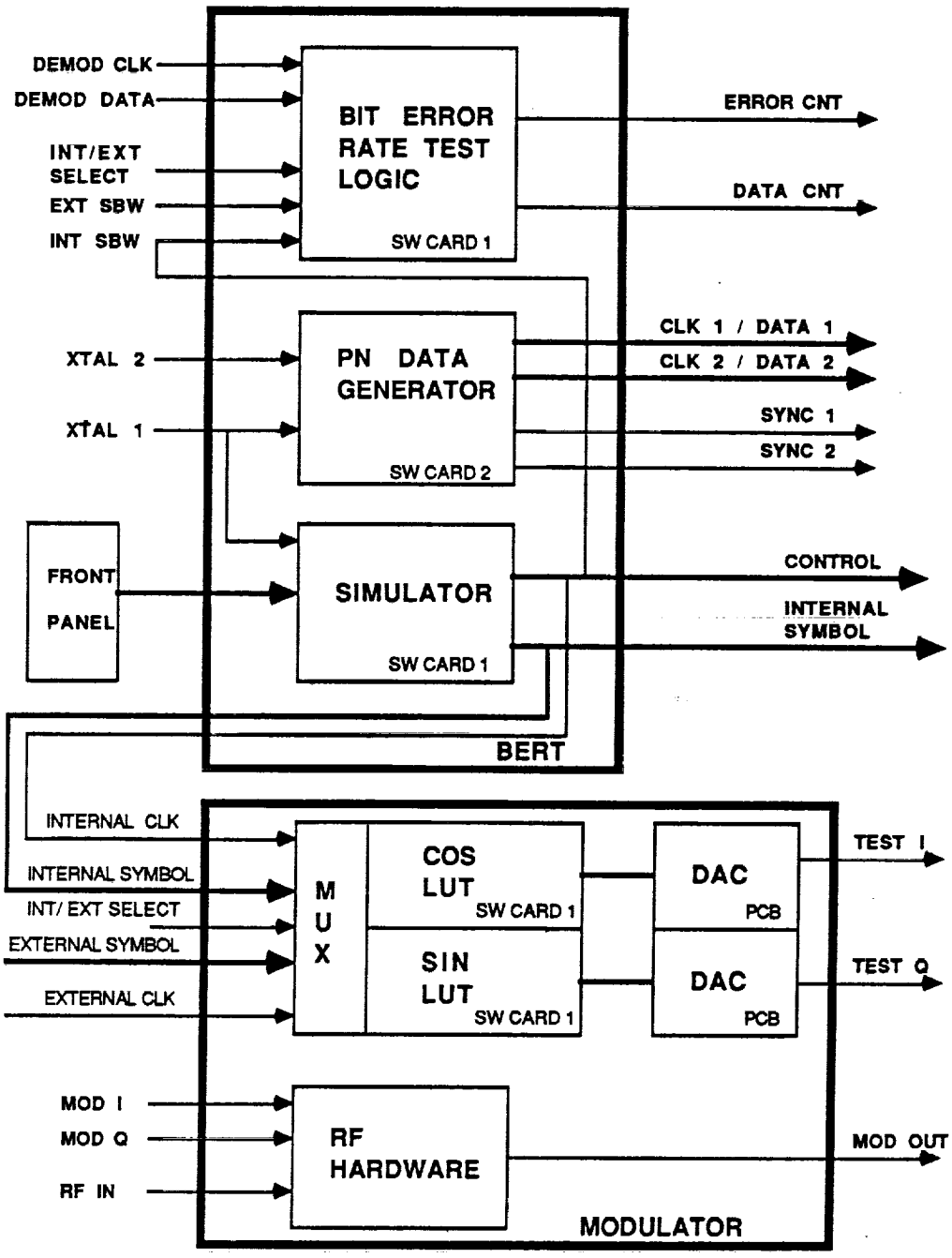
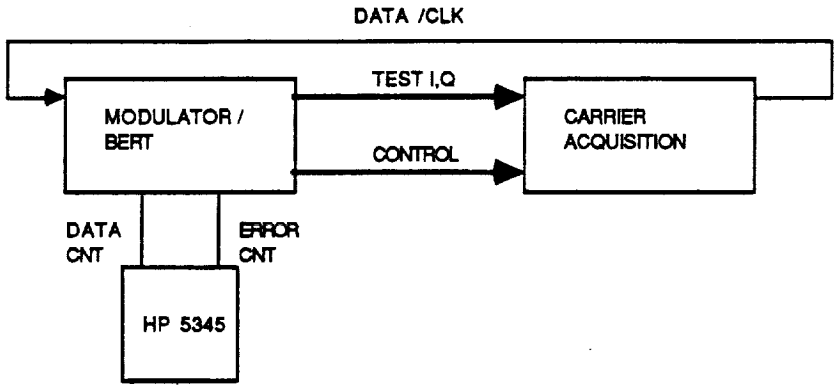
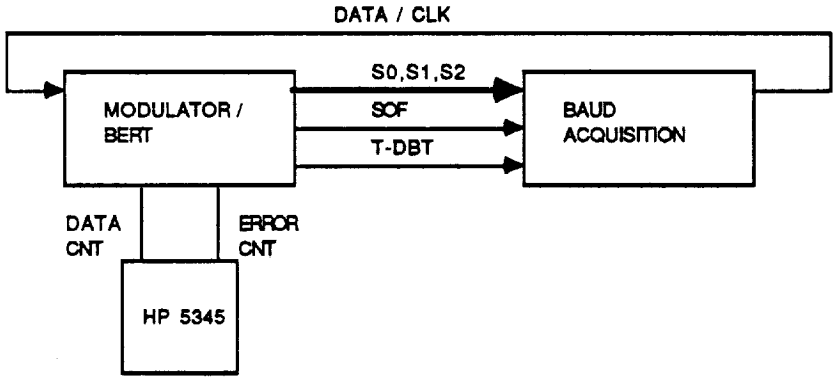


FIGURE 1

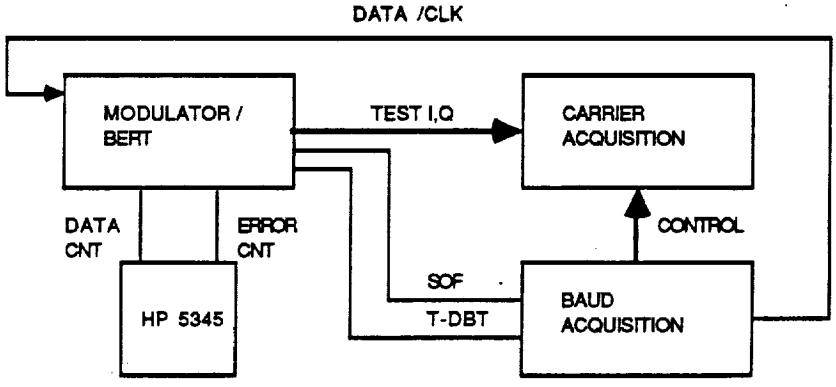
MODULATOR / BERT
BLOCK DIAGRAM



A. Simulator replacing the Modulator, Quadrature Detector, and Baud Acquisition Chassis



B. Simulator replacing the Modulator, Quadrature Detector, and Carrier Acquisition Chassis.



C. Simulator replacing the Modulator, and Quadrature Detector

FIGURE 2

SIMULATION CONFIGURATIONS

allowing each chassis to be brought on line individually. This increases system confidence as each level of the system integration may be fully tested.

The simulator generates a shortened frame that is 1024 symbols in length (excluding guard symbols) for a dual burst frame, or 512 symbols for a single burst frame. The burst content is defined by the simulator data PROM which contains 512 x 4 bits of memory.

1.1.3. **BERT** The actual Bit Error Rate Test logic, shown in Figure 3, consists of the same $2^{11}-1$ PN sequence logic used in the PN Data generator. The PN generator may be considered as an encoder that takes a constant logic state and encodes it with the $2^{11}-1$ PN sequence. The BERT logic then decodes the demodulated data stream and in the absence of bit errors reconstructs a "constant" logic state. By monitoring the transitions that occur on the output of the decoder the number of bit errors may be determined. By keeping track of the total number of data bits that have been received a bit error rate may be calculated. Because each data bit is compared three times in order to "decode" the data stream, the displayed error rate will be three times greater then the actual error rate.

1.2. **MODULATOR** The digital modulator, shown in Figure 4, consists of the Sin and Cosine look up table (LUT) Read Only Memories (ROM), the Digital-to-Analog Converters (DAC), the double-balanced mixers, phase shifter and RF combiner. The 8-PSK modulation is actually defined in the ROM LUTs, which have been programmed for the correct constellation. By simply reprogramming the ROM LUT any constellation may be obtained. The modulator utilizes a carrier centered at 3.373056 GHz.

2. FRONT PANEL

The front panel, shown in Figure 5, consists of the following functional groups: AC power, modulator, Control, Data Configuration, Test Points, BERT, PN/CLK.

2.1. **AC POWER** The AC power group consists of the AC circuit breaker switch and the "AC power on" LED indicator.

2.2. **MODULATOR** The Modulator group consists of the modulated signal output connecter. The modulated output is centered at 3.373056 GHz and is at approximately -30 dBm.

2.3. **CONTROL** The Control group consists of the following switches:

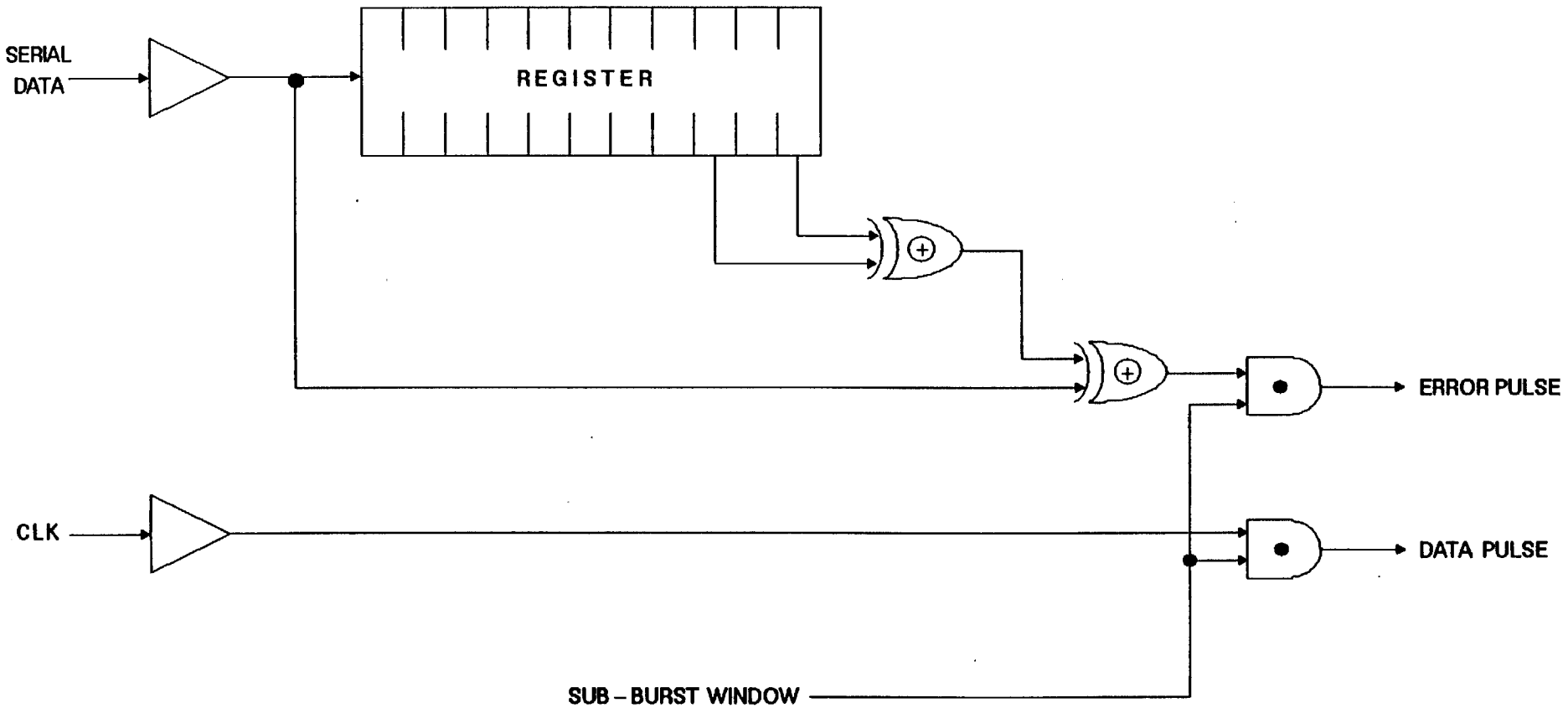


FIGURE 3

BIT ERROR RATE TEST LOGIC

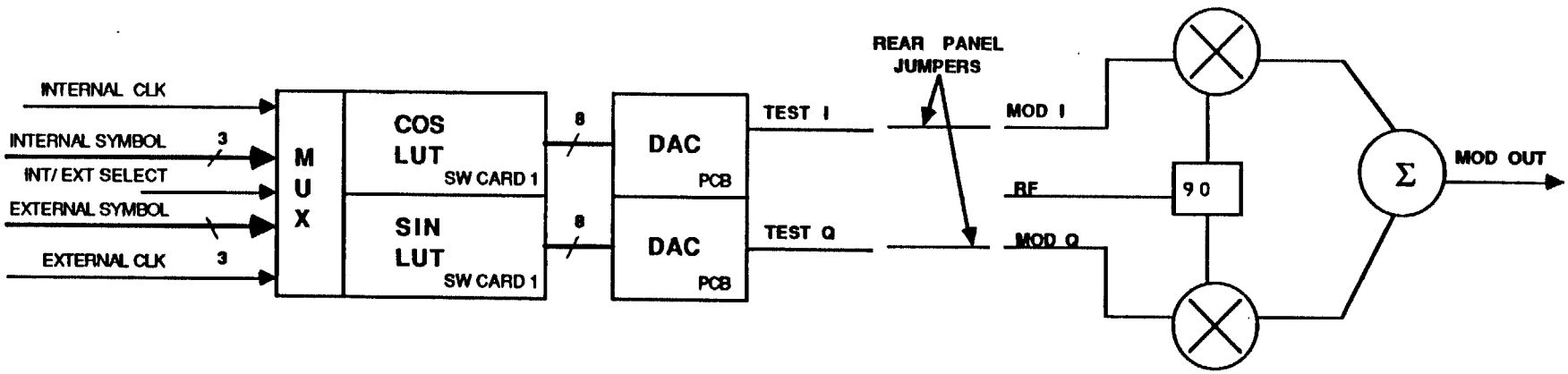


FIGURE 4

MODULATOR

BLOCK DIAGRAM

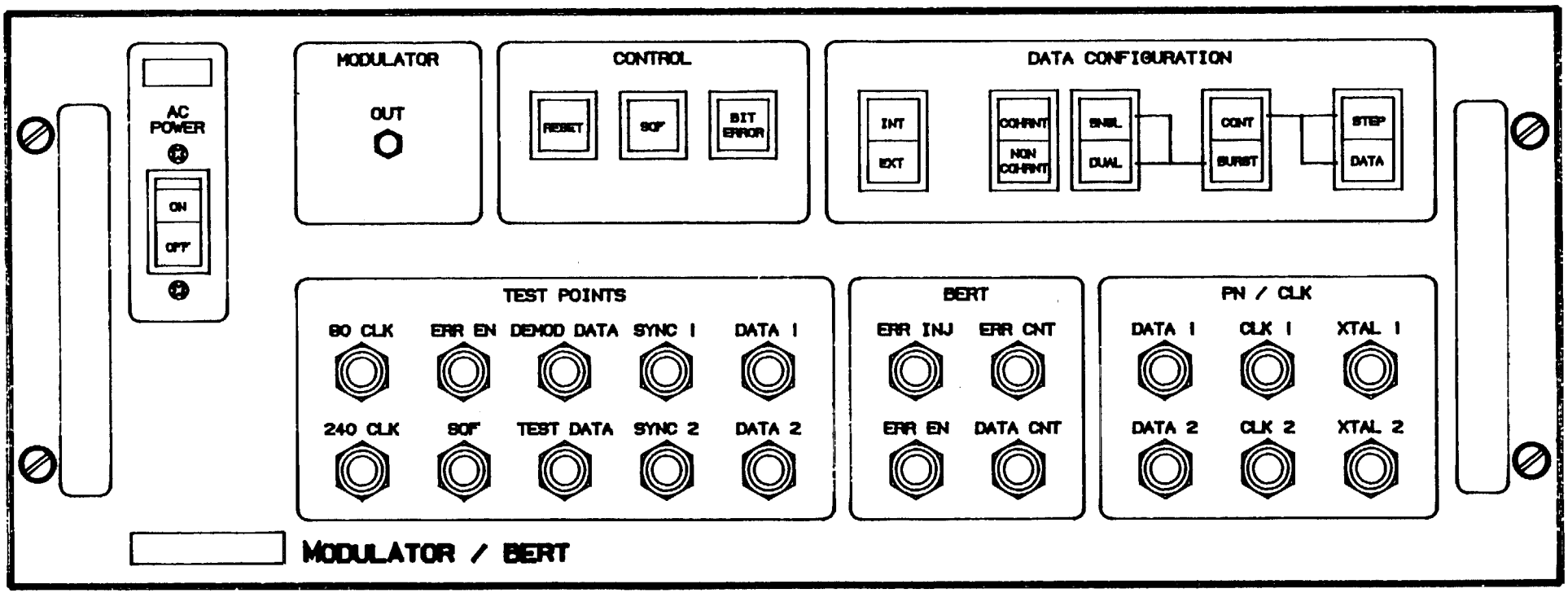


FIGURE 5

FRONT PANEL

RESET — RESET is a momentary switch that will reinitalize the frame counter for the simulator hardware.

SOF — The SOF switch controls the transmission of the Start of Frame signal in the simulator mode. When SOF is enabled, indicated by the SOF LED, a Start of Frame signal is transmitted to the Baud Acquisition chassis. If SOF is turned off, the Start of Frame signal is suppressed.

BIT ERROR — Bit Error is a momentary switch that will cause a single error to be inserted into the simulator data stream.

2.4. DATA CONFIGURATION The Data Configuration group consists of the following rocker switches:

INT/EXT — When the INT/EXT rocker switch is placed in the INT position the BERT is configured as a simulator that may replace many of the AMTD system chassis, as demonstrated in Figure 1. In the internal (simulator) mode the BERT uses data obtained from high speed PROMs. The data is read out in 3 bit symbol form and applied to the modulator.

When the INT/EXT rocker switch is placed in the EXT position the BERT is configured to accept 3 bit symbols and the 80 MHz clock from an external source (Burst Generator). The external data is used to drive the digital modulator and the simulator is no longer functional.

The INT/EXT switch also determines which Sub-Burst window[1] (error enable) signal is applied to the bit error rate logic (see Figure 3). If the BERT is configured as a simulator (INT asserted) then the simulator Sub-Burst Window is used. If EXT is asserted then the signal which is applied to the input labeled ERR EN on the front panel (in the BERT group) will be utilized.

---

1 The term Sub-Burst Window and Error Enable are interchangeable and refer to the same signal.

The following group of switches are only valid when in simulation mode (INT asserted):

COHRNT/ NON COHRNT — The COHRNT/NON COHRNT mode is used to simulate non-coherent or coherent quadrature detection and is thus only valid when the BERT is being utilized as a simulator to replace the Quadrature Detector and the modulator, as shown in Figure 2c. When the simulator is in the coherent mode (COHRNT asserted) the 8-PSK constellation is constant and the data symbol / phase relationship is fixed. When the simulator is in the non-coherent mode the 8-PSK constellation is shifted by 11.25° between each burst. This shift approximates the continual constellation rotation that takes place during non-coherent quadrature detection.

SNGL/ DUAL — If the simulator is in the Burst mode (refer to the following paragraph) the SNGL/DUAL mode will determine whether one or two bursts will be sent with each frame. In dual mode two bursts of 512 symbols are generated per frame. The symbol (80 Mhz) clocks will be coherent, but have a phase shift of at least 120°.

CONT/ BURST — If the CONT/BURST switch is in the CONT position the simulator will generate data according to the setting of the STEP/DATA switch (refer to the following paragraph). If the simulator is in the Burst mode then a frame will be generated with its associated control signals. The frame content will be dictated by the SNGL/DUAL switch.

STEP/ DATA — If the simulator is in the continuous mode and STEP is asserted the simulator will apply a zero data symbol and a phase offset, determined by the phase DIP switches, to the modulator. This enables the user to step through the 8-PSK constellation statically in order to adjust the modulator's DACs and the carrier acquisition DACs.

In DATA mode the simulator transmits burst data continually without start of frame reference signals.

2.5. TEST POINTS This group has the following outputs which are AC coupled:

80 CLK	80 MHz clock derived from XTAL 1 input.
240 CLK	240 MHz clock derived from XTAL 1 input.
ERR EN	Error Enable signal which is used to enable bit error rate counting.
SOF	Start of frame signal generated when the BERT is in the simulator mode.
DEMOD DATA	Serial 240 MBPS Demodulated data that is applied to the bit error rate logic.
TEST DATA	Serial 240 MBPS simulator data from the symbol data PROMs.
SYNC 1	4 nS pulse which occurs once per pseudorandom sequence for Data 1.
SYNC 2	4 nS pulse which occurs once per pseudorandom sequence for Data 2.
DATA 1	240 MBPS $2^{11}-1$ serial PN data sequence.
DATA 2	240 MBPS $2^{11}-1$ serial PN data sequence.

2.6. BERT The Bit Error Rate Test group contains the following inputs:

ERR INJ	Injects a single error into the simulator data steam for every positive transition that occurs. ERR INJ is an ECL level signal.
ERR EN	If the BERT is in the external mode (EXT asserted) then ERR EN controls when the bit error rate logic is enabled. ERR EN is a positive asserted, ECL level signal.

The Bit Error Rate Test group contains the following outputs which are AC coupled:

ERR CNT	ERR CNT is asserted 3 times for each bit error that is detected in the demodulated data.
DATA CNT	DATA CNT is asserted each time a demodulated data bit is received by the bit error rate logic.

2.7. **PN/CLK** The PN/CLK group contains the connecter interface for the PN data generator hardware. The group contains the following ECL coupled inputs:

XTAL 1	240 MHz clock source used to generate DATA 1 and CLK 1 outputs. The XTAL 1 input will also be utilized to derive the clocks used by the simulator hardware.
XTAL 2	240 MHz clock source used to generate DATA 2 and CLK 2 outputs.

The PN/CLK group contains the following ECL coupled outputs:

DATA 1	240 MBPS 2^{11}-1 serial PN data sequence.
DATA 2	240 MBPS 2^{11}-1 serial PN data sequence.
CLK 1	240 MHz clock derived from XTAL 1 input.
CLK 2	240 MHz clock derived from XTAL 2 input.

3. REAR PANEL

The rear panel, shown in Figure 6, consists of the following groups:

3.1. **DEMODULATOR** The demodulator group consists of 4 pair of ECL differentially driven signals that are generated by the simulator hardware and are to be connected to the Carrier Acquisition or Baud Acquisition chassis, depending on the test configuration. See Figure 2.

80 CLK	80 MHz symbol clock
240 CLK	240 MHz clock
SOF	Start of Frame signal transmitted at the beginning of each frame if the SOF switch is asserted (see section 2.3).
T-DBT	Simulated detected baud transition signal. A 2 nS pulse is transmitted each time a data symbol differs from the previous data symbol.

3.2. **BERT** The BERT group consists of 4 pair of ECL differential signals that are utilized by the BERT logic. The output test signals may be used to perform diagnostic and baseline checks on the BERT logic by connecting them to the BERT group inputs. The outputs consist of the following signals:

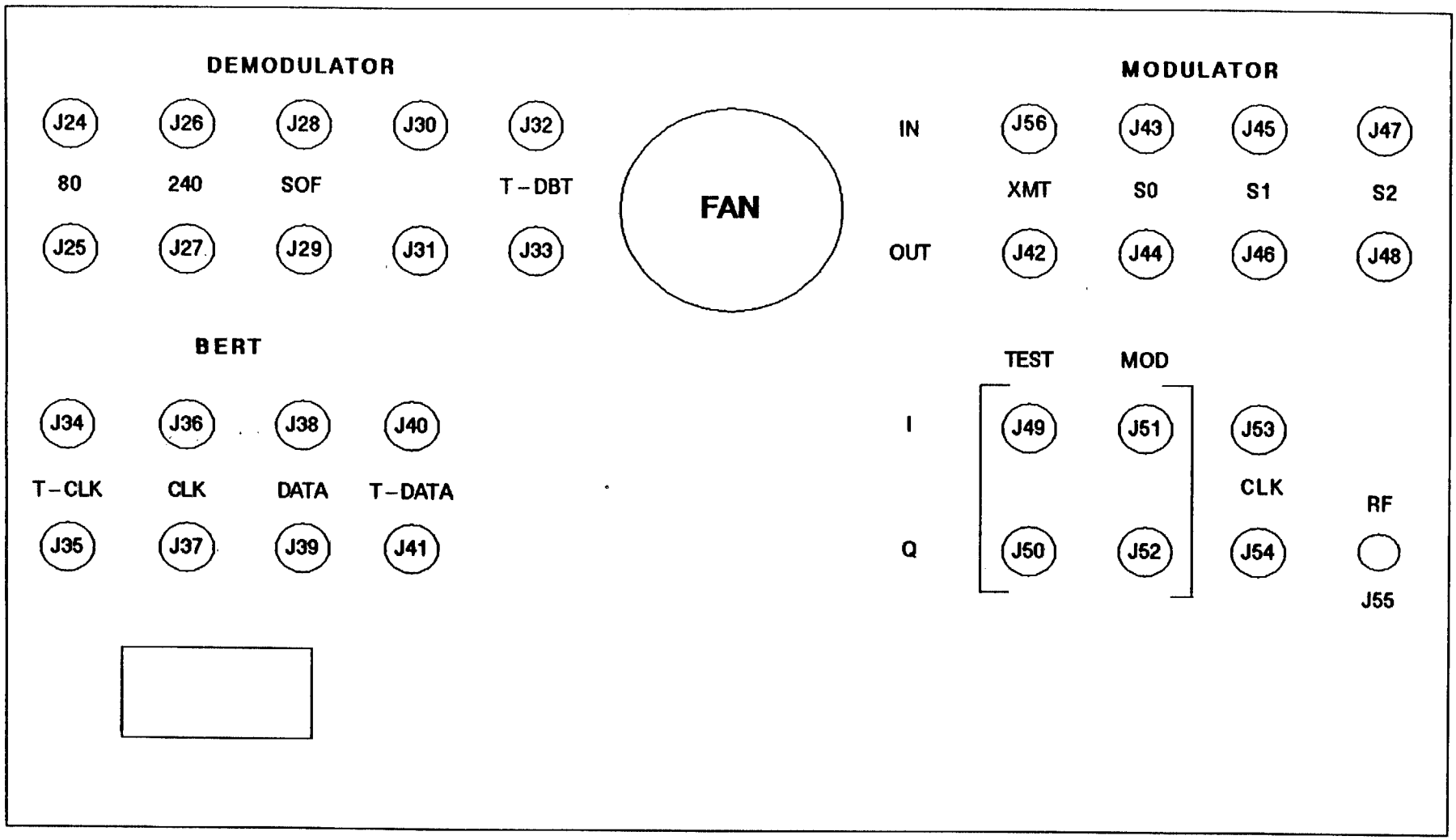


FIGURE 6

REAR PANEL

T-CLK 240 MHz clock generated by the simulator hardware and aligned with the T-DATA signal.

T-DATA 240 MBPS frame data generated by the simulator hardware.

The BERT group consists of the following inputs:

CLK 240 MHz clock to be utilized by the BERT logic.

DATA 240 MBPS serial data to used to perform bit error rate testing.

By connecting the test outputs to the BERT inputs the BERT logic can be tested to insure that it is not contributing to the system bit error rate. Errors may also be inserted into the test data by utilizing the BIT ERROR switch (see section 2.3) or BIT ERR input (see section 2.6), to ensure that the BERT logic is performing correctly.

3.3. **MODULATOR** The Modulator interface group consists of both digital ECL coupled signals and analog I and Q signals. The digital input signals consist of the following:

XMT Transmit control used to enable the carrier to the modulator.

S0 Least significant symbol data bit

S1 Middle significant symbol data bit

S2 Most significant symbol data bit

CLK 80 MHz clock used to drive the digital portion of the modulator. Must be synchronous with the input symbol data S0-S2. The positive edge of the clock should be within ± 1 nS of data baud center.

The digital outputs consist of the following:

XMT Transmit control signal which is asserted during the transmission of the simulator generated bursts.

S0 Least significant symbol data bit

S1 Middle significant symbol data bit

S2 Most significant symbol data bit

The digital inputs are used to control the modulator when in the external mode (EXT asserted, refer to section 2.4), and the digital outputs are used to simulate the Burst Generator when in the internal (simulator) mode.

The analog input signals consist of the following:

MOD I	Modulator In-phase signal
MOD Q	Modulator Quadrature-phase signal
RF	Carrier input

The analog output signals consist of the following:

TEST I	In-phase signal generated from the COSINE LUT.
TEST Q	Quadrature-phase signal generated from the SIN LUT.

When the simulator is being utilized to replace the modulator and the Quadrature Detector, as shown in Figures 2.b-c, then the TEST I and TEST Q outputs would be connected to the I and Q inputs of the Carrier Acquisition chassis. When the simulator is not being utilized (EXT asserted) then the TEST I and TEST Q output should be connected to the MOD I and MOD Q inputs in order to utilize the modulator. As shown in Figure 4, the analog output signals represent the separation of the digital portion of the modulator from the RF portion, which is driven by the analog inputs.

4. INTERNAL CONTROLS

The BERT simulator hardware provides the following switches on the A2 logic tray, card 1, located as shown in Figure 7, to control the operation of the simulation mode.

o	Guard (C19-TOP)	These switches set the number of guard symbols between bursts.
o	Phase Offset (C19-BOTTOM)	For these switches to be active the chassis has to be in continuous and step mode on the front panel. The phase offset switches rotate the 8-PSK constellation by 11.25° per increment. This facilitates static testing and adjustment of the 8-PSK analog hardware.

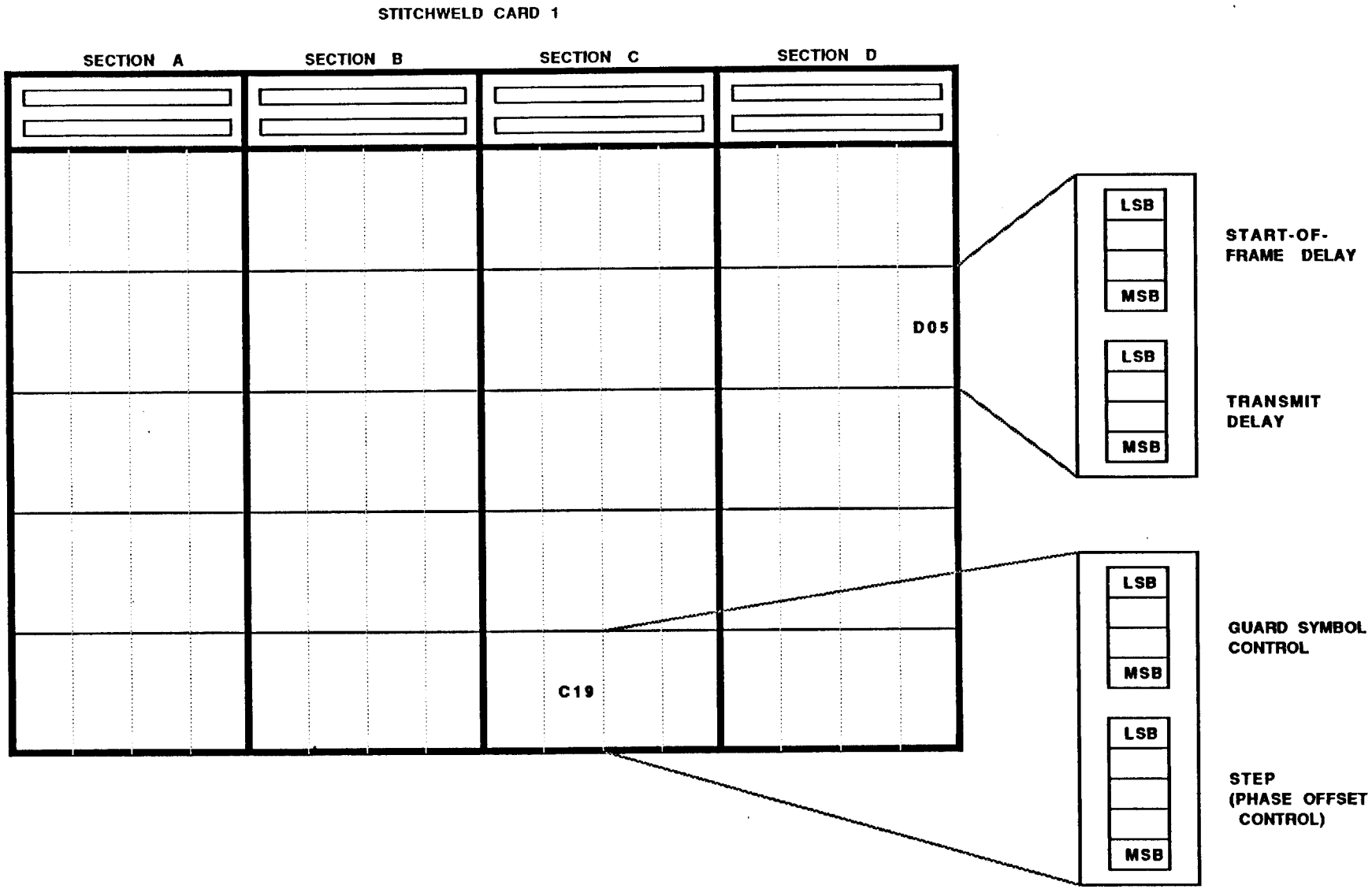


FIGURE 7

BERT
INTERNAL CONTROLS

o	Start-of-Frame (SOF-D5-TOP) (Burst 1)	The Burst 1 signal is asserted during the transmission of Burst 1. The rising edge of this signal is the Start-of-Frame indicator. These switches can delay the Burst 1 signal by a number of steps. Each step is 12.5 nS.
o	Transmit (D5-BOTTOM)	The simulator provides a Transmit control signal to be used by the modulator to enable the carrier. These switches can delay the start of this control signal by a number of steps. Each step is 12.5 nS.

5. OPERATION

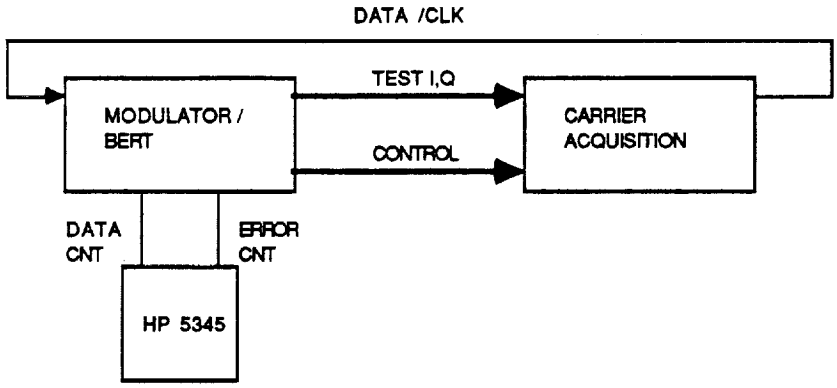
5.1. PN DATA GENERATOR The following steps outline the procedure for operating the PN data generator:

1. Connect a 240 MHz ECL compatible source to XTAL 1.
2. If two PN data sources are required connect a second 240 MHz ECL compatible source to XTAL 2.

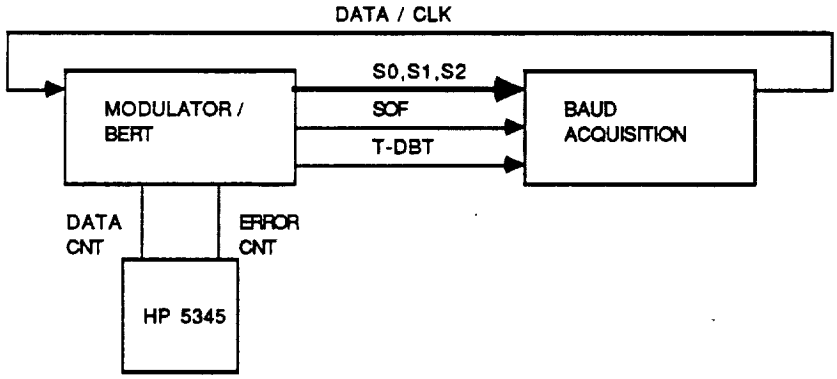
The data and clock outputs are located on the front panel as outlined in section 2.7.

5.2. SIMULATOR The BERT maybe configured to simulate many portions of the overall AMTD system configuration. Some of the possible system simulation setups are shown in Figure 2, which has been duplicated in Figure 8 for the readers convenience. The following steps will outline general procedures that are required whenever the BERT is utilized as a simulator:

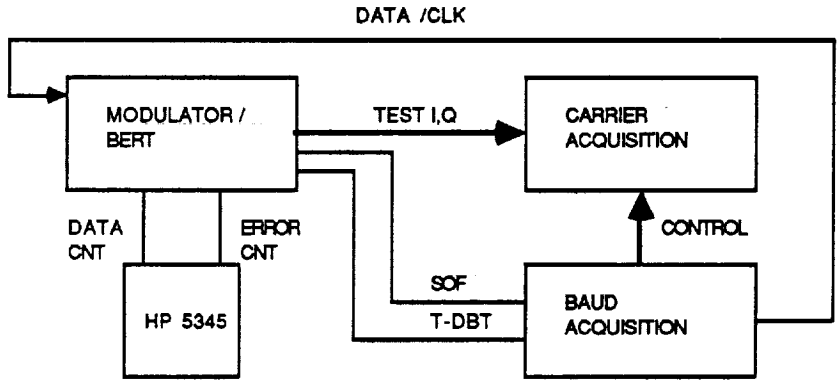
1. Connect a 240 MHz source to the XTAL 1 input located in the PN / CLK section on the front panel.
2. Place the BERT in the simulation mode by asserting the INT switch located in the DATA CONFIGURATION section on the front panel.



A. Simulator replacing the Modulator, Quadrature Detector, and Baud Acquisition Chassis



B. Simulator replacing the Modulator, Quadrature Detector, and Carrier Acquisition Chassis.



C. Simulator replacing the Modulator, and Quadrature Detector

FIGURE 8

SIMULATION CONFIGURATIONS

3. Make the desired data configuration selections (Refer to section 2.4).

4. Make the necessary chassis interconnections for the particular simulation being performed.

The following sections contain the specific information required to carry out the simulation configurations depicted in Figure 8:

5.2.1. Modulator, Quadrature Detector, and Baud Acquisition Chassis Simulation This simulation mode allows the Carrier Acquisition Chassis to be isolated from the overall system. The following specific chassis interconnections should be made:

1. Connect the Test I (J49) and Test Q (J50) outputs from the rear panel of the BERT to their respective I and Q inputs on the rear panel of the Carrier Acquisition chassis.

2. Connect the following differential output signals located on the BERT rear panel in the Demodulator section (See Figure 6) to their respective inputs located on the rear of the Carrier Acquisition chassis:

   - 80 MHz clock (J24,J25)
   - 240 MHz clock (J26,J27)
   - SOF (J28,J29)

3. Connect the respective Carrier Acquisition chassis outputs to the following BERT rear panel inputs which are located in the BERT section (See Figure 6):

   - CLOCK (240 MHz) (J36, J37)
   - DATA (J38, J39)

4. Adjust the Carrier Acquisition Chassis timing at the Analog-to-Digital Card to reflect the system timing change.

5. Perform BER testing. (See section 5.3)

5.2.2. Modulator, Quadrature Detector, and Carrier Acquisition Chassis Simulation This mode allows the Baud acquisition chassis to be isolated from the overall system. The following specific chassis interconnections should be made:

1. Connect the following differential output signals located on the BERT rear panel in the Modulator section (See Figure 6) to their respective inputs located on the rear of the Baud Acquisition chassis:

   - S0 (Least significant data bit) (J44)
   - S1 (Middle significant data bit) (J46)
   - S2 (Most significant data bit) (J48)

2. Connect the following differential output signals located on the BERT rear panel in the Demodulator section (See Figure 6) to their respective inputs located on the rear of the Baud Acquisition chassis:

   - SOF (J28,J29)
   - T-DBT (J32,J33)

3. Connect the respective Baud Acquisition chassis outputs to the following BERT rear panel inputs which are located in the BERT section (See Figure 6):

   - CLOCK (240 MHz) (J36, J37)
   - DATA (J38, J39)

4. Perform BER testing. (See section 5.3)

5.2.3. Modulator, and Quadrature Detector Chassis Simulation This mode allows the "digital" portion of the demodulator to be isolated and tested. The following specific interconnections should be made:

1. Connect the Test I (J49) and Test Q (J50) outputs from the rear panel of the BERT to their respective I and Q inputs on the rear panel of the Carrier Acquisition chassis.

2. Connect the following differential output signals located on the BERT rear panel in the Demodulator section (See Figure 6) to their respective inputs located on the rear of the Baud Acquisition chassis:

   - SOF (J28,J29)
   - T-DBT (J32,J33)

3. Connect the respective Baud Acquisition chassis outputs to the following BERT rear panel inputs which are located in the BERT section (See Figure 6):

   - CLOCK (240 MHz) (J36, J37)
   - DATA (J38, J39)

4. Make the necessary chassis interconnections between the Baud Acquisition and Carrier Acquisition chassis.

5. Adjust the Carrier Acquisition Chassis timing at the Analog-to-Digital Card to reflect the system timing change.

6. Perform BER testing. (See section 5.3)

5.3. BERT logic The following steps outline the procedure for performing bit error rate testing:

1. Connect the demodulated data and clock to their respective inputs on the rear panel. The more positive side of the differential signal should be connected to the top most connector.

2. Connect the ERR CNT output from the front panel to the B channel input of an HP 5345 electronic counter.

3. Connect the DATA CNT output from the front panel to the A channel of the HP 5345 electronic counter.

4. Configure the HP 5345 in the B/A mode and observe the rate on the counter.

5. After waiting the appropriate time for the particular test being conducted, see the test procedure document for a complete table, observe the final rate on the counter and divide by three to obtain the true BER.

5.4. MODULATOR The Modulator may receive its data input from either the simulator hardware or from an external source. The following steps outline the procedure necessary in order to operate the modulator from an external source (such as the Burst Generator):

1. Connect the following rear panel input signals:

- RF - J55 (3.373056 GHz carrier at TBD dBm)
- XMT IN - J56 (Carrier enable signal)
- S0 - J43 (LSB symbol data)
- S1 - J45 (Middle SB symbol data)
- S2 - J47 (MSB symbol data)
- CLK - J53 (80 MHz clock)

2. On the rear panel, connect the TEST I output to the MOD I input, and the TEST Q output to the MOD Q input.

3. Place the INT/EXT rocker switch in the EXT position.

4. Align the positive edge of the symbol clock to within ± 1 nS of the data baud center.

SPECIFICATION: SE587939
VER: 5.0
9-02-88

SPECIFICATION

MODULATOR / BERT
(AMTD)

TABLE OF CONTENTS

1.0 SCOPE

This specification establishes the performance, design, test and manufacture requirements for the Modulator / BERT for the Advanced Modulation Technology Development (AMTD) system.

2.0 APPLICABLE DOCUMENTS

The latest issues of the following documents are a part of this specification.

(a)	NAS 3-24678	Advanced Technology Satellite Demodulator Development, Statement of Work
(b)	17 Jun 1986	Preliminary Design Review Package
(c)		AMTD System Specification

3.0 DESIGN REQUIREMENTS

3.1 Functional Description

The Modulator / BERT, as shown in Figure 1, contains two major parts: The modulator and the Bit Error Rate Test hardware.

The digital modulator, shown in Figure 2, consists of the Sin and Cosine look up table (LUT) Read Only Memories (ROM), the Digital-to-Analog Converters (DAC), the double-balanced mixers, phase shifter and RF combiner. The 8-PSK modulation is actually defined in the ROM LUTs, which have been programmed for the correct constellation. By simply reprogramming the ROM LUT any constellation may be obtained. The modulator utilizes a carrier centered at 3.373056 GHz.

The Bit Error Rate Test (BERT) portion of the Modulator / BERT chassis actually contains three major hardware functions: Pseudo-random data and clock generation, AMTD system hardware simulator, and Bit Error Rate Test logic.

The PN data generator consists of two separate data / clock sources which produce two individual, non-coherent 240 MBPS serial data streams with their associated 240 MHz clocks. The PN generator produces a sequence with a period of $2^{11}-1$ bits and requires a 240 MHz clock input in order to operate.

The Simulator portion of the BERT allows several portions of the AMTD system to be eliminated for testing purposes. When in "simulation" mode the BERT chassis will produce all of the signals necessary to replace the Burst Generator, Modulator, Quadrature Detector, and either the Baud Acquisition or Carrier Acquisition chassis. The different possible test configurations are shown in Figure 3.

The simulator facilities smooth system integration by allowing each chassis to be brought on line individually. This increases system confidence as each level of the system integration may be fully tested.

The simulator generates a shortened frame that is 1024 symbols in length (excluding guard symbols) for a dual burst frame, or 512 symbols for a single burst frame. The burst content is defined by the simulator data PROM which contains 512 x 4 bits of memory.

The actual Bit Error Rate Test logic, shown in Figure 7, consists of the same $2^{11}-1$ PN sequence logic used in the PN Data generator. The PN generator may be considered as an encoder that takes a constant logic state and encodes it with the $2^{11}-1$ PN sequence. The BERT logic then decodes the demodulated data stream and in the absences of bit errors reconstructs a "constant" logic state. By monitoring the transitions that occur on the output of the decoder the number of bit errors may be determined. By keeping track of the total number of data bits that have been received a bit error rate may be calculated. Because each data bit is compared three times in order to "decode" the data stream, the displayed error rate will be three times greater then the actual error rate.

3.2 Physical Description

The Modulator / BERT is a stand-alone chassis, that can be mounted in a rack. The front panel (7 inches high) and rear panel layouts are shown in Figure 4 and 5 respectively.

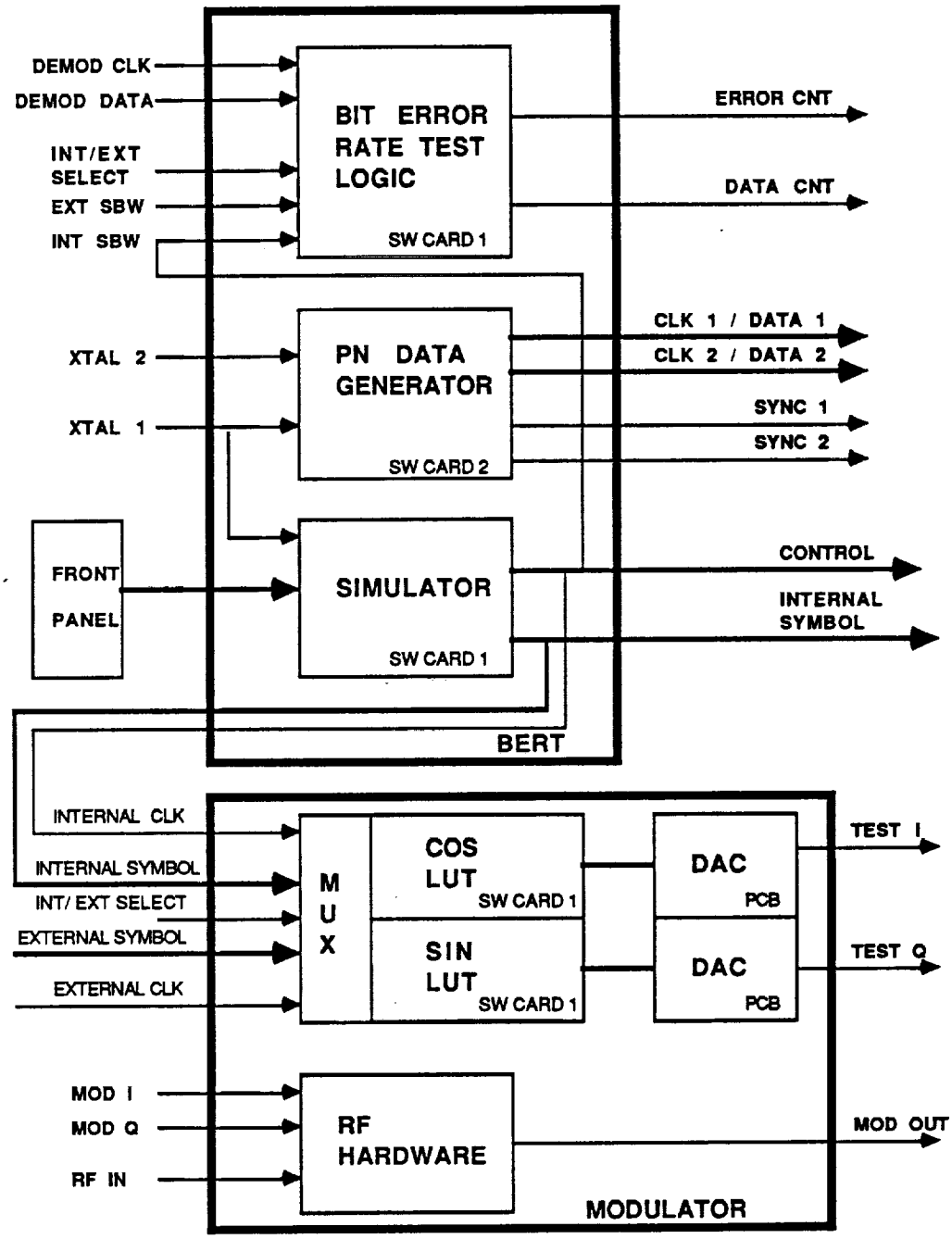


FIGURE 1

MODULATOR / BERT
BLOCK DIAGRAM

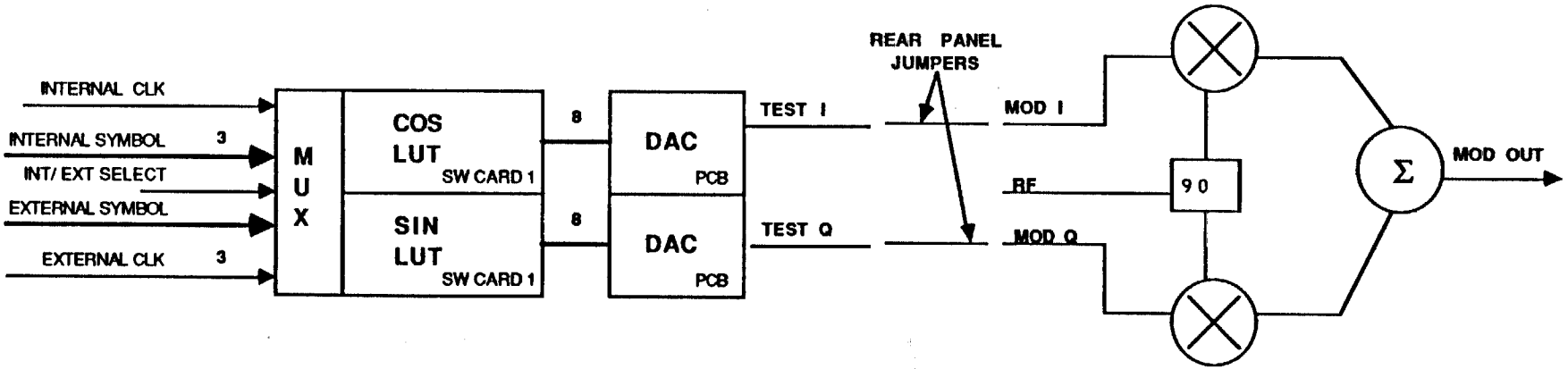
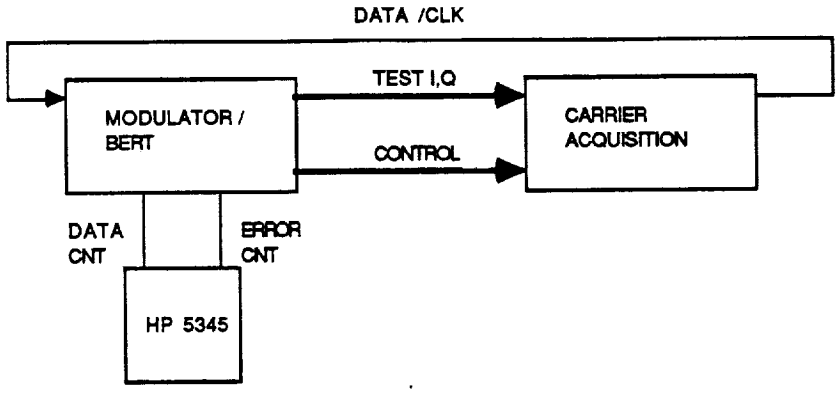


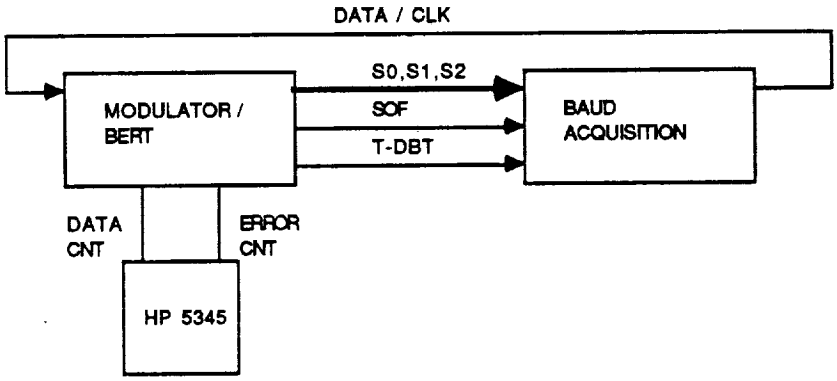
FIGURE 2

MODULATOR

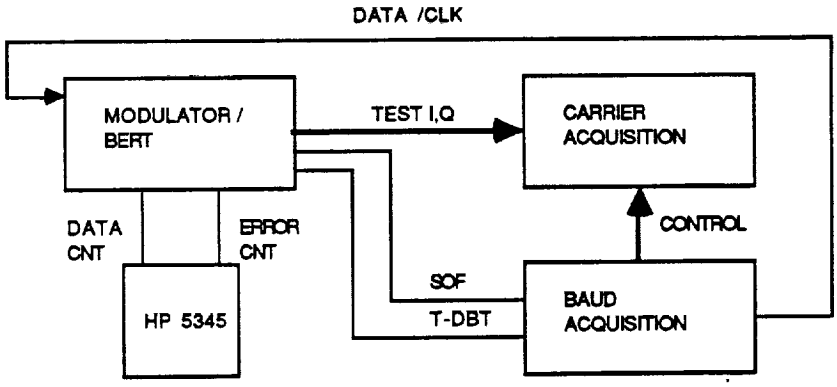
BLOCK DIAGRAM



A. Simulator replacing the Modulator, Quadrature Detector, and Baud Acquisition Chassis



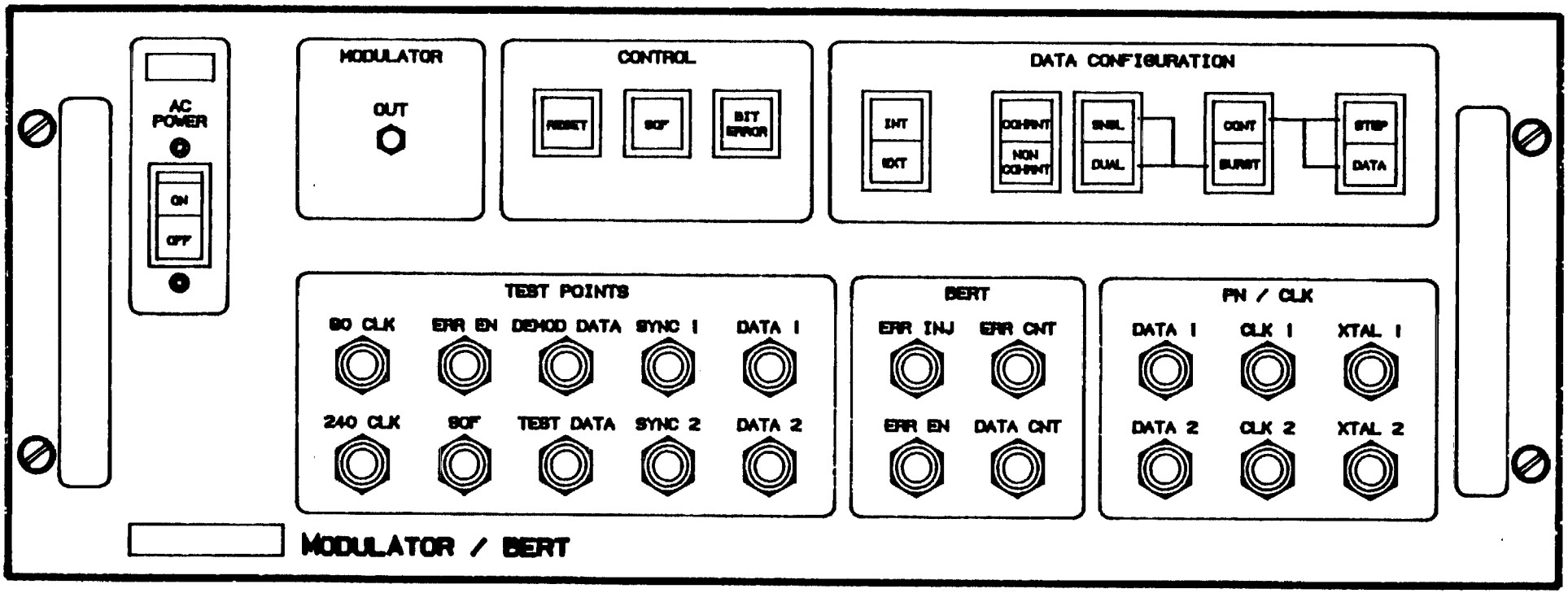
B. Simulator replacing the Modulator, Quadrature Detector, and Carrier Acquisition Chassis.



C. Simulator replacing the Modulator, and Quadrature Detector

FIGURE 3

SIMULATION CONFIGURATIONS



A00021
MISC

FIGURE 4

FRONT PANEL

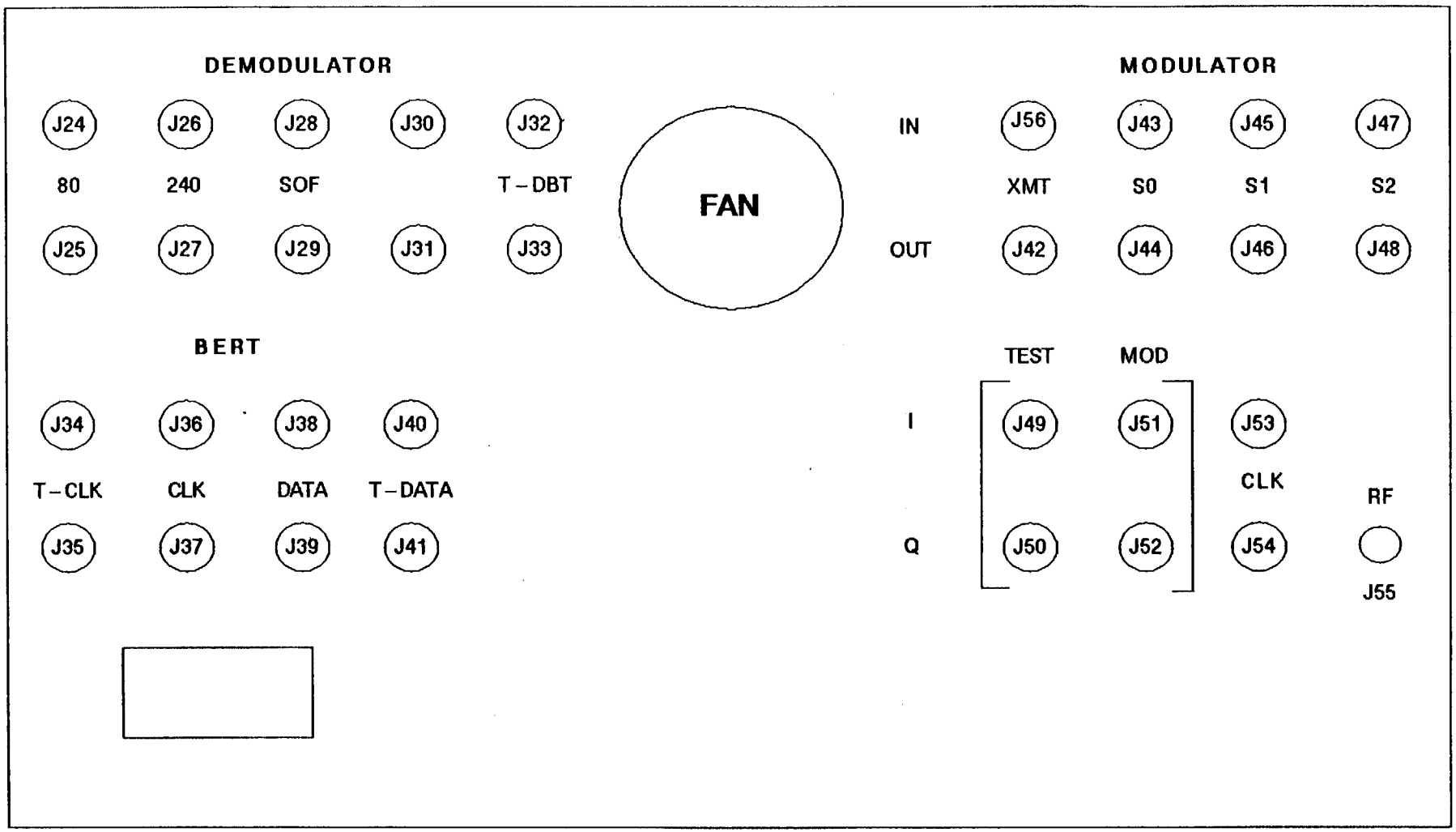


FIGURE 5

REAR PANEL

3.3 Performance Specifications

The Modulator / BERT chassis has two major parts: The Modulator which consists of the digital Read Only Memory (ROM) Look Up Table (LUT) and the analog RF hardware; and the Bit Error Rate Test hardware which contains the PN data / clock source, the AMTD system simulator and the BER logic.

3.3.1 Modulator The digital portion of the modulator is located on stitchweld card 1, which is mounted on tray A2. The digital hardware includes the ROM LUTs, latches, and a multiplexer (which allows the user to choose whether symbols from the Burst Generator or symbols from the BERT simulator are used by the modulator). Analog-to-Digital convertor boards for the I and Q channels are located on separate printed circuit boards which are also mounted on tray A2. The RF hardware is mounted on tray A1.

The modulator will accept baseband modulation data from 0-100 MHz and may utilize carrier inputs from 1-4 GHz. The intermediate I and Q outputs from the DACs will have an approximate settling time of 3 nS. The phase error will be less than 1° and the magnitude error will be less than 7 mV.

3.3.2 BERT

3.3.2.1 PN / Clock Source The pseudo-random data generator hardware is located on stitchweld card 2, which is a two section card mounted on top of stitchweld card 1 on tray A2. The PN data generator will produce a serial data stream that repeats after every $2^{11}-1$ bits. The generator will produce data at rates up to 300 MBPS.

3.3.2.2 AMTD Simulator The Simulator, shown in Figure 6, generates bursts of symbols, separated by guard times. In the single mode of operation all bursts are generated from the same 80 MHz clock. In the dual mode of operation the bursts are generated from alternate 80 MHz clocks. These two clocks are coherent, but they have a phase shift of at least 120°.

A burst has 512 symbols, and consists of pre-amble zero symbols (1-255), "unique word" symbols (8),

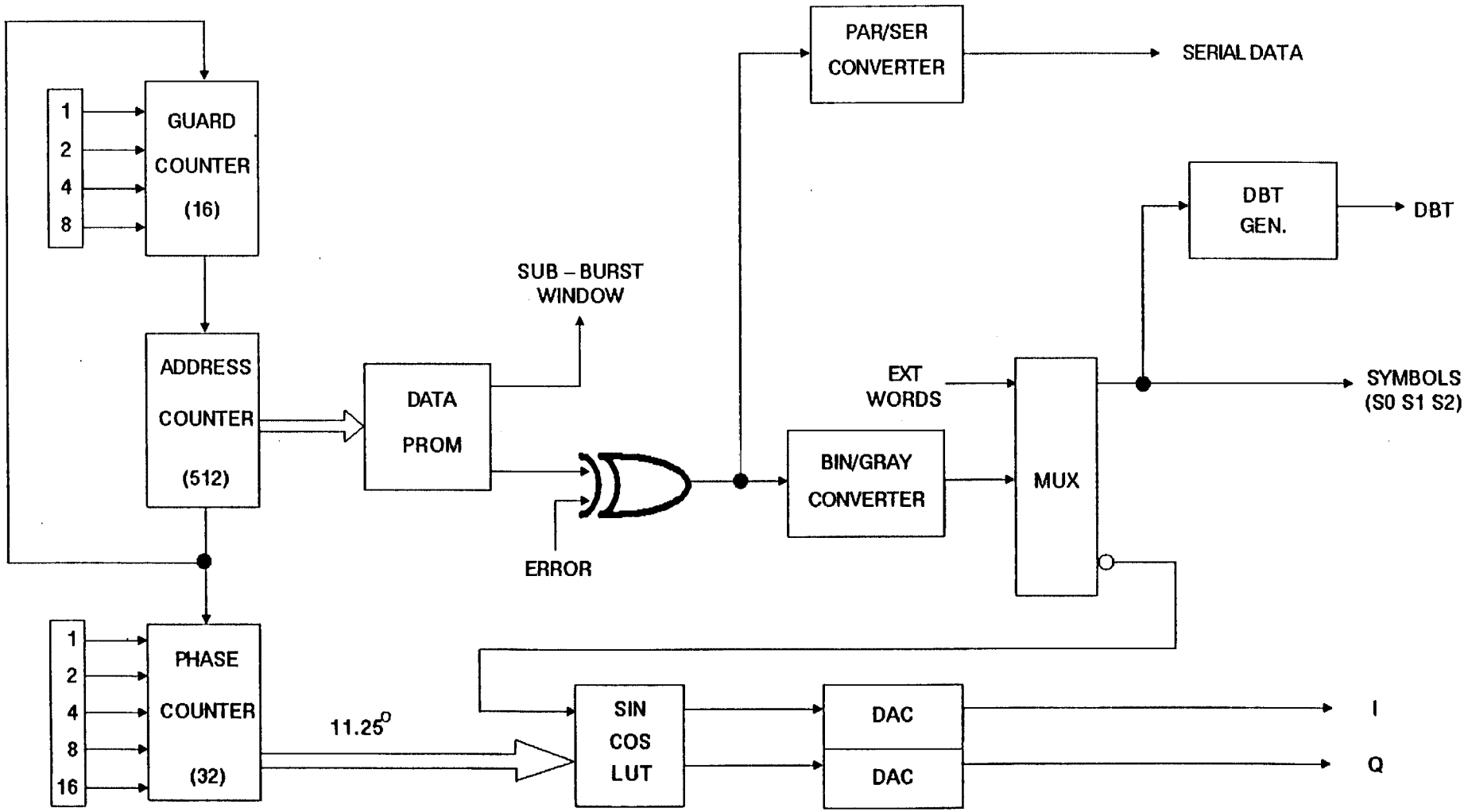


FIGURE 6
SIMULATOR
BLOCK DIAGRAM

and data symbols. The burst configuration is determined by the contents of the simulator data PROMs. The PROM memory consists of 512 x 4 bits. The simulator can inject single bit errors in the burst data.

The guard time between bursts is programmable from 2 to 16 symbols.

The simulator provides the 3 bit symbols in parallel format (S0 S1 S2) at 80 MSPS, in serial format (most significant bit first) at 240 MBPS, or in an 8-PSK constellation as I and Q channels. The Phase Counter can rotate this 8-PSK constellation in steps of 11.25° per burst.

The DBT (Detected Baud Transition) generator provides a pulse of 2 nS, whenever a symbol differs from the previous one.

The simulator provides a Sub-Burst Window (SBW) for the Error Logic. The start of this SBW signal is adjustable from 1-16 data symbols, and the length of this window is adjustable from 1-512 data symbols.

3.3.2.3 Bit Error Rate Test Logic The Error Logic, shown in Figure 7, has a pseudo-random sequence generator, consisting of an 11 bit register and an exclusive or gate. It generates a sequence with a period of $2^{11}-1$ symbols, with a primitive polynomial of $x^{11} + x^2 + 1$. The Error Logic compares the incoming data bits with the generated data bits, and provide an error pulse when these bits differ. Since the "error" also propagates through the register a total of three error pulses will be generated for each difference.

The logic also generates a data pulse for each clock signal received. These pulses are provided to an external BER counter during the Sub-Burst Window.

3.3.3 Control and Status Specification

Switches on the front panel control the operation of the BERT as specified in section 3.3.3.1.

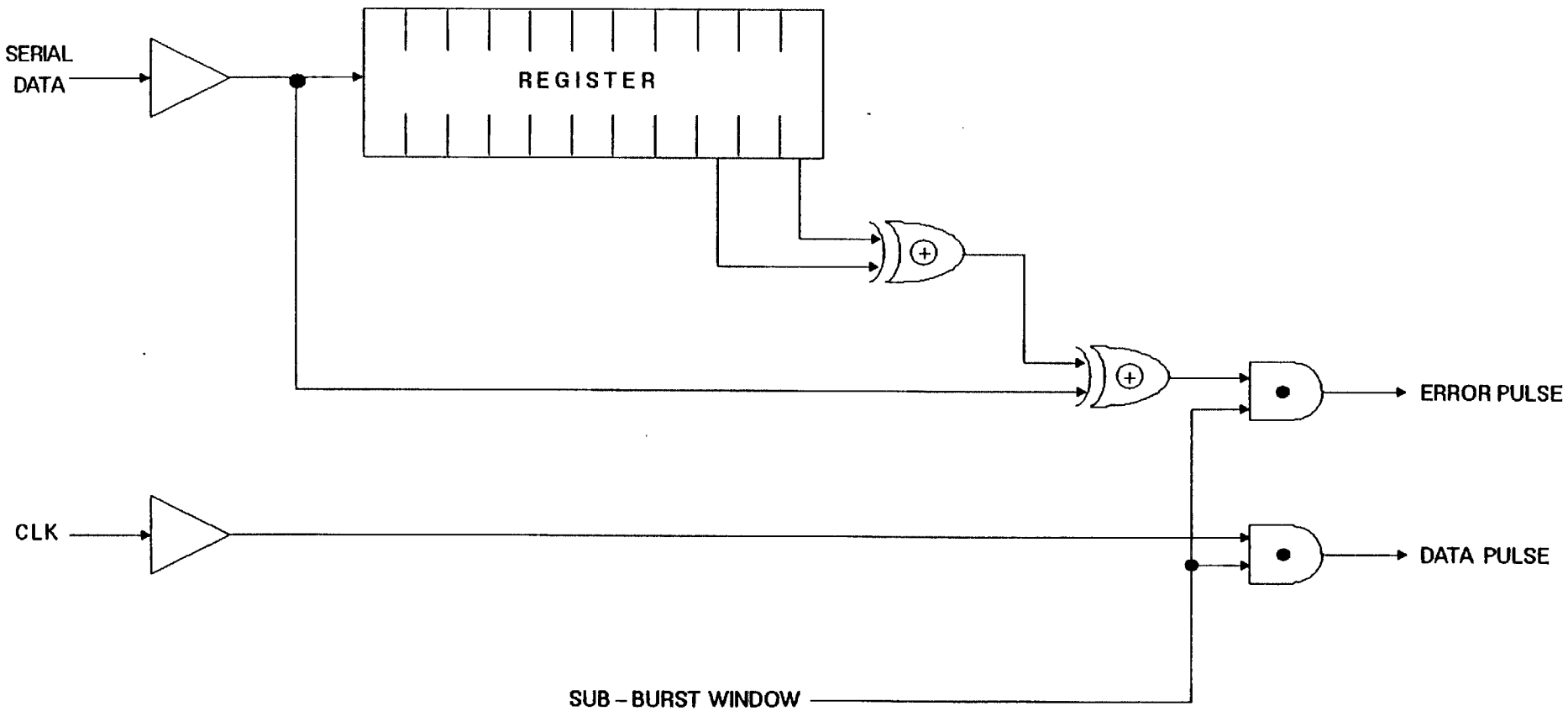


FIGURE 7

BIT ERROR RATE TEST LOGIC

Switches on the A2 logic tray control the operation of the BERT hardware as specified in section 3.3.3.2.

The positions of the switches in sections 3.3.3.1 and 3.3.3.2 provide the status of the operation of the Modulator / BERT chassis.

3.3.3.1 Front Panel Controls. The Modulator / BERT provides the following switches on its front panel to control the operation of the chassis:

o Power On/Off	This switch controls the main power to the supplies in the chassis.
o Reset	Activating this switch initializes the chassis to the start of a burst.
o SOF	When SOF is asserted (LED on) the Start-of-Frame signal is transmitted with each frame that is sent. If SOF is not asserted (LED off) then the Start-of-Frame signal is suppressed.
o Bit Error	For each push of this switch one error is inserted into the burst.
o Ext/Int	In the Internal Mode of operation the BERT provides bursts as described in section 3.3.2.2. In the External Mode of operation the BERT provide symbols under total control of external inputs.

o	Coh./NonC	In the Coherent Mode the 8-PSK constellation remains at a fixed phase state determined by the Phase Offset DIP Switches. In the Non-Coherent mode the 8-PSK constellation rotates in 11.25° steps between bursts.
o	Single/Dual	In Single Mode only one burst of 512 symbols is generated per frame. In Dual Mode two burst of 512 symbols are generated per frame. The 80 MHz clocks are coherent, but have a phase shift of at least 120°.
o	Cont/Burst	In the Burst Mode the BERT provides bursts as described in section 3.3.2.2. In the continuous mode the BER Test Set provides the symbols as described for the next switch.
o	Step/Data	When in continuous mode: And in Data Mode the BERT provides bursts without guard symbols between burst.

In Step Mode the BERT provides one symbol, continuously. This symbol is set on the Phase Offset DIP switches described in section 3.3.2.2.

3.3.3.2 Internal Controls. The BERT provides the following switches on the A2 logic tray, located as shown in Figure 8, to control the operation of the simulator hardware.

- o Guard (C19-TOP) — These switches set the number of guard symbols between bursts.
- o Phase Offset (C19-BOTTOM) — For these switches to be active the chassis has to be in continuous and step mode on the front panel.

  The phase offset switches rotate the 8-PSK constellation by 11.25° per increment. This facilitates static testing and adjustment of the 8-PSK analog hardware.
- o Start-of-Frame (SOF-D5-TOP) (Burst 1) — The Burst 1 signal is asserted during the transmission of Burst one. The rising edge of this signal is the Start-of-Frame indicator.

  These switches can delay the Burst 1 signal by a maximum of 8 steps. Each step is 12.5 nS.

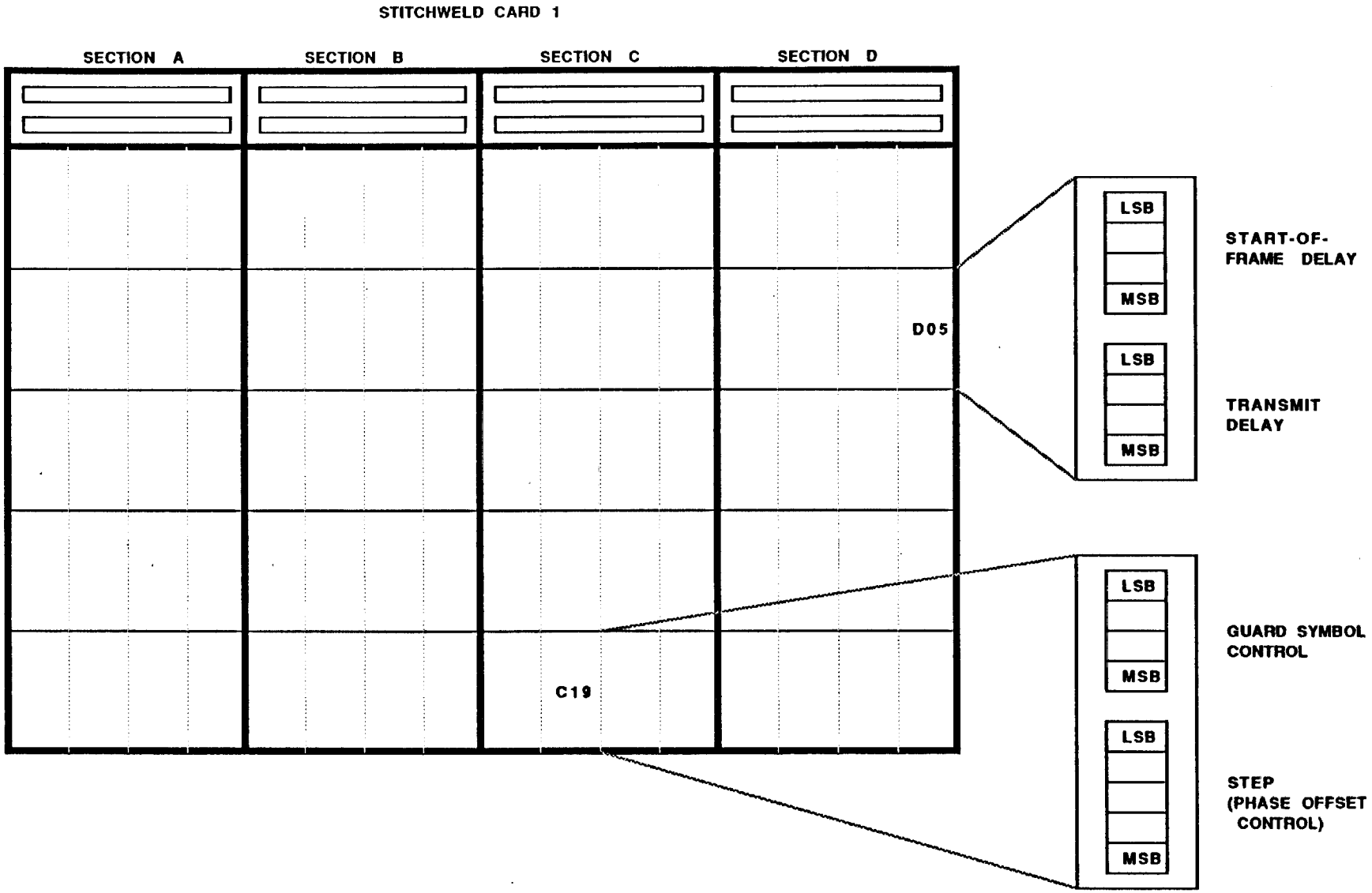


FIGURE 8

BERT
INTERNAL CONTROLS

o	Transmit (D5-BOTTOM)	The BERT provides a Transmit control signal to be used by the Modulator to enable the carrier. These switches can delay the start of this control signal by a maximum of 8 steps. Each step is 12.5 nS.

3.3.3.3 Monitoring Point. The front panel has 4 groups of monitoring points. The Modulator, Test Points, Bit Error Rate Test (BERT) group and the PN/Clock group.

I. Modulator This output is the 8-PSK modulated RF signal.

II. Test Points This group has the following outputs which are AC coupled:

o 80 CLK	80 MHz Symbol Clock derived from the XTAL 1 input when INT is asserted. 80 CLK is derived from the MOD CLK input when EXT is asserted.
o SOF	Start of Frame signal which is asserted for the duration Burst 1
o DEMOD DATA	Input Data to the Error Logic
o SYNC 1	4 nS pulse which occurs once per pseudo-random sequence for Data 1
o DATA 1	$2^{11}-1$ pseudo-random serial data

- o 240 CLK — 240 MHz Serial Clock derived from XTAL 1 input
- o ERR EN. — Sub-Burst Window
- o TEST DATA — Serialized Output Data from test PROM (240MBPS)
- o SYNC 2 — 4 nS pulse which occurs once per pseudo-random sequence for Data 2
- o DATA 2 — $2^{11}-1$ pseudo-random serial data

III. BERT Group This group has the following inputs at ECL logic levels:

- o ERR INJ — An error is inserted into the symbol, when this input changes from a logic "0" to a logic "1".
- o ERR EN — In External mode a logic "1" at this input provides a sub-burst window.

This group has the following outputs which are AC coupled:

- o ERR CNT — Error Count Pulse
- o DATA CNT — Data Count Pulse

IV. PN/CLK Group The P/N portion provides a $2^{11}-1$ pseudo random sequence with clock for the Burst Formatter chassis. Outputs at ECL levels:

- o DATA 1 — Serialized P/N data at 240 MBPS
- o CLK 1 — 240 MHz serial clock
- o DATA 2 — Serialized P/N data at 240 MBPS
- o CLK 2 — 240 MHz serial clock

CONN.	SIGNAL	INTERFACE
J24	80 MHz CLOCK OUT	CARRIER AC. – J6
J25	80 MHz CLOCK OUT – INV	CARRIER AC. – J14
J26	240 MHz CLOCK OUT	CARRIER AC. – J7
J27	240 MHz CLOCK OUT – INV	CARRIER AC. – J15
J28	TRANSMIT OUT	CARRIER AC. – J8
J29	TRANSMIT OUT – INV	CARRIER AC. – J16
J30	DBT – ANALOG	CARRIER AC. – J1
J31	DBT – INV ANALOG	CARRIER AC. – J9
J32	DETECTED BAUD TRANS. – TEST OUT	BAUD AC. – J3
J33	DETECTED BAUD TRANS. – TEST OUT – INV	BAUD AC. – J4
J34	TEST CLOCK OUT (SELF TEST)	SERIAL CLK – J36
J35	TEST CLOCK OUT – INV	SER CLK INV – J37
J36	SERIAL CLOCK IN	BAUD AC. – J17
J37	SERIAL CLOCK IN – INV	BAUD AC. – J18
J38	SERIAL DATA IN	BAUD AC. – J11
J39	SERIAL DATA IN – INV	BAUD AC. – J12
J40	TEST DATA OUT (SELF TEST)	SERIAL DATA – J38
J41	TEST DATA OUT – INV	SER DATA INV – J39
J43	SYMBOL BIT S0 IN	BURST GEN – J3
J45	SYMBOL BIT S1 IN	BURST GEN – J2
J47	SYMBOL BIT S2 IN	BURST GEN – J1
J42	START – OF – FRAME OUT	BAUD AC. – J1
J44	SYMBOL BIT S0 OUT	BAUD AC. – J5
J46	SYMBOL BIT S1 OUT	BAUD AC. – J7
J48	SYMBOL BIT S2 OUT	BAUD AC. – J13
J49	TEST I	CARRIER AC. – J5
J50	TEST Q	CARRIER AC. – J13
J51	MOD I	TEST I – J49
J52	MOD Q	TEST Q – J50
J53	MODULATOR SYMBOL CLOCK	BURST GEN – J21
J54	SPARE	
J55	3.373056 CARRIER INPUT	
J56	POWER 115VAC – 60Hz	

TABLE 3.4.1

BER TEST SET INTERFACE CONNECTORS

The clock group contains the following inputs at ECL levels:

- o XTAL 1 — 240 MHz serial clock source
- o XTAL 2 — 240 MHz serial clock source

3.4 Interface Specifications

This section describes the external interfaces. These interfaces are via the rear panel. Table 3.4.1 lists the connector assignments to the Carrier Acquisition and Baud Acquisition Chassis.

3.4.1 Carrier Acquisition Interface. The BERT provides the following test signals for the Carrier Acquisition Chassis:

3.4.1.1 Clock Signals. The BERT provides two clock signals to the Carrier Acquisition Chassis: 80 MHz and 240 MHz, both associated with the burst data.

The 80 MHz clock signal has a 33 percent duty cycle, and shall be coupled as shown in Figure 9.

The 240 MHz clock signal has a 50 percent duty cycle, and shall be coupled as shown in Figure 9.

3.4.1.2 Transmit Control Signals. The Transmit control signal indicates the presence of the burst when the (+) output is more positive than the (INV) output.

Burst $1/\overline{2}$ indicates the presence of one burst when the (+) output is more positive than the (INV) output, and the presence of the other burst when the (+) output is more negative than the (INV) output.

Both control signals are ECL driven and shall be DC coupled as shown in Figure 10.

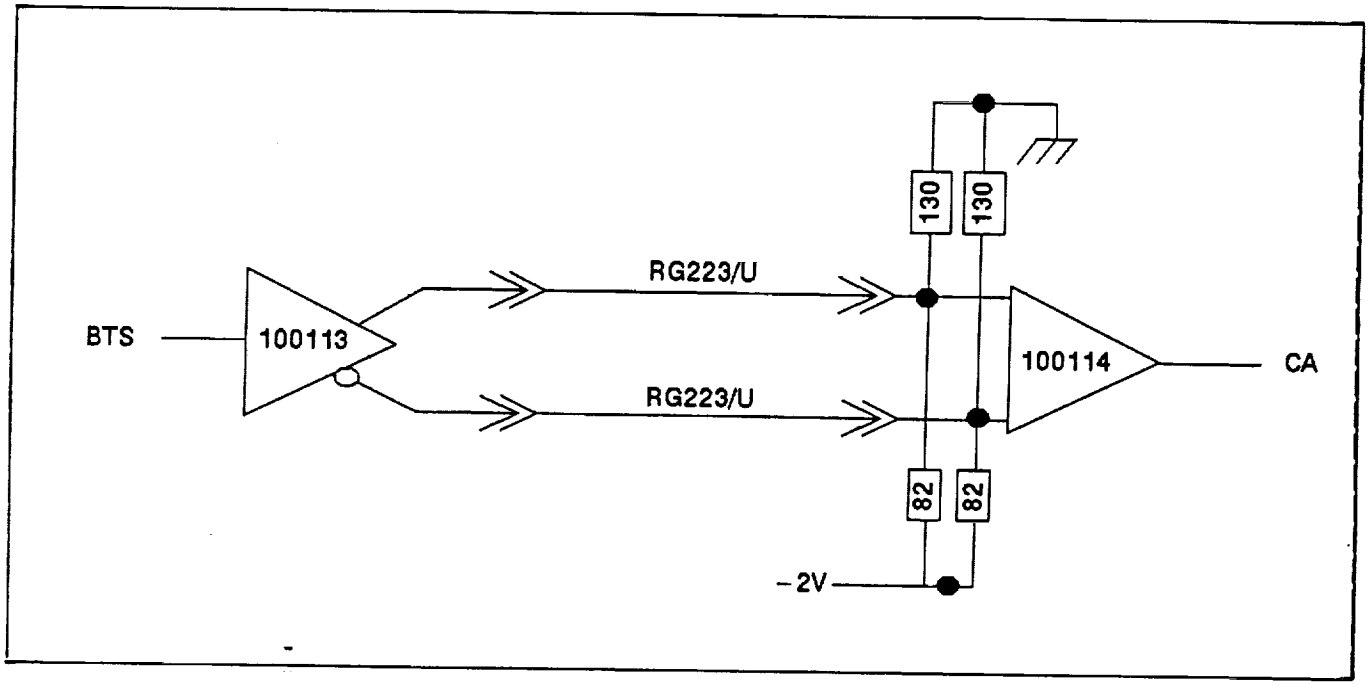


FIGURE 9
CLOCK INTERFACE

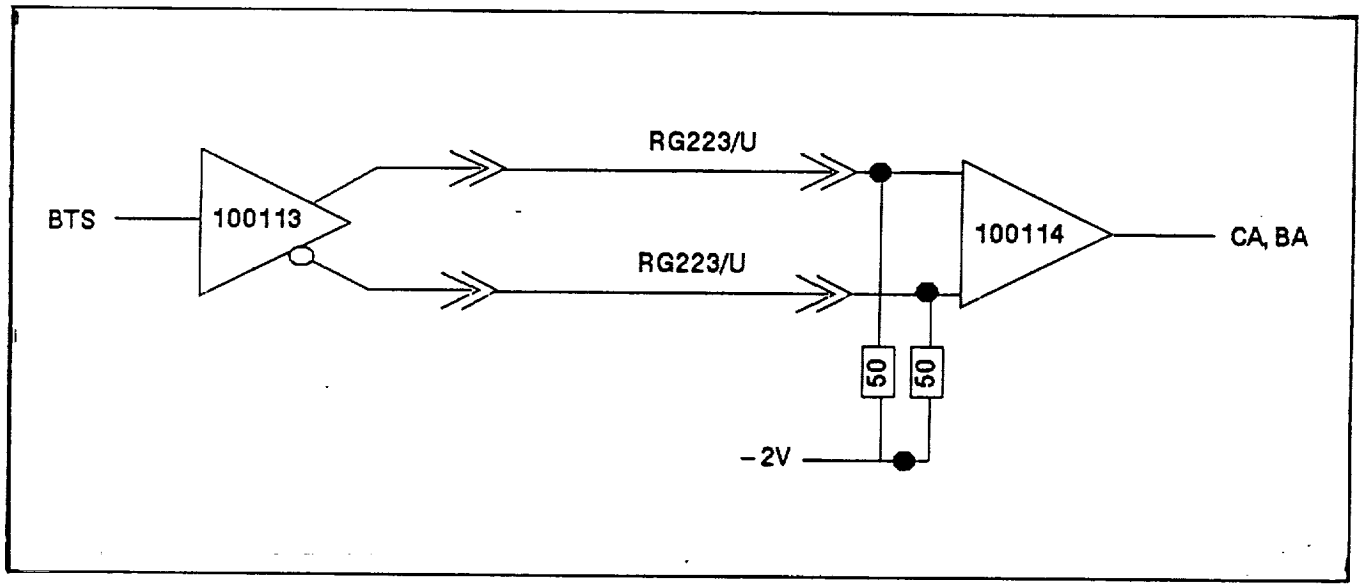


FIGURE 10
CONTROL INTERFACE

3.4.1.3 8-PSK Constellation Interface. The BERT provides two single ended analog data signals (Test I and Test Q), which are associated with the transmit control signal and the 80 MHz clock.

The analog data signals shall have the following performance:

- Data Rates. The outputs are analog signals to be recognized to change in steps at a rate of 80 mega steps per second.
- Analog Voltage. The analog outputs shall be measured in steps of 4 mVolts. The minimum voltage is -2 volts ±2% (binary equivalent is 000.000). The maximum voltage is 0 volts ±2% (binary equivalent is 111.111).
- Input Impedance. The data lines have an impedance of 50 ohm ±5% to ground.
- Interface Circuit. The single ended data lines shall be DC coupled as shown in Figure 11.

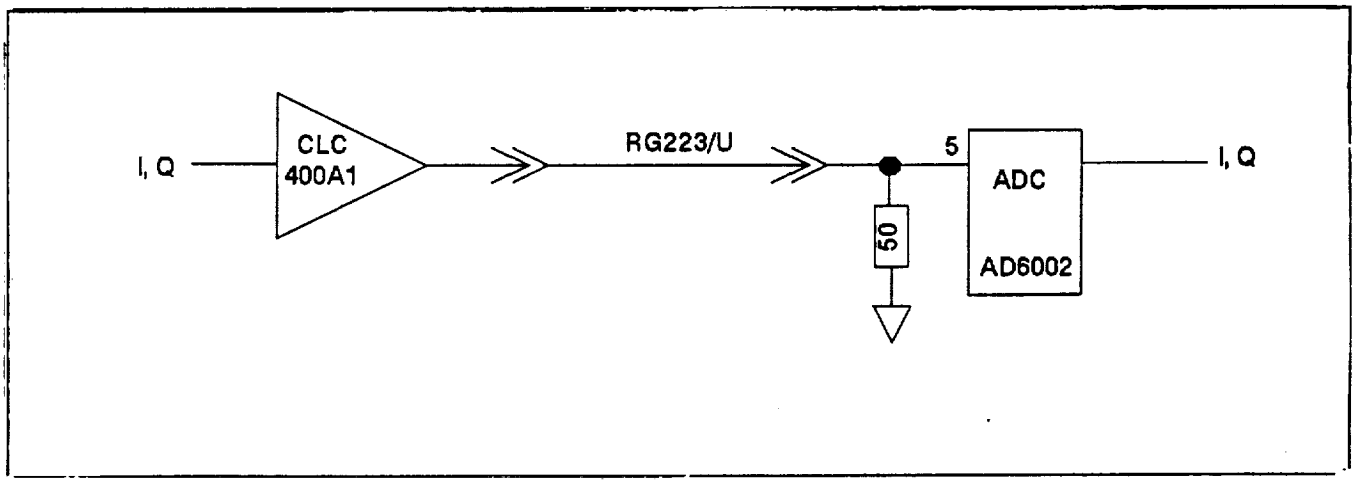


FIGURE 11
ANALOG INTERFACE

3.4.2 Baud Acquisition Interface. The BERT provides the following test signals for the Baud Acquisition Chassis.

3.4.2.1 Detected Baud Transitions. The BERT provides a pulse of 2 nS, in phase with the 80 MHz clock, whenever a symbol differs from the previous one.

This positive going pulse is an ECL signal at a maximum rate of 80 MHz. It shall be DC coupled as shown in Figure 9.

3.4.2.2 Start-of-Frame (SOF). The Start-of-Frame signal is asserted for the duration of Burst 1 and marks the beginning of each new Frame.

This positive going pulse is an ECL signal, it is single-ended and shall be DC coupled as shown in Figure 12.

3.4.2.3 Burst Symbol Words. These words contain three bits: S2 (MSB), S1 and S0 (LSB). Each bit represents a binary "1", when the output level is -1.0V ± 0.1V; and a binary "0" when the output level is -1.7V ± 0.1V.

These signals are ECL driven, single-ended and shall be DC coupled as shown in Figure 12.

The BERT receives the following test signals from the Baud Acquisition Chassis:

3.4.2.4 Serial Data In. The BERT accepts the valid data words in gray code and in serial format,

at a rate of 240 MBPS ±2%, most significant bit first. This data signal is ECL driven and shall be DC coupled as shown in Figure 13.

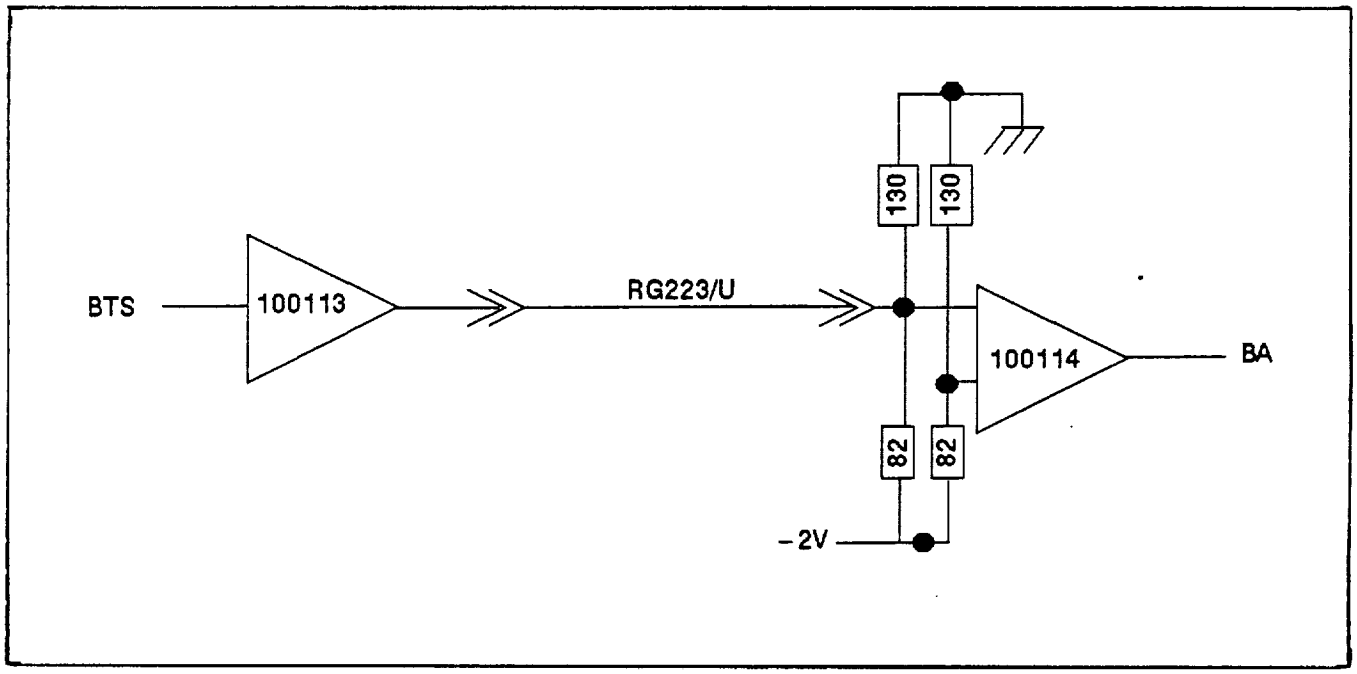


FIGURE 12

SINGLE-ENDED INTERFACE

3.4.2.5 Serial Clock In. The BERT accepts the associated serial clock at a rate of 240 MHz ±2%.

This Clock signal is ECL driven and shall be DC coupled as shown in Figure 13.

The phase difference between data and clock is less than 0.55 nanoseconds, (see Figure 14). This is measured at the rear panel.

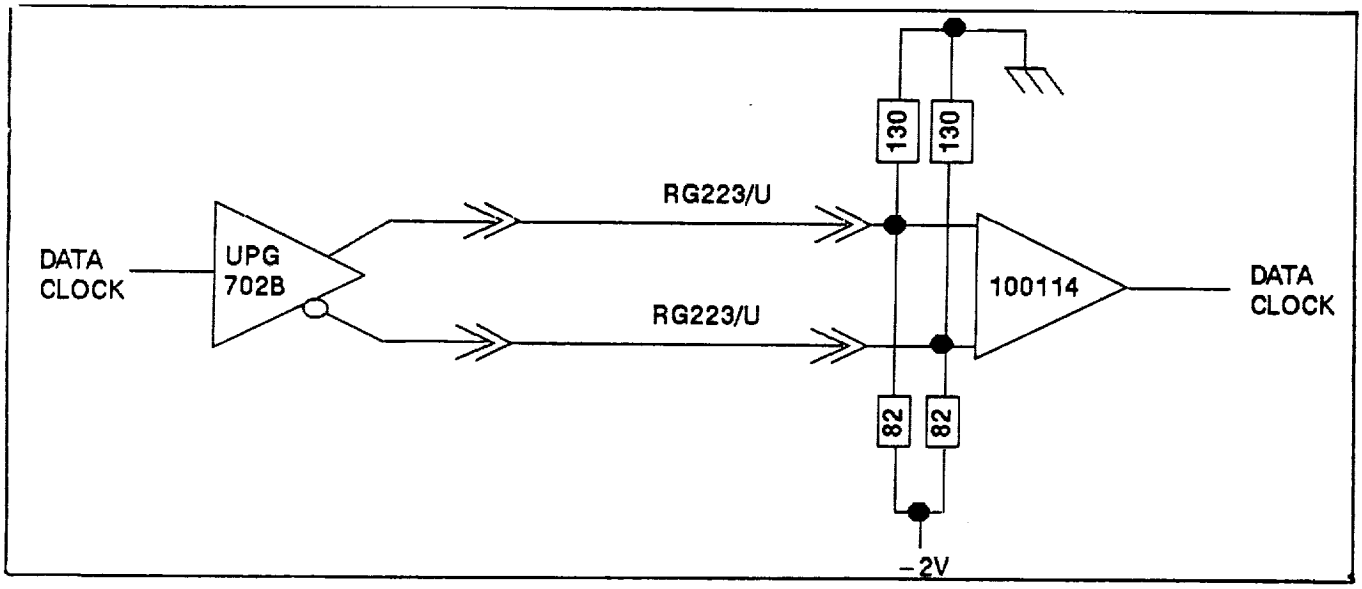


FIGURE 13

SERIAL INPUT INTERFACE

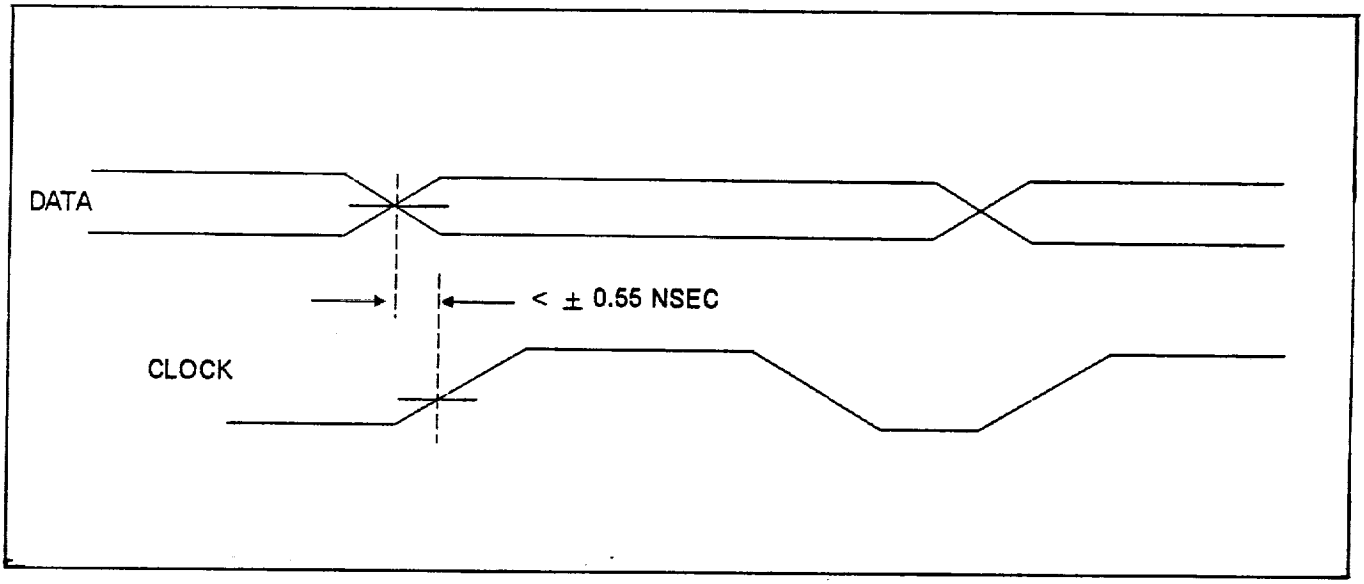


FIGURE 14

DATA / CLOCK TIMING DIAGRAM

3.4.3 Modulator Interface. The modulator accepts external symbols, symbol clock, and carrier enable (transmit) control signal with the following characteristics:

3.4.3.1 External Symbol. The external symbols shall contain three bits: S2 (MSB), S1 and S0 (LSB). Each bit represents a binary "1" when the input level is -1.0V ± 0.1V; and a binary "0" when the output level is -1.7V ± 0.1V.

The baud center of each symbol will be aligned to within ± 1 nS of the rising edge of the symbol clock.

These bit signals shall be ECL driven, they are single-ended and shall be DC coupled as shown in Figure 12.

3.4.3.2 External Modulator Clock. The modulator requires the symbol data clock along with the symbol data. The clock may have a duty cycle between 25-50% and is a single-end input. The input shall be ECL driven and DC coupled as shown in figure 12.

3.4.3.3 Transmit (IN). The Transmit signal will be used to enable the carrier with each burst of data. The Transmit signal must be aligned so that it is asserted within 1 nS of the first valid symbol. Transmit is a negative asserted signal.

3.4.4 Reference Test Interface. The BERT provides reference test data and test clock for loop tests on the serial data and serial clock inputs.

3.4.4.1 Serial Data Out. The BERT provides the three bits of the valid data words in gray code and in serial format, at a rate of 240 MBPS ±2%, most significant bit first.

3.4.4.2 Serial Clock Out. The BERT provides the associated serial clock at a rate of 240 MHz ±2%.

This Clock signal is ECL driven and shall be DC coupled as shown in Figure 13.

The phase difference between data and clock is less than 0.55 nS. (see Figure 14), measured at the rear panel.

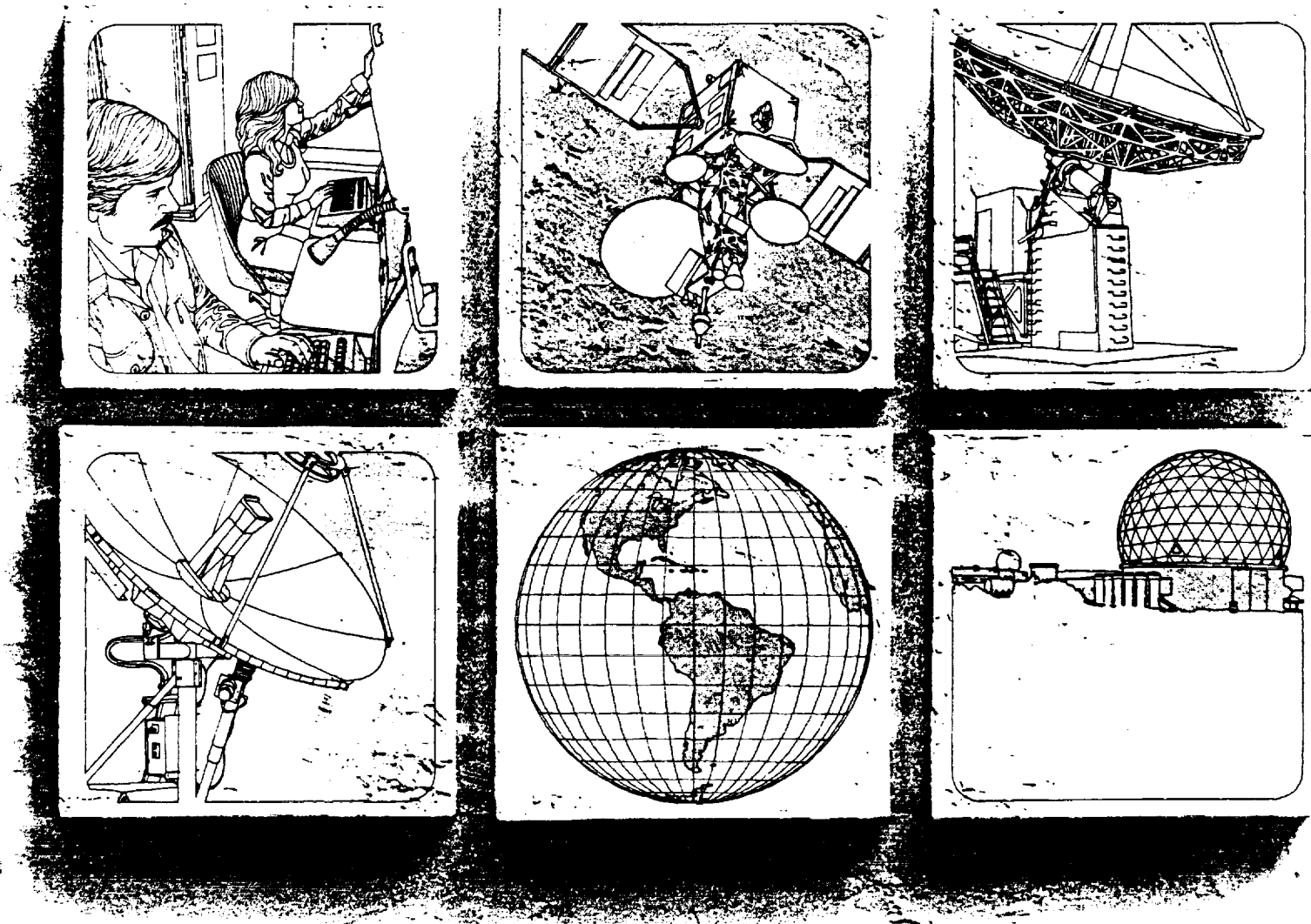
3.4.5 AC Power. The BERT operates on 120 volts AC ±10% and 60 Hz ±5%. The maximum current is 3 amps.

AMTD

SPECIAL TEST EQUIPMENT

SYSTEM DOCUMENTATION

QUADRATURE DETECTOR
OPERATIONS MANUAL



Ford Aerospace/Space Systems Division

AMTD

SPECIAL TEST EQUIPMENT

SYSTEM DOCUMENTATION

QUADRATURE DETECTOR
OPERATIONS MANUAL

MAY 24, 1989

OPERATIONS MANUAL

QUADRATURE DETECTOR

(AMTD)

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1.0 GENERAL DESCRIPTION

The Quadrature Detector performs several vital functions:

1. Amplification of the incoming modulated signal.

2. Resolution of the modulated signal into In-phase(I) and Quadrature-phase(Q) components.

3. Down conversion of the I and Q components to baseband using a suitable local oscillator.

4. Amplification and DC offsetting of the baseband I and Q signals to allow A/D conversion.

5. Recovery of the symbol clock from the modulated signal.

These tasks are accomplished using the circuit shown in Figure 1. The main incoming signal is amplified by 26 dB, followed by a variable attenuator. Power used for the DBT and the noise calibration is split off using a 10 dB coupler. The coupled signal is amplified and is used for the DBT. Another 10 dB coupler provides the calibration output. The main signal is split into I and Q components by a 3 dB 90 degree hybrid. The isolated hybrid port is terminated and the I and Q ports are connected to the RF sides of a pair of double balanced mixers. The mixer LO ports are connected to the local oscillator via a 3 dB power divider. A line stretcher is provided in one of the LO paths to adjust to varying path lengths in the mixers or the hybrid. An RF switch allows the selection of a external(coherent) LO or the internal LO. The LO ports of the mixers are then amplified using the wide bandwidth video amplifiers. The second video amplifier also adds a DC offset to the signal as required by the A/D converter in the digital demodulator.

The energy coupled to the symbol clock recovery circuit is used to drive a diode detector. If Nyquist filtering is used, it can be shown that amplitude peaks in the modulated signal will appear at the center of the eye opening. The diode detector output feeds a comparator which then produces an ECL level recovered symbol clock.

2.0 FRONT PANEL

The front panel, shown in Figure 2, consists of four functional groups: AC power, DBT, Gain, and Demod.

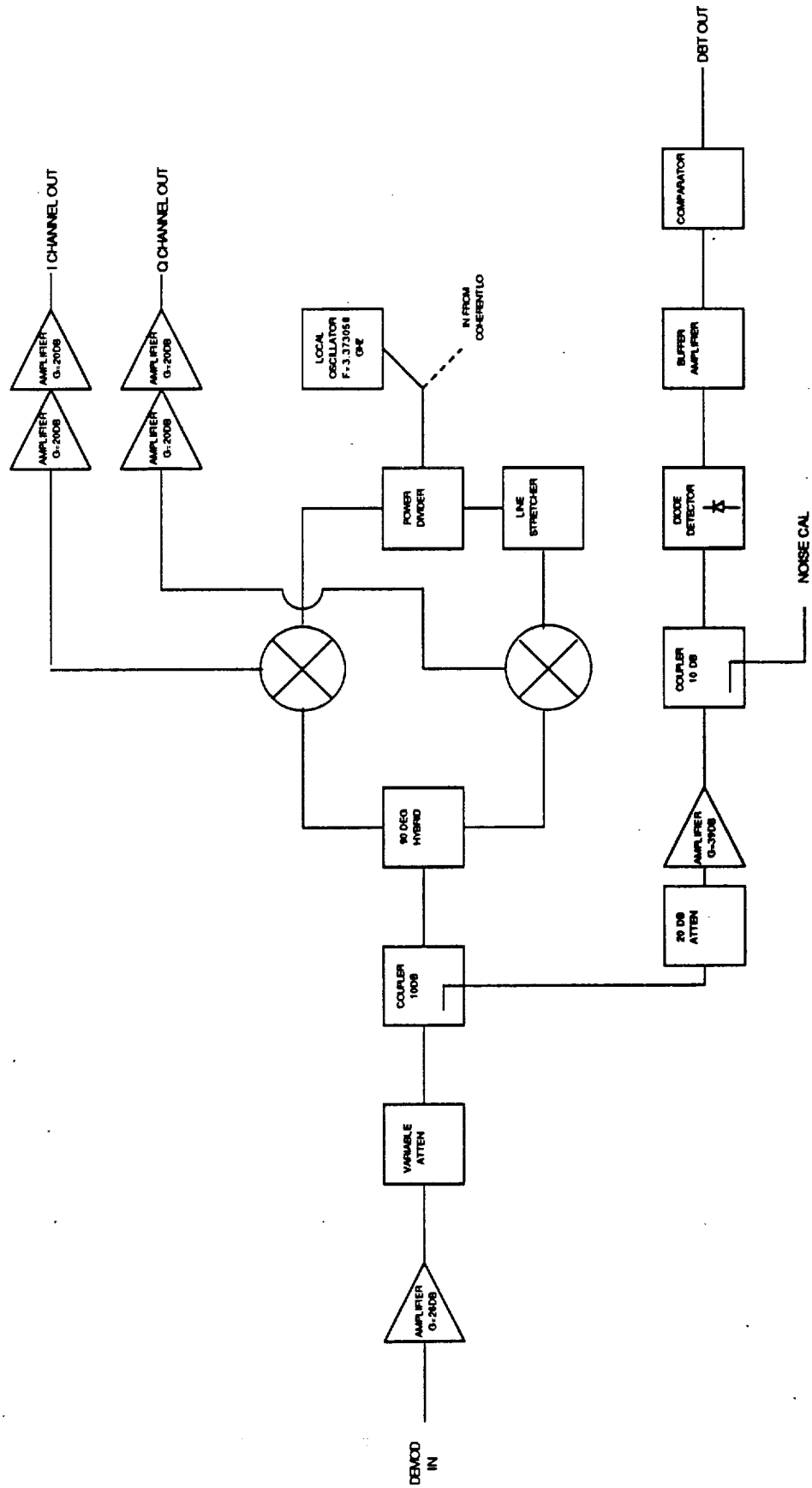


Figure 1 Quadrature Detector Block Diagram

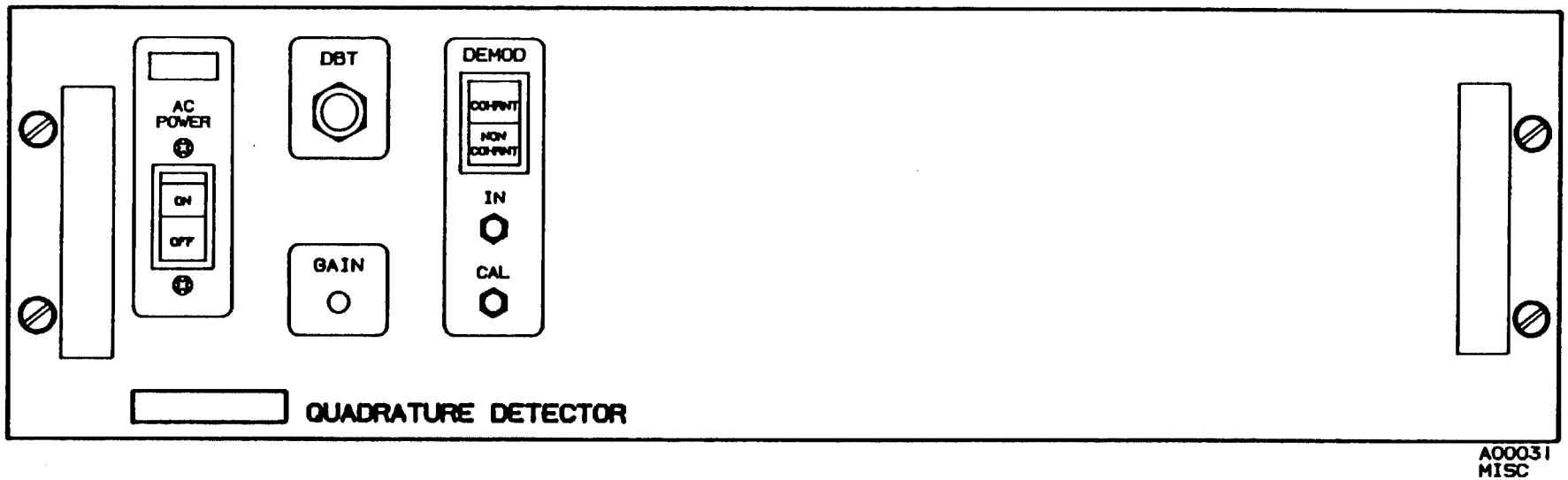


Figure 2 Quadrature Detector Front Panel

2.1 AC POWER

The AC power group consists of the circuit breaker and the "power on" LED indicator.

2.2 DBT

The detected baud transition BNC female connector provides a test port to view the recovered symbol clock. This output is at ECL levels.

2.3 GAIN

The gain section provides a screwdriver adjust for the quadrature detector gain. This adjustment affects all outputs.

2.4 DEMOD

2.4.1 Coherent/Non-coherent Switch

This switch allows the selection of the internal 3.373056 GHZ local oscillator(non-coherent) or an external oscillator(coherent if same as modulator LO). It is recommended that the coherent LO be between 2 to 4 GHZ at >+7 dBm for best operation.

2.4.2 Input Connector

The IN SMA female connector receives the main modulated signal.

3.0 REAR PANEL

Figure 3 shows the Quadrature Detector rear panel.

3.1 INPUTS

3.1.1 AC Power

The AC power connector uses 120V.,60 hz AC power.

3.1.2 Coherent LO

This SMA female connector allows connection of an external local oscillator(usually the same as the modulator).

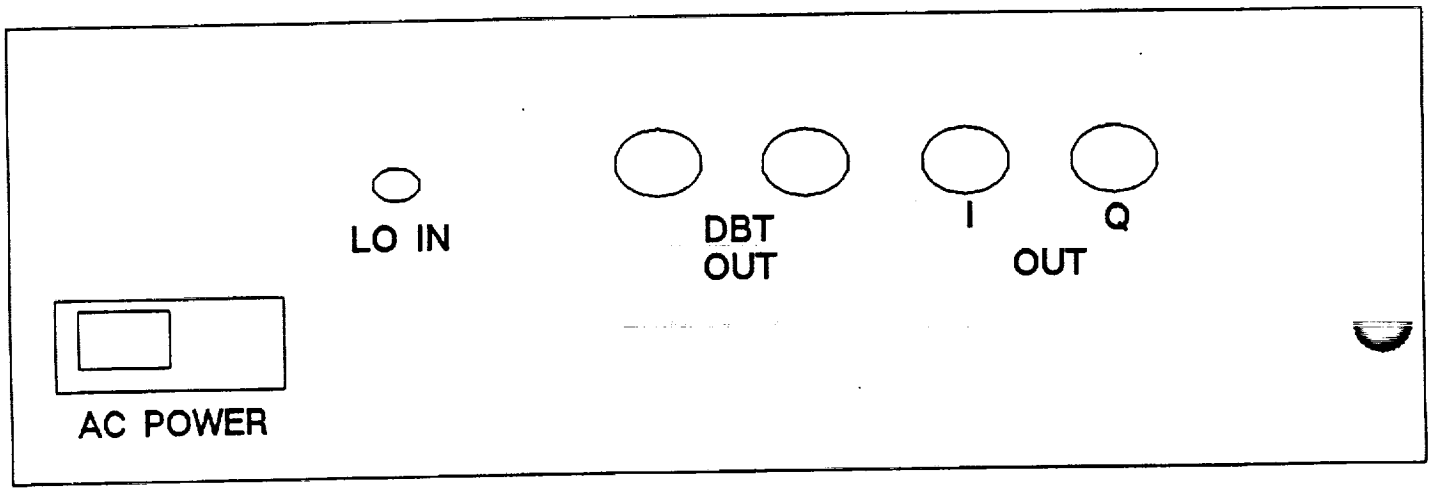


Figure 3 Quadrature Detector Rear Panel

3.2 OUTPUTS

3.2.1 I AND Q CHANNELS

The I and Q Channel TNC female outputs provide the necessary signal needed for A/D conversion by the demodulator. Nominal levels are -2 to 0 V p-p.

3.2.2 DBT OUTPUT

These TNC female connectors provide symbol clock recovery to the digital demodulator at ECL levels.

4.0 OPERATION

4.1 CALIBRATION

4.1.1 I and Q Gain

To adjust I and Q gain, first adjust the RF input power to the quadrature detector by measuring with a power meter at the calibration port. This can be done by adding attenuators or adjusting those contained in the Interference/Noise Generator or the Modulator. The power detected should be -20 dBm. This level will provide the proper drive for the A/D converters in the demod. If an external oscillator is being used(other than the transmitting oscillator), its level may need adjustment for best performance.

4.1.2 I and Q Offset

To adjust I and Q offset, disconnect the modulated signal and measure the quiescent I and Q voltages. They should be -1V +/-.005V. Adjust this value by removing the cover of the quadrature detector and adjusting the video amplifier DC offset potentiometers. These are adjusted with a screwdriver through holes in the amplifier covers. It may be necessary to adjust these levels while viewing the bit error rate to achieve optimum performance.

4.1.3. Noise Calibration

To determine Signal to Noise Ratio for a given signal, connect the power meter to the calibration port. Set the noise level to a minimum on the Interference and Noise test set and measure the RF power detected. Note the value, and then turn off the RF power to the Modulator. The power now read is the total noise power. Subtract the noise power from the signal power to get the S/N ratio. The power meter db[ref] function may be used for

convenience. Use the noise attenuator(s) on the Interference and Noise test set to adjust the noise to the desired level.

4.1.4 Miscellaneous Adjustments

4.1.4.1 I and Q Phase Quadrature

In the unlikely event that an adjustment of I and Q phase quadrature is required, first connect the I and Q channels to an oscilloscope with an unmodulated carrier input. Use the internal local oscillator(non-coherent) and trigger on the I channel. The I and Q channels should be simple sine waves. Viewing I and Q simultaneously, they should appear to be 90 degrees out of phase. To adjust this, remove the cover of the Quadrature Detector and locate the phase trimmer connected to one of the mixers. Loosen the trimmer locknut and adjust its length until the I and Q channels are in quadrature. Lock the trimmer position.

4.1.4.2 Local Oscillator Frequency Adjustment

If the local oscillator drifts too far from the Modulator oscillator frequency, first connect either the I or Q channel to an oscilloscope. Verify that the beat frequency is out of the required range. Be sure that the local oscillator has had sufficient time to warm up and the beat frequency is stable. Adjust the LO frequency by removing the Quadrature Detector cover and located the local oscillator. On the back of the LO, facing away from the front panel, is a screw into the LO housing. Remove the screw, taking care to avoid any shock hazard. Adjust the frequency with a screwdriver by rotating the potentiometer located in the hole. The oscillator will jump each time the pot is touched, so let the oscillator settle to get accurate readings after each adjustment.

Quadrature Detector Data Sheet

Operator_____
Date_____

Para	Title	Measured Value	Ideal Value
4.1.1	I & Q Level	I_____Q_____	2 V p-p
4.1.2	I & Q Offset	I_____Q_____	-1 V
4.1.3	Noise Calibration Carrier Level	_____	-20 dBm
4.1.4.1	Phase Quadrature	_____	90° +_ 1°
4.1.4.2	Local Oscillator	_____	+_1.5 kHz

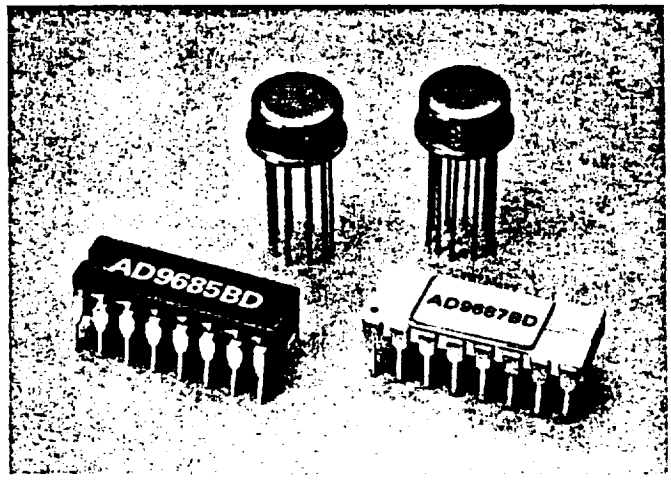
APPENDIX A
DBT TECHNICAL DATA

ANALOG DEVICES

Ultra-Fast Comparators

FEATURES
2.2ns Propagation Delay – AD9685BD/BH
2.7ns Propagation Delay – AD9687BD
0.5ns Latch Set-Up Time
Pin-Compatible to Am685/687 but FASTER
+5V, −5.2V Supply Voltages

APPLICATIONS
Ultra-High-Speed A/D Converters
Ultra-High-Speed Line Receivers
Peak Detectors
Threshold Detectors



GENERAL DESCRIPTION

The AD9685BD/BH and AD9687BD are ultra-fast comparators manufactured with a high performance bipolar process which makes it possible to obtain incredibly short propagation delays and latch set-up times.

The AD9685BD/BH is a single comparator which is pin-compatible with the Am685, but has speed capabilities that far outstrip the earlier unit. The AD9687BD is pin-for-pin compatible with the Am687 and, like its predecessor, is a dual comparator; its speed capabilities are far superior to the Am687.

Both Analog Devices units have differential inputs and complementary outputs fully compatible with ECL logic levels. Their output current levels are capable of driving 50Ω terminated transmission lines, and their high resolution make them ideally suited for a variety of analog-to-digital signal processing applications.

AD9685BD/BH Single Comparator

A latch function allows the AD9685BD/BH to be operated in a sample-hold mode. When the Latch Enable (LE) is ECL HIGH, the comparator functions normally. When the Latch Enable is driven LOW, its outputs are locked in the logic state dictated by the input conditions at the time of the latch input transition. If the latch function is not used, the Latch Enable input should be connected to ground.

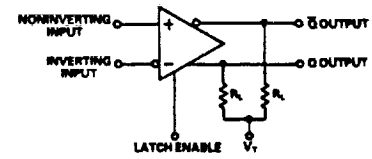
In addition to its speed advantages over the earlier Am685, the AD9685BD/BH also dissipates less power because it operates on a positive 5 volt supply instead of the 6 volts required by the AMD device.

AD9687BD Dual Comparator

The latch function of the AD9687BD provides an ability to operate the unit in either a track-hold or sample-hold mode. The latch function inputs are separated on the two comparators and are designed to be driven from the complementary outputs of a standard ECL logic gate. When LE is High and $\overline{LE}$ is LOW, the normal comparator function is in operation. When LE is forced LOW and $\overline{LE}$ is driven HIGH, the outputs of the comparator being exercised are locked in their existing logical states, as determined by the input conditions present at the time of arrival of the latch signal. If the latch function is not used on either one of the two comparators in the AD9687BD, the appropriate Latch Enable input should be connected to ground; the companion $\overline{Latch\ Enable}$ input can be left open.

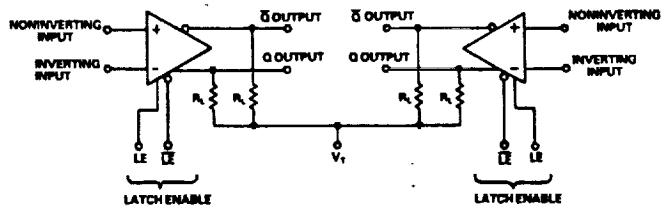
The AD9687BD is basically two AD9685BD/BH units in a single package and operates in a similar fashion to a pair of the single comparators.

AD9685BD/BH FUNCTIONAL BLOCK DIAGRAM



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω–200Ω CONNECTED TO −2.0V; OR 200Ω–2000Ω CONNECTED TO −5.2V.

AD9687BD FUNCTIONAL BLOCK DIAGRAM



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P.O. Box 280; Norwood, Massachusetts 02062 U.S.A.
Tel:617/329-4700 Twx: 710/394-6577
Telex: 924491 Cables: ANALOG NORWOODMASS

SPECIFICATIONS (typical @ +25°C with nominal supply voltages unless otherwise noted)

ABSOLUTE MAXIMUM RATINGS	AD9685BD/BH	AD9687BD
Supply Voltages (V_{CC} and V_{EE})	±6V	*
Power Dissipation	336mW	500mW
Input Voltage	±5V	*
Differential Input Voltage	3.5V	*
Output Current	30mA	*
Operating Temperature Range	−30°C to +85°C	*
Storage Temperature Range	−55°C to +150°C	*
Lead Temperature (soldering, 10 seconds)	300°C	*

ELECTRICAL CHARACTERISTICS	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage[1]	V_{OS}	−5		+5	*		*	mV
Temperature Coefficient	$\Delta V_{OS}/\Delta T$		20			*		µV/°C
Input Offset Current	I_{OS}			5			*	µA
Input Bias Current	I_B		10	20		*	*	µA
Input Voltage Range	V_{CM}	−2.5		+2.5	*		*	V
Common Mode Rejection Ratio	CMRR	80			*			dB
Input Resistance	R_{IN}	60			*			kΩ
Input Capacitance	C_{IN}		3			*		pF
Input/Output Logic Levels								
Output HIGH Voltage	V_{OH}	−0.96		−0.81	*		*	V
Output LOW Voltage	V_{OL}	−1.85		−1.65	*		*	V
Positive Supply Voltage	V_{CC}	+4.75	+5	+5.25	*	*	*	V
Negative Supply Voltage	V_{EE}	−4.95	−5.2	−5.45	*	*	*	V
Positive Supply Current	I_{CC}		19	23		30		mA
Negative Supply Current	I_{EE}		23	34		54		mA
Supply Voltage Rejection Ratio	S_{VRR}		60			*		dB
Power Dissipation	P_{DISS}		210	300		430		mW
SWITCHING CHARACTERISTICS								
Propagation Delays[2]								
Input to Output HIGH	$t_{pd}+$		2.2	3		2.7	4	ns
Input to Output LOW	$t_{pd}-$		2.2	3		2.7	4	ns
Latch Enable to Output HIGH	$t_{pd}+(E)$		2.5	3		2.7	4	ns
Latch Enable to Output LOW	$t_{pd}-(E)$		2.5	3		2.7	4	ns
Latch Enable								
Pulse Width	$t_{pw}(E)$	3	2		*	*		ns
Minimum Set-Up Time	t_s		0.5	1		*	*	ns
Minimum Hold Time	t_h			1			*	ns

NOTES
[1] R_s = 100 ohms
[2] Propagation delays measured with 100mV pulse; 5mV overdrive.
* Specifications same as AD9685BD/BH.
Specifications subject to change without notice.

DEFINITION OF TERMS

V_{OS} INPUT OFFSET VOLTAGE – The potential difference required between the input terminals to obtain zero potential difference between the outputs.

I_{OS} INPUT OFFSET CURRENT – The difference between the currents into the inputs when there is zero potential difference between the outputs.

I_B INPUT BIAS CURRENT – The average of the two input currents. This is a chip design trade-off parameter. Internally, it is desirable to have high values of I_B for circuit performance requirements; externally, it is desirable to have I_B as low as possible.

V_{CM} INPUT VOLTAGE RANGE – The range of input voltages for which offset and propagation delay specifications are valid.

CMRR COMMON MODE REJECTION RATIO – The ratio of input voltage range to the peak-to-peak change in input offset voltage over that range.

R_{IN} INPUT RESISTANCE – The resistance looking into either terminal with the other grounded.

C_{IN} INPUT CAPACITANCE – The capacitance looking into either input pin with the other grounded.

V_{OH} OUTPUT HIGH VOLTAGE – The logic HIGH output voltage with an external pull-down resistor returned to a negative supply.

V_{OL} OUTPUT LOW VOLTAGE – The logic LOW output voltage with an external pull-down resistor returned to a negative supply.

I_{CC} POSITIVE SUPPLY CURRENT – The current required from the positive supply to operate the comparator.

I_{EE} NEGATIVE SUPPLY CURRENT – The current required from the negative supply to operate the comparator.

S_{VRR} SUPPLY VOLTAGE REJECTION RATIO – The ratio of the change in input offset voltage to the change in power supply voltage producing it.

P_{DISS} POWER DISSIPATION – The power dissipated by the comparator with both outputs terminated in 50 ohms to −2V.

$t_{pd}+$ INPUT TO OUTPUT HIGH DELAY – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

$t_{pd}-$ INPUT TO OUTPUT LOW DELAY – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{pd}+(E)$ LATCH ENABLE TO OUTPUT HIGH DELAY – The propagation delay measured from the 50% point of the Latch Enable (LE) signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{pd}-(E)$ LATCH ENABLE TO OUTPUT LOW DELAY – The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

$t_{pw}(E)$ MINIMUM LATCH ENABLE PULSE WIDTH – The minimum time the Latch Enable signal must be HIGH to acquire and hold an input signal.

t_s MINIMUM SET-UP TIME – The minimum time before the negative transition of the Latch Enable pulse that an input signal must be present to be acquired and held at the outputs.

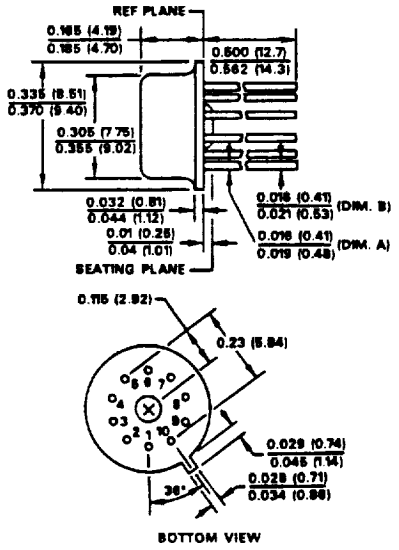
t_h MINIMUM HOLD TIME – The minimum time after the negative transition of the Latch Enable signal that an input signal must remain unchanged to be acquired and held at the outputs.

OTHER SYMBOLS

T_C	Case Temperature	V_T	Output load terminating voltage
R_S	Input source resistance	R_L	Output load resistance
V_S	Supply voltages	V_{IN}	Input pulse amplitude
V_{CC}	Positive supply voltage	V_{OD}	Input overdrive
V_{EE}	Negative supply voltage	f	Frequency

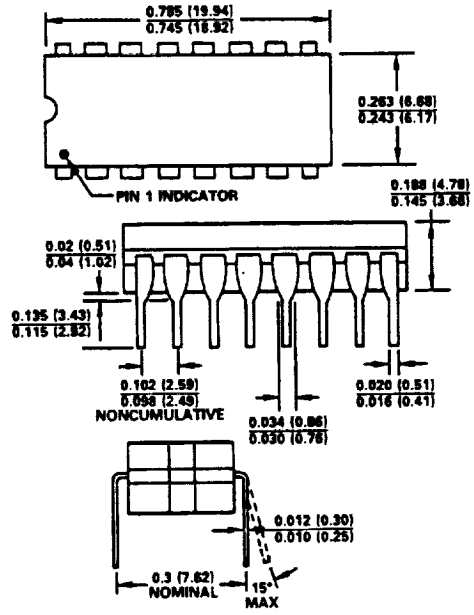
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



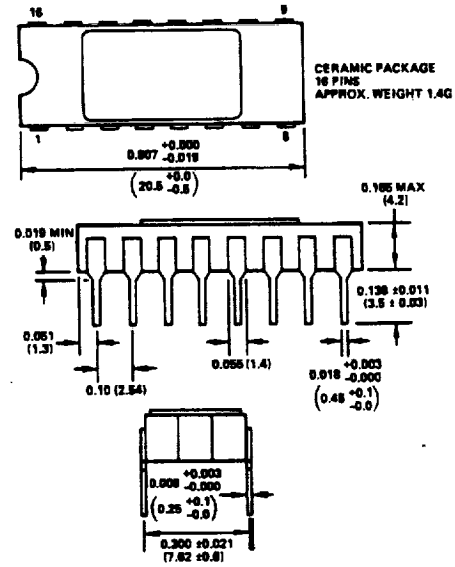
AD9685BH

TO-100



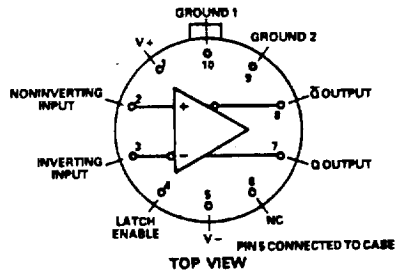
AD9685BD

DIP

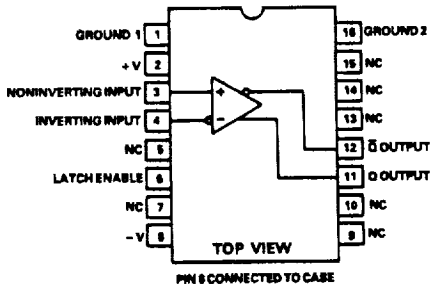


AD9687BD

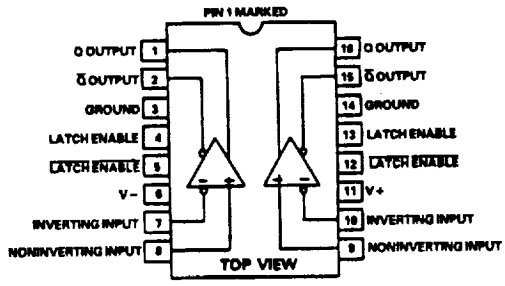
DIP



AD9685BH Pin Configuration



AD9685BD Pin Configuration

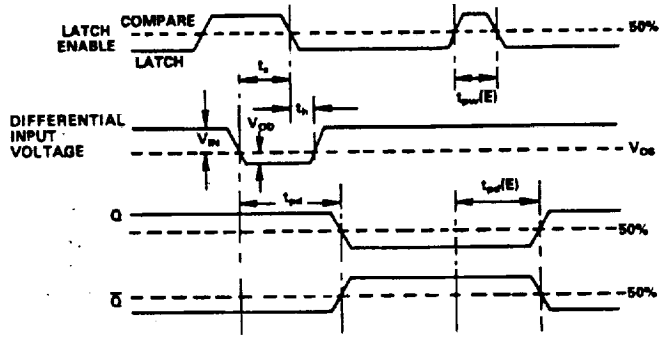


AD9687BD Pin Configuration

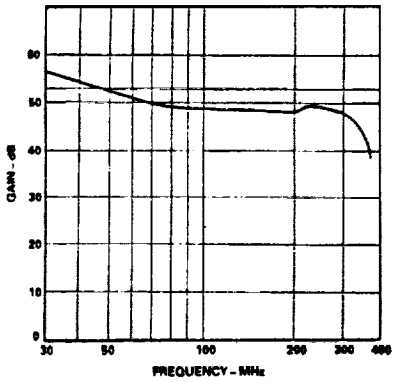
TIMING DIAGRAM

The Timing Diagram illustrates a series of events in the AD9685BD/BH; the terms and their relationships are also valid for the AD9687BD. The relationships which are shown should not be interpreted as "typical", since several parameters have multiple values; and the worst case conditions are shown in the Timing Diagram.

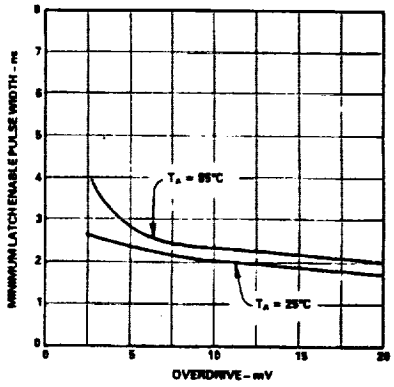
The top line of the diagram shows two Latch Enable (LE) pulses; each is high for "compare" and low for "latch". The first pulse illustrates the compare function in which part of the input action takes place during the "compare" mode. The second one illustrates a compare function interval during which there is no change in input.



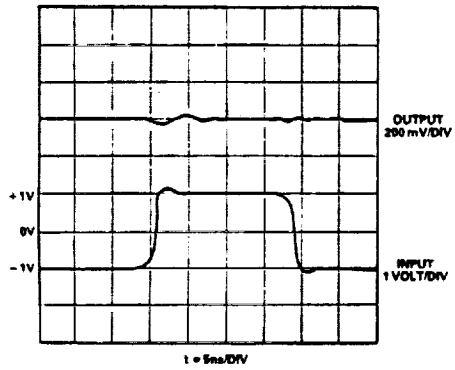
The leading edge of the input signal, shown here as a large amplitude, small overdrive pulse, switches the comparator after a time interval t_{pd}. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch trailing (falling) edge and, to be acquired, must be maintained for a time t_h after that edge. After t_h, the output is no longer affected by the input status until the latch is again strobed. A minimum latch pulse width of tpw(E) is required for the strobe operation, and the output transitions occur after a time $t_{pd}(E)$.



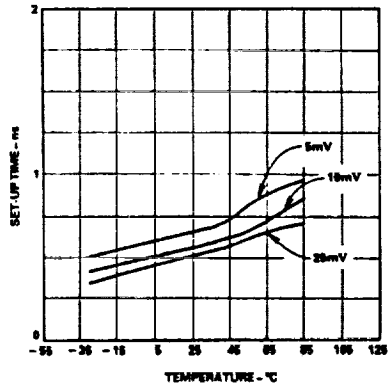
Open Loop Gain vs. Frequency (Unlatched Mode)



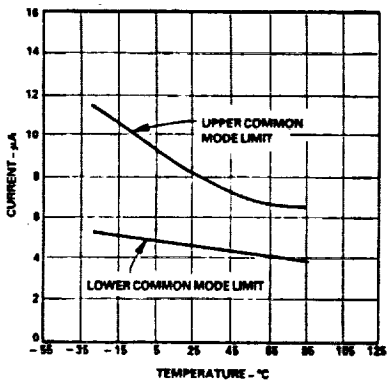
Latch Enable Width vs. Overdrive



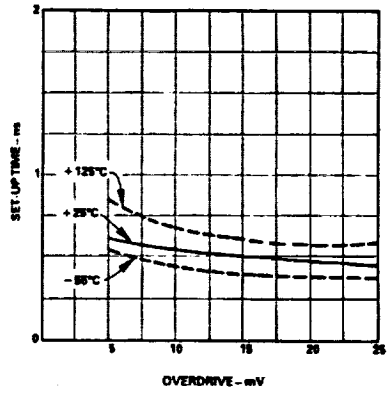
Common Mode Pulse Response



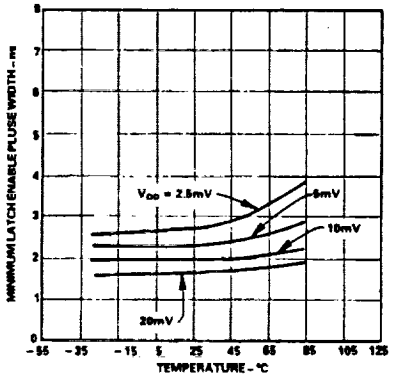
Set-Up Time vs. Temperature



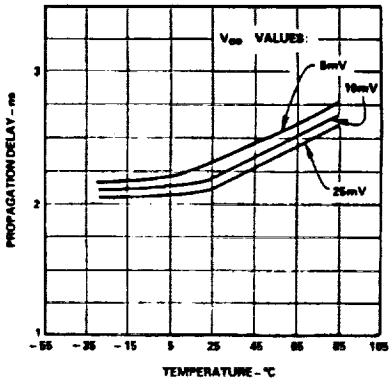
Input Bias Currents vs. Temperature



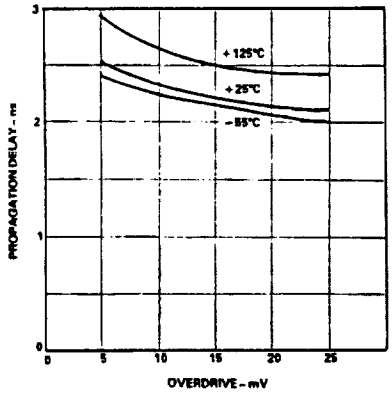
Set-Up Time vs. Input Overdrive



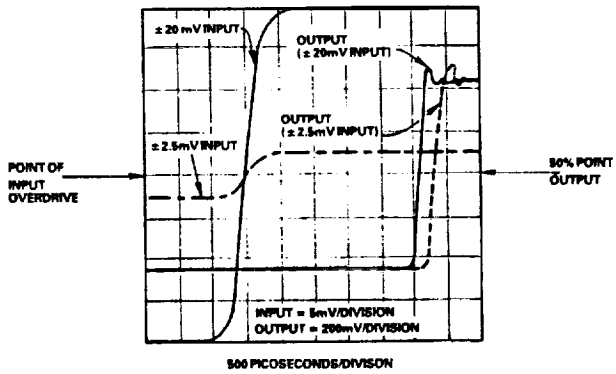
Latch Enable Width vs. Temperature



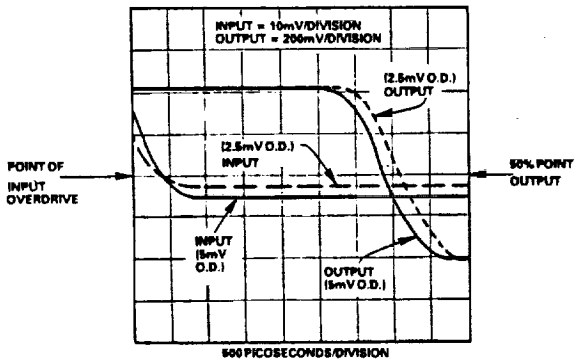
Latch Propagation Delay vs. Temperature



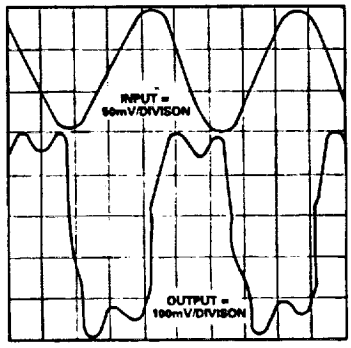
Latch Propagation Delay vs. Overdrive



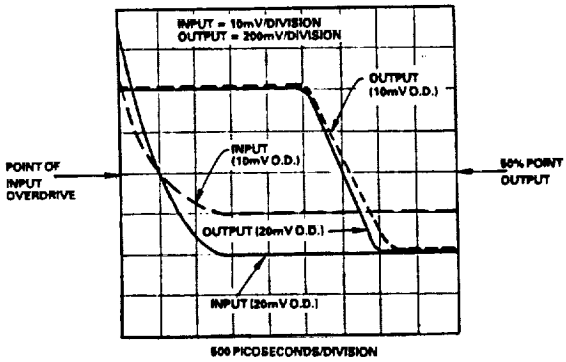
Response vs. Input Levels



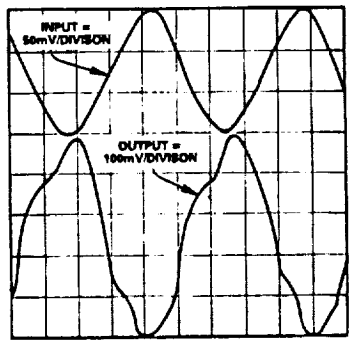
Propagation Delay vs. Overdrive (t_{pd}—)



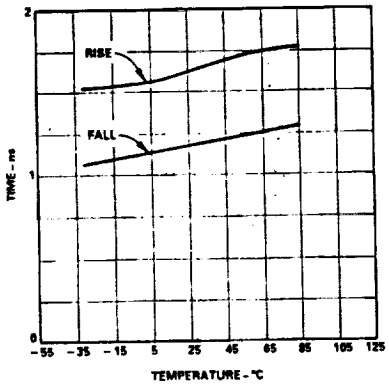
Response to 100MHz Sine Wave



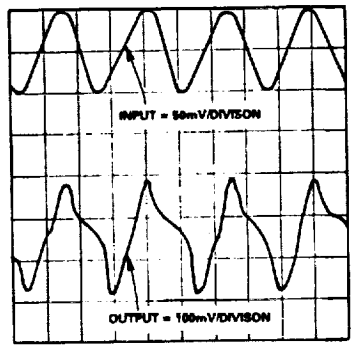
Propagation Delay vs. Overdrive (t_{pd}—)



Response to 200MHz Sine Wave



Output Rise and Fall vs. Temperature



Response to 400MHz Sine Wave

THEORY OF OPERATION

The "dictionary definition" states a comparator is "a circuit for performing amplitude selection either between two variables or between a variable and a constant."

A voltage comparator, then, is a device which selects amplitudes between two voltages.

The Analog Devices' AD9685 and AD9687 are sampling comparators, which is not radically different from a voltage comparator when one visualizes the sampling comparator as being simply an extension of a voltage comparator. That extension (difference) means the outputs can be latched into logic states established by whatever input signal conditions are present at the instant the latch signal is applied. If the latch function is not used, the LATCH ENABLE input is connected to ground and the units operate as conventional voltage comparators.

It is important to recognize comparators of this type do not use a strobe signal but use, instead, a latch signal. As defined in these types of devices, a strobe forces the output of the comparator to some fixed state, regardless of the input signal conditions. A latch, on the other hand, can cause either a high or low output state, depending on the comparator input conditions at the time the latch is enabled.

This characteristic means a latch allows the comparator to perform a sample-and-hold function; it makes the latch infinitely more useful than a strobe for high-speed processing. With the use of the latch, input signals of extremely short duration can be detected and held for additional processing.

In the Analog Devices units, the latch operates directly on the input stage. This means the signal is not subjected to additional delays through the comparator, making it possible to acquire and hold signals which are present for only a few nanoseconds.

Of necessity, the minimum width of the latch enable pulse is less than the propagation delay through the comparator. As a consequence, the unit can be unlatched for a fraction of its propagation delay, and the outputs will change to reflect the input conditions which were present at the time of the (un)latch signal. This, then, is the sample-and-hold function alluded to earlier.

The role intended for comparators requires that they have a set of characteristics which are mutually exclusive but, as much as possible, need to be achieved in concert. Specifically, they should have:

1. Wide small-signal bandwidth
2. High gain
3. Minimum voltage swings
4. High slew rates for large signals

As in any design situation, the comparator designer makes the necessary "trade-offs" to obtain the optimum combination of these contradictory requirements.

The AD9685 and AD9687 are exceptional examples of successful implementation of this philosophy and offer designers remarkable devices for a multiplicity of circuit applications.

TESTING COMPARATORS

The input signal which stresses the performance of a comparator to its maximum is a large-amplitude pulse that exceeds the input threshold by a miniscule amount. This type of pulse forces the input stage to swing from a state of either fully "on" or fully "off", to a point near the center of its linear range. Accomplishing this in minimum time is also an integral part of the requirement. Unless the comparator has a good blend of the characteristics enumerated above, it will find this kind of exercise too demanding.

Not surprisingly, one of the standards of performance calls for a propagation delay measurement which uses a pulse of 100mV amplitude, with an overdrive component 5mV or 10mV above the input threshold. If larger pulses were used, there is an inherent possibility the generator supplying the pulse would introduce ripple on the top of the waveform. Even small percentages of ripple on the input could affect the amplitude (and therefore, the accuracy) of the overdrive signal. The result? An error in propagation delay measurement.

The set-up (t_s) and hold (t_h) times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuits. Input signal changes occuring before t_s will be detected and held; those occuring after t_h will not be detected. Changes between t_s and t_h may or may not be detected (see Timing Diagram).

The measurement of gain of a comparator is another difficult task. Input noise and the possibility of oscillations when the device is operating in its linear region compound the problem of assessing its performance. For a full ECL output level swing, the required unlatched input swing is approximately 1mV. Input signals of smaller magnitude could cause the comparator to be operating in its linear region, with the attendant possibility of oscillations confounding the measurement.

In the latched mode, the useable resolution is markedly smaller–100μV–because the feedback action of the latch tends to enhance the gain and limit the difference in the noise/oscillation level. It is extremely important to recognize this 100μV resolution is possible only with careful circuit design and layout.

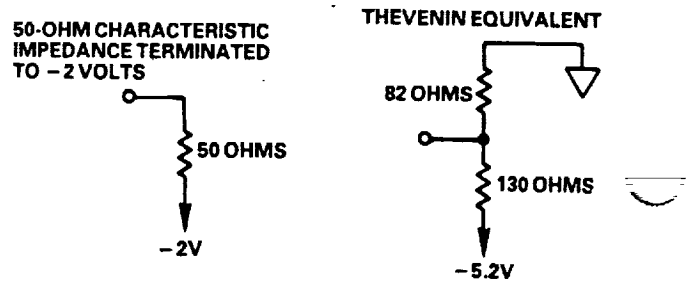
APPLICATIONS

It is an axiom of high-speed components that special precautions are needed in circuit board design if optimum system performance is going to be achieved. The Analog Devices' AD9685 and AD9687 comparators are subject to the same rules of conduct.

A large, low-inductance ground plane is mandatory for working successfully with these units. All lead lengths must be kept as short as possible; and decoupling capacitors should be mounted as close as possible to the power supply pins. Almost without exception, the comparators should be soldered into the circuit board, rather than using socket assemblies. If sockets must be used despite this caveat, individual pin sockets are overwhelmingly preferred.

There are also other factors to be considered if optimum performance is going to be assured. The input source resistance (R_S) needs to be matched as closely as possible between the differential inputs of the comparators; if it is not, hysteresis will detract from their performance. If several comparators are going to be operated in parallel, they should be driven from a low-impedance microstrip transmission line.

The output lines of the comparator should be designed as microstrip transmission lines backed by the massive ground plane; characteristic impedance should be between 50 and 150 ohms. Terminations to −2V, or their Thevenin equivalents, should be used.



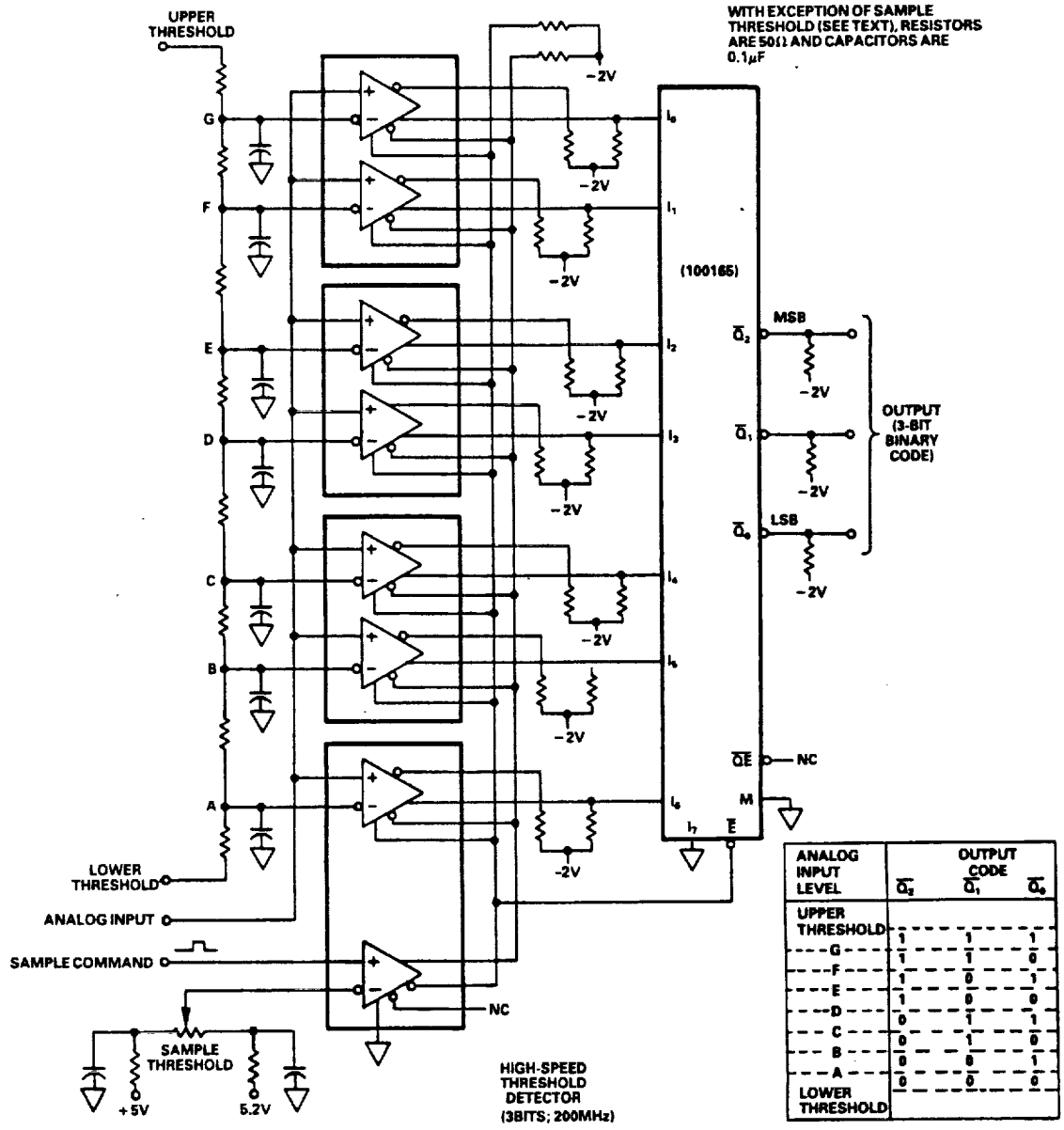


Figure 1.

The gain/bandwidth combination of these comparators can create instability problems when the device outputs are in the transition region. These, in turn, can induce oscillations if poor circuit layout is used and/or the source impedance of the circuit is high. Poor layout increases the feedback caused by parasitic capacitance; and even small amounts of parasitic coupling can cause oscillations if the source impedance is sufficiently high.

It is inevitable that a certain amount of power will be dissipated as heat when operating these comparators. This heat increases the temperature of the die in relation to the ambient temperature. ECL III and ECL 10,000 logic normally uses air flow as a means of package cooling; to be compatible, the characteristics of the AD9685 and AD9687 are specified with an air flow across the package of 500 linear feet per minute (LFPM) or greater.

This assures that even though different ECL circuits on a printed circuit board may have different power dissipations, all of them will have the same input levels, output levels, etc. as long as all of them are subjected to the same air flow and air temperature. This precaution eases design, since the only change in characteristics between devices is due to the increase in ambient temperature, combined with individual temperature coefficients of the devices themselves. If the AD9685 and AD9687 are operated without air flow, the change in electrical characteristics must be taken into account.

In summary, the user of the AD9685 and AD9687 high-speed comparators who expects to obtain maximum performance from these devices must carefully observe the tenets of designing with high-speed circuits. The AD9685BD/BH and AD9687BD are ultra-fast devices capable of outstanding performance in a variety of applications whose range is limited only by the imagination.

THRESHOLD DETECTION

The high-speed threshold detector shown in Figure 1 is essentially a high-speed 3-bit "flash" A/D converter. In most situations, however, three bits of resolution are not sufficiently accurate to be useful for analog-to-digital conversion, so the pictured circuit is more correctly a threshold detector.

This circuit provides a 3-bit binary code to indicate the instantaneous value of the analog signal applied to the circuit at the instant of the sample command.

The eight possible combinations of digital output codes indicate seven levels of threshold detection. Each logic output code indicates which level of threshold has been exceeded. As an example, an instantaneous value of analog input (at the time of the sample command) which is anywhere between voltage level F and voltage level G will result in a digital output code of 110. The various output codes and their associated detection levels are shown in the table which is part of the figure.

The comparators which are pictured are four AD9687BD dual comparators.

One (half of one dual) comparator operates as a single-ended line receiver and receives the Sample Command supplied by the user; it uses that positive-going pulse to generate Latch Enable commands for the remaining seven comparators. The complementary output of the first comparator is applied to the 100165 priority encoder to enable it.

When the Sample Command is "low", no sampling is taking place. The outputs of the (7) comparators are changing, but have no effect on the output of the circuit. This is true because the priority encoder is not enabled; comparator outputs applied as priority encoder inputs I_0 through I_6 will be unable to change the $\overline{Q_0}$, $\overline{Q_1}$, and $\overline{Q_2}$ signals.

When the Sample Command supplied by the user switches to "high", the outputs of the (7) comparators will be latched and held at the analog input value which is present at the time of the leading edge of the Sample Command. (The comparator used as a line receiver will use the Sample Command to generate Enable pulses for the other comparators.)

The complementary output of the line receiver comparator is applied to the $\overline{E}$ input of the 100165 priority encoder, enabling it. This allows the priority encoder to accept the latched comparator signals and modify the three-bit digital output code to reflect a new binary output code indicative of the instantaneous value of the analog input.

When the Sample Command changes from "high" back to "low", the entire process is reversed . . . the (7) comparators are unlatched, and begin following all changes in analog input; the priority encoder is inhibited, and its output can no longer be affected by signals I_0 through I_6. The three-bit binary code remains at whatever value was established by the just-completed sampling process and will remain at that value until the next low-to-high change of the Sample Command.

No value is shown for the potentiometer labeled Sample Threshold because its value will be determined by the user, based on the type of logic being used as a Sample Command. TTL, ECL, or any other negative-to-positive voltage change can be used as a signal whose leading edge will cause the sampling process to take place.

The setting of the Sample Threshold is selected to cause the 50% point of the Sample Command to operate the system.

It is impossible to overemphasize the criticality of circuit layout if 200MHz update rates are going to be obtained with this circuit configuration. On the component side of the printed circuit board, the only breaks in the overall ground plane should be those required for installing component leads. With these exceptions, the component side must be one solid ground plane.

Component placement is also extremely important to assure minimum lengths of circuit runs on the reverse side of the pc board. Within the restrictions imposed by good high-speed circuit design rules, the circuit should be laid out in the smallest possible area. The analog input signal path should be as large as possible to maintain the lowest possible impedance for the analog signal being sampled.

As indicated elsewhere in this data sheet, microstrip transmission line techniques, careful attention to circuit layout, and good high-speed design precautions are all required for operating high-performance comparators of this type in high-frequency applications such as the one illustrated here.

C743a–5–2/84

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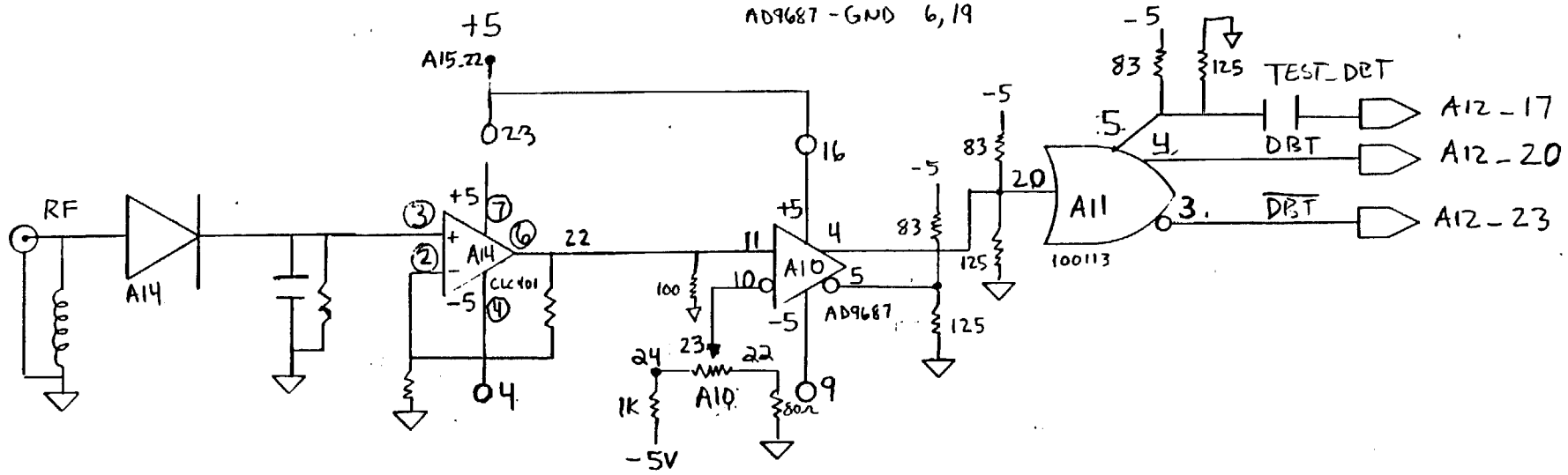


FUNCTION	AD9687 PIN	ECL PIN*
Q_1 OUT	1	4
$\overline{Q_1}$ OUT	2	5
GND	3	6
$LATCH_1$ EN	4	7
$\overline{LATCH_1}$ EN	5	8
V−	6	9
$\overline{INPUT_1}$	7	10
INPUT 1	8	11
INPUT 2	9	14
$\overline{INPUT_2}$	10	15
V+	11	16
$\overline{LATCH_2}$ EN	12	17
$LATCH_2$ EN	13 +	18
GND	14	19
$\overline{Q_2}$ OUT	15	20
Q_2 OUT	16	21

* BASED ON AD9687 PIN 1 PLACED IN SOCKET #4 OF AUGAT 624-HG29-4T ADAPTOR

+ PIN 13 of the AD9687 should be bent up so AS NOT TO be connected to −5 volts

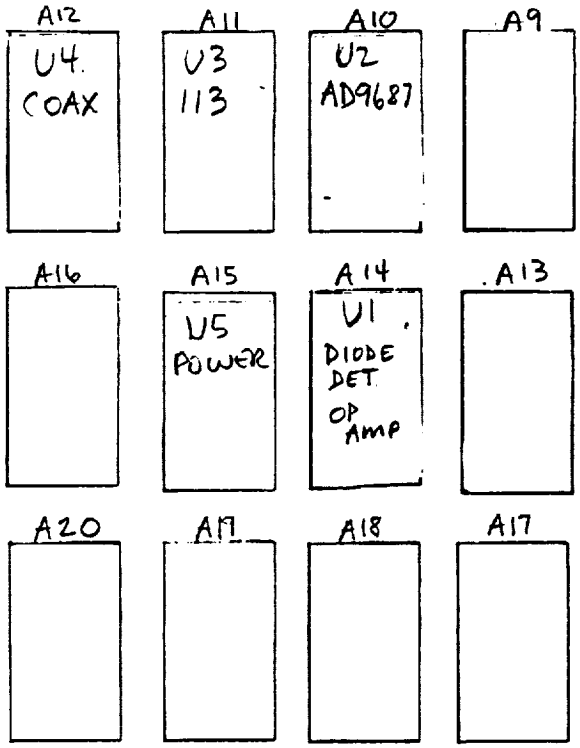
AMTD.
QUAD DETECTOR

DBT DECTECTOR
6-1-88 J. OTT

ORIGINAL PAGE IS
OF POOR QUALITY

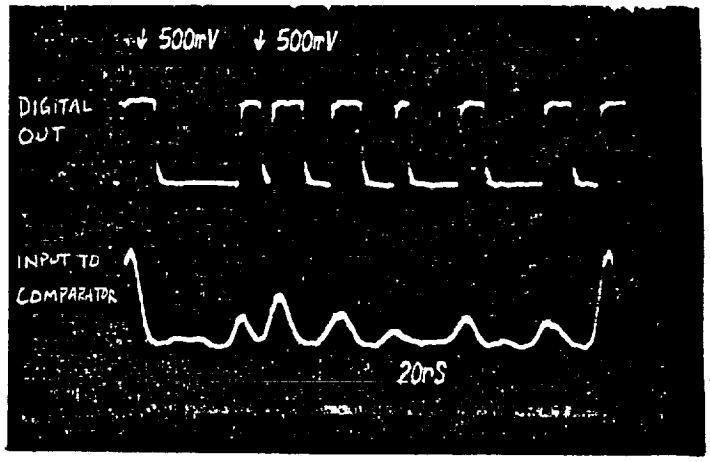
6-1-88

DBT GENERATOR
LAYOUT
AMTD
J. OTT

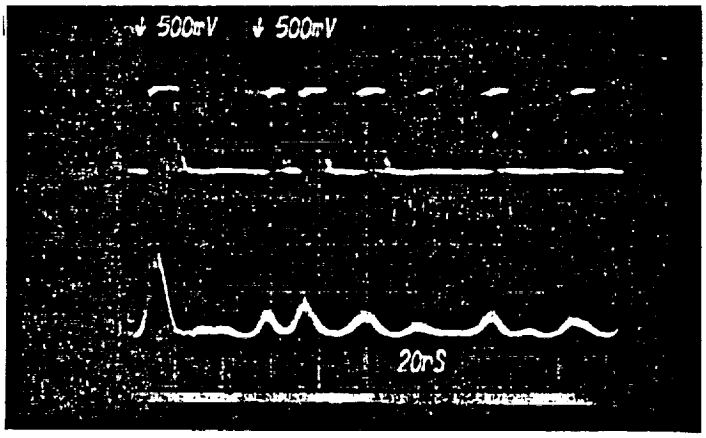


DETECTED BAUD TRANSITION

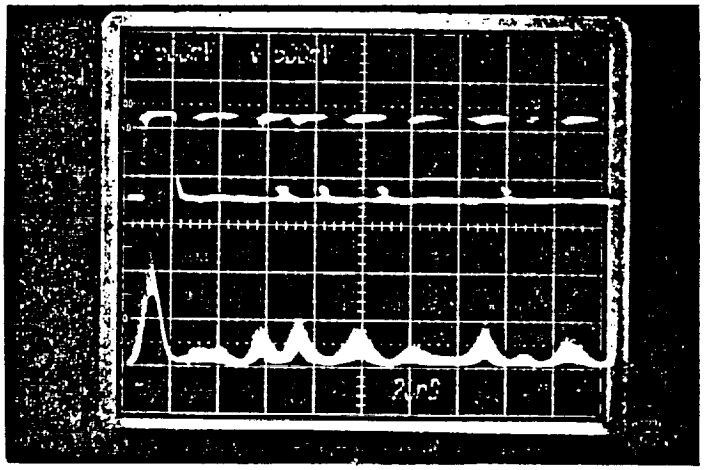
TOP - COMPARATOR OUTPUT
BOTTOM - AM DETECTED SIGNAL



Es/No = 34 dB



Es/No = 19 dB



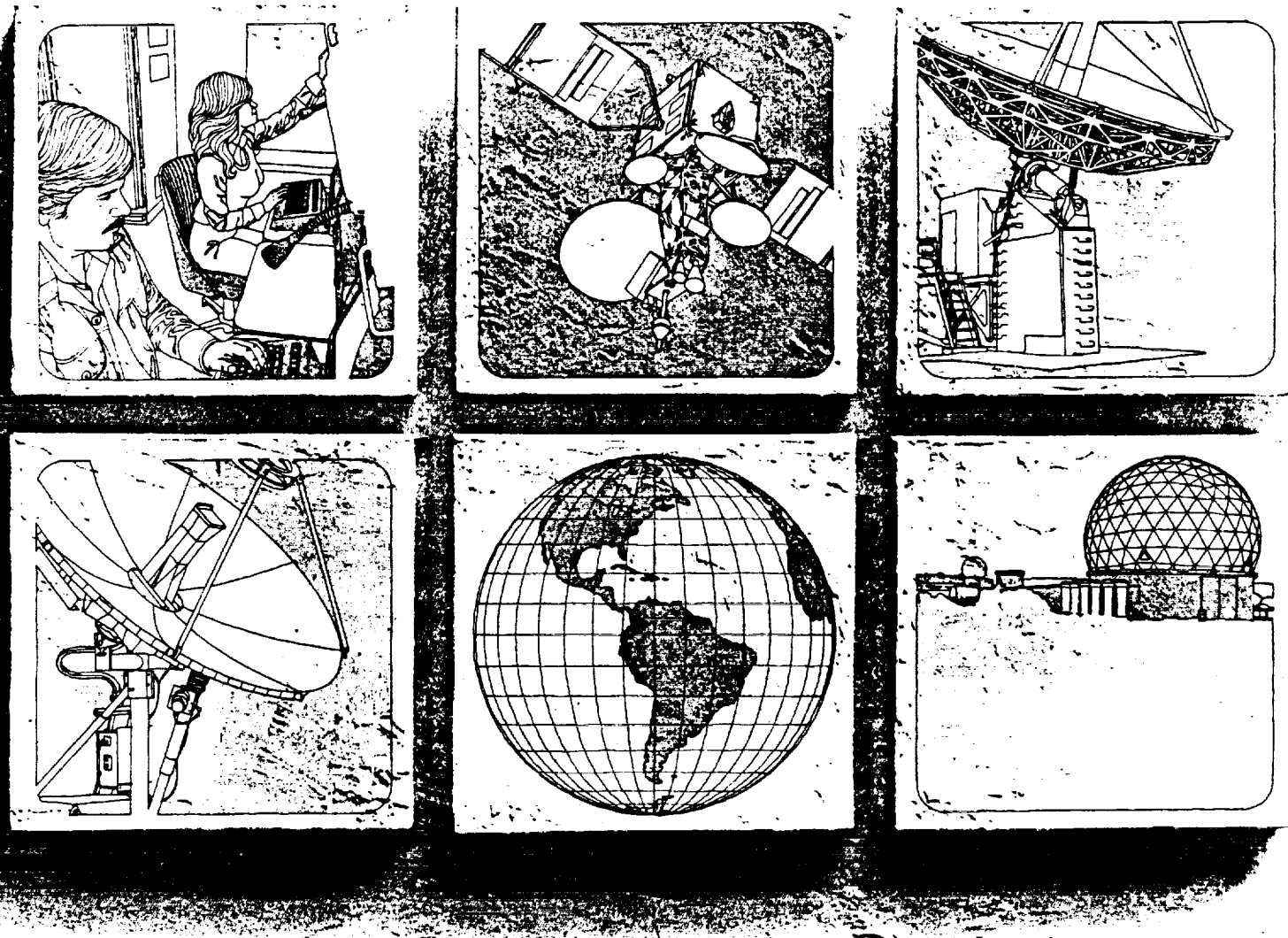
Es/No = 14 dB

AMTD

POC DEMODULATOR

SYSTEM DOCUMENTATION

CARRIER ACQUISITION / BAUD ACQUISITION
SPECIFICATION



Ford Aerospace/Space Systems Division

AMTD

POC DEMODULATOR

SYSTEM DOCUMENTATION

CARRIER ACQUISITION / BAUD ACQUISITION
SPECIFICATION

SEPTEMBER 13, 1988

Ford Aerospace &
Communications Corporation
Western Development
Laboratories Division

3939 Fabian Way
Palo Alto, California 94303

Code Ident. No. 11530

Specification No. SE587939

Title

PROOF-OF-CONCEPT

CARRIER ACQUISITION CHASSIS

AND

BAUD ACQUISITION CHASSIS

(AMTD)

Program/Site _____ Prime Contract Number _____

Spec. Engr. Date	
Resp. Engr.	Program
Product Assurance	
Operations Design	Outside WDL
Engineering Manager	Release Date _____ Page ___ of ___

WDL 572A
12/76

1.0 SCOPE

This specification establishes the performance, design, test, manufacture requirements for the Carrier Acquisition Chassis and the Baud Acquisition Chassis for the Proof-of-Concept (POC) version for the Advanced Modulation Technology Development (AMTD) system.

2.0 APPLICABLE DOCUMENTS

The latest issues of the following documents are a part of this specification.

(a) NAS3-24678 Advanced Technology Satellite Demodulator Development, Statement of Work

(b) 17 Jun 1986 Preliminary Design Review Package

(c) 14 Apr 1988 AMTD Modulation/Demodulation System Specification.

3.0 DESIGN REQUIREMENTS

3.1 Functional Description

The Carrier Acquisition Chassis, as shown in Figure 1, accepts I and Q analog data, the associated clocks at 80 and 240 MHz, and the transmit and burst 1/2 control signals. The chassis acquires the starting phase from a pre-amble of all "zeroes", and then continues to track the carrier phase during the data burst. The chassis provides detected 3-bit data words, in parallel format, at a rate of 80 MBPS; or in serial format, at a rate of 240 MBPS.

The Baud Acquisition Chassis, as shown in Figure 2, accepts the 3-bit words from the Carrier Acquisition Chassis. The chassis detects the Unique Words in the frame format, and generates the transmit and burst 1/2 control signals for the Carrier Acquisition Chassis. The chassis accepts the Detected Baud Transitions (DBT) and generates the 80 MHz clock signal, in phase with the I and Q analog data, for the Carrier Acquisition Chassis. The chassis provides the valid 3-bit words, in serial format, at a rate of 240 MBPS, for further analysis.

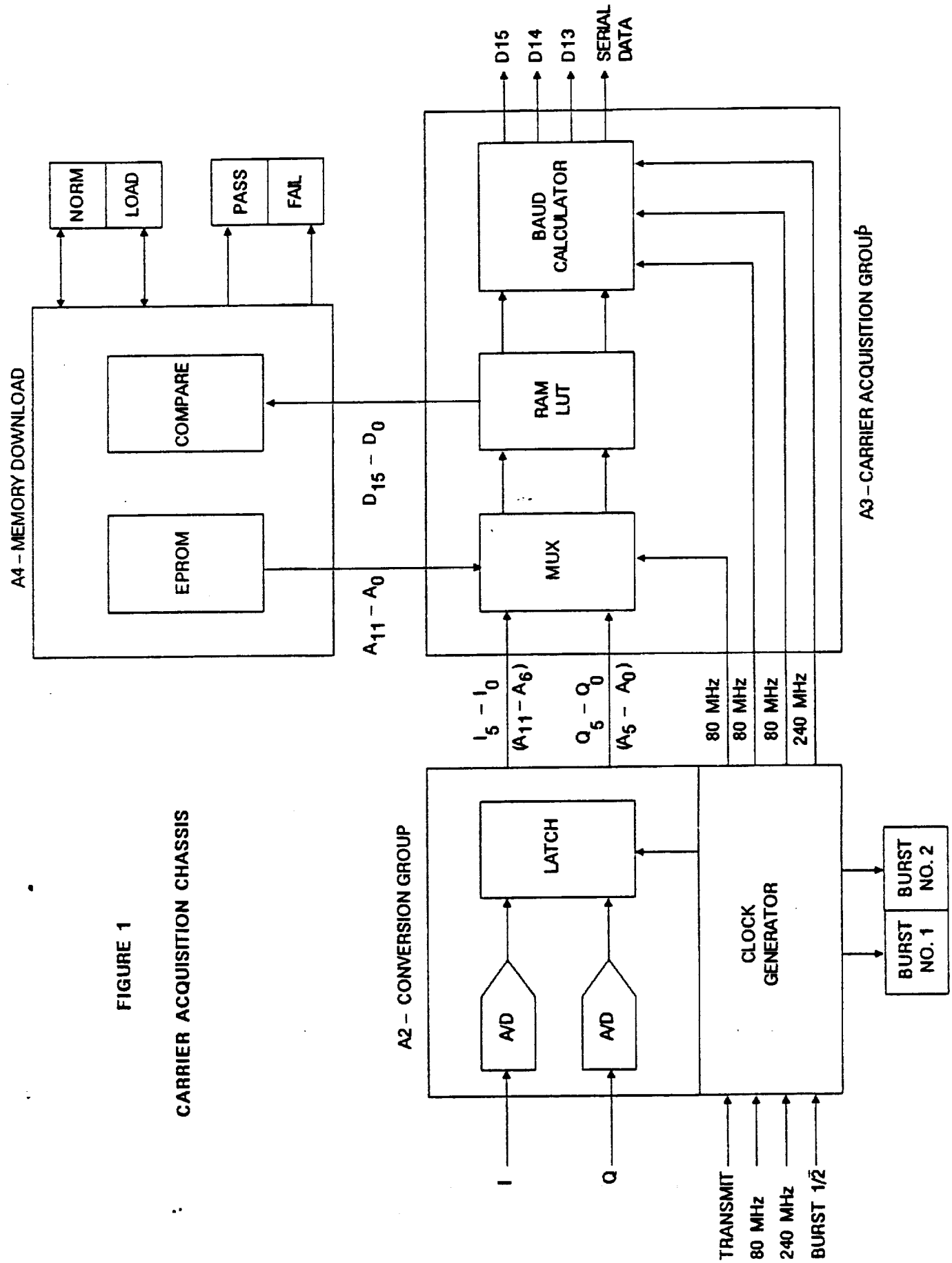
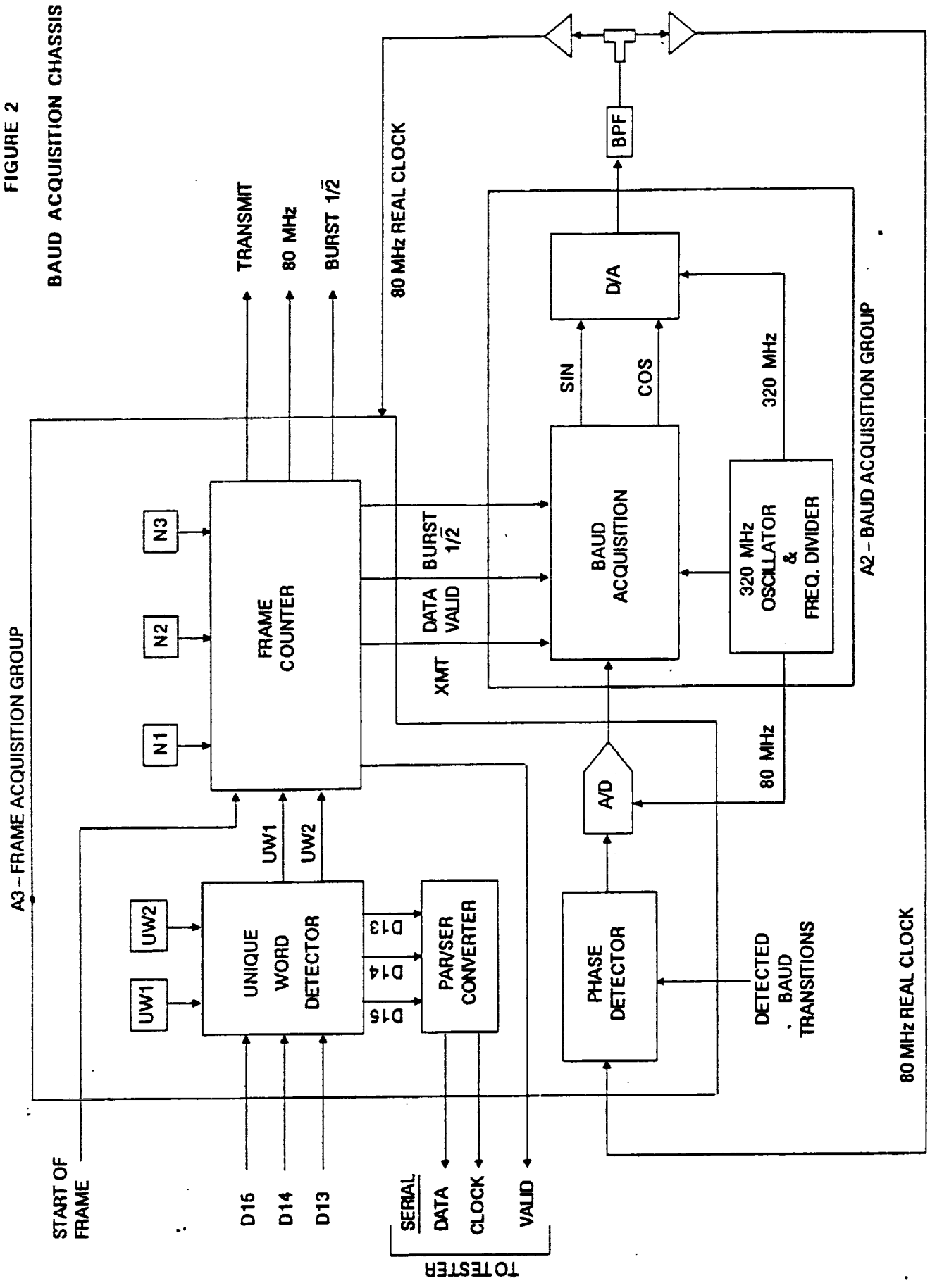


FIGURE 1

CARRIER ACQUISITION CHASSIS

FIGURE 2

BAUD ACQUISITION CHASSIS



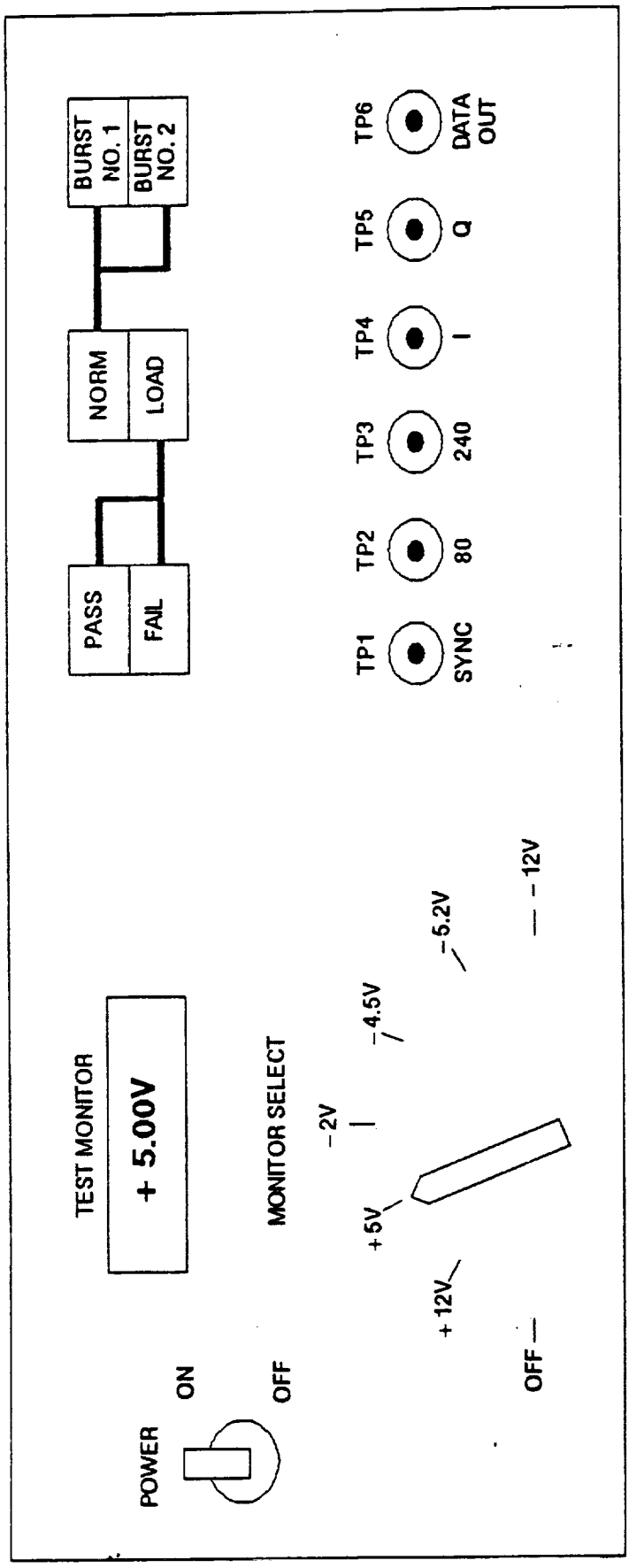


FIGURE 3

CARRIER ACQUISITION FRONT PANEL

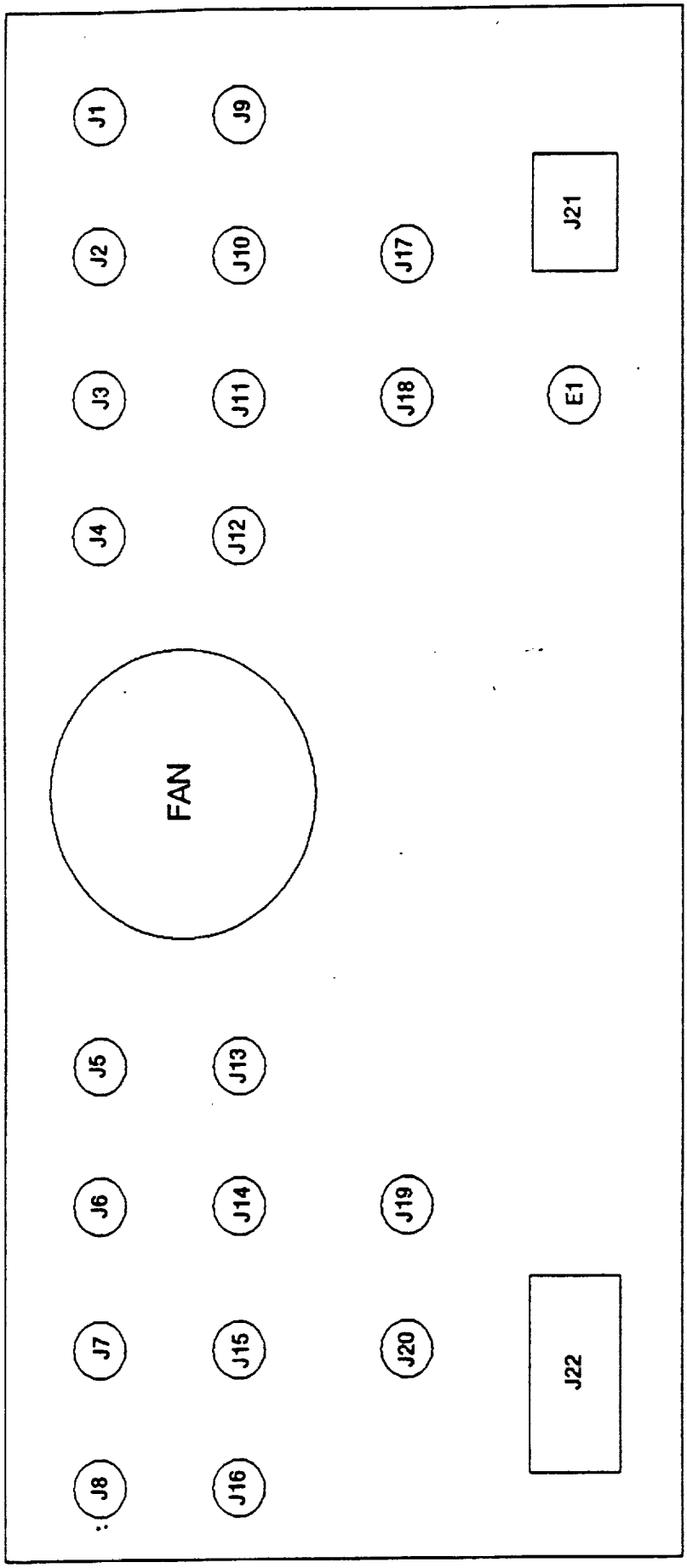


FIGURE 4

CARRIER ACQUISITION REAR PANEL

3.2 Physical Description

The Carrier Acquisition Chassis is rack mounted on slides. The front panel (8 3/4 inches high) and rear panel layouts are shown in Figures 3 and 4 respectively.

The Baud Acquisition Chassis is rack mounted on slides. The front panel (7 inches high) and rear panel layouts are shown in Figures 5 and 6 respectively.

All front panel controls, with the exception of AC Power On/Off, are activated by solid state switches. All front panel status is displayed by LED indicators or digital meters.

3.3 Performance Specifications

3.3.1 Carrier Acquisition Configuration

The Carrier Acquisition Chassis has three major parts: The Conversion Group (A2), the Carrier Acquisition Group (A3), and the Memory Download (A4).

3.3.1.1 Conversion Group (A2). The Conversion plate consists of two AD9002 Evaluation Circuits; and one Clock Generator logic board. The evaluation boards convert the I and Q analog signals into digital equivalent bytes of 6 bits each, at a maximum sample rate of 80 mega samples per second. The two bytes of 6 bits each form the 12 address lines for the Memory Look-Up Table in the Carrier Acquisition Group.

The Clock Generator logic board accepts the transmit and burst 1/2 control signals, and the associated clocks of 80 and 240 MHz. It distributes these clocks through the Carrier Acquisition Module.

3.3.1.2 Carrier Acquisition Group (A3). The Carrier Acquisition plate consists of the Multiplexer logic board, the Memory Look-Up Table, and the Baud Calculator logic board. The Multiplexer selects the 12 address lines from the AD9002 boards during normal operation, and selects the 12 address lines from the Memory Download during the download operation.

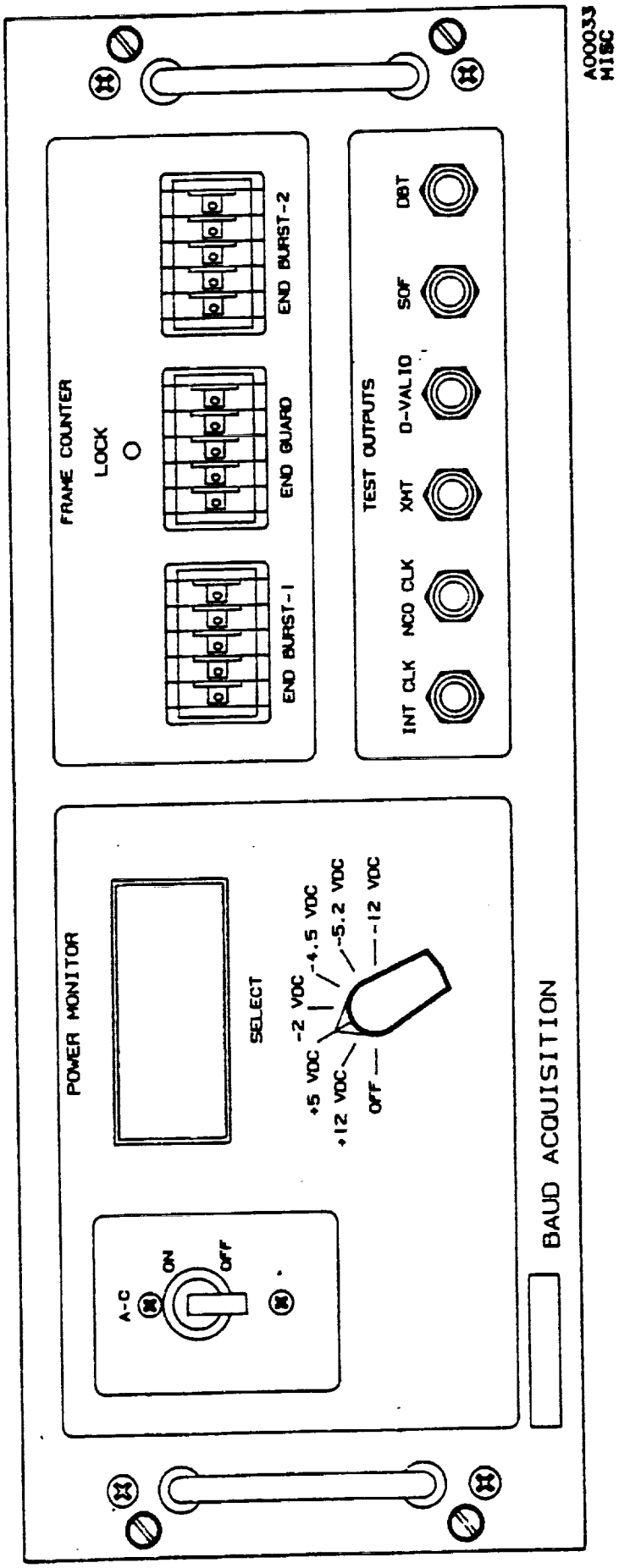


FIGURE 5

BAUD ACQUISITION FRONT PANEL

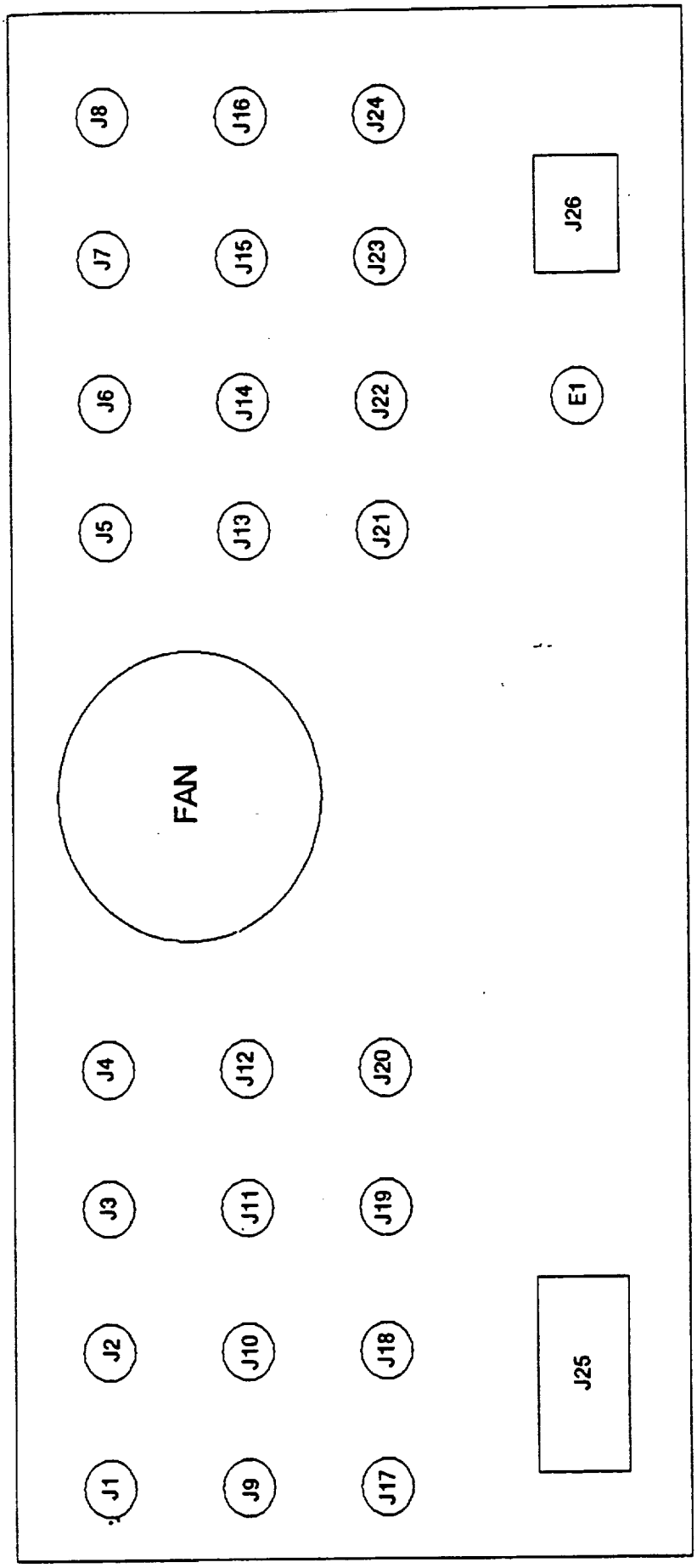


FIGURE 6

BAUD ACQUISITION REAR PANEL

The Memory Look-Up Table provides a cartesian to polar conversion, using the I and Q inputs as the cartesian coordinate address. The board contains high speed RAM chips, which have their contents determined at the time of the memory download.

The Baud Calculator, shown in Figure 7 establishes the starting phase during acquisition, when 32 "zeroes" are transmitted. During acquisition data shifts from 2 to 5 places to the right, to reduce the loop gain. In the track mode the calculator subtracts the averaged carrier phase from the incoming data word, and adds 0.5 for phase correction to detect the 8 PSK data words.

The three most significant bits of this word are passed-on to the Baud Acquisition Chassis. They are also shifted out serially at a maximum rate of 240 MBPS, most significant bit first.

3.3.1.3 Memory Download (A4). The Memory Download board contains two 4Kx16 EPROM locations to provide writing and comparing capabilities for the Look-Up Table (LUT).

At start-up or for a download command the data from the EPROM is written into the Memory LUT. When all 4K words have been written, the download starts the read cycle, to compare each written word with the data in the EPROM. When all words compare correctly, the Memory Download automatically switches the multiplexer back to the normal operating mode. The PASS display illuminates on the front panel. If an error is detected during the compare cycle, then the download stops at the erroneous address. The FAIL display warns the operator of this condition.

Figure 8 gives the memory configuration for the EPROMs and the RAMs.

3.3.2 Baud Acquisition Configuration

The Baud Acquisition Chassis has two major parts: The Baud Acquisition Group (A2) and the Frame Acquisition Group (A3).

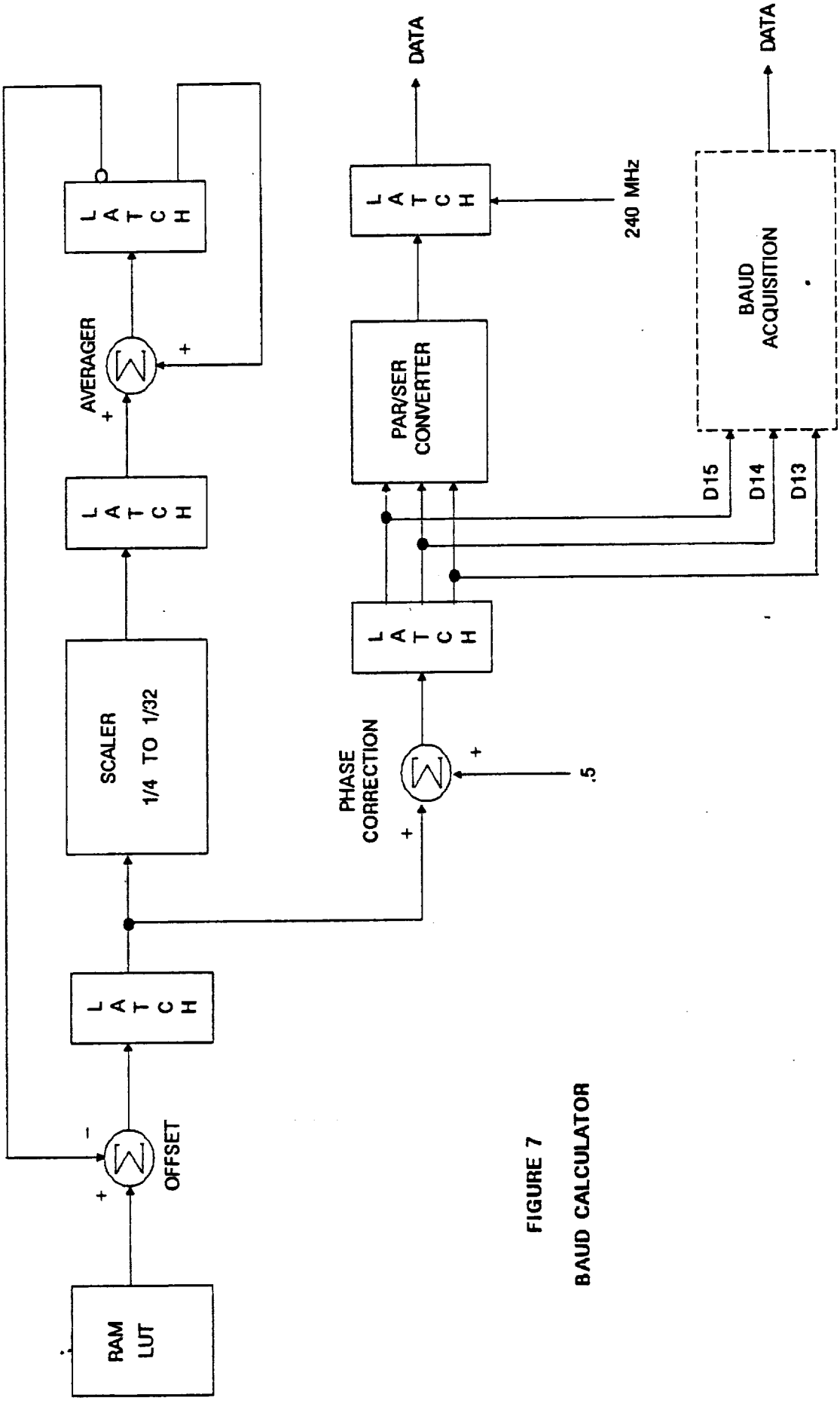


FIGURE 7

BAUD CALCULATOR

Two EPROM files each has two 4096X 8 bit entries

The relation between address and I and Q is:

A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
I_5	I_4	I_3	I_2	I_1	I_0	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0

The entries are made to the following graph:

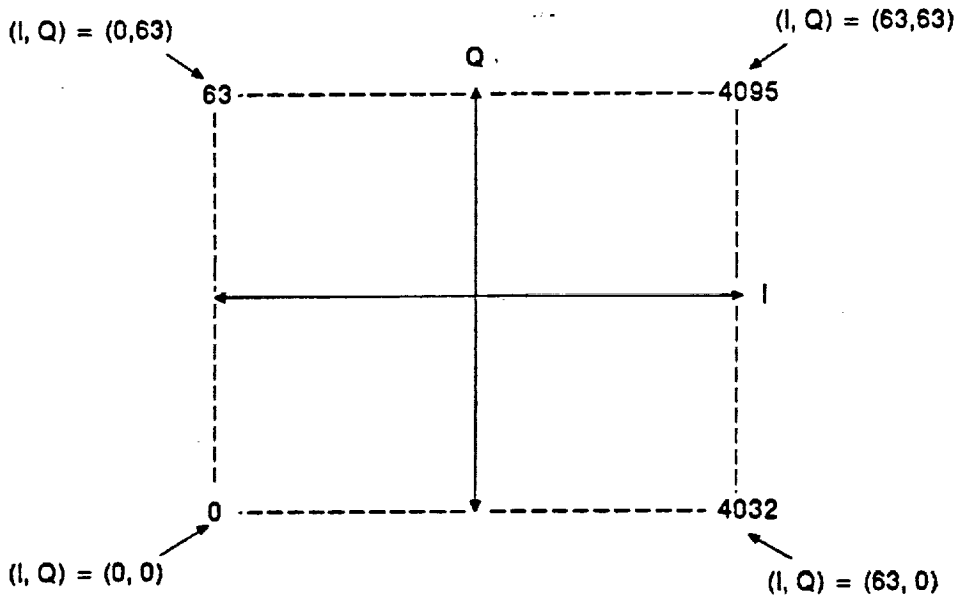


FIGURE 8

PROM FILES FOR CARTESIAN TO POLAR CONVERSION

3.3.2.1 Baud Acquisition Group (A2). The Baud Acquisition tray contains the Oscillator Printed Wiring (PW) logic board, the Baud Acquisition logic board and the Digital/Analog Converter PW logic board. The Oscillator board generates the 320 MHz and 80 MHz clocks to perform the baud calculations.

The Baud Acquisition board shown in Figure 9 generates the real-time clock. This clock is locked in phase with the incoming detected Baud Transitions (DBT), which occur at the 8 PSK symbol transitions. The positive zero crossing of the 80 MHz real-time clock shall be at zero degrees phase, relative to the positive zero crossing of the DBT (see Figure 10). The degrees difference between these two crossings is called Δphase. The Phase Detector measures this Δphase as an analog voltage, and the Analog/Digital Converter converts this voltage into degrees, in digital form. The Baud Acquisition reduces this Δphase to zero. (Both the Phase Detector board and the A/D Converter board are located on the Frame Acquisition tray.) Normally this real time clock and the 80 MHz from the Oscillator are not in phase. In Figure 10 this phase relation is shown as 0_1 for burst 1 and 0_2 for burst 2. The Baud Acquisition retains this phase relation (as point 1 in Figure 10) between bursts. The Baud Acquisition also corrects for any drifts that may exists between the real-time clocks and the Oscillator clock.

PROMs translate the phase relation (0_1, 0_2) into $\pm SIN0_{1,2}$ and $\pm COS0_{1,2}$, which give the amplitudes for 4 points in one period of the real-time clock. The Digital/Analog Converter board in conjunction with the 80 MHz Band Pass Filter (BPF) generates an 80 MHz sine wave from these 4 amplitudes.

3.3.2.2 Frame Acquisition Group (A3). The Frame Acquisition tray contains the Phase Detector PW logic board, the CX20116 A/D Converter PW logic board, the Frame Acquisition logic board, and the Parallel-to-Serial Converter PW logic board.

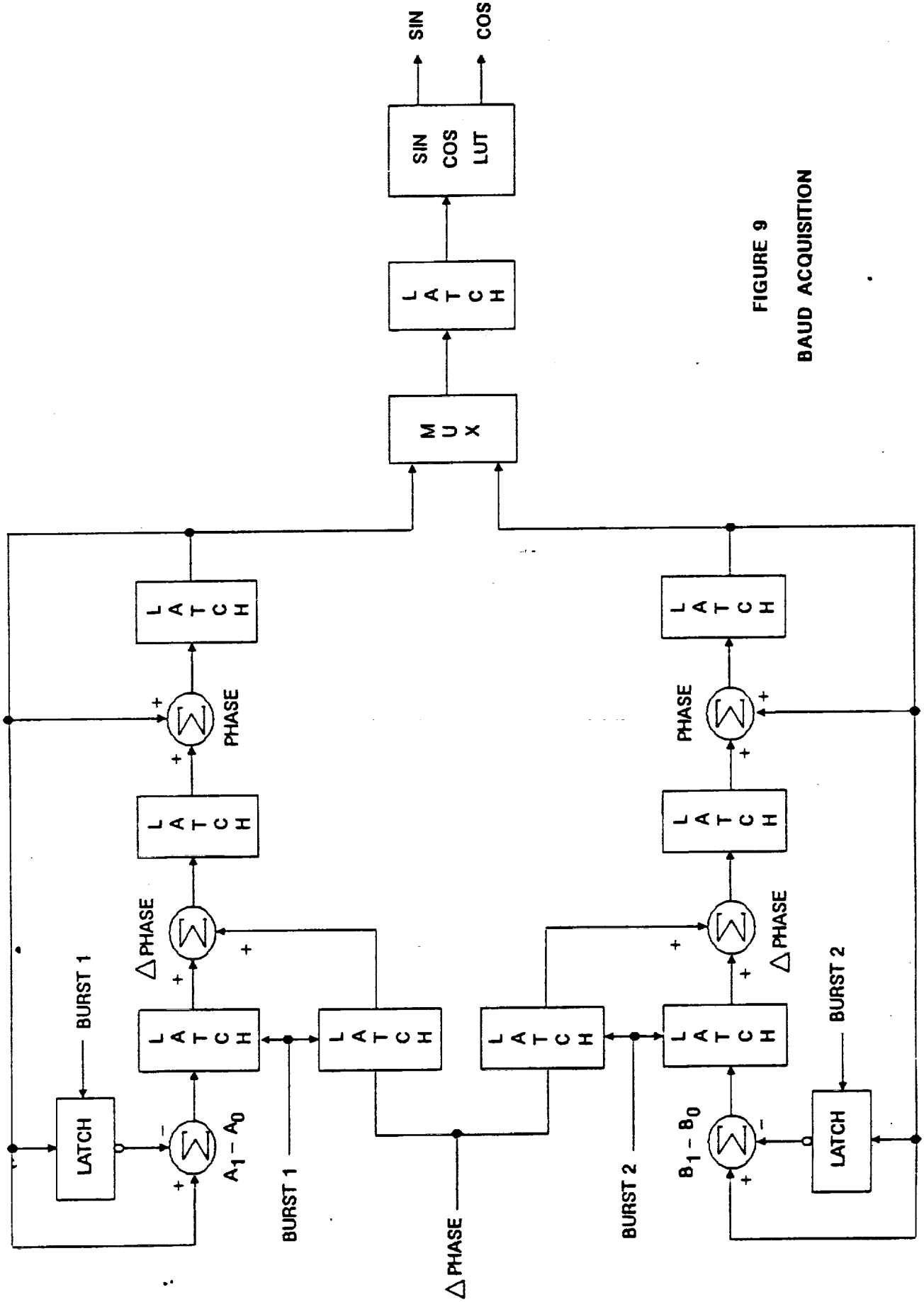


FIGURE 9

BAUD ACQUISITION

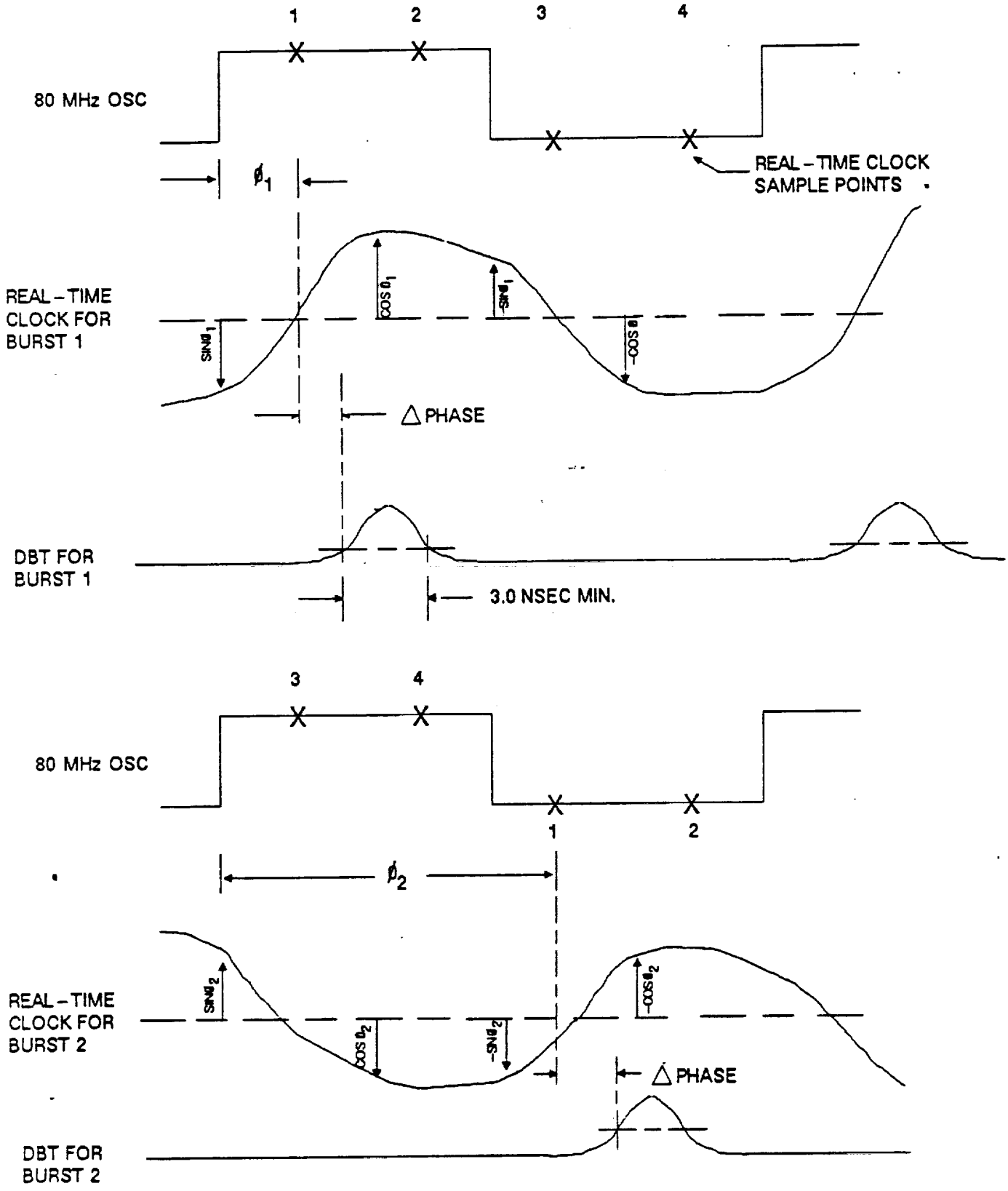


FIGURE 10

BAUD ACQUISITION WAVEFORMS

The Frame Acquisition logic consists of the Unique Word Detector and the Frame Counter. The Frame Counter has adjustable settings for the start and the length of the Burst 1 and Burst 2 messages, as well as for the length of the frame (see Figure 11). It also generates the windows in which Unique Word 1 and Unique Word 2 are allowed to be detected.

The Unique Word Detector has adjustable settings for Word 1 and Word 2, and during the windows these settings are compared to the incoming data streams. At coincidence the data is allowed to pass through the logic to the Parallel-to-Serial Converter. This board converts the three-bit parallel digital data words into a serial format at a maximum rate of 240 MBPS, most significant bit first.

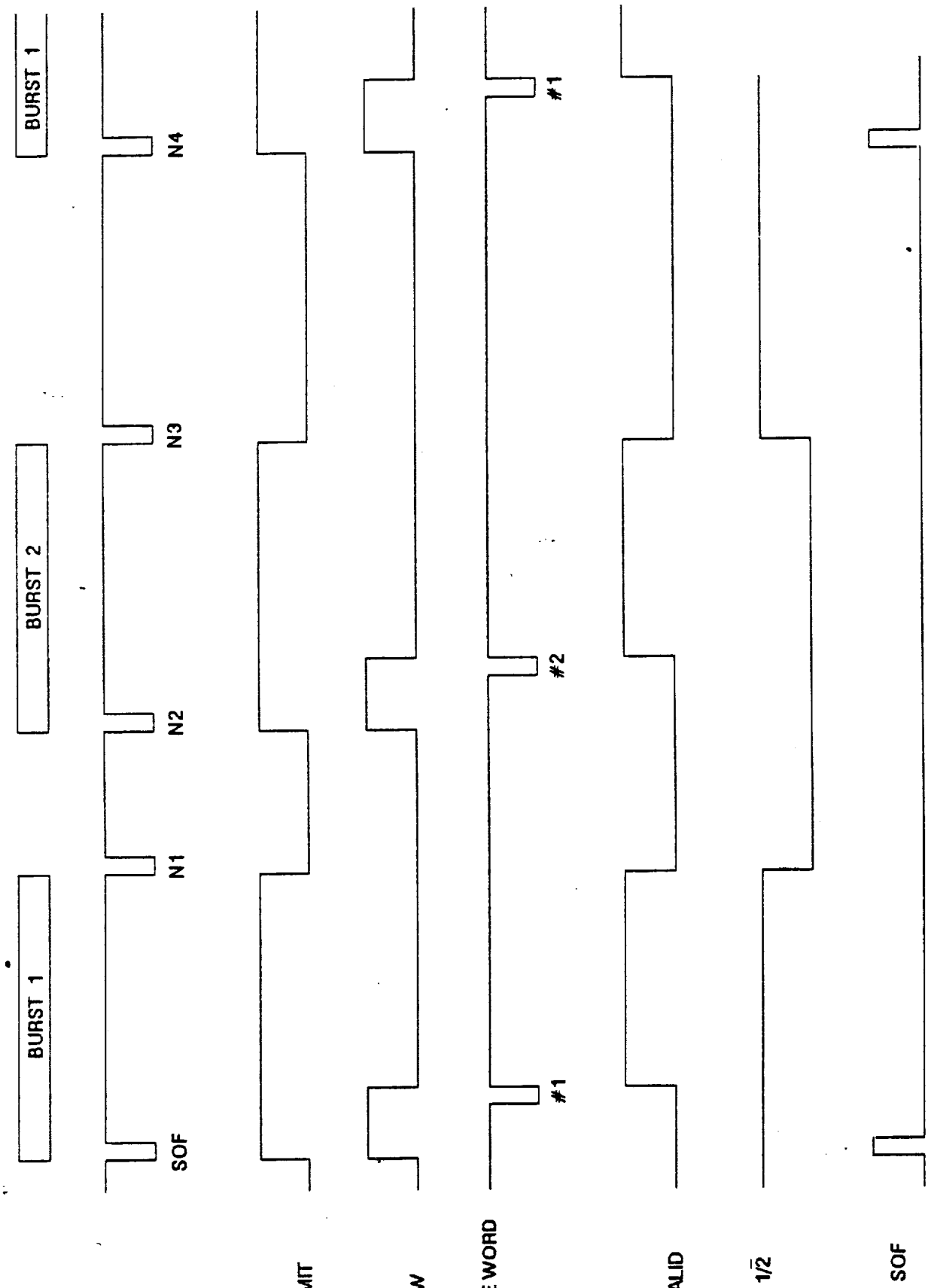
The Start-of-Frame (SOF) signal from the Burst Formatter is received for acquisition only. After detection of the first Unique Word 1 the Frame Counter runs autonomously in the locked mode. For each detection of Unique Word 1 the Frame Counter is preset to an adjustable number, so that this counter remains synchronized with the Frame Counter in the Burst Formatter.

3.3.3 Control And Status Specifications

Switches on the front panel control the operation of the Carrier Acquisition Chassis as specified in section 3.3.3.1.

The Carrier Acquisition Chassis monitors the status of its operation for display on the front panel as specified in section 3.3.3.2.

Switches on the front panel control the operation of the Baud Acquisition Chassis as specified in section 3.3.3.4.



FIUGRE 11

FRAME COUNTER TIMING DIAGRAM

3.3.3.1 Carrier Acquisition Control Functions. The Chassis has three switches for local control of the chassis operation. These switches provide the following functions:

- o Power On/Off — This switch controls the main power to the power supplies.
- o Norm/Load — This switch controls the mode of operation. In the NORM position the Multiplexer selects the A/D outputs as address lines to the Memory LUT. In the LOAD position the Memory Download performs the operation described in section 3.3.1.3.
- o EPROM 1/EPROM 2 (+12V) (-12V) — This switch selects one of the two EPROM locations on the Memory Download. With the monitor switch in the +12V position the Memory Download selects EPROM No. 1. With the monitor switch in the -12V position the Memory Download selects EPROM No. 2.

3.3.3.2 Carrier Acquisition Status Functions. The chassis has the following displays to monitor its operation:

- o PASS/FAIL — This display indicates the results of the last down-load. The PASS indicator is lit, when the last down-load was error free. The FAIL indicator is lit, when an error occurred in the last down-load.

- o NORM/LOAD — This display indicates the mode of operation. The NORM indicator is lit, when the module is in normal operation. The LOAD indicator is lit, when the module performs the down-load operation.

- o BURST 1/BURST 2 — This display indicates which burst is active. The BURST 1 indicator is lit, when the Frame Counter selects burst 1. The BURST 2 indicator is lit, when the Frame Counter selects burst 2.

3.3.3.3 Carrier Acquisition Monitoring Points. In addition to the displays the following signals appear on output jacks, with appropriate drivers for monitoring on oscilloscopes:

- o TP 1 SYNC - Start of the frame
- o TP 2 80 - 80 Mhz real clock
- o TP 3 240 - 240 MHz serial clock
- o TP 4 I - Reconstructed I input
- o TP 5 Q - Reconstructed Q input
- o TP 6 DATA - Serial data out

3.3.3.4 Baud Acquisition Control Functions. The front panel has one power switch and three sets of thumbwheel switches for local control of the chassis operation. These switches provide the following functions:

- o Power On/Off — This switch controls the main power to the power supplies.

- o End Burst 1 — This set provides the control Function N1, the end of Burst No. 1. The 5 digit number is in hexadecimal format.

- o End Guard — This set provides the control Function N2, the end of the guard between bursts. The 5 digit number is in hexadecimal format.
- o End Burst 2 — This set provides the control Function N3, the end of Burst No. 2. The 5 digit number is in hexadecimal format.

3.3.3.5 Baud Acquisition Status Function. The chassis has the following display to monitor its operation:

- o LOCKED — This display indicates the mode of the Frame Counter. The display is OFF when the Frame Counter is in the acquisition mode. The display is ON when the Frame Counter is in the autonomous (locked) mode.

3.3.3.6 Baud Acquisition Monitoring Points. The front panel has the following signals appearing on output jacks, with appropriate drivers for monitoring on oscilloscopes:

- o TP 1 INT CLOCK - 80 MHz from oscillator
- o TP 2 NCO CLOCK - 80 MHz real clock
- o TP 3 XMT - Transmit signal
- o TP 4 DATA VALID - Data valid signal
- o TP 5 SOF - Incoming Detected Baud Transition
- o TP 6 DBT - Incoming Start-of-Frame

3.4 Interface Specifications

This section describes the external interfaces to both chassis. All interfaces are via the rear panels. Table 3.4.1 lists the connector assignments for the Carrier Acquisition Chassis, and Table 3.4.2 lists the connector assignments for the Baud Acquisition Chassis.

3.4.1 Burst Formatter Interface. The Baud Acquisition Chassis receives the following signal from the Burst Formatter:

3.4.1.1 Start-of-Frame (SOF) or Transmit Control signal. This signal indicates the presence of a burst 1 when Transmit (+) is more positive than Transmit (Inv).

This control signal shall be ECL driven and DC coupled as shown in Figure 12.

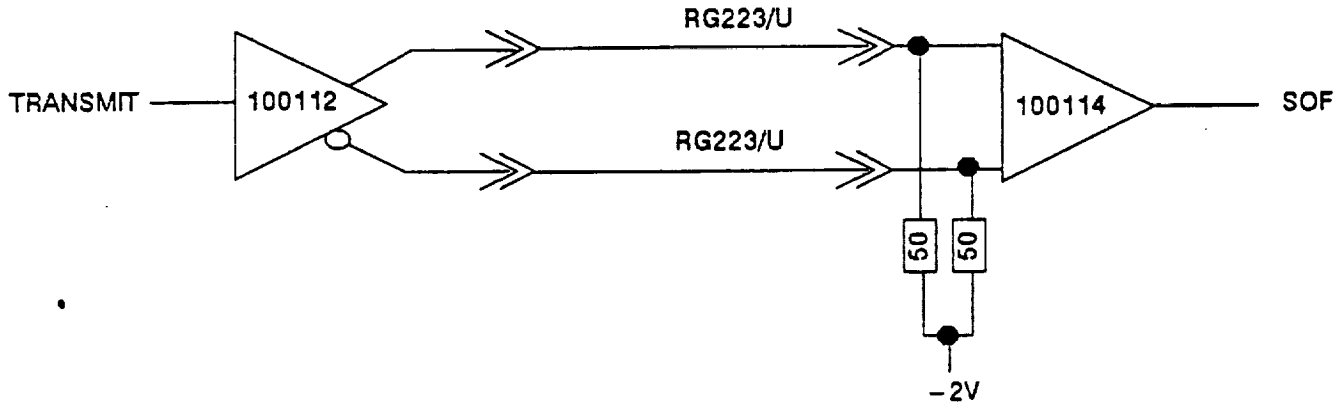


FIGURE 12

SOF INTERFACE CIRCUIT

CONN.	SIGNAL	INTERFACE
J1	BURST 1/2 IN	BAUD AC. – J21
J2	DATA OUT – D15	BAUD AC. – J5
J3	DATA OUT – D14	BAUD AC. – J7
J4	DATA OUT – D13	BAUD AC. – J13
J5	ANALOG IN – I	QUAD DET. – I
J6	CLOCK IN – 80 MHz	BAUD AC. – J23
J7	CLOCK IN – 240 MHz	
J8	TRANSMIT IN	BAUD AC. – J15
J9	BURST 1/2 IN – INV.	BAUD AC. – J22
J10	DATA OUT – D15 – INV.	BAUD AC. – J6
J11	DATA OUT – D14 – INV.	BAUD AC. – J8
J12	DATA OUT – D13 – INV.	BAUD AC. – J14
J13	ANALOG IN – Q	QUAD DET. – Q
J14	CLOCK IN – 80 MHz – INV.	BAUD AC. – J24
J15	CLOCK IN – 240 MHz – INV.	
J16	TRANSMIT IN – INV.	BAUD AC. – J16
J17	SER. CLOCK OUT – INV.	
J18	SER. CLOCK OUT	
J19	SER. CLOCK OUT – INV.	
J20	SER. DATA OUT	
J21	POWER 115VAC – 60 Hz	
J22	SPARE	

TABLE 3.4.1

CARRIER ACQUISITION INTERFACE CONNECTORS

CONN.	SIGNAL	INTERFACE
J1	START – OF – FRAME	BURST FORM.
J2	START – OF – FRAME – INV.	BURST FORM.
J3	DET. BAUD TRANS.	BURST FORM.
J4	DET. BAUD TRANS. – INV.	BURST FORM.
J5	DATA IN – D15	CARRIER AC. – J2
J6	DATA IN – D15 – INV.	CARRIER AC. – J10
J7	DATA IN – D14	CARRIER AC. – J3
J8	DATA IN – D14 – INV.	CARRIER AC. – J11
J9	DATA VALID OUT	TESTER
J10	DATA VALID OUT – INV.	TESTER
J11	SER. DATA OUT	TESTER
J12	SER. DATA OUT – INV.	TESTER
J13	DATA IN – D13	CARRIER AC. – J4
J14	DATA IN – D13 – INV.	CARRIER AC. – J12
J15	TRANSMIT OUT	CARRIER AC. – J8
J16	TRANSMIT OUT – INV.	CARRIER AC. – J16
J17	SER. CLOCK OUT	TESTER
J18	SER. CLOCK OUT – INV.	TESTER
J19	SPARE	
J20	SPARE	
J21	BURST $1/\bar{2}$ OUT	CARRIER AC. – J1
J22	BURST $1/\bar{2}$ OUT – INV.	CARRIER AC. – J9
J23	CLOCK OUT – 80 MHz	CARRIER AC. – J6
J24	CLOCK OUT – 80 MHz – INV.	CARRIER AC. – J14
J25	SPARE	
J26	POWER 115VAC – 60 Hz	

TABLE 3.4.2

BAUD ACQUISITION INTERFACE CONNECTORS

3.4.2 Quadrature Detector. The Carrier Acquisition Chassis receives two single ended analog data signals (I and Q), which are associated with Detected-Baud-Transitions. The Baud Acquisition Chassis receives these DBTs.

The analog data signals shall have the following performance:

3.4.2.1 Data Rates. The inputs are analog signals which are recognized to change in steps at a rate of maximum 80 mega steps per second. The accuracy is ±.25%.

3.4.2.2 Analog Voltage. The analog inputs shall be measured in steps of 4 mVolts. The minimum voltage is -1 volts ±2% (binary equivalent is 000.000). The maximum voltage is 0 volts ±2% (binary equivalent is 111.111).

3.4.2.3 Input Impedance. The data lines have an impedance of 50 ohm ±5% to ground.

3.4.2.4 Input Circuit. The single ended data lines are DC coupled as shown in Figure 13.

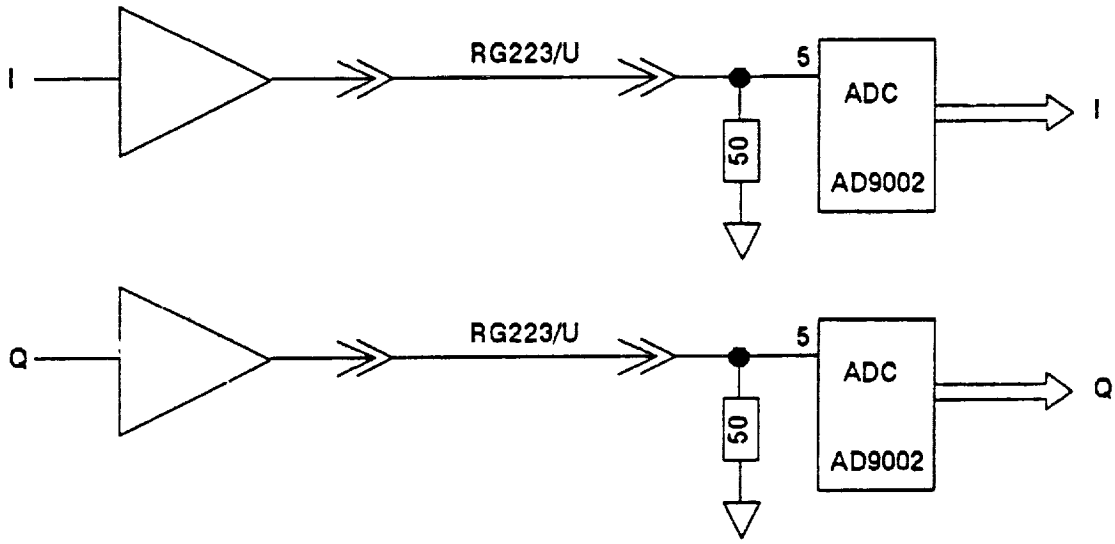


FIGURE 13

ANALOG INTERFACE CIRCUIT

3.4.2.5 Detected-Baud-Transitions (DBT) or the 80 MHz pulses, which are associated with the real-time clock.

The DBT shall be an ECL signal at a nominal rate of 80 MPPS. The pulse width shall be at least 3 nsec. It shall be DC coupled as shown in Figure 14.

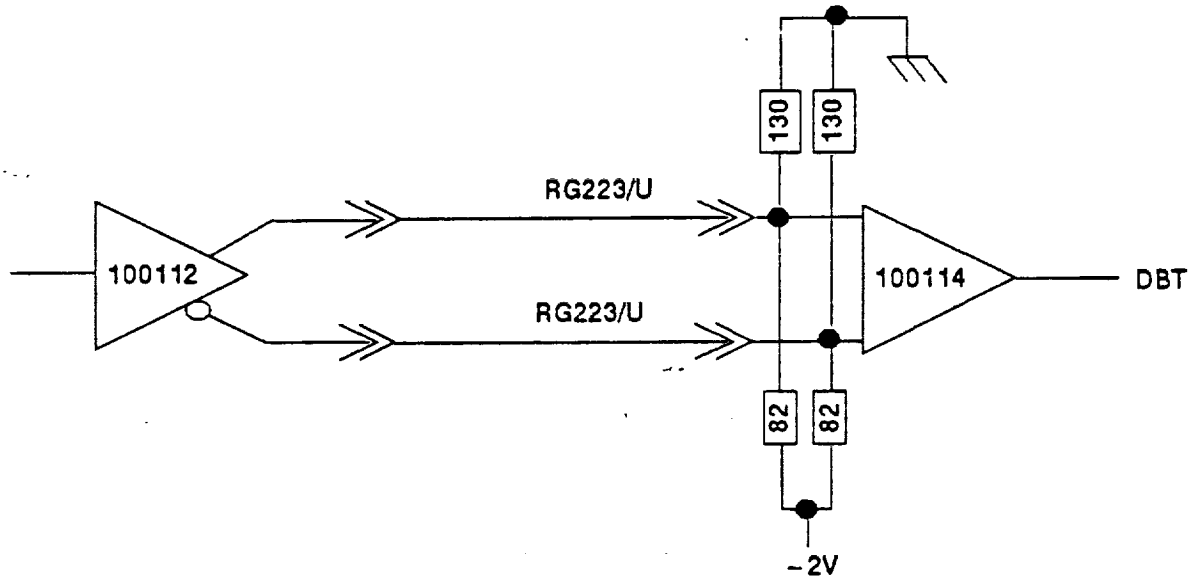


FIGURE 14

DBT INTERFACE CIRCUIT

3.4.3 Tester Interface. The Baud Acquisition Chassis transmits the following three signals to the tester:

3.4.3.1 Data Valid. This signal indicates valid data on the Serial Data Output when Data Valid (+) is more positive than Data Valid (Inv.)

This control signal is ECL driven and shall be DC coupled as shown in Figure 15.

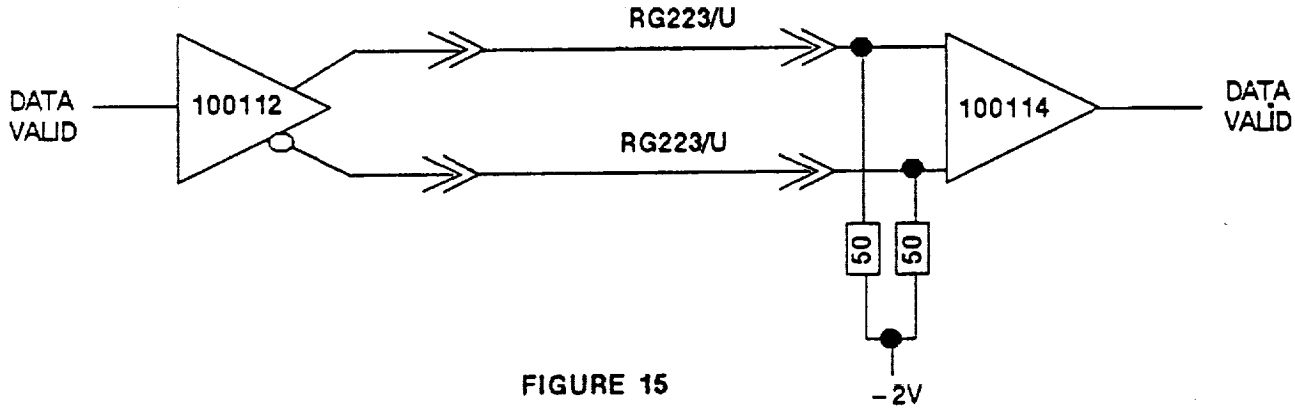


FIGURE 15

DATA VALID INTERFACE CIRCUIT

3.4.3.2 Serial Data Out. The Baud Acquisition Chassis provides the three most significant bits of the valid data words in gray code and in serial format, at a rate of 240 MBPS ±2%, most significant bit first.

This data signal is ECL driven and shall be DC coupled as shown in Figure 16.

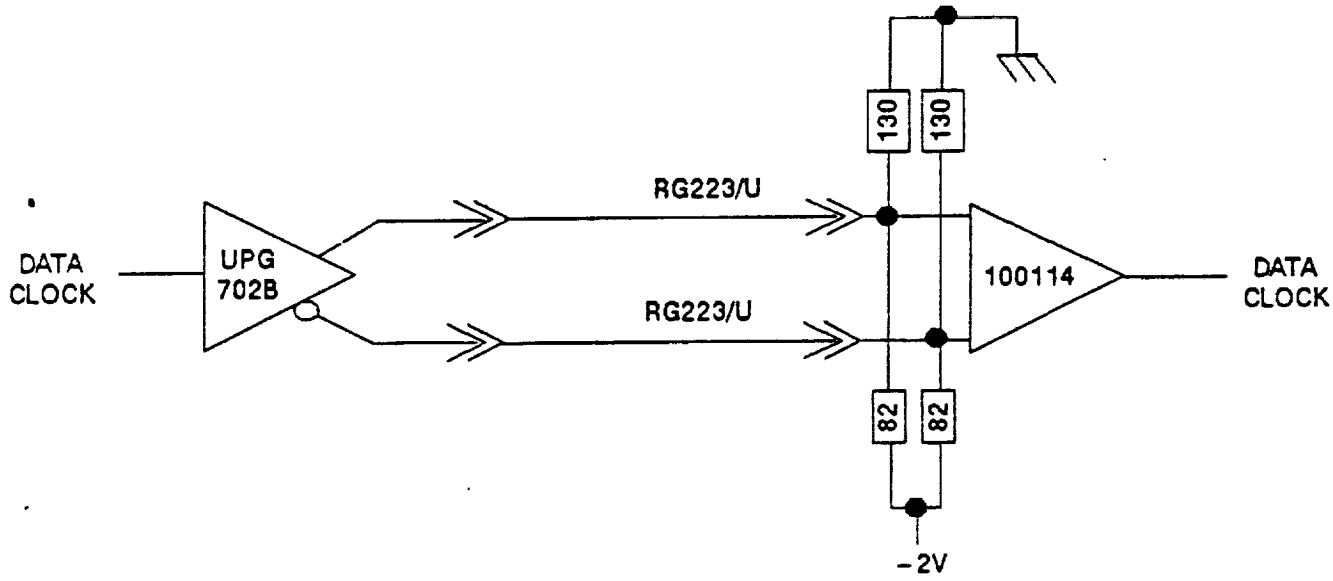


FIGURE 16

SERIAL OUTPUT INTERFACE

3.4.3.3 Serial Clock Out. The Baud Acquisition Chassis provides the associated serial clock at a rate of 240 MHz ±2%.

This Clock signal is ECL driven and shall be DC coupled as shown in Figure 17.

The phase difference between data and clock is less than 0.55 nanoseconds, (see Figure 15). This is measured at the rear panel.

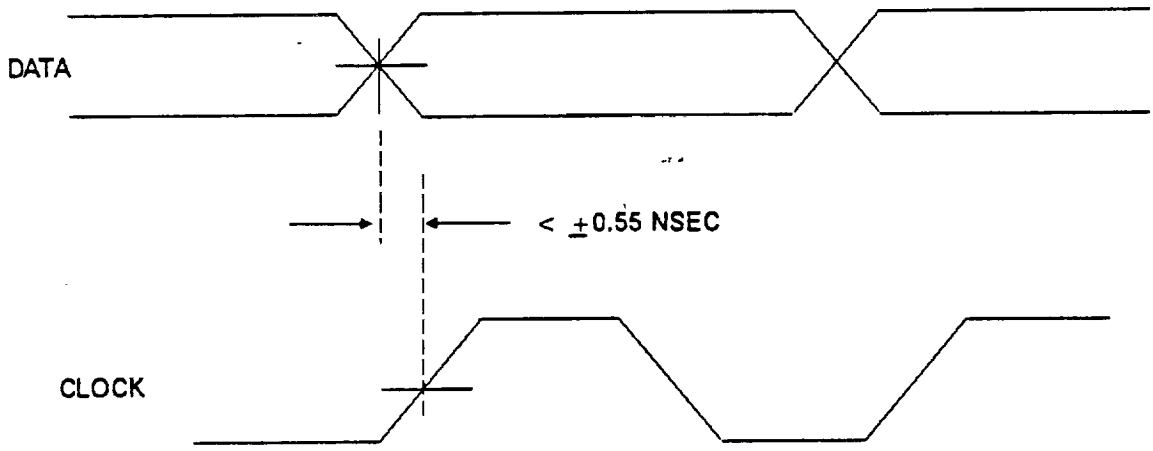


FIGURE 17

SERIAL OUTPUT WAVEFORMS

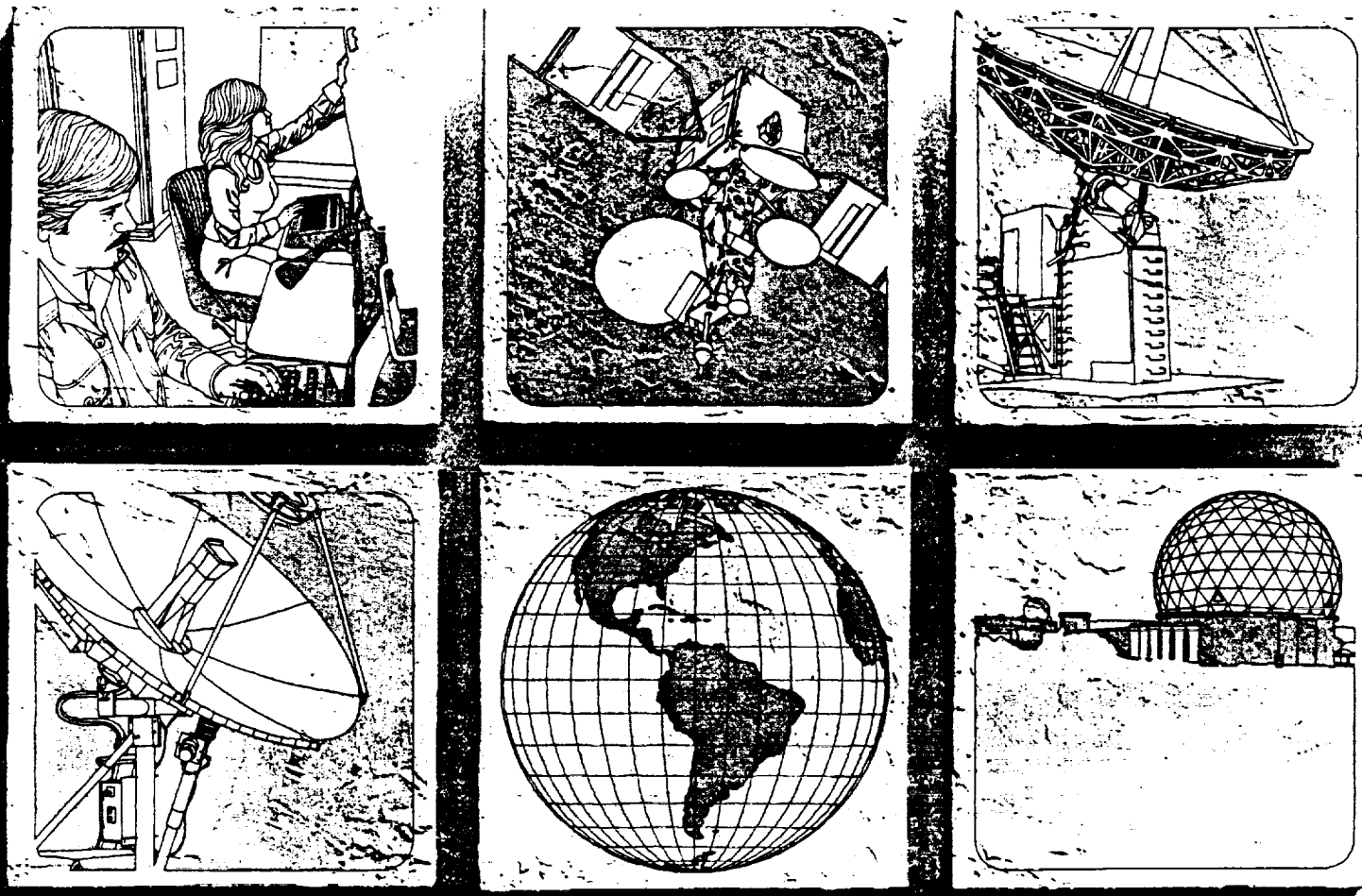
3.4.4 AC Power Both Acquisition Chassis operate on 120 volts AC ±10% and 60 Hz ±5%. Their combined maximum current is TBD Amps.

AMTD

SPECIAL TEST EQUIPMENT

SYSTEM DOCUMENTATION

INTERFERENCE/NOISE GENERATOR
OPERATIONS MANUAL



Ford Aerospace/Space Systems Division

AMTD

SPECIAL TEST EQUIPMENT

SYSTEM DOCUMENTATION

INTERFERENCE/NOISE GENERATOR
OPERATIONS MANUAL

MAY 24, 1989

OPERATIONS MANUAL

INTERFERENCE/NOISE GENERATOR

(AMTD)

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TABLE OF FIGURES

1. GENERAL DESCRIPTION

The Interference/Noise Generator provides for the following conditions to simulate actual signal path degradations:

1. Insertion of transmit and receive Nyquist filtering.

2. Addition of average white Gaussian noise to the received signal.

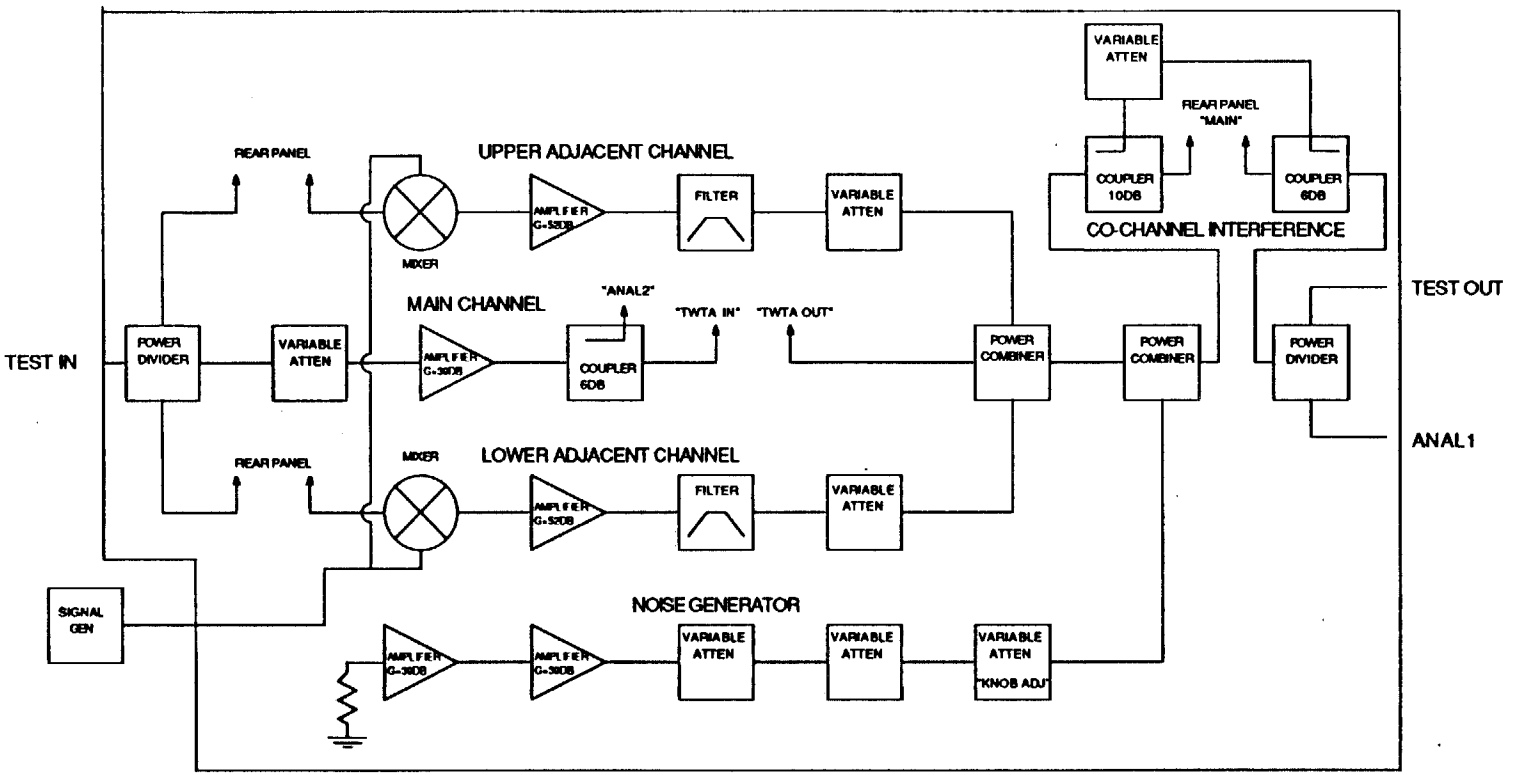
3. Addition of two interfering signals centered 96 MHz away from the main signal path.

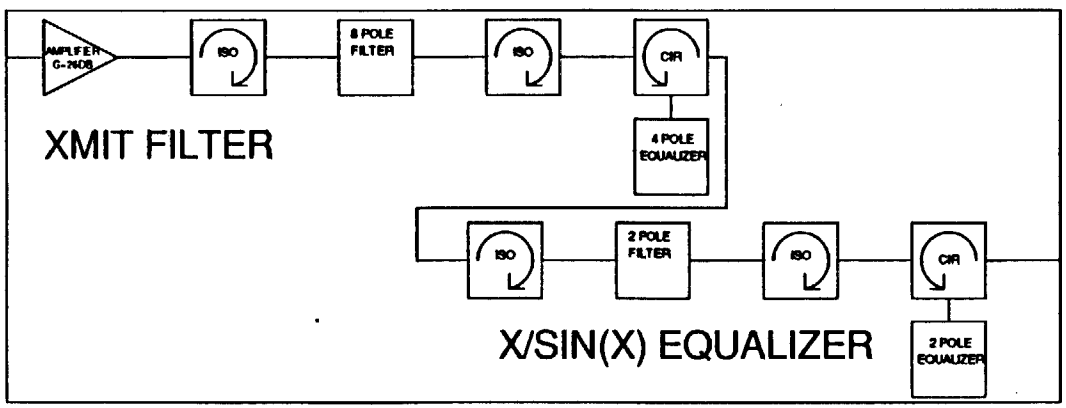
4. Traveling wave tube amplification to simulate saturated conditions.

5. Addition of co-channel interference to due inadequate antenna feed isolation.

Figure 1 shows the block diagram of the Interference/Noise Generator. The Nyquist filters are contained in the same box as the Interference equipment but are not internally connected. The modulated signal first is filtered by the transmit square root Nyquist filter, along with a sin(x)/(x) equalizer to correct for rectangular pulses. An amplifier is added to compensate for the filtering losses. The filtered signal is connected by an external cable to the Interference section. The signal is there split three ways. The main channel is first fed to a variable attenuator, and then to a 40 dB amplifier. External connectors allow the insertion of a TWTA after the 40 dB amplifier. By adjusting the variable attenuator it is possible to adjust the amount of TWTA backoff desired. After amplification, the signal is attenuated and combined with the adjacent frequency interfering signals. The interfering signals are created by first adding a delay and then mixing the main signal with a 96(nominal) MHz external oscillator. The upper and lower interferers are delayed internally by a image rejection filter and connecting cables(~30 ns). Greater delays may be added using external cables connected to the back of the unit. The mixers are followed by an amplifier, a variable attenuator and an filter(to pick out the appropriate signal), and then combined with the main signal. Noise is added to the combined signals using a pair of cascaded 40 dB amplifiers. Two screw adjustable attenuators and one front panel knob adjustable attenuator reduce the noise power to the desired level. A 2 way combiner adds this noise to the modulated signal. Co-channel interference is added by using 2 couplers to create a parallel signal path adjustable by a variable attenuator. The signal is then split 2 ways and fed to the front panel to allow monitoring of the resultant spectrum. An external cable feeds the modulated, interfered signal to the receive square root Nyquist filter, which then provides the output to the Quadrature Detector.

AMTD INTERFERENCE AND NOISE TEST SET CHASSIS





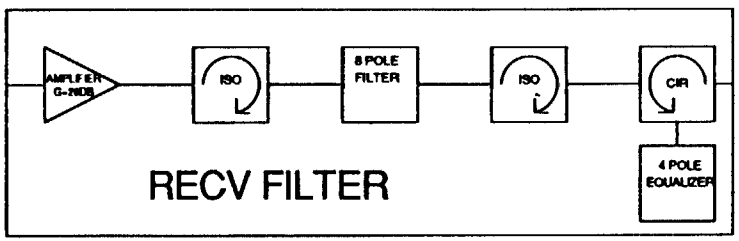


Figure 1 Interference/Noise Generator Block Diagram

2. FRONT PANEL

The front panel is shown in Figure 2.

2.1 AC POWER

The AC power group consists of the circuit breaker and a LED on indicator.

2.2 ADJ FREQ

The Adjust Frequency group is a SMA female connector used for input of the adjacent channel interference offset frequency.
The input level should be set to 3(nominal) dBm on the HP8601A generator.

2.3 SIG LEVEL

The Signal Level group provides a screwdriver adjustment for the main, adjacent channel, and noise power levels. Approximately 20 dB of adjustment is possible for the modulated levels and 40 dB for the noise power levels.

2.4 XMIT

The Xmit group are SMA female inputs and outputs to the transmit Nyquist filters. Also included in this circuit is a 26 dB amplifier, giving an overall gain of ~13 dB.

2.5 TEST/TEST PT

The Test group are SMA female inputs and outputs to the Interference and Noise Test circuits. Added in this block are the noise, adjacent channel, TWTA saturation, and co-channel interferers. Its overall gain is approximately 0 dB for the main modulated channel. The Test Pt group consists of ANAL1, which is identical in output to the Test Out port, and ANAL2, which is a 6 dB coupler for sampling the TWTA input drive.

2.6 RCV

The Rcv group are SMA female inputs and outputs to the receive Nyquist filters. This group has an overall loss of ~3 dB.

2.7 NOISE LEVEL

The noise level group consists of a vernier adjustment of the added noise power for use in making BER curves. The adjustment

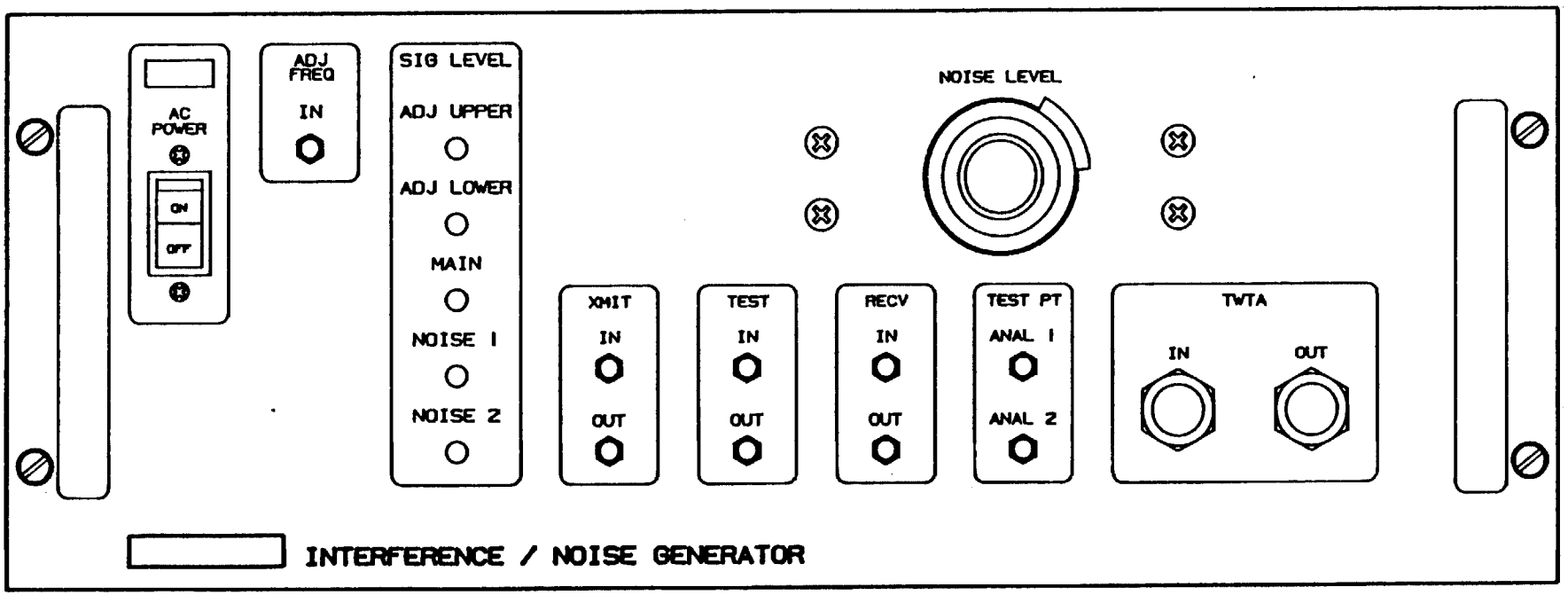


Figure 2 Interference/Noise Generator Front Panel

available is ~20 dB. This adjustment, along with the screwdriver adjust noise attenuators make over a 50 dB range of noise power.

2.8 TWTA

The TWTA group are Type N female inputs and outputs to the external HP 491 TWTA. The TWTA has a gain of typically 30 dB. A 30 db attenuator should be added after the TWTA to compensate for its extra gain. The gain of the TWTA may be adjusted using the knob on the front panel of the TWTA.

3. REAR PANEL

The rear panel is shown in Figure 3.

3.1 AC POWER

An AC power socket requires 120 V. 60 hz input via a HP type power cable.

3.2 ADJACENT CHANNEL DELAYS

Two pairs of Type N female connectors provide means of adding delays to the adjacent channels.

3.3 MAIN CHANNEL DELAYS

A pair of Type N female connectors provide means of adding delays to the main channel.

3.4 CO-CHANNEL ATTENUATOR

An opening on the right side of the rear panel allows adjustment of the co-channel interference level.

4. OPERATION

4.1 INITIAL SET-UP

To set up the Interference/Noise Generator requires an HP435A power meter with a 8484A power sensor, the modulator,the synthesizer LO, the TWTA(if desired), the HP8601A adjacent channel LO, the HP8566 spectrum analyzer, and the Quadrature Detector. Connect these units as shown in Figure 4. In all cases, it is important to terminate all unused ports or performance may be degraded. A data sheet is provided at the end of this manual.

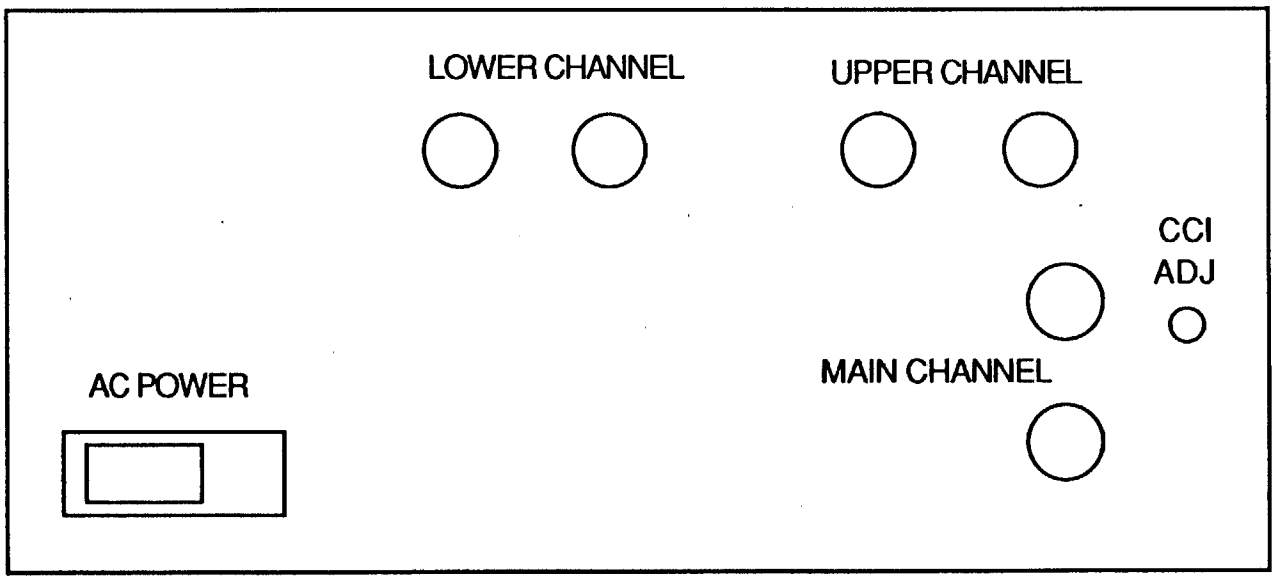


Figure 3 Interference/Noise Generator Rear Panel

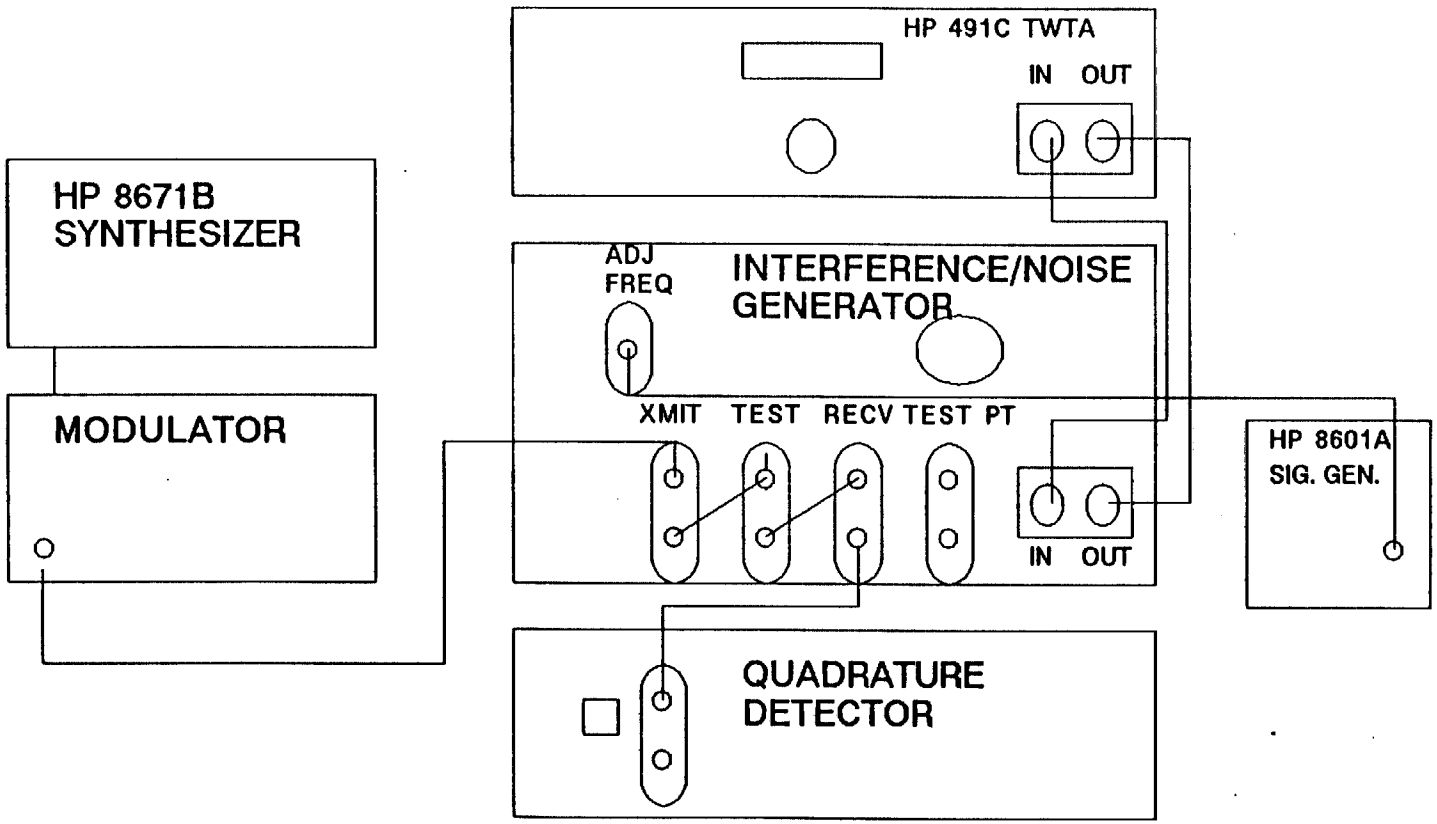


Figure 4 Interference/Noise Generator Initial Set Up

4.2 MAIN CHANNEL SET-UP

View the transmitted signal spectrum on the HP8566 spectrum analyzer. Set the adjacent channel offset LO to at least 112 MHz and at least 3 dBm. Turn the adjacent channel and noise attenuators fully clockwise. Connect the bypass cable to the TWTA ports if the TWTA is not in use. If the TWTA is being used, connect it to the TWTA ports, and add a 30 dB attenuator to its output. Switch it on and wait until the internal relay clicks, at which point the TWTA may be switched to On. Monitor the power level at the Quadrature Detector Cal output. Adjust the Main channel gain and the Quadrature Detector gain until the power meter reads -20 dBm. Zero the meter at that point.

4.3 ADJACENT CHANNEL SET-UP

Connect the spectrum analyzer to one of the Test Pt ports on the Interference/Noise Generator after having performed the main channel set-up. Adjust the Adjacent Channel LO to the desired frequency. Disconnect the Main channel by either switching off the TWTA or removing the bypass cable. View the adjacent channels and adjust the adjacent channel LO power to eliminate any LO feedthrough in the Main channel bandwidth(if any). In the case this cannot be done, add the supplied Mini-circuits filter to the LO. Reconnect the TWTA ports(or turn the TWTA back on) and adjust the adjacent channel attenuators to achieve the desired interfering levels.

4.4 CO-CHANNEL INTERFERENCE SET-UP

The Co-channel interference is accomplished using an internal coupler network. Add this interference by disconnecting the main channel cable on the rear panel connectors. The Co-channel interference level will be shown on the power meter. Adjust this using the rear panel attenuator. Reconnect the main channel cable. Turn the attenuator fully clockwise to eliminate the interference if desired.

4.5 NOISE SET-UP

To add average white Gaussian noise to the signal, connect the power meter to the calibration port on the Quadrature Detector. Turn off the modulator synthesizer LO power. Adjust the noise attenuators until the power meter reads <-60 dBm. If this is not possible, re-zero the power meter. Turn the LO back on and set a reference on the power meter. The absolute level should be -20 dBm. Turn off the LO and read the added noise. Turn the noise vernier fully counterclockwise. Now adjust the screwdriver adjust noise attenuators until the maximum desired added noise is read. Now use the vernier attenuator to make a table of attenuation settings versus added noise power, if desired. Turn the LO back on and use

the table to obtain S/N ratios for BER testing.

4.6 TWTA SATURATION SET-UP

To set the TWTA to its maximum saturated power, first set up the main channel per 4.1.1. Using the ANAL2 port, monitor the input power to the TWTA as well as the output power at ANAL1. Using the main channel attenuator to back off the TWTA, make a table of input to output power. The TWTA can then be set to any level of backoff using this table. When making measurements it will be necessary to adjust the Quadrature Detector gain to return to the desired -20 dBm level(or 0 dB if previously zeroed).

Interference/Noise Generator Data Sheet

Operator_____ Date_____

Para.	Title	Measured Value	Ideal Value
4.3	Adjacent Channel Interference-Upper	_____	20 dB max
4.3	Adjacent Channel Interference-Lower	_____	20 dB max
2.2	Adjacent Channel Frequency Offset	_____	96 MHz
4.4	Co-Channel Interference	_____	-20 dB max

4.5 Added Noise	Attenuator Setting	S/N Ratio
	_____	_____
	_____	_____
	_____	_____
	_____	_____
	_____	_____
	_____	_____
	_____	_____
	_____	_____
	_____	_____
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NASA
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Report Documentation Page

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
NASA CR-185127		

4. Title and Subtitle
ADVANCED TECHNOLOGY SATELLITE DEMODULATOR DEVELOPMENT

5. Report Date
July 1989

6. Performing Organization Code

7. Author(s)
Stephen A. Ames

8. Performing Organization Report No.

10. Work Unit No.
650-60-21

9. Performing Organization Name and Address
Ford Aerospace Corporation
Space Systems Division
3925 Fabian Way
Palo Alto, CA 94303-4697

11. Contract or Grant No.
NAS3-24678

13. Type of Report and Period Covered
Contractor Report Final

12. Sponsoring Agency Name and Address
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
LEWIS RESEARCH CENTER
21000 Brookpark Road
Cleveland, OH 44135-3191

14. Sponsoring Agency Code

15. Supplementary Notes
Project Manager, Mary Jo Shalkhauser, Space Electronics Division, NASA Lewis Research Center

16. Abstract

The report covers the design, development, and testing of a proof-of-concept (POC) 8PSK TDMA modem and codec for 200 Mbps data coded with a rate 5/6 set of block codes and transmitted at 80 M symbols/s. Design goals were to achieve bandwidth efficiency of 2 bits/sec/Hz, implementation loss of less than 2 dB, ACI and CCI loss of less than 1 dB in 20 dB interference, and a preamble of less than 100 data intervals (500 ns). A mostly digital POC model was built and tested which yielded 1.8 bits/sec/Hz bandwidth efficiency with a 4.5 dB implementation loss. The design concept was proven and a miniaturized next stage project was recommended. The digital portion of the satellite engineering model demodulator could be built on two ECL gate arrays with commensurate miniaturization feasible on the analog portions. The company funded codec work is reported in a separate report.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
Demodulator Bandwidth Efficient 8-PSK TDMA Satellite Communications	Unclassified - Publicly Available Subject Category 32

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No of pages	22. Price*
Unclassified	Unclassified	216	A10

NASA FORM 1626 OCT 86

*For sale by the National Technical Information Service, Springfield, Virginia 22161