DISTRIBUTED DIGITAL SIGNAL PROCESSORS FOR MULTI-BODY STRUCTURES

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Interim Report

by

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ABSTRACT

The objectives of this project are to investigate several digital filter designs which may be used to process sensor data from large space structures and to design digital hardware to implement the distributed signal processing architecture. Several experimental test articles are available at NASA Langley Research Center to evaluate these designs. In this interim report, a summary of some of the digital filter designs is presented, an evaluation of their characteristics relative to control design is discussed and candidate hardware micro-controller/microcomputer components are given. Future activities include software evaluation of the digital filter designs and actual hardware implementation of some of the signal processor algorithms on an experimental testbed at NASA Langley.

I. INTRODUCTION

With large dimensional systems such as Space Station, distributed control is a viable approach in reorientation maneuvers with vibration suppression requirements. In a distributed control architecture, the system is partitioned into subsystems (by modes or by state dynamics) such that local controllers may perform the compensation; a supervisor may be employed to handle global information. With the large amount of data required, particularly sensor and actuator

information, signal processing at the local level is required. The purpose of this interim report is to discuss distributed signal processing, particularly filtering for multi-body structures.

Two experimental testbeds, the evoluting phase zero model and the 10-bay flexible structure are candidates to tests the proposed algorithms discussed in this interim report; this is the subject of the continual work to be done in the second part of this effort. This is discussed in more detail in Section IV.

The initial model of the plant considers the most significant frequencies between the range of zero to 30 Hz. The 10-bay structure is predicted to have modal shapes below 10Hz while the evoluting phase zero has a significant frequency range below 30Hz. A NASA Langley researcher is conducting work in analog filter design (see Figures 1 and 2) on the evoluting phase zero model - a 48-mode structure with noise. In Figures 1 and 2, the cut-off frequency for two Butterworth filter design is 15Hz with a frequency sampling period of 0.01 Hz. This on-going research effort

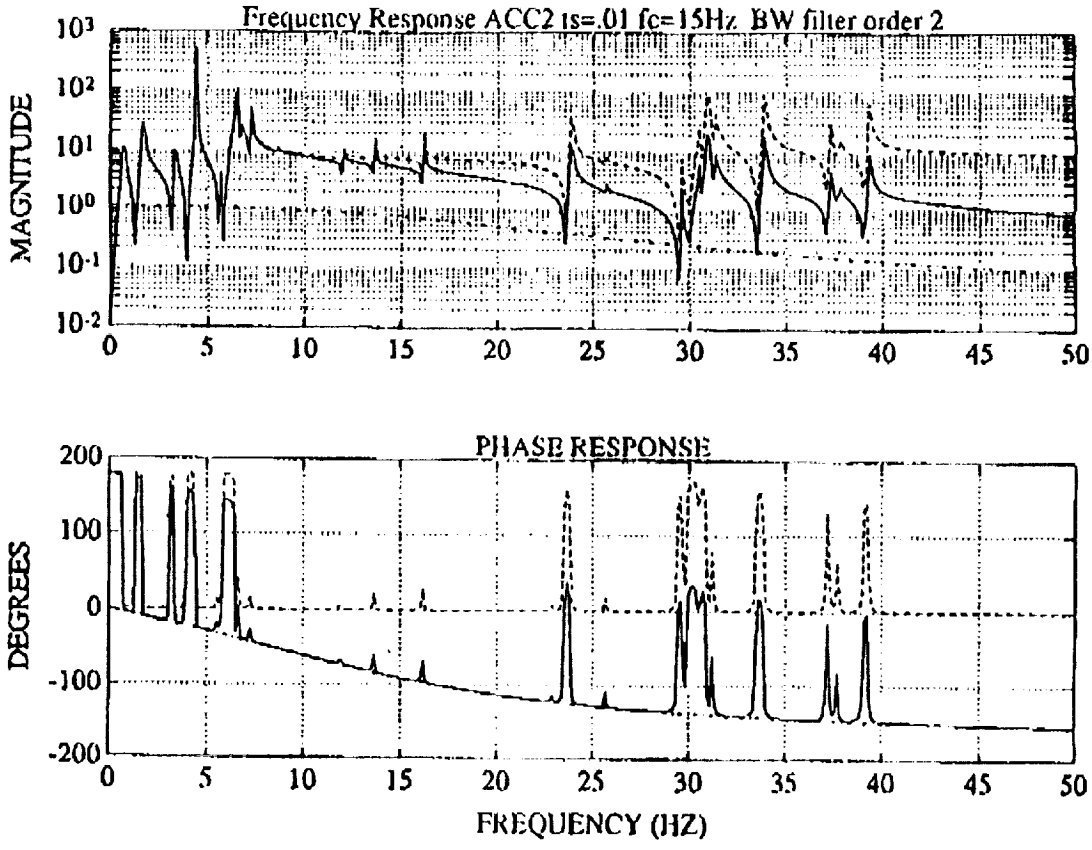

Figure 1: Evolution phase zero frequency response with Butterworth filter of order 2

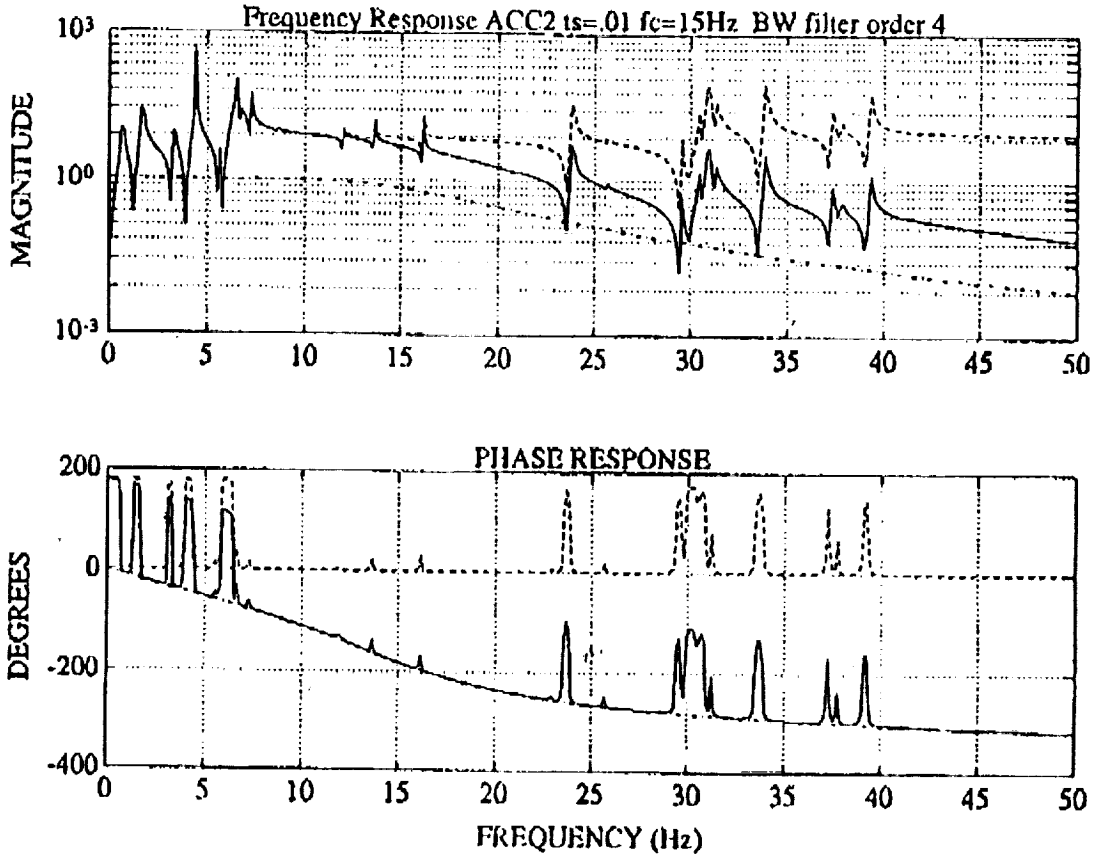

Figure 2: Evolution phase zero frequency response with Butterworth filter of order 4

concentrates on digital filter design. Section II discusses some design criteria while Section III presents some hardware candidates for digital filter implementation.

II. DIGITAL FILTER DESIGNS

The design specifications are selected to conform with the test articles under investigation. Based upon discussion with NASA personnel, two analog filter architectures are considered: a low pass filter and a band pass filter (Figure 3). Pertinent specifications include f_c: cut-off frequency (in Hz) and f_s: stop-band frequency (in Hz).

The frequency response of a filter is usually divided into the passband (the frequency range in which the signal is transmitted through the filter) and the stopband (the frequency range in which the signal is rejected by the filter). The cut-off frequency is that frequency which divides the

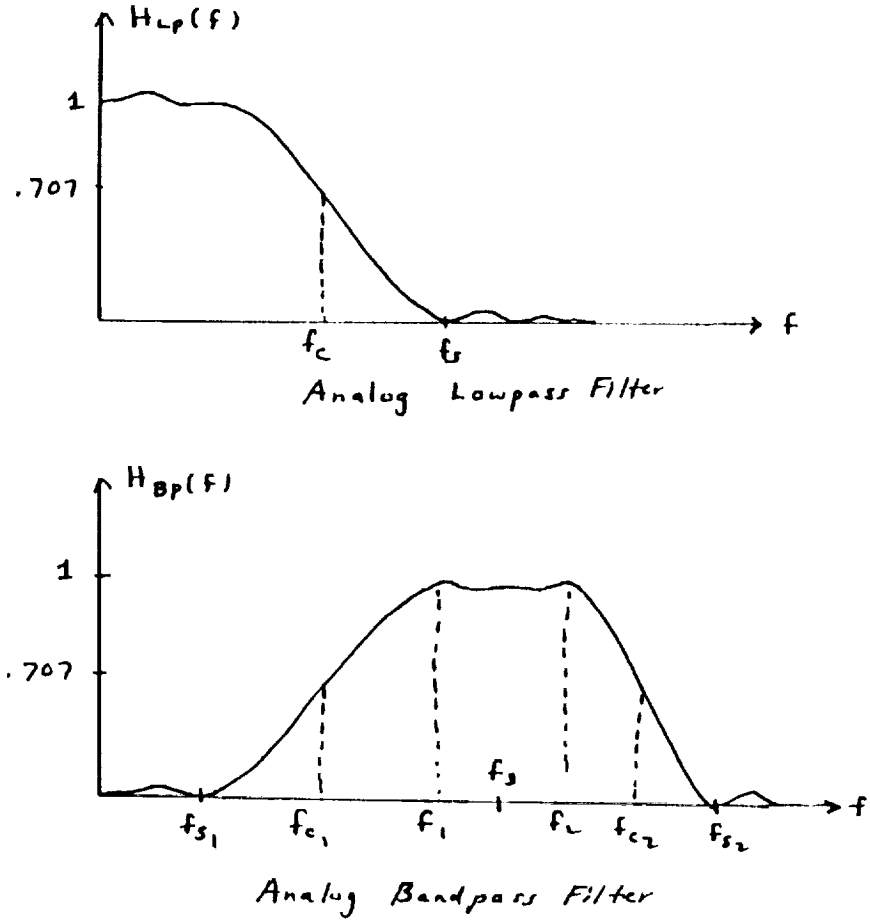

Figure 3: Frequency Response of Filters under Study

frequency response magnitude of the transfer function from the passband to the stopband range. Practical filters have a transition band between these regions. The stopband frequency then is that frequency separating the transition band from the stopband and the cut-off frequency is that frequency separating the passband from the transition band.

Given a low pass filter design, a band pass filter design may be constructed using

$$\omega_{Lp} = \omega_{Bp} + \frac{(2\pi f_2)^2}{\omega_{Bp}} \qquad f_3 = \sqrt{f_1 f_2}$$

where ω is the independent frequency variable in the appropriate filter transfer function.

Digital filter designs may be categorized into analog invariance (usually Infinite Impulse Response architecture) or direct digital (usually Finite Impulse Response architecture). In selecting one approach over another, various characteristics may be evaluated as in Table 1. Because of the real-time requirements, IIR filters have been selected in this study.

Table 1: Comparison of FIR and IIR filters

	Characteristic	IIR	FIR
1.	Data length of impulse response stored	Large	Moderate
2.	Time delays (and multipliers) required	Moderate	Large
3.	Phase characteristics	May be nonlinear	Linear
4.	Design Procedure	Simple to moderate	Moderate
5.	Stability Issue	Analog filter must stable	Always stable
6.	Sensitivity to quantization errors	May be sensitive	Less sensitive

Several IIR designs have been suggested and classical techniques are discussed in [1-4] for example. These techniques include bilinear-z approximation, impulse-invariance and covariance-invariance, which are the three algorithms selected for the initial phase of this study (the first two methods are presented in this report).

For analog invariance techniques, an analog filter must first be designed; then a digital filter is developed to follow the analog response (time or frequency). In selecting a filter structure, one must consider the application. In this study, the filter is one component of processing between sensor and actuator, for a multi-body structure. A table of some of the characteristics of filters which enhance the control processing is given in Table 2.

Three analog filter designs were selected. These are:

1. Butterworth Filter - this filter has the property that its magnitude squared is maximally flat (at the d.c., all derivatives are zero). For normalized unity d.c. magnitude, its cut-off frequency is at a frequency response magnitude of 0.707. Further, as its order approaches infinity, a Butterworth filter approaches an ideal filter.
2. Chebyshev Filter - this filter has ripples in the passband or stopband but generally has a sharper cut-off, i.e., narrower transition band than the Butterworth filter, for the same order.
3. Elliptic Filter - this filter has ripples in both the passband and stop, but has an even sharper cut-off than the Chebyshev filter.

The first two types of filters were studied up to this point and the third filter is currently under investigation.

Table 2: Design Considerations for Filter Selection Using the Filter as a Pre-processor for Control

1. Minimal time delays for real time implementation
2. Implementation requirements (hardware, software, firmware)
3. Magnitude and phase characteristics
4. Specialization vs. flexibility of design
5. Sampling rate constraints
6. Memory requirements (finite-word length)
7. Reliability
8. Control of precision
9. Commonality of individual filter components and well as commonality between filter and control hardware
10. Simplicity of design

All these analog filters have phase distortion which is directly linked to time delays. Hence an all-pass filter needs to be designed to reduce this distortion. This all-pass filter is used in with the analog filter and essentially gives unity magnitude in its frequency response. First order and second-order all-pass filters were designed in this effort.

Initial results are as follows: For the low-pass filter designs, we found

1. Butterworth 2-nd order low-pass using bilinear-z transformation

$$H(z) = \frac{5.872 \times 10^{-2} (1 + 2z^{-1} + z^{-2})}{1 - 1.207z^{-1} + 0.442z^{-2}}$$

2. Chebyshev 3-rd order low-pass using bilinear-z transformation (1.0 db ripple in stopband)

$$H(z) = \frac{6.223 \times 10^{-2} (1 + 2z^{-1} + z^{-2})}{1 - 1.266z^{-1} + 0.5411z^{-2}}$$

3. Butterworth 2-nd order low-pass using impulse invariance

$$H(z) = \frac{1.19448 \times 15^{8} z^{-1}}{1 - 1.02656z^{-1} + 0.26372z^{-2}}$$

4. Chebyshev 3-rd order low-pass using impulse invariance

$$H(z) = \frac{8.7751 \times 10^{-5} x^{-1}}{1 - 1.19168z^{-1} + 0.355382z^{-2}}$$

These designs are based upon the specification of: cut-off frequency f_c = 15 Hz; stop-band frequency f_s = 50 Hz, sampling rate of 1000 Hz. Results of the frequency responses are shown in Figures 4-7.

Further two bandpass filters are currently being designed based upon analog Butterworth and Chebyshev filters. In particular , we have

1. Butterworth 5-th order bandpass using bilinear-z transformation

$$G(p) = \frac{1}{1 + 3.236p + 5.236p^2 + 5.236p^3 + 3.236p^4 + p^5}$$

where the digital filter is:

$$H(z) = G(p) \text{ with } p = 65.129\left[\frac{z^2 - 2z + 1}{z^2 - 1}\right]$$

2. Chebyshev 5-th order band pass with bilinear-z transformation (1.0 db ripple in stopband)

$$G(p) = \frac{1}{0.1228 + 0.5805p + 0.97439p^2 + 1.6888p^3 + 0.93682p^4 + p^5}$$

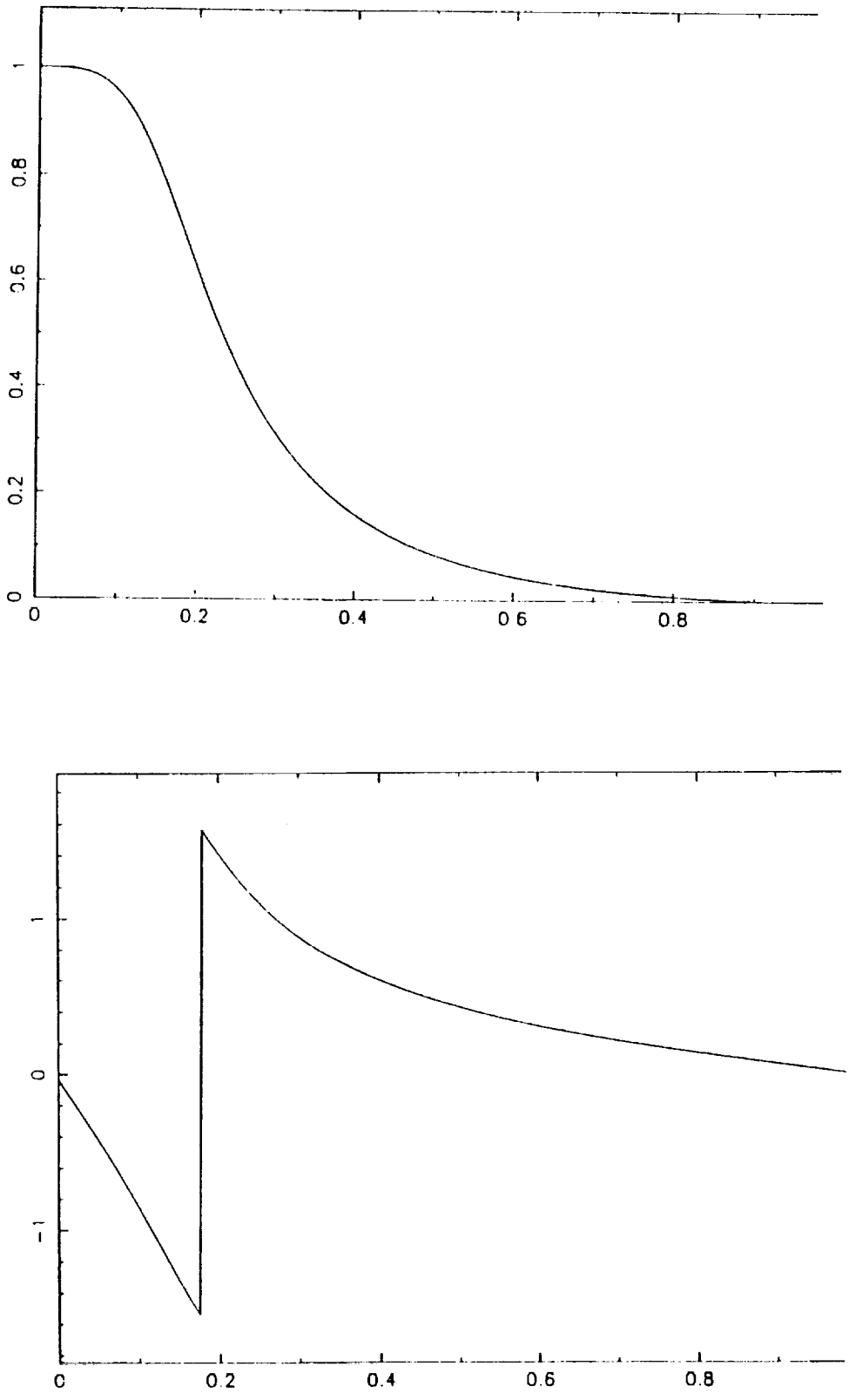

Figure 4: Butterworth 2nd-order Lowpass Frequency Response Using Bilinear-z Transformation

Note: All frequency responses show magnitude and phase plots with a normalized fold-over frequency. Phase plots exhibit a modular 2 discontinuity, characteristics of the arctangent function.

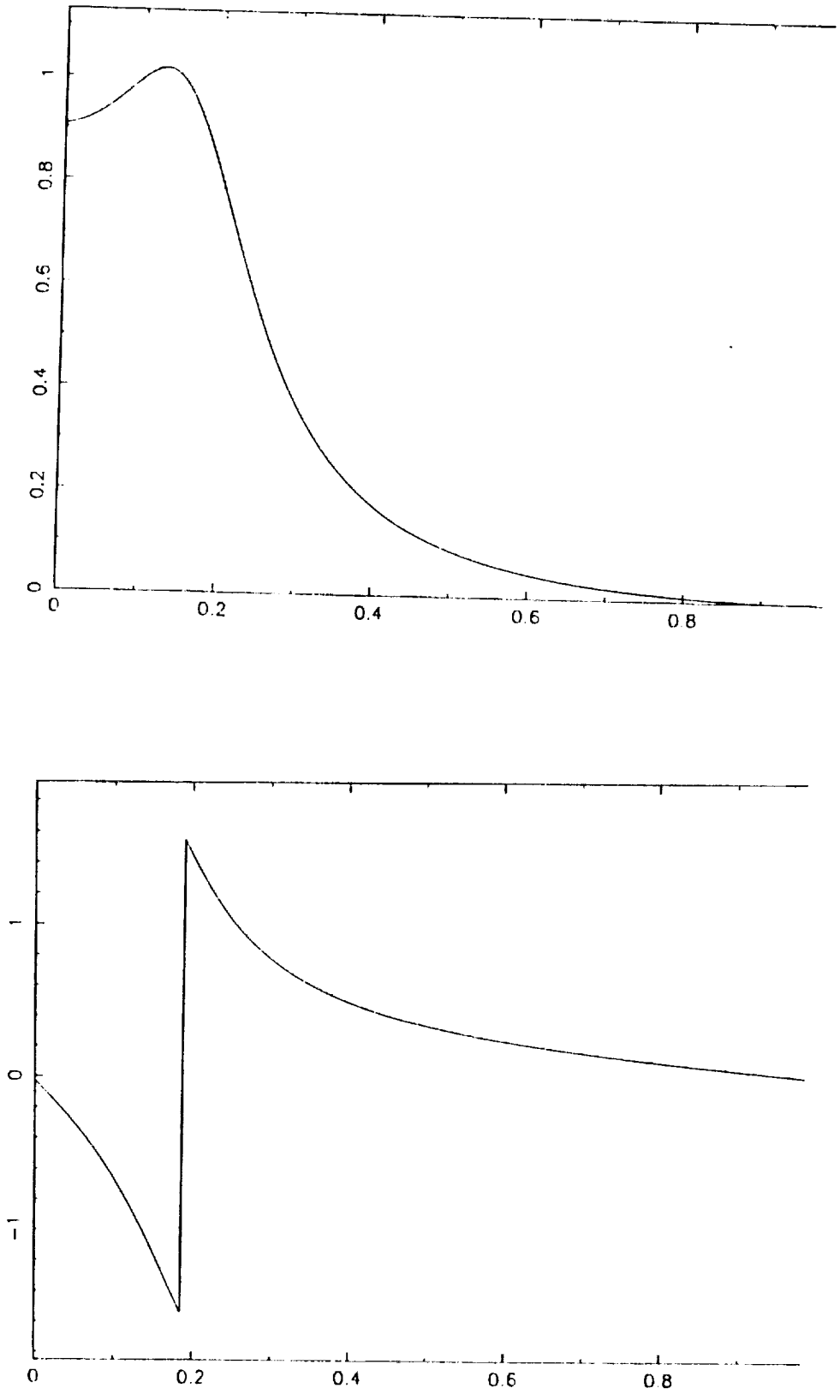

Figure 5: Chebyshev 3rd-order Lowpass Frequency Response Using Bilinear-z transformation

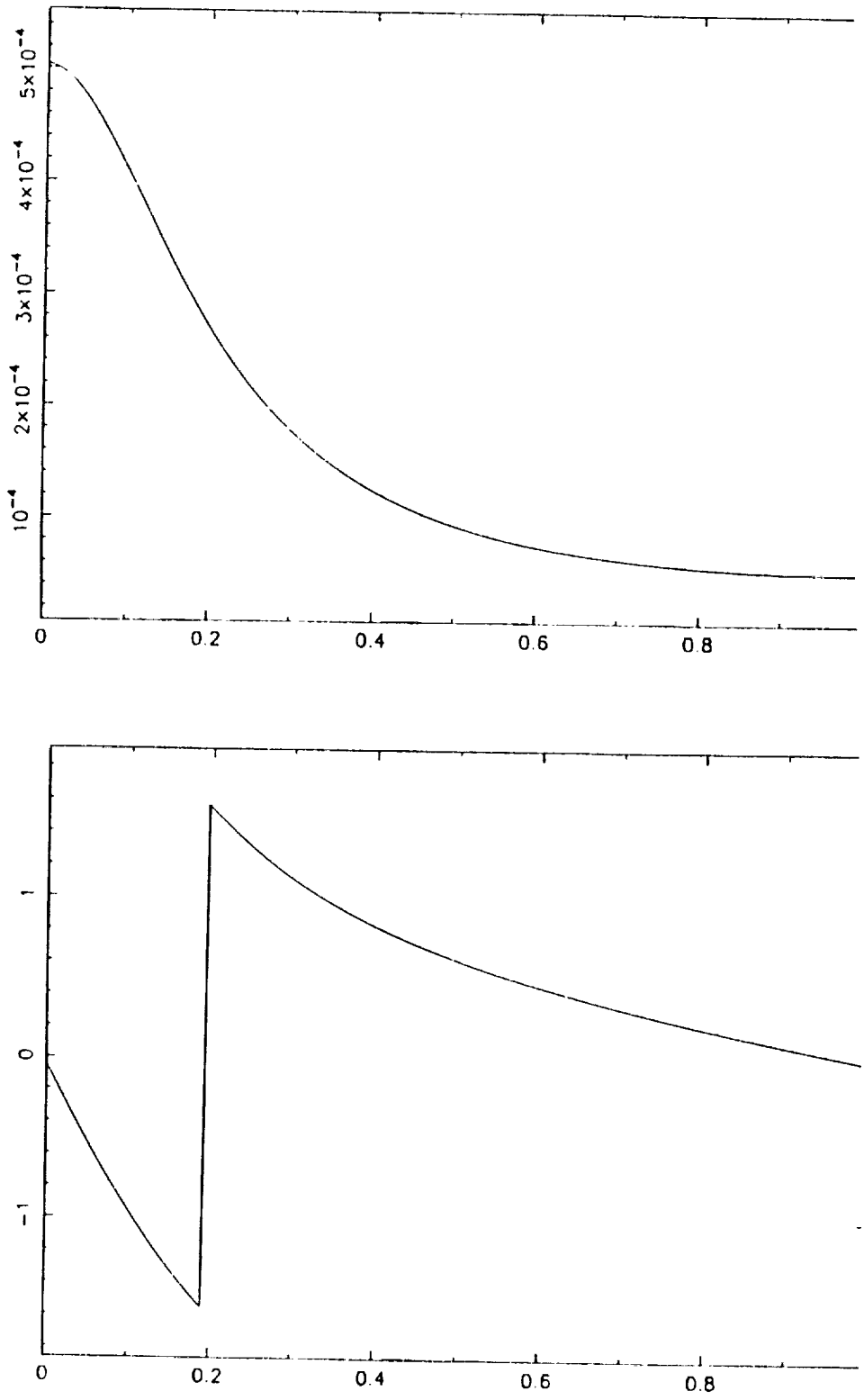

Figure 6: Butterworth 2nd-order Lowpass Frequency Response Using Impulse Invariance

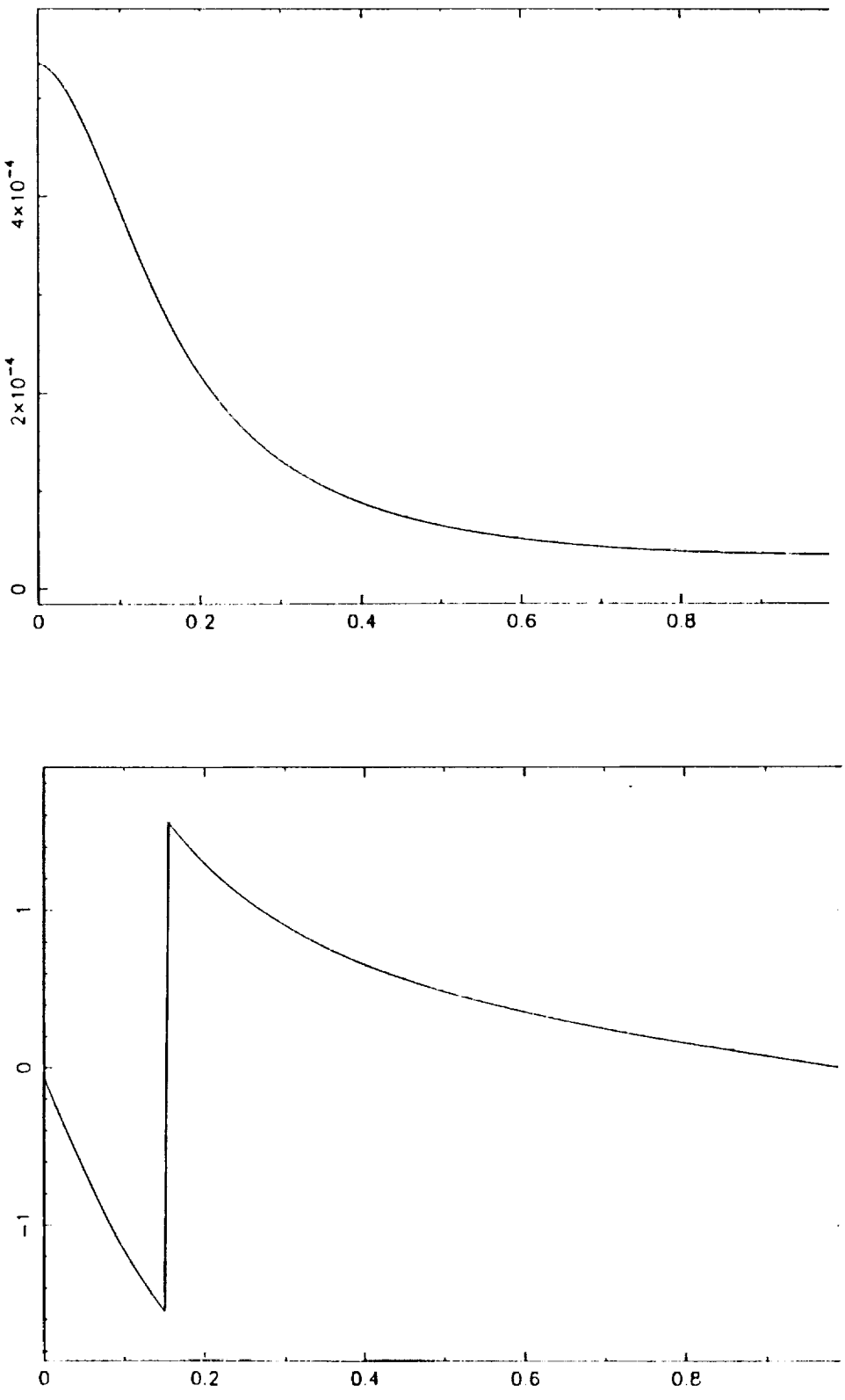

Figure 7: Chebyshev 3rd-order Lowpass Frequency Response Using Impulse Invariance

with the same H(z) substitution for p as in (1). The specifications for these designs are: $f_1 = 1$ Hz; $f_3 = 29$ Hz; T = 0.01 sec; $f_{s_1} = 0.5$ Hz; $f_{s_3} = 29.5$ Hz. Frequency response curves are still being generated and investigated for these bandpass designs.

Note that from these frequency responses, there are phase distortions which produce more than just a time delay in the output. These nonlinear effects need be corrected.

Hence two all-pass filters have been designed. The purpose of an all-pass filter is to correct the phase distortion of the low or band pass filter, yet maintain the magnitude frequency response characteristics of these filters. These all-pass filters are characterized by the following.

1. All pass first-order filter using bilinear-z transformation $T(s) = \frac{s - a}{s + a}$. If we choose $a = \omega_c = 30\pi$ rad/sec and T = 0.01 sec, then

$$H(z) = \frac{0.1266 - z^{-1}}{1 - 0.1266z^{-1}}$$

2. The pass second-order filter using bilinear-z transformation

$$T(s) = k\frac{s^2 - bs + a}{s^2 + bs + a}.$$

where we decreased the sampling period to T = 0.001 sec. Following [5], for a simple low pass filter, we can initially select k, b and a as:

$$T(s) = \frac{s^2 - 94.247s + 5071.99}{s^2 + 94.247s + 5071.99}$$

when the cut-off frequency is 15 Hz. Then

$$H(z) = \frac{0.882 + 1.8744z^{-1} + z^{-2}}{1 + 1.8744z^{-1} + 0.882z^{-2}}$$

The frequency response for these all-pass filters are shown in Figure 8. Note that these filters would be in the cascade with the low pass or band pass filter, as shown in Figure 9. Note also that the impulse invariance method can not be employed here as T(s) contains the same number of zeros as poles.

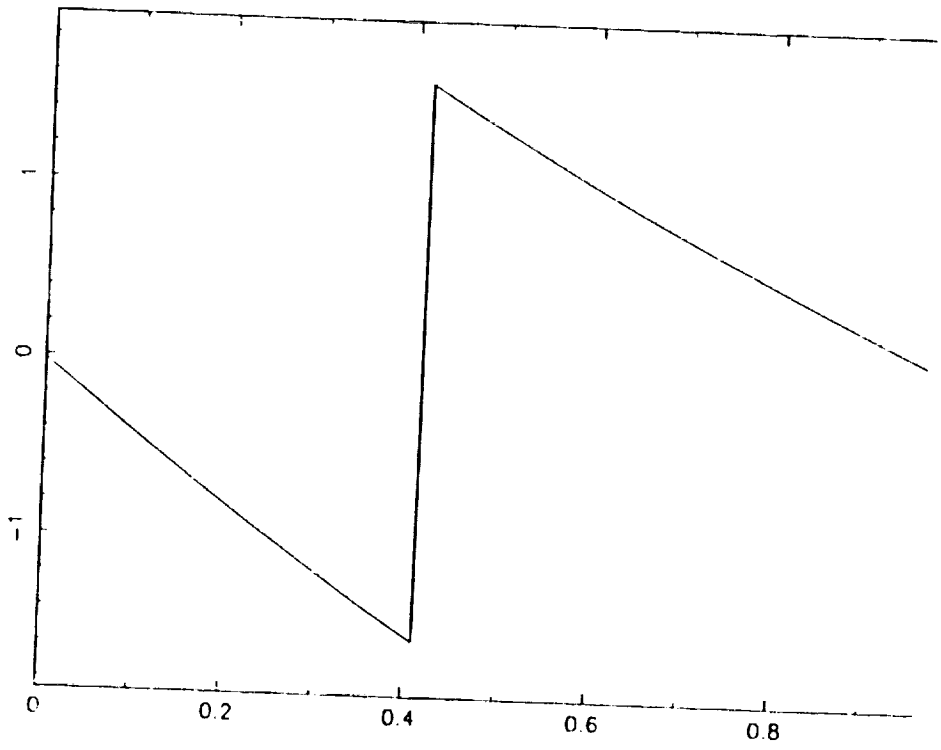

Figure 8a: First-order All-pass Filter Phase Frequency Response Using Bilinear-z Transformation

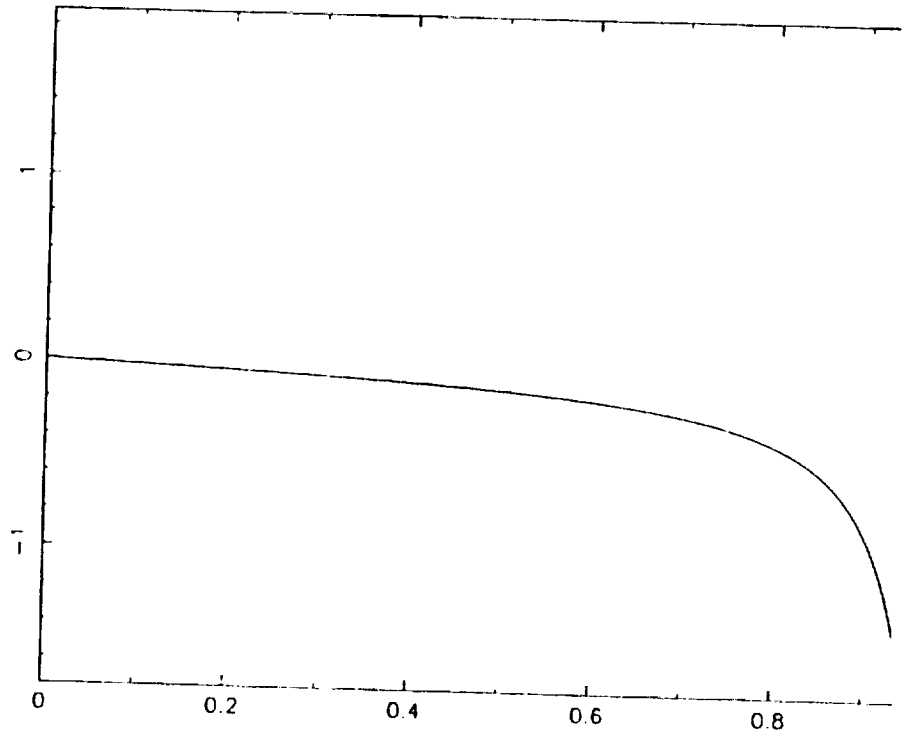

Figure 8b: Second-order All-pass Filter Phase Frequency Response Using Bilinear-z Transformation

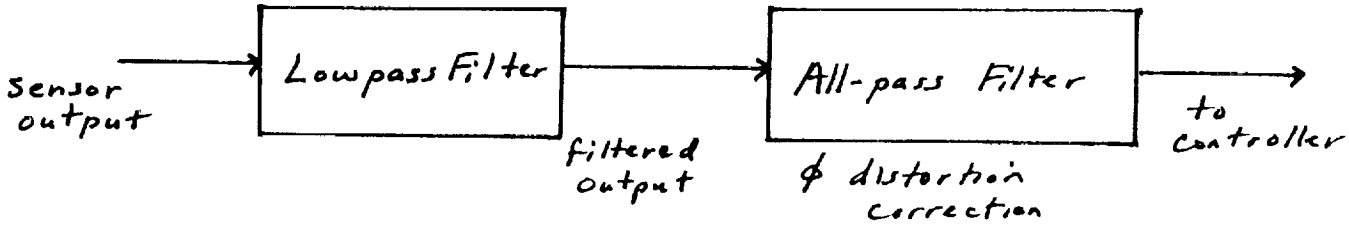

Figure 9: Block Diagram of Filter Structure

All of these filters are currently being evaluated in terms of the criteria of Table 2.

III. CANDIDATE HARDWARE IMPLEMENTATION

These filter designs may be implemented on a computer or using specialized sequential logic (registers and gains). In this study, three microcontroller chips are being investigated. A microcontroller architecture is selected over other configurations because the microcontroller system offers the best of two worlds: a flexible architecture which can be changed without hardware substitution yet a system with little overhead in the system development (design, testing and debugging) when compared to other larger microcomputer configurations. By having less overhead, the microcontroller provides many functions in a simpler form, thus processing a more reliable structure. Further the microcontroller can be used in a real-time environment and as one component of a distributed configuration.

The basic microcontroller is shown in Figure 10 [6,7]

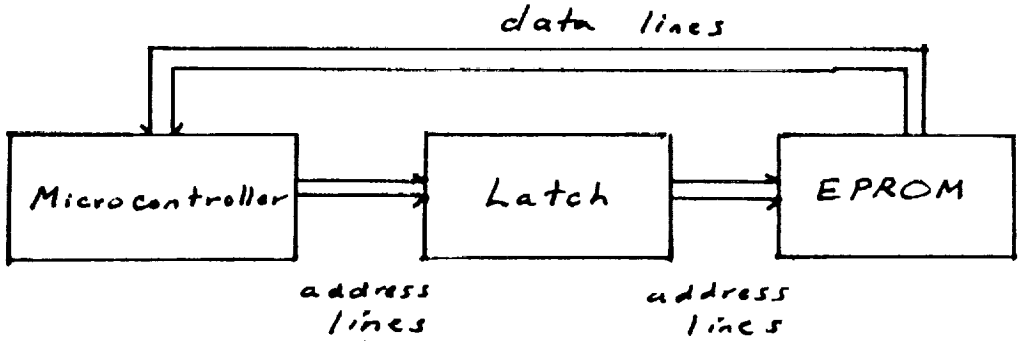

Figure 10: Microcontroller Structure

The microcontroller chip sends address requests to the EPROM (erasable programmable read-only memory) and the EPROM sends data back to the microcontroller. A latch is used to separate stored line sequencing between data and address. A RAM (random access memory) chip may also be attached to the EPROM as additional memory .

One can add Analog-to-digital and Digital-to-analog ports to connect to a personal computer for development. Then a higher level language such as PASCAL or BASIC may be used to program the microcontroller.

For this study, all interfaces are TTL compatible. The latch may be chosen as a 74LS573 and the EPROM can be a standard 2764. For the microcontroller, the following are being studied:

1. The Intel 8031 or more advanced MSC-96. The MSC-96 is a 16-bit microcontroller with 8-bit or 16-bit external bus, five 8-bit I/0 ports, 8K byte on-chip ROM/EPROM, on-chip A/D and multiply/divide in hardware. With a 12 MHz input frequency, this chip provides a multiplexer, interrupts and a 16-bit watchdog timer.
2. The Texas Instrument TM 990 - This is a classical processor chip, available for over 10 years. It has RAM and ROM on-chip, a 2MH clock, a 16-bit I/O port and features the TMS 9980A microprocessor as the controller.
3. The BASICON MC-2i programmable microcontroller - This is one of a family of microcontrollers and is CMOS technology. It has 8K-byte RAM, 36 I/O lines, an 11MHz clock and up to 32K-byte ROM. The 80C31 processor is the main driver. This chip runs under MS-DOS and is currently the leading controller for this project.

IV. FUTURE ACTIVITIES

For the second half of this research effort, the rest of the digital filter designs will be completed (the elliptical filters and the covariance invariance techniques). Further the bandpass filter frequency responses will be generated.

The author will be working with Nancy Nimmo of NASA LaRC Spacecraft Structures Branch to generate magnitude and phase plots in a standard format. Further a comparison of the

digital designs developed by the P.I. with analog designs developed by NASA LaRC will be performed.

Finally a microcontroller will be selected and some of the candidate digital filters will be implemented and tested on an experimental test article, either the 10-bay structure or the evolution phase zero model. Results will be conducted according to Table 2 and possible future activities will be suggested.

IV. REFERENCES

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