National Aeronautics and
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September 26, 1990

TO: NASA Headquarters
Attention: Office of Assistant General
Counsel for Patent Matters

FROM: Administration and Management Directorate
Office of Patent Counsel

SUBJECT: Patent Application for STAR GSC 13,265-1

Enclosed are two copies of the patent application, two copies of the awards digest and drawings relative to the subject case.

Filing Date 8/31/90

Serial Number 07/575,694

Print Fig 2A

D. Saresi

Enclosures:
Patent Application 2
Awards Digest & Drawings 2

(NASA-Case-GSC-13265-1) METHOD OF FABRICATING GERMANIUM AND GALLIUM ARSENIDE DEVICES Patent Application (NASA) 10 p

N91-14066

Unclas
G3/76 0320462

AWARDS DIGEST

GSC 13,265-1

METHOD OF FABRICATING GERMANIUM AND GALLIUM ARSENIDE DEVICES

As shown in Figs. 1A-1E, there is disclosed a method of semiconductor diode fabrication which relies on the epitaxial growth of a precisely doped thickness layer of gallium arsenide or germanium on a semi-insulating or intrinsic substrate, respectively, of gallium arsenide or germanium by either molecular beam epitaxy (MBE) or by metal-organic chemical vapor deposition (MOCVD) and which involves: depositing a layer of doped or undoped silicon dioxide 14 on a germanium or gallium arsenide wafer or substrate 10, selectively removing the silicon dioxide layer 14 to define one or more surface regions 16 for a device to be fabricated thereon, growing a matched epitaxial layer 18 of doped germanium or gallium arsenide of an appropriate thickness using MBE or MOCVD techniques on both the silicon dioxide layer and the defined one or more regions; and thereafter etching the silicon dioxide 14 and the epitaxial material 18 on top of the silicon dioxide to leave a matched epitaxial layer 22 of germanium or gallium arsenide on the germanium or gallium arsenide substrate, respectively, and upon which a field effect device can thereafter be formed as shown in Figs. 2A and 2B

Novelty is believed to lie in the concept of a relatively simple method of using the intrinsic resistivity of the bulk material for isolation and reduction in leakage paths between neighboring devices formed on a germanium or gallium arsenide substrate.

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Employer: National Aeronautics and Space Administration

GSC-13265-1
Ser. # 07/515,694
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Print fig 2A

GSC-13265-1
Ser # 07/575,694
Filed Aug. 31, 1990
Print Fig 2A

METHOD OF FABRICATING GERMANIUM AND GALLIUM ARSENIDE DEVICES

Origin of the Invention

The invention described herein was made by an employee of the United States Government and may be manufactured and used by or for the Government for governmental purposes without the payment of any royalties thereon or therefor.

Background of the Invention

This invention relates generally to the fabrication of semiconductor devices and more particularly to the fabrication of germanium and gallium arsenide devices such as junction field effect transistors and metal-semiconductor field effect transistors.

In known prior art methods for fabricating integrated circuit structures, particularly those with germanium devices, such devices resulted in being inherently leaky or resistive at room temperature. As a result, one had to resort to building isolation devices into the substrate or into an epilayer covering the structure. Previous methods relied on junction isolation, that is, introducing an impurity of opposite polarity such as p+ into a n- layer and then reverse biasing the junction in order to obtain isolation. However, this has been found to be ineffective in gallium arsenide (GaAs) and germanium devices. Prior art techniques were also known which would etch out islands out of the epilayer but the etching process is not self limiting, since both the epilayer and substrate are equally susceptible to the etchant utilized. Consequently, top down etching has been found to be very imprecise and as a result can require one or more additional fabrication steps.

It is an object of the present invention, therefore, to provide an improvement in methods for fabricating

semiconductor devices.

It is another object of the invention to provide improvement in the method of fabricating germanium and gallium arsenide type devices.

It is a further object of the invention to provide a method for providing device isolation in gallium arsenide and germanium devices while providing a controlled method of forming one or more active channel regions therein.

It is still another object of the invention to provide an improved method for fabricating gallium arsenide and germanium devices utilizing the intrinsic resistivity of the bulk material itself for providing isolation between neighboring devices.

Summary

Briefly, the foregoing objects and advantages are provided by a method which relies on the epitaxial growth of a precisely doped thickness layer of gallium arsenide or germanium on a semi-insulating or intrinsic substrate, respectively, of gallium arsenide or germanium by either molecular beam epitaxy (MBE) or by metal-organic chemical vapor deposition (MOCVD) and which comprises the steps of: depositing a layer of doped or undoped silicon dioxide on a germanium or gallium arsenide wafer or substrate; selectively removing the silicon dioxide layer to define one or more surface regions for a device to be fabricated thereon; growing a matched epitaxial layer of doped germanium or gallium arsenide of an appropriate thickness using MBE or MOCVD techniques on both the silicon dioxide layer and the defined one or more regions; and thereafter etching the silicon dioxide and the epitaxial material on top of the silicon dioxide to leave a matched epitaxial layer of germanium or gallium arsenide on the germanium or gallium arsenide substrate, respectively, and upon which a field

effect device can thereafter be formed in a well known manner. It is of particular significance that a non-crystalline compatible material such as silicon dioxide is first deposited on the substrate.

Brief Description of the Drawings

The following description will be more readily understood when taken in conjunction with the accompanying drawings in which:

Figures 1A-1E are schematic cross sections of a device in accordance with this invention depicting its preferred method of fabrication; and

Figures 2A and 2B are schematic cross sections further illustrative of the fabrication of a field effect transistor from the device shown in Figure 1E.

Detailed Description of the Invention

Referring now to the drawings and more particularly to Figure 1A, reference numeral 10 denotes a semi-insulating or intrinsic wafer of gallium arsenide (GaAs) or germanium (Ge) having a nominal thickness in the order of 15 mils (millimeters). Next, as shown in Figure 1B, amorphous, i.e. non-crystalline compatible material is deposited on the surface 12 of the wafer 10 which acts as a substrate for a device to be formed thereon. The amorphous material comprises a layer 14 of heavily doped silicon dioxide (SiO_2) having a thickness ranging between 1000Å and 10,000Å. When desirable, however, undoped SiO_2 can be used.

This is followed by selectively removing a portion(s) of the SiO_2 layer 14 to define one or more surface regions 16 as shown in Figure 1C and which is thereafter followed by growing a layer 18 of material which will match the substrate 10 and more particularly an epilayer of Ge is grown on a Ge substrate while an epilayer of GaAs is grown on a substrate of GaAs. This epitaxial growth is carried out by

conventional molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD). The layer 18 is typically formed to a thickness ranging between 1000Å and 10,000Å depending on the exact device to be fabricated at the surface region 16 and is grown with a precise impurity doping concentration, typically $10^{15}/cm^3$. While either n type or p type impurities could be utilized, an n type layer 18 is grown as shown in Figure 1D. With such a structure, the usual boundary interface 20 disappears. This additionally results in forming a mismatch to the adjoining SiO_2 regions 14.

Next as shown in Figure 1E, the structure shown in Figure 1D is subjected to an appropriate etchant such as HF to remove the portions 14 of SiO_2 and the deposited material 18 on the top of the SiO_2 portions, leaving islands or mesas 22 of epitaxial grown layers which can be further processed as shown in Figure 2.

Referring now to Figures 2A and 2B, the substrate 10 and mesa 22 of matching material, either germanium or gallium arsenide, is subjected to conventional fabrication steps of depositing another layer 24 of the SiO_2 forming a pattern thereon and etching openings 26 therein for defining drain and source regions of a field effect transistor, for example, through which arsenic or silicon, depending upon whether Ge or GaAs is utilized, to implant n- impurities in the mesa 22 for forming a n- channel region in the layer 18. This is followed by masking and defining drain and source regions 28 and 30 followed by implantation of n+ impurities. This is followed by depositing and patterning a layer of metallization on the surface 32 for defining metallic electrodes 34 for the drain (D), gate (G) and source (S) regions as shown.

Thus what has been shown and described is an improved

method of fabricating semiconductor devices such as field effect devices having improved isolation between adjacent devices while providing a controlled method of forming the active channel region. The lift off technique described selectively removes only SiO_2 while preserving the underlying bulk material so that the intrinsic resistivity of the bulk material is used for isolation and reduction in leakage paths between adjacent devices. Further, the number of masking steps required to fabricate devices is reduced.

Having thus shown and described what is at present considered to be the preferred method of the subject invention, it should be noted that the same has been made by way of illustration and not limitation. Accordingly, all modifications, alterations and changes coming within the spirit and scope of the invention as set forth in the appended claims are herein meant to be included.

METHOD OF FABRICATING GERMANIUM AND GALLIUM ARSENIDE DEVICES

Abstract of the Disclosure

A method of semiconductor diode fabrication which relies on the epitaxial growth of a precisely doped thickness layer of gallium arsenide or germanium on a semi-insulating or intrinsic substrate, respectively, of gallium arsenide or germanium by either molecular beam epitaxy (MBE) or by metal-organic chemical vapor deposition (MOCVD) and which involves: depositing a layer of doped or undoped silicon dioxide on a germanium or gallium arsenide wafer or substrate, selectively removing the silicon dioxide layer to define one or more surface regions for a device to be fabricated thereon, growing a matched epitaxial layer of doped germanium or gallium arsenide of an appropriate thickness using MBE or MOCVD techniques on both the silicon dioxide layer and the defined one or more regions; and thereafter etching the silicon dioxide and the epitaxial material on top of the silicon dioxide to leave a matched epitaxial layer of germanium or gallium arsenide on the germanium or gallium arsenide substrate, respectively, and upon which a field effect device can thereafter be formed.

FIG. 1A

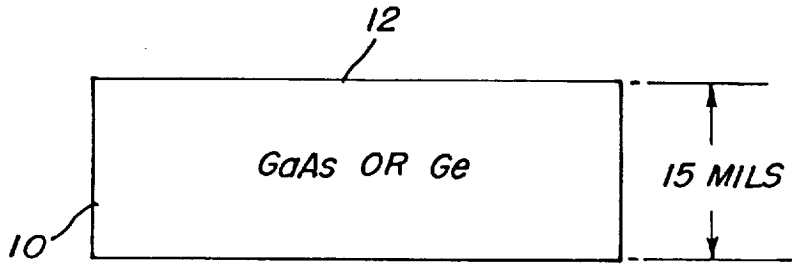


FIG. 1B

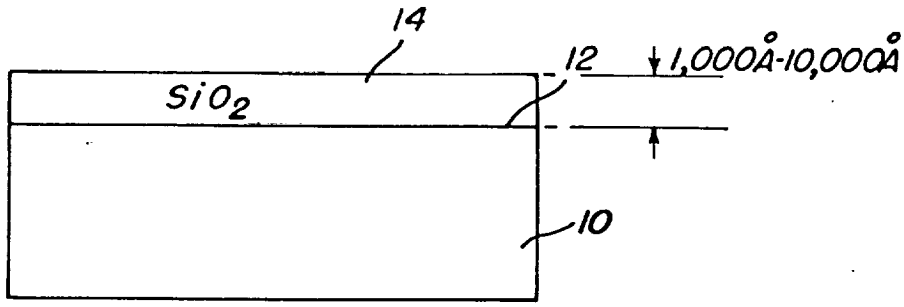


FIG. 1C

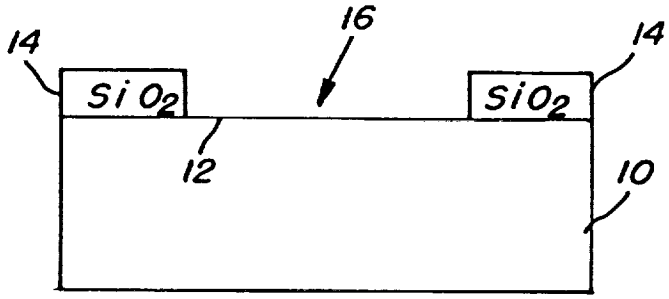


FIG. 1D

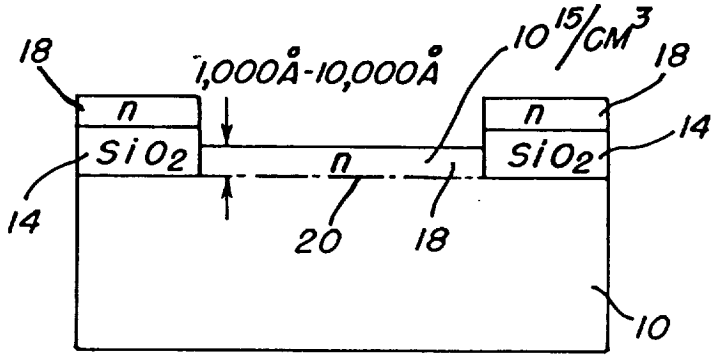
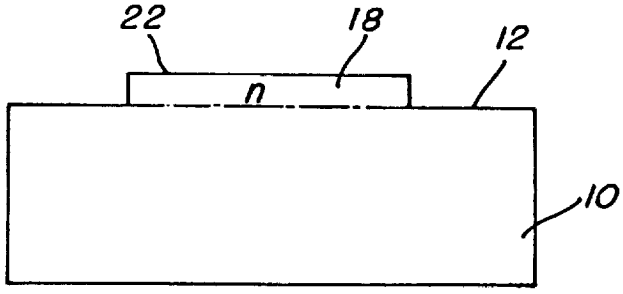


FIG. 1E



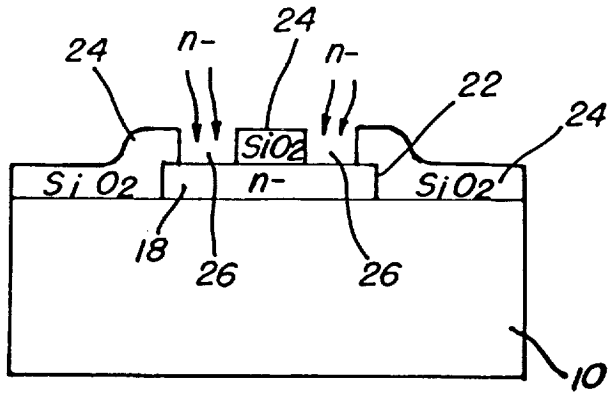

24
n-
24
n-
22
24
SiO2
Si O2
n-
SiO2
18
26
26
10

FIG. 2A

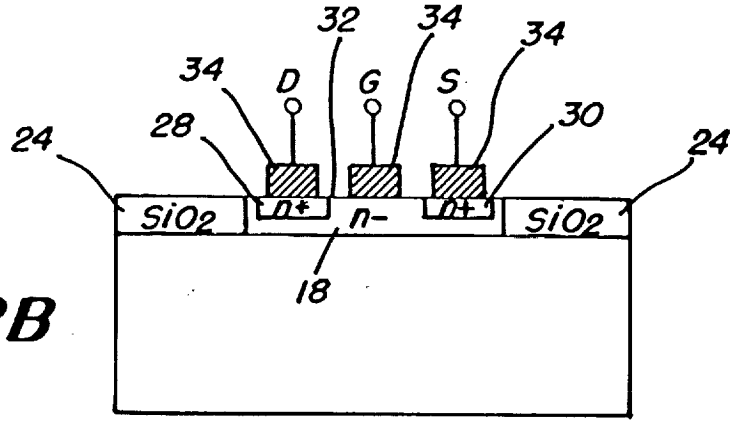

32
34
34
34
D
G
S
28
30
24
24
SiO2
n+
n-
n+
SiO2
18

FIG. 2B