ISSUES AND DIRECTIONS IN IR DETECTOR READOUT ELECTRONICS

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Abstract

An introduction to the major issues encountered in the read out of imaging detector arrays in the infrared will be presented. These include circuit issues such as multiplexing, buffering, and noise, as well as materials issues.

Future directions in infrared readout electronics will also be discussed. These include on-chip signal processing and advanced hybridization schemes. Finally, recent work at Columbia on 2DEG-CCDs for IR detector multiplexing will be described.

Issues in FPA Readout Electronics

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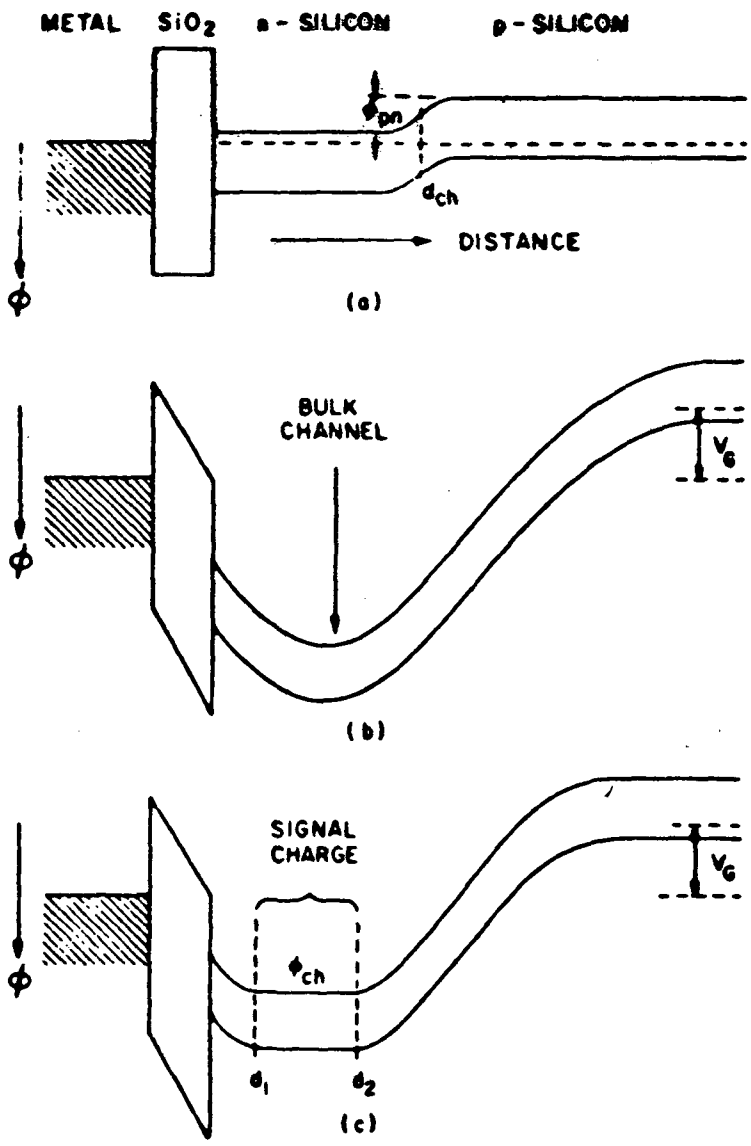
ERF

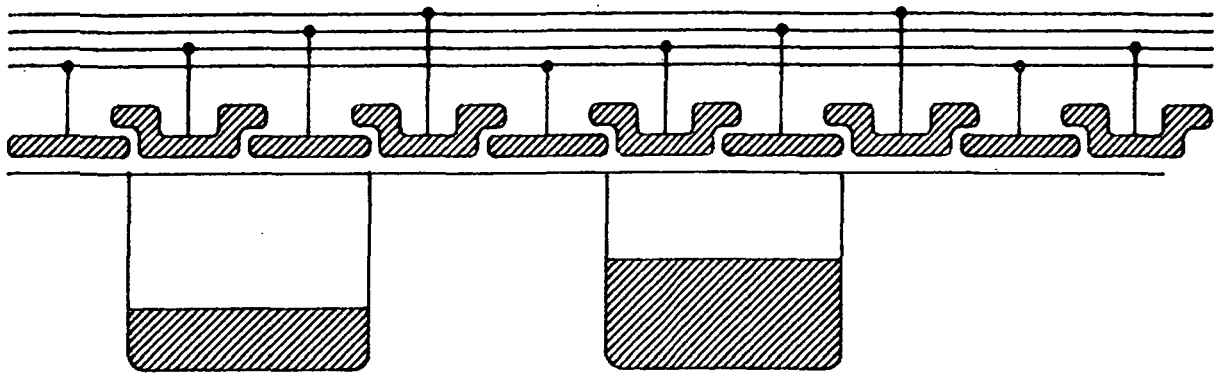
Outline

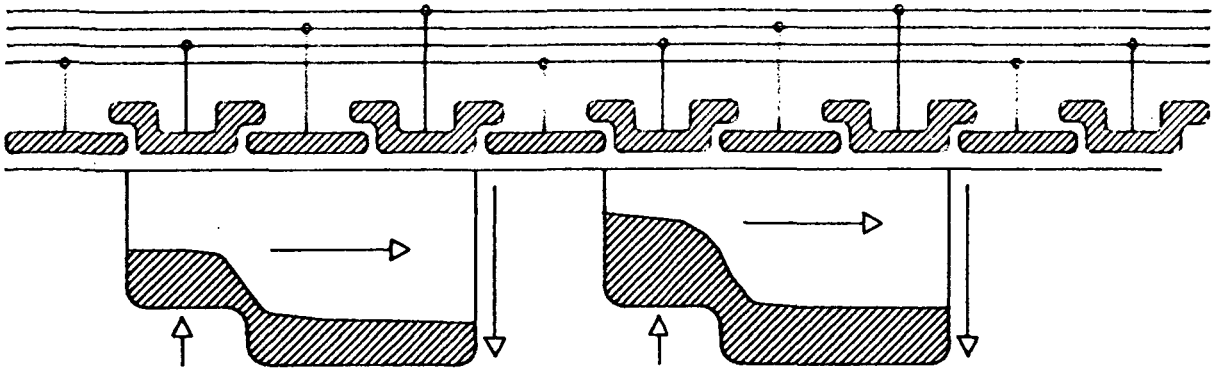
1. Present Imager Readout Architectures
2. Special Problems in LWIR Readout
3. GaAs CCD Readout
4. On-chip Signal Processing

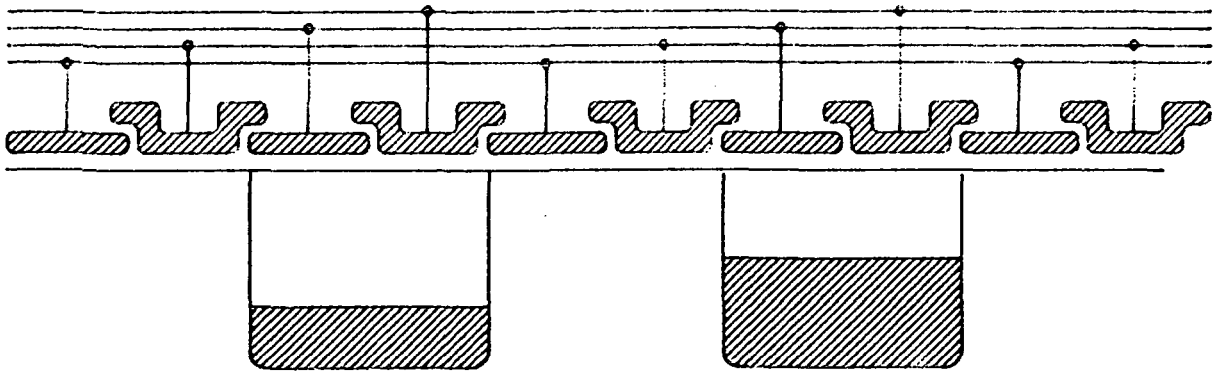
ERF


METAL
SiO2
n - SILICON
p - SILICON
φpn
dch
DISTANCE
φ
(a)
BULK
CHANNEL
VG
φ
(b)
SIGNAL
CHARGE
VG
φch
φ
d1
d2
(c)

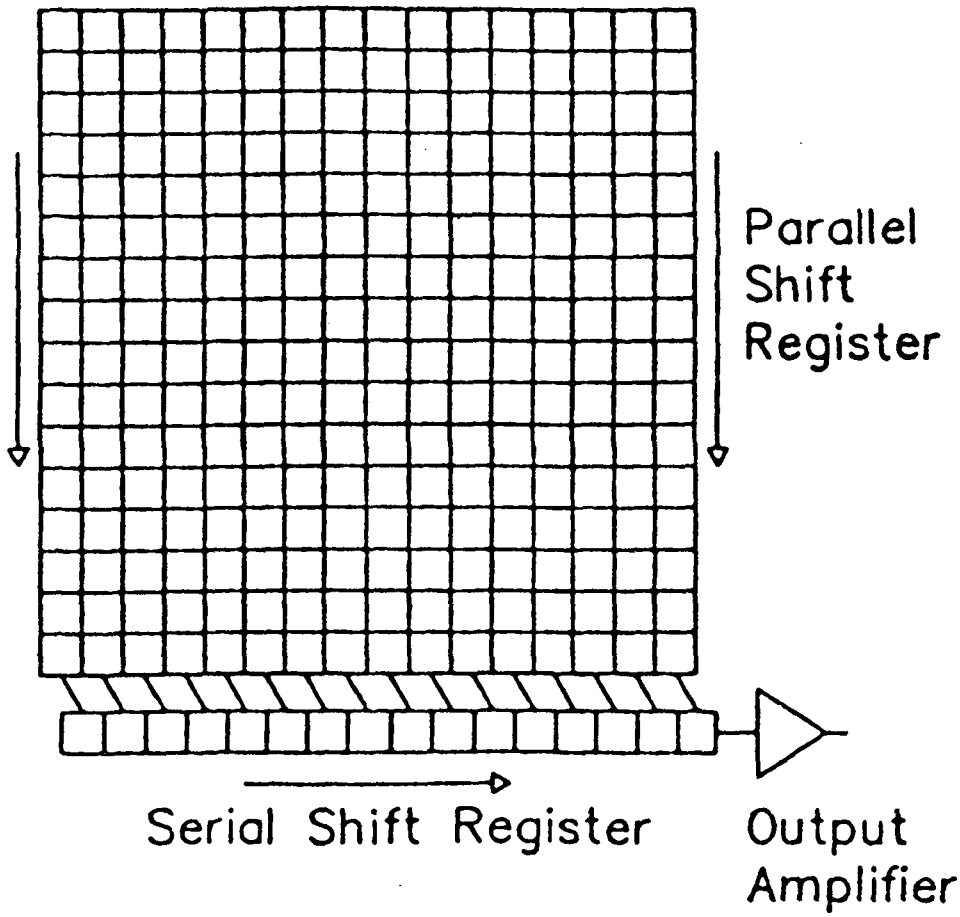
4-PHASE CHARGE TRANSFER







Schematic illustration of a charge-coupled device (CCD) imager read-out structure.

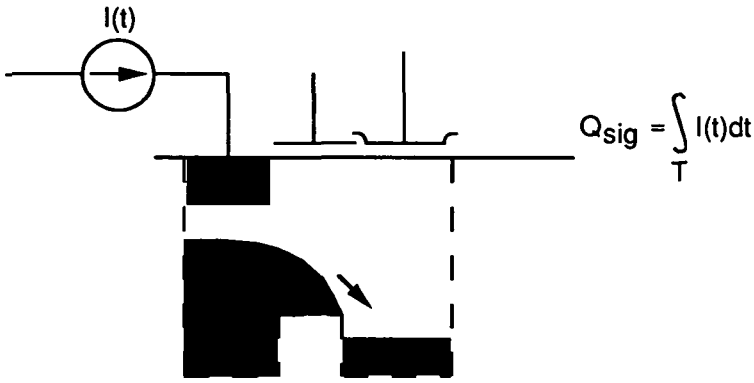


COMMERCIALLY-AVAILABLE CCDS

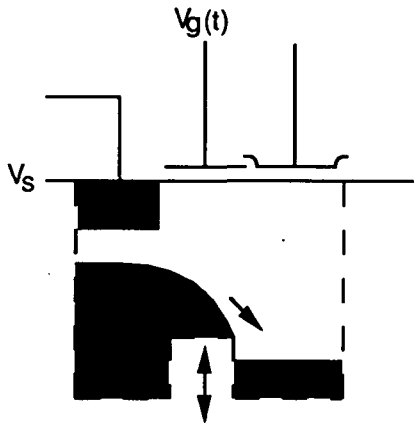
MANUFACTURER	DEVICE	FORMAT	STRUCTURE	PIXEL SIZE, μm	DIMENSIONS, mm	GATES/PIXEL	
EG&G Reticon (US)	RA0256B	256x256	Full Frame	40x40	10.2x10.2	4	
Fairchild (US)	CCD222	488x380	Interline	30x18	8.8x11.4	2	
Photometrics (US)		516x516	Full Frame	20x20	10.3x10.3	4	
Tektronix (US)	TK512M	512x512	Full Frame	27x27	13.8x13.8	3	Thinned
	TK2048M	2048x2048	Full Frame	27x27	55.3x55.3	3	Thinned, Develop.
Videk (US)	Megaplus	1320x1035	Full Frame	6.8x6.8	9.0x7.0	2	
Amperex (Holland)	NKA1010	604x294	Frame Transfer	10x15.6		4/3	
Dalsa (Canada)	IA-D1-0256	256x256	Frame Transfer	16x16	4.1x4.1		
Eng. Elec. Valve (UK)	P-86131	576x385	Full Frame	22x22	12.8x8.5		
Sanyo (Japan)		572x485					
		640x480					
Texas Inst. (Japan)	T1241	754x488	Frame Transfer	11.5x27		1	
	TC215	1024x1024	Full Frame	12x12	12.3x12.3	1	
	TC217	1134x486	Frame Transfer	7.8x13.6		1	
Thomson CSF (France)	TNX31156	1024x1024	Full Frame	19x19	19.5x19.5	4	Develop.
	TNX7863	576x384	Full Frame	23x23		4	
Toshiba (Japan)		1920x1036					

INTEGRATING INPUTS

1. DIRECT INJECTION



2. GATE MODULATION



$$Q_{sig} = \int_T I(V_g(t))dt$$

COULD BE SUBTHRESHOLD
OR WEAK INVERSION
OR INVERSION

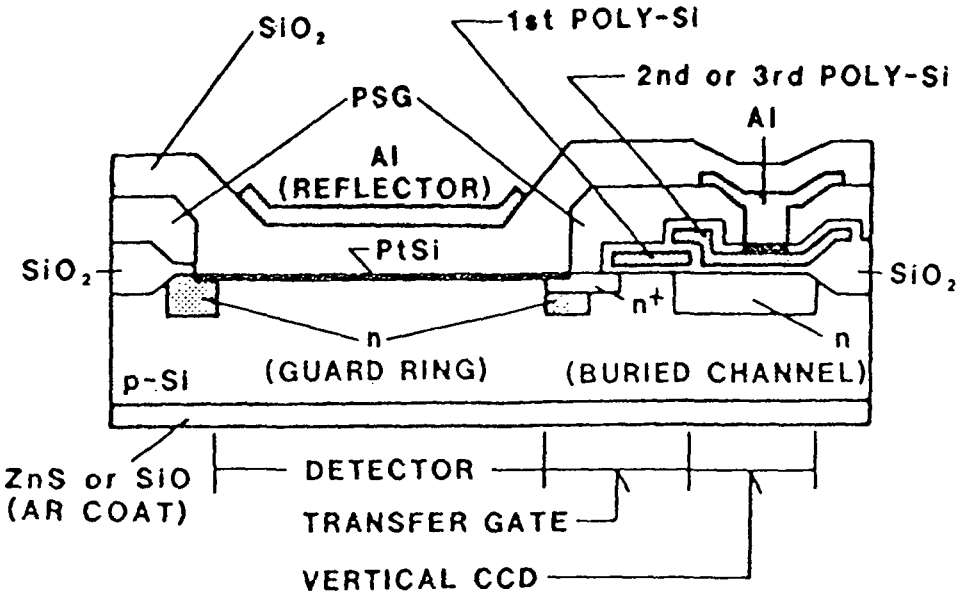


Fig. 5. Pixel cross section of 256 × 256 element IR-CCD image sensor.

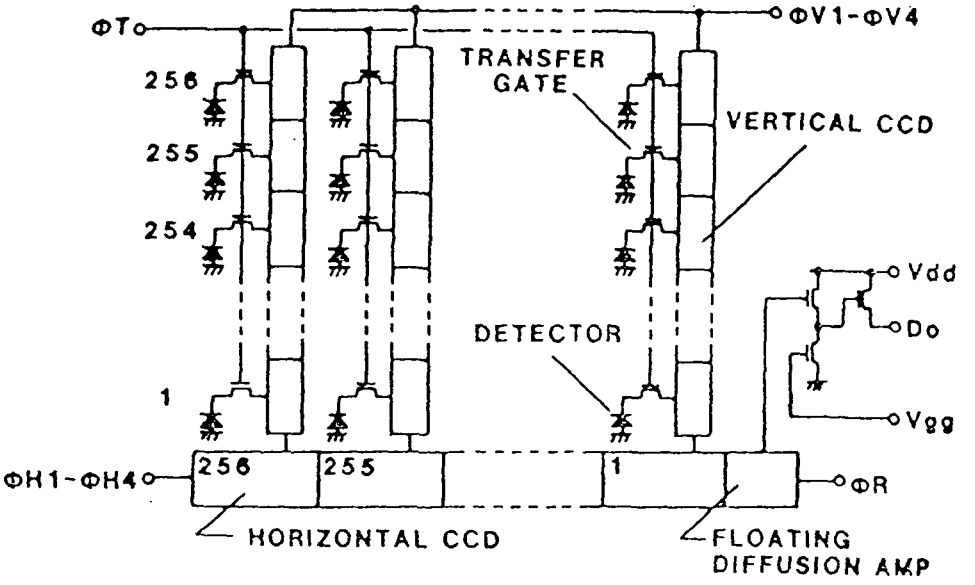


Fig. 3. Schematic diagram of 256 × 256 element IR-CCD image sensor.

Kimata, et al. Opt. Eng 26(3) 211 (1987).

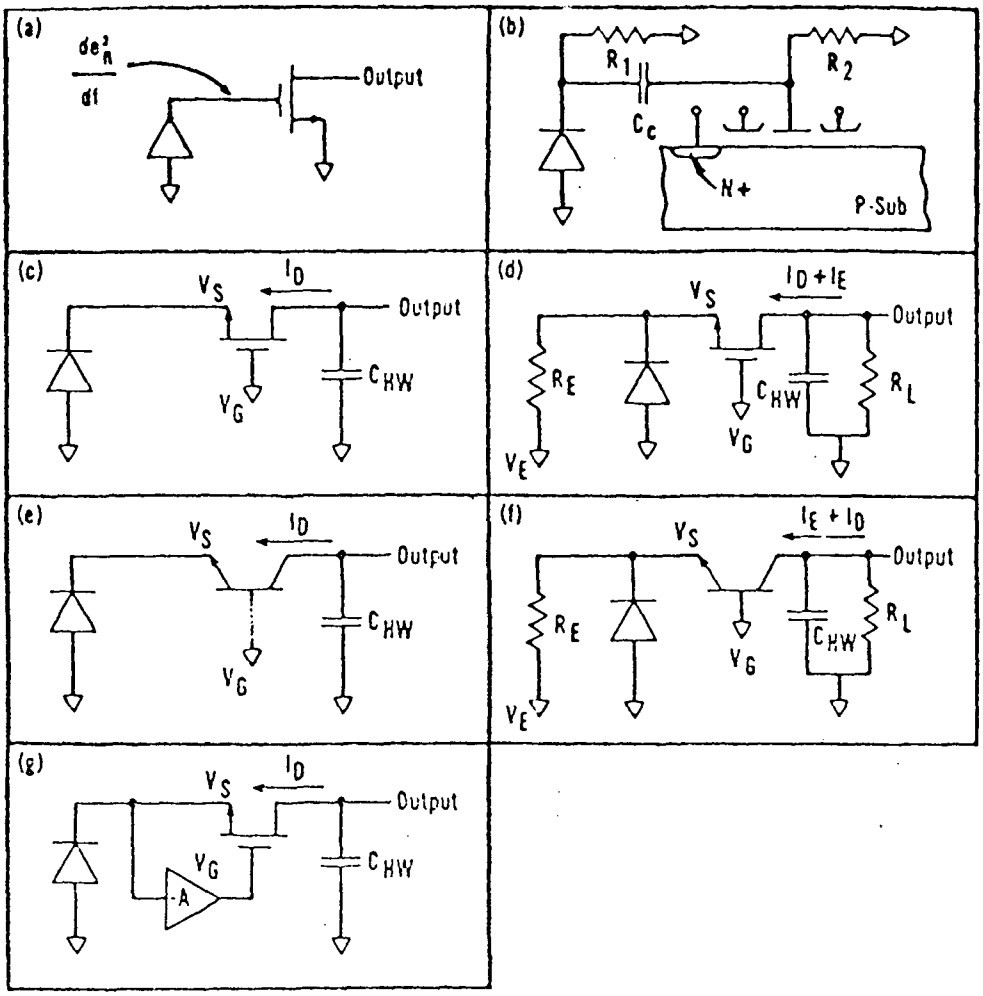
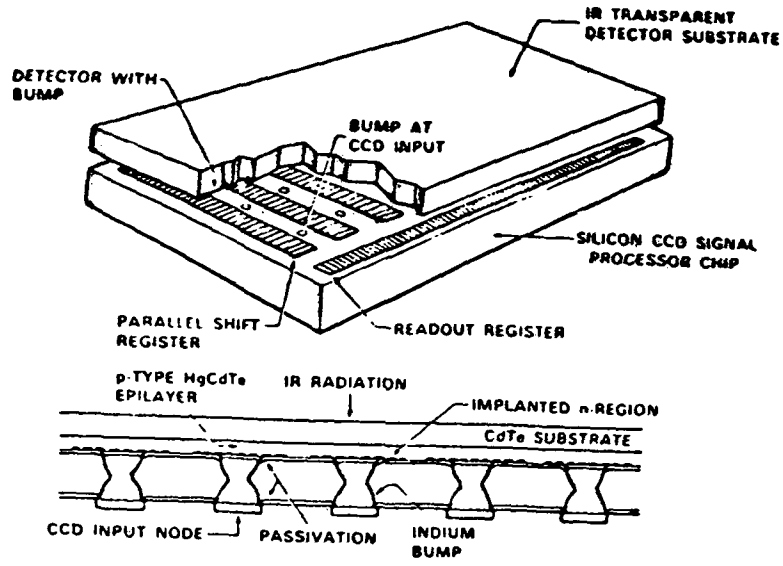


Fig. 2. Various detector readout structures: (a) gate readout (GRO); (b) gate-coupled readout (GCRO) to CCD; (c) direct-injection (DI) current readout; (d) direct-injection ancillary current (DIAC) readout; (e) direct-injection bipolar (DIB) current readout; (f) direct-injection bipolar ancillary current (DIBAC) readout; (g) buffered direct-injection (BDI) current readout.

Bluzer and Jensen Opt. Eng. 26(3) 241 (1987).



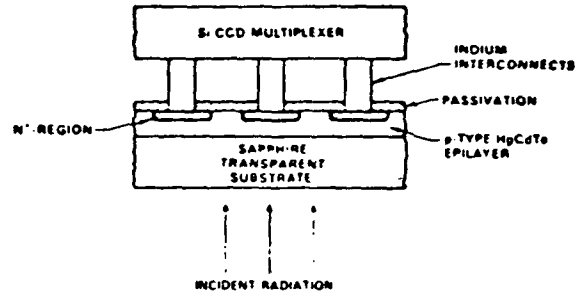


Fig. 8. Backside-illuminated hybrid FPA.

VURAL

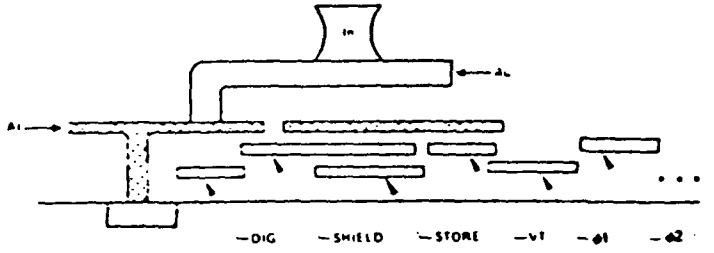
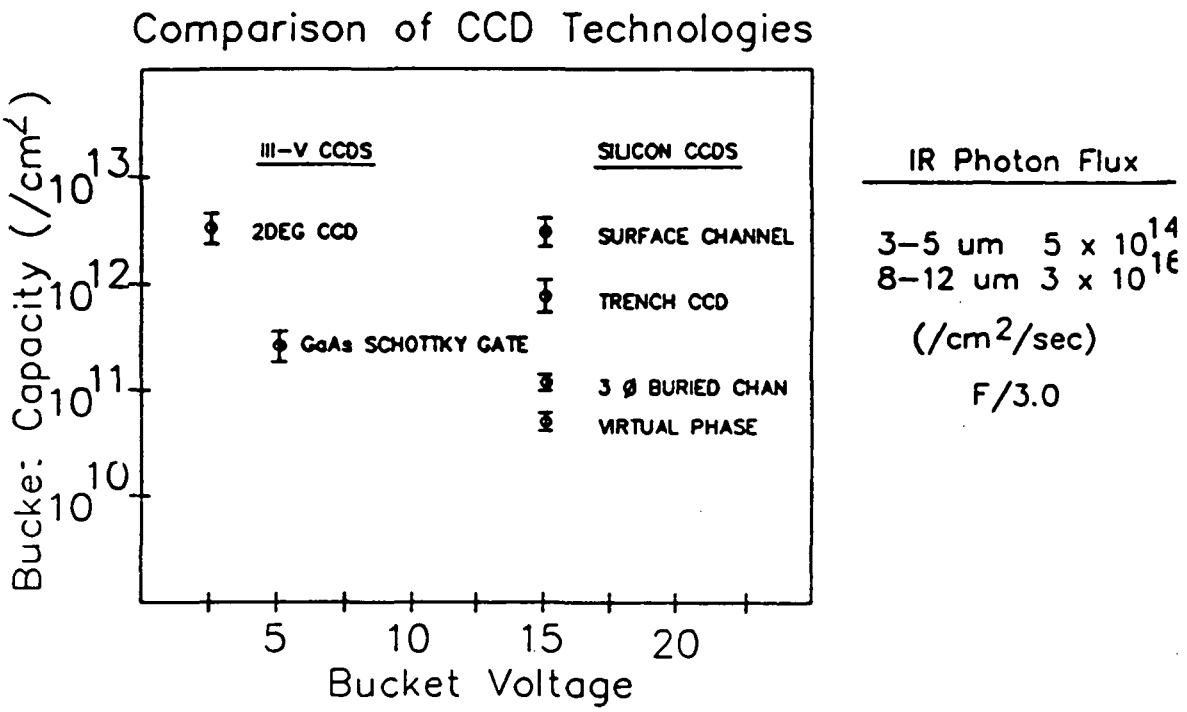
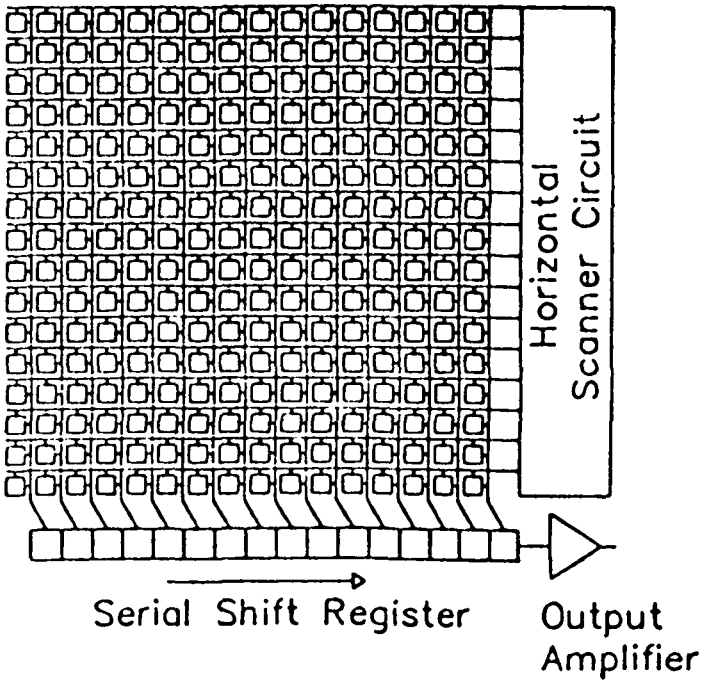


Fig. 6. Direct-injection input circuit schematic for 64 x 64 multiplexer.



Schematic illustration of a MOS-CCD imager read-out structure.



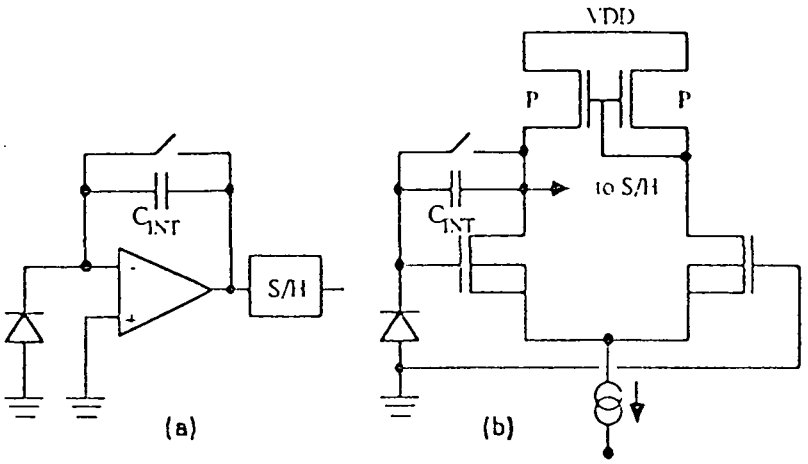


Fig. 5. Reset integrator input circuit: (a) functional block diagram, (b) MOSFET implementation.

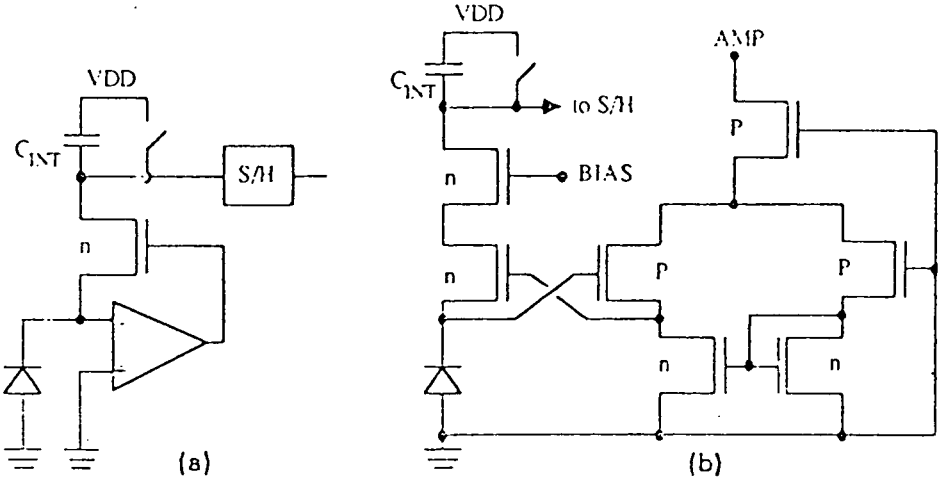


Fig. 6. Buffered common gate input circuit: (a) functional block diagram, (b) MOSFET implementation.

Lockwood and Parrish, Opt. Eng 26(3) 228 (1987).

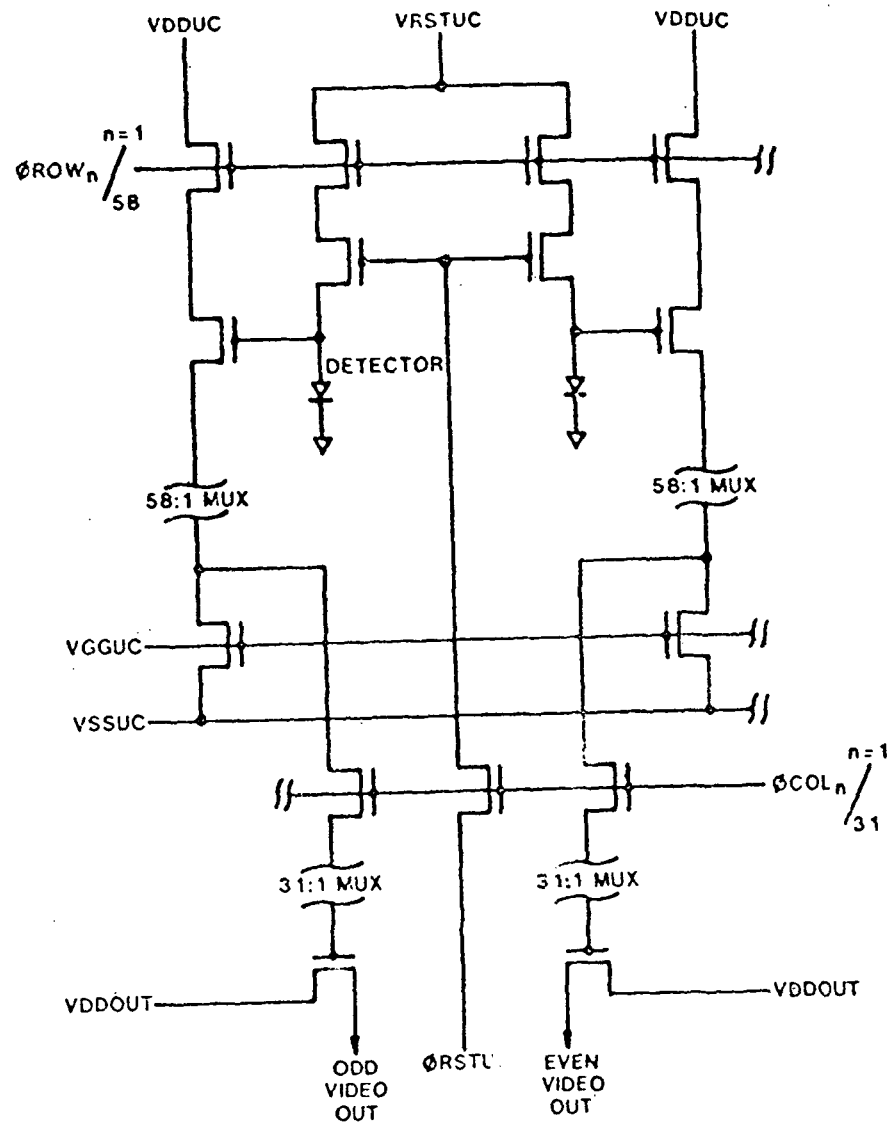


Fig. 2. Simplified schematic of the direct readout circuit used for this array.

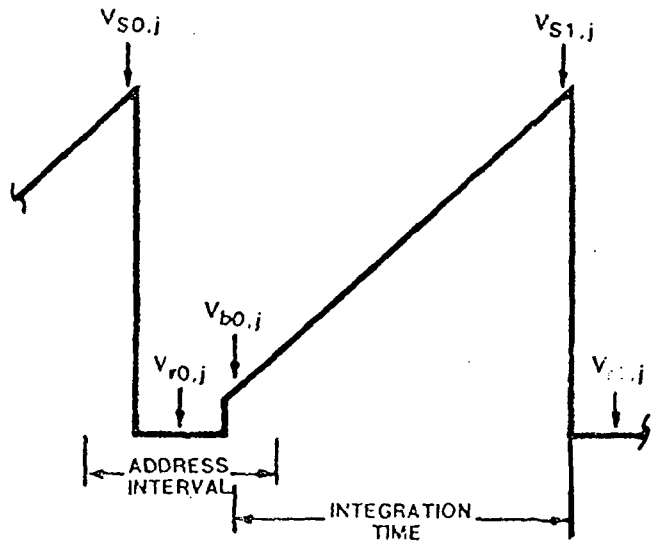


Fig. 5. Representation of the voltage across a single pixel during an integration interval at the detector node.

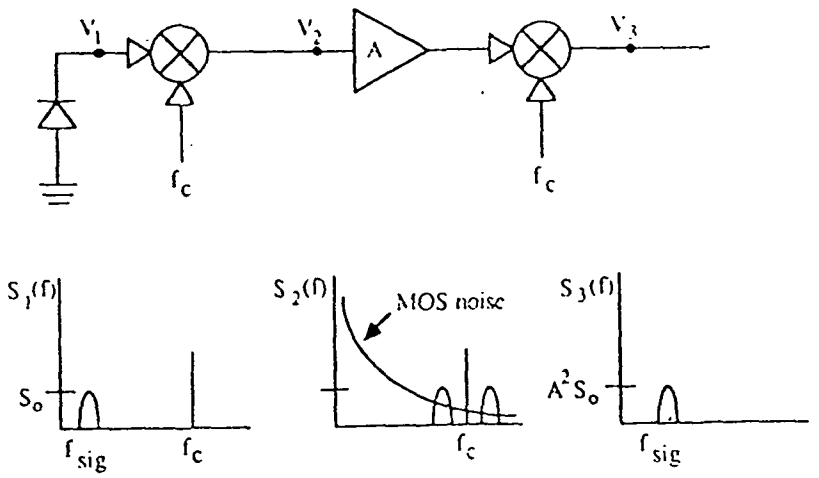


Fig. 8. Carrier modulation scheme used to upconvert detect signals to higher frequencies where MOSFET noise is low.

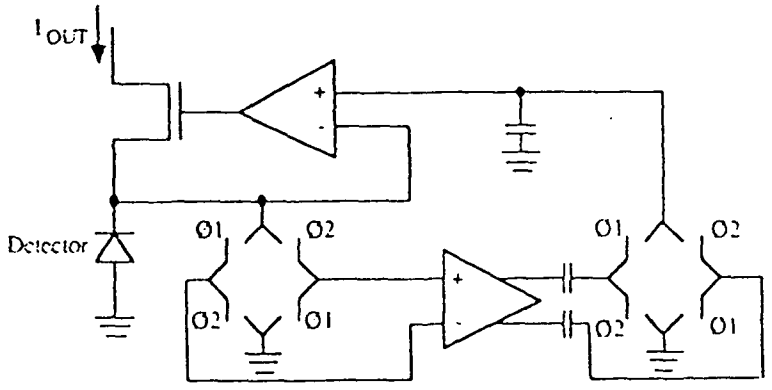


Fig. 9. Buffered common gate readout input circuit using chopp stabilization to reduce detector bias offsets and amplifier 1/f noi

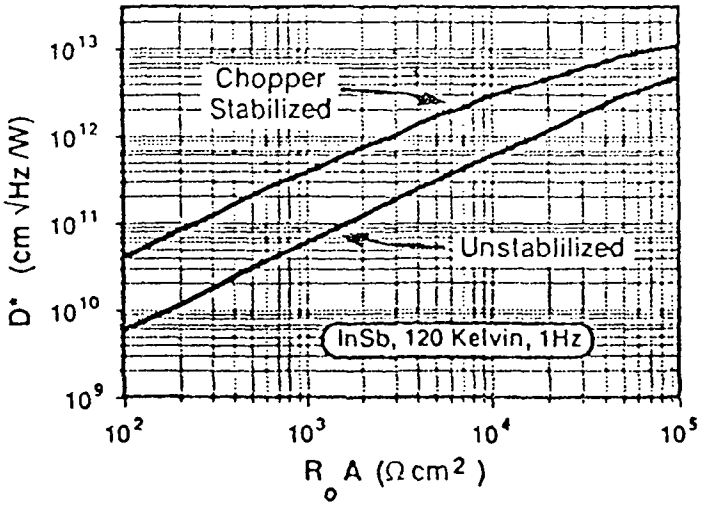


Fig. 10. Projected chopper-stabilized InSb focal plane perfc mance.

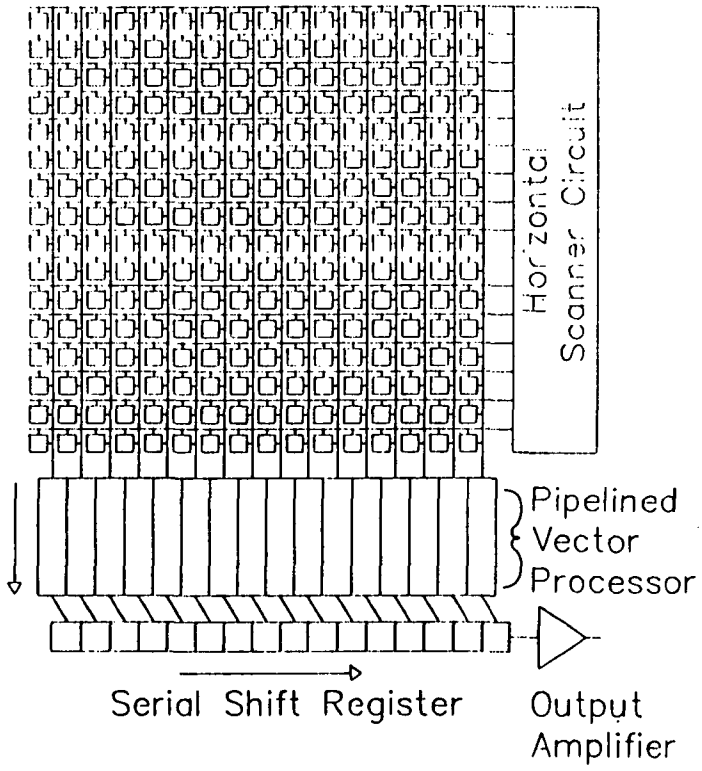
Lockwood and Parrish, Opt. Eng 26(3) 228 (1987).

IMAGE ACQUISITION

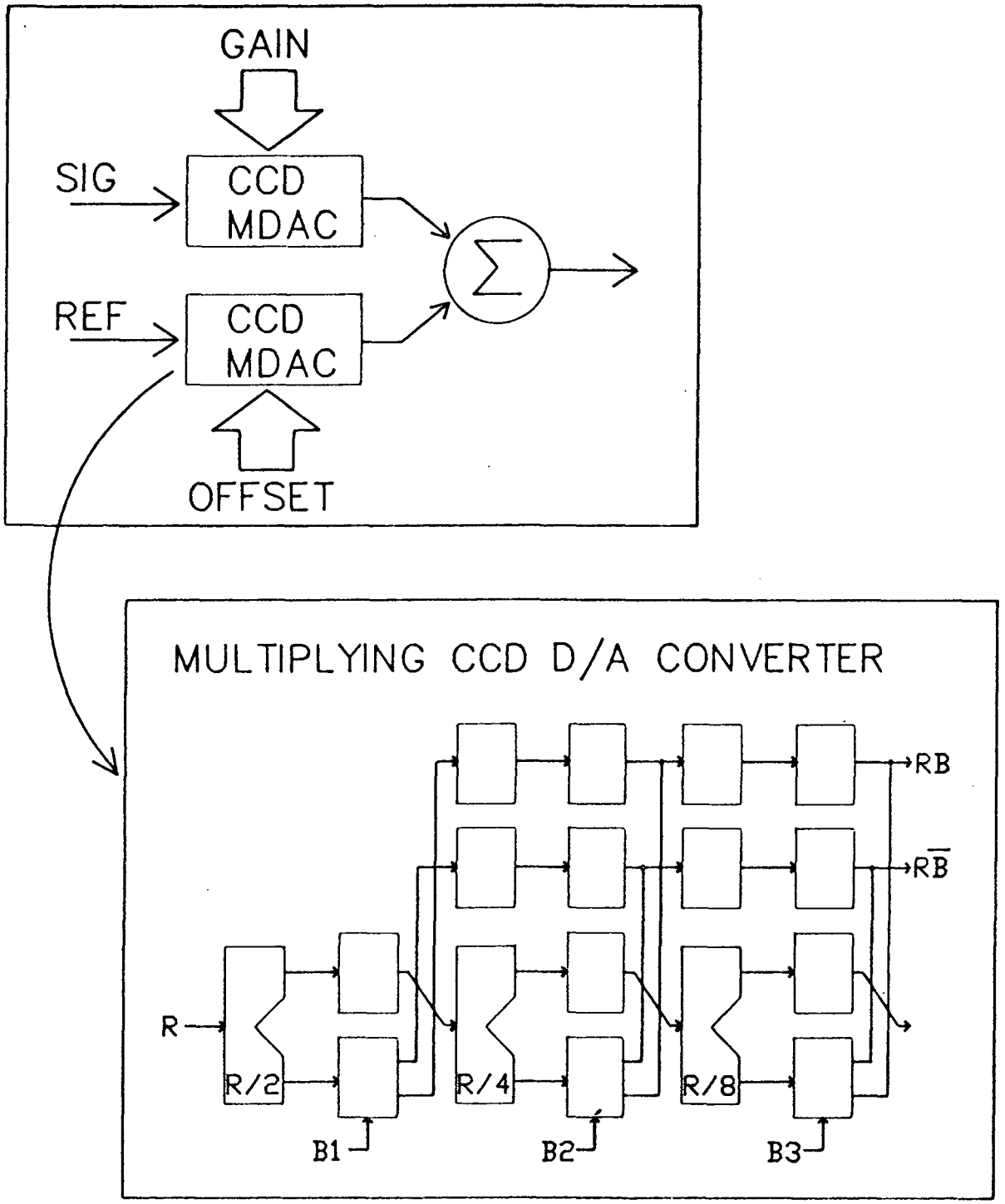
+ IMAGE PROCESSING

FOCAL PLANE IMAGE PROCESSING

WHY	WHY NOT
NOISE	YIELD
DISTORTION	CHIP SIZE
POWER	COOLING
SIZE	NON-UNIFORMITY CORRECTION
RELIABILITY	
COST	



NON-UNIFORMITY CORRECTION



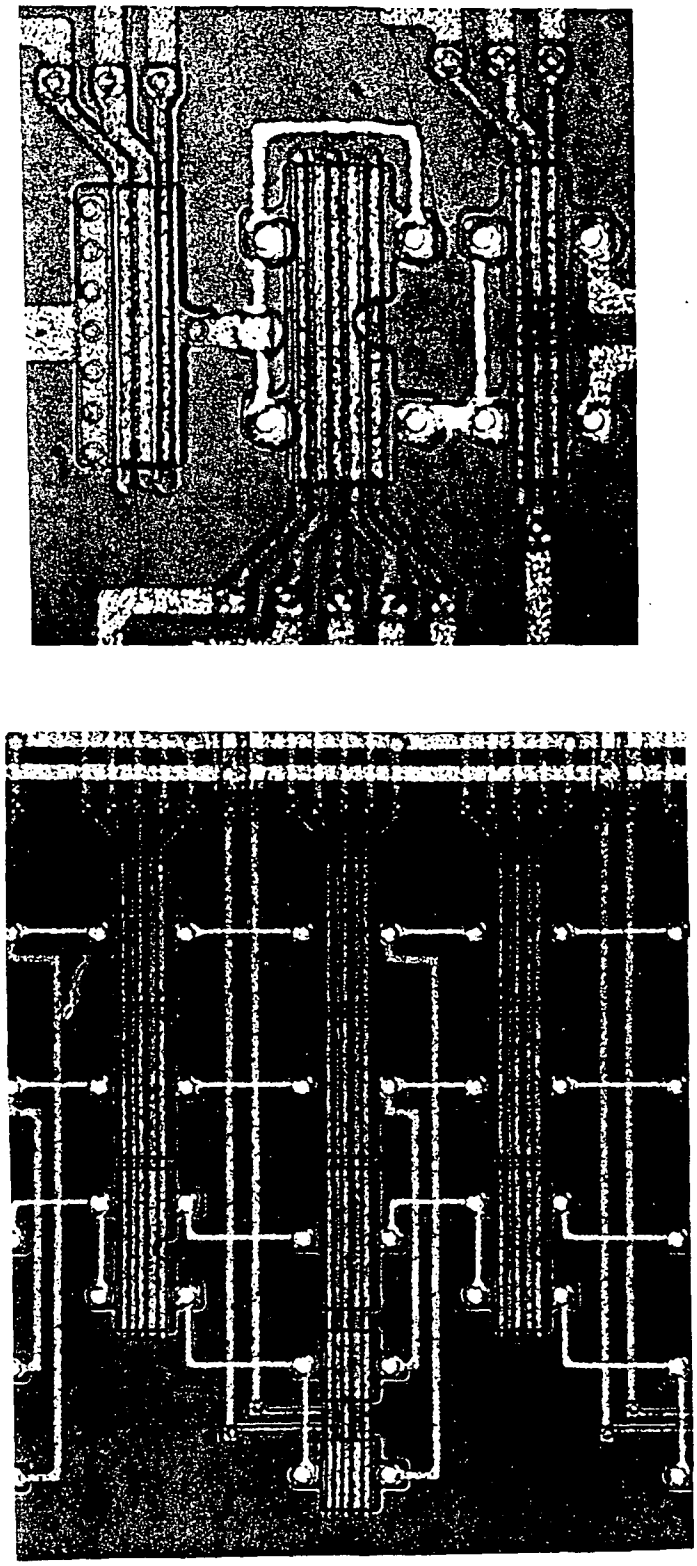


Fig. 2. Photograph of (a) serial recursive circuit and (b) single stage of pipeline circuit.

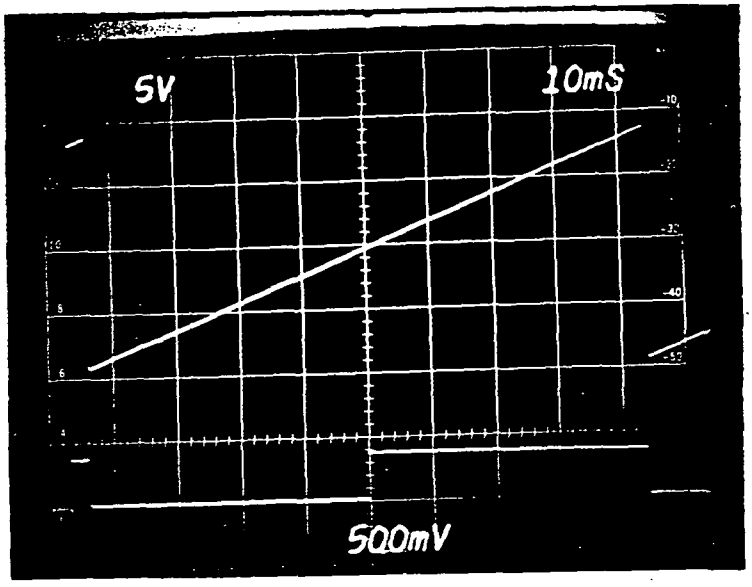


Fig. 3. Oscilloscope photograph showing analog output of pipeline programmable gain control circuit in response to a digital ramp (upper trace) and MSB of digital control word (lower trace).

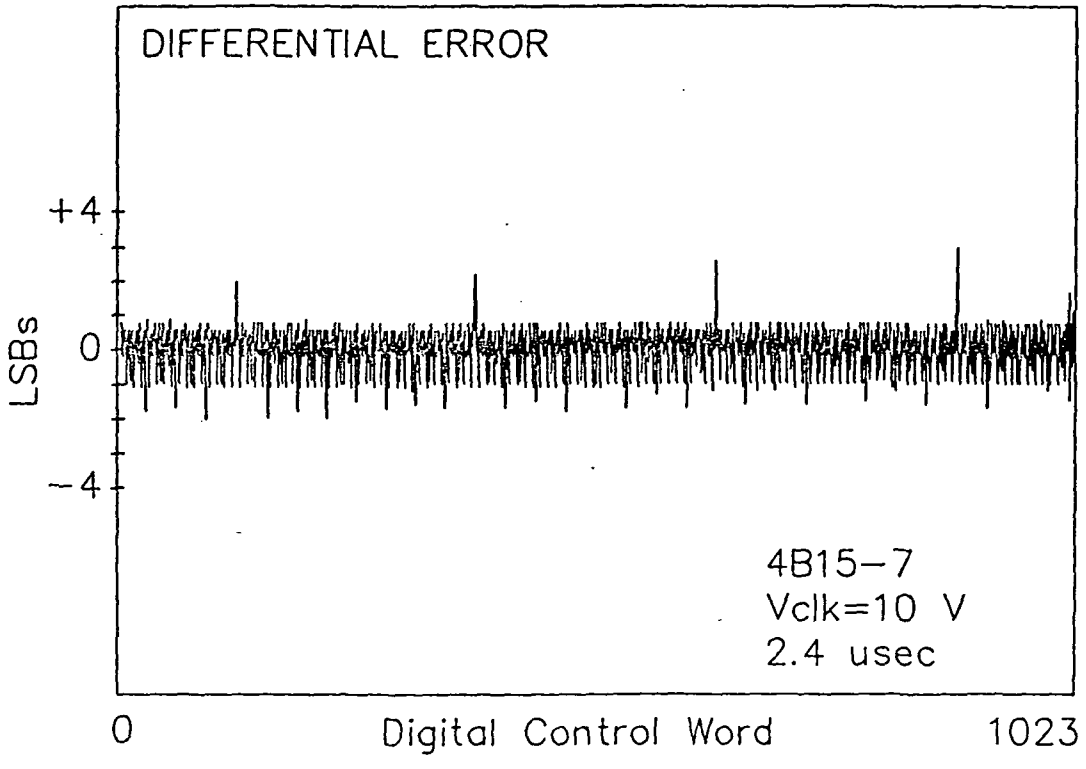
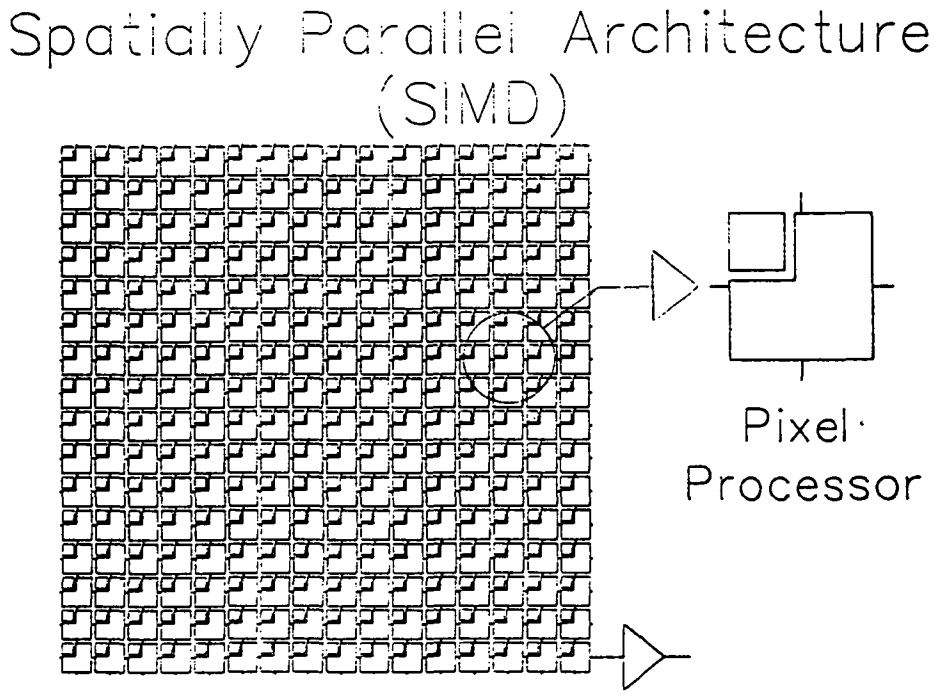


Fig. 4. Differential linearity error of pipeline circuit. Note that 1 LSB tic mark corresponds to 1/1024 of full scale.

CCD Programmable Gain Control Circuit

Performance Summary

	Pipeline	Serial
Technology	3 μ m CCD	3 μ m CCD
Circuit Size	0.4 mm^2	0.013 mm^2
Resolution	10 bits	variable
Integral Linearity	8 bits	6 bits
Differential Linearity	8 bits	6 bits
Clock Voltage	10 volts	10 volts
Bucket Cap. (electrons)	$5x10^6$	$5x10^6$
Power (10^3 conv/sec)	2 μ W	2 μ W
Max. Conversion Rate	$>8x10^6$/sec	$>0.5x10^6$/sec



FPA CCC POWER CONSIDERATIONS

TO TRANSFER 1 BUCKET (HALF FULL) $\Delta V = 10$ VOLTS

ENERGY = 8 pJ

ARRAY WITH 1500 PEs OPERATING IN PARALLEL

12 nJ

SAY EACH INSTRUCTION REQUIRES 10 TRANSFERS,
SAY 100 INSTRUCTIONS PER PIXEL TO PREPROCESS

12 μJ PER FRAME

SAY 1000 Hz FRAME RATE*

12 mW CHIP DISSIPATION

ADD IN DRIVERS, PARASITICS, MULTIPLY BY 2

25 mW

FOR 1 kHz REAL TIME PREPROCESSED IMAGERY

* AT 100 nsec/TRANSFER, CAN OPERATE AT 1MHz INSTRUCTION RATE, OR 10 kHz FRAME RATE POSSIBLE

NOISE CONSIDERATIONS

SAY BIAS = 10 V ⟶ 8 VOLT BUCKET

~250,000,000 ELECTRONS/HOLES

SAY WANT 8-BIT EQUIVALENT ACCURACY W/ SNR = 4 ON LSB

⟶ MAXIMUM NOISE ~ 250,000 CARRIERS

NOISE SOURCES:

1) CAPACITIVELY COUPLED CIRCUITS

$$n_{RMS} = \left(\frac{kTC}{q}\right)^{1/2} \lesssim 1000 \text{ CARRIERS}$$

2) TRANSFER

$$n_{RMS} = (2\,E\,\bar{N})^{1/2} \lesssim 5000 \text{ CARRIERS}$$

($E = 0.05$, $\bar{N}$ = FULL)

3) INTERFACE

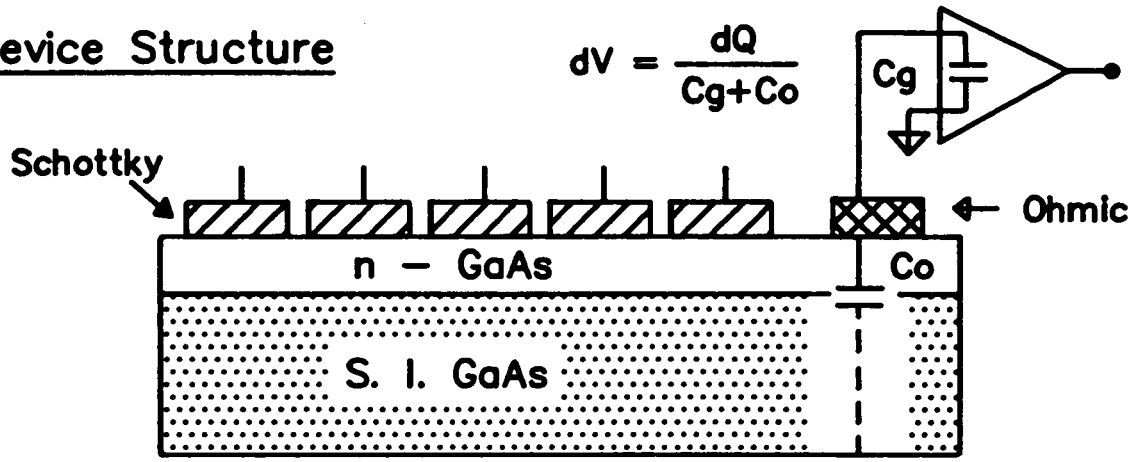
$$(1.4\,kTD_{IT}A_E)^{1/2} \lesssim 200 \text{ CARRIERS}$$

CCC PROGRAM, SAY 50 TRANSFERS AND 10 FILL & SPILLS

⟶ RMS 35,000 CARRIERS

WHY GaAs CCDs ?

Device Structure

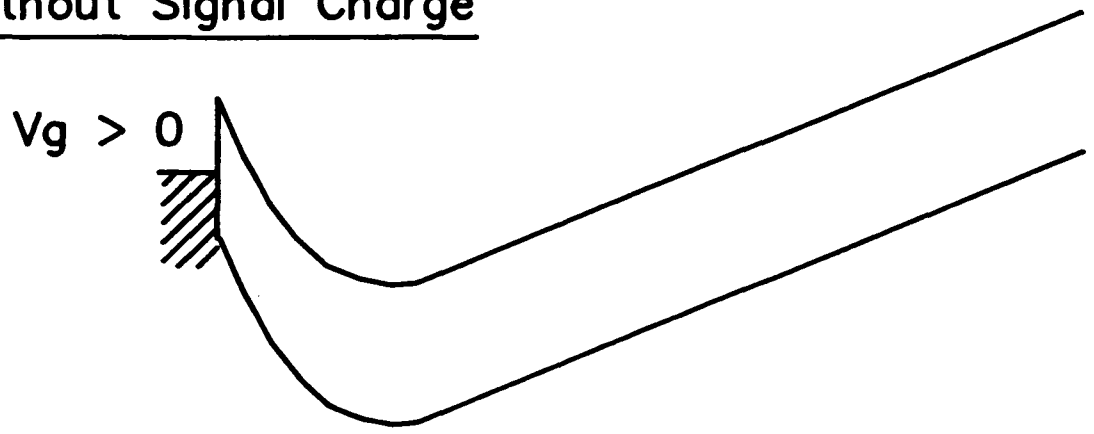


Features

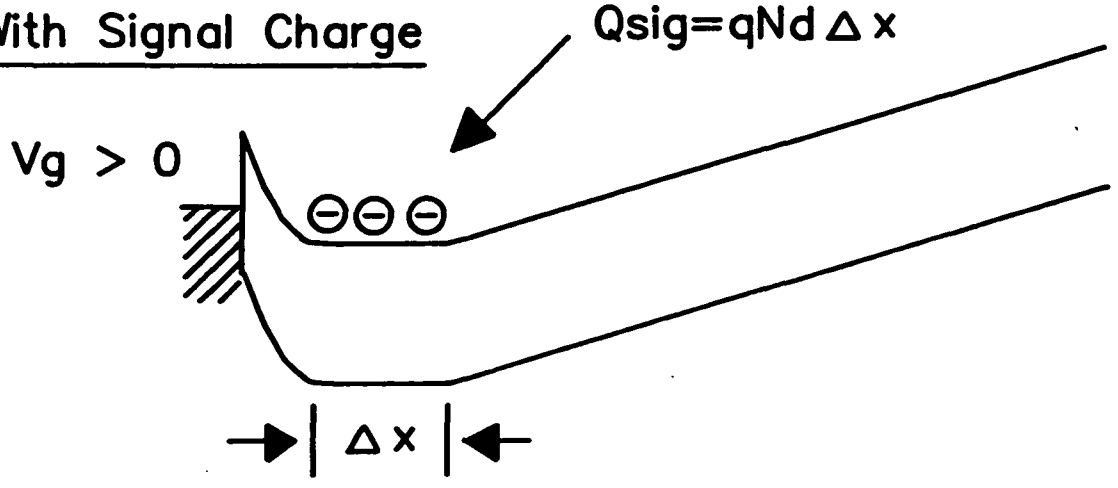
- High Electron Mobility
  - High Transfer Speed
  - High f_t Transistors
- Wide Bandgap
  - Radiation Hard
  - Low Noise
- Semi–Insulating Substrate
  - Low Parasitic Capacitance
  - Mesa Isolation
- Compatibility with III–V Detectors

BAND DIAGRAM OF GaAs CCD

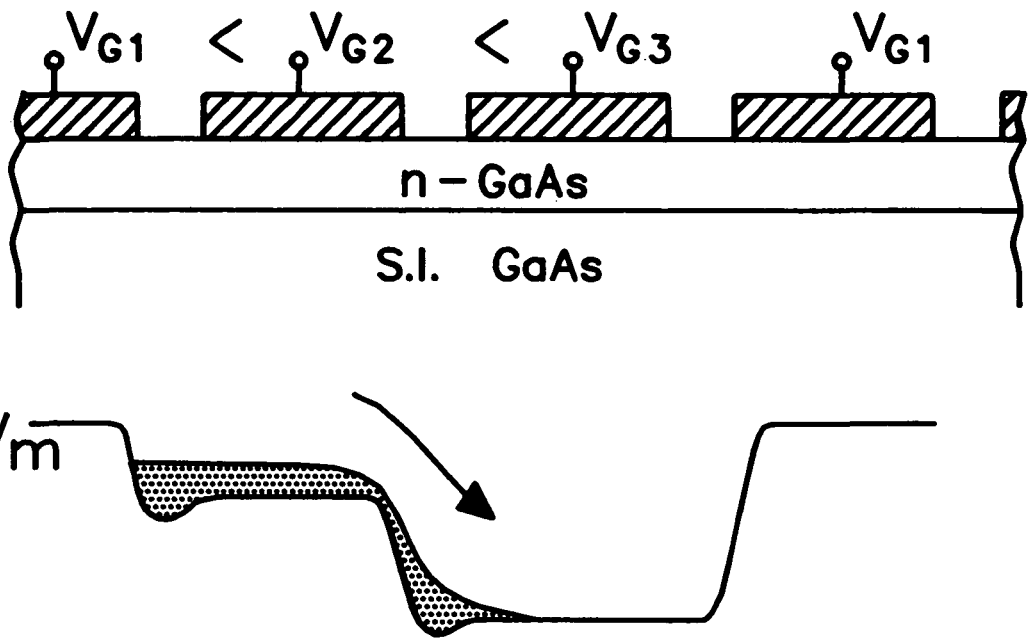
Without Signal Charge



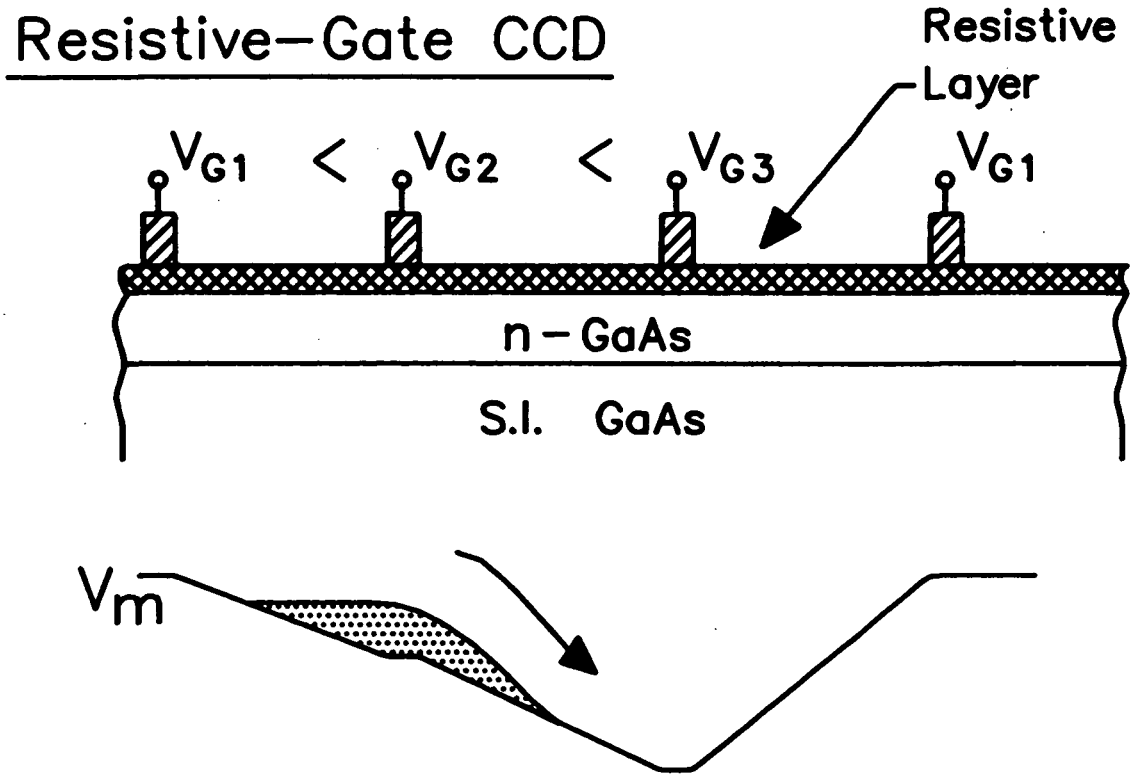
With Signal Charge

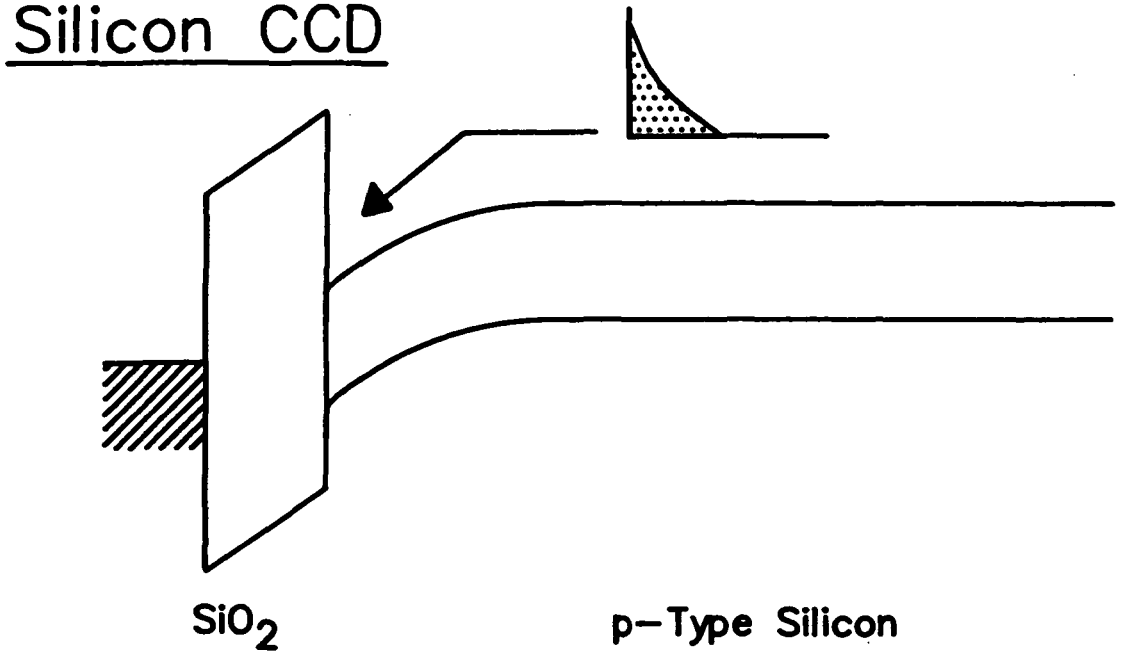


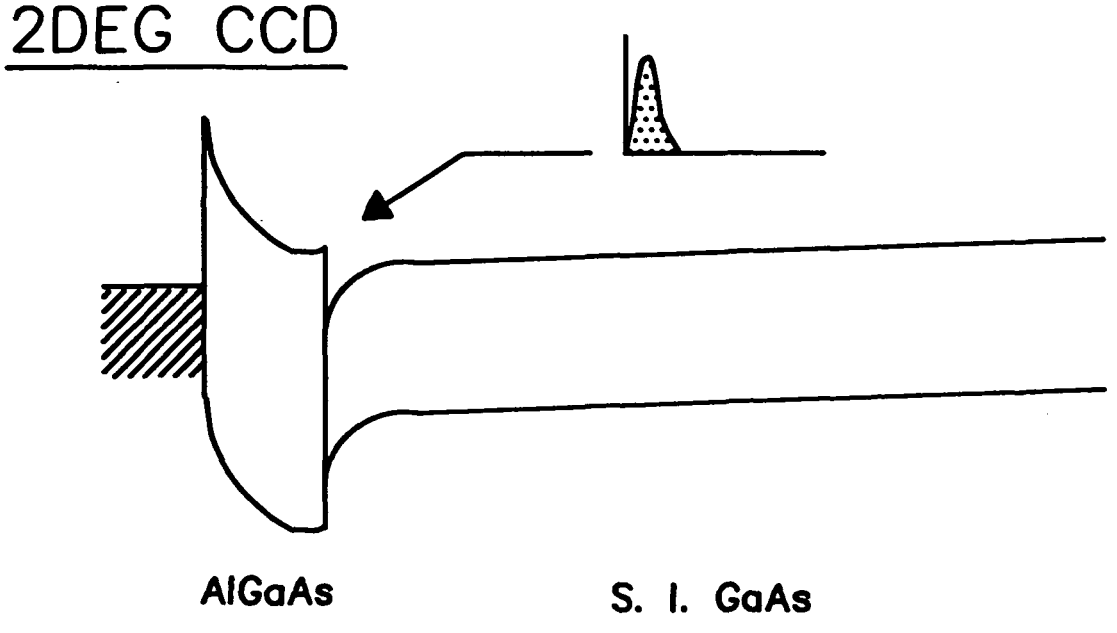
Capacitive–Gate CCD



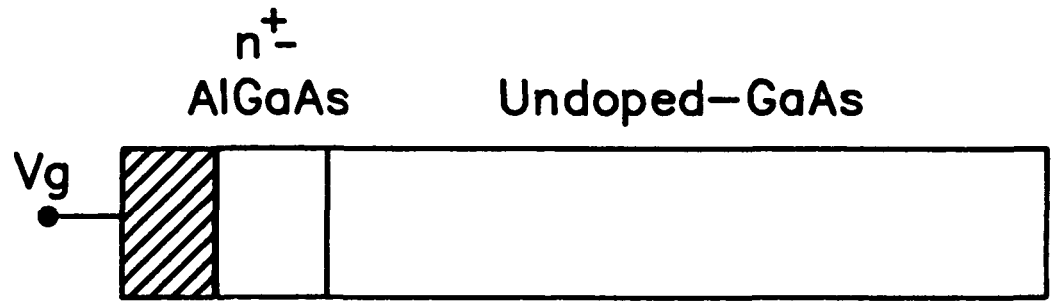
Resistive–Gate CCD



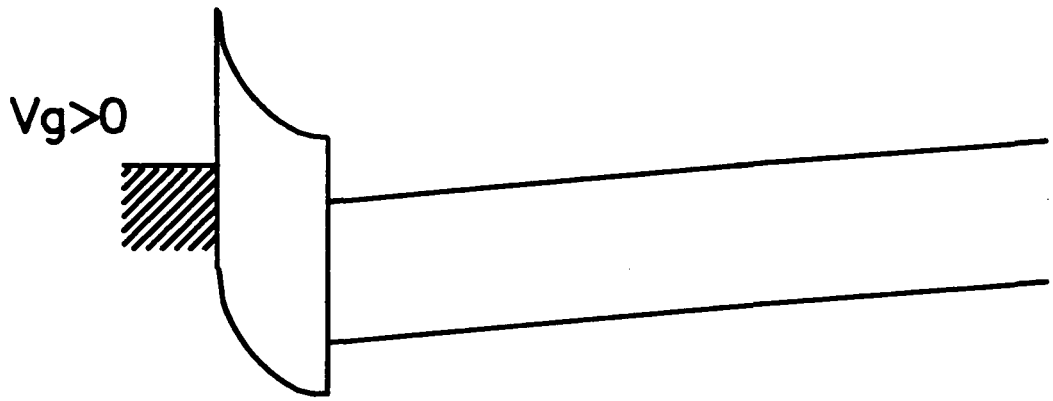

Silicon CCD
SiO_2
p–Type Silicon


2DEG CCD
AlGaAs
S. I. GaAs

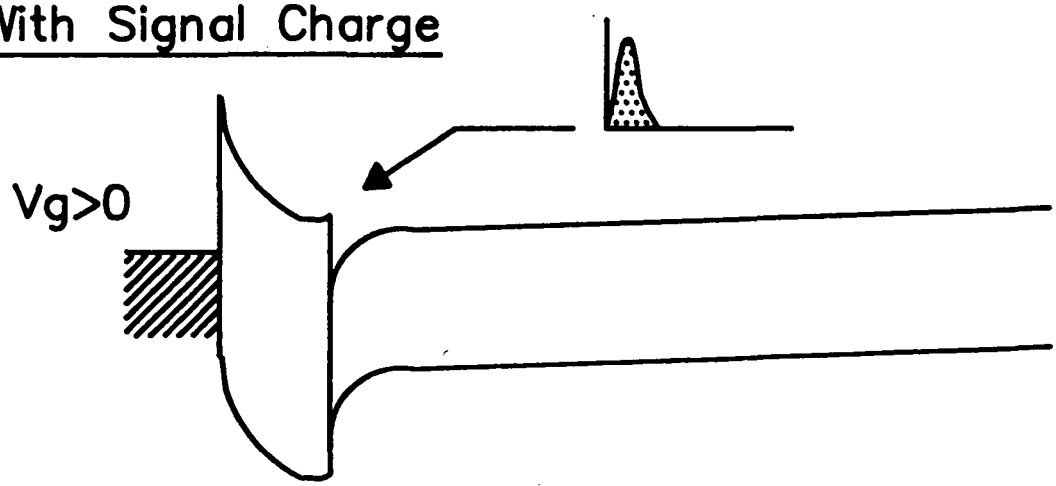
BAND DIAGRAM OF 2DEG CCD



Without Signal Charge

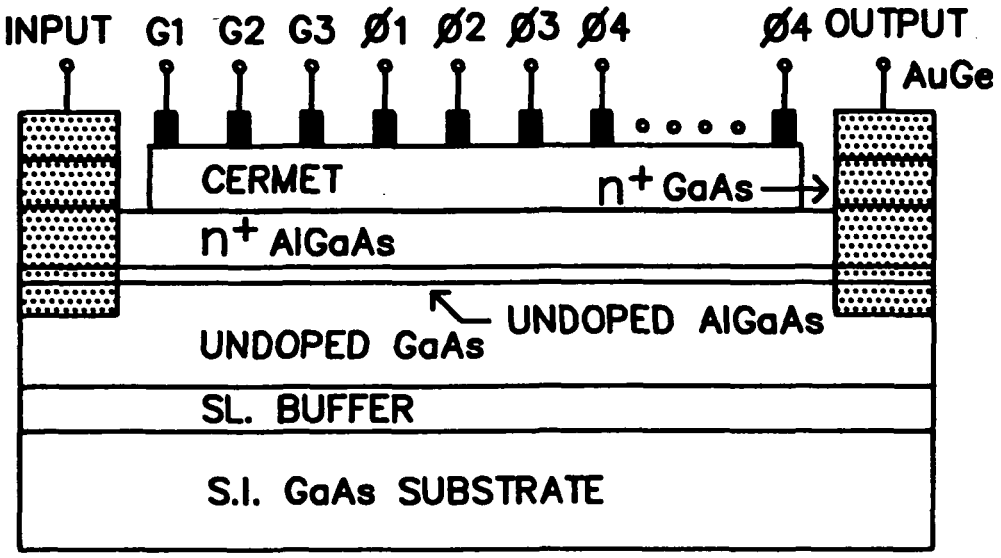


With Signal Charge



2DEG RGCCD

Device Structure



Features

- High Electron Mobility

  High Transfer Speed

  High Performance 2DEGFET
- Large Dynamic Range

  $n_s > 1 \times 10^{12} /cm^2$
- High Sensitivity Input
- Enhanced

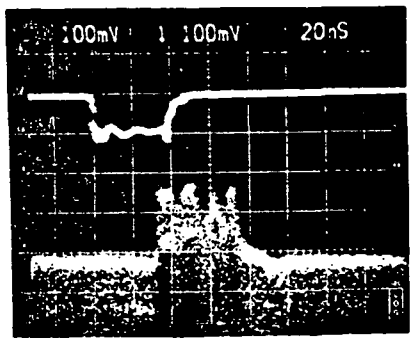
  Low Temperature Performance

OPERATION OF 2DEG RGCCDs

Room Temperature

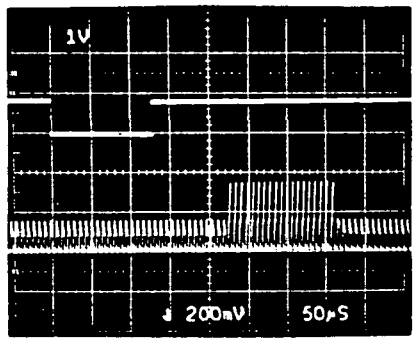
4 Phase Clocking, 32 Stages (128 Transfers)

1 um Electrode Width, 4 um Spacing, 100 um Channel Width



Uniform–Doped 2DEG RGCCD

CTE = 0.999 At 1 GHz



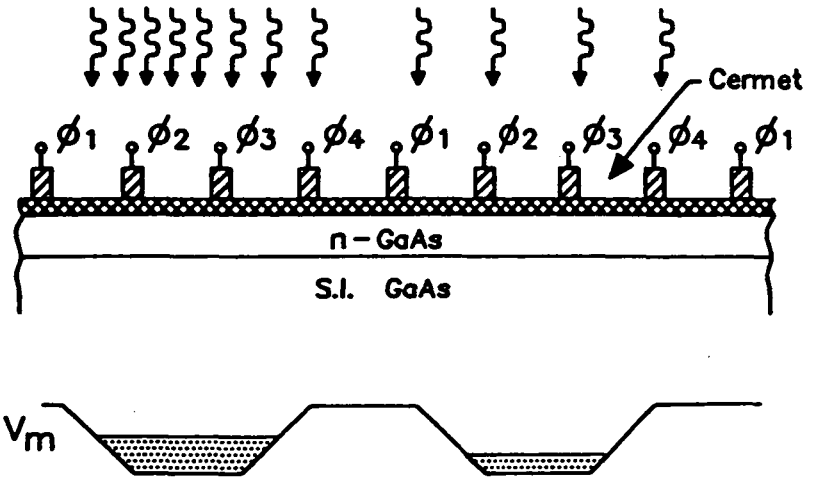
Planar–Doped 2DEG RGCCD

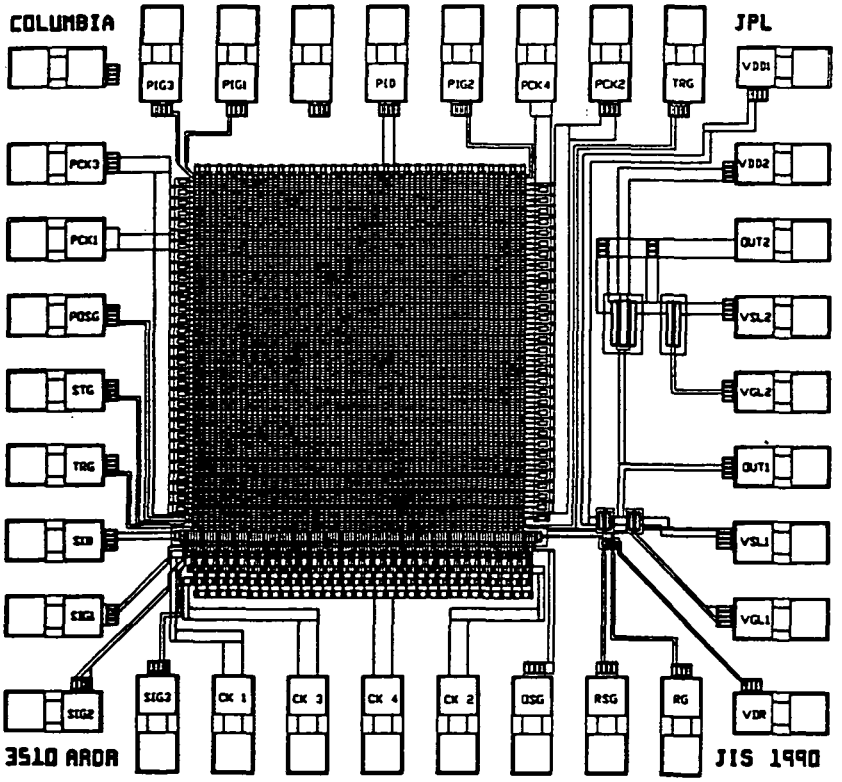
CTE > 0.999 At 133 KHz

Advances in 2DEG CCDs

Year	Group	Channel Layer Material	Gate Structure	Gap Size	Gate Length x Width (um)	Clock Freq–uency	CTE	Test Condi–tions
1982	Rockwell	AlGaAs /GaAs	Capacitive	2	40 x 400	< 83 KHz	0.98	300 K
1983	Rockwell	AlGaAs /GaAs	Capacitive	1	5 x	< 83 KHz	< 0.9	300 K
							0.989	77 K
1990	Columbia	AlGaAs /GaAs	Resistive	N/A	5 x 100	13 MHz – 1 GHz	0.999	300 K
1990	Columbia	AlGaAs /GaAs (δ–Doped)	Resistive	N/A	5 x 100	130 KHz – 1 GHz	> 0.999	300 K
1990	Columbia	InAlAs / InGaAs (δ–Doped)	Resistive	N/A	5 x 100			

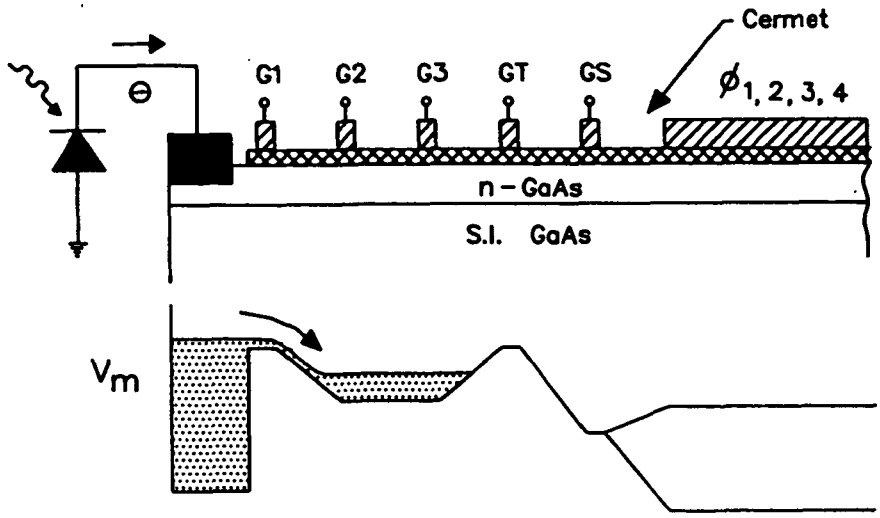
DIRECT DETECTION





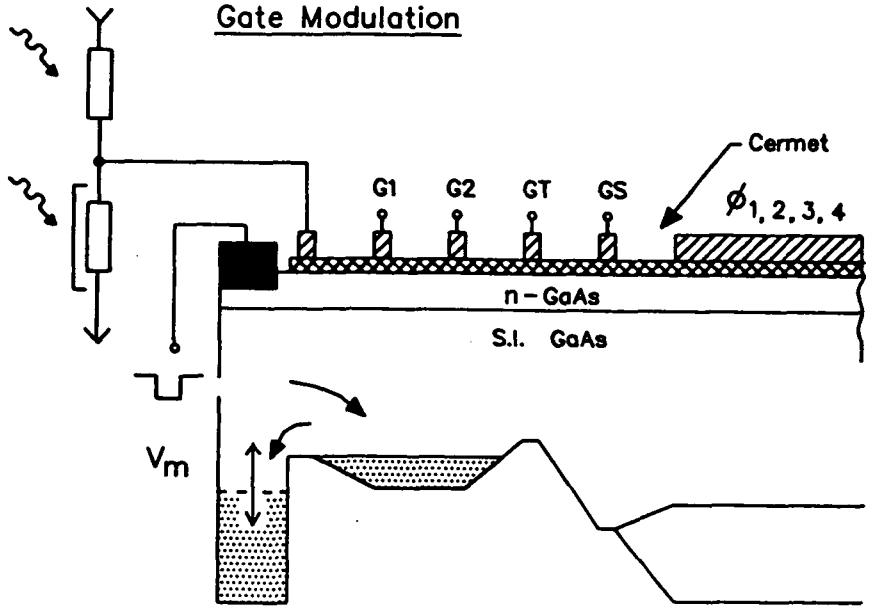
INDIRECT DETECTION

Direct Injection



INDIRECT DETECTION

Gate Modulation



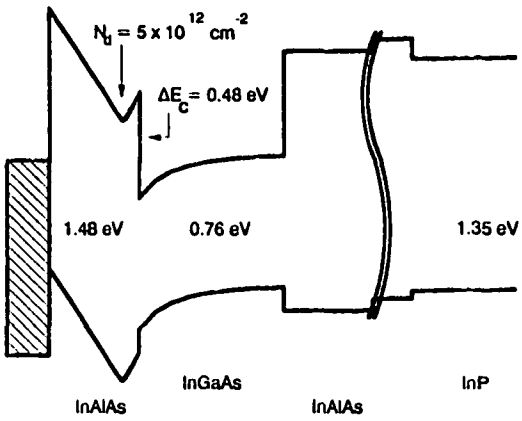
GaAs CCD MULTIPLEXER DESIGN

- Linear Arrays (32 Stages, RGCCD, CGCCD)
  - Direct Detection
  - Indirect Detection
    - Direct Injection
    - Gate modulation
- 2–D Arrays (32x32, RGCCD)
  - Direct Detection

RESEARCH ISSUES

- Leakage Current Reduction
  - Transport Mechanisms
  - Materials Quality
  - Structure
- Dynamic Range
  - Pinch Off Voltage
  - Leakage Current
- New Material System (InAlAs/InGaAs)
  - Higher Electron Mobility
  - Larger Dynamic Range

Planar-Doped In Al As / In Ga As RGCCD
0.52 0.48 0.53 0.47



- High Mobility ($\sim$20,000 $\frac{cm^2}{Vs}$ at 77 K)
- Large Sheet Carrier Density
- SWIR Direct Detection
- Compatible with Fiber-optic Integration

Present and Future Issues in Readout Electronics

Hybridization Technology
- center-to-center spacing
- array size
- buttability
- reliability

Multiplexer Material
- thermal match
- low 1/f noise devices

On-Chip Signal Processing
- random event correction
- detector non-uniformity correction
- image processing
- signature recognition

4/13/90 ERF