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A SUPPORT SYSTEM FOR A 1750A VHSIC MULTIPROCESSOR

STEPHEN L. RUGGLES

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Langley Research Center
Hampton, Virginia 23665

SUPPORT SYSTEM FOR A 1750A VHSIC MICROPROCESSOR

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INTRODUCTION

NASA Langley Research Center is presently conducting research in very high-speed integrated circuit (VHSIC) microprocessors and multiprocessors to investigate the potential for insertion of VHSIC components into future NASA missions. As a part of these studies, NASA Langley has purchased a Brassboard VHSIC Processor (BBVP) which utilizes the MIL-STD-1750A Instruction Set Architecture. The BBVP was purchased with the intention of making comparative studies of VHSIC processors.

To operate the BBVP, a support system is required. The minimum support system involved consists of a DC power source to handle the power requirement, a means to control temperature, circuitry to interface the processor with a host computer, and mechanical structure to house the BBVP.

The objective of this report is to describe the support system, which was fabricated to functionally test and evaluate the BBVP. This report will describe a hardware design and implementation approach to meet the power and temperature requirement for the support system. A functional description of the interface circuitry and mechanical structure to form a complete support system will also be discussed.

The use of brand or trade names in this report is for completeness and does not imply NASA endorsement.

SUPPORT SYSTEM OVERVIEW

The support system organization which would satisfy a working system to functionally test and evaluate the BBVP is shown in Figure 1. The major subsystems which make up the support system are: the Power Supply Unit (PSU), the Temperature Controller Unit (TCU), an Input/Output Module (I/O module), and the Test Fixture (TF). Each one of these subsystems functions as an integral part of the overall system.

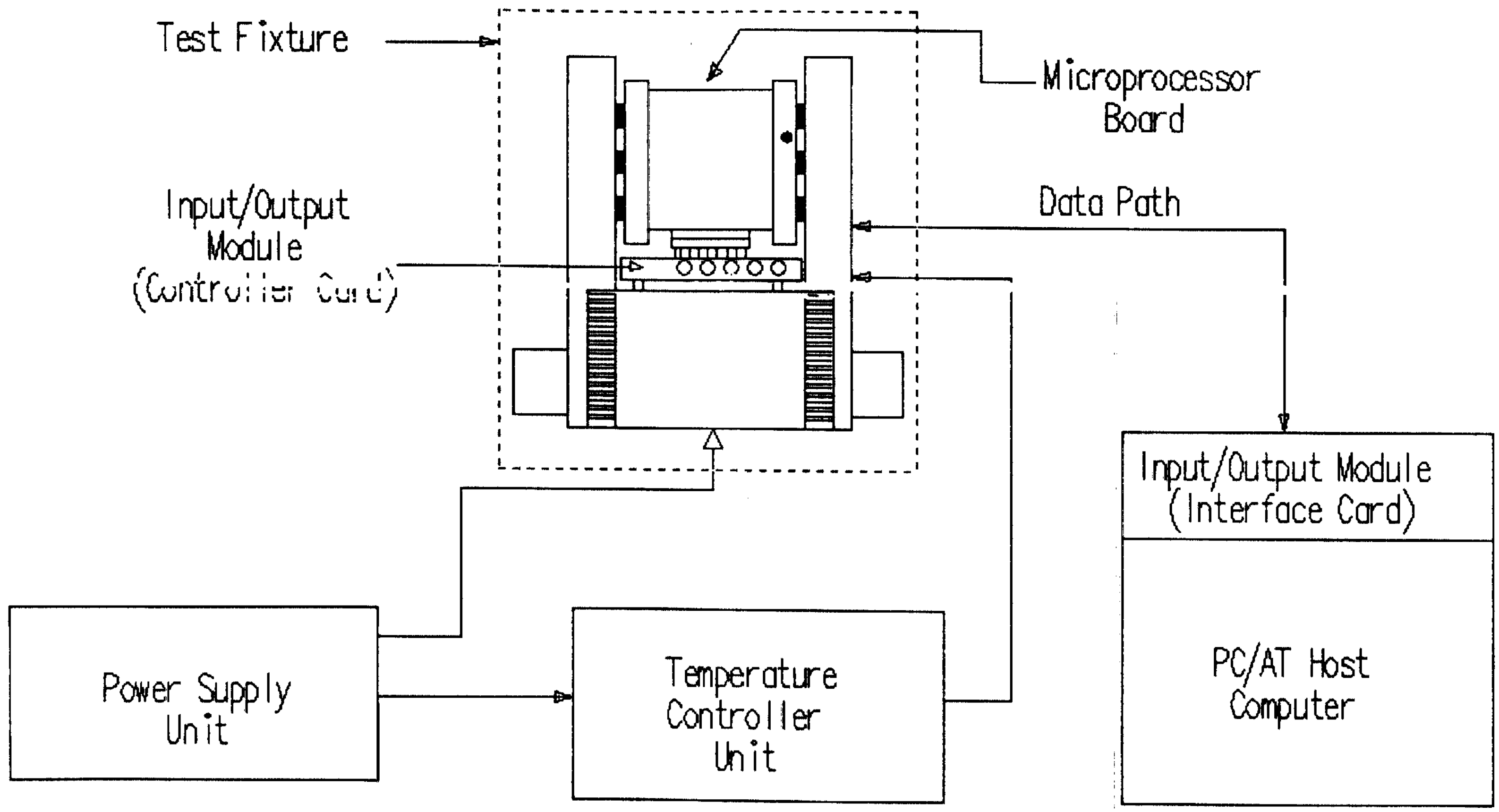


FIGURE 1. Block diagram of the support system

The Power Supply Unit (PSU) provides DC power to the BBVP, the I/O module (controller card), and the TCU. The manufacturer of the BBVP and designer of the I/O module has given power source requirements which consist of high currents and low voltages. These specifications require three separate voltages +2.0v, +3.3v, and +5.0v to be regulated within 10 percent under varying load conditions while providing large current capability. The specifications are met by selecting power sources which could deliver the required current and by designing and implementing voltage regulation circuits to maintain stable voltages. Voltage limitation circuits were also employed for an added measure of safety. The power sources for the TCU are off-the-shelf power supplies. These power supplies were selected by incorporating standard voltages into the design of the TCU's components.

The average expected power dissipation of the BBVP is 45 watts with a worst case of 75 watts. This much power dissipation requires the BBVP to be cooled (approximately ambient temperature) to insure proper operation. To maintain the BBVP within +/- 5 percent of ambient temperature, a TCU is required. The TCU monitors and controls the temperature of a cold plate which absorbs heat dissipated by the BBVP.

The TCU is composed of two identical temperature control systems, one for each cold plate on either side of the symmetrically constructed test fixture. Each system functions independently to control the temperature of its respective cold plate. Each temperature control system consists of a temperature control circuit, which controls thermoelectric coolers, and a muffle fan. A solid state temperature sensor, calibrated in millivolts per degree Kelvin, is used to detect temperature.

A design for the I/O module was acquired from the BBVP vendor and an implementation of this design was completed in-house. The I/O module provides for the control and exchange of data between host computer and the BBVP. Major functions of this I/O module are: control and timing, bus communication, data buffering, and error detection. The control circuitry regulates the flow of data on the bus lines between the host computer and BBVP. The I/O module generates timing sequences (clocks) to synchronize incoming data and the data buffered for short-term storage. Error detection is employed to give the user the status of the BBVP. A brief description of this I/O module is presented in the Support System Component Designs Provided By Vendor section.

The TF (chassis) was implemented in-house from a design acquired from the vendor of the BBVP. The TF is a mechanical structure constructed of anodized fined aluminum members. It is a free-standing assembly which provides a physical means of attaching electronic hardware. The TF assembly functions are similar to the functions of a card cage assembly. The TF permits one card (the BBVP) to be inserted into a backplane (the I/O module). The composition and design of the TF provides heat exchanging capabilities which helps satisfy the BBVP temperature constraints. A brief description of the TF is described in further detail in the Support System Component Designs Provided By Vendor section.

SUPPORT SYSTEM DESIGNS DEVELOPED IN-HOUSE

Power Supply Unit

The Power Supply Unit (PSU) design is shown in Figure 3. Four DC power supplies with six separate outputs are incorporated into the design of the PSU. Power supplies labeled PS1, PS2, and PS4 are single output supplies, while PS3 is a triple output supply. The outputs from PS1, PS2, and the +5V output of PS3 supplies are cascaded to an electronic circuit board. The electronic circuit design is employed for voltage regulation and voltage limiting on each of the three outputs powering the BBVP and I/O module. The other two outputs of power supply PS3 and PS4, which do not require regulation, supply power to the TCU.

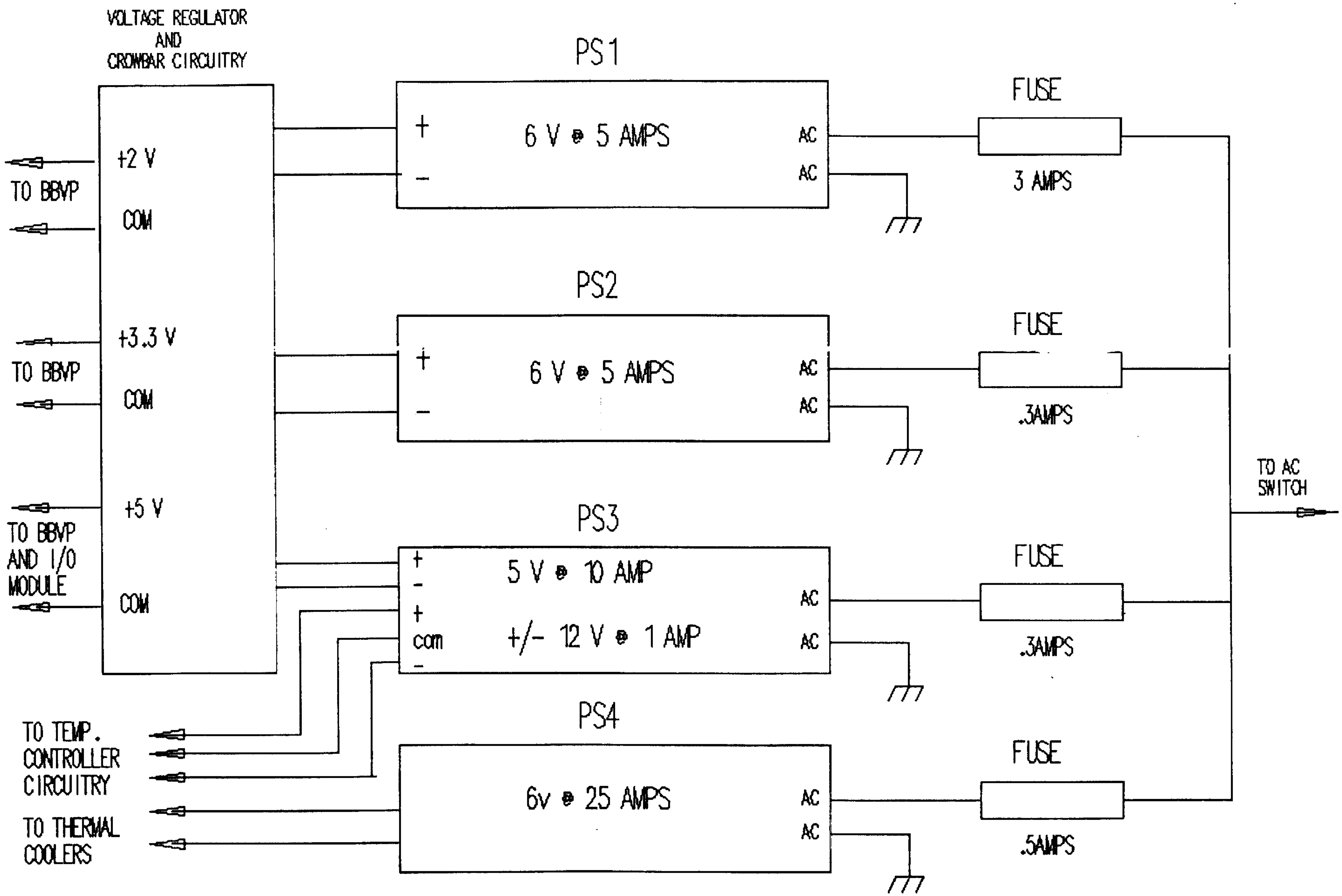


FIGURE 3. Power Supply Unit

Power requirements for the BBVP and I/O module are given in Table 1. The specifications given require the +2, +3.3, and +5 voltages to be regulated to within +/- ten percent (10 %) under varying load conditions while providing large current capability.

Power supplies PS1 and PS2 have a DC output rating of +6 volts, 5 amps which are regulated to meet the +2 and +3.3 volts specification. These two power supplies provide 30 watts each which is more than adequate for the required DC power. The +5 volt output of PS3, which is internally regulated, has a DC output voltage and current rating of: +5 volts, 10 amps. The 5 volts, 10 amps supply provides 50 watts of power which is sufficient for the 5 volts, 5.5 amps requirement.

To maintain precision voltages under varying loads, a voltage regulator was employed on the outputs of PS1 and PS2 to regulate these power supplies to +2V and +3.3V respectively. The LM 350 voltage regulator was chosen because it features an adjustable output voltage (1.2V-33V). Further, both line regulation and load regulation are comparable to discrete designs.[1] The three terminal device is easy to use and requires only two external resistors (to adjust the output voltage), R1 and R2 as shown in Figure 4.

In normal operation, the device develops a voltage of 1.25 volts between the output and adjustment terminals, referred to as a voltage reference (Vref). This constant voltage is established across a fixed resistance R1 producing a constant current I1, which flows through R1 and R2. The output voltage Vout is determined by

$$V_{out} = V_{ref} (1 + R2/R1) + I_{adj} R2.$$

Iadj represents a small error term typically 50 microamps, which is inherent to the device. The design of the device minimizes the Iadj term for varying line voltages and load changes.

For further safety of overvoltage transients or regulator failures, a "crowbar" voltage limiting protection circuit was employed in conjunction with the voltage regulator. This

TABLE 1

POWER

BBVP	+2V +/- 10% @ 7.8A MAX.
BBVP	3.3V +/- 10% @ 6.7A MAX.
BBVP & I/O	+5V +/- 10% @ 5.5A MAX.

DISSIPATION

TYPICAL	45 WATTS
WORST CASE	75 WATTS

BBVP AND I/O MODULE POWER REQUIREMENT

VOLTAGE SELECTION

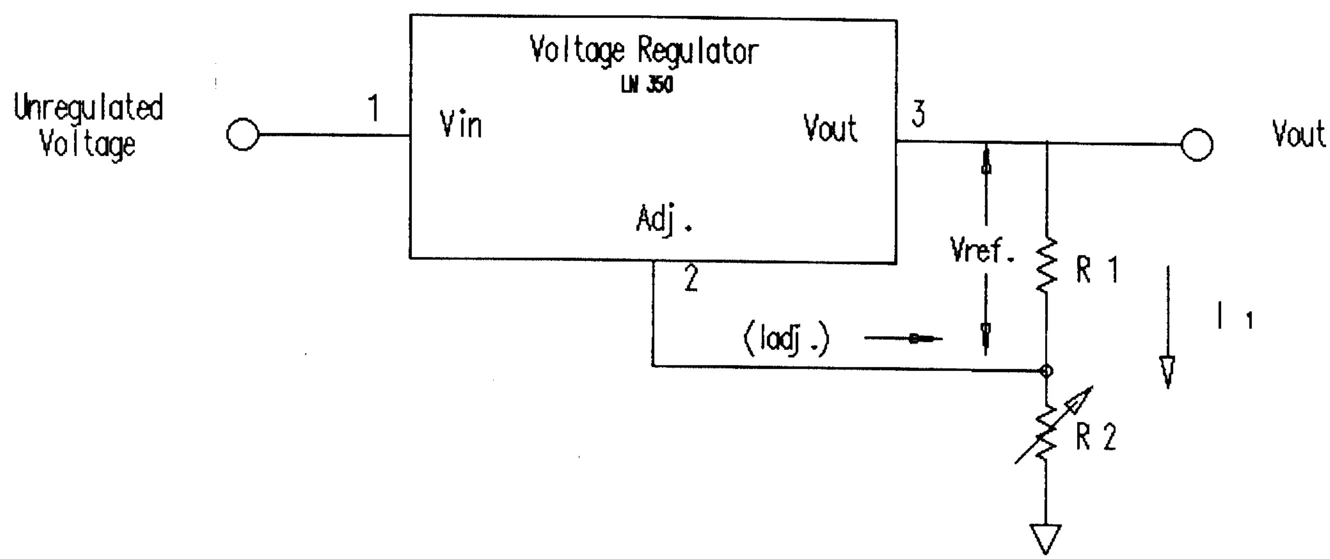


FIGURE 4

circuit monitors the output of the power supply and instantaneously throws a low resistance across the output terminals of the power supply whenever the voltage exceeds a predetermined voltage threshold.

The "crowbar" circuit design, shown in Figure 5, has an overvoltage sensing network and utilizes the characteristics of a silicon controlled rectifier (SCR). The overvoltage sensing network monitors the output voltage of the power supply or in this case, the voltage regulator, and determines a threshold voltage by varying R1. In this case, the threshold voltage is 10 percent over the output voltage of the voltage regulator. If the threshold voltage is exceeded, a sufficient amount of SCR gate current (Igate) will flow and drive the SCR into its conduction region. The SCR when turned on acts as a low impedance path across the supply voltage. This means the output current of the supply will flow through the SCR and limit the supply voltage (less than one volt) across the SCR. The "crowbar" circuit will stay in this state, protecting the circuits on the output, until the power supply is shut down.

The configuration for cascading the voltage regulator circuit with the crowbar circuit is shown in Figure 6 for the +2, +3.3, and the crowbar circuit for the +5 voltage supplies. These circuits were tested under simulated loads and met all requirements.

To complete the PSU design, three voltage sources were used to implement the TCU's power requirements. As shown in Figure 3, power supplies PS3 and PS4 provide the power sources for the TCU. The +12 and -12 volt output of PS3, each capable of delivering 1 ampere, were used for the TCU's temperature control circuits. Power supply PS4 has an output rating of 5 volts at 25 amps, which supplies a maximum of 125 watts to the TCU's thermoelectric coolers. The design requirement for 125 watts is determined by the amount of heat each thermoelectric cooler would have to absorb from the dissipated heat of the BBVP to maintain the BBVP at ambient temperature. The design analysis of the power requirement for the thermoelectric coolers is discussed in the TCU section.

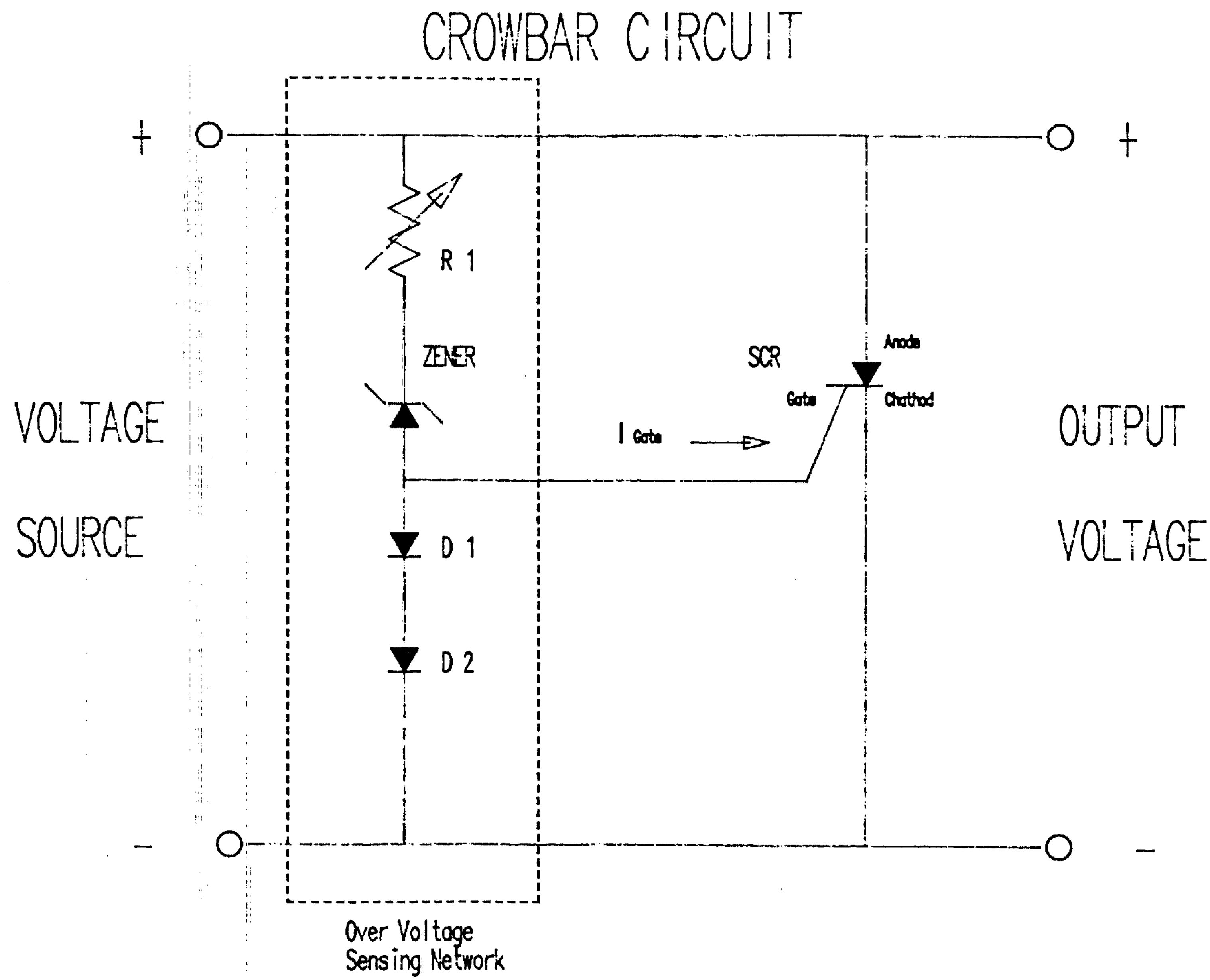

CROWBAR CIRCUIT
+
VOLTAGE
SOURCE
-
R 1
ZENER
D 1
D 2
Over Voltage
Sensing Network
SCR
Anode
Gate
Chathod
I Gate
+
OUTPUT
VOLTAGE
-

FIGURE 5

VOLTAGE REGULATOR & CROWBAR CIRCUIT

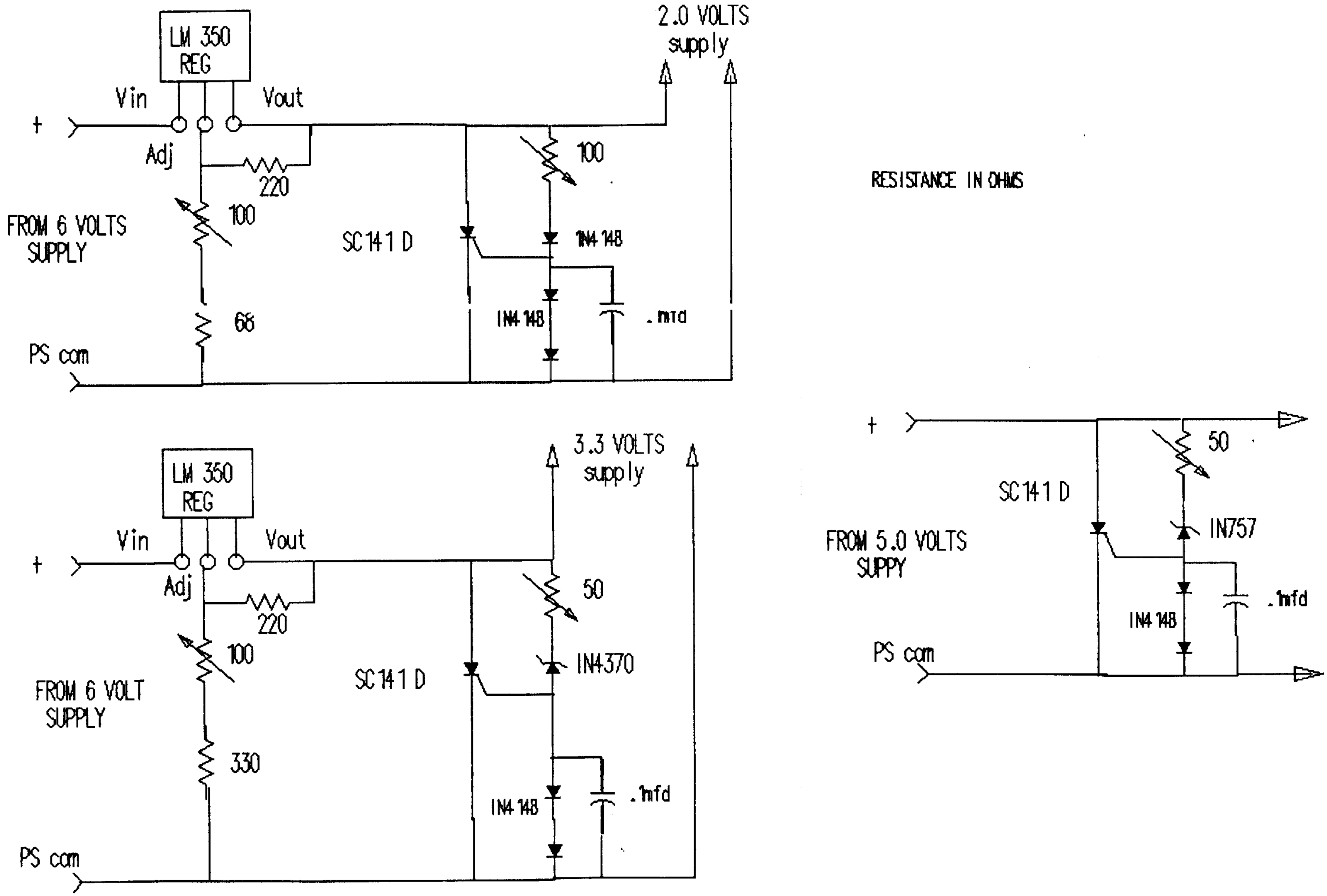


FIGURE 6

Temperature Controller Unit

The TCU is composed of dual temperature control systems, one for each side of the symmetrically constructed test fixture. Each system has identical functions. The design of the temperature controller system, half of which is shown in Figure 7, contains three primary element: a temperature controller circuit, thermoelectric coolers, and a fan. The temperature controller circuit monitors the temperature of the card guide rail, which is attached to the test fixture. The card guide rail is thermally coupled to the BBVP, therefore the temperature of the BBVP and the card guide rail are approximately the same. The temperature controller circuit activates the thermoelectric coolers and a muffle fan to maintain the BBVP at ambient temperature.

The temperature controller circuit design is described in two stages. The schematic of the first stage, shown in Figure 8, consists of a solid state temperature sensor, a differential comparator network, and an integration unit. The controller functions in the following manner: a precision voltage reference source is connected to one half of a comparator circuit; this establishes a bias operating point equivalent to ambient temperature for one side of a differential comparator; the other input is connected to the terminal of a solid state sensor, a LM 135; the output from the sensor is scaled in millivolts per degree Kelvin. When a temperature swing in either direction occurs, the sensor responds accordingly. If the temperature is elevated above 25 degrees Centigrade, the sensor's output has a differential relation to the fixed voltage reference source connected to the adjacent input. When a differential of one millivolt or more is detected, the comparator thresholds.

When the sensor's voltage exceeds the threshold level setting of the comparator, its output produces a negative swing of 6 volts cutting off the transistor switch in the succeeding stage. As the second stage turns off, its output rises to power supply potential.

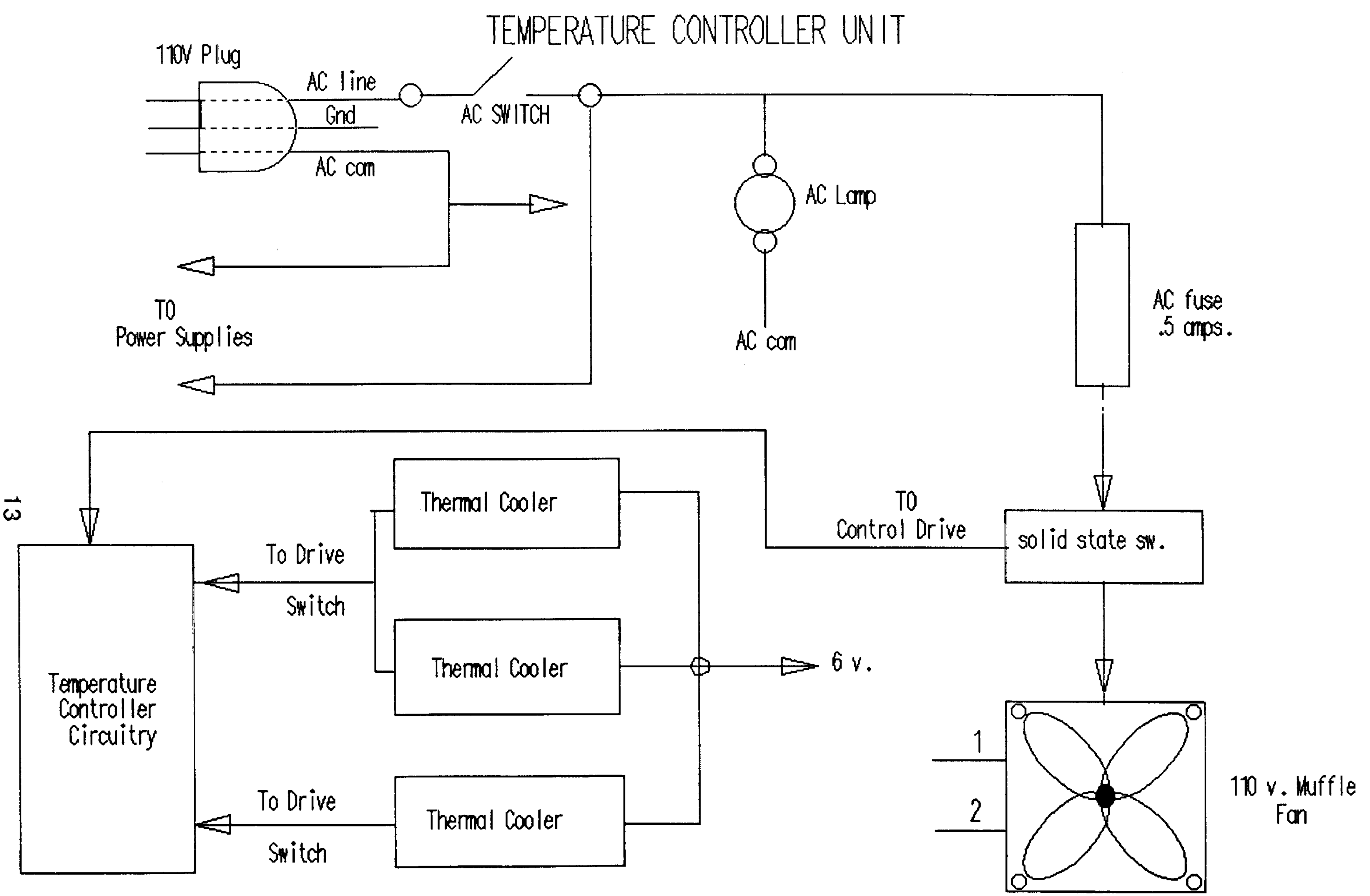
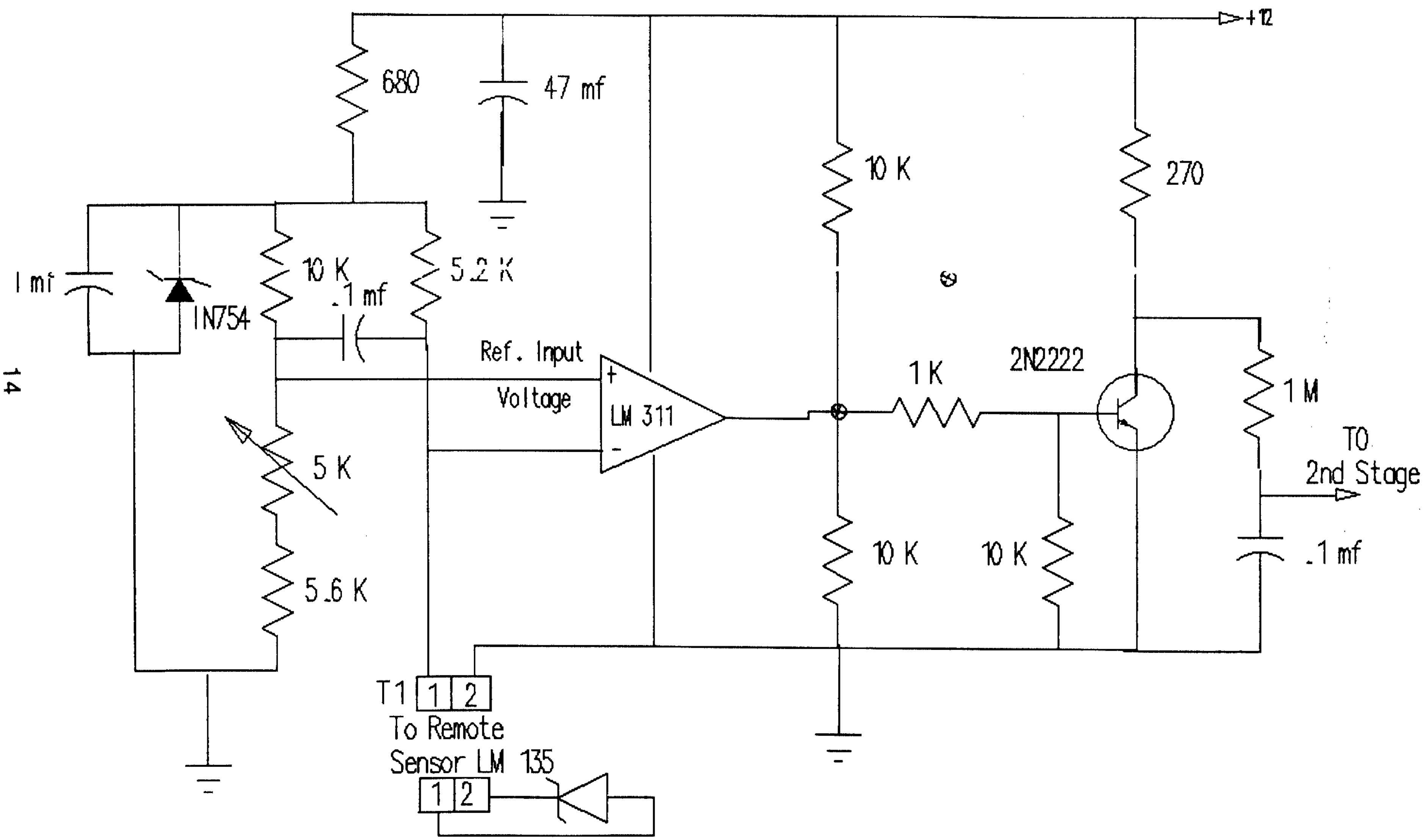


FIGURE 7

This diagram shows 1/2 of the TCU

FIGURE 8 FIRST STAGE OF TEMPERATURE CONTROLLER CIRCUITRY



Following the inverter stage is a RC time constant needed to dampen the comparator's response which occurs in a nanosecond time interval. The integrator's output is coupled to the input of two differential amplifiers in the second stage, shown in Figure 9. Each amplifier has an input source impedance of several megohms, thus eliminating any loading of the integrator which would distort its natural response. The integrator's output is also connected to a precision bias network in the second stage allowing a proportionate amount of control signal to be adjusted and maintained. This sets a zero crossing point for the differential amplifiers.

The schematic of the second stage, shown in Figure 9, consists of two differential amplifiers, one drives an optoisolator for an AC muffle fan control and the other drives two Darlington power switches to activate the thermoelectric coolers. The differential amplifier meets the need for high isolation to the integrator; however, its output current was limited, requiring a Darlington power switch to drive a thermoelectric cooler as opposed to a single bipolar switch driver. The LM 353 is a standard operational amplifier having a source current capability of 5 milliamperes. This amplifier provides adequate current to the optoisolator for fan control but does not provide enough drive current to the thermoelectric coolers.

To work within the differential amplifier's output current constraints, a Darlington configuration was designed in order to switch an adequate amount of power to be delivered to the thermoelectric coolers. A Darlington configuration is a two transistor circuit in which the collectors are tied together and the emitter of the first transistor is directly coupled to the base of the second transistor. This configuration is equivalent to a single transistor with a Beta equal to the Beta of the first transistor multiplied by the Beta of the second transistor B = B1XB2. This "Beta Squared" term means that the Darlington configuration can provide an increase in current gain, giving more power switching capability for the thermoelectric coolers than a single switching transistor.

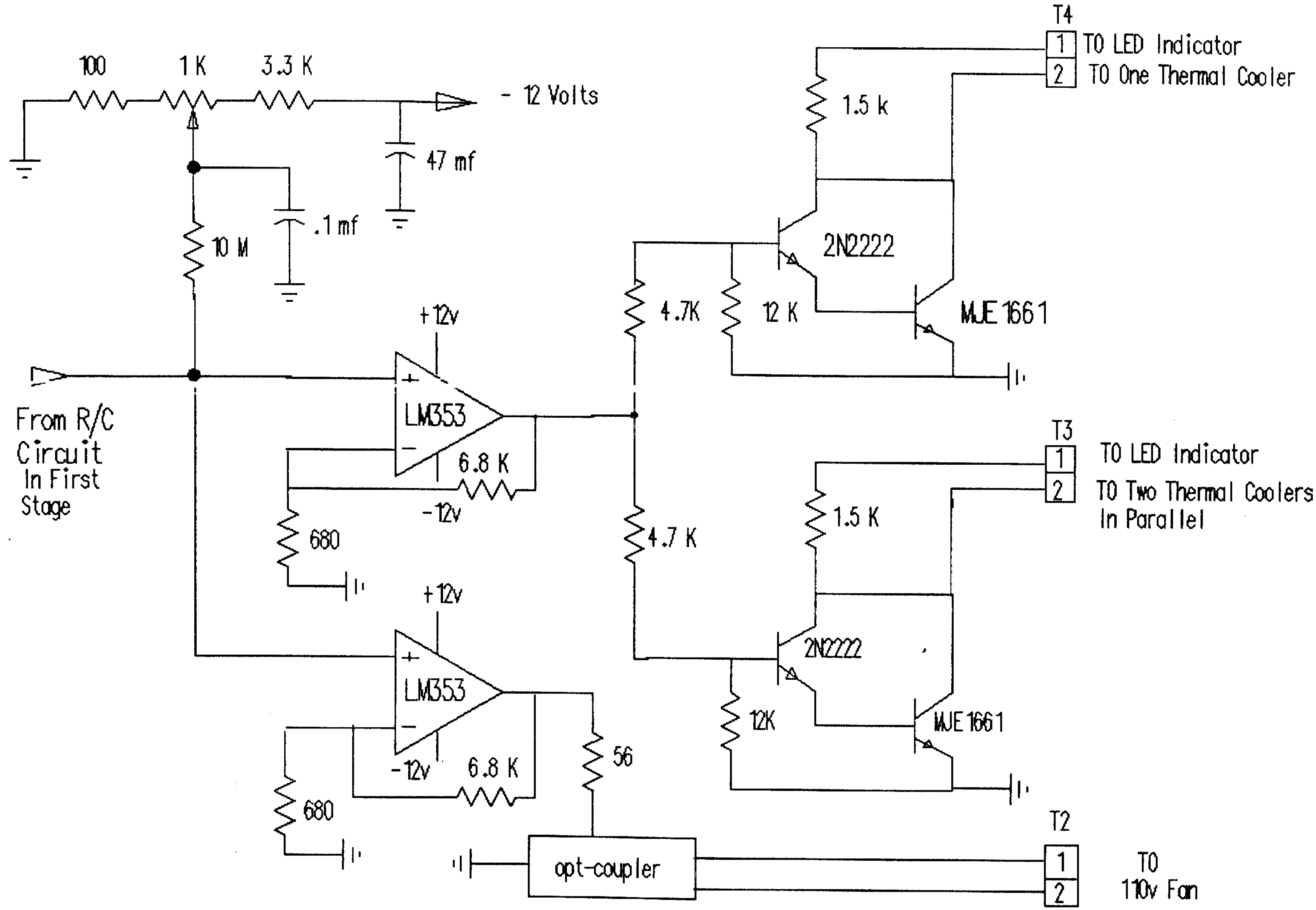


FIGURE 9. SECOND STAGE OF TEMPERATURE CONTROLLER CIRCUITRY

A thermoelectric cooler is a solid state device incorporating a group of diodes that are connected in series. The diodes are sandwiched in a metal embodiment with one of its metal plates acting as a sink to remove both the elevated temperature of the microprocessor card and the temperature generated as result of biasing the diodes. The other metal plate interfaces to the body which is to be cooled. To achieve differential cooling, both metal bodies must be thermally isolated from each other, otherwise both plates become heat radiators and no cooling is achieved. When the device is operated in a reversed biased manner, it has the capability of absorbing heat. The trade off for this heat absorbing characteristic is the power required to operate the device.

The operating parameters for the thermoelectric coolers and selection of transistors for the Darlington power switches in the second stage were determined from manufacturer's specifications. Shown by the dotted lines in Figure 10, a thermal response needed to maintain the thermal gradients of the BBVP to a 25 degree Centigrade position (dT) would require the solid state coolers to be biased at a potential ranging from 5 to 6 volts. At these potentials the current would be expected to be 3.57 amperes. To operate the cold junction at this thermal gradient would require an input power between 17.85 watts and 21.42 watts. Each thermoelectric cooler would pump out or absorb 13 watts of power, as shown in Figure 10. This value was determined by extrapolation of the "heat wattage" Q between variables 12 and 14. Once the Q is determined, a line is then drawn on the manufacture's data sheet to intersect the voltage point below.

The average expected power dissipation of the BBVP is 45 watts with a maximum of 75 watts. Assuming the BBVP dissipates the maximum power of 75 watts and that each thermoelectric cooler absorbs 12.5 watts (Q), then 6 coolers would be required to absorb a total of 75 watts. Six MI 1063T thermoelectric coolers were selected for the design of the TCU, three mounted on either side of the test fixture.

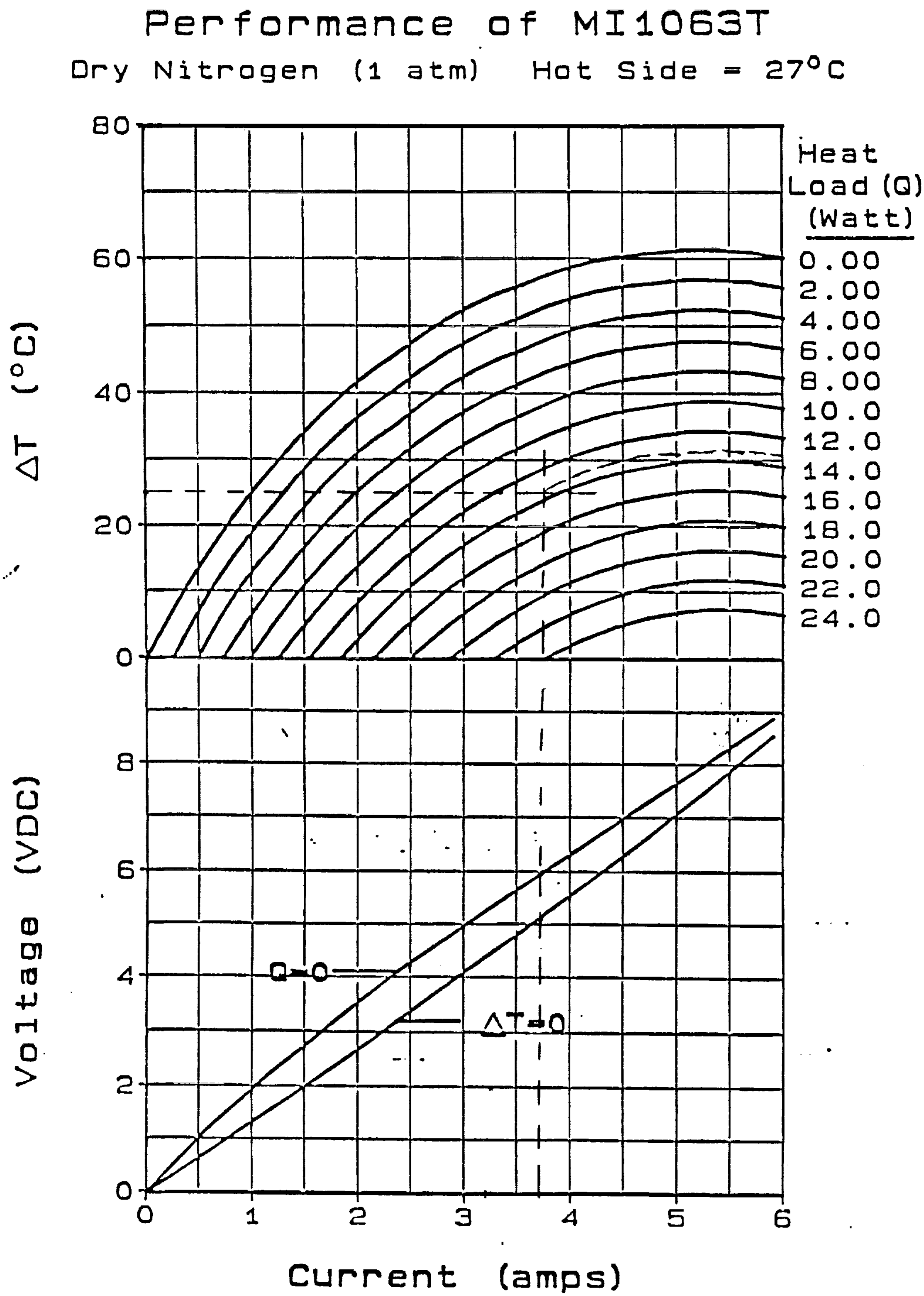

Performance of MI1063T
Dry Nitrogen (1 atm) Hot Side = 27°C
Heat Load (Q) (Watt)
0.00
2.00
4.00
6.00
8.00
10.0
12.0
14.0
16.0
18.0
20.0
22.0
24.0
ΔT (°C)
80
60
40
20
0
Voltage (VDC)
8
6
4
2
0
Q=0
ΔT=0
0
1
2
3
4
5
6
Current (amps)

FIGURE 10

In order for each thermoelectric cooler to absorb 12.5 watts and maintain a thermal gradient of 25 degrees centigrade demands an operating potential of 5 volts. At this potential each cooler would draw 3.5 amperes. The combined input power for the 6 coolers would be 105 watts. A DC power supply rated at 5 volts, 25 amps was selected to power the 6 thermoelectric coolers. This power supply provides up to 125 watts and is an integral part of the PSU.

If each thermoelectric cooler operates at 3.5 amperes, then the 3 coolers controlled by the temperature control circuit require a total of 10.5 amperes. To satisfy the current demand imposed by the thermoelectric coolers, a NPN power transistor switch (MJE1661) having a current capability of 10 amperes was selected for the output side of the Darlington configuration, while the driver transistor could be any NPN transistor having moderate gain and current capability (2N2222).

Due to the current demand of the coolers, two of the coolers were connected together in a parallel arrangement and controlled by one power switch. The remaining cooler was controlled by a separate power switch. This ensured that one power switch was not switching the total amount of current.

The Darlington power switches are shown in the output of the second stage in Figure 9. These switches were implemented with a 2N2222 transistor to drive a MJE1661 NPN power transistor. This combination delivered the necessary current to the coolers while maintaining a saturation resistance of .5 ohms or less.

The layout and artwork shown in Figure 11 was processed for a printed circuit board from the first and second stage schematics of the temperature control circuit design. A completed printed circuit board of the temperature controller circuit design is shown in Figure 12.

A simulation test was performed to bound the expected temperature variation of the BBVP. This test utilized the TCU and a specialized test board to simulate the BBVP. The test board was built by placing a number of resistors onto a printed circuit board

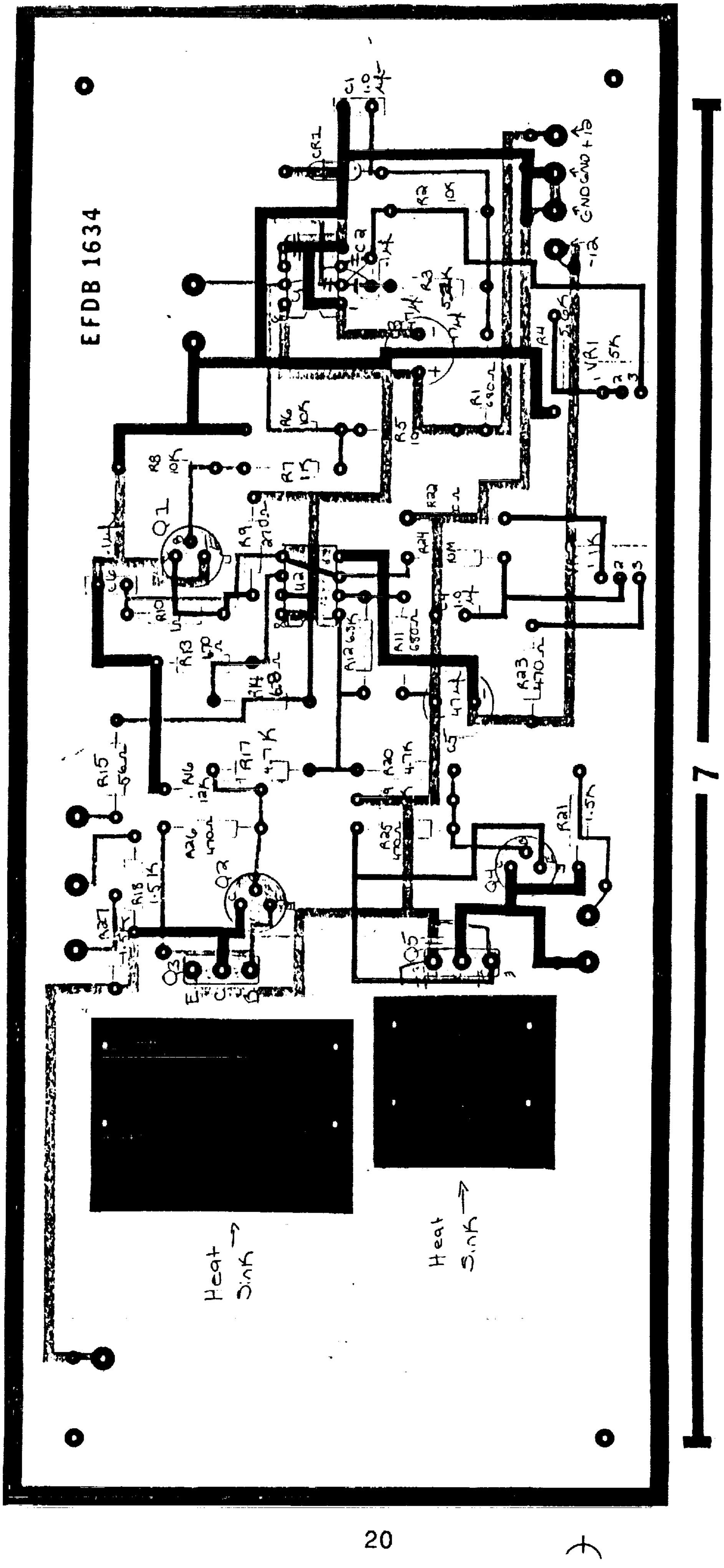


FIGURE 11

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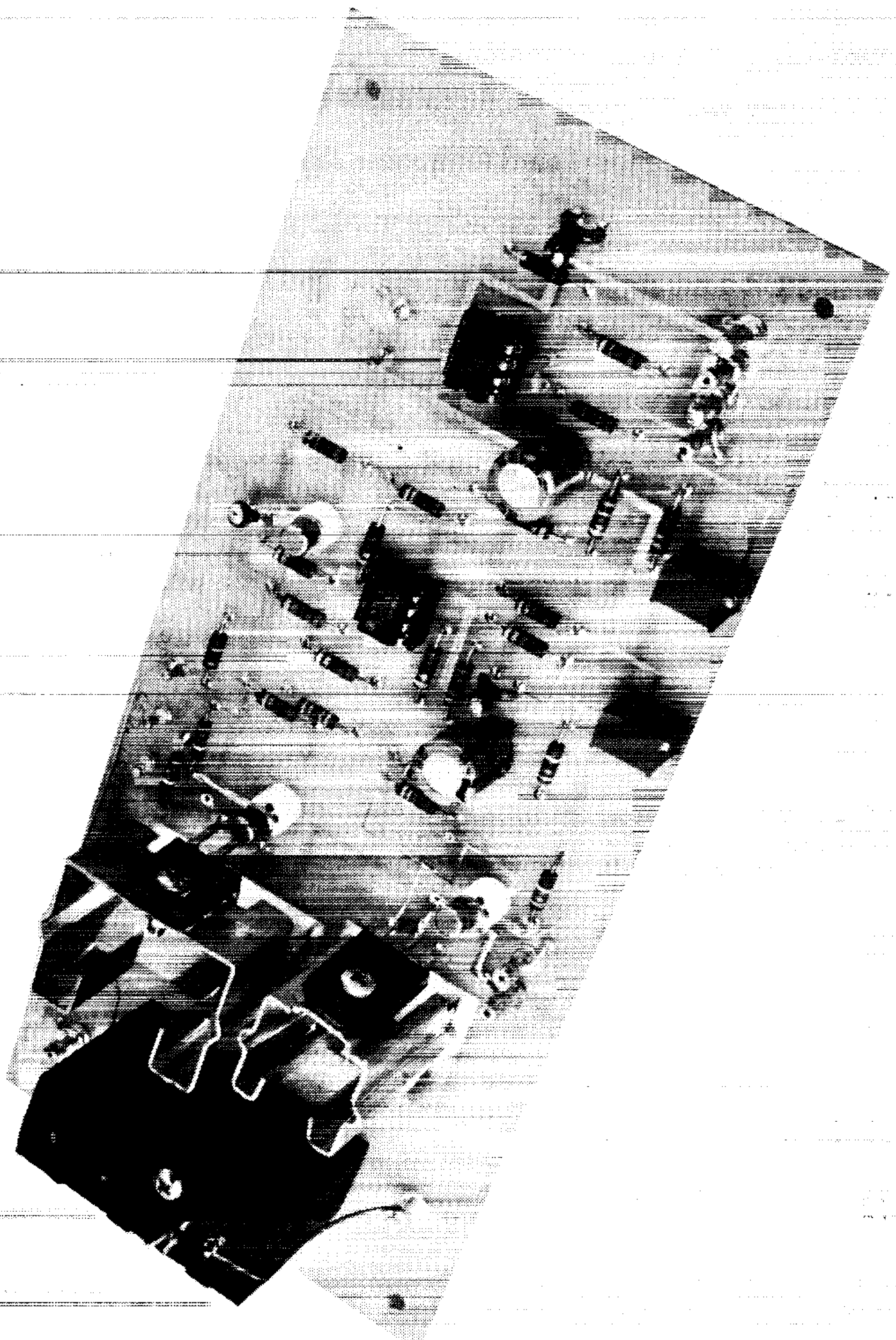

FIGURE 12

scaled in direct proportion to the BBVP's physical dimensions. Both sides of the test board were laminated with .032 inch copper clad material. The test board would simulate the heat path normally applied in the microprocessor design. The resistors were distributed on the copper laminated test board for a more realistic modeling of the distribution of integrated circuits employed on the actual microprocessor board. The resistors were connected in a parallel/series arrangement and an AC voltage could be applied to match the power consumption that would be applied in normal BBVP operation.

The simulation test was performed by adjusting the TCU's temperature control printed circuit boards to respond to temperatures above ambient temperature. The test consisted of setting a reference threshold voltage of 2.98 volts, which corresponds to an ambient temperature of 25 degrees Centigrade. The next step was to vary the power applied to the test board from 45 to 75 watts, the expected dissipated power of the BBVP. The temperature of the test board was monitored by a digital temperature meter.

The following two observations were made from this test: 1) The duty cycles of the muffle fans and thermoelectric coolers employed in the TCU increased with an increase in input power to the test board, and 2) The temperature of the test board initially moved above ambient temperature, as much as 3 to 5 degrees Celsius. The steady state response of the TCU would hold the temperature of the test board between 1 and 2 degrees Celsius above ambient temperature.

The results of these observations were: 1) The duty cycles of the fans and coolers were expected to change as the input power is varied. The design of the TCU took into account that the duty cycles could be as much as 100 percent. 2) The BBVP can function with small variations of temperature, therefore the initial fluctuation in temperature is not critical. The steady state temperature response is in acceptable limits.

SUPPORT SYSTEM COMPONENT DESIGNS PROVIDED BY VENDOR

Input/Output Module

The I/O module is needed to operate and control the BBVP from a remote location. The network consists of two individual digital circuit boards. The first digital circuit board is commercially available. It supports data I/O transfer that is capable of servicing 96 input/output ports. A second digital circuit board is used to interface from the first board to the BBVP and provides the major functions of interfacing. Major functions, such as control and timing requirement, bus communication, and error detection, will be discussed in what follows.

The first board, the 96-channel I/O card, resides in the host computer. The I/O card consists of 4 general-purpose programmable I/O digital circuit devices with each having 24-channel capability. This card's main function is to allow communication between an 8-bit bus and a 16-bit bus. This is done first by selecting the desired option, read or write. When in "write" mode, the host computer is then sending data to the BBVP; this is accomplished by four successive "writes" to the I/O board. (Each of these "writes" are 8-bits wide giving a result of one 16-bit word: data and address.) After each pair of 8 bits are written, a clock signal is then transferred into the board. The clock signal is accomplished by selecting a different channel group and writing first a "1", then a "0", and then writing a "1" again, thereby creating a "clock". Data are read basically in the same manner. The address is written to the I/O board and data are read from a different port. This frees the host program from having to change the direction of each general-purpose I/O device; each port remains in "read" or "write" mode once programmed by the host.

The second digital circuit board, the controller board, is a "smart" backplane board for the BBVP. This board handles all of the basic synchronization requirements. It allows single stepping of either the System Memory Bus (SMB) or the System Bus (SB). The board gives a visual reading of the BBVP status as it is running. It also contains the necessary clock buffering stages to allow for distribution to the processor and the controller board.

The displays generated on the controller board are the current physical address (a 5-digit Hex Address), the data on the System Bus (4-digit hex display), and various status indicators for bus transactions and" Read/Write". To create the Hex displays, drivers are connected to the System Bus lines to drive Hex displays. The necessary decoding of the 4-bit binary to an alpha-numeric is built into the individual LEDs.

The synchronization of the incoming data is handled in the controller board but is based on the clock signals coming from the host computer. For isolation purposes, the controller board incorporates several data buffers. The data buffers also serve as a means of temporary storage, before the data is requested from the BBVP.

There are four different clocks utilized by both the controller card and the BBVP. The first clock, the system clock or "Clock-In", is generated from the main external clock. The second clock, the "S-Clock", is generated by taking the external clock, dividing by 2 and then putting it through a programmable delay line. The delay line allows for skewing of the system clock and switching times. The third clock signal, the "IA-Clock", is also derived from the divided by 2 signal, but goes through a longer programmable delay line; this gives two identical signals that are a few nanoseconds apart. The last clock signal, the "T-Clock", is a 100 KHz clock derived from an internal 10 MHz crystal oscillator. The "T-Clock" is utilized for timing sequences (timers) required by the Mil-Std-1750A Instruction Set Architecture specifications.

Test Fixture

The TF shown in Figure 13 is a mechanical structure which is designed for mounting the BBVP and I/O module (the controller board). It also serves as a heat sink to dissipate heat from the BBVP. The basic structure of the TF consists of the Connector

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TEST FIXTURE

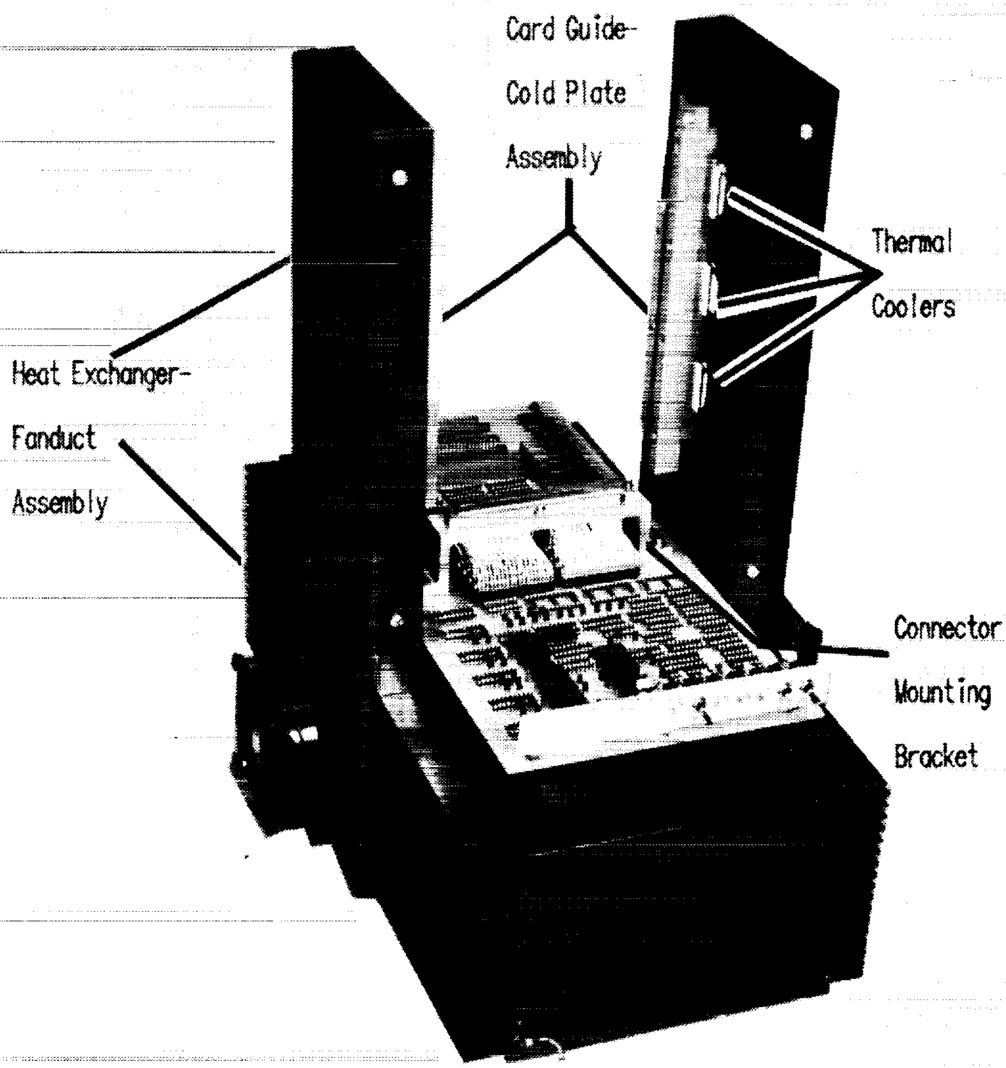

FIGURE 13

Mounting Bracket (CMB), the Card Guide-Cold Plate Assembly (CG-CPA), and Heat Exchange-Fanduct Assembly (HE-FA).

The CMB (Fig. 13) is machined from aluminum. Its purpose is to bridge a high-density connector (304 pin contact) across the I/O module thereby preventing damage to the I/O module. The connector is attached perpendicularly to the bracket by two machine screws. The bracket itself is fastened to the HE-FA (chassis). It is located transversely to and in the center of the I/O module, under the CG-CPA. The bracket offsets the connector from the I/O module with wires running from the contacts of the connector to contacts on the I/O module. Mounting the connector to a bracket in this fashion enables the connector to "bridge" the I/O module. There is considerable amount of insertion force placed on the I/O module when inserting the BBVP, the bracket provides a means to absorb this force, which is then distributed to the chassis, preventing the I/O module from being damaged.

The CG-CPA (Fig. 13) is used for alignment and to absorb heat from the BBVP. The BBVP has a high-density edge connector which plugs into the opposite gender connector attached to the CMB. With a high density connector of this sort, the alignment of the BBVP, with respect to the I/O module is critical. However, with the CG-CPA the BBVP can be guided into position, enabling the contacts of the connectors to be aligned properly.

The CG-CPA is machined from a rectangular piece of aluminum to form a channel bar. The width of the channel is greater than the thickness of the BBVP to allow for easy insertion of the BBVP, also to allow sufficient space for a "lok-tainer" to be attached to the inside of channel. A "lok-tainer" is a mechanical device which acts as a leaf spring and when tightened, clamps the BBVP into place after insertion.

The BBVP is a double-sided printed circuit board with a metal material in the core. This board design enables heat, which is generated by the BBVP, to be transferred to the metal core and the clamped edges by conduction.

The CG-CPA is mounted to the HE-FA with thermal coolers sandwiched between the two. These thermal coolers, when activated, produce a differential in temperature between the CG-CPA and HE-FDA with the cold junction being the CG-CPA. This configuration allows heat to be transferred by conduction from the metal core of the BBVP to the CG-CPA.

The HE-FA is a mechanical structure which serves as a chassis or base and a heat sink. The HE-FDA is made of an aluminum finned material shown in Figure 13. The picture shows the two longitudinal members with two aluminum plates as cross members attached at either end to form a rectangular base. At the center of each longitudinal member, another member is mounted perpendicular to the base with a sheet metal covering to form a duct. A muffle fan is attached at the foot of each duct to provide air-flow. This structure provides a foundation for mounting the CG-CPA, I/O module, and BBVP. It was discussed in the previous section that there existed a temperature differential between the HE-FDA and CG-CPA which the CG-CPA was the lower temperature side. The higher temperature side is the HE-FDA. To remove the heat from the HE-FDA, the fans mounted on the HE-FDA are activated, forcing cool air through the ducts, thus removing heat by convection.

CONCLUSION

A BBVP support system has been developed and fabricated. The system architecture provides for external support elements necessary to functionally operate and test a VHSIC 1750A microprocessor brassboard. The support system elements were the power supplies, the temperature control, the input/output interface, and the mechanical structure. Voltage control was emphasized in the power supplies for the brassboard, to prevent damage from varying loads and excess voltage. Temperature control was employed to maintain the brassboard at operational temperatures. An input/output interface technique was provided to communicate between the brassboard and a host computer. A mechanical structure was utilized to house the electronics and the brassboard. The elements which make up the support system provide for the laboratory testing of a VHSIC 1750A microprocessor brassboard under controlled conditions. The support system could be adapted to other processors via modification of the I/O Control Module.

REFERENCES

1. National Semiconductor Corp., " Linear Application Handbook," 1980.

APPENDIX

LIST OF ACRONYMS

CG-CPA	Card Guide - Cold Plate Assembly
CM	Connector Mounting Bracket
FET	Field-Effect Transistor
GVSC	Generic VHSIC Spaceborne Computer
HE-FA	Heat Exchanger - Fanduct Assembly
IBM	International Business Machines
I/O module	Input/Output Module
ISA	Instruction Set Architecture
PSU	Power Supply Unit
SCR	Silicon Controlled Rectifier
TCU	Temperature Controller Unit
TF	Test Fixture
BBVP	Brassboard VHSIC Processor
VHSIC	Very High Speed Integrated Circuits

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Stephen L. Ruggles	
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16. Abstract

This manuscript is to present a design approach for a support system or test station necessary to functionally operate a Very High-Speed Integrated Circuit (VHSIC) microprocessor brassboard. Major subsystems which make up the support are the following: (1) power supply unit, (2) temperature controller unit, (3) input/output module, and (4) mechanical test fixture. Theoretical analyses and experimental techniques were utilized to design and implement the power and temperature requirements for the VHSIC processor. A functional description of the input/output module and test fixture is discussed in the paper. The support system provides the means to evaluate and functionally test a VHSIC microprocessor.

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