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**Former Employee

† Managed by Martin Marietta Energy Systems, Inc., for the U.S. Department of Energy under contract DE-AC05-84OR21400

Custom Electronic Subsystems For The Laboratory Telerobotic Manipulator*

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ABSTRACT

The National Aeronautics and Space Administration (NASA) Space Station Program presents new opportunities for the application of telerobotic and robotic systems. The Laboratory Telerobotic Manipulator (LTM) is a highly advanced 7 degrees-of-freedom (DOF) telerobotic/robotic manipulator. It was developed and built for the Automation Technology Branch at NASA's Langley Research Center (LaRC) for work in research and to demonstrate ground-based telerobotic manipulator system hardware and software systems for future NASA applications in the hazardous environment of space. The LTM manipulator uses an embedded wiring design with all electronics, motor power, and control and communication cables passing through the pitch-yaw differential joints. This design requires the number of cables passing through the pitch/yaw joint to be kept to a minimum. To eliminate the cables needed to carry each pitch-yaw joint's sensor data to the VME control computers, a custom-embedded electronics package for each manipulator joint was developed. The electronics package collects and sends the joint's sensor data to the VME control computers over a fiber optic cable. The electronics package consist of five individual subsystems: the VME Link Processor, the Joint Processor and the Joint Processor power supply in the joint module, the fiber optics communications system, and the electronics and motor power cabling.

INTRODUCTION

The NASA Space Station Program presents new opportunities for the application of telerobotic and robotic systems in the hazardous environment of space. The Space Station Program will require a significant increase in extravehicular activity and the hazards associated with such activities. To reduce the extravehicular activity by humans during the construction and the maintenance of the space station, new research and development emphasis is being placed on teleoperation and robotic systems for space applications. The LTM was developed and built by Oak Ridge National Laboratory (ORNL) for the Automation Technology Branch at NASA's Langley Research Center (LaRC). LTM is being used at LaRC for research and to demonstrate ground-based telerobotic

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manipulator system hardware and software systems for future NASA applications in the hazardous environment of space.

LTM is a highly advanced, 7-DOF telerobotic/robotic manipulator system. LTM incorporates force transmission traction drives, joint modularity, redundant kinematics, state-of-the-art hardware, and software hierarchical control techniques. The LTM manipulators allow for robust, high-dexterity teleoperations and autonomous robotic operation [1].

LABORATORY TELEROBOTIC MANIPULATOR SYSTEM

The LTM system is designed for teleoperation and robotic operation with capabilities for future enhancements of both the hardware and the software systems. For teleoperation, the LTM system consists of right and left master/slave pairs of redundant kinematic manipulators. For robotic operation, the slave manipulators operate independently of the master manipulators and function as a single pair of robot manipulators with redundant kinematics.

Each manipulator consists of three 2-DOF (pitch-yaw) modules (shoulder, upper arm, forearm) connected together with "L" brackets to form a 6-DOF manipulator. The manipulator's seventh DOF is the wrist roll module attached to the forearm module. Attached to the master manipulator wrist roll module is the operator hand controller and attached to the slave manipulator wrist roll module is a motor-driven gripper.

The LTM computer system consists of two separated commercial, modular, multiprocessor VMEbus computer systems. One computer system controls the master manipulator pair. The second computer system controls the slave manipulator pair in either teleoperation or robotic operation (FIG. 1). Each computer system consisted of three Motorola single-board 68020 computers operating in parallel with a 16.67-MHz clock. A 1-MB global memory board is used for the shared data base. One computer board is used for system control and data communication between the VME computers and to and from the manipulators. The other two computer boards, one for each manipulator, run the manipulator control algorithms, safety checks, robotics, and electronic counterbalancing. The two VME computer systems swap the manipulators' data and system data at 250 Hz over a 10-Mbaud high-speed, serial fiber optics link [2].

The computer interface to the manipulator hardware is provided by an I/O board, A/D board, and D/A boards, and two link processor motherboards. The digital I/O board is used to monitor and control the pulse width modulation (PWM) motor drives. The A/D boards, one per manipulator pair, are for monitoring the system voltages and the manipulator motor current sensors. The D/A boards, one per manipulator, send the control signals to the joint motor PWM amplifiers. The link processor motherboards collect the joint module data (FIG. 2).

The LTM manipulator utilizes an embedded wiring design with all of the electronics power, motor power, and control and communication cables passing through each of the joint module pitch-yaw differential joints (FIG. 3). The cable design eliminates cables and connectors outside the manipulator framework. Because of the limited mechanical size of the joint module, the LTM design requires that the number of cables passing through each of the pitch/yaw joints of the module be minimized. To eliminate those cables required to carry the pitch-yaw joint sensor and control data to the VME control computer system, a custom-embedded electronics data collection package for the manipulator joint modules was developed.

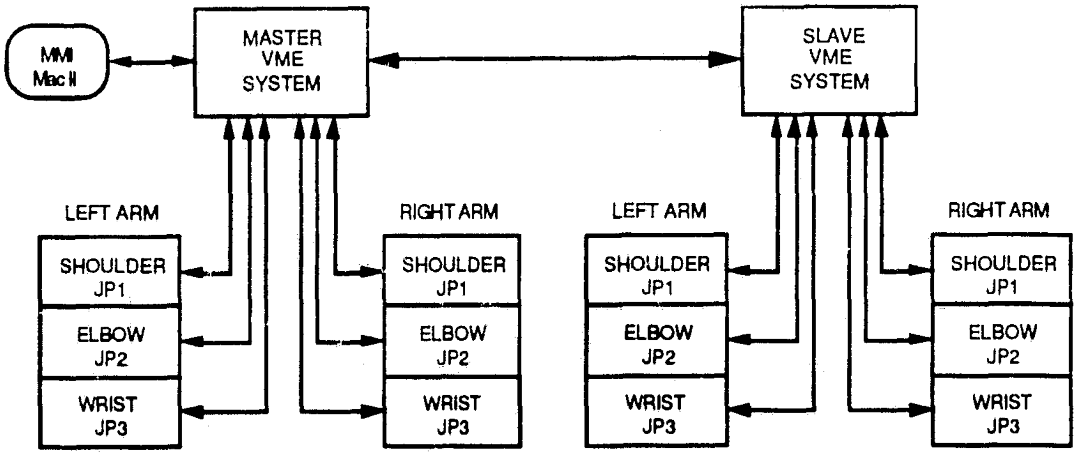

FIG. 1. The LTM block diagram.

The electronics package collects and packages the joint module sensor data and sends the data packet to the VME control computer over a single, fiber optic line. The electronic package also sends command packets from the computer system to the joint module over the same fiber optic line. The electronics package for the joint modules consists of five individual subsystems: the Link Processor (LP) on a VME motherboard, the Joint Processor logic (JPl) and the Joint Processor power supply (JPp) in the joint module, the fiber optic communications system, and the electronics and motor power cabling.

The LTM manipulator consists of two types of joint module sizes: a large joint module for the shoulder and elbow on the slave manipulator, and a smaller size for the other joint modules used in the master and slave manipulators. The electronics packages are identical for each of the joint modules of the manipulators except in one detail. The velocity filters for the resolver-to-digital convertors for the JPls in the the large joint module differ from the filter circuits in the small joint modules. The reason for this difference is the lower geardrive ratio for the large joint module. The filters consist of discrete resistors and capacitors for the converters and can be easily changed. Therefore, any component of the electronics package, except the JPl, can be moved to any location within the manipulator system, and any JPl may be moved to any joint module that has the same converter filters.

LINK PROCESSOR

The LP is the interface between the VME computer system and a joint module. The LP is a single-circuit module that plugs into a VMEbus motherboard with an 80-pin connector. The motherboard provides the address decoding and the data bus between the VMEbus and each of the three LP modules, one LP for each of the manipulator joint modules. There is a separate motherboard for each of the manipulator arms.

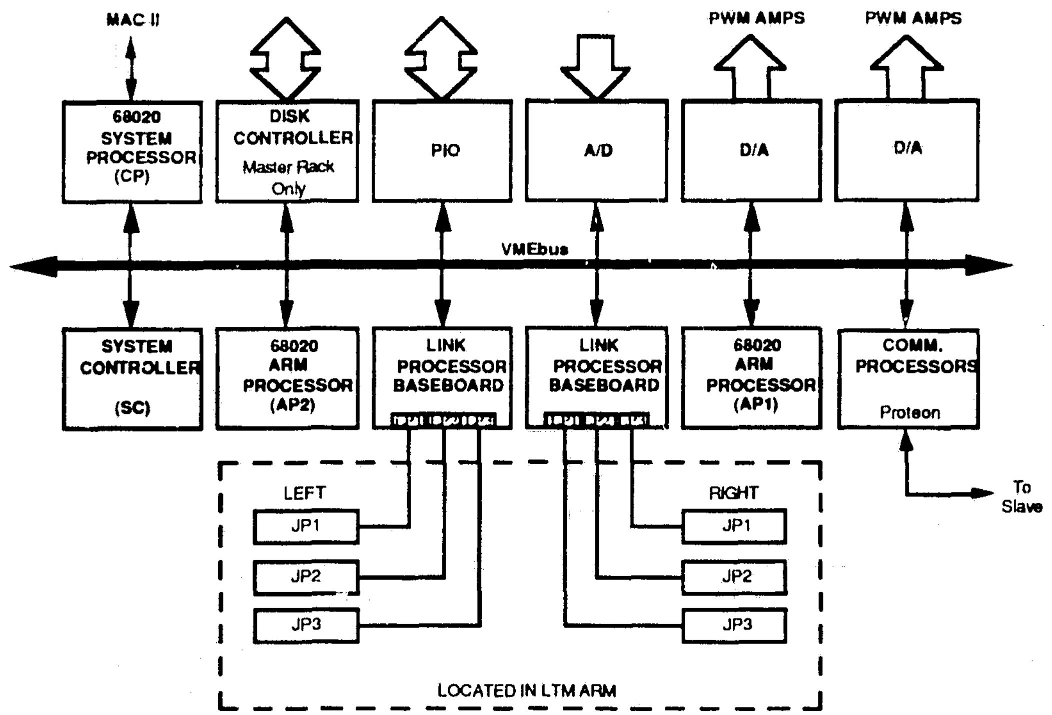

FIG. 2. The LTM board level block diagram.

The LP module is a 2- by 4-in., 4-layer, double-sided printed circuit board with 15 surface-mounted device (SMD) chips and a pin gate array (PGA) dual-port RAM chip. The VME computer system communicates with the LP through the 4 KB of memory-mapped dual-port RAM, IDT7133L70G. The microprocessor used on the LP is the Intel N80C196KA microcontroller operating with a 10-MHz clock. The microcontroller has a 16-bit multiplexed data and address bus, high-speed I/O pins, and an RS-232 port. The LP system has 16 KB of PROM, N27C64, which contains the startup and the communication code. There are 16 KB of SRAM, IDT7164L, which holds the application code that is downloaded from the VME system at LP startup or restart. The LP board address decoding is provided with an Altera EP600LC programmable logic array chip. Communication with the JPI via the fiber optics link is controlled by an Intel N82588, a 2-Mbaud local area network controller chip, using a 16-MHz crystal. Using the Maxim MAX232 chip and the microprocessor RS-232 port, the LP is provided with RS-232 for direct serial communications for debugging the LP independently of the VME interface. Other support chips on the LP include the data and address line buffers, 74HC373 and 74HC245, and the system reset circuit with a reset button on the front of the LP motherboard.

The startup and communication code is the same on the LP as that on the JPI [3]. The startup code is used to bring the LP on-line with the VME computer, then the LP is used to bootstrap the JPI. The LP application program is downloaded to the LP from the VME system after LP startup or reset. The application program can be changed at any time to meet any new requirements for LP. The LP application program is used to request, collect, sort, store, and perform safety checks on the data from the JPI. To collect the joint module data, the LP sends a request to the JPI for joint data and after receiving and sorting the joint data, the LP passes the data to the VME system via the memory-mapped dual-port RAM. The LP sends the data

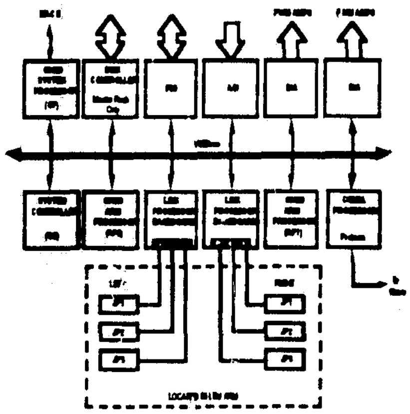

FIG. 3. The LTM electronics and placement.

request commands every 1.6 ms asynchronous to the VME system operation of 4 ms. The LP also passes commands from the VME system to the JPl.

The LP fiber optic transceiver module is mounted on a separate circuit board and is connected to each of the LPs with a cable. The cable connects the communications chip, the Intel N82588, directly to the differential driver and receiver chip, SN75179BD. The differential driver output is connected to the current driver circuit, which powers the LED transmitter in the transceiver module. The transceiver optical receiver detector is connected to the differential receiver. A detailed discussion of the complete transceiver is given later in this paper.

JOINT PROCESSOR

The data acquisition module in each joint module consists of two circuit boards. One board, the JPl, contains the computer and I/O systems, and the other board is the JPl power supply, JPp. Each board is mounted in the joint module inside its own metal container with a removable cover for access. The containers are used to shield the circuit boards from electromagnetic noise of the motor power during joint operation. The two containers are mounted in spaces next to the drive motors of the joint module.

The JPl is the data collection board for the LP-JPl pair for each joint module. The JPl basic computer and communication systems are the same as that on the LP. The JPl uses the same chip devices for the following functions: 16-bit microprocessor, 16 KB of PROM and SRAM, buffer and RS-232 chips, and the fiber optic communication chips. The PROM contains the same startup and communication code as the LP. The SRAM holds the JPl application program, which is downloaded from the VME system via the LP at system startup or reset. The communication system for the JPl is the same as that on the LP system. The JPl collects the joint module data and sends these data to the LP when requested by the LP. The data collected by the JPl consist of the joint module pitch and yaw position and velocity, and the velocity, torque, position, and temperatures of the motors. The JPl for the wrist joint also collects data from the wrist roll position. For the master manipulator, the wrist JPl collects the master grip commands. The

JPl also carries out commands from the VME system, such as locking and unlocking the brakes.

The JPl is a 2- by 7-in., 8-plane double-sided printed circuit board with a total of 39 SMD chips mounted on both sides of the board. The JPl uses the equivalent cpu, RAM, PROM, PAL, communication chips, and startup software as the LP. Five of the eight circuit board planes carry for the digital signals between the JPl devices. Two planes are dedicated for power, one for the +5 VDC and another for the +/-12 VDC. Between the two power planes, the digital and the analog ground plane is sandwiched. The two grounds are tied together at the two analog-to-digital converter ground connection pins. The power and ground planes are not solid planes but are configured in a grid pattern to allow the printed circuit board to flex. The analog signals to the analog-to-digital converters are embedded within the ground plane to shield the analog signals from the noisy digital lines.

The JPl has five resolver-to-digital (R/D), 16-bit, type-II tracking converter chips, Analog Devices AD2S82JP, with analog velocity outputs. Two R/Ds are used for each of the pitch and yaw resolvers and one R/D is used for the wrist roll resolver. The pitch and yaw resolvers are two-speed (X1 and X16) resolvers from Vernitron Corporation. The reference frequency to the primary winding is 2-KHz 7.5-Vrms signals and is supplied by the JPp board. The upper 4 bits from the 16-bit word of the X1 winding R/D are used to give the correct sector out of the 16 sectors that the resolver rotor can be located. The upper 12-bits from the 16-bit word of the X16 winding R/D are combined with the 4 bits of the X1 to give an accurate 16-bit position of the joint. Each R/D is tuned for its resolver and resolver winding. The tuning circuits are discrete resistors and capacitors, not SMD devices, to allow rapid and easy retuning of the R/D circuits.

The JPl has two encoder chips, THCT2000FN from Texas Instruments, one for each motor encoder. The two quadrature phase signals, A and B, from the motor encoder controls the count direction of the 16-bit counter. The motor encoder generates 512 A and B pulse pairs per motor revolution, but the encoder chip will generate 4 counts per pulse pair for 2048 counts per motor revolution.

The joint module contains a torque sensor between the output of the motor gear reducer and the input preload mechanisms for each motor. The torque sensor reference voltage is +/-5VDC and is supplied from the JPp board. There is a high-gain instrumentation amplifier for each of the torque sensors. The amplifiers are Analog Devices AD524CE instrumentation amplifiers and are set to a fixed gain value with a single resistor. The amplifier output voltage can be nulled to zero output voltage for a zero input voltage with a potentiometer.

The JPl has two high-speed 12-bit, 5 μs conversion analog-to-digital (A/D) converters, Analog Devices AD7672KP05, with an input voltage range of +/-5 VDC. A high-speed precision sample-and-hold amplifier, Analog Devices AD585JP, is on each A/D input. The inputs to both of the sample-and-hold amplifiers are from a dual four-channel analog multiplexer, Analog Devices AD7502SE. The multiplexer inputs are a torque signal, a motor velocity from the motor tachometer, and a joint velocity (either pitch or yaw) from an R/D. The fourth input to each of the dual analog multiplexer channels is from an eight-channel fault-protected analog multiplexer, Maxim MAX358CWE. One eight channel multiplexer inputs can be the wrist roll velocity from the wrist roll R/D or the joint module temperatures or motor temperatures. The other eight channel multiplexer has as its inputs the master manipulator hand controller signals. On each scan of the joint module data, only one channel of the eight-channel multiplexer is collected, or on eight scans of collecting joint module data, a complete set of the eight-channel multiplexer data will be collected.

The JPl miscellaneous controls include the brake relay control, RS-232 interface, and JPl reset. The JPl controls the motor brakes with commands from the LP or, as a safety measure, locks the brakes upon loss of communication with the LP. The motor brake power is controlled by solid-state relays that are located on the JPp board. The JPl has an RS-232 interface similar to that on the LP to allow direct communications with the JPl for stand alone debugging purposes. The reset circuit on the JPl also performs the same function as on the LP.

The JPl uses ten Du Pont Minitek connectors to connect the JPl to the sensors and to the JPp board. The connectors are located on the top side of the JPl and have crimp-to-wire contact on a 0.079 center and a very low profile to allow the JPl to fit within the joint module. To allow testing of the JPl without removal from the joint module, test and calibration signals that are only available on the underside of the JPl are connected to unused pins on the connectors. This configuration allows the test and calibration signals to be available on the top of the JPl.

JOINT PROCESSOR POWER SUPPLY

The JPp is the power circuit for the JPl. It is a 2- by 7-in., double-sided printed circuit board. The JPp is supplied with +24 VDC from a power supply in the cable breakout cabinet located at the base of the manipulator. The JPp uses three DC-DC 5-W converters to supply +5, +/-12 VDC onboard and to the JPl. The JPp also supplies the 2-KHz resolver reference drive to the resolvers primary, and the +/-5 VDC reference signal to the two torque sensors. The fiber optic transceiver is mounted on the JPp . The motor brake's solid-state relays are located on the JPp but are controlled by the JPl. The JPp is connected to the JPl and the resolver and torque sensors with interface cables using Molex connectors.

SURFACE-MOUNTED DEVICES

Surface-mounted devices (SMDs) were used because of the space constraints on the JPls and LPs. SMDs included both IC chips and discrete components, resistors and capacitors. The size of a SMD chip is approximately one-fourth the size of a standard IC chip. SMD discrete components required only a small fraction of the circuit board area compared than would standard discrete components. The soldering of SMD requires special soldering techniques. Three different soldering techniques were used: hot air, vapor phase, and infrared. Infrared soldering was the most successful and was performed by an outside contractor. The Instrumentation and Controls Division at ORNL performed any needed repairs to the boards by using a hot air desoldering and soldering station. The largest chip that had to be removed and replaced was a 68-pin microcontroller chip that had a bad I/O pin. There was no damage to either the circuit board or any nearby components.

FIBER OPTIC SYSTEM

The Fiber Optic system consists of two full-duplex bidirectional transceivers and a single high-strength fiber for each Link and JPl pair. The LP transceiver is located in the VME computer system rack and the JPl transceiver is located on its power supply board. The transceivers used are the CAF model manufactured by ADC Telecommunications, Inc.. The transceiver use bidirectional, full-duplex signal transmission over a single optic fiber. The transceiver is a self-contained, circuit-board-mountable device that contains the transmitting LED, the receiving photodetector, and the beam splitter. The transceivers are a matched pair which utilize two different light frequencies for receiving and transmitting. This configuration allows for full-duplex and bidirectional operation over a single fiber optic line. The optic fiber connects to the transceivers with SMA-type connectors.

The optic fiber used is the Ensign-Bickford Optics Company's "Avioptics" cable. The fiber is a 200/230-μm hard clad, silica type with a proof test of 200 ksi and a numerical aperture of 0.37. The complete optic cable has a temperature range of -65 to 125 ° C, 10-mm-bend radius, and a tensile strength of 100 kg. This optic cable was selected because of the large fiber diameter for optic coupling and ease of working with a high-proof test and a tight cable bend radius.

The fiber optic connectors that were used were manufactured by ITT Cannon. The connectors used at the transceivers are of the SMA-type. Those used from the computers to the manipulators were Cannon's fiber optic multi-channel connector (FOMC), and the connections between the joint modules were spring-loaded connectors that fit within a coaxial "D" subminiature connector. The connectors were selected because of their jewel alignment of the fiber. The jewel allows for very accurate fiber alignment between connectors that reduces the dB loss per connector. The connector loss is very important for LTM because there are seven connectors between the wrist JPl board and its LP board. Each connector end has a precisely aligned jewel with a hole sized for the fiber/cladding diameter; for LTM, this diameter is 230 μm. The fiber is inserted into the jewel, epoxied, and the end is polished. The fiber optic system worked without problems, even though the system had many connectors and continually flexing optic lines.

ELECTRICAL CABLING SYSTEM

The cabling of the manipulator system passes internally through both the joint module and the pitch-yaw differential joint of the module. Power cables are required for each manipulator motor PWM power, for the 24 VDC power to the JPp board, and for separate 24 VDC power for the motor brakes. Power and signal cables are required for the hardwired deadman switch on the master hand controller. Because of the small size of the joint differential and the number of cables still required to provide all of the signal and power requirements of the manipulator, a custom cable was designed and used. W. L. Gore manufactured a custom ribbon cable with 20 shielded, twisted, color-coded wire pairs. The diameter of one shielded, twisted wire pair is 0.10 in. The cable is designed for an excess of 1 million flexing operations inside the joint differential. The cables where terminated to high-density 52-pin "D" connectors. The connector size is that of a 25-pin "D" standard connector. A system design requirement was that any joint module could be used anywhere within the manipulator system. To meet this design requirement and to keep the cables to the minimum number required, the cable design used offset connector termination for the joint motor power and communications. This is a technique where the cables passing through the joint are not connected to the same joint bottom connector terminations as those used in the top connector, but the terminations are offset at the bottom connector to the same terminations to the next joint module's top connector terminations for motor power and communication. This technique allows any joint module to serve as any manipulator joint without any change to the computer system.

SAFETY INTERLOCK SYSTEM

To ensure personal and equipment safety, there is an interlock board in each master and slave computer system. The deadman switches on the master hand controllers are wired directly to the safety interlock board and the operator must hold the master hand controller grip to allow for system operation. Holding the hand controller enables the release of the motor brakes and enables the motor PWM amplifiers in the master and slave manipulator pair. The computer system monitors the deadman lines for system status and for commands to operate the brakes and PWM with the interlock board acting as a watchdog to the computer system. This design ensures a separate level of protection for personal and equipment safety independent of the computer system. The safety interlock boards also monitor the system power supplies, and can lock the manipulators if any power supply fails.

CONCLUSION

The solution to reducing the number of embedded cables for the LTM was solved by using the custom-design data collection system. The electronics, optic, and power cabling have performed well since delivery to NASA. The rate of data collection by the LP and JPI for each joint module for the LTM has been more than adequate for the control algorithms used. Future expansion of the LTM or new manipulator designs could be improved with the use of Very Large Scale Integration devices. The electronics packaging would be smaller, and reliability could improve because of the decreased number of components required.

The design of the electronics for the LP and JPI system could be used in most modular manipulator designs or by designs that necessitate acquiring, sending, and collecting remote data by a VME-based computer system.

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