NASA Contractor Report 182098

LINEAR LASER DIODE ARRAYS FOR IMPROVEMENT IN OPTICAL DISK RECORDING

G. A. Alphonse
D. B. Carlin
J. C. Connolly

DAVID SARNOFF RESEARCH CENTER
Princeton, NJ 08543- 5300

FINAL REPORT for Period of September 2, 1989 to June 30, 1990

NASA

National Aeronautics and
Space Administration

Langley Research Center
Hampton, Virginia 23665-5225

Preface

This report describes work performed for the period of September 2, 1989 to June 30, 1990 at the David Sarnoff Research Center in the Optoelectronics Research Laboratory, M. Ettenberg, Director, to complete Tasks 4, 6, and 7 under Contract NASA 1-18226. Tasks 4 and 7 were specifically aimed at the development of 10-element linear diode arrays for optical recording. The goal of Task 6 was the development of high-power AlGaAs channeled-substrate-planar (CSP) lasers. The work described herein pertains to the design, fabrication, life and yield assessment of CSP structures for use in optical recording and to our progress to date on the inverted CSP laser structure. D. B. Carlin was Project Manager and G.A. Alphonse was Project Scientist for the latter part of this work. Other contributors to this research were J. C. Connolly, C. G. Dupuy, M. G. Harvey, T. R. Stewart, D. A. Truxal, A. R. Dholakia, F. Z. Hawrylo, S. L. Palfrey, G. C. Taylor, S. N. Subbarao, P. D. Gardner, D. T. Tarangioli, D. J. Holmes, J. P. Bednarz, M. Toda, J.B. Berkshire, S.R. Miller, J. E. Economou, and A. Greyserman.

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EXECUTIVE SUMMARY

We report on the development of individually addressable monolithic ten-diode laser arrays for high-performance multitrack magneto-optic (MO) recorders for space stations. Such recorders require the use of high-power laser array sources that deliver greater than 30 mW cw with linear-light-vs-current characteristics and low relative intensity noise. The channel-substrate-planar (CSP) structure, grown by liquid phase epitaxy (LPE) and configured as a monolithic linear array of individually addressable CSP lasers was considered a first choice for this application because of its high output power capability and moderate individual diode yield from good wafers.

Our effort to fabricate, characterize, burn-in, and lifetest CSP ten-diode arrays was extensive. Lifetesting was performed on eight arrays for various lengths of time. Testing on one array carried to 1632 h and tests on another array to 2240 h revealed a projected useful life of approximately 10,800 h, if end-of-life is assumed to be the time required for the current to double in order to maintain 30 mW cw output power. The wavelength and far-field diffraction pattern were found to be very stable. The average change (increase) in wavelength was less than 1.9 nm for the duration of the tests. The yield of high performance CSP arrays was found to be low. Despite the low yield and the realization that a different structure, such as the inverse CSP grown by MOCVD, could be more desirable, it was necessary to continue the CSP work in order to deliver arrays to exercise a demonstration unit under development at GE Aerospace in Camden, NJ. Three arrays were delivered to NASA. One was used to demonstrate, for the first time, the simultaneous recording of eight independent tracks at an effective data raate per track of 16.67 MBits/s for a combined user rate of 133 MBits/s. The linear diode array was also used to evaluate system parameters, such as cross-talk, S/N ratio, C/N ratio, focus and tracking accuracy, erasure and erasability.

The results of extensive computer modeling have shown that, in addition to growth non-uniformity, alignment tolerances of the zinc diffusion stripe to the CSP channel are some of the main reasons for the low CSP yield.

Following the delivery of three CSP arrays, we initiated our work toward the development of inverted CSP (I-CSP) arrays. Results on QW ridge laser arrays made from this structure reveal low threshold current (15 mA) and low current (about 40 mA) to obtain 30 mW cw output power. Following the

development of the technology to regrow GaAs on AlGaAs, we made I-CSP arrays with performance comparable to the ridge, with the important new feature that they were mounted for the first time in the p-up configuration. The low drive current and p-up mounting capabilities make the I-CSP a potentially reliable device and simplify its packaging for space application.

In the Appendix, we describe an extensive statistical analysis of array yield as a function of number of array elements and as a function of the yield for individual elements. We have used this model to confirm the observed yield of 9 contiguous good elements in a 10-element array and indicate required steps to increase yield.

Section I

INTRODUCTION

The NASA high performance Spaceflight Optical Disk Recorder (SODR) is an 8-channel, 10 GB capacity read-write recorder with 300 Mbps data rate. For writing, reading, and erasing, the system actually requires 9 laser diodes, out of which 8 are used for data and and one is used for tracking. [1-5]

The individual lasers within the arrays required stable output power exceeding 30 mW, with a high degree of uniformity among elements, and low relative intensity noise (RIN). The channel substrate planar (CSP) structure, grown by liquid phase epitaxy (LPE), appeared as a suitable laser structure for this application, because preliminary studies had indicated that the structure was capable of producing high power in a single element configuration. However, we have found that accurate alignment to within a fraction of a micron is required to achieve high power in a single mode. This represents a serious fabrication problem because the CSP structure is not self-aligned. Consequently, the yield of CSP arrays was very low. The inverted CSP (I-CSP), which is a ridge or mesa structure with a regrown layer of GaAs between the mesas, provides optical guiding in the same manner as the CSP. It is self-aligned and can be grown by MOCVD (metal-organic chemical vapor deposition). For both of these reasons, it is likely to be fabricated with a higher yield than the CSP.

In the course of our work, it became necessary to provide laser diode arrays for the technology demonstration unit (TDU) that was under construction by GE Aerospace, Camden, NJ. Although it was clear that it was desirable to move into the MOCVD technology, it was also evident that the only way to provide GE the necessary support in 1989 was to continue making CSP arrays, despite the low yield, in order to provide a handful of arrays to exercise the TDU. For this reason, the major growth and fabrication effort in this program was placed on CSP until some deliverables could be made available to the customer and to the TDU. Our arrays contain 10 elements, although only 9 are required. This provides some degree of redundancy, but the choice was made mainly because equipment is available in our laboratories to simultaneously test 10 individual elements.

In a previous report, [6] we discussed at length the problems of design, fabrication and bonding of CSP arrays, as well as the growth and processing of I-CSP arrays. We studied several techniques for enhancing the operation of

magneto-optic (MO) systems, as well as the issues involved in the choice, design, and fabrication of high power mode-stabilized lasers. This report will address the work we have performed toward the completion of the CSP array tasks and the initiation of our development work on I-CSP arrays performed near the end of the contract. Some discussion will be included on our lifetesting studies conducted on CSP arrays from and on the subject of array fabrication yield in general.

Section II

CSP LASER ARRAYS

A. DESIGN AND FABRICATION

The CSP array package developed at the David Sarnoff Research Center is illustrated in part in Fig. II-1. It consists of a monolithic array of CSP lasers with 150 μm center-to-center spacing and 50 μm isolation channels between lasers. The depth of the channel is chosen to provide electrical separation and thermal isolation between individual lasers. The array is mounted epi-side down (p-side down if the layers are grown on a n-doped substrate, as it is in the current design) on a beryllium oxide (BeO) submount, which is then mounted on a copper block and thermoelectric cooler. The BeO is chosen because of its high thermal conductivity and its matching coefficient of thermal expansion with the GaAs laser substrate. Electrical connections are made to the p-electrodes through finger contacts plated on the BeO. Indium solder, together with flux is used to bond the p-electrodes to the contacts on the BeO. The other side of the BeO, which is fully metallized, is bonded to a copper heatsink by means of a low temperature indium-tin solder.
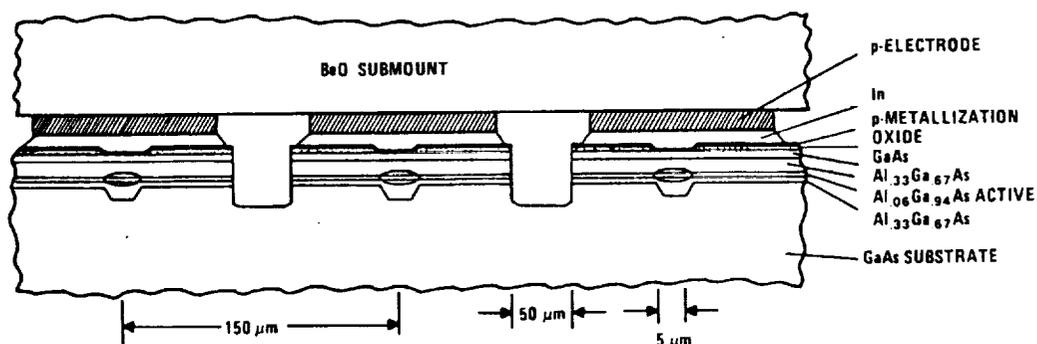
Figure II-1. Partial view of CSP array on BeO submount.

The CSP structure is fabricated in a one-step epitaxial growth consisting of a n-cladding layer, a thin active layer (< 1000 Å thick), a p-cladding layer, and a p-cap (obtained by zinc diffusion in a n-cap) layer on a substrate in which a V-groove (channel) has been etched. Material growth by LPE produces smooth layers over the channel substrate. For emission at 830 nm, the active layer contains 6% aluminum, and the cladding layers have about 30% aluminum in order to provide confinement of the optical field. The p-contact is defined by a 5 μm zinc diffusion stripe aligned with the channel through a narrow window in an oxide mask. The choice of n-cladding layer thickness, channel and stripe widths have been obtained through optimization by the use of extensive computer modeling together with experimental confirmation of that modeling.[7-10] In order for the laser to operate in the fundamental waveguide mode, the stripe width must be about 5 μm or less. Modeling also requires the channel to be wider than the zinc diffusion stripe in order to reduce substrate absorption while lowering the threshold current and increasing differential quantum efficiency. For these reasons we have chosen 5 μm for the stripe width, and > 6 μm for the channel width. These widths are fine-tuned by controlling their etching time and rate.

As mentioned earlier, the CSP structure is not self-aligned in the sense that the channel is not visible after epitaxial growth, which makes the subsequent zinc diffusion stripe alignment difficult. One of the important results of our modeling study is that the stripe and channel must be almost perfectly aligned in order to prevent saturation at low power. This saturation is observable as a rollover in the P-I characteristics at fairly low power.[10] We found both theoretically and experimentally that a misalignment by 0.5μm is sufficient to cause a rollover of output power at levels below the 30 mW cw required, as shown in Fig. II-2. This can be understood intuitively from the fact that guiding in CSP lasers is influenced by the losses in the wings of the CSP channel. When the stripe and the channel are misaligned, as soon in Fig. II-2, the laser is pumped partly over the lossy region at one of the wings. The high optical loss over that wing causes the junction temperature to be higher than in ordinary CSP lasers, resulting in loss of efficiency and saturation at low power. Another effect of misalignment is to cause laser output instabilities, which appear as jumps in the near-field as the current increases beyond a certain value. Our model shows that this alignment problem can be reduced, to some extent, by increasing the zinc diffusion stripe width. However, this approach deviates from the optimum design. It increases threshold and reduces differential quantum efficiency.

The steps involved in the actual fabrication of CSP arrays are shown in Figs. II-3 and II-4. They have been discussed in a preceding report issued in January 1990 and are summarized below. Figure II-3 illustrates the front-end processing, starting from a 25 mm x 17 mm n^+GaAs substrate. A 120 nm CVD SiO_2 layer is deposited on the substrate as a mask to photolithographically define the CSP V-channels. Following channel etching in the substrate and removal of the SiO_2 mask, the laser structure (n-clad, active layer, p-clad, n-cap) is grown over the grooved substrate. Another mask is then prepared by SiO_2 and photolithography to define stripes through which zinc is to be diffused to create a heavily p-doped region for ohmic contact. Zinc diffusion is carried in an ampoule containing a mixture of $ZnAs_2$ and powdered GaAs at a temperature of 650° for a precise length of time to limit the diffusion depth to the upper half of the p-clad layer (the diffusion depth must not be allowed to get too close to the active layer to prevent diode short circuits and premature degradation).
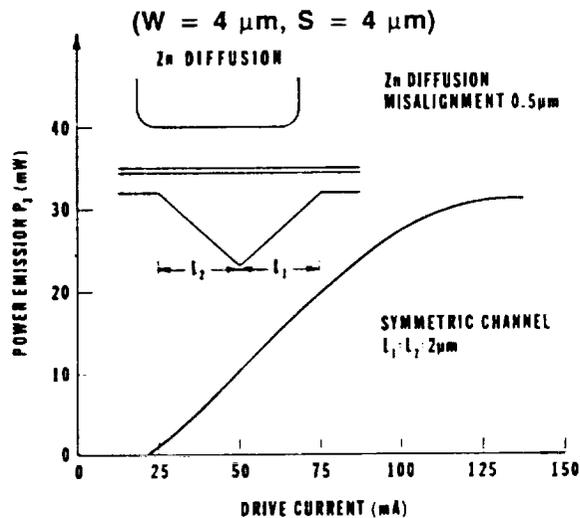
Figure II-2.   Rollover of CSP laser P-I characteristics due to stripe-channel misalignment.

The remaining steps to complete the wafer fabrication are illustrated in Fig II-4. Ohmic contact is made to the zinc diffusion stripe by deposition of a thin layer of titanium-platinum-gold over the p-side. The wafer is then thinned to a thickness of 100 μm as needed for proper cleaving, and a layer of germanium-gold-nickel-gold is deposited and sintered on the n-side, for ohmic contact on that side. The n-side is then gold plated to lower its electrical resistance. Not shown

5

in the figure is an ion beam milling step that is used to cut a 2- to 3-μm deep channel 50 μm wide to electrically and thermally separate the diodes in an array. To complete the fabrication, the wafers are cleaved into bars whose facets are dielectric-coated to obtain prescribed facet reflection, and the bars are diced into ten-diode arrays, ready for testing and evaluation.

```
┌──────────────────┐          ┌──────────────────┐
│ STARTING         │          │ 120 nm CVD SiO2  │
│ SUBSTRATE        │─────────▶│ DEPOSITION       │
│ n+ GaAs          │          │ (370 C)          │
│ 25 mm x 17 mm    │          │                  │
└──────────────────┘          └──────────────────┘
                                        │
                                        ▼
┌──────────────────┐          ┌──────────────────┐
│ V-GROOVE         │          │ LITHOGRAPHY TO   │
│ CHANNEL ETCH     │◀─────────│ OPEN CHANNELS    │
│ AND ETCH SiO2    │          │ (5 μm) IN PHOTORE-│
│                  │          │ SIST AND ETCH SiO2│
└──────────────────┘          └──────────────────┘

                              ┌──────────────────┐
                         ┌───▶│ MEASURE ETCH PROFILE│
                         │    │ BY PROFILOMETER  │
                         │    └──────────────────┘
┌──────────────────┐          ┌──────────────────┐
│ LASER            │          │ ANGLE LAPPING    │
│ STRUCTURE        │─────────▶│ TO               │
│ GROWTH BY LPE    │          │ MEASURE LAYER    │
│                  │          │ THICKNESSES      │
└──────────────────┘          └──────────────────┘
        │                               │
        ▼                               ▼
┌──────────────────┐          ┌──────────────────┐
│ SiO2 DEPOSITION  │          │ PHOTOLUMINESCENCE│
│ (370 C) AND      │          │ TO MEASURE Al    │
│ DENSIFICATION    │          │ CONTENT          │
│ (800 C)          │          │                  │
└──────────────────┘          └──────────────────┘
        │
        ▼
┌──────────────────┐
│ REOPEN           │
│ CHANNELS         │─────────▶  FOR Zn DIFFUSION
│ AND ETCH SiO2    │
└──────────────────┘
```

Figure II-3. Front-end CSP processing flow chart.
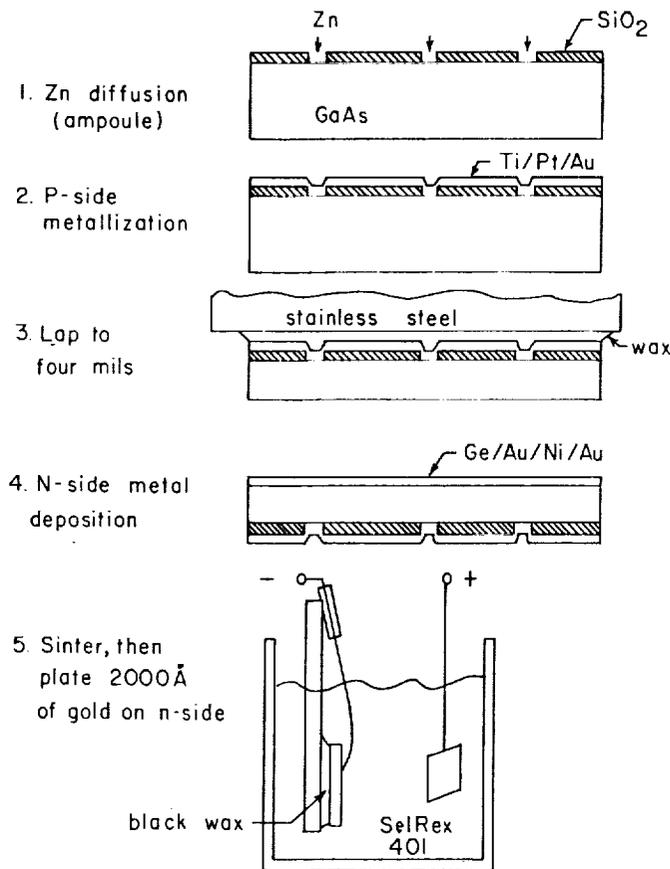
Figure II-4. Back-end processing steps for CSP fabrication.

The steps involved in the testing and evaluation of ten-diode arrays are shown in Fig. II-5. The arrays are probe-tested (without being permanently bonded) in an instrument that was specifically designed for that operation. Their threshold current, output power, far-field and beam stability are checked using a video monitor. Output power-vs-intensity (P-I) and far-field plots are obtained for those arrays that appear to have comparable threshold, stable far-field and near-field, and high output power. A part number label is then assigned to arrays that have been so characterized.

```
                    ┌─────────────────┐
                    │     START       │
                    │   IAA CHIP      │
                    └─────────────────┘
                             │
                             ▼
             ┌───────────────────────────────┐
             │  Probe Test Unmounted Chips   │
             │    Vf, Ith, Far-Field, and    │
             │     10 Diode Array Yield      │
             └───────────────────────────────┘
                             │
                             ▼
             ┌───────────────────────────────┐
             │    Mount Acceptable Array     │
             │     Chips to BeO Submount     │
             └───────────────────────────────┘
                             │
                             ▼
        ┌────────────────────────────────────────┐
        │   Characterize Mounted Array Chips     │
        │      Vf, Ith, Power Capability,        │
        │   Far-Fields, Spectra, and Yield       │
        │        (cw operation-30 mW)            │
        └────────────────────────────────────────┘
                             │
                             ▼
             ┌─────────────────────┐        ┌──────────────────────────────┐
             │     Burn-In         │───────▶│          Lifetest            │
             │                     │        │       25°C, 30 mW,  cw       │
             │     100hrs.         │        │  re-characterize - 200 hrs.  │
             └─────────────────────┘        └──────────────────────────────┘
                             │
                             ▼
             ┌───────────────────────┐
             │  Mount Acceptable Arrays │
             │     on Cu Heatsink     │
             └───────────────────────┘
                             │
                             ▼
             ┌───────────────────────────┐
             │  Individually Addressable │
             │  Ten Diode CSP Laser Array│
             │         Assembly          │
             └───────────────────────────┘
```

Figure II-5. Flow chart for characterizing ten-diode arrays.

Following probe testing, the labeled arrays meeting a set of criteria are selected for soldering on BeO submounts. The criteria are that greater than nine contiguous elements have:

- Threshold current less than 80 mA, with less than 15 mA variation among elements within a single array
- Output power exceeding 50 mW in the pulsed mode (duty cycle $\simeq 0.001$), with linear P-I characteristics
- Superimposed, stable far-field radiation pattern at 50 mW peak power in the pulsed mode
- Stable near-field radiation pattern, as observed using a video monitor

The arrays that are mounted on BeO are characterized by measuring their emission wavelength cw P-I and far-field at rated power. Again, those that pass a certain set of criteria are selected for permanent mounting on a copper heatsink (using In-Sn solder) for burning-in, delivery, or lifetesting. The criteria are as follow:

- Threshold current less than 80 mA cw, with less than 15 mA variation among elements within a single array
- Output power of 30 mW cw, with linear P-I characteristics
- Superimposed stable far-field radiation pattern at 30 mW cw
- Single longitudinal mode at about 830 nm, with secondary side lobes less than 13dB below the main lobe, and with wavelength spread within an array to be no more than ± 5 nm

Arrays that had 9 or 10 elements meeting the above criteria were burned-in for 100 h at full rated power, and then retested in cw mode. Those that still meet these criteria after burn-in at full rated power of 30 mW were delivered to NASA. Those having at least six adjacent elements but less than nine meeting these criteria after 100-h burn-in were used in lifetest measurements.

The lifetesting and burn-in facility is a six-array setup consisting of a heatsink temperature block with temperature control and a set of power supplies,

as shown in Fig. II-6. The heatsink block is equipped with a cooling fan and six thermoelectric coolers on which the array-on-BeO-on-Cu block can be mounted. Temperature controllers monitor and maintain the temperature of each array independently. Burn-in and life-testing are done at 23°C. A power supply unit consisting of six racks of 10 independent power supplies (60 power supplies altogether) provide the necessary drive current for each individual diode of each of the arrays under test. Operation is at constant current adjusted periodically to maintain 30 mW output power. The necessary drive current for 30 mW output power (about 120 mA to 150 mA) for each diode in an array is obtained from the individual P-I characteristics curves, and current is maintained for the time interval of the test.
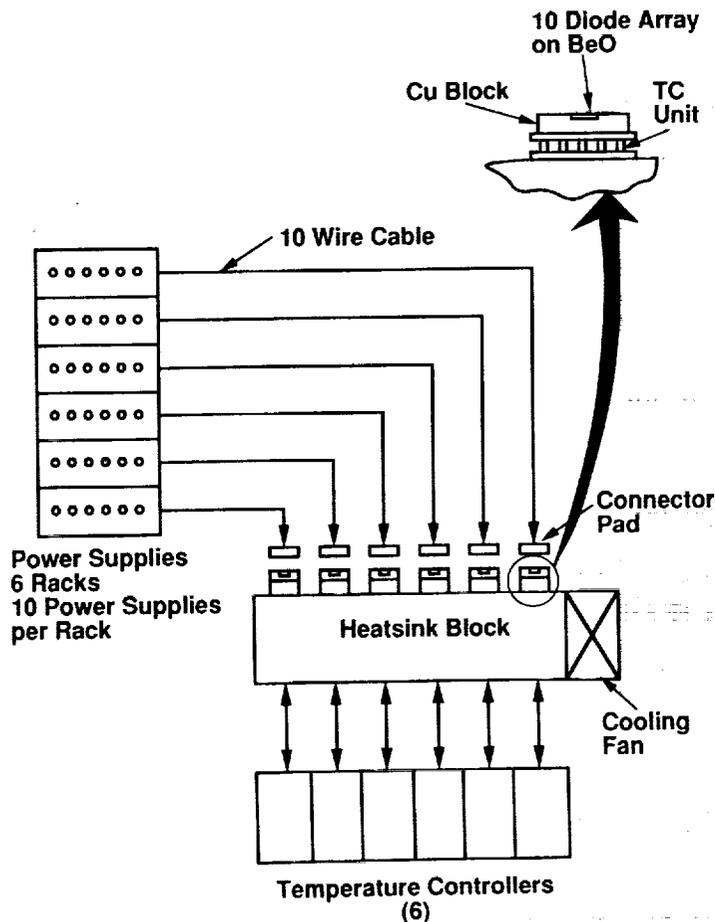
Figure II-6. Lifetest and burn-in set-up.

Table II-1 and Fig. II-7 summarize the screening effort. We grew 38 LPE wafers, but we actually tested only a handful of arrays from 15 of them because the grown wafers did not fall within characterization tolerances. We ended up testing 558 arrays, of which 150 came from a single wafer, TJ300 (Note, a single LPE wafer contains approximately 500 array sites). Thus, it appears that the CSP wafer yield is about 39%, but the wafer yield to produce the special high-power diodes for this program was much lower, perhaps one out of 15 of those that appeared to be acceptable immediately after growth, based on angle-laps and photoluminescene spectra.

Table II-1

SUMMARY OF SCREENING RESULTS

LPE Runs	Probe Testing		Mounting		Burn-in & Life tested	Deliver- ables	Delivered
	Probe Tested	Plotted	BeO	Cu Block			
TJ 270	8	1	0	0	0	0	0
TJ 288	8	1	0	0	0	0	0
TJ 289	28	2	0	0	0	0	0
TJ290	4	0	0	0	0	0	0
TJ 291	72	5	0	0	0	0	0
TJ 293	5	0	0	0	0	0	0
TJ 294	24	1	0	0	0	0	0
TJ 296	97	0	0	0	0	0	0
TJ 300	150	24	17	13	13	3	2
TJ 301	5	0	0	0	0	0	0
TJ 308A*	12	2	3	0	0	0	0
TJ 308B*	19	8	0	0	0	0	0
TJ309A*	30	6	2	0	0	0	0
TJ 310AL*	5	4	0	0	0	0	0
TJ 310AS*	8	4	0	0	0	0	0
TJ 310B*	6	2	0	0	0	0	0
TJ 311A*	5	0	0	0	0	0	0
TJ 311B*	21	12	0	0	0	0	0
TJ 312A*	11	5	0	0	0	0	0
TJ 312B*	40	9	0	0	0	0	0
TOTAL 15 LPE	558	86	22	13	13	3	2

* Split Wafers

Selected LPE wafers

in process | completed

4 | 15

Probe test diode arrays

in process | completed

50 | 558

Array selection (>9 elements
to > 50 mW pulsed)

reject

472 | 86

Array selection for linear P-I,
far field, and > 9 elements

reject

64 | 22

Mounting and characterization
on BeO submounts (> 9 elements,
linear P-I, 30 mW cw) and mounting
on copper heatsink

reject

9 | 13

TJ-300 ONLY

100 hour burn-in (linear and clustered P-I,
single mode to > 30 mW cw) and recharac-
terization

reject

2 | 11

Selection for life test (< 9 elements
surviving) or delivery (> or = 9 elements
surviving)

life test | deliverables

8 | 3

Deliverables

available for eval. | delivered

1 | 2

Figure II-7. Screening process for selection of ten-diode arrays.

Out of the 558 tested arrays, complete probe testing data was generated for 86 units, of which 22 were selected for mounting on BeO and cw characterization. Following this step, 11 arrays were found suitable for 100-h burn-in, and finally 3 arrays were delivered and 8 were used for lifetesting. Four arrays were delivered, but one was found to be damaged and returned for lifetesting. Thus, the overall yield was very low, about 4/558 or 0.7%. All of the 11 arrays submitted to burn-in and lifetesting came from the same wafer, TJ-300, so the 10-diode array yield for that wafer was 4/150 or 2.7%.

B. LIFETESTING

The lifetesting racks can accommodate six ten-diode arrays simultaneously. We have lifetested a total of eight arrays for various lengths of time. Testing is done at constant current for periods of several hundreds of hours and the array characteristics (P-I, far-field radiation pattern and wavelength) are measured after each period. Arrays containing six to eight elements that satisfy the acceptance criteria are then placed on the lifetest rack again. Arrays containing nine or ten satisfactory diodes are set aside for delivery, and arrays having less than six satisfactory elements are rejects. At the beginning of each new period, a new value of current for 30 mW light output is applied to the diodes, as determined from the latest P-I measurements.

Six arrays were tested to over 900 h, one was tested to over 1600 h and another for over 2200 h. Lifetesting on the rack is terminated if an array shows excessive kinks or rollover. Our general observation is that the characteristics of surviving diodes change relatively slowly over time, but not slowly enough for space qualification. Table II-2a and II-2b give lifetest data of array AT-207. This array contained nine elements and was tested for 1632h. Table II-2a gives the current required to maintain 30 mW cw output power for each diode at several times during the test. Element #5 degraded sometime after the 100h point. The wavelength data is shown in Table II-2b. One conclusion that can be drawn from this data is that the wavelength is very stable over the time period of the test. Figure II-8 shows the operating current required to maintain 30 mW cw for the elements of this array, and Fig. II-9 shows the *average* threshold current and current for 30 mW for this array. Similar data for 7 elements in array AT-212 are given in Tables II-3a and II-3b, and Figs. II-10 and II-11. For AT-212, elements

#7 and #8 were damaged by the operator after 100 h of test, and #5 either degraded or was damaged after 608 h of test.

A linear fit for the average current to maintain 30 mW cw vs time gives the following:

$$\text{AT-207} \quad I = 135 + 0.0125\,h$$

$$\text{AT-212} \quad I = 130 + 0.012\,h$$

where I is the current in milliamperes and h is the time in hours. If the end of life is specified as the time for the current to double, both of these equations give a life of about 10,800 h. This life span may be considered adequate for ground environment, but not for space application.

The most stable characteristic is the emission wavelength and the far-field pattern. For both arrays described in this report, the average wavelength change (increase) was less than 1.9 nm. Figure II-12 is a set of spectra to show the wavelength stability of the AT-212 diodes after 2240 h of lifetest. Similar data after 100 h of test for an array delivered to NASA appear in Figure II-15 of report entitled, "Linear Laser Diode Array for Improvement in Optical Disk Recording For Space Stations, January 1990."[6]

C.   RECORDING MILESTONE WITH NINE-ELEMENT ARRAY

One of the arrays delivered to NASA (AT-214) was incorporated in a prototype technical demonstrator unit (TDU) of the Spaceflight Optical Disk Recorder (SODR) being developed by GE Aerospace in Camden, NJ. This unit is a read-write-erase nine-track (eight data channel, and one tracking channel) recorder with a 10 GB capacity and data rate up to 150 Mbit/s, (300 Mbit/s for two units running in parallel) using a 14-in.-diameter magneto-optic disk as the storage medium. The array was used successfully for the following:

- Demonstration of 9-diode laser beams through common optics and a single objective lens

- Demonstration of independent write, read and erase cycling and simultaneous operation of all eight data channels at user data rate of 133 Mbit/s NRZ (extendable to 150 Mbit/s)

- Demonstration of single pass erasure of prerecorded tracks

- Demonstration of diffraction-limited spot size of about 0.95 μm

Table II-2a

LIFETEST DATA OF ARRAY AT-207

Diode No.	24 Hrs I(th) mA	24 Hrs I(30) mA	288 Hrs I(th) mA	288 Hrs I(30) mA	1080 Hrs I(th) mA	1080 Hrs I(30) mA	1632 Hrs. I(th) mA	1632 Hrs. I(30) mA
1	69	147	70	142	73	144	73	157
2	65	142	73	143	72	144	73	159
3	63	126	63	130	64	133	66	143
4	64	130	67	140	76	133	73	170
5	69	149	95	X	95	X	X	X
6	64	127	66	134	68	142	72	159
7	65	131	69	138	73	146	77	160
8	65	131	69	140	73	150	77	170
9	69	136	73	144	76	155	81	173
10	69	137	73	145	74	146	74	154

Table II-2b

WAVELENGTH DATA (nm) FOR ARRAY AT-207

Diode No.	A 100 hr nm	B 1080 hr. nm	B-A nm	C 1632 Hrs. nm	C-A nm
1	814.32	816.36	2.04	816.3	1.98
2	816.53	816.74	0.21	817.6	1.07
3	816.96	817.9	0.94	818	1.04
4	818.03	817.53	-0.5	818.3	0.27
5	815.79	N/A	X	X	X
6	817.25	817.86	0.61	819.4	2.15
7	814.86	819.66	4.8	821.2	6.34
8	816.84	817.5	0.66	818	1.16
9	818.98	820	1.02	820.4	1.42
10	818.37	819.23	0.86	819.3	0.93
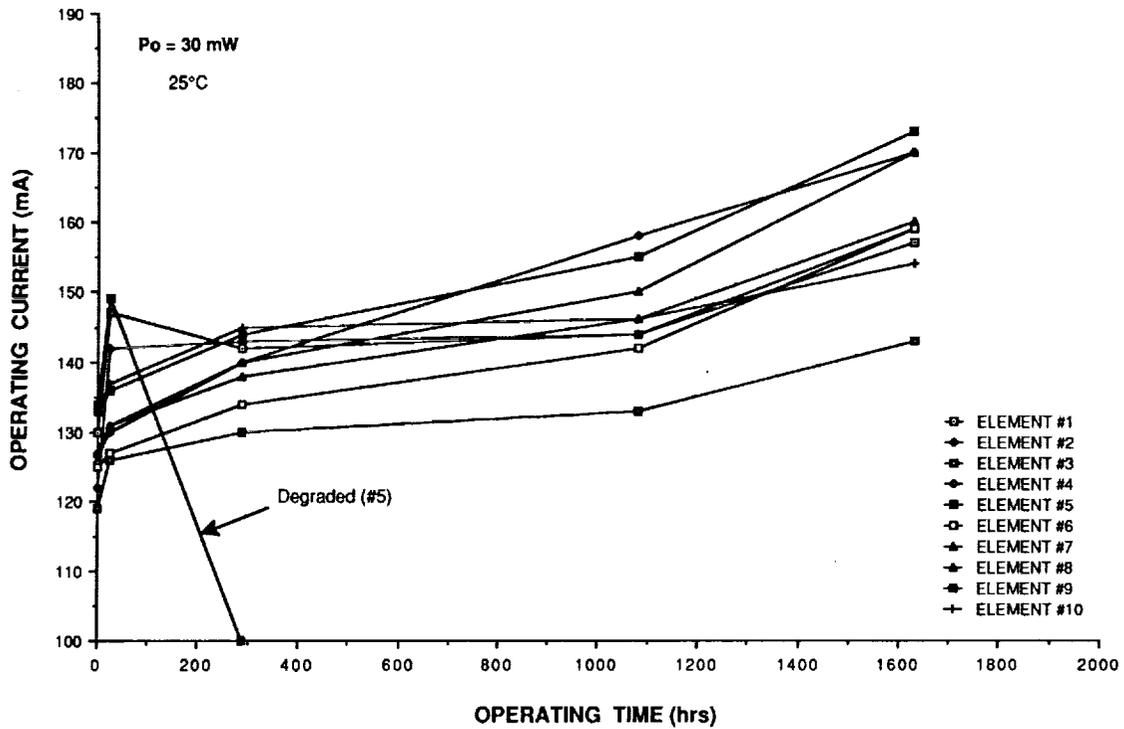
Figure II-8. Operating current vs time to maintain 30 mW cw for individual diodes of array AT-207.
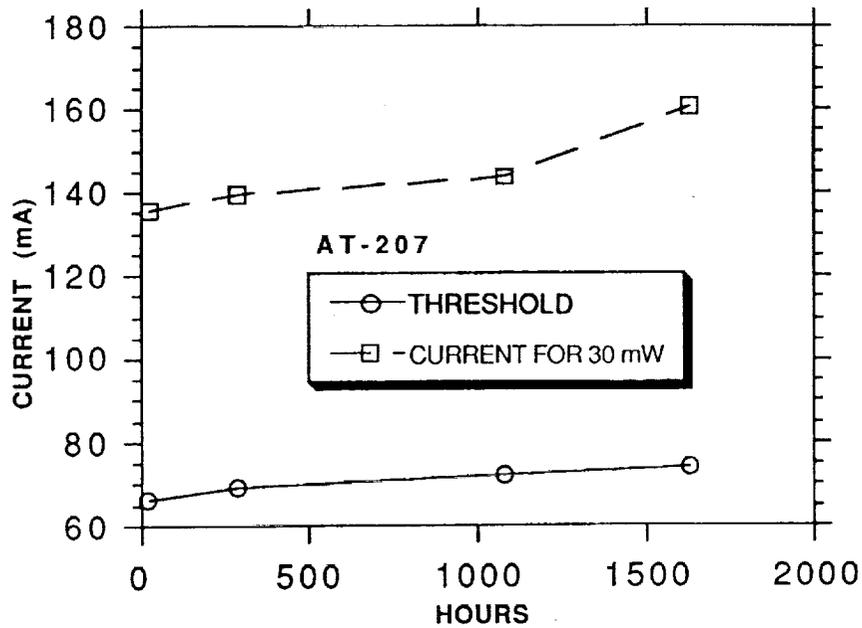
Figure II-9. Average threshold and current for 30 mW cw for diodes of AT-207.

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Table II-3a

LIFETEST DATA OF ARRAY AT-212

Diode No.	100 Hrs I(th) mA	100 Hrs I(30) mA	370 Hrs I(th) mA	370 Hrs I(30) mA	608 Hrs I(th) mA	608 Hrs I(30) mA	896 Hrs I(th) mA	896 Hrs I(30) mA	1688 Hrs I(th) mA	1688 Hrs I(30) mA	2240 Hrs I(th) mA	2240 Hrs I(30) mA
1	71	140	84	168	72	148	92	167	100	190	105	180
2	62	128	63	131	63	132	66	132	65	137	68	159
3	62	127	65	131	63	130	65	130	65	133	68	142
4	64	132	65	134	63	133	70	135	70	140	75	152
5	64	131	65	133	66	132	X	X	X	X	X	X
6	66	130	68	134	67	133	72	135	72	140	75	148
7	69	142	X	X	X	X	X	X	X	X	X	X
8	67	138	X	X	X	X	X	X	X	X	X	X
9	69	141	71	184	70	142	72	142	72	145	75	153
10	69	139	70	154	79	155	80	155	84	160	86	170

Table II-3b
WAVELENGTH DATA (nm) FOR ARRAY AT-212

Diode No.	A 100 Hrs. nm	B 1688 Hrs. nm	B-A nm	C 2240 Hrs. nm	C-A nm
1	814.86	817.5	2.64	817.4	2.54
2	817.31	818.5	1.19	819.9	2.59
3	816.51	818.83	2.32	817.7	1.19
4	816.86	818.93	2.07	819.7	2.84
5	817.24	X	X	X	X
6	816.82	817.76	0.94	817.9	1.08
7	818.44	X	X	X	X
8	N/A	X	X	X	X
9	816.89	817.26	0.37	817.4	0.51
10	815.58	817.57	1.99	817.8	2.22
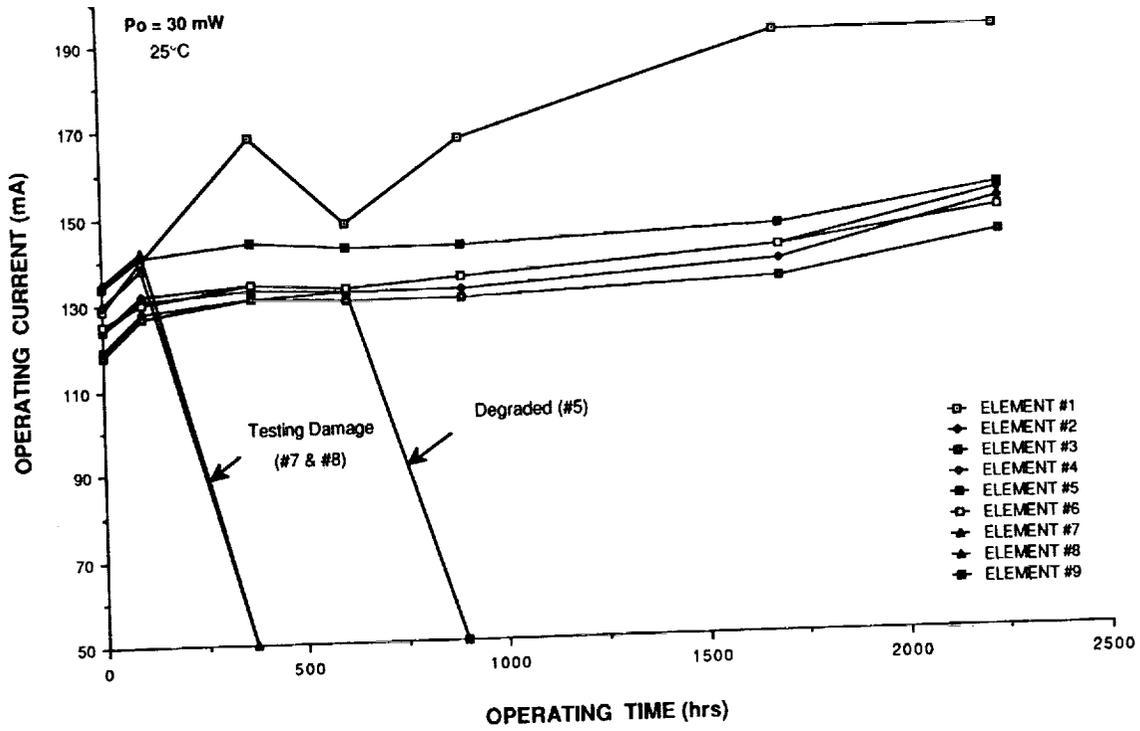
Figure II-10.   Operating current vs time to maintain 30 mW cw for individual diodes of array AT-212.
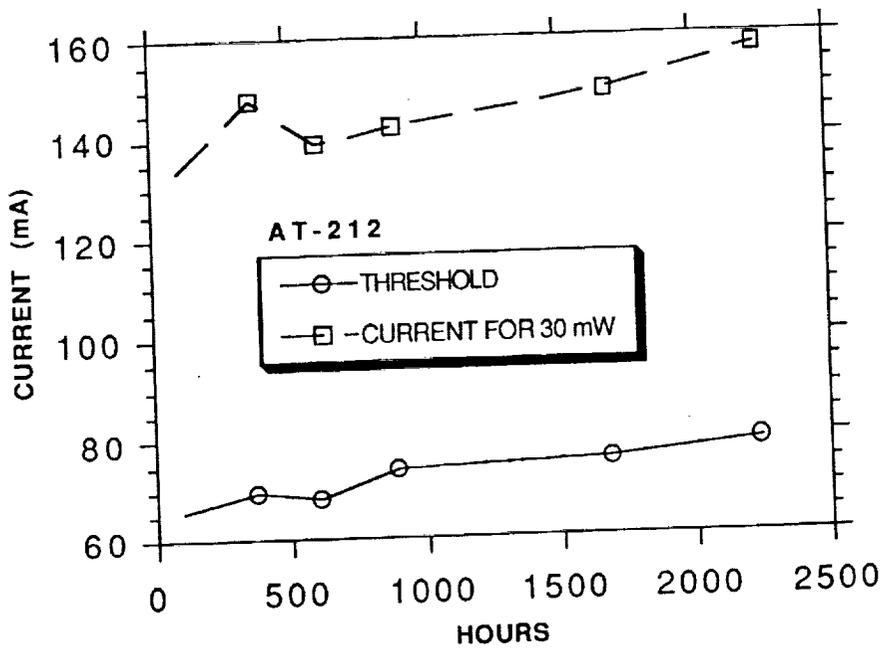
Figure II-11. Average threshold and current for 30 mW cw for diodes in array AT-212.

DATE 02.08.90
TIME 17:26

SPECTRUM AT-212 30MW 23C   MEM1

25
μ

10
μ

807.5   817.5nm   827.5
SWP   2nm/ YS   5μ/ RES .1nm AVR   1
WMKR   817.36nm
LMKR   22.1μ

DATE 02.08.90
TIME 17:28

SPECTRUM AT-212 30MW 23C   MEM2

30
μ

10
μ

809.9   819.9nm   829.9
SWP   2nm/ YS   5μ/ RES .1nm AVR   1
WMKR   819.90nm
LMKR   25.3μ

DATE 02.08.90
TIME 17:29

SPECTRUM AT-212 30MW 23C   MEM3

30
μ

10
μ

807.7   817.7nm   827.7
SWP   2nm/ YS   5μ/ RES .1nm AVR   1
WMKR   817.73nm
LMKR   29.4μ

DATE 02.08.90
TIME 17:30

SPECTRUM AT-212 30MW 23C   MEM4

30
μ

10
μ

809.9   819.9nm   829.9
SWP   2nm/ YS   5μ/ RES .1nm AVR   1
WMKR   819.90nm
LMKR   30.2μ

DATE 02.08.90
TIME 17:31

SPECTRUM AT-212 30MW 23C   MEM6

30
μ

10
μ

807.9   817.9nm   827.9
SWP   2nm/ YS   5μ/ RES .1nm AVR   1
WMKR   817.90nm
LMKR   29.0μ

DATE 02.08.90
TIME 17:32

SPECTRUM AT-212 30MW 23C   MEM9

30
μ

10
μ

807.4   817.4nm   827.4
SWP   2nm/ YS   5μ/ RES .1nm AVR   1
WMKR   817.40nm
LMKR   33.5μ

DATE 02.08.90
TIME 17:33

SPECTRUM AT-212 30MW 23C   MEM10

30
μ

10
μ

807.0   817.0nm   827.0
SWP   2nm/ YS   5μ/ RES .1nm AVR   1
WMKR   817.00nm
LMKR   33.2μ

Figure II-12. Section of elements of array AT-212 after 2240 h of lab tests.

The purpose of those experiments was to measure system performance, and evaluate parameters, such as cross talk, S/N ratio, focus and tracking accuracy, and erasure-rewritability of disks with the powers available from the laser diode array. The array was used in several demonstrations of multichannel recording and continues to be operational after several hundred hours at the time of this writing. This work represented a true milestone in optical data recording technology.

D. YIELD OF CSP ARRAYS

The yield for monolithic individually addressable CSP ten-diode arrays is low. One reason for the low yield is the fact that the requirements are very stringent. The array must have nine *contiguous* lasers having identical characteristics: the same threshold current, the same current for an output of 30 mW cw, linear P-I characteristics (no kinks, no rollover) to beyond 30 mW cw, identical far-field, single stable longitudinal and transverse mode with less than ± 5 nm wavelength separation among diode elements. An example of a ten-diode array meeting those requirements is shown in Fig. II-13. It shows the spectra, far-field, and P-I characteristics for array AT-214, which was delivered to NASA after a 100 h burn-in. This array had an emission wavelength of 817 nm with a spread of less than 3 nm, threshold of about 65 mA, and its elements required about 125 mA for 30 mW cw output power.

The overall yield of arrays meeting the above characteristics is about 0.7% of the arrays probe-tested. There are two principal factors involved in the assessment of the yield for individually addressable laser diode arrays. They are: the individual element yield and the array yield. The individual element yield is the number of "good" elements obtained from a wafer, and it depends on several factors. The first factor is the LPE growth itself, which is known to be non-uniform. The second one is the alignment of the Zn diffusion stripe with respect to the channel. As described earlier, this misalignment is responsible for rollover and kinks in the P-I characteristics, often at low power. Such misalignment may occur for individual diodes in an otherwise properly aligned set of masks as a result of local variations of etching rates for either the channel or the stripe. The third factor that can also seriously affect yield is in the area of processing. There are three processing steps that are likely to reduce yield when improperly monitored. They are: metallization, cleaving, and facet coating. In particular, a

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p-metallization layer that does not properly adhere to the wafer leads to difficulty with bonding to a submount and to high thermal resistance. The effect of high thermal resistance is to cause heating at low power and reduce differential quantum efficiency at higher current, with a resulting rollover in the P-I characteristics similar to the rollover due to misalignment. The processes of cleaving and facet coating can introduce damage in parts of the array. In particular, the end devices (i.e., No. 1 and 2 or No. 8 or 9) are partially susceptible to cleaving damages.
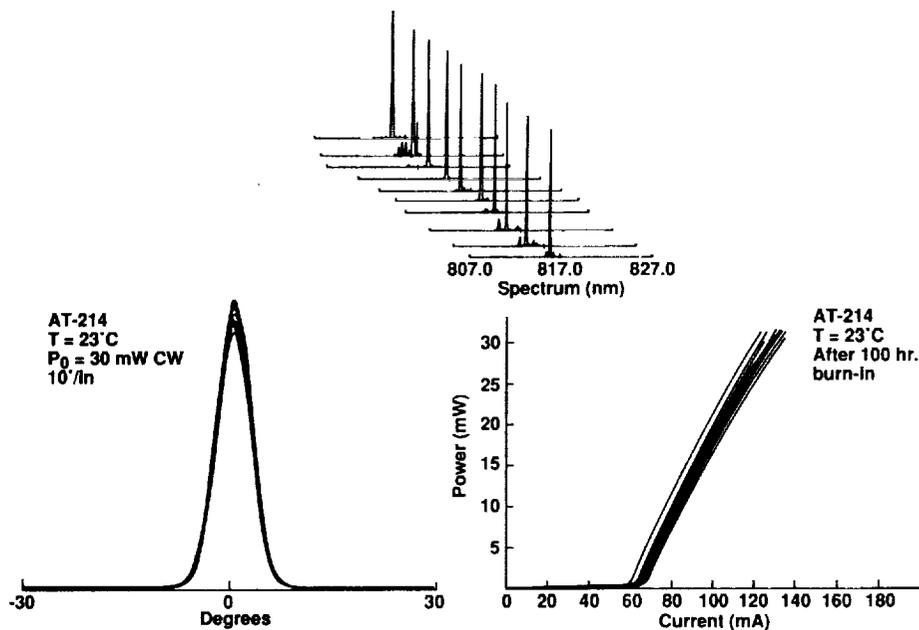
Figure II-13. Characteristics of diode array suitable for magneto-optic (MO) recording (far-field pattern, P-I characteristics, and spectral emission).

The subject of rollover in the P-I curve was of major concern, and at one point it was assumed to be caused by the poor thermal conductivity (high thermal resistance) of the SiO_2 dielectric layer that is used as a zinc diffusion mask. This layer is normally not removed because it helps in lateral current confinement. Silicon nitride, Si_3N_4, has a thermal resistance that is about 16 times lower than SiO_2, and may, in principle, help make a better device.

In addition to the individual element yield, the array must be considered as well. The array yield is the number of "good" arrays obtained from a wafer. It is a function of the single device yield, and it is significantly lower than if by virtue of the fact that not only the required number of devices in a given array is high, but

also that the devices must be *adjacent* to one another. Mathematically, the overall yield or probability of getting arrays that meet out prescribed requirement by counting the number of possible situations that would satisfy our requirements as a fraction of the total number of possibilities. This is done in the Appendix. The result is that, in order to obtain a high array yield, the individual element yield should be as high as possible. *If the individual element yield cannot be made close to 100%, then either one should design a system for fewer good elements per array, or the whole bar should be tested for the desired number of good adjacent elements prior to dicing the arrays.*

Section III

I-CSP AND MOCVD GROWTH

A. DESIGN AND FABRICATION

We have seen that the CSP structure is not self-aligned, and that its performance is critically affected by the alignment between the V-channel and the zinc diffusion stripe. We also know that LPE growth is not uniform. Both growth uniformity and stripe alignment affect the yield of individual CSP lasers. Also, a low individual yield results in a much reduced ten-diode array yield. A structure is desired that is self-aligned and that can be grown by MOCVD. This process provides uniform growth with increased individual yield can be increased. The inverse CSP (I-CSP) has the desired characteristics, and it can be designed in a double heterojunction (DH) or a quantum well (QW) configuration. Each configuration has its own advantages. The DH, with active layer thickness 500 Å to 800 Å has higher saturation power and narrower perpendicular far-field divergence than the QW, but the QW has lower threshold current and higher differential quantum efficiency. Effort to reduce the perpendicular far-field of the QW will require some trade-off with the threshold current. However, this is not objectionable, since the threshold current of the QW device is already quite low. Both the configurations are viable I-CSP approaches. A QW I-CSP laser structure grown at Sarnoff is illustrated in Fig. III-1
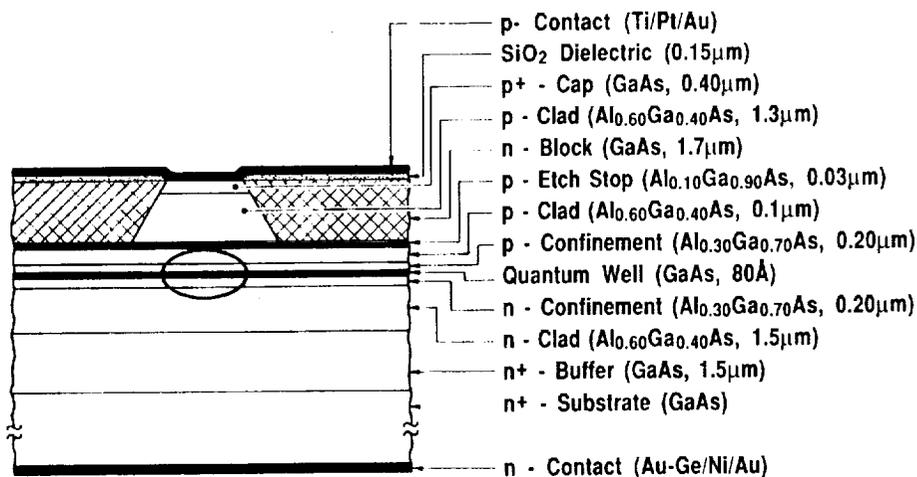
Figure III-1. Schematic diagram of the QW I-CSP structure.

Basically, the QW I-CSP is a laser structure in which the p-clad outside of the stripe is partially replaced by a layer that absorbs light at the laser emission wavelength, in order to obtain the loss-guiding characteristics of CSP that result in single lateral mode at high power. In AlGaAs lasers, the absorber can be GaAs. It is created by regrowth after an etching step that removes the p-clad everywhere except along a ridge or mesa that defines the laser waveguide. The regrown GaAs is illustrated by the crosshatched portions of the figure. To provide thickness uniformity for the confining p-clad and regrown layers at the waveguide wings, an etch-stop layer is incorporated in the structure. It is a thin (0.03 μm) layer of AlGaAs containing a small fraction (about 10%) of aluminum to prevent absorption in the region above the waveguide. The p-clad has a high aluminum content (60%). The ridge is defined using a SiO$_2$ mask and lithography to expose the high aluminum content p-clad outside the ridge, and the exposed area is etched with a differential etch, such as diluted hydrochloric acid at 0°C. This solution etches rapidly the p-clad, but it does not affect the low aluminum content etch stop and, therefore, the etching depth is the same throughout the wafer. The etch stop layer is not necessary if ion beam milling is used for etching or removal of the p-clad. Following etching and cleaning, the wafer is reintroduced in the reactor and a n-doped GaAs layer is regrown in the etched regions, then the wafer is metallized. The n-doping causes the regrown region to be reverse biased region when current is applied to the structure. Thus, it functions as a blocking layer that confines the applied current to the lasing region only. A sketch of an I-CSP array on a BeO submount is shown in Fig. III-2.
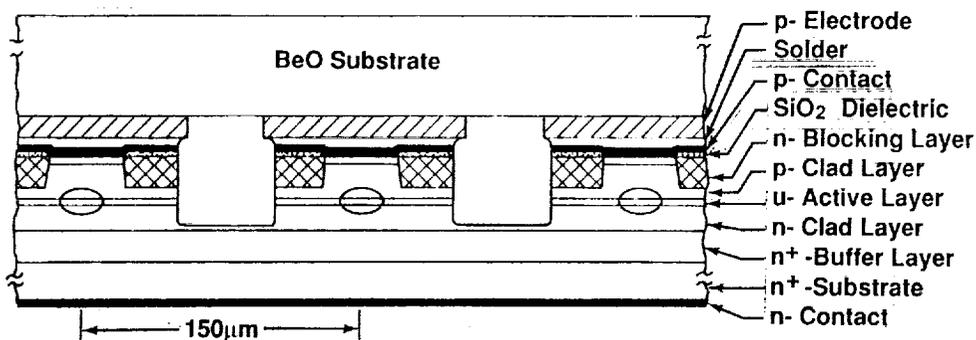
Figure III-2. Monolithic I-CSP array on a BeO submount.

Figure III-3a-c shows actual photographs of cross-sections of the I-CSP structure at various stages of fabrication. Figure III-3a represents the structure after etching the p-clad, leaving the mesa structure covered with the SiO_2 mask. Figure III-3b shows a planar structure obtained after regrowth. The SiO_2 has been left on the mesa to prevent epitaxial growth over the mesa. Figure III-3c shows the completed device, with a Ti-Pt-Au contact layer over the whole wafer.

A top view of the processed wafer after regrowth is shown in Fig. III-4a, and the region near a stripe in the SiO_2 mask is shown in Fig. III-4b illustrating the uniformity of the regrown layer and the absence of growth on the SiO_2 mask.

Figure III-5 is a block diagram of the process flow from start of growth to completion of ten-diode arrays. The process is straight-forward except that some care must be exercised to remove contamination of the etched areas prior to regrowth.

An interesting feature of I-CSP structures is that some performance tests can be made immediately after the creation of the ridges to ascertain growth quality. Figure III-6 illustrates a ridge laser made simply by metal coating a portion of the wafer. This step has been used to show that our QW I-CSP structures have low threshold and linear characteristics to beyond 30mW cw with high differential quantum efficiency at room temperature. Such characteristics are shown in Fig. III-7, demonstrating threshold of 12 to 15 mA, and only about 40 mA of drive current for output power of 30 mW. The perpendicular far-field radiation pattern has a full width half power (FWHP) of 50°. In order to reduce to 30°, it will be necessary to reduce the confinement layer thickness, at the expense of the confinement factor, which affects quantum efficiency. However, there is room for trade-offs, since the quantum efficiency is already approximately twice as high as that of the CSP.

Figure III-8 shows the calculated dependence of the perpendicular beam divergence on the confinement layer thickness. To get 30° perpendicular beam divergence, the confinement layer thickness should be about 0.05μm.
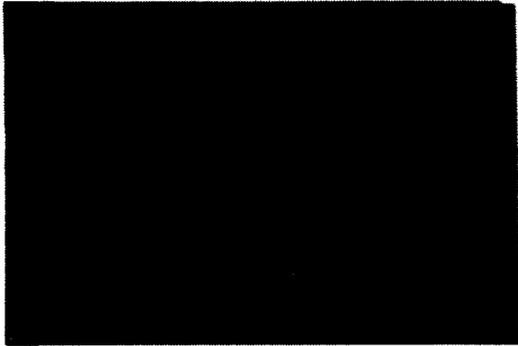
a) Base Structure Showing ICSP MESA
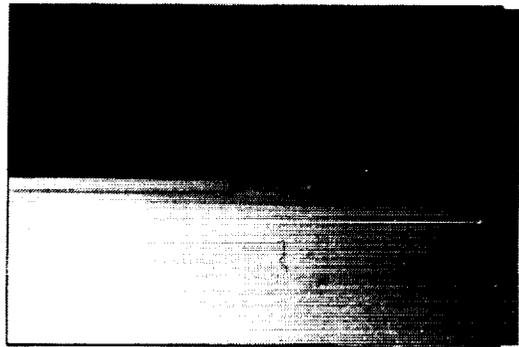
b) After MOCVD Regrowth with SiO$_2$ Still in Place

Figure III-3.   Photographs of I-CSP cross-section at various processing stages. a) etched mesa, and b) after MOCVD regrowth.
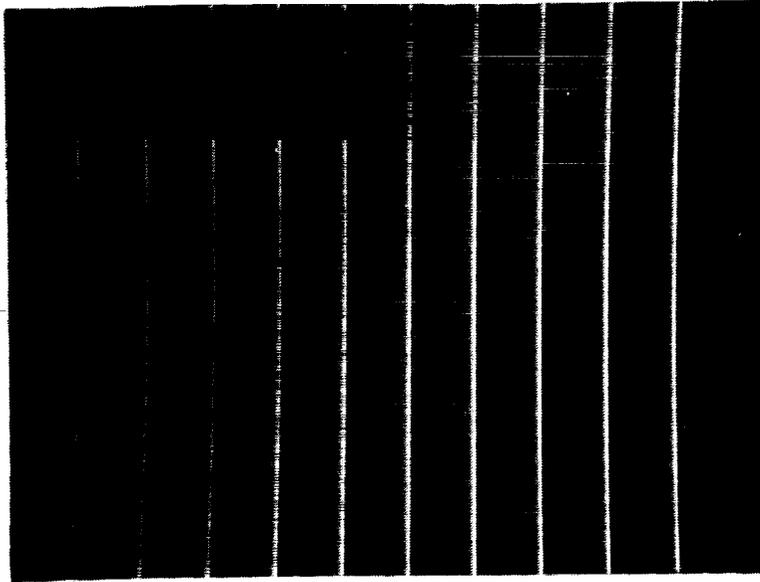
**Wafer Surface
After MOCVD
Regrowth**

$\vdash\!\!\!-\!\!\!-\!\!\!\dashv$
300 μm
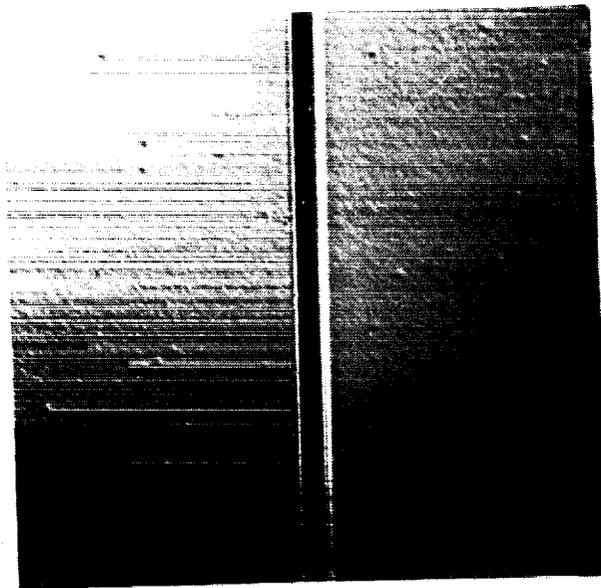
**Single Element
With SiO$_2$ Mask**

$\vdash\!\!\!-\!\!\!\dashv$
25 μm

Figure III-4.   Top view of processed wafer. a) after regrowth, b) stripe in SiO$_2$
mask showing no regrowth over SiO$_2$.

```
START           MOCVD Growth    3 μm stripe      5 μm stripe
GaAs Sub.  -->  QW         -->  Zn Diffusion --> Photoresist/SiO2
                Laser Structure

                                                      |
                                                      v
5 μm Contact Stripe    MOCVD Growth           Ion Beam Milling
Photoresist/SiO2   <-- Current Blocking   <-- ICSP Mesa
                       Layer

   |
   v
E-Beam p-side      Thin wafer              Device Isolation
metallization  --> Chemical/Mechanical --> Ion Beam Milling
                   (100 μm)                (100 μm)

                                                |
                                                v
                                           E-Beam n-side
                                           Metallization

                                                |
                                                v
Individually           Mount, Test, and    Probe Test      Cleave/Coat
Addressable Ten    <-- Characterization <-- Evaluation  <-- Emitting Facets
Diode ICSP Laser
Array
```

Figure III-5.   Process steps for I-CSP arrays.

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p- Contact (Ti/Pt/Au)
SiO$_2$ Dielectric (0.15μm)
p$^+$ - Cap (GaAs, 0.40μm)
p - Clad (Al$_{0.60}$ Ga$_{0.40}$ As, 1.3μm)
p - Etch Stop (Al$_{0.10}$ Ga$_{0.90}$ As, 0.03 μm)
p - Clad (Al$_{0.60}$ Ga$_{0.40}$ As, 0.1μm)
p - Confinement (Al$_{0.30}$ Ga$_{0.70}$ As, 0.20μm)
Quantum Well (GaAs, 80Å)
n - Confinement (Al$_{0.30}$ Ga$_{0.70}$ As, 0.20μm)
n - Clad (Al$_{0.60}$ Ga$_{0.40}$ As, 1.5μm)
n$^+$ - Buffer (GaAs, 1.5μm)
n$^+$ - Substrate (GaAs)

n - Contact (Au-Ge/Ni/Au)
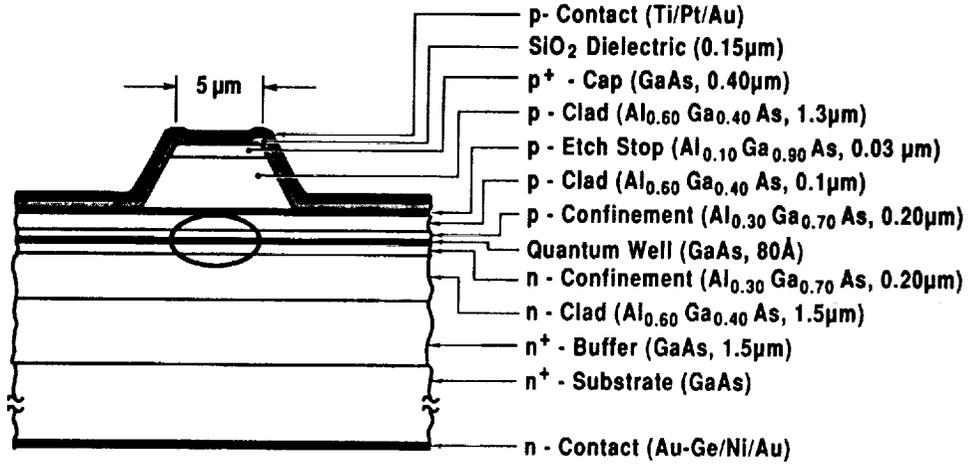
Figure III-6. Ridge laser made from I-CSP structure to evaluate wafer growth quality.
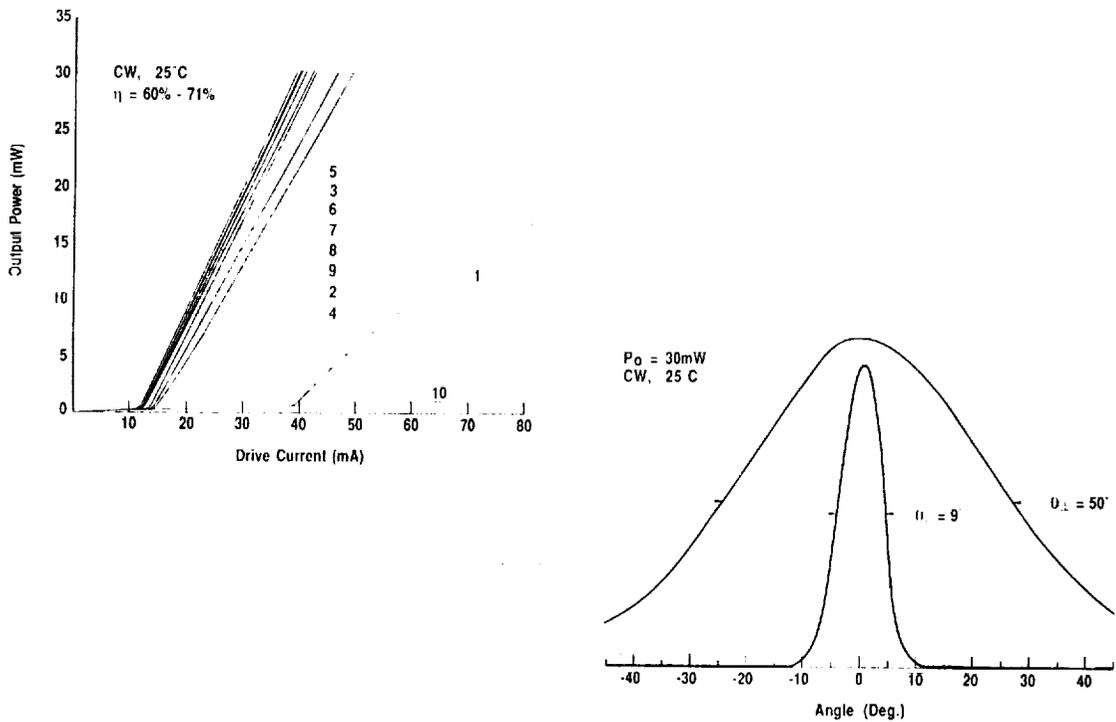
Figure III-7.   Characteristics of ridge laser array made from I-CSP structure, showing low threshold and linearity at high power (Diodes No. 1 and No. 10 were damaged in handling).
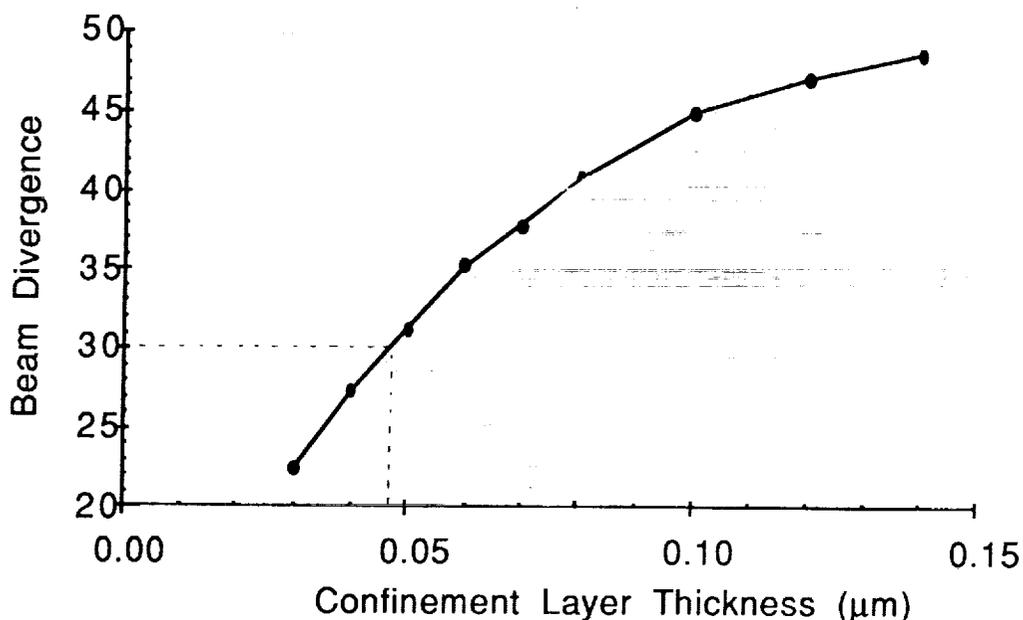
Figure III-8. Calculated dependence of beam divergence on confinement layer thickness for QW lasers.

B. REGROWTH OVER AlGaAs

It is not as easy to regrow over AlGaAs as it is to regrow over GaAs. The formation of native oxide on AlGaAs when exposed to air impedes epitaxial growth over it. Therefore, the oxide or surface impurity must be removed prior to regrowth, a step that must be done inside the MOCVD growth reactor. This problem can be encountered for the I-CSP where a layer of GaAs is regrown over an etch-stop layer containing 10% of aluminum, or over a portion of p-clad material. One approach to solving this problem is to chemically etch the region of the wafer slated for regrowth, then to bake the wafer in the reactor at high temperature (about 850°C) in a reducing atmosphere of hydrogen to remove the oxide, while using an over-pressure of arsine to prevent the evaporation of arsenic from the material. The amount of etch and the length of bake depend on the thickness of the native oxide. Excessive etch or prolonged baking time would remove too much material and destroy or dissolve the thin etch stop and confining layers in the I-CSP structure.

For the first experimental regrowth of I-CSP lasers, we used our experience with DFB laser regrowth. Our DFB lasers were made by regrowth of material over a grating that has been prepared by photolithography and etching. The grating fabrication process leaves impurities as well as native surface oxide, and a baking duration of about 30 minutes was found desirable in order to regrow successfully over the grating. Initially, the same assumption regarding impurities and native oxide was made for the I-CSP, and upon testing the finished devices we found them to be non-lasing or to require large currents to operate, although ridge structures made from the same material had produced low threshold lasers. Microscopic examination of angled-lap sections of the wafer indicated that the p-confining and the active layers had disappeared from the regrowth region.

We have learned that the pre-regrowth treatment of the I-CSP wafers should not be as drastic as that for DFB lasers. In particular, although pre-bake is desired, its time duration should be much less than for DFB lasers because of the low aluminum content of the etch-stop layer. We have now successfully achieved the desired regrowth, and we have successfully tested several two-diode I-CSP arrays.

C. RESULTS

Figure III-9 shows the characteristics of I-CSP two-diode QW arrays after regrowth. There are three important points to be noted in this data. The first and most important one is that the arrays were mounted in the junction up (p-up) configuration in a standard TO-46 package. The second point is that the threshold current for this regrown structure is 15 mA, which is the same as for the ridge waveguides. The third point is that the diodes have linear characteristics well beyond 30 mW cw. This demonstrates Sarnoff's ability to make high-power, low-threshold I-CSP lasers. These diodes exhibited single mode operation in both the longitudinal (Fabry-Perot) and spatial (waveguide) characteristics. The far-field radiation patterns were 9° by 34°, close to the final array specifications, and we expect to reduce the layer angle to below 30° by using a double QW structure. The p-up operation is possible because of the low threshold and low operating current (57 mA and 70 mA respectively for 30 mW cw). These diodes were driven to 100 mW cw in this p-up configuration, and their operation was kink-free (single mode) to beyond 50 mW cw.

From the results obtained so far on several two-diode arrays, we estimate the yield and reproducibility to be significantly higher for the I-CSP than for the ordinary CSP. We plan to develop this technology further and perform work toward the fabrication of 9 or 18-element arrays with 100 μm spacing (instead of 150 μm).
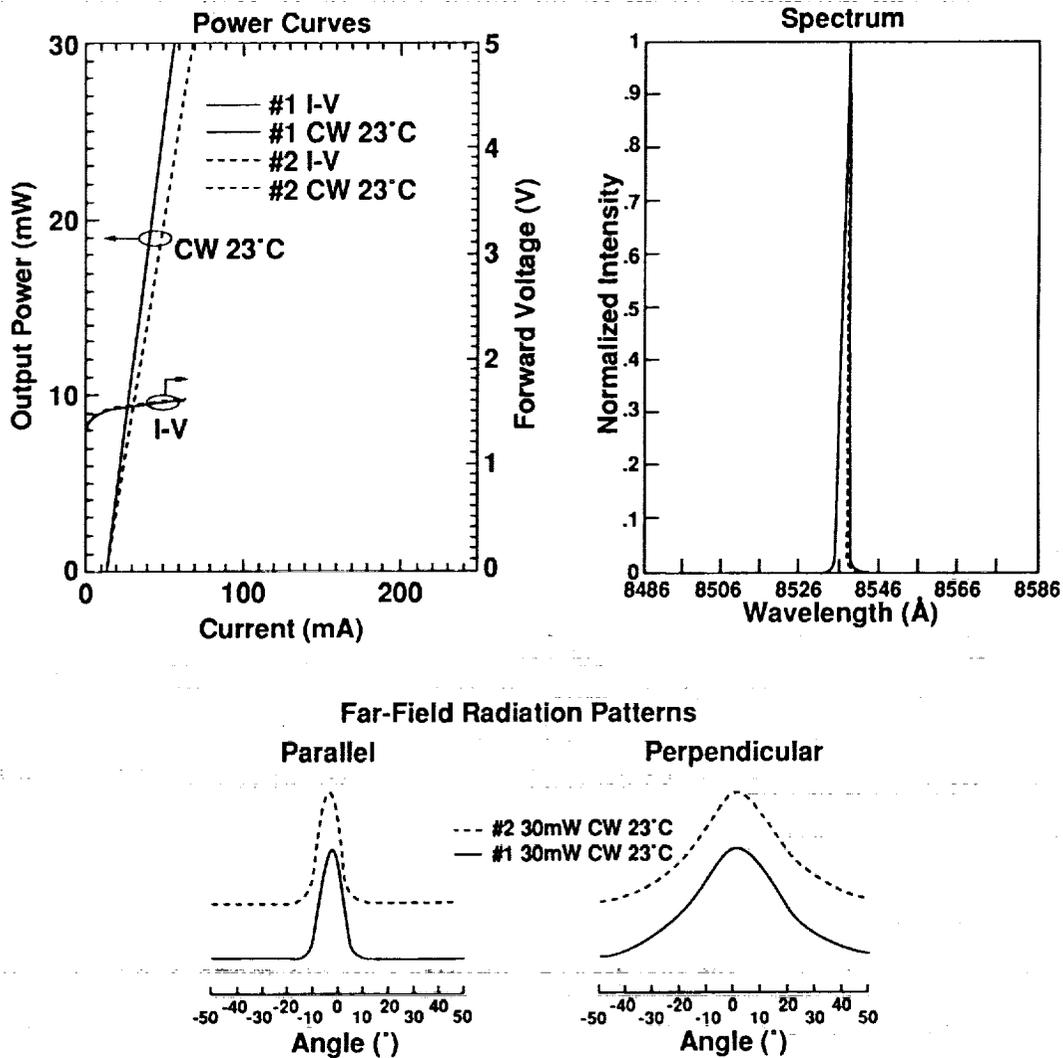
Figure III-9. Light-current characteristics, spectra, and far-field radiation patterns of two-diode QW I-CSP array.

Section IV

CONCLUSION

We have conducted an extensive development study of monolithic individually addressable 10-diode laser arrays for NASA's high-performance 10 GB capacity 300 Mbps magneto-optic read-write recorder. The arrays have stable output power exceeding 30 mW, with a high degree of uniformity among the elements. Most of the development work was focused on the CSP structure. This structure was chosen because its waveguiding characteristics make it suitable for high output power in a single lateral mode. We delivered three ten-diode arrays to NASA, and one of them was used in a technical demonstrator unit (TDU) at GE in Camden, NJ to demonstrate, for the first time, simultaneous operation (write, read, erase) for eight data channels and one tracking channel, at a user data rate of 133 Mbit/s.

The CSP structure, grown by LPE, was considered a suitable laser structure for the SODR because preliminary studies had indicated that it was capable of producing high single-mode output power in a single-element configuration. Our effort to fabricate, characterize, burn-in, and lifetest CSP 10-diode arrays was extensive. However, both the wafer yield and the array yield were found to be very low for the required level of performance. Extensive modeling and experiments indicate that the alignment of the zinc diffusion stripe, with respect to the channel, is required to be to within a fraction of a micron in order to achieve the required performance in an array. This alignment difficulty is the chief reason for the low yield of high performance arrays for this program. A statistical analysis was used to estimate the yield of individual diodes from the observed array yield and to outline procedures to increase array yields in general. The result of this analysis will be useful in the design of future arrays. Despite the low yield and the realization that a different structure, such as the I-CSP grown by MOCVD, could be more desirable, it was necessary to continue the CSP work in order to make enough arrays available for the TDU.

The I-CSP is a ridge or mesa structure with a regrown layer of GaAs between the mesas, provides optical guiding in the same manner as the CSP. It is self-aligned and can be grown by MOCVD. For both of these reasons, it is likely to have a higher yield than the CSP. The development work on I-CSP was accelerated at the conclusion of the CSP work. First, QW ridge laser arrays were

made to ascertain the low threshold current (15mA) characteristics and the low current (40 mA) required to obtain 30 mW cw output power. Then, following the development of the regrowth procedure, we successfully made 2-diode arrays that had similar characteristics as the ridges while in a p-up mounting configuration. This is considered significant because it demonstrates not only our capability to make this new structure with high performance and reproducible characteristics, but also that the power dissipation is low enough to allow p-up mounting. This could eliminate the use of a BeO submount and its related alignment complications.

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Appendix

APPENDIX

YIELD ANALYSIS OF LINEAR DIODE ARRAYS

The yield for monolithic individually addressable CSP ten-diode arrays is low. The purpose of this Appendix is to quantitatively assess this and indicate steps that can be taken to improve it.

There are two principal factors to be considered in the assessment of yield for monolithic multi-element laser diode arrays: the individual element yield, and the yield for a number of such elements to be contiguous in an array. The individual yield is the number of "good" elements obtained in a wafer. In the case of CSP lasers, it depends on the LPE growth, the alignment of the zinc diffusion stripe (lithography) and the processing steps themselves. LPE growth affects the yield because it is non uniform. Stripe misalignment is responsible for rollover and kink in the P-I characteristics and makes the devices unable to reach rated power. Processing, i.e., the steps that include metallization, cleaving and facet coating, may have several pitfalls. In particular, poor metallization may lead to bonding difficulties and high thermal resistance which causes heating.

The array yield is the number of "good" arrays obtained from a wafer. It is a function of the single device yield, but it is significantly lower than if by virtue of the fact that the devices must be *adjacent* to one another. Consider, for example, a ten-diode array. There are eleven ways to get at least 9 good elements in it: one perfect 10-element array, and ten ways to get *any* nine elements (the bad element can occupy any one of 10 positions). However, there are only three ways to get 9 *contiguous* elements: one perfect array and two having all good elements except the first or the last element. Similar counting procedures can be used to calculate the yield of 9 contiguous elements in a population higher than ten. A large number would be obtained.

Mathematically, this yield (probability) can be calculated by counting the number of situations that satisfy a given condition as a fraction of the total number of possibilities. Let p be the yield of "good" diodes, i.e., the yield of individual diodes meeting our requirements. Let G be the desired number of contiguous good diodes, and let N be the number of diodes in an array cleaved from a wafer. N is greater than or equal to G. We assume that if N > G, then, only the G contiguous devices will be used in the optical recorder, and that the "bad" portion of the array can be cleaved off and discarded. Then the probability

P(G,N) of getting G contiguous or adjacent devices from a population (array size) of N is given by the formula:

$$P(G,N) = \sum_{r=G}^{N} \binom{N}{r} p^r (1-p)^{N-r} \tag{A-1}$$

$$\cdot \left[1 - \frac{\sum_{s=1}^{S} \binom{N-r+1}{s} \sum_{i=0}^{I} (-1)^i \binom{s}{i} \binom{r-1-(G+1)i}{s-1}}{\binom{N}{r}} \right]$$

where $S = \min(r, N-r+1) \equiv$ minimum of r and N - r + 1,

$$I = \min \left(s \frac{r-s}{G+1} \right)$$

and where parentheses of the form $\binom{N}{r}$ represent the number of ways r objects can be chosen out of a group of N, i.e.,

$$\binom{N}{r} = \frac{N!}{(N-r)! \, r!} \tag{A-2}$$

In Eq. A-1, the terms on the left of the bracket represent the probability of obtaining G good devices in an array of N, given the yield p of good individual devices. The expression inside the large brackets represents the fact that only the configurations having contiguous devices are acceptable.

In practice, the wafer on which the devices are fabricated is 25 mm x 17 mm in size, and the diodes are processed in a pattern defined by masking and photolithography, so that the whole wafer is covered with diodes. The wafer is then cleaved into bars containing several arrays, and the facets of the bars are coated to the desired reflectances: 90% for the "back" facet, and 10% for the "front" facet. In general, there is a relatively large number M of diodes per bar, and each bar may contain several arrays of N elements. A typical bar has M = 44 to 48. After facet coating, the bars are cut into arrays of the desired length N and they are bonded on submounts.

Ideally the ratio M/N should be an integer. If it is not, then the excess diodes are wasted, and the array yield is reduced. The number of whole arrays of length N per bar of length M is thus given by TRUNC (M/N), i.e., the integer part of the ratio M/N. Thus, if M = 44 and N = 10, the number of arrays in the bar is TRUNC (44/10) = 4. On the other hand, if N = 12, then TRUNC (44/12) = 3, a smaller number. Thus, although the probability of obtaining a certain number G of good contiguous diodes in an array N increases with N, it is offset by the fact that TRUNC (M/N) is reduced if M is fixed. Therefore, the average number of good arrays per bar is $\bar{P}$ (G,N), given by

$$\bar{P} \ (G,N) = TRUNC \ (M/N) \ P \ (G,N) \qquad\qquad (A\text{-}3)$$

where TRUNC (M/N) decreases in integer steps as P(G,N) increases with increasing N, if M is constant

Our program requirement was to make arrays having nine (G = 9) contiguous good diodes in an array. In Fig. A-1, we plot $\bar{P}$ for G = 9 vs the number of diodes N per array cut from bars containing M = 44 diodes, with the yield of p of individual diodes as a parameter ranging from 0.4 to 0.9. Note the reduction effect of the truncation at N = 12, 15, and 23 where TRUNC (M/N) decreases by unity, leaving a wasted residual, offsetting the increase of yield with increasing N. We also show in Fig. A-2, similar curves for G = 5. The data also shows the importance of increasing the individual diode yield.
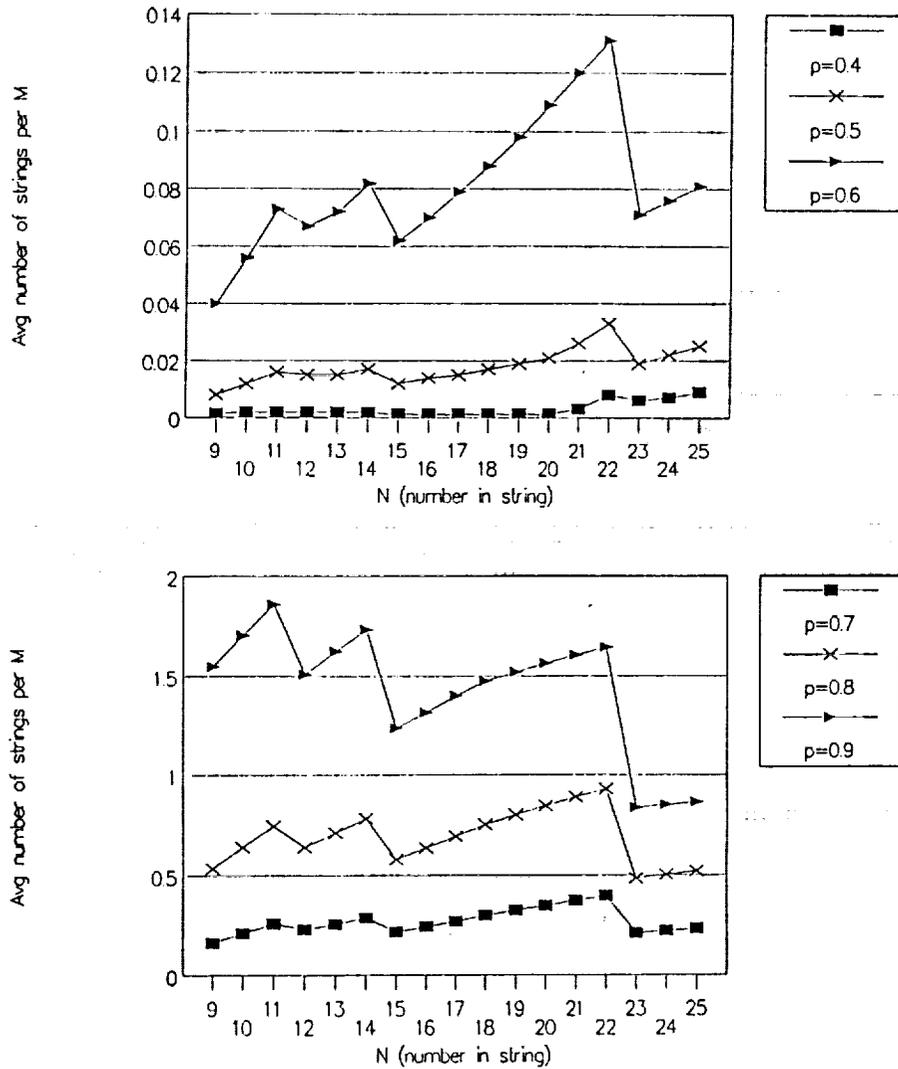
Figure A-1.   Average number of nine good adjacent diodes as a function of array size, with individual yield as a parameter. The arrays are cut from bars containing 44 diodes.

Conditions: G=5; M=44
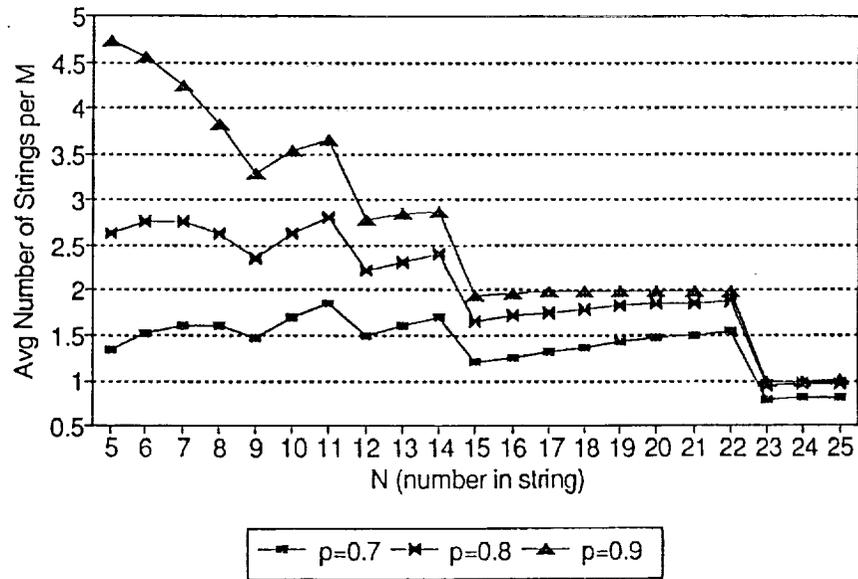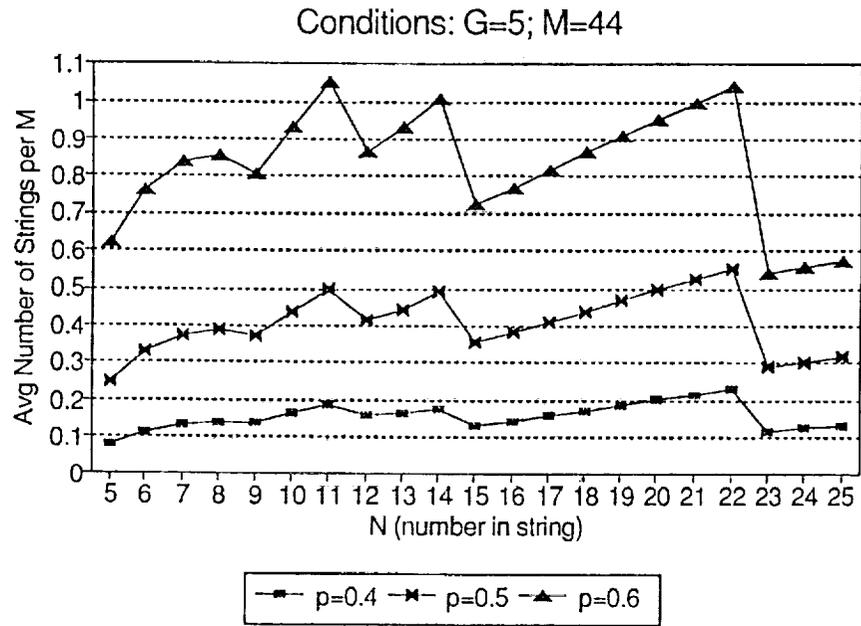
Figure A-2. Average number of five good adjacent diodes as a function of array size, with individual yield as a parameter. The arrays are cut from bars containing 44 diodes.

We can use the results of this analysis together with our own experimental data, to calculate the individual yield of CSP arrays and to determine a possible approach to obtain a reasonable number of good arrays. We recall that our ten-diode array yield was found to be about 0.7% (4 good arrays out of about 558) tested.

In Fig. A-3, we plot, as a function of individual diode yield, the yield of 9 good contiguous diodes from a 10-diode array and a 22-diode array, together with the yield of 5 good contiguous elements also from an array of ten elements and from an array of twenty-two elements. The data for these plots are taken from Fig. A-1 to Fig. A-2 for the given range of values of p, and the yields are obtained by dividing the average number by the appropriate value of TRUNC (M/N). The bottom curve, G9N10 is the yield for 9 good adjacent diodes in our ten-diode array as a function of individual diode yield. This data shows that the individual CSP yield was about 56%, in order for the array yield to be 0.7%.

This data also shows the importance of increasing the individual diode yield and the array size. For example, had we chosen N = 22 for this program (i.e., G9N22), our yield of 9 contiuous diodes per array would have increased from 0.7% to 3%. As another example, if the required number of good elements were only 5, then with the same individual yield, the array yield would go up to 14% for N=10 and to almost 30% for N=22. For all cases, the array yield increased rapidly as the individual yield is improved. The conclusion from this study is very clear. Efforts should obviously be made to get the highest possible individual yields. *If the individual element yield cannot be made close to 100%, then either one should design a system for fewer good elements per array, or the whole bar should be tested for the desired number of good adjacent elements prior to dicing the arrays. Future test sst-ups should be designed with the capability to probe test larger arrays than the one (N = 10) that was built for this program.*
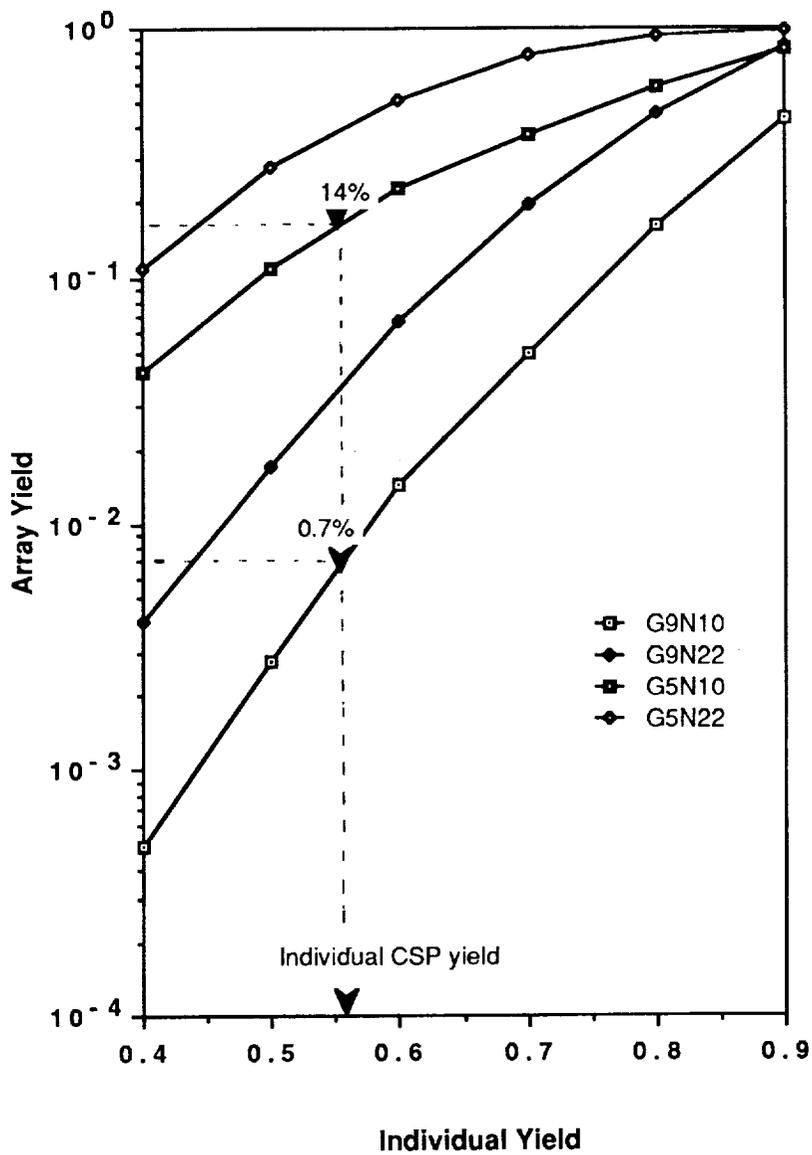
Figure A-3. Yield of five and nine good adjacent elements in arrays containing 10 and 22 elements, respectively, as a function of individual yield.

NASA Report Documentation Page

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
NASA CR-182098		

4. Title and Subtitle	5. Report Date
Linear Laser Diode Arrays for Improvement in Optical Disk Recording	December 1990
	6. Performing Organization Code

7. Author(s)	8. Performing Organization Report No.
G.A. Alphonse D.B. Carlin J.C. Connolly	
	10. Work Unit No.
	506-44-21-01

9. Performing Organization Name and Address	11. Contract or Grant No.
David Sarnoff Research Center CN 5300 Princeton, NJ 08543-5300	NAS-1-18226 Task No. 7
	13. Type of Report and Period Covered
12. Sponsoring Agency Name and Address National Aeronautics and Space Administration Langley Research Center Hampton, Virginia 23665-5225	Contractor Report Sept.2, 1989 to June 30, 1990
	14. Sponsoring Agency Code

15. Supplementary Notes

Langley Technical Monitor: H.D. Hendricks

Final Report - Task 7

16. Abstract

   We report on the development of individually addressable laser diode arrays for multitrack magneto-optic recorders for space stations. Three multi-element channeled-substrate-planar (CSP) arrays with output power greater than 30 mW with linear light vs current characteristics and stable single mode spectra were delivered to NASA. These devices have been used to demonstrate for the first time the simultaneous recording of eight data tracks on a 14-inch magneto-optic erasable disk. The yield of these devices is low, mainly due to non-uniformities inherent to the LPE growth that was used to fabricate them. However, we have recently developed the inverted CSP, based on the much more uniform MOCVD growth techniques, and have made low threshold quantum well arrays requiring about three times less current than the CSP to deliver 30 mW cw in a single spatial mode. The inverted CSP is very promising for use in space flight recorder application.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
Laser, semiconductor laser, laser array, magneto-optic, optical recording	Unclassified - Unlimited Subject category 34

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of pages	22. Price
Unclassified	Unclassified	54	A04

NASA FORM 1626 OCT 86