SILICON DEVICE PERFORMANCE MEASUREMENTS TO SUPPORT TEMPERATURE RANGE ENHANCEMENT

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Performance of Semiconductor Power Devices at High Temperature

INTRODUCTION

Semiconductor power devices are typically rated for operation below 150°C. Space based power systems typically generate high currents at low voltages, with attendant temperature increases. To reduce losses and weight associated with such requirements, it would be advantageous to locate the power conversion and conditioning electronics as close to the primary source as possible. Location, however, is limited by the local temperature generated by the power source. Electronics capable of operating at higher temperatures could be placed nearer the power source. In addition, conversion and conditioning electronics produce significant heat which must ultimately be removed. Enhanced temperature electronics would result in a higher heat rejection temperature for the thermal management system resulting in a reduction in the size of the thermal radiators, decreasing launch weight.

Little data are available for power semiconductors over 150°C. In most cases, the device is derated to zero operating power at 175°C. At the high temperature end of the temperature range, the intrinsic carrier concentration increases to equal the doping concentration level and the silicon behaves as an intrinsic semiconductor. The increase in intrinsic carrier concentration results in a shift of the Fermi level toward mid-bandgap at elevated temperatures. This produces a shift in devices characteristics as a function of temperature. By increasing the doping concentration higher operating temperatures can be achieved. This technique has been used to fabricate low power analog and digital devices in silicon with junction operating temperatures in excess of 300°C. Additional temperature effects include increased p-n junction leakage with increasing temperature, resulting in increased resistivity. The temperature dependency of physical properties results in variations in device characteristics. These must be quantified and understood in order to develop extended temperature range operation.

LABORATORY SETUP

A variety of equipment is needed to characterize the relevant devices parameters. The instrumentation in the lab is linked using an IEEE-488 (GPIB) interface and a PEP-301 (80386-16 compatible) computer, for automated testing and data acquisition. Table 1 lists the equipment (hardware and software) available to perform the tests and the GPIB address of each device. The general layout of the lab is shown in Figure 1. Connections to the DUT (device under test) are made using Teflon insulated wire, to withstand temperatures up to 200°C.

DEVICES UNDER TEST

The devices were chosen for similar current carrying capability (approximately 50A). (see Table 2)

DEVICE MEASUREMENTS

The software for each of testing procedures included the same temperature control subroutine. This subroutine instructed the test chamber to bring the ambient temperature within +/-0.2°C of the desired test temperature. This temperature was then held for 5 minutes to allow the entire device to achieve the ambient chamber temperature. The individual test was then performed and the temperature raised. The test temperatures ranged from 20°C to 200°C in 10°C increments.

Test performed using the TEKTRONICS 371 high power curve tracer utilized pulse current measurement. The pulse rate (half amplitude pulse width) employed by the curve tracer is 250us +/- 10%, with a rise/fall time of 40us to 120us. The repetition rate is 0.25 times the line frequency at power levels of 3kW and 0.5 times the line frequency at power levels of 300W.

RESULTS

In high voltage and current switching applications, the saturation voltage V_{CEsat} can be a crucial design parameter. Saturation voltage, and collector current play a major role in determining the transistor losses. Figure 2 illustrates the Collector-Emitter saturation voltage and its temperature dependance. This test was conducted using the TEKTRONICS 371 high power curve tracer. In accordance with the data sheets supplied, V_{CE} was measured at a forced Beta of 10, using I_B=5A and I_C=50Hx

Under normal switch or inverter conditions, the major part of the voltage drop across the transistor occurs in the nonconductivity modulated region close to the N^+ layer. This voltage drop is given by:

$$V_{IR} = \frac{I_C \rho_{epi} W_R}{A}$$

where w_R=W_b-x_o (W_b- base width, x_o- oxide thickness). The value of internal base-collector voltage due to injection of the hole concentration $p(W_b)$ is given under high level injection by:

$$V_{BC}=2V_t\ln[\frac{p(W_b)}{n_i}]$$

Assuming that the base has also entered the high injection level, the base-emitter voltage is given as:

$$V_{CEsat}=V_{BE}-V_{BC}+\frac{I_C\rho_{epi}W_R}{A}$$

and the total value of collector-emitter saturation voltage is thus:
The temperature dependance of these equations can be shown by the temperature dependance of the intrinsic carrier concentration, n_i, where:

$$n_i=\sqrt{N_CN_V}e^{-(E_G/2kT)}$$

the "effective" densities of conduction and valence band states are:

$$N_C=2[\frac{2\pi m_n^*kT}{h^2}]^{3/2}$$

$$N_V=2[\frac{2\pi m_p^*kT}{h^2}]^{3/2}$$

and the energy bandgap ($E_G=E_C-E_V$) is:

$$E_G(T)=E_G(0)-\frac{\alpha T^2}{T+\beta}$$

(in silicon $E_G(0)$ = 1.170eV, alpha = 4.73×10^{-4}, beta = 636)
The resistivity of the epitaxial layer:

$$\rho_{epi} \sim \frac{1}{q\mu_n N_{epi}}$$

where the electron and hole mobilities are determined using the equations:

$$\mu_n = 88T_n^{-0.57} + \frac{7.4\times10^8 T^{-2.33}}{1+[N/(1.26\times10^{17}T_n^2.4)]0.88T_n^{-0.146}}$$

$$\mu_p = 54.3T_n^{-0.57} + \frac{1.36\times10^8 T^{-2.23}}{1+[N/(2.35\times10^{17}T_n^{2.4})]0.88T_n^{-0.146}}$$

where T_n=T/300. Without using exact values for the B-E and C-E junction hole and electron concentrations, and picking a estimated figure of $N_{epi}=10^{16}cm^{-3}$ for the epitaxial doping level, Table 3 demonstrates the increase in V_{CEsat} with temperature. The results calculated are similar to the measured data.

Table 3.

Temperature (deg C)	intrinsic carrier concentration n_i (cm^{-3})	epitaxial resistivity (ohm-cm)	delta V_{CEsat} (V)
20	4.85×10^9	0.4727	0.768
80	3.68×10^{11}	0.6961	1.127
140	8.42×10^{12}	0.9605	1.560
200	9.07×10^{13}	1.2689	2.062

Figure 3 illustrates Collector-Emitter leakage current as a function of temperature. This data was generated by applying a C-E voltage with the HP6030A power supply, shorting the base and emitter leads and reading the collector current with the TEKTRONICS DM5120 programmable digital multimeter.

I_{CE} is a measure of the reverse biased Collector-Base leakage current. The equation for the reverse bias saturation current in a p-n junction is shown below. It can be seen that the

intrinsic carrier concentration plays an important role in this equation.

$$I_o = qA\left[\frac{D_N}{L_N}n_{p0} + \frac{D_P}{L_P}p_{n0}\right] = qA\left[\frac{D_N}{L_N}\frac{n_i^2}{N_A} + \frac{D_P}{L_P}\frac{n_i^2}{N_D}\right]$$

The approximate fractional change in the leakage current of a reverse biased pn junction is given by:

$$\frac{1}{I_o}\left(\frac{\partial I_o}{\partial T}\right) = \frac{1}{2}\left(\frac{3}{T} + \frac{E_G}{\sqrt{N_C N_V}}\right)\Big|_{V_R\text{-constant}}$$

is approximately +8% per ^oC, or a doubling of leakage current for every 12^oC rise in junction temperature. Figure 3 shows the increase in leakage current with temperature but with an initial plateau. The flattening of the curve indicates saturation of a junction in the device, most likely due to a fabrication process in the device manufacture.

In the portion of the curve not effected by the saturation, (100^oC to 200^oC) the leakage current was found to follow the expected relationship. [I_{CE}(150^oC)=1.2x10^{-4}A I_{CE}(200^oC)=1.5x10^{-3}A (1.5x10^{-3} - 1.2x10^{-2})/50^oC = 2.76x10^{-5} A/^oC]

The results of the Emitter-Base leakage current versus temperature test are plotted Figure 4. This test also involves the leakage current in a reverse bias p-n junction. The data was generated by applying an emitter-base voltage using the PS5010 programmable power supply and measuring the leakage current using the DM5120 programmable digital multimeter. The device again demonstrated a saturation of leakage current in the lower temperature range. An initial increase in the V_{EB}=7V curve, indicates the onset of E-B junction breakdown. And again the non-saturated portion of the curve exhibits the leakage doubling effect. [I_{CE}(150^oC)=1.3x10^{-4}A I_{CE}(200^oC)=2.3x10^{-3}A]

The DC current gain of the bipolar transistor was measured using the TEKTRONICS 371 curve tracer at a constant V_{CE} of 2.6V, as per the device data sheet. Figure 3 shows a typical set of curves for this test. These curves show the peak in Beta as the generation and diffusion currents dominate the E-B junction, and the Beta "fall-off" due to high level injection, Kirk effect and/or the series resistance of the base and collector.

Using simplified equations for the operation under the normal "active region" bias, and considering the practical situation were $V_{BE} >> V_t$, we obtain the expression for dc current gain:

$$\beta_o = \frac{I_C}{I_b} \approx \frac{W_e D_n N_{De}}{W_b D_p N_{Ab}}$$

Table 4 shows the results of substituting estimated numbers for doping levels ($N_{Ab}=10^{16}cm^{-3}, N_{De}=10^{18}cm^{-3}$), assuming comparable values for emitter and base regions ($W_e=W_b=10^{-6}m$), then calculating the electron and hole mobilities, and the diffusion coefficients. The calculated values approximate the measured results.

Leakage current testing on the MOSFET device included Gate-Source leakage and Drain-Source leakage measurements. In both

Table 4.

Temperature (deg C)	mobility electron (cm^2/sec)	mobility hole (cm^2/sec)	diffusion coeff. electron (cm^2/sec)	diffusion coeff. hole (cm^2/sec)	Beta
20	246.3	467.5	6.222	11.810	52.7
80	232.8	325.8	7.084	9.914	71.5
140	218.4	241.5	7.779	8.598	90.5
200	203.7	187.6	8.305	7.649	108.6

cases, bias voltage was provided by the HP6030A power supply and the current read by the DM5120 digital multimeter.

Analysis of the Gate-Source leakage data indicated currents of less than 10nA (this data was lost in the noise resolution of our equipment) at all temperatures for a gate-source voltage range of +/-15V. This was deemed a negligible amount for any practical circuit design.

Drain-Source leakage measurements versus temperature were taken at gate-source voltages of 0V and -5V. Figures 6 and 7 show the results of the measurements. They exhibit the same doubling of leakage current for every 12°C as the bipolar leakage currents. [$I_{DS}(100°C)=10^{-7}A$, $I_{DS}(200°C)=4x10^{-4}A$]

The attempt to reduce the drain-source leakage by applying a negative gate-source voltage only reduced the current by a factor of two over the entire temperature range. For the negative biased gate-source data the drain-source voltage taken to a maximum of 40V to avoid exceeding the maximum rated drain-gate voltage.

The transfer characteristic curve of a MOSFET (I_D vs V_{GS}) shows how the saturated drain current varies with applied gate-source voltage for a constant value of drain-source voltage. There are three distinct regions on the device's transfer curve.

In the region close to the V_{GS} axis, a small amount of drain

current flows, but V_{GS} is below the MOSFET threshold voltage V_T this is known as the sub-threshold region. In the region farthest from the axis, the transfer curve becomes linear. This linearization is the result of the effect known as "velocity saturation". But the middle region is the most important. In this region, the drain current is proportional to the square of the difference between V_{GS} and V_T. Obviously a plot of $I_D^{1/2}$ versus V_{GS} in this region should be linear.

The data for the device's transfer curve was acquired from the TEKTRONICS 371 curve tracer at a V_{DS} of 5V. Figure 8 shows the data plotted as $I_D^{1/2}$ vs V_{GS} and the threshold voltage interpolated as the straight line intercept of the I_D=0A (V_{GS}) axis. Figure 9 depicts the calculated threshold voltages as a function of temperature. Using the equation for the square law region,

$$\frac{\partial I_D}{\partial T} = I_D\left[\frac{1}{\mu}\times\frac{\partial \mu}{\partial T}\times\frac{2}{V_{GS}-V_T}\times\frac{\partial V_T}{\partial T}\right]$$

and the equation for the next region (velocity saturated),

$$\frac{\partial I_D}{\partial T} = \frac{C_{OX}Z}{2}\left[(V_{GS}-V_T)\frac{\partial V_{SAT}}{\partial T} - V_{SAT}\frac{\partial V_T}{\partial T}\right]$$

The temperature dependance can be shown by:

$$\phi_F = -\frac{kT}{q}\ln(N_D/n_i)$$

$$V_T = 2\phi_F + \frac{K_S x_o}{K_O}\sqrt{\frac{4qN_A}{K_S\varepsilon_o}\phi_F}$$

It can be shown that the derivative magnitude of the MOSFET threshold voltage with respect to temperature is negative and reasonably constant at about -3 to -6mV/°C. (Figure 9, slope of -4.5mV/°C). The derivative of carrier mobility and saturation velocity are also both negative, although V_{SAT} is less sensitive to temperature than the mobility.

The temperature dependance of the threshold voltage can also be shown by the intrinsic carrier concentration and the doping concentration reference voltage.

$$\phi_F = -\frac{kT}{q}\ln[N_D/n_i]$$

$$V_T = 2\phi_F + \frac{K_S x_o}{K_O}\sqrt{\frac{4qN_A}{K_S\varepsilon_o}\phi_F}$$

On-resistance (R_{DSon}) and RMS drain current determine both the voltage drop and power loss in a MOSFET. There is a limit to the minimum resistance of the channel. As the gate-body potential is increase, more charge collects in the channel region. This charge acts like an electrostatic shield to reduce the field in the rest of the body. This action very closely resembles the effect of space charge in a vacuum tube which acts to reduce the electron emission from the cathode. In the MOSFET, the "space charge" acts to limit the additional charge in the channel so that the channel resistance quickly reaches it minimum.

Figure 10, On-Resistance Versus Temperature, was also generated with data from the TEKTRONICS 371 curve tracer, using a pulse I_D of 75A and a constant $V_{GS}-V_T$ of 6.5V.

Analysis of the V_{DS}, based on the bulk-charge theory results in:

$$V_{DS} = V_{GS} - V_T - V_W\left[\left(\frac{V_{GS}-V_T}{2\phi_F} + \left(1+\frac{V_W}{4\phi_F}\right)^2\right)^{1/2} - \left(1+\frac{V_W}{4\phi_F}\right)\right]$$

With $V_{GS}-V_T$ and I_D=75A held constant, the doping concentration reference voltage is the major contributor to the equation. As shown above the reference voltage has a negative temperature dependance, resulting in the increasing R_{DS} shown in Figure 10.

CONCLUSION

Although further testing is necessary, circuit design for elevated temperature utilizing both devices appears possible. Leakage currents for both devices increased but not beyond a usable range.

Future testing will include bipolar breakdown voltage and switching and life-testing under load for both the MOSFET and bipolar devices. Other devices to be investigated include the MOS-controlled thyristor (MCT) and the insulated gate bipolar transistor (IGBT).

Table 1.

Software	Description
TEK EZ-TEST	GPIB TEST DEVELOPMENT SOFTWARE FOR PERSONAL COMPUTERS
TEK GURU II	GPIB USER'S RESOURCE UTILITY FOR THE IBM PERSONAL COMPUTER
MICROSOFT	QUICK BASIC

Device Name	GPIB Primary address
TEK371	1
D2440	2
TK11401	4
HP6030A	5
AFG510	7
DM5120	8
DM5110A	16
DM5110B	17
PS5010A	22
PS5010B	23
DD9023	27

Table 2.

Device	Current	Voltage
NPN 2N6023	50A	150V
N-MOSFET RFH75N05E	75A	50V
MCT MCTA60P60	60A	-600V
IGBT TA9898	50A	500V

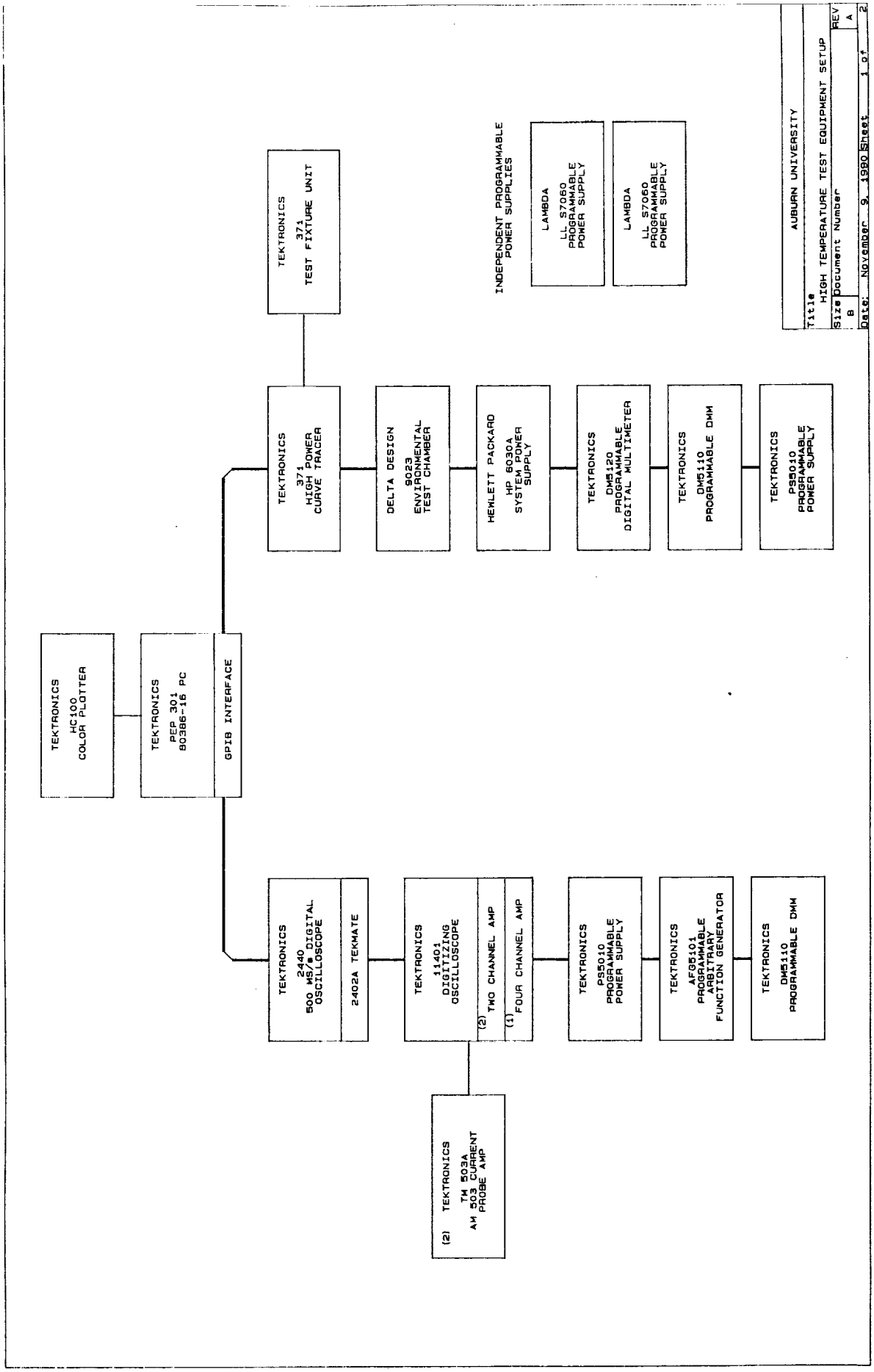

Figure 1.

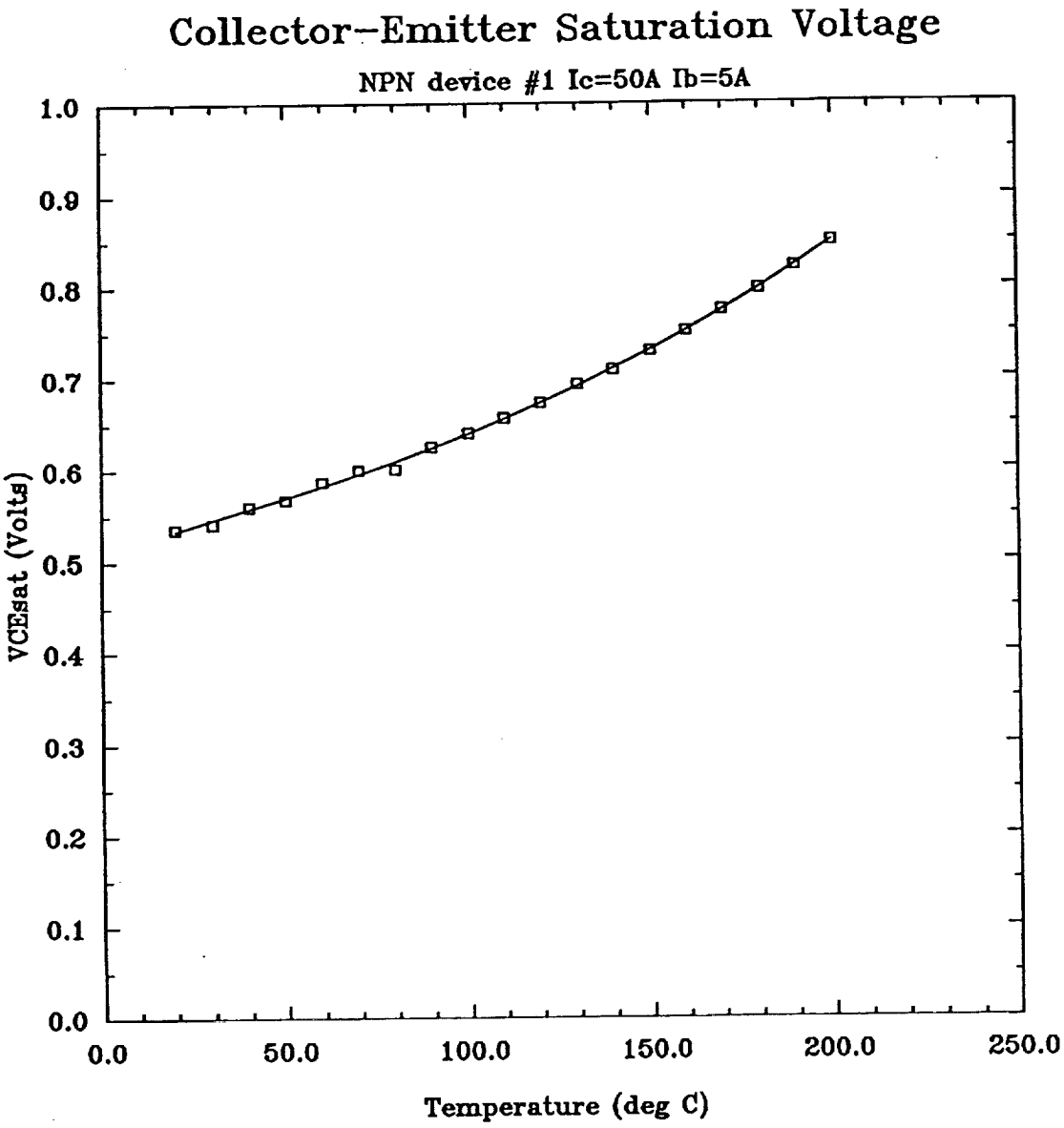
Collector–Emitter Saturation Voltage
NPN device #1 Ic=50A Ib=5A
VCEsat (Volts)
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0.0
50.0
100.0
150.0
200.0
250.0
Temperature (deg C)

Figure 2.

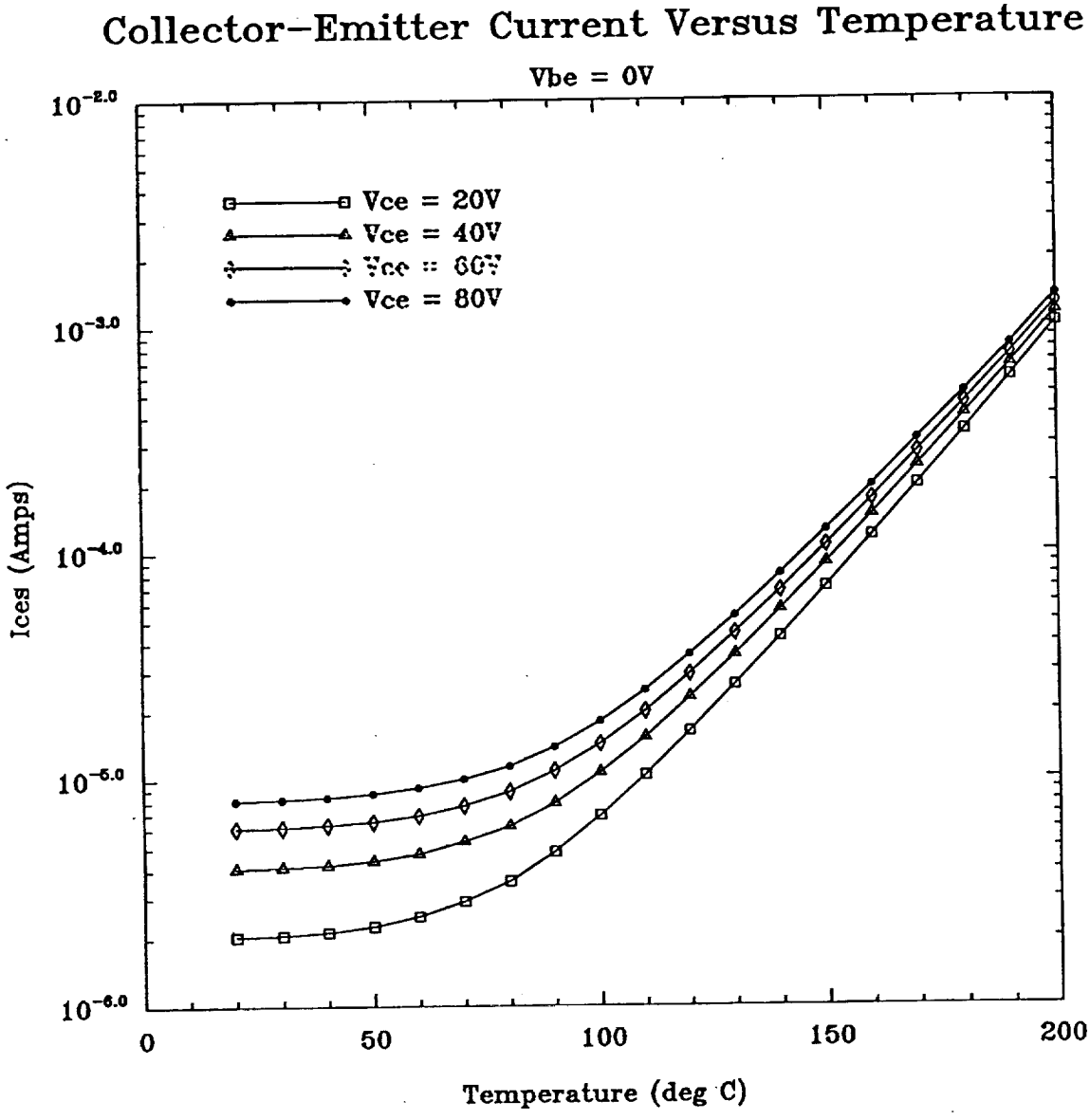
Collector–Emitter Current Versus Temperature
Vbe = 0V
Vce = 20V
Vce = 40V
Vce = 60V
Vce = 80V
Ices (Amps)
10^-2.0
10^-3.0
10^-4.0
10^-5.0
10^-6.0
0
50
100
150
200
Temperature (deg C)

Figure 3.

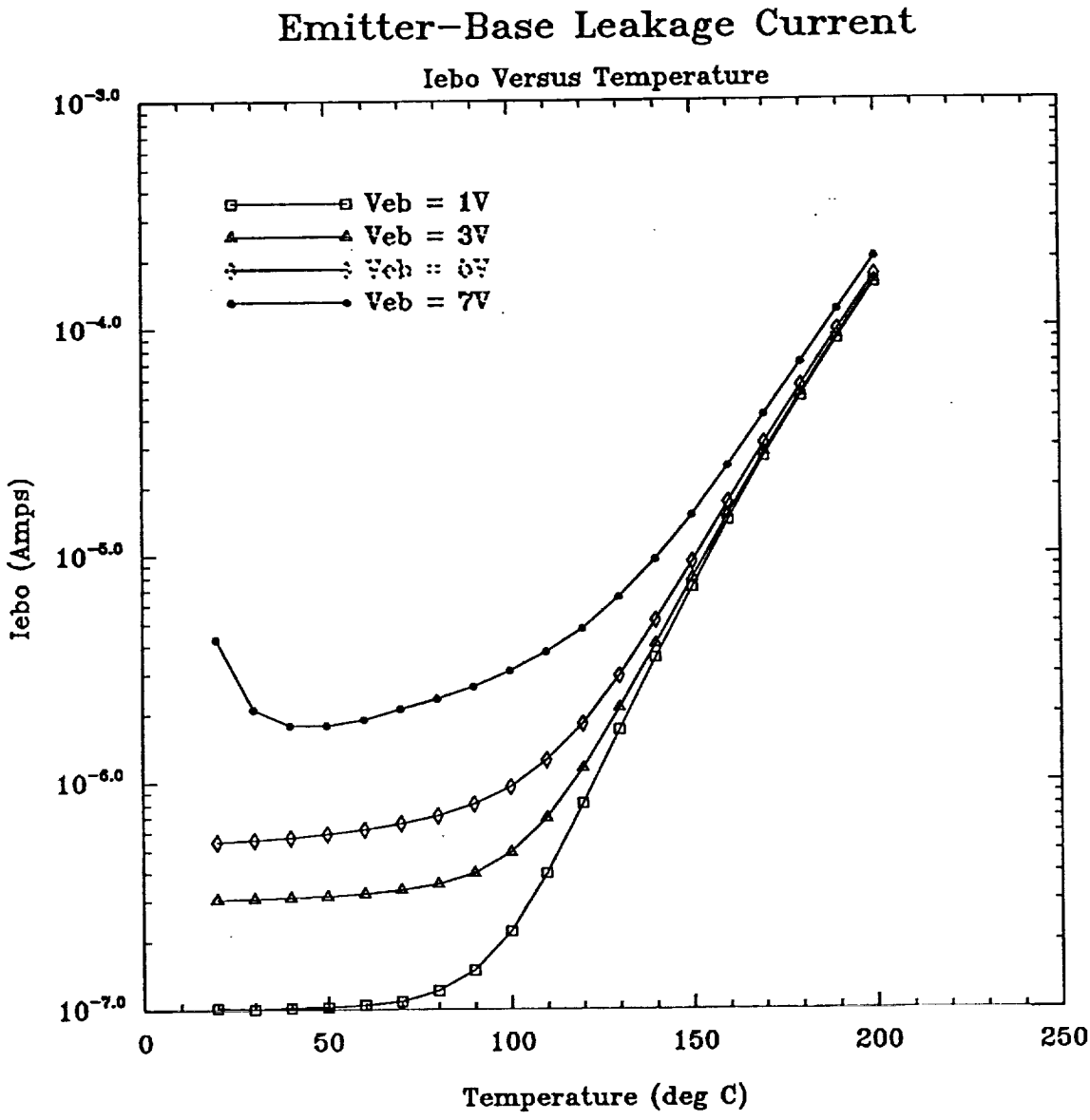
Emitter–Base Leakage Current
Iebo Versus Temperature
Veb = 1V
Veb = 3V
Veb = 5V
Veb = 7V
Iebo (Amps)
10^-3.0
10^-4.0
10^-5.0
10^-6.0
10^-7.0
0
50
100
150
200
250
Temperature (deg C)

Figure 4.

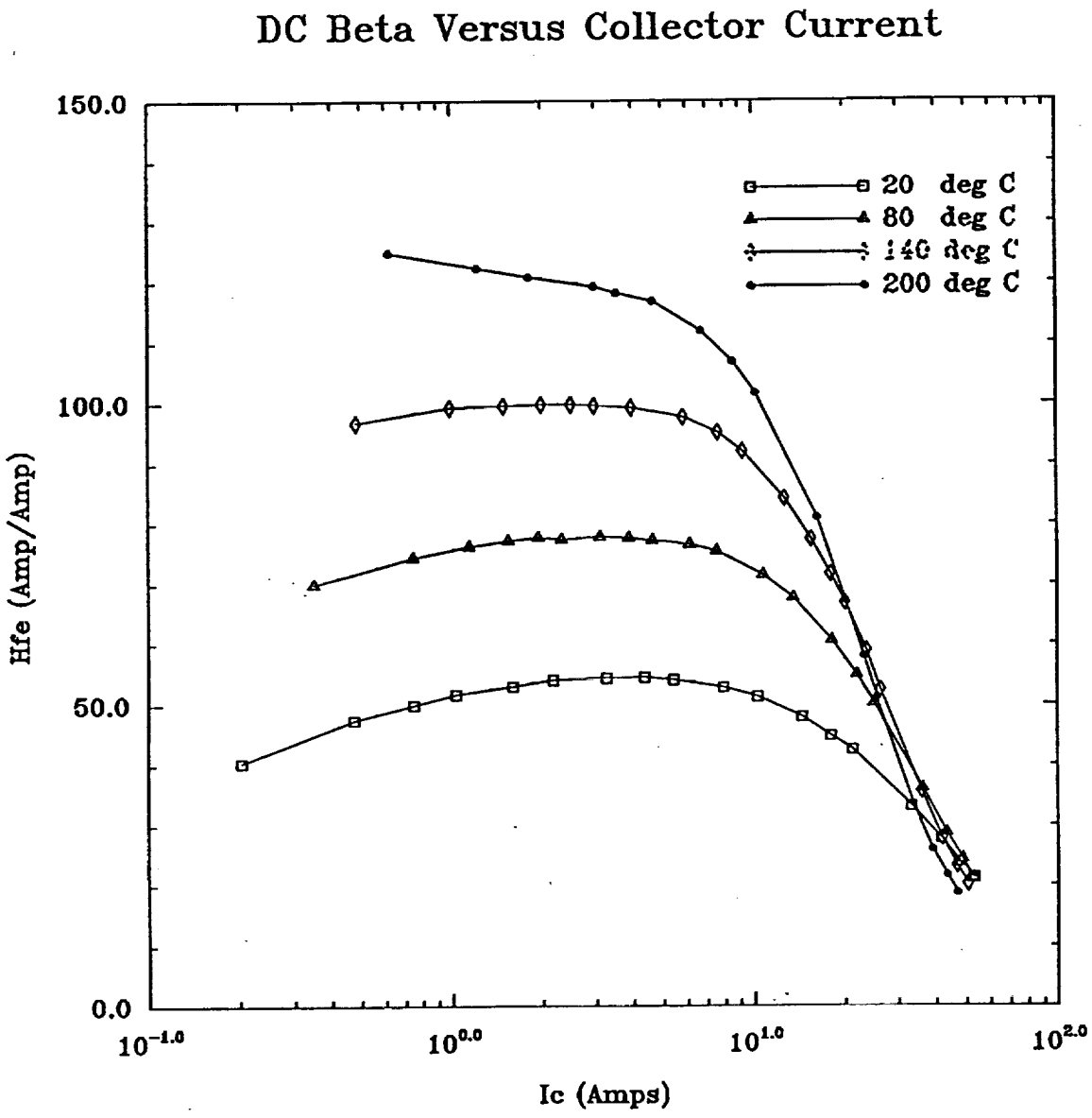
DC Beta Versus Collector Current
150.0
100.0
50.0
0.0
Hfe (Amp/Amp)
20 deg C
80 deg C
140 deg C
200 deg C
$10^{-1.0}$
$10^{0.0}$
$10^{1.0}$
$10^{2.0}$
Ic (Amps)

Figure 5.

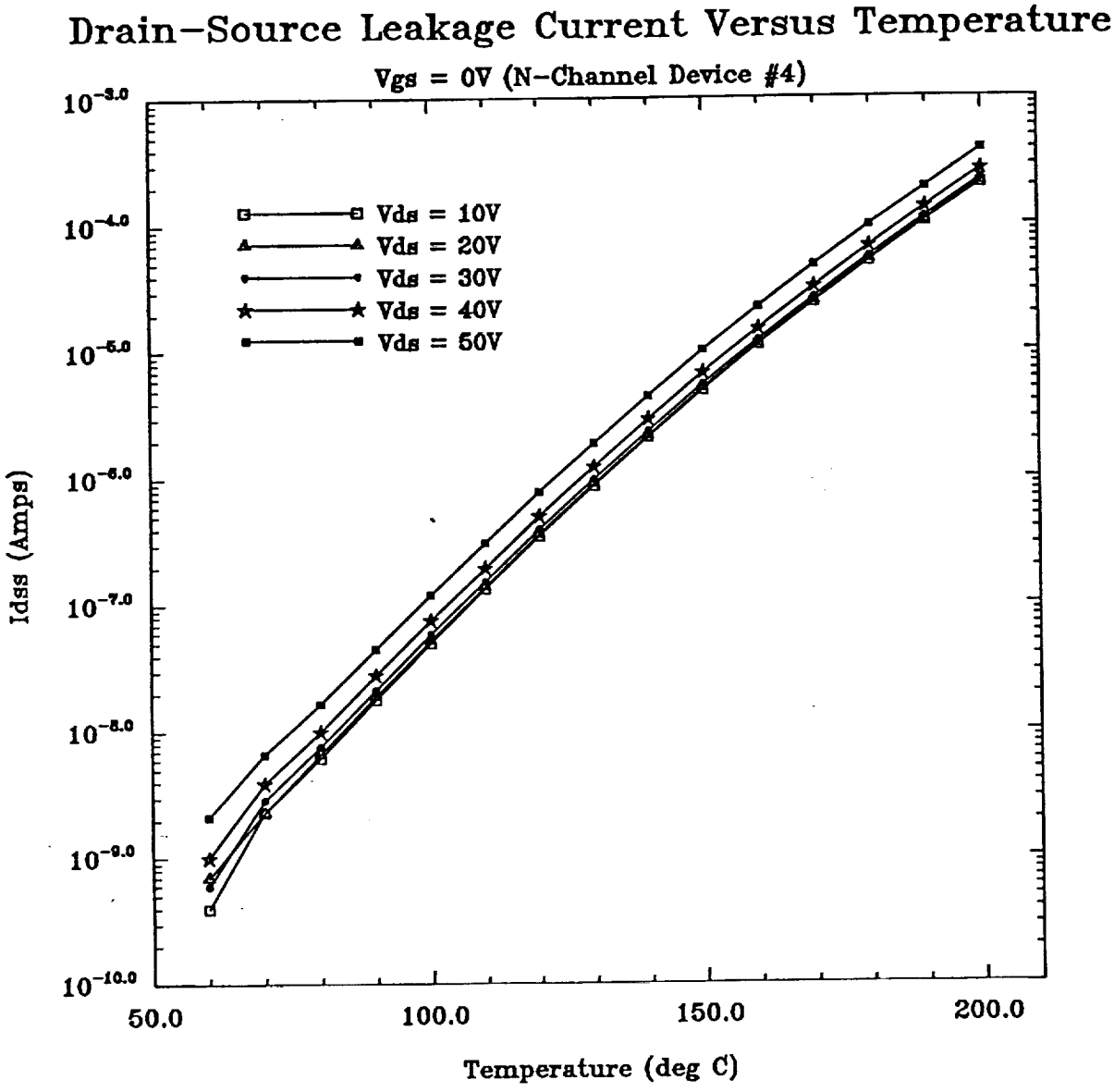
Drain–Source Leakage Current Versus Temperature
Vgs = 0V (N-Channel Device #4)
Vds = 10V
Vds = 20V
Vds = 30V
Vds = 40V
Vds = 50V
Idss (Amps)
10^-3.0
10^-4.0
10^-5.0
10^-6.0
10^-7.0
10^-8.0
10^-9.0
10^-10.0
50.0
100.0
150.0
200.0
Temperature (deg C)

Figure 6.

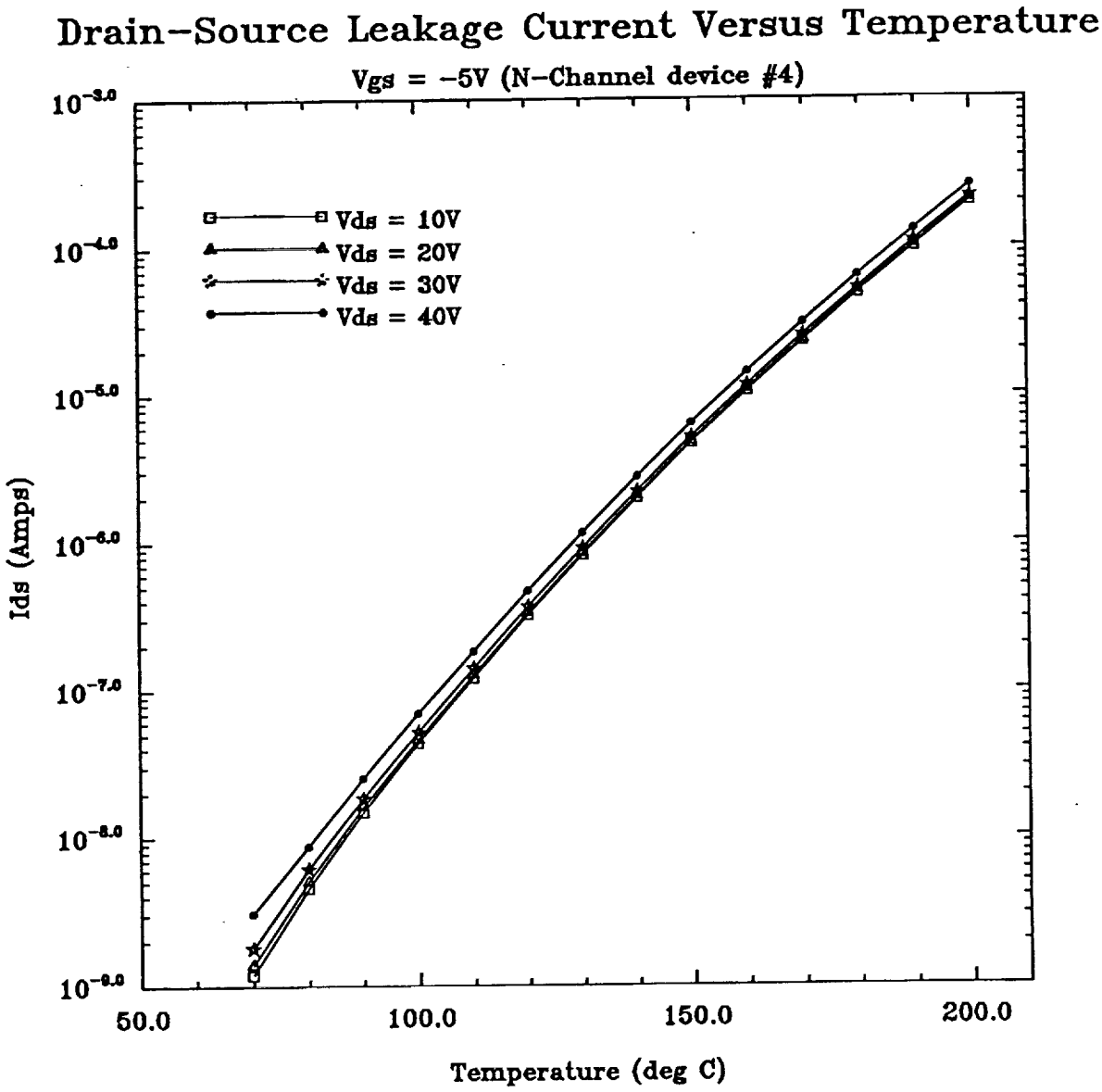
Drain-Source Leakage Current Versus Temperature
Vgs = -5V (N-Channel device #4)
Vds = 10V
Vds = 20V
Vds = 30V
Vds = 40V
Ids (Amps)
Temperature (deg C)
50.0
100.0
150.0
200.0

Figure 7.

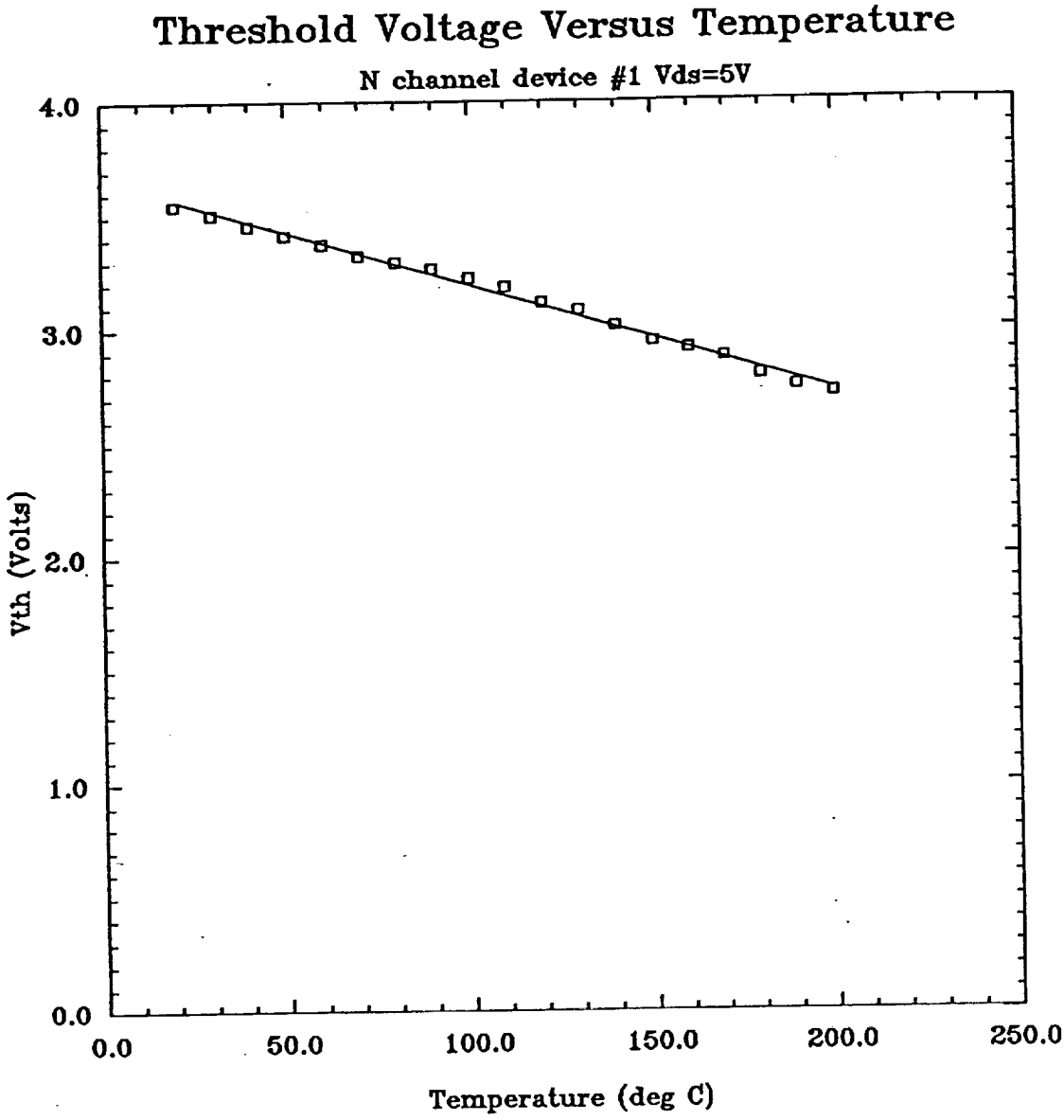
Threshold Voltage Versus Temperature
N channel device #1 Vds=5V
4.0
3.0
2.0
1.0
0.0
Vth (Volts)
0.0
50.0
100.0
150.0
200.0
250.0
Temperature (deg C)

Figure 8.

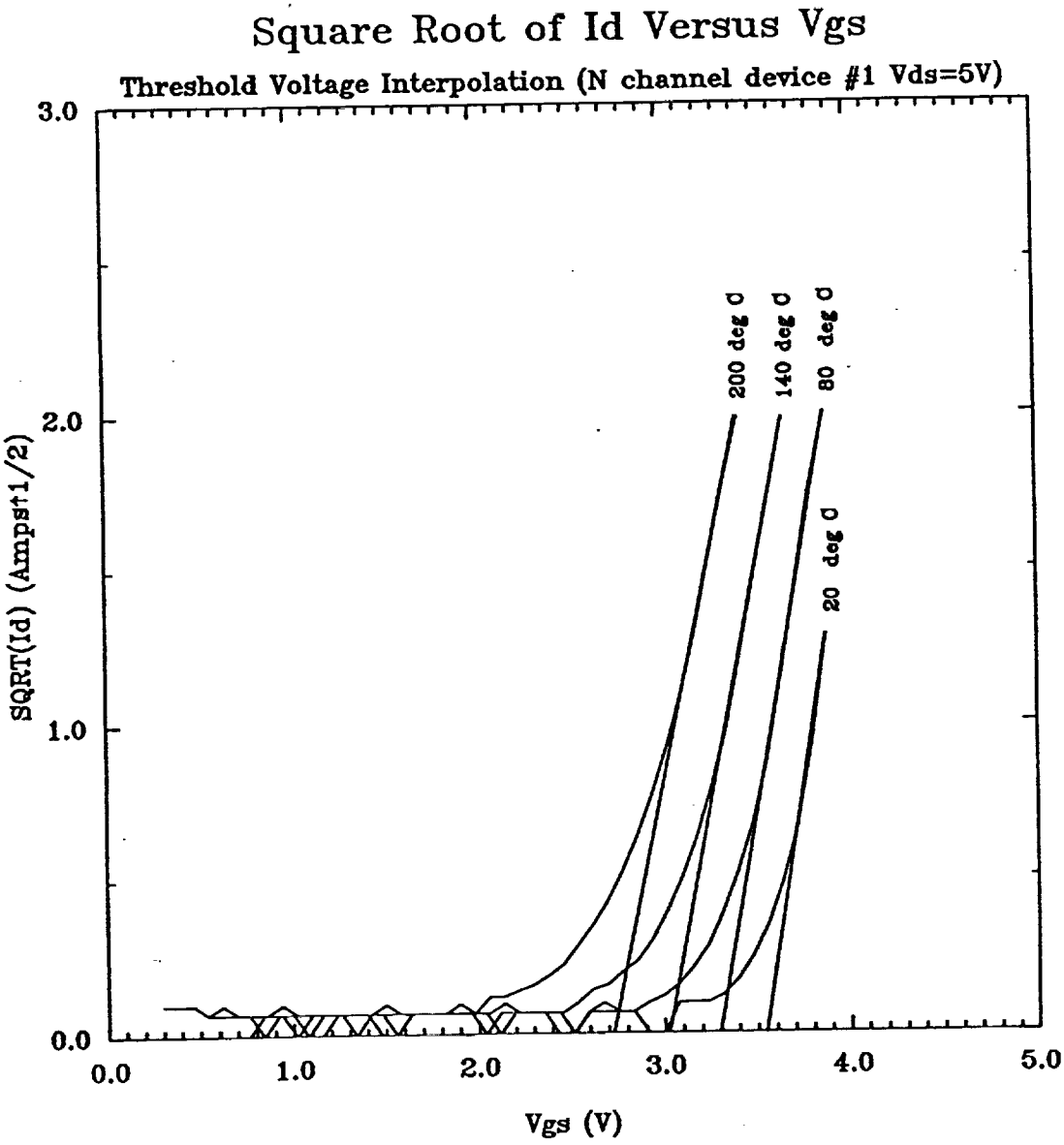
Square Root of Id Versus Vgs
Threshold Voltage Interpolation (N channel device #1 Vds=5V)
SQRT(Id) (Amps^1/2)
Vgs (V)
200 deg C
140 deg C
80 deg C
20 deg C
3.0
2.0
1.0
0.0
0.0
1.0
2.0
3.0
4.0
5.0

Figure 9.

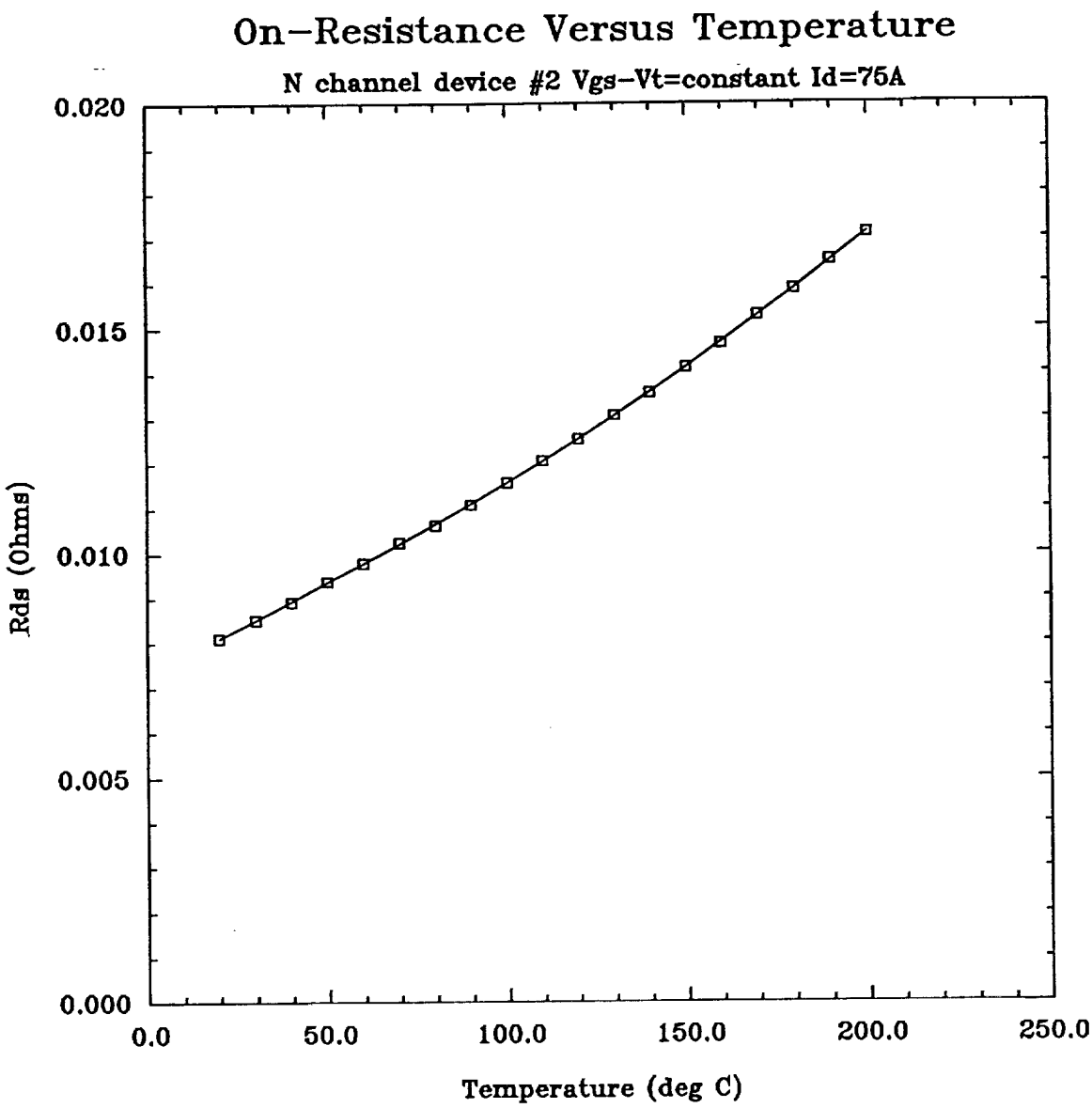
On-Resistance Versus Temperature
N channel device #2 Vgs-Vt=constant Id=75A
0.020
0.015
0.010
0.005
0.000
Rds (Ohms)
0.0
50.0
100.0
150.0
200.0
250.0
Temperature (deg C)

Figure 10.