N91-19019

1990

NASA/ASEE SUMMER FACULTY FELLOWSHIP PROGRAM

MARSHALL SPACE FLIGHT CENTER
THE UNIVERSITY OF ALABAMA

IMPLEMENTATION STRATEGIES for LOAD CENTER AUTOMATION on the SPACE STATION MODULE/POWER MANAGEMENT AND DISTRIBUTION TESTBED

Prepared By:	Karan Watson
Academic Rank:	Associate Professor
University and Department:	Texas A&M University Electrical Engineering
NASA/MSFC:	
Laboratory:	Information and Electronic Systems
Division:	Electrical
Branch:	Electrical Power
MSFC Colleague:	Louis Lollar
Contract No:	NGT-01-002-099 The University of Alabama

THE LOAD CENTER AUTOMATIOM ON THE SSM/PMAD

The Space Station Module/Power Management and Distribution, SSM/PMAD, testbed has been developed at the NASA-Marshall Space Flight Center in order to study the tertiary power management on modules in large spacecraft. This testbed has been developed to be flexible (as an example of this it was changed from a 20Khz to a DC system in 1989). The goal has been to study automation techniques, not necessarily develop flight ready systems. Because of the confidence gained in many of the automation strategies investigated, it is appropriate at this time to study, in more detail, implementation strategies in order to find better trade-offs for nearer to flight ready systems. These trade-offs particularly concern the weight, volume, power consumption and performance of the automation system. With this in mind the Load Center automation systems were studied. These systems, in their present implementation are described in sections I-IV. In section V a recommendation for a new implementation strategy is made.

I. THE RPC

The purpose of the Power Controller, RPC, is to provide the actual switch which will control power to a load. The current switching activity is accomplished by FET's. The Generic Controller, GC commands the switch on or off. In addition to the GC commanding the switch on or off, there is surge current conditioning and detection which can independently trip the switch off in the event of a large overcurrent. In this circuitry an inductor has been sized to control the slope (V/L) of the surge current. If a significant surge current occurs the gate control circuitry for the FETs switches these FETs from the on mode to the linear mode. In this mode the FETs absorb the excess power generated by the faulty current and limit the current. Also during this time a capacitor begins charging, and if the current does not drop within rated values then the charged capacitor will cause the gate control circuitry to turn the FETs off. This sequence is referred to as the FAST trip.

The RPC can provide five sensor signals to the GC. One signal **SWITCH 2**, indicates if the FETs are conducting or not. The magnitude of the current, **I1**. The signal **VDC+**, is a digital bit which is low if the line voltage is $\leq$ 60Vdc and is high if the line voltage is $\geq$ 60Vdc. A thermal resistor, **LM335**, is used to detect temperature readings on the RPC. Signal leads for a second current detection, **I2**, are on the board, but there is no sensor for this signal at this time (this should be the sensor for ground fault detection).

II. THE GC

The purpose of the Generic Controller, GC, is to accept sensor readings from the Remote Power Controller, RPC, and commands from the Switchgear Interface Card, SIC, in order to generate appropriate signals to the switch located on the RPC. The GC will pass status information and current, I, data to the SIC, when enabled to do so. The GCs are in the same card cage as the SICs for a given load center. Communication between these cards is accomplished over a wire-wrapped back-plane bus (Specialized- non-commercial nor standard bus).

The heart of the GC logic is programmed in the Altera 1800J chip. The main functions contained in this logic are: The Trip logic, the data sending logic, and the state machine. There are a few logic functions off chip: an A/D converter to generate **ADDATA** (which is **I1** in 8 bit digitized data in serial form); a timer; and powerup logic to assure we start in the correct state.

The state machine is a bit, six state encoder. The purpose of the state machine is to remember which state (On, Off, or Tripped) we are in, and move us from state to state as the inputs deem appropriate. Outputs to the RPC are determined by the state.

In the trip logic the digital signals from analog comparators for **SRGEI**, **I2TRIP**, **GNDTRP**, **UNDVLT**, **TMPTRP** are latched until a **RESET** command is given. The signal for a **FAST** trip is generated if we are in the on state and the RPC says the switch goes off. Any of these indicators can cause the **TRIP** signal to latch which will send us to the tripped state, if we were in the on state, and turns the switch off.

There is a 4 bit binary counter in the logic which synchronized with the SIC clock to generate the serial DATA response to the SIC inquiries and commands.

III. THE SIC

The purpose of the Switchgear Interface Card, SIC, is to control the communication flow between the Lowest Level Processor, LLP, and up to 14 Generic Controllers, GCs, as well as one A/D card as via the special, wire wrapped, backplane in the testbed (not a commercial or standard backplane). The interface to the LLP is accomplished via an RS-422 connection.

The hardware on the SIC include hardware for serial reception and transmission of data from the LLP and the GCs. The heart of the SIC is a Motorola 6800 microprocessor, with associated clock generators, reset circuitry, bus drivers, memory, parity generation and checking device, and address decoding circuitry. Thememory consists of 8 KBytes of EPROM for the firmware, and 8 KBytes of RAM. There are Mux's and FETs for selecting and driving control signals to the GCs and A/D card.

The firmware for the SIC is written in 6800 assembly language. Basically the code initializes the system, executes data in the continuous buffer, watches for the trigger for the once buffer, checks the input buffer for incoming commands, and puts data and status responses in the output buffer. Execution proceeds according to the continuous buffer commands or an incoming command.

IV. THE LLP

The purpose of the Lowest Level Processor, LLP, is to provide the Load Centers with an interface between the functions occurring in the Load Center and the higher level computing systems, which will interface with operators and crew members. Thus, the LLP serves as the data gatherer and formatter for the Fault Recovery And Management Expert System, FRAMES, which runs of a Solborn workstation. The link between the LLPs and the FRAMES is accomplished by TCP/IP on an ETHERNET. The current LLP configuration is a 20 MHz 386 microcomputer with 1.2 MByte of RAM, a floppy disk drive, a 422 communication card, and an ETHERNET card. The operating system is DOS 3.3, and the software is coded in TURBO PASCAL.

V. RECOMMENDATIONS FOR NEW IMPLEMENTATION

After this review of the functions and the implementation of the Load Center automation systems the primary recommendation, at this time, is to incorporate the use of commercially available microcontrollers in the automation system. To illustrate the advantage of these devices, several microcontrollers were reviewed (Motorola 68HC11, TI 37010, Intel 87196) and one was chosen to illustrate the advantages of microcontrollers. For this report the Intel 87196 was chosen. This initial choice was based primarily upon the fact that the 87196 has: A CMOS implementation and a power save mode to minimize power consumption, a serial I/O port, timers, 8-channel-10-bit A/D conversion, multiple output ports, on chip EPROM for the program, and is more compatible with the Intel 386 systems already in the LLPs.

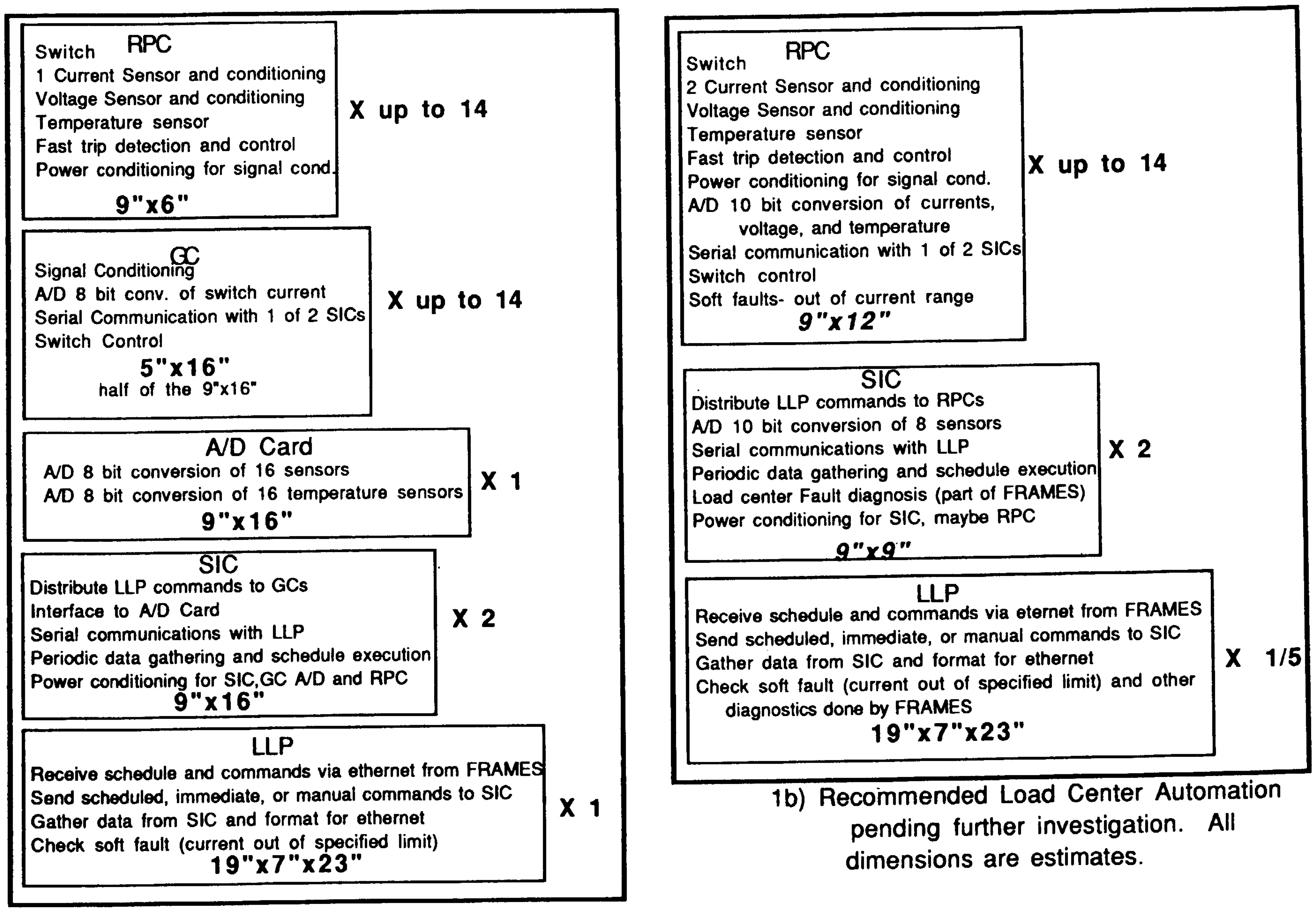
The strategy for new Load Center automation is illustrated in figure 1. This strategy calls for the replacement of the GC card with a 68-pin 87196, reset circuitry, a crystal, and possibly bus drivers. All of this new GC implementation should reside on the RPC card, thus eliminating the GC card. The gains in the new implementation are clear in volume and weight, and should be substantial in power consumption. We also gain in functionality and performance.

In a similar manner, a small board involving an 87196 can be used to replace the SIC and the A/D card. In this strategy we need the 68-pin 87196, the reset circuitry, a crystal, bus drivers to send signals to the GCs, and, if the exact programming strategy as used in the current SIC were used, one RAM chip is needed. In this case we gain some functionality and performance while reducing weight, power consumption and volume. We can relieve the LLP of many of its communication formatting and status checking functions.

The LLP functions should remain in the 386 based computer. This system should now be able to absorb some of the FRAMES processing done in the SOLBORNE. (At a minumum it will provide more refined information to FRAMES.) The possibility of combining present LLP functions into fewer 386 processors is possible. Currently it appears that if no new functions were added to the LLP level then one machine might handle all 5 load centers envisioned in the testbed. However, before this tradeoff was made a careful study of the distribution and faulty tolerance effects should be made.

VI. CONCLUSIONS

The functions and implementations in the Load Center Automation systems (RPC, GC, SIC, LLP) have been reviewed. The general conclusion is: now that automation strategies have been studied, a more integrated implementation is possible, which saves weight, volume, and power consumption, while costing no reduction in functional performance or flexibility. This new strategy should incorportae the use of commercially available microcontrollers, as discussed above. The use of microcontrollers, and other highly integrated automation systems should be actively pursued and demonstrated on the SSM/PMAD testbed.


RPC
Switch
1 Current Sensor and conditioning
Voltage Sensor and conditioning
Temperature sensor
Fast trip detection and control
Power conditioning for signal cond.
9"x6"
X up to 14
GC
Signal Conditioning
A/D 8 bit conv. of switch current
Serial Communication with 1 of 2 SICs
Switch Control
5"x16"
half of the 9"x16"
X up to 14
A/D Card
A/D 8 bit conversion of 16 sensors
A/D 8 bit conversion of 16 temperature sensors
9"x16"
X 1
SIC
Distribute LLP commands to GCs
Interface to A/D Card
Serial communications with LLP
Periodic data gathering and schedule execution
Power conditioning for SIC,GC A/D and RPC
9"x16"
X 2
LLP
Receive schedule and commands via ethernet from FRAMES
Send scheduled, immediate, or manual commands to SIC
Gather data from SIC and format for ethernet
Check soft fault (current out of specified limit)
19"x7"x23"
X 1
RPC
Switch
2 Current Sensor and conditioning
Voltage Sensor and conditioning
Temperature sensor
Fast trip detection and control
Power conditioning for signal cond.
A/D 10 bit conversion of currents, voltage, and temperature
Serial communication with 1 of 2 SICs
Switch control
Soft faults- out of current range
9"x12"
X up to 14
SIC
Distribute LLP commands to RPCs
A/D 10 bit conversion of 8 sensors
Serial communications with LLP
Periodic data gathering and schedule execution
Load center Fault diagnosis (part of FRAMES)
Power conditioning for SIC, maybe RPC
9"x9"
X 2
LLP
Receive schedule and commands via eternet from FRAMES
Send scheduled, immediate, or manual commands to SIC
Gather data from SIC and format for ethernet
Check soft fault (current out of specified limit) and other diagnostics done by FRAMES
19"x7"x23"
X 1/5

1a) Present Load Center Automation

1b) Recommended Load Center Automation pending further investigation. All dimensions are estimates.

Figure 1 Present versus Recommended Load Center Automation Implementation