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AUGMENTATION OF THE SPACE STATION MODULE POWER MANAGEMENT AND DISTRIBUTION BREADBOARD

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ABSTRACT

The Space Station Module Power Management and Distribution (SSM/PMAD) Breadboard, located at NASA's Marshall Space Flight Center (MSFC) in Huntsville, Alabama, models power distribution and management, including scheduling, load prioritization, and FDIR, within a Space Station Freedom Habitation or Laboratory module. This 120 VDC system is capable of distributing up to 30 kW of power among more than 25 loads.

In addition to the power distribution hardware, the system includes computer control through a hierarchy of processes. The lowest level consists of fast, simple (from a computing standpoint) switchgear, capable of quickly safing the system. At the next level are local load center processors, called Lowest Level Processors (LLP's), which execute load scheduling, perform redundant switching, and shed loads which use more than scheduled power. Above the LLP's are three cooperating Artificial Intelligence (AI) Systems which manage load prioritizations, load scheduling, load shedding, and fault recovery and management. Recent upgrades to hardware and modifications to software at both the LLP (now based on 80386's) and AI System levels promise a drastic increase in speed, a significant increase in functionality and reliability, and potential for further examination of advanced automation techniques.

BACKGROUND

As the electrical power requirements for spacecraft have increased, the problems of managing these large power systems have also increased. America's first space station, Skylab, employed an eight kW power bus which required fifteen to twenty ground support personnel to monitor and control. Extensive crew involvement was also required at times to correct system faults. After the final crew left and Skylab was powered down, the EPS was evaluated . In the conclusion of this evaluation, ten recommendations for future spacecraft electrical power systems were presented. Seven of the ten recommendations can be implemented by the use of automation techniques. Based on these results and experience from other spacecraft EPSs, NASA/MSFC began to investigate automating a spacecraft EPS .

The first steps taken toward an automated EPS began in 1978 with the start of the The Autonomously Managed Power System (AMPS) program. The AMPS program was funded by NASA's Office of Aeronautics and Space Technology (OAST) and managed by MSFC through a contract with TRW. The AMPS program was a three phase program. The first phase identified a reference photovoltaic electrical power system for a 250 kW class low earth orbit (LEO) satellite. The second phase developed the autonomous power management approach for the reference EPS. The third phase developed a breadboard test facility to evaluate, characterize, and verify the concepts and hardware resulting from phases 1 and 2.

Based on the results of AMPS, a project to investigate automation techniques appropriate to a large PMAD system such as will exist on Space Station Freedom modules was begun in 1984 at MSFC. With the support of Martin Marietta Space Systems Group, the SSM/PMAD test bed was developed . Originally delivered as a 20kHz, 208V ring bus system, the SSM/PMAD power system has evolved with Space Station Freedom into its current 120VDC Star Topology. Development of the automation software

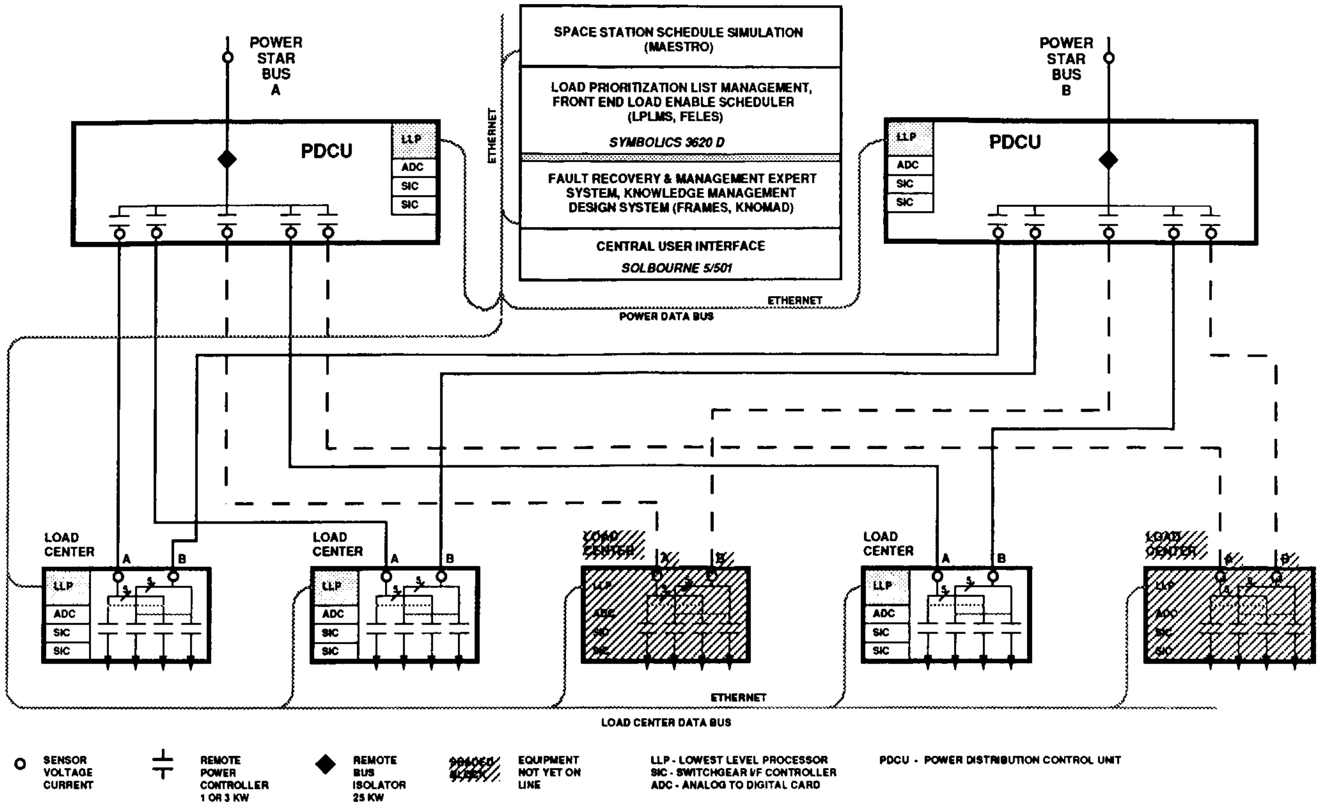

Figure 1 -- SSM/PMAD Breadboard Topology

continues, but the system has already demonstrated fully autonomous operation, including scheduling, implementation of the schedule, and the ability to handle and diagnose several kinds of faults.

SSM/PMAD

The Space Station Module/Power Management and Distribution breadboard power system (Figure 1) is a two bus system, each consisting of a 120 Vdc power supply, one 15 kW Remote Bus Interrupter (RBI), five 3kW Remote Power Controllers (RPCs), and several 1 kW RPCs at the load center level. Each power bus is configured in a star bus arrangement with each RPC equipped with sensors that detect undervoltage, surge current, ground fault, high temperature, and I^2t conditions. If any of these conditions arise, the RPC will trip and then store the trip condition in its memory. Each RPC also provides switch status and data from a built-in current sensor. The system load banks are resistive and switchable in two 250 W increments, and one 500 W step to provide up to 1 kW of load to each RPC.

The system software is distributed through several types of processors. Processing at the level nearest the power hardware is performed by the Lowest Level Processors (LLPs). The LLPs are rack mounted 80386-based IBM/PC compatible computers with boards for Ethernet Local Area Network communications. Each LLP is responsible for controlling its associated switches and for monitoring all sensor readings and switch status in its center. The LLP also notifies the next higher machine, a Solbourne (Sun compatible) workstation, of any anomalies noted. Each LLP communicates down to one or two Switch Interface Cards (SICs), which communicate with the RPCs and the Analog to Digital Converter (A/D) Cards for sensor packets.

The Solbourne workstation contains the heart of the system software. The workstation houses the Fault Recovery and Management Expert System (FRAMES) and serves as the user interface for the breadboard in both manual and autonomous mode.

FRAMES monitors the system for anomalies. It receives the schedule from Maestro at the same time it is being sent down to the LLPs. Each LLP sends notification of any anomalies it sees, such as tripped switches or shed loads. Sensor reading messages are also sent to FRAMES. FRAMES uses the information which comes to it and attempts to find an explanation. If this explanation requires removing some pieces of equipment from service, FRAMES does so and notifies Maestro to adjust the schedule accordingly. FRAMES explains to the user the reasoning it followed, and shows on its system diagram screen the results of the fault or anomaly.

Maestro is a resource scheduler which can create a schedule based on multiple constraints. In the SSM/PMAD Breadboard the constraints currently used include number of crew members required, equipment resources, and power resources, with power being the resource of most concern in this breadboard. Power is allocated not just by the amount available to the system, but also by the ability of intervening components to supply the power. Maestro is housed on a Symbolics 3620D AI workstation.

The third system, the LPLMS, uses information from the event list and the active library, along with its own rules, to dynamically assign relative priority to each active load in the system. A new list is sent down to the LLP's at least every 15 minutes (less if a contingency occurs). The load priority list can be used to shed loads in case of a reduction in power.

INTERFACE TO LERC TEST BED

In an effort to share technology and demonstrate the effectiveness of advanced automation techniques, a joint project with Lewis Research Center (LeRC) has been initiated. An interactive link will be forged between the LeRC power system automation test bed and the SSM/PMAD system. A simple scenario to demonstrate basic functionality between the two is scheduled for the end of July 1990, with a demonstration due by the end of November. A more robust demonstration will be planned using the knowledge gained from these initial tests for the July 1991 time frame.

As currently envisioned, this project will consist of a link, via Ethernet, between the two breadboards. The link will operated at two levels: the power system level and the control level. At the power system level, the SSM/PMAD system will appear as a load to the LeRC test bed, and the LeRC system as a source to SSM/PMAD. This will be accomplished by letting the LeRC control one (and, ultimately, both) of the power supplies of the SSM/PMAD system, while the SSM/PMAD system will control the characteristics of a programmable load attached to the LeRC system. At the control level, information will go back and forth between the two systems negotiating power requirements versus available resources for the scheduling systems, and notification of any faults or contingencies for the FDIR functionality.

The initial demonstration will show only the control link, using simple negotiation algorithms. Functionality will be added as the interconnection becomes more robust.

LASEPS

The AMPS high power DC breadboard was mentioned in the introduction as a precursor to SSM/PMAD. AMPS still exists, and shares the lab with SSM/PMAD. The Large Autonomous Spacecraft Electrical Power System (LASEPS) is an in-house effort to combine the strengths of both systems, resulting in a single source to load power breadboard. AMPS' contribution will be to replace the existing 120 Vdc power supplies with its two power channels, thus giving the system a solar array/battery network power source more representative of an actual flight power system. Each power channel will have its own Solar Array Simulator and 108 cell, 189 Ampere hour Ni-Cd battery supplying a 145 +\- 15 Vdc bus.

A Programmable Power Processor (P^3) will be used on each bus as an interface between AMPS and SSM/PMAD. These P^3's, developed in the late 1970's for a 25 kW power module, are microprocessor controlled voltage regulators with an input voltage range up to 400 Vdc, and an output range from 24 to 180 Vdc at a maximum of 100 A. These specifications qualify the P^3's as a convenient and efficient interface between the two breadboards.

This complete, complex, high-power breadboard will enable the MSFC team to further investigate techniques and criteria required for any large space power system such as will be required for the Lunar/Mars initiative, large platforms envisioned for Mission to Planet Earth, or other new agency goals, all without compromising the function of the SSM/PMAD system which is a part of it.

FUTURE PLANS

As SSM/PMAD matures, more and more effort will go into making sure the technology being developed is used. This includes identifying the necessary impacts to the design, development, and operation of Space Station Freedom for implementation of the technology at both Permanent Manned Compatible (PMC) and Assembly Complete (AC) stages. Work continues with Boeing to support WP01 SSF tasks, encouraging use of the breadboard where possible. Demonstrations of the breadboard's capabilities will be as broad-based as possible, including personnel from the other NASA centers, their prime contractors, and Headquarters.

Efforts will also continue to make the technology more amenable to actual flight use. Code will be converted to Ada, starting at the lowest levels and moving up. Functionality will continue to be moved to as low a level as possible to take advantage of the power of distributed computing. A study into the possibility of using microcontrollers to perform some or all of the LLP and lower functionality is now underway. The demonstrations with LeRC will help to point out weaknesses of both systems as part of a larger system. LASEPS will be of similar value. Development of the user interface will help in showing the true power of the system, and will actually increase that power by making it more accessible.

The system is already capable of autonomous operation. An important basic addition to the breadboard will be intermediate modes of autonomy, enabling a user to take "semi-manual" control -- that is, being able to modify the system without having to take full manual control. This will result in a much safer, more robust system than is possible with only fully autonomous or fully manual operation.

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