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PHASE-LOCK-LOOP APPLICATION FOR FIBER OPTIC RECEIVER

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By

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INTRODUCTION

A phase-locked loop is a closed-loop feedback circuit in which a generated signal establishes a synchronization or "lock" with an input signal. Phase-locked loop (PLL) circuits are frequently used in applications such as FM detection, frequency multiplication and division, tracking, establishing a noise-free reference in the presence of noise. In particular, digital phase-locked loop circuits can be utilized with optical communication applications. The phase-locked loop is used for extraction of data clock synchronization and for data detection in high-speed fiber optic systems. This is an initial effort to become familiar with the design and fabrication of a phase-lock loop at moderate frequencies (1 to 50 MHz). The intent of this report is to document the design and implementation of a lower frequency phase-lock loop (PLL), which can be used to extract a clock signal from a data signal. The knowledge and experience gained will be beneficial for the future design of a PLL operating at gigabit data rates for a fiber optic application.

At the system level from Figure 1, one can see the overall vehicle for transmitting coded data via fiber optic cables at very high data rates. In an optical transceiver system, the digital phase-lock loop is connected to the output of the receiver to extract a clock from the received coded data. The clock signal is then used to reconstruct or recover the original data from the coded data. Figure 2 illustrates how the PLL is used to extract the clock (frequency of the VCO) from the received coded data. This report describes a theoretical approach in the design of a digital PLL operating at 1 MHz and 50 MHz. Hardware implementation of a breadboard design (1 MHz) and a printed-circuit board (50 MHz) were assembled using Emitter Coupled Logic (ECL) to verify experimentally the theoretical design. In the future this analysis will be applied in the design of a very high-speed optical system.

THEORY

A block diagram of the basic phase-lock loop is shown below in Figure 3.

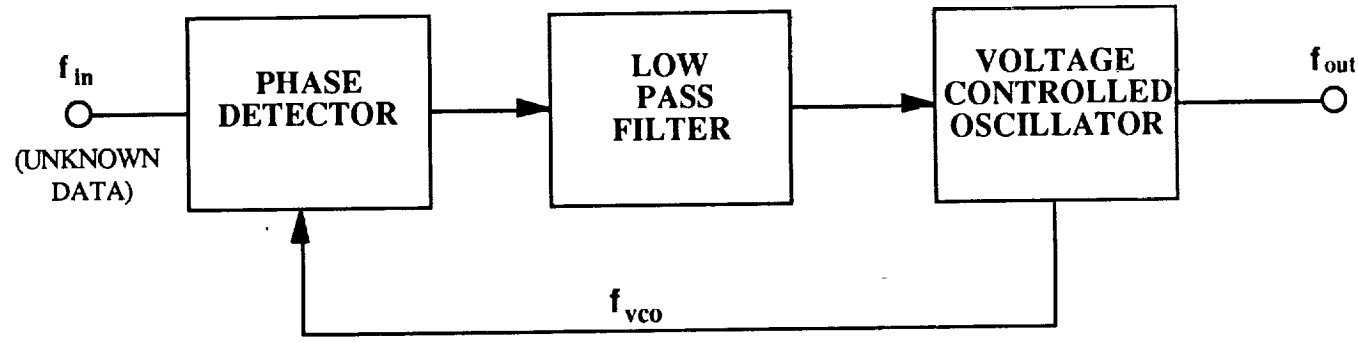
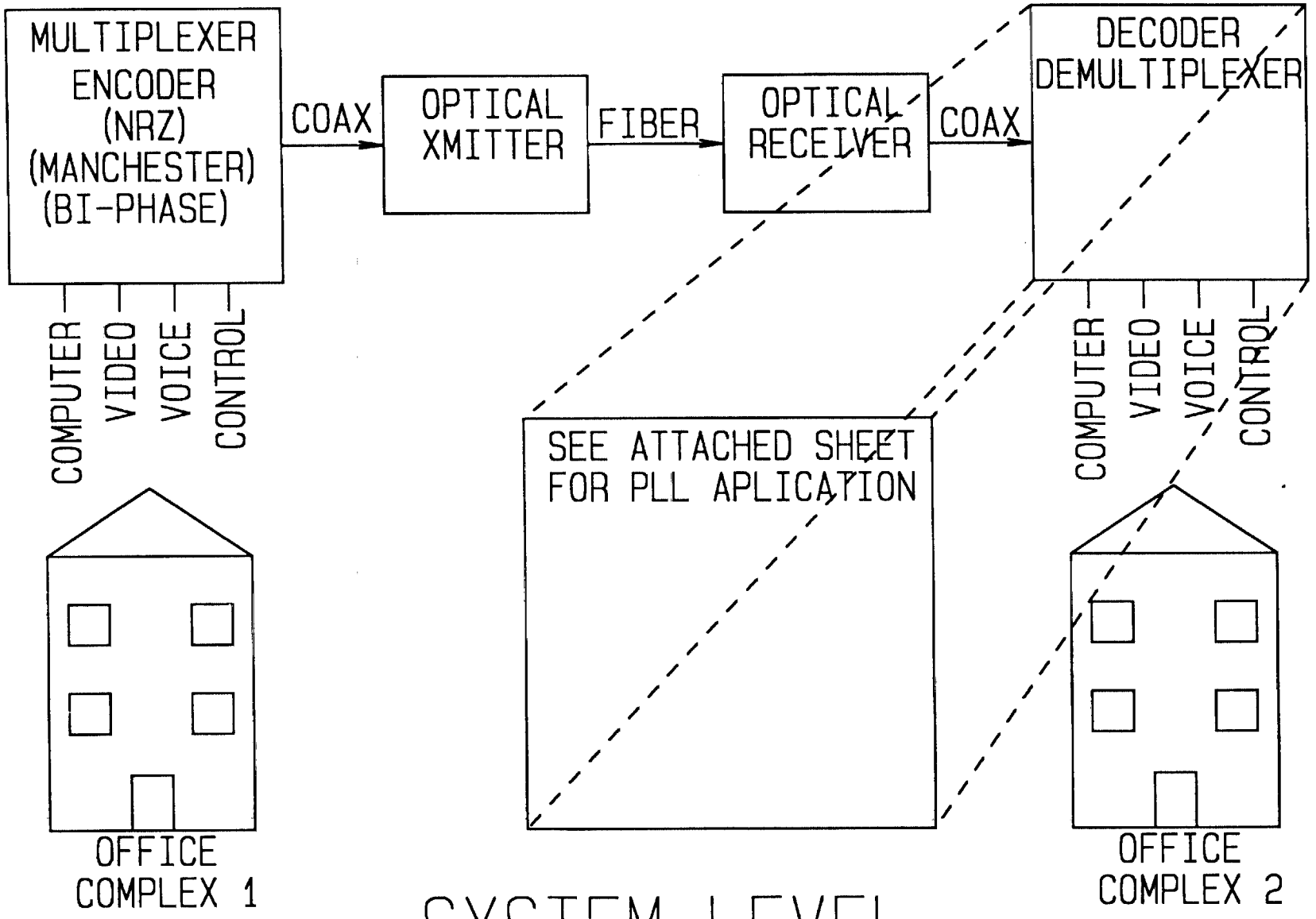


Figure 3. Block Diagram of a Phase-Lock Loop.



SYSTEM LEVEL

Figure 1. SYSTEM LEVEL BLOCK DIAGRAM

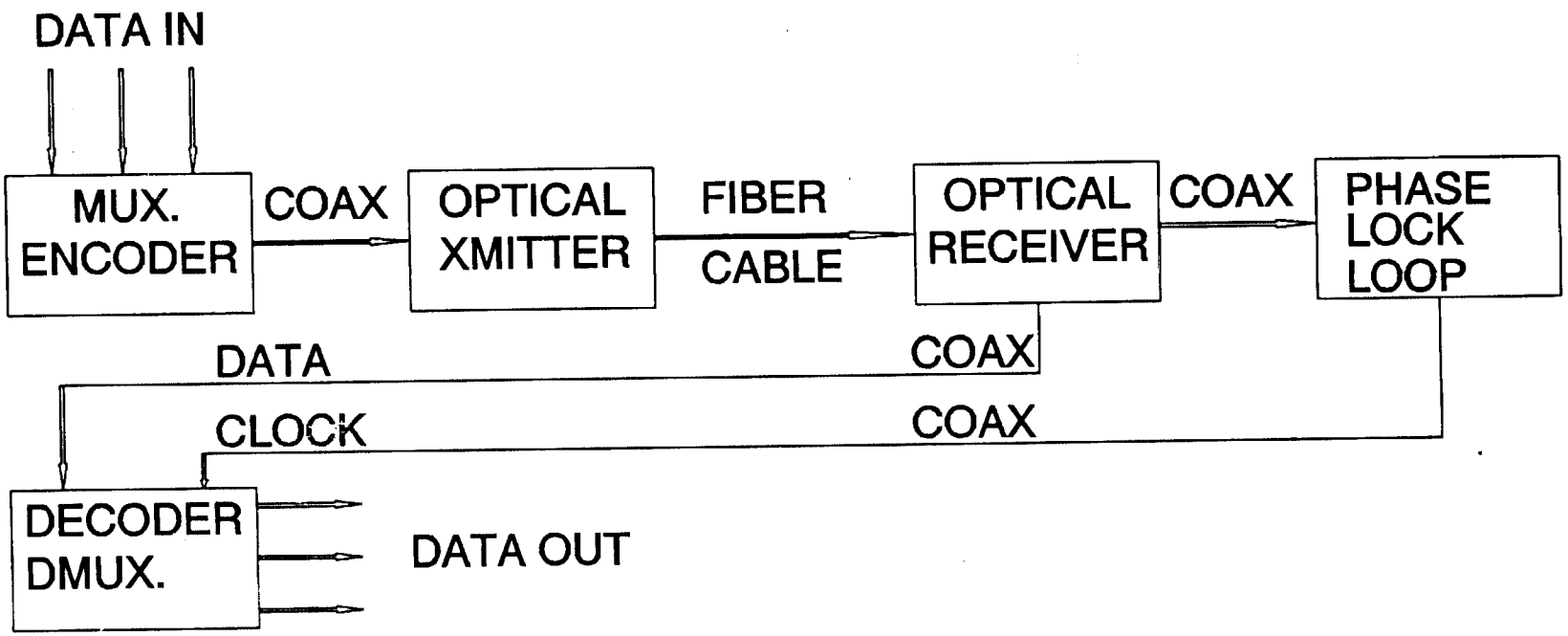


FIGURE 2. SYSTEM COMPONENT LEVEL

The phase detector, low pass filter and the voltage controlled oscillator are in the forward path of the loop. The connection between the VCO and the phase detector is the feedback path.

The VCO is a free-running oscillator. Its frequency is determined by an external resistor-capacitor network or by an inductor-capacitor network. The frequency of the voltage controlled oscillator (fvco) is fed back to the phase detector and is compared to the input frequency containing the unknown coded data. The output of the phase detector produces an error voltage, which is an average dc voltage that is directly proportional to the phase difference between the input to the PLL and the VCO output. This error voltage is then filtered by the low pass filter, thus removing traces of higher frequency noise and the error voltage is then fed to the VCO to complete the loop. This error voltage forces the frequency of the VCO to change in a direction that reduces the frequency difference between the input and the VCO. Once the VCO starts changing in frequency, in order to track the input, the loop is in the capture state. This continues until the VCO and input frequencies are equal in magnitude. At this point the loop is phase locked, or synchronized.

During phase lock there exists a finite phase difference between the VCO and the input. This phase difference is necessary to generate the error voltage which shifts the VCO frequency and keeps the loop in phase lock. The low pass filter dictates the dynamic characteristics of the phase-lock loop. If the input and VCO frequencies are significantly large, the resultant signal may be too high to be passed by the filter. Thus, the signal is out of the capture range of the loop. When the loop is phase locked, the filter is the only limitation on the speed of the loop's ability to track changes in the input frequency.

DESIGN CONSIDERATIONS

Because circuit speed will be extremely important for the design of the phase-lock loop, Motorola's Emitter Coupled Logic (MECL) is an obvious design choice. MECL offers one of the highest speeds of any Integrated Circuit (IC) logic available. Other advantages of MECL are low cost, low noise and low crosstalk between signal leads. The design is basically divided into three areas consisting of a phase detector, a low pass filter, and a voltage controlled oscillator. Each of these areas will be dealt with on an individual basis.

DESIGN CONSIDERATIONS FOR THE PHASE DETECTOR

As stated before, phase-locked loop systems use a phase detector which produces an error voltage that is directly proportional to the phase difference between the input and the VCO output. This may be described by the relation

$$Vo = K\phi\Delta\phi \qquad \text{(Ref. 1, pg. 151)}$$

where Vo is the average output voltage of the phase detector in volts, $K\phi$ is the phase detector conversion gain in volts/radian, and $\Delta\phi$ is the input phase difference in radians.

The objective of a phase-lock loop system is to produce a frequency out of the VCO (fvco) that is equal to the input frequency, while maintaining a finite (small) phase difference which produces a large enough error voltage to drive the VCO. The VCO may be thought of as a voltage-to-frequency converter. If the above is true in this case, then the frequency of the extracted clock has locked on to the input frequency (unknown coded data).

One major design consideration for the phase detector is to make certain the phase detector is fast enough to process the information, such that the system time constant does not depend on the speed of the phase detector. Our choice for the phase detector is the MC12040. The MC12040 is a logic network designed to be used as a phase comparator for MECL-compatible input signals. The MC12040 determines the "lead" or "lag" phase relationship and the time difference between the leading edges of two waveforms (fin and fvco). The error voltage generated from the MC12040 is shown in Figure 4. The leading edge of the fin (unknown data) triggers the rising

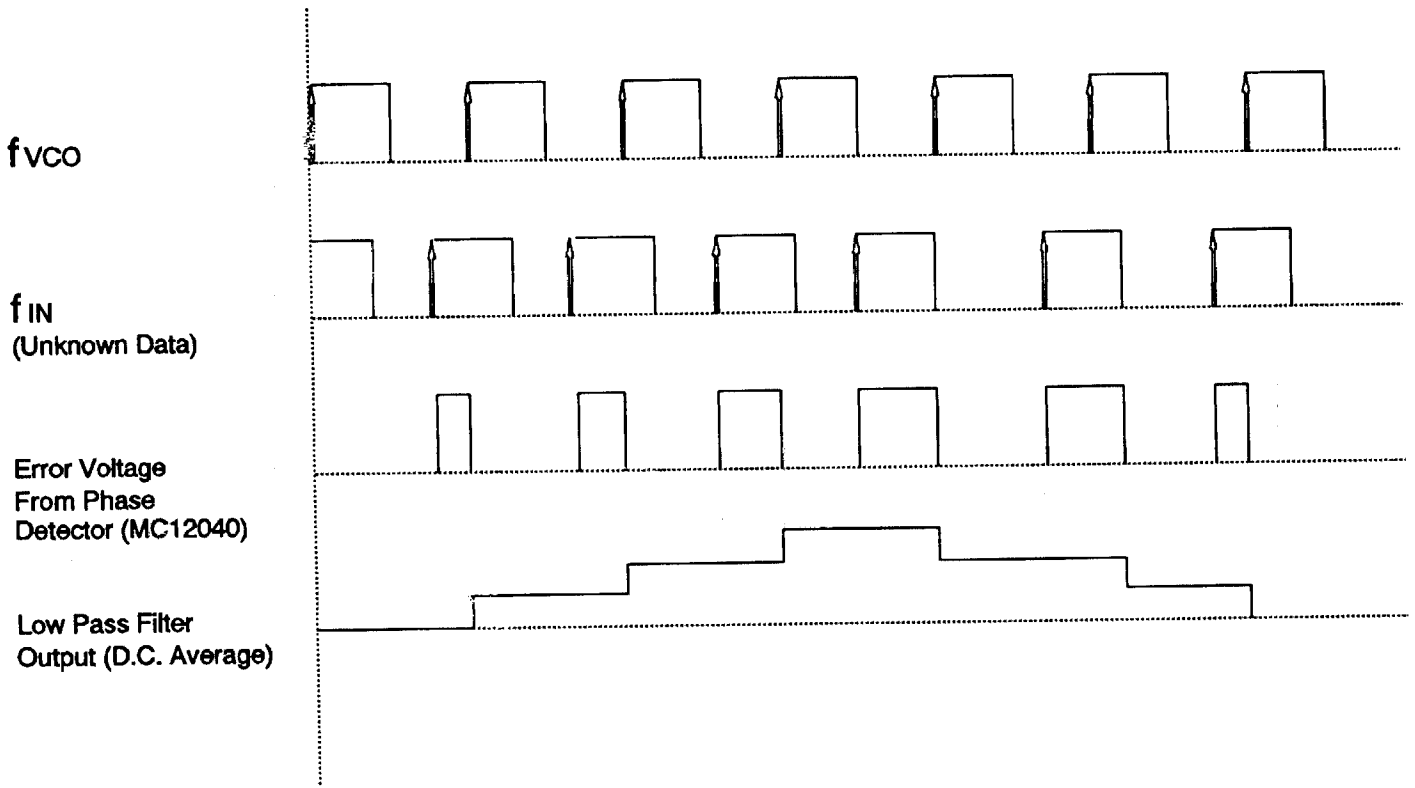


FIGURE 4. TIMING DIAGRAM OF PHASE DETECTOR OUTPUT ERROR VOLTAGE

edge of the error voltage pulse while the leading edge of the fvco triggers the falling edge of the error voltage pulse.

Figure 4 illustrates how the error voltage is produced. One should note that as the error voltage increases, fvco increases in an effort to lock onto the fin (unknown data). Likewise, if the error voltage decreases, fvco decreases.

DESIGN CONSIDERATIONS FOR THE LOOP FILTER

The loop filter is shown below in Figure 5 where, $V_f = Vo\ F(s)$.

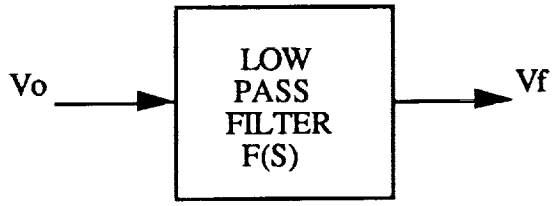


Figure 5. Block Diagram for the Low Pass Filter.

The output voltage of the filter appears at the input of the VCO, thus controlling the output frequency of the VCO. The loop filter in Figure 6 is the type of filter chosen in this design.

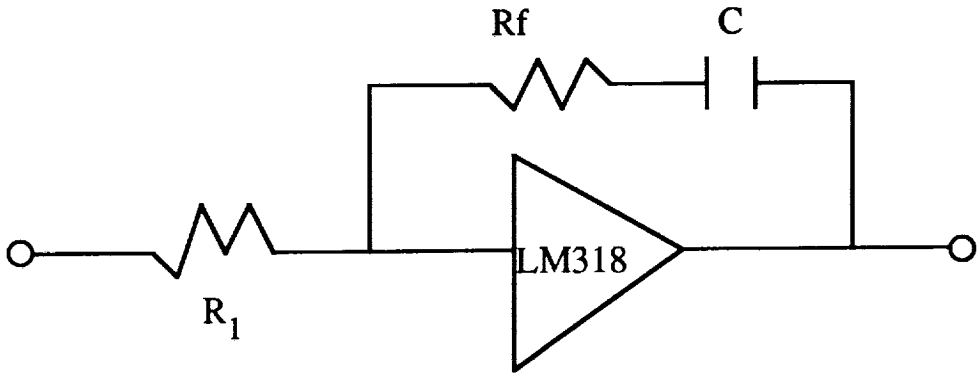


Figure 6. The Low Pass Filter Layout.

The cutoff frequency is written as

$$\omega_{Lpf} = \frac{1}{R_1 C} \quad \text{(RAD/SEC)} \qquad \text{(Ref. 1, pg. 67)}$$

and the loop natural frequency and damping factor are found by

$$\omega_N = (K\phi\ Ko\ \omega_{Lpf})^{1/2} \text{ (RAD/SEC)}$$

and,

$$\zeta = \frac{Rf\ C}{2}\ \omega_N \qquad \text{(Ref. 1, pg. 67)}$$

$K\phi Ko$ is the dc loop gain. For the active filter shown in Figure 6, the transfer function is given by

$$Fc(s) = \frac{T_2 S + 1}{ST_1} \qquad \text{(Ref. 1, pg. 154)}$$

where, $T_1 = R_1 C$

and $T_2 = R_f C$

thus yielding the system transfer function in terms of Ko & $K\phi$

$$Tc(S) = \frac{K\phi\, Ko\, (1 + ST_2)}{S^2 + \left(\frac{K\phi\, KoT_2}{T_1}\right) S + \frac{K\phi Ko}{T_1}} \qquad \text{(Ref. 1, pg. 154)}$$

where, $$\omega_N = \left(\frac{K\phi Ko}{T_1}\right)^{1/2} = \left(\frac{K\phi Ko}{R_1 C}\right)^{1/2} = (K\phi Ko\omega_{Lpf})^{1/2}$$

and $$\zeta = \frac{T_2}{2}\left(\frac{K\phi Ko}{T_1}\right)^{1/2} = \frac{R_f C}{2}\underbrace{\left(\frac{K\phi Ko}{R1\, C}\right)^{1/2}}_{\omega_N}$$

or $$\zeta = \frac{Rf\, C}{2}\ \omega_N$$

such that the equation for the system time constant can be rewritten as

$$Tc(s) = \frac{2\zeta\omega_N S + \omega_N^2}{S^2 + 2\zeta\omega_N S + \omega_N^2}.$$

The dominant characteristics may be approximated by the 2nd order system

$$S2 + 2\zeta\omega_N S + \omega_N^2.$$

For the breadboarded design of 1 MHz, a capture range of 10 percent (0.9 MHz to 1.1 MHz) is desired. The capture range may be written as

$$\omega c = 2\zeta\omega_N$$

and recall that $$\zeta = \frac{R_f C}{2}\,\omega_N$$

and $$\omega_N = (K\phi Ko\omega_{Lpf})^{1/2}$$

thus $$\omega c = 2\zeta\omega_N = 2\left(\frac{R_f C}{2}\right)\omega_N^2 = \frac{Rf\ C\ K\phi Ko}{Ri\ C}$$

or $$\omega c = \frac{Rf\ K\phi Ko}{Ri} \rightarrow fc = \frac{1}{2\pi}\left(\frac{Rf\ K\phi Ko}{Ri}\right)$$

Since

(Capacitance Ratio) $$CR = \frac{Cv\ min}{Cv\ max} = \left(\frac{V\ max}{V\ min}\right)^{\rho}$$ (Ref. 2, pp. 3-8)

from data book $$K\phi = \frac{0.16V}{\pi RAD}$$

now solving for Ko:

$$\omega o = \frac{1}{(LC)^{1/2}} = \frac{1}{\left[L\ CV_{min}\left(\frac{Vmin}{Vop}\right)^{\rho}\right]^{1/2}}$$

$$Ko = \frac{d\omega o}{dv} = \frac{1}{(L\ 120pf)^{1/2}}\left(\frac{Voper.}{2}\right)^{\left(\frac{\rho}{2}-1\right)}\left(\frac{1}{2}\right)$$

Voperating = 5 volts, ρ = 1.43, L = 0.25 mH

$$Ko = \frac{1}{2p[(.25mh)(120pf)]^{1/2}}\left(\frac{5}{2}\right)^{\left(\frac{1.43}{2}-1\right)}\left(\frac{1}{2}\right)$$

$$Ko = 353{,}769\ \frac{Hz}{VOLT}$$

$$fc = \frac{1}{2\pi}\frac{Rf}{Ri}K\phi Ko = \frac{1}{2\pi}\left(\frac{1.6K}{2K}\right)\left(\frac{0.16V}{\pi\ RAD}\right)\left(353{,}769\ \frac{Hz}{VOLT}\right)$$

$fc = 90.4$ KHz $\approx$ 100 KHz

Since $$\omega_N = \left(\frac{K\phi Ko}{Ri\ C}\right)^{1/2}$$ and $$fn = \frac{1}{2\pi}\left(\frac{K\phi Ko}{Ri\ C}\right)^{1/2}$$

$$\zeta = \frac{Rf\ C}{2}\omega_N = \frac{Rf\ C}{2}\left(\frac{K\phi Ko}{Ri\ C}\right)^{1/2}$$

$$\zeta^2 = \frac{Rf^2C^2}{4}\left(\frac{K\phi Ko}{Ri\,C}\right) = \left(\frac{Rf}{Ri}\right)\left(\frac{1}{4}\right) Rf\,C\,K\phi Ko$$

and substituting

$\zeta = 0.8$

$0.64 = (0.8)(1/4)(1.6)(C)(113{,}280)2\pi$

$0.0028uF = C$

thus, design valves

$Rf = 1.6K,\ Ri = 2K,\ C = 0.0028uF$

$fc \approx 100\ KHz,\ \zeta = 0.8$

DESIGN OF LOOP FILTER FOR 50 MHz PC BOARD

It is necessary to make sure that the integration time of the low pass filter (integrator) is fast enough in order to keep the overall system from becoming sluggish. The RC time constant needs to be drastically reduced to process the information rapidly. With R set at 1.6kΩ, a value of 56pF is chosen for a time constant of 8.9×10^{-8} Sec.

DESIGN CONSIDERATIONS FOR THE VCO

The voltage controlled oscillator is a network whose output frequency is directly proportional to its input control voltage as shown in Figure 7.

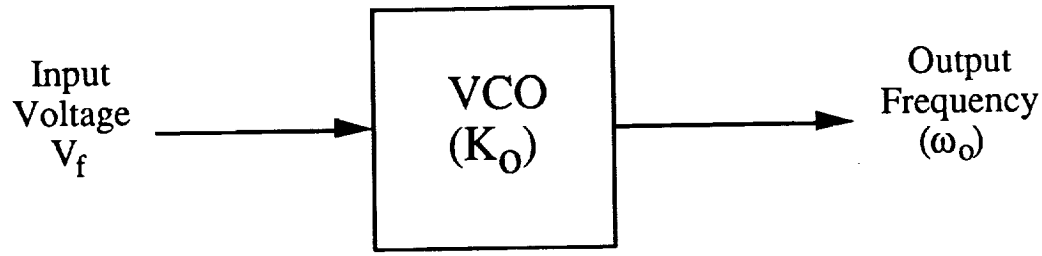


Figure 7. VCO Block Diagram.

The VCO can be thought of as a voltage to frequency converter and may be represented by the relation

$$\omega_o = K_o V_f \qquad \text{(Ref. 1, pg. 54)}$$

ωo is the VCO output frequency, Vf is the input voltage that appears at the VCO from the loop filter and Ko is the VCO conversion gain.

The MC1648 (MECL 14 Pin package) is chosen for the VCO integrated circuit. The emitter-coupled device requires an external parallel inductor-capacitor or LC "tank" network to produce oscillation. When the MC 1648 is used as a VCO in phase-locked loop systems, a voltage controlled diode (MV1404) is generally used as part of the tank circuit.

DESIGN OF THE VCO: (1 MHz)

The ratio of the capacitance at two separate applied voltages for the varactor is defined by

$$\text{(Capacitance Ratio)} \quad CR = \frac{Cv\ min}{Cv\ max} = \left(\frac{V\ max}{V\ min}\right)^{\rho}$$

and from the data sheet for Vr = 2V and 1 MHz, we have a CR = 10 and a voltage range of 2 to 10 volts for the MV1404. Thus solving for ρ we have

$$10 = \left(\frac{10\ VOLTS}{2\ VOLTS}\right)^{\rho}$$

$$10 = 5^{\rho}$$

$$\log 10 = \rho \log 5$$

$$1.43 = \rho$$

Now solving for Cv max:

$$\frac{Cv\ min}{Cv\ max} = \left(\frac{V\ max}{V\ min}\right)^{\rho}$$

$$\frac{120pf}{Cv\ max} = \left(\frac{10}{2}\right)^{1.43}$$

$$Cv\ max = 12pf\ \text{(at 10 Volts)}$$

Now solving for Cvmin:
Since Cr = 10, and from previous step Cvmax = 12pf

$$CR = \frac{Cv\ min}{Cv\ max}$$

$$10 = \frac{Cv\ min}{12pf}$$

$$[\text{at 2 Volts}]\ 120pf = Cv\ min$$

Now, our attention will turn to the resonant frequency of the tank circuit. Recall the design is for 1 MHz. Since

$$f = \frac{1}{2\pi (LC)^{1/2}}$$

different L&C values will be tried to find a suitable operating range around 1 MHz.

Try L = 2.5mh, from data book Cin = 6pf

$$f_{min} = \frac{1}{2\pi\,[L(C_{pmax} + C_{in})]^{1/2}}$$

$$f_{min} = \frac{1}{2\pi\,[2.5mh\ (120pf + 6pf)]^{1/2}}$$

$$f_{min} = 283\ KHz$$

$$f_{max} = \frac{1}{2\pi\,[L(C_{pmin} + C_{in})]^{1/2}}$$

$$f_{max} = \frac{1}{2\pi\,[2.5mh\ (12pf + 6pf)]^{1/2}}$$

$$f_{max} = 750\ KHz$$

Try L = .25mh

$$f_{min} = 896\ KHz$$

$$f_{max} = 2.3\ MHz$$

$$C\ operating \approx 100\ pf\ (from\ data\ book)$$

$$So\ f\ (operating\ point) = \frac{1}{2\pi\,[0.25\ mh/(100\ pf)]^{1/2}}$$

$$frequency\ (operating\ point) = 1.007\ MHz$$

Thus for 1 MHz:

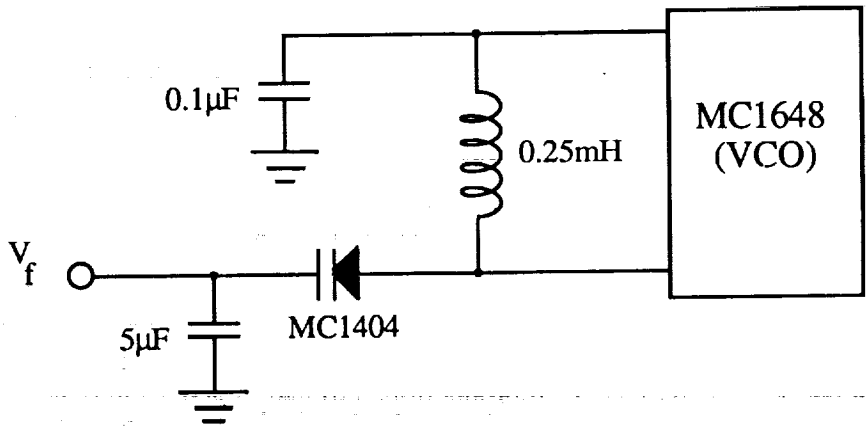


Figure 8. DESIGN FOR VCO.

DESIGN CONSIDERATIONS FOR VCO DESIGN AT 50 MHz

The inductor value L will be based on the capacitance value. Looking at the capacitance:

$$C_T \geq C\ min + C\ parasitic + C\ in$$

$$C_T \geq 10pF + 0.5pF + 6pF$$

$$C_T \geq 16pF$$

Assume c ≈ 20pF for some operating voltage

$$f = \frac{1}{2\pi (LC)^{1/2}}$$

or

$$L = \frac{1}{(2\pi f)^2 C}$$

$$L = \frac{1}{(2\pi \ 50x10^{-6})^2 (20x10^{-12})}$$

$$L = 0.5 \text{ uH}$$

Since the fvco is the extracted clock that is used to aid in the recovering of the unknown input data, it would be informative to see a typical example of how this extracted clock is fed through a decoding circuit to reconstruct the data. The details of the decoding circuit are described in Figure 9. One can see the gating used ($fin \cdot \overline{4fin} \cdot fctr$) to recover the input data where fctr is simply some multiple of the extracted clock.

The only major changes in component size for the 50 MHz pc board compared to the 1 MHz layout are the Cf = 56pF and for the VCO (L = 0.5uH).

DESIGN CONSIDERATIONS FOR A HIGH FREQUENCY PC BOARD USING SMARTWORK

The use of a software package to design the artwork for modern electronic layouts of printed-circuit boards (PCB) has replaced the generation of taped artwork. The design and production of artwork for the phase-lock loop (PLL) printed-circuit board (PCB) was achieved by the use of a software package known as "Smartwork".

"Smartwork" is a software package used with a compatible personal computer, which has color/graphics capabilities. It is intended to aid in the design and production of artwork for printed-circuit boards. The screen of the computer monitor becomes a window that shows a portion of a large layout workspace. This window can be moved around the workspace to show any portion of this layout. One side or both sides of the board can be viewed simultaneously.

Using the keyboard, pads and traces can be placed or removed. All conductors are perfectly vertical, horizontal, or at 45 degrees. The program insures that conductor spacing is adequate and that widths do not become too narrow for reproduction. All pad to pad spacing is fixed at multiples of .05 inches. The program also understands electrical connections. For example, if the user wants to connect two conductors with a conductive trace, the user identifies the two conductors using the cursor. The program will automatically find the shortest route and connect the two conductors. The program will not allow any other conductor to be crossed. Two trace widths are allowed. These are a thin trace for low current connections and a wider trace for higher current, such as, power supply traces (VCC and ground connections). If more space is needed between traces or conductors, the program allows the user to spread the layout along any vertical or horizontal axis. Any connection which existed before spreading the layout is maintained by appropriate conductors. The spreading is limited to a maximum board size of ten by sixteen inches. The layout may be saved as a standard DOS disk file when completed or before further editing is needed. These files may be duplicated or used to make different revisions to a board

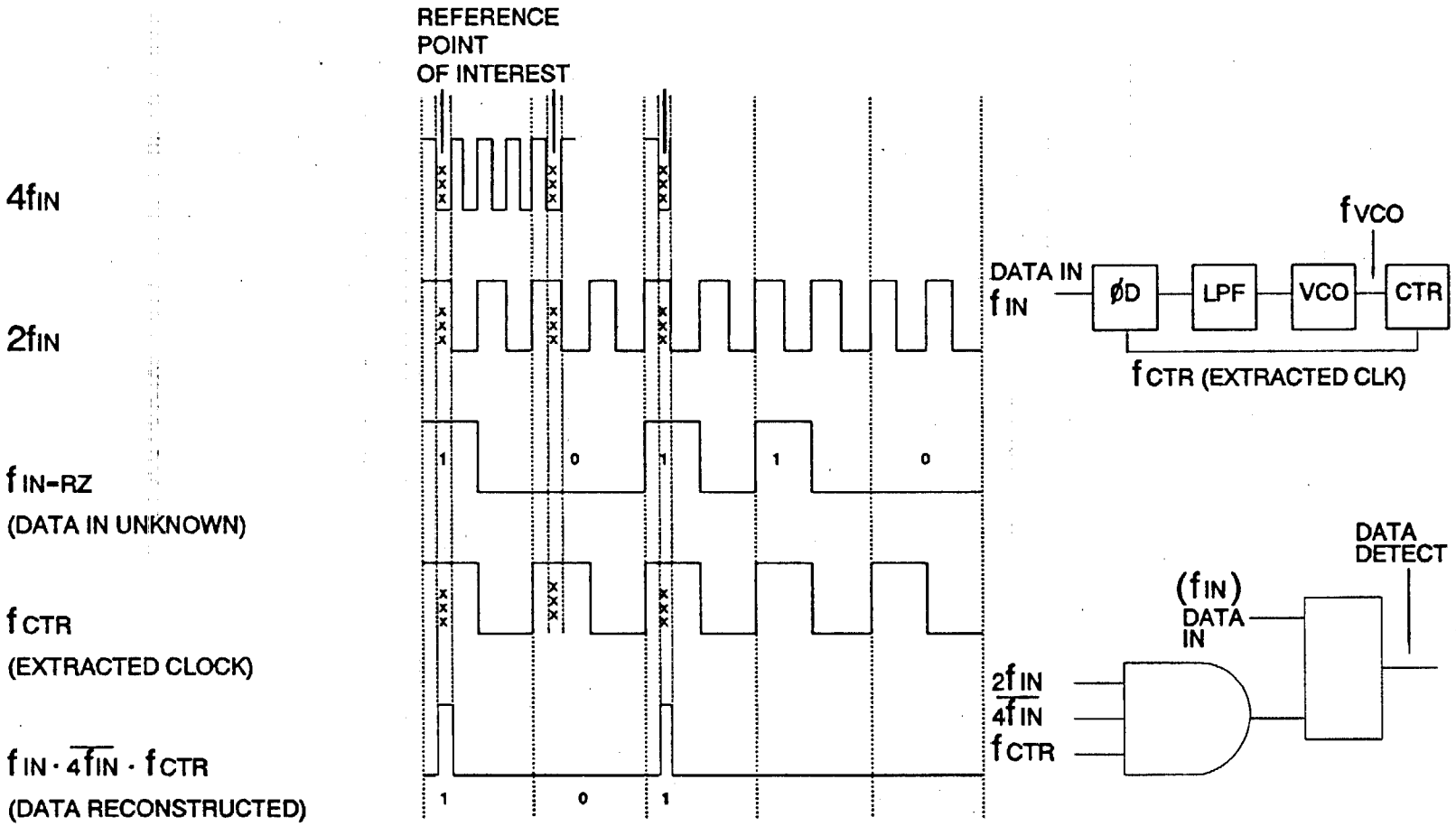


FIGURE 9. ILLUSTRATION OF TYPICAL DECODING CIRCUIT USED TO RECONSTRUCT UNKNOWN INPUT DATA

starting from a single master. Paper copies of the artwork are produced using a dot-matrix printer. Paper, vellium, or polyester copies may be created using a pen-and-ink plotter. Camera-ready artwork is available from either output device at twice the normal size (2x artwork). A normal-size (1x artwork) checkplot can also be printed to verify that components will be physically fit on the printed-circuit board (see figures 10 and 11).

PROCEDURES FOR THE FABRICATION OF A HIGH FREQUENCY PC BOARD

1. Implement the art work for the pc board using Smartwork on a compatible personal computer.
2. Print out the artwork on printer. A positive of both the top and bottom of the pc board to be made.
3. At this point you will have to send in the positives to the photolab to be made into negatives. Finished negatives should be on polyester film. The top half of the negative should end up with the emulsion side on the bottom of the polyester film. The bottom half of the negative should end up with the emulsion side on the top of the polyester film.
4. After receiving your negatives back from the photolab, you are now ready to make your pc board. To make your pc board, obtain a photosynthesized pc board. Before removing it from its cover, make sure you are in an area where the light is subdivided.
5. Place the negatives on the appropriate sides of the pc board. Make sure the negatives are aligned properly on both sides.
6. Place each side of the photosynthesized pc board under ultraviolet light for 2 minutes.
7. Next, place the pc board in a glass tray containing trichloroethlene. Leave each side submerged for approximately 3 minutes.
8. Pour Ferric Chloride into the etcher and place pc board into the solution for approximately 4 minutes. The machine will etch the pc board (Etching process).
9. The board is now cut to desired size and drilled accordingly.
10. Submerge pc board into the Tin Plating Solution (Tinning Process).

EXPERIMENTAL RESULTS

Figure 12 is the circuit diagram for the PLL operating at 1 MHz. The only major changes in the components for the 50 MHz PC board (see Figure 12) are the feedback capacitor is 56pF (loop filter) and the inductor (0.0028uF for 1 MHz) for the VCO is 0.5 uH (0.25mH for 1 MHz). Also, the capacitors at the stage between the output of the phase detector and the input of the loop filter are 220pF (0.1uF for 1 MHz). After the circuit was breadboarded at 1 MHz, operation of the VCO was found to be at around 600 KHz for the 5 volt nominal operating point. Measurements were made to confirm the inductance of the coil. The value of parasitic capacitances were also determined to be around 6pF from the manufacture's data sheets. All deviations from expected values failed to resolve the difference in predicted versus measured operating frequency. It was apparent that the varactor capacitance differed considerably from the manufacture's specifications. The calculated capacitance of 100pF was put in place of the varactor and fvco approached 1 MHz, thus confirming the varactor capacitance discrepancy. Final measurements for the 1 MHz PLL capture range are shown in Table 1.

Similar design procedures were utilized for the 50 MHz printed-circuit board. Laboratory measurements are shown in Table 2. Problems and observations were much like the ones encountered with the 1 MHz circuit. A photograph of the 50 MHz printed-circuit board is shown in figure 13.

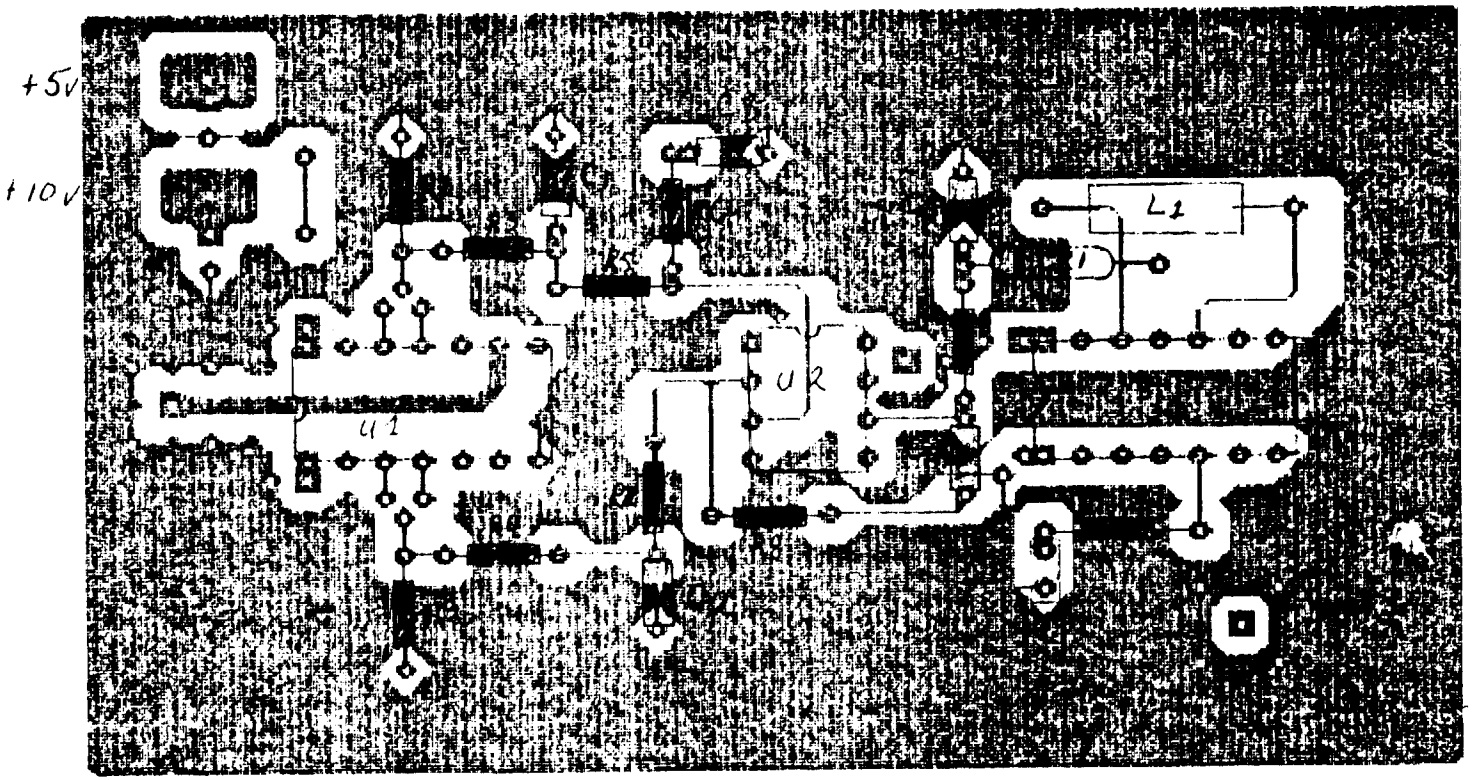


FIGURE 10. ARTWORK (2X) COMPONENT SIDE

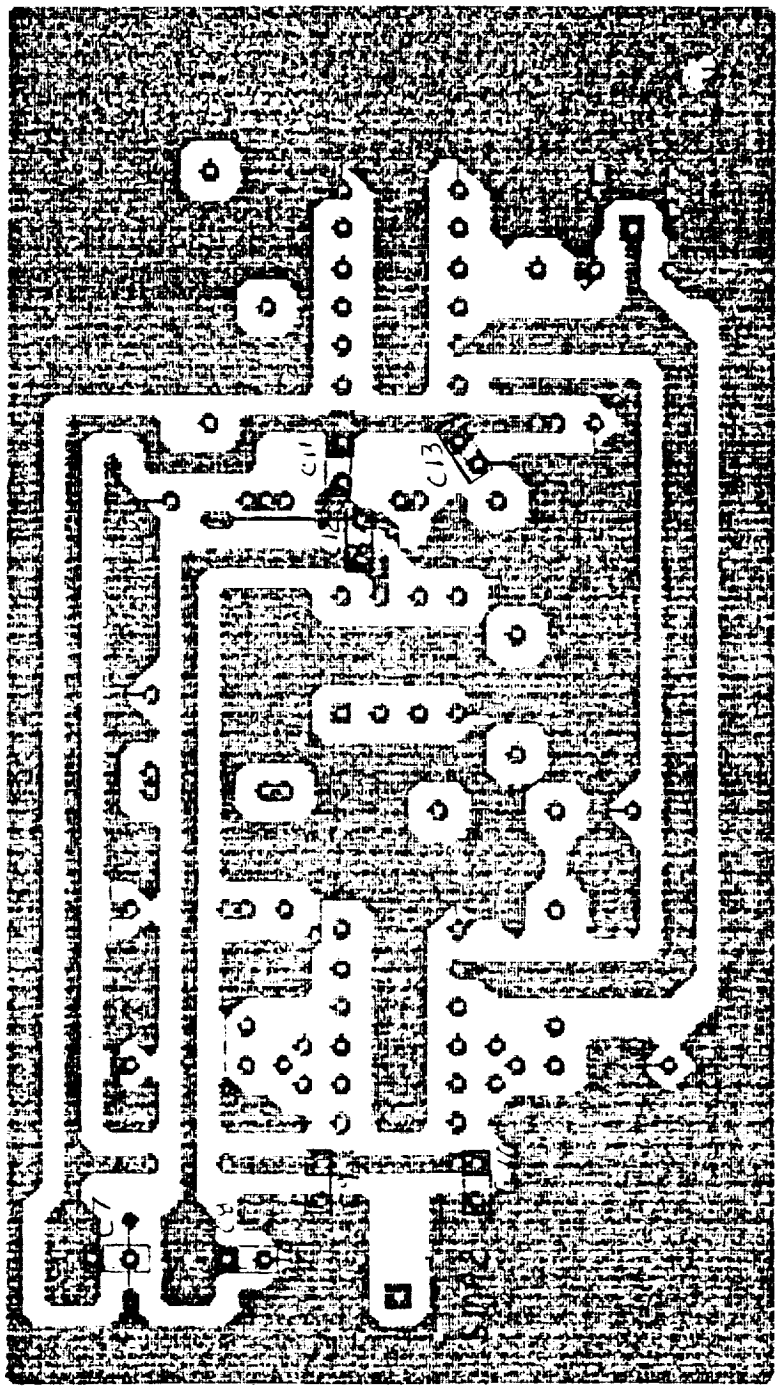


FIGURE 11. ARTWORK (2X) SOLDER SIDE

Table 1: PLL 1 MHz (Breadboard)

Desired Capture Range (Lower End)	900 KHz
Actual Capture Range (Lower End)	800 KHz
% Error	11.1%
Desired Capture Range (Upper End)	1.1 MHz
Actual Capture Range (Upper End)	1.2 MHz
% Error	9.09%

Table 2: PLL 50 MHz (Printed-Circuit Board)

Desired Capture Range (Lower End)	45 MHz
Actual Capture Range (Lower End)	38 MHz
% Error	15.5 %
Desired Capture Range (Upper End)	55 MHz
Actual Capture Range (Upper End)	62 MHz
% Error	12.73 %

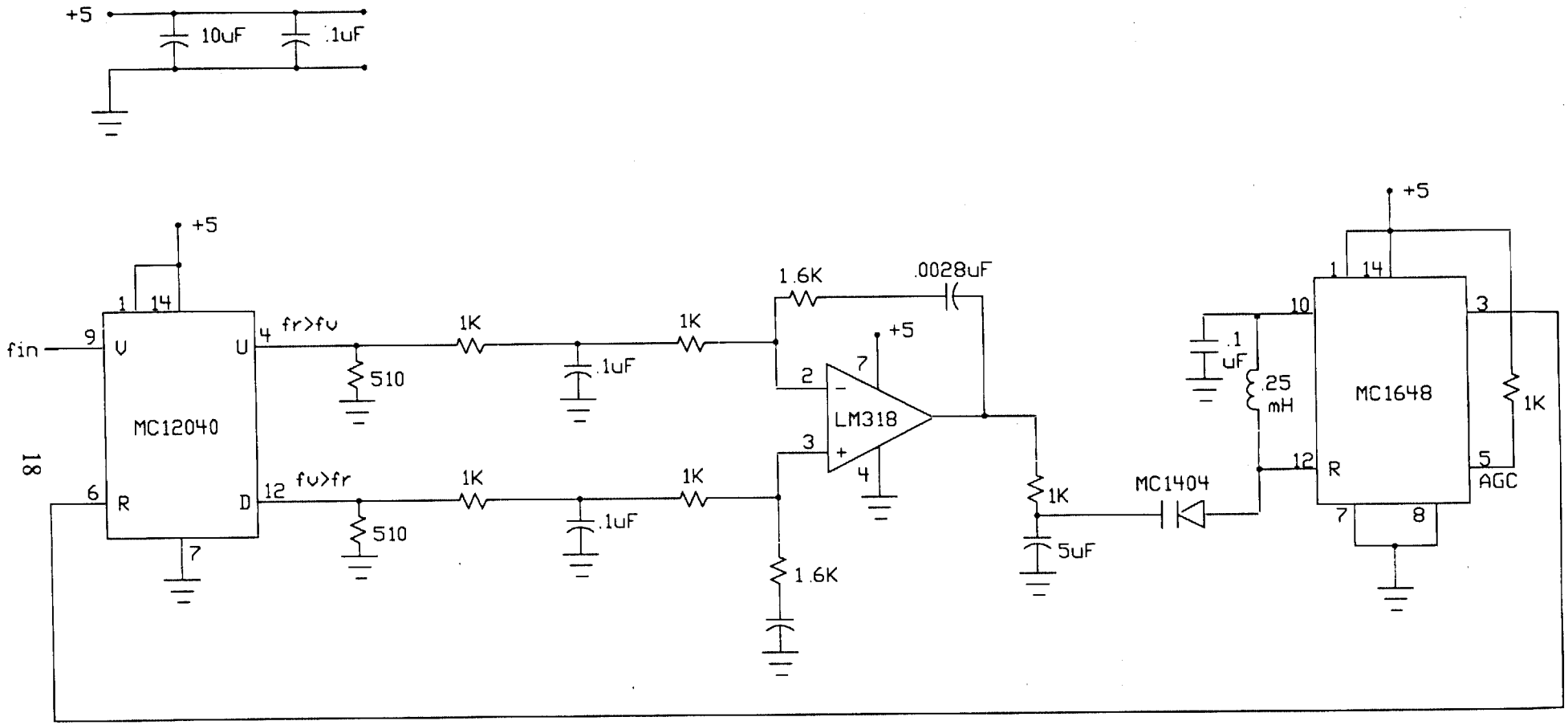
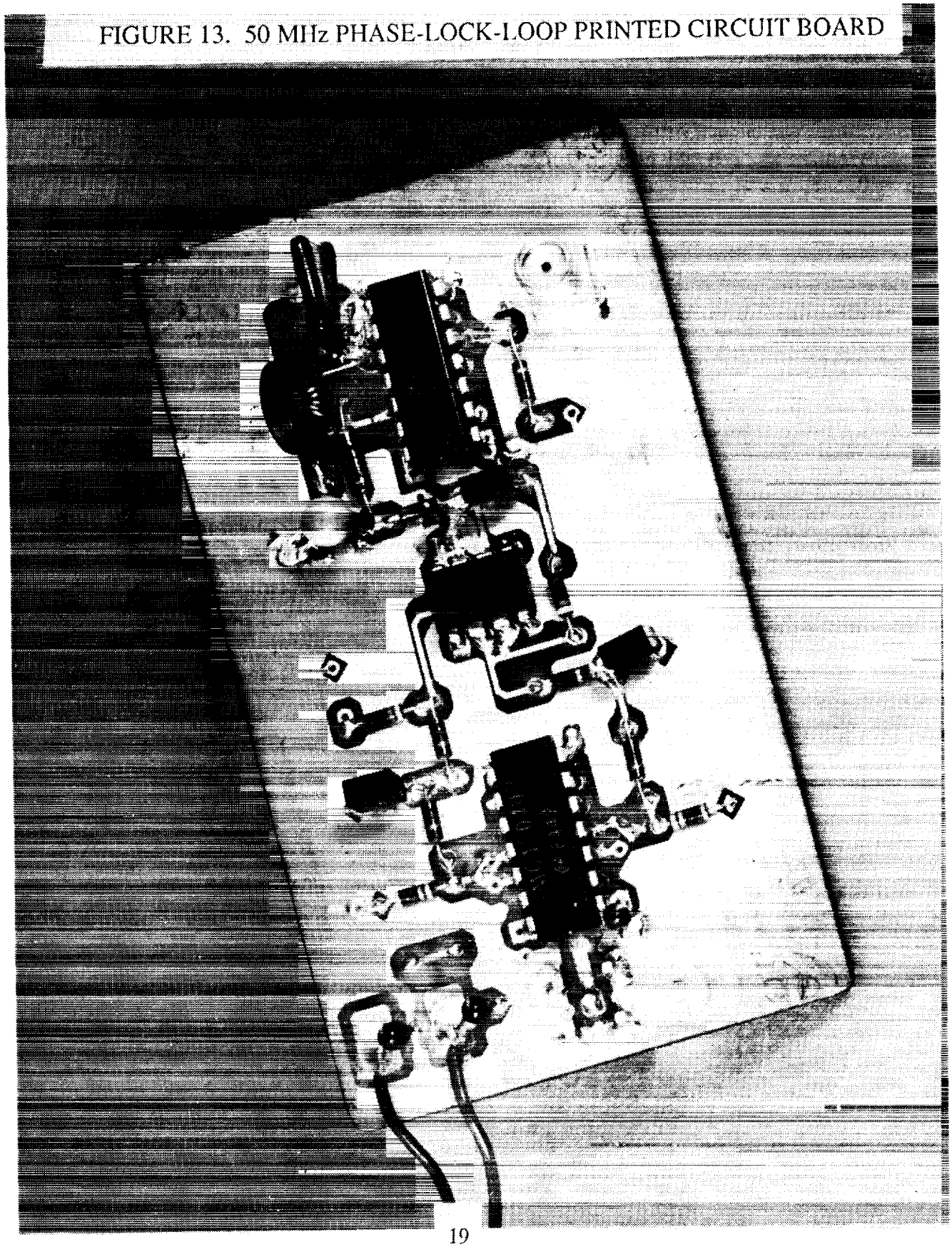


FIGURE 12: PHASE-LOCK-LOOP CIRCUIT DIAGRAM

FIGURE 13. 50 MHz PHASE-LOCK-LOOP PRINTED CIRCUIT BOARD



CONCLUSIONS

Due to the rapid evolutionary advances of integrated-circuit technology, the phase-lock loop system has established itself as one of the basic building blocks in the electronics revolution. Fifteen years ago when the PLL was fabricated out of transistors, the cost overshadowed applications in industry. It is now feasible to fully realize the capabilities of the phase-locked loop system.

This report formulates a theoretical approach for designing a phase-lock loop circuit. The theoretical analysis can be used with faster components, such as gallium arsenide (GaAs) devices to design PLL's at higher data rates. A high-speed PLL would provide NASA with one of the integral parts of an optical transceiver which is necessary to achieve high data rates in an optical communication system.

The capture range of the circuit design is fairly narrow in frequency. The PLL circuit should perform much better if the capture range were greater. However, greater capture range implies more instability, at the very least, from insufficient filtering of the output of the phase detector. That is, residual ripple from the square wave output from the phase detector will cause greater and greater instantaneous jitter in the VCO output as observed in the laboratory.

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16. Abstract

Phase-locked loop circuits are frequently employed in communication systems. In recent years digital phase-locked loop circuits have been utilized in optical communications systems. In an optical transceiver system the digital phase-locked loop circuit is connected to the output of the receiver to extract a clock signal from the received coded data (NRZ, Bi-Phase or Manchester). The clock signal is then used to reconstruct or recover the original data from the coded data. This report describes a theoretical approach to the design of a digital phase-locked loop circuit operating at 1 MHz and 50 MHz. These theoretical design analyses could be applied to an optical transceiver system design. Hardware implementation of a breadboard design to function at 1 MHz and a printed-circuit board designed to function at 50 MHz were assembled using Emitter Coupled Logic (ECL) to verify experimentally the theoretical design.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
Phase-Lock Loop, Phase Detector, Low Pass Filter, Voltage Controlled Oscillator	Unclassified - Unlimited Subject Category 33

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