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SILICON CARBIDE, AN EMERGING HIGH TEMPERATURESEMICONDUCTOR

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ABSTRACT

In recent years, the aerospace propulsion and space power communities have expressed a growing need for electronic devices that are capable of sustained high temperature operation. Applications for high temperature electronic devices include development instrumentation within engines, engine control and condition monitoring systems, and power conditioning and control systems for space platforms and satellites. Other earth-based applications include deep-well drilling instrumentation, nuclear reactor instrumentation and control, and automotive sensors.

To meet the needs of these applications, the High Temperature Electronics Program at the Lewis Research Center is developing silicon carbide (SiC) as a high temperature semiconductor material. Research is focussed on developing the crystal growth, characterization and device fabrication technologies necessary to produce a family of silicon carbide electronic devices and integrated sensors. This paper will present the progress made in developing silicon carbide and discuss the challenges that lie ahead.

INTRODUCTION

In recent years, the aerospace propulsion and space power communities have acknowledged the growing need for electronic devices that are capable of sustained high temperature operation. Applications for high temperature electronic devices include development instrumentation within engines such as multiplexers analog-to-digital converters, and telemetry systems capable of withstanding hot section engine temperatures in excess of 600^0 C. Similarly, engine mounted integrated sensors and electronics could reach temperatures which exceed 500^0 C while uncooled operation of control and condition monitoring equipment in advanced sustained supersonic aircraft would subject electronic devices to temperatures in excess of 300^0 C (1). Hypersonic vehicles will ultimately pose even more severe demands on electronic devices and sensors.

In addition to aeronautics, there are many other areas that would benefit from the existence of high temperature electronic devices. Space applications include power electronic devices for Space Station Freedom, space platforms, and satellites. Since power electronics require radiators to dissipate waste energy (heat), electronic devices that are capable of operating at higher temperatures would allow a reduction in radiator size. This results in a weight savings and thereby reduces the cost of placing the hardware into orbit.

The need for electronic devices capable of sustained operation at high temperature is not restricted to the aerospace community. Earth-based applications include deep-well drilling instrumentation, power electronics for motor control, nuclear reactor instrumentation and control and automotive electronics and sensors.

To meet the needs of the applications mentioned above, the High Temperature Electronics Program at the Lewis Research Center is developing silicon carbide (SiC) as a high temperature semiconductor material. This program supports two major elements of the Center's mission: to perform basic and developmental research aimed at improving (1) aerospace propulsion, and (2) power systems. Research is focussed on

developing the crystal growth, crystal characterization and device fabrication technologies necessary to produce a family of SiC devices.

SILICON CARBIDE: THE SEMICONDUCTOR

Silicon Carbide (SiC) is familiar to most as the abrasive grit material on sandpaper. It is, however, a material that possesses many other useful properties. Crystalline SiC can be found in refractory, structural and electrical applications as well as the common abrasive applications. Due to its extreme hardness (only diamond and boron carbide are harder) SiC grit is used extensively in lapping, grinding, cutting, and polishing operations. As a refractory material, SiC is used as a protective coating on components exposed to high temperature and/or corrosive environments. In the aerospace industry, SiC fibers are of interest as a high strength, low density reinforcement material.

It is the semiconducting properties of electronic grade SiC crystals that make it particularly attractive for high temperature applications. This is because SiC possesses a wide energy bandgap. The maximum operating temperature for a semiconductor is determined by the forbidden bandgap energy. The useful temperature limit is reached when the number of intrinsic carriers, thermally excited across the energy gap, approaches the number of purposely added (extrinsic) carriers. This temperature (when expressed as the absolute temperature) is roughly proportional to the energy bandgap. Depending on the particular polytype (structural form) of SiC, the bandgap energy varies from 2.2 eV to 3.3 eV.

Based on the inherent solid state properties of silicon (bandgap energy of 1.1 eV), the maximum temperature at which a silicon device could theoretically operate is 300^0 C. Conventional silicon electronic devices are rated to operate at temperatures up to 125^0 C, i.e., the MIL-SPEC (military specifications) limit. Since the desired operating temperature for some of the applications mentioned above approaches 600^0 C, it is clear that a new semiconductor material will have to be developed. Another choice as a high temperature semiconductor based upon its bandgap energy might be gallium arsenide which could theoretically operate at 460^0 C, but it has not proven operationally stable at this temperature. Using the same criteria as applied to silicon, SiC could theoretically be employed as a semiconductor at temperatures as high as 1200^0 C. A more reasonable, shorter term goal is to produce electronic devices capable of 600^0 C operation.

In comparing potential candidate materials for high temperature semiconductor devices, SiC stands out not only because of its excellent high temperature electronic properties but also because it is a very stable ceramic material up to temperature of 1800^0 C. The combination of the material's high thermal conductivity (heat transfer) and high breakdown field (tolerant of high electric fields) provides the potential for improved power electronic systems and for increasing the number of devices per unit area. Those properties which determine the high frequency characteristics of semiconductor devices also appear to be excellent for SiC and superior to those of silicon or gallium arsenide.

Component reliability is a key issue in all aerospace applications because failure can lead to expensive or tragic consequences. Electronic devices or sensors that are capable of operating at high temperatures have the immediate payoff of improved reliability when operated at lower temperatures. For example, if electronic devices capable of 300^0 C operation possess the same failure rate at 300^0 C as devices specified for 125^0 C operation, the failure rate will be reduced by 1000 when the "300^0C" electronic devices are operated in a 125^0 C environment. This three orders of magnitude improvement in reliability is due to the exponential dependence of failure rates on temperature. Based on its properties, the reliability of electronic devices and sensors fabricated from SiC should be much higher than that obtainable from any current semiconductor material.

SILICON CARBIDE CRYSTAL GROWTH

With all the advantages that SiC possesses, why has SiC technology not been incorporated into electronic systems? The main problem has been the lack of SiC single crystals suitable for device fabrication purposes. Until recently, there was no process whereby single crystals of SiC with sufficient size, purity, and perfection

could be grown reproducibly. SiC does not melt at any reasonable temperature and pressure conditions so this rules out the "growth-from-melt" technique commonly used to obtain other semiconductor single crystals such as silicon and gallium arsenide.

Historically, vapor phase growth processes have proven to be the most successful method for producing SiC crystals. Early research was done on SiC crystals that were a by-product of the industrial Acheson process for making sandpaper grit and abrasives (2). In the Acheson process, SiC is formed at 2400^0 by the reaction of silica and coke. At this temperature, gas pockets can form within the SiC reaction product. The SiC sublimes and then condenses on the inside walls of gas pockets located at cooler parts of the reaction product. Occasionally, isolated SiC crystals are produced within these pockets during the production process. The larger and better crystals were hand selected for electrical research purposes.

In 1955, Lely developed a laboratory version of the industrial sublimation process and was able to produce rather pure SiC crystals (3). Encouraged by the Lely process, NASA Lewis and other laboratories pursued the development of SiC semiconductor devices during the 1960's and early 1970's. Though SiC devices were demonstrated above 400^0 C, by the early seventies the Lely process and other processes had not matured to the point where high-quality large-area crystals could be grown reproducibly. Since crystal substrates are crucial to device fabrication, interest in SiC waned, and from 1973 to 1980, there was very little effort in the U.S. on SiC. However, research did continue in Japan and in Europe during this period.

In 1980, because of the increased need for high temperature electronics in advanced turbine engines, NASA Lewis again embarked on a high temperature electronics program. The emphasis again has been on developing SiC. The problem regarding the crystal growth of SiC is rooted in the fact that SiC crystals can take on many different structural forms called polytypes. The many polytypes of SiC (over 140) differ from one another in the stacking sequence of the SiC double layers. Depending on the stacking, either cubic, hexagonal or rhombohedral structures are possible. The two most common SiC polytypes are 3C-SiC and 6H-SiC representing the cubic and hexagonal structures, respectively. In the early research, SiC crystals grown by sublimation techniques were a mixture of different polytypes. Since each SiC polytype has its own electronic properties (i.e., bandgap energy, carrier mobility, etc.), sublimation grown SiC crystals usually contain heterojunctions and possess unpredictable and non-uniform electronic properties.

To favor growth of a single polytype of SiC, epitaxial growth on a host crystalline substrate from gases containing silicon and carbon was hypothesized. The host crystal imparts its crystalline regularity to the thin growing layer. Since silicon is available in perfect, large, and low-cost crystals, many attempts at the heteroepitaxial growth of SiC on Si were made. These efforts were largely unsuccessful because of the large lattice mismatch that exists between Si and SiC (e.g., the SiC lattice is 20% smaller that the Si lattice).

Large area heteroepitaxial growth of 3c-SiC on Si was finally achieved at the NASA Lewis Research Center in 1982 by using a chemical vapor deposition (CVD) process (4). Crystal growth takes place at atmospheric pressure in a fairly conventional horizontal CVD system. A complete system description is given in reference 5. The CVD reaction system is illustrated schematically in Figure 1. To grow a single crystal 3C-SiC, first an electronic grade silicon substrate is placed on an rf-heated graphite susceptor. The essential step in the growth process is a rapid temperature ramp from near room temperature to a growth temperature of 1360^0 C in the presence of a hydrocarbon gas. The NASA Lewis Research Center process uses propane as the carbon containing gas. During the first two minutes of growth, a single crystal 3C-SiC film about 20-nm-thick is produced on the Si substrate. After this initial SiC growth, silane gas is added to provide a silicon source for the final step, the bulk growth of 3C-SiC to the desired thickness. During this time, the 3C-SiC layer grows at a rate of 3 to 4 μ m/hr.

3C-SiC is a transparent, yellow crystal which fractures into regular rectangular pieces. Although visually the material appears to be of relatively good quality, in actuality a high density of defects exists in the crystal. Certain defects can adversely affect the electrical properties of SiC devices. During the past eight years, much progress has been made in understanding problems associated with 3C-SiC grown on Si but much research remains to be done in this area.

A recent development in SiC crystal growth is having an enormous impact on SiC research. A SiC research team at North Carolina State University announced the successful implementation of a seeded-growth sublimation method to produce the 6H-SiC polytype in boule (large cylinder) form (6). A private company, Cree Research, Inc., has developed this process to the point where 1-inch diameter wafers of 6H-SiC crystals can now be used as substrates for SiC epitaxial growth via the CVD processes already developed. Growth of high quality 6H-SiC epitaxial films has now been achieved at NASA Lewis using 6H-SiC wafers as substrates (7). Figure 2 is a photograph comparing a Cree Research Inc. SiC wafer with available Lely SiC crystals. Prior growth experiments had been performed on irregular-shaped Lely or Acheson SiC crystals but the small size and uncertain quality of these crystals make them unsuitable for commercial production.

Doping (intentional insertion of the extrinsic carriers) the epitaxial films with electrical impurities to produce n-type and p-type SiC is vital to the realization of electronic devices. Addition of nitrogen gas to the growth process gases results in nitrogen incorporation into the SiC lattice. Since nitrogen is a donor impurity in SiC, n-type SiC is produced. To produce p-type SiC, aluminum has been used as an acceptor impurity. Aluminum is incorporated by adding trimethylaluminum to the growth process gases.

CHARACTERIZATIONOF SiC FILMS

Initially, the transition from the Si substrate to the 3C-SiC epitaxial layer was thought to occur by means of a thin buffer layer or transition layer of the order of 20-nm-thick (4). However, high resolution transmission electron microscopy (TEM) has demonstrated that the SiC/Si interface is abrupt with no transition region (8). the 3C-SiC films do contain a large density of defects that include interfacial twins, stacking faults, and inversion domain disorder (9). The defect density in the films is greatest near the SiC/Si interface and decreases with distance away from the interface.

A particular type of lattice defect, called inversion domain boundaries (IDB's) was reported to be present in all SiC films grown on Si (10). The IDB's can be made visible by chemical etching, sputter etching, wet oxidation or 3C-SiC growth in the presence of diborane (11). IDB's form in the initial stages of growth on the Si substrate when SiC islands of opposite phase nucleate and grow together. Across the IDB, the chemical bonding is between like atoms (i.e., Si-Si or C-C), instead of the normal Si-C bond between neighboring atoms.

Normally, in epitaxial growth on Si, the surface of the Si substrate is oriented precisely parallel to an atomic plane, e.g., the (001) plane. It had been found in the growth of gallium arsenide on Si, that IDB's are eliminated by orienting the substrate slightly off-axis from the (001) plane. This technique was applied to SiC growth at NASA Lewis with the result that for Si substrates that were tilted 1^0 to 4^0 from the (001) plane, all IDB's were eliminated from the films grown. In addition, the resultant SiC films were smoother by a factor of 2 to 3 than the films grown on-axis substrates (11). Further work is needed to determine the effect on electrical properties and the performance of devices fabricated from these films. Also, the optimum tilt angle and the direction of tilt have yet to be determined.

Electrical characterization to determine electrical properties of the SiC films is an important and necessary evaluation step if high quality SiC films are to be achieved. To determine the carrier concentration and carrier mobility, room temperature Hall measurements were made on n-type 3C-SiC films grown at NASA Lewis using the van der Pauw configuration (12). Ohmic electrical contacts consisted of sputtered tantalum followed by sputtered gold. In order to perform a detailed analysis of the charge carrier concentration, three 3C-SiC films were selected for Hall measurements over the temperature range 50-300K. Experimental results for the films studied showed that the films are highly compensated with a ratio of acceptor (p-type) to donor (n-type) atoms of 0.90. At this time, the identity of the donor and acceptor impurities is not clear. Crystal defects such as vacancies, interstitial atoms, antisite atoms, stacking faults, or dislocation may be acting as donor and acceptor impurities.

It is believed that all present day 3C-SiC films grown at NASA Lewis and elsewhere are compensated. The consequence of compensation is degradation of device quality. Compensated semiconductors have many

ionized impurities (positive for donors and negative for acceptors) embedded in the crystal lattice and these ions serve as scattering centers for moving charge carriers. This increases the impurity scattering and reduces the total mobility of the charge carrier compared to uncompensated material with the same density of free carriers. Identification and eventual elimination of the compensating impurities remains a research goal.

As mentioned above, the 3C-SiC films epitaxially grown on Si substrates contain many lattice defects indicating that Si is not the perfect host substrate, at least not when using the current growth processes. The availability of 6H-SiC substrates for epitaxial growth of SiC films is now steering the growth research away from 3C-SiC growth on Si and toward 6H-SiC growth on 6H-SiC.

The defect density in 6H-SiC films grown on 6H-SiC substrates is reduced by a minimum of three orders of magnitude compared to the 3C-SiC films. This is expected to have a very positive effect on SiC device characteristics. As more 6H-SiC films are produced, characterization techniques that have been developed for 3C-SiC films will be systematically employed. At this time, structural characterization (cross sectional transmission electron microscopy), optical characterization (low-temperature photoluminescence), and electrical characterization of both n and p type 6H-SiC films are underway.

Sic DEVICE FABRICATIONTECHNOLOGY

The availability of SiC substrates now allows NASA Lewis to place increasing emphasis on device fabrication. In-house research is pursuing the fabrication of in-situ grown junction diodes and metal-insulator-semiconductor field effect transistors (MISFETs).

Junction diodes were produced by first growing an 8-micrometer-thick n-type 6H-SiC film, and then growing an additional 0.75-micrometer-thick p-type 6H-SiC film with trimethylaluminum added to the process gases. Aluminum was incorporated into the growing SiC film to produce p-type material. An array of diode mesa structures was then formed by photolithography followed by reactive ion etching using sulfur hexafluoride and oxygen gases. Electrical contacts, aluminum to the p-type and gold/tantalum to the n-type, were applied by sputter deposition.

A typical current-voltage (I-V) curve for one of the 6H-SiC grown-junction diodes at room temperature and at 600^0 C is shown in Figure 3. the function of a diode is to allow current to pass in one direction (the forward direction), but not in the opposite (reverse) direction. Hence, an ideal I-V curve would be nearly vertical in the forward direction, and nearly horizontal in the reverse direction. As seen in the I-V curves, the electrical characteristics of the SiC diode change very little when operated from room temperature to 600^0 C. This is a significant result because the diode (e.g., p-n junction) is a basic building block for electronic devices. In addition to rectification, junctions are also used extensively as isolation layers. For example, an n-channel field-effect-transistor (FET) can be fabricated by first growing a p-type layer followed by an n-type layer. Current flow will then be confined to the n-layer if the voltage polarities are chosen so as to reverse bias the junction.

A depletion-mode metal-oxide-semiconductor field-effect-transistor (MOSFET) was fabricated using the principles of channel isolation as described above. In an FET structure, the current flow is controlled by applying a voltage to the gate electrode. For an n-channel FET, a negative voltage applied to the gate will deplete the channel of electrons and thus "pinch-off" the current flow. In this manner, an FET resembles a switch. The switch is turned on and off by the application of the gate voltage. Figure 4 shows the I-V characteristics of the MOSFET at room temperature and at 500^0 C. Although the electrical characteristics of the FET are not ideal, the achievement of transistor I-V characteristics at 500^0 C is an extremely important starting point.

CONCLUDING REMARKS

Ultimately, the goal of the NASA Lewis High Temperature Electronics Program is to develop SiC integrated circuits and monolithic sensors with compensating and signal conditioning electronics integrated into the sensor structure. Electronic devices and sensors that are capable of operating at elevated temperatures eliminate or reduce the amount of cooling that is required. In many space applications, this can be a significant weight savings. Other payoffs of high temperature integrated sensors include reduced cabling and shielding requirements and development of distributed control architectures, i.e., smart actuators.

The development of semiconductor materials does not occur over night. First germanium, then silicon and then gallium arsenide, for example, have come to the marketplace after years in the laboratory and many dollars spent for development cost. The history of SiC as a high-temperature semiconductor has been one of high expectations followed by disappointment. Recent advances in crystal growth of SiC and the increased knowledge of the bulk material properties of the grown SiC are cause for renewed enthusiasm. Although the development of SiC falls into the category of high-risk research, the future looks very promising and the potential payoffs are tremendous. SiC now appears ready to emerge as a useful semiconductor material.

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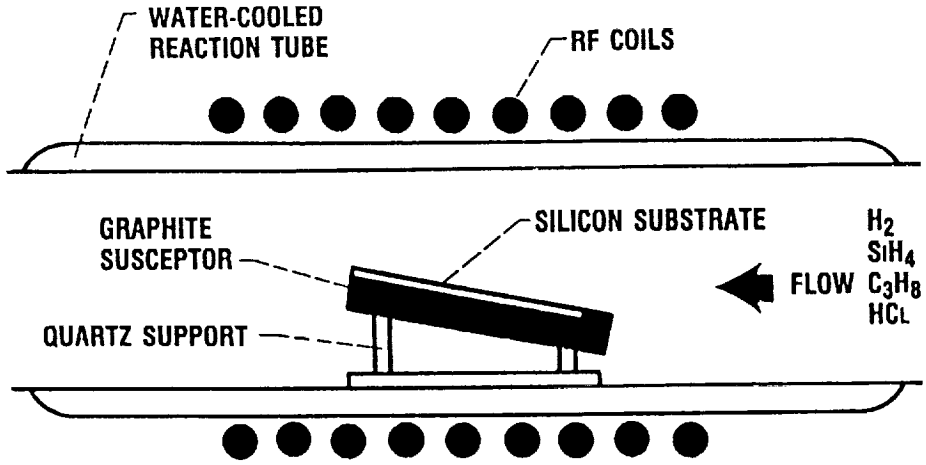


FIGURE 1. SCHEMATIC DIAGRAM OF REACTION CHAMBER FOR EPITAXIAL SiC CRYSTAL GROWTH

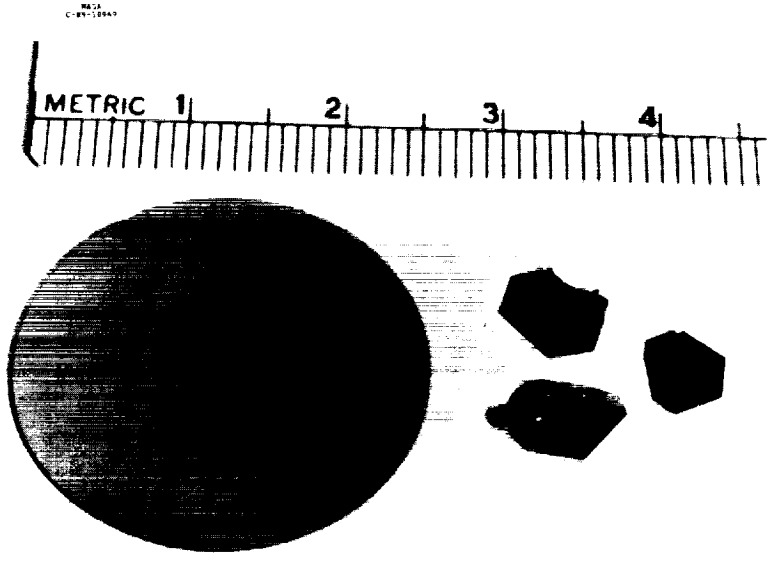


FIGURE 2. LEFT: CREE RESEARCH INC. 6H-SiC WAFER
RIGHT: LELY 6H-SiC CRYSTALS

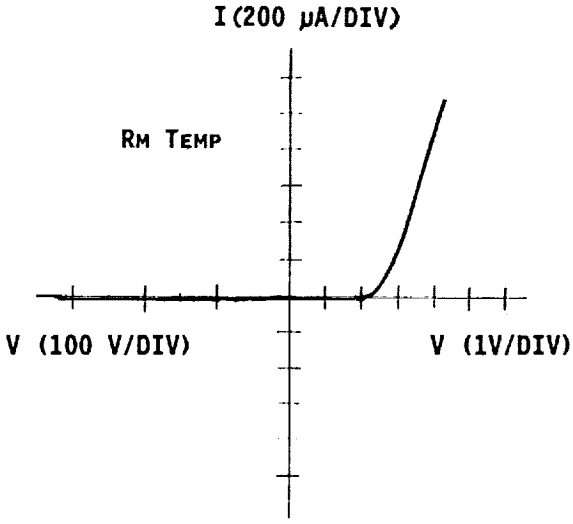


FIG. 3A

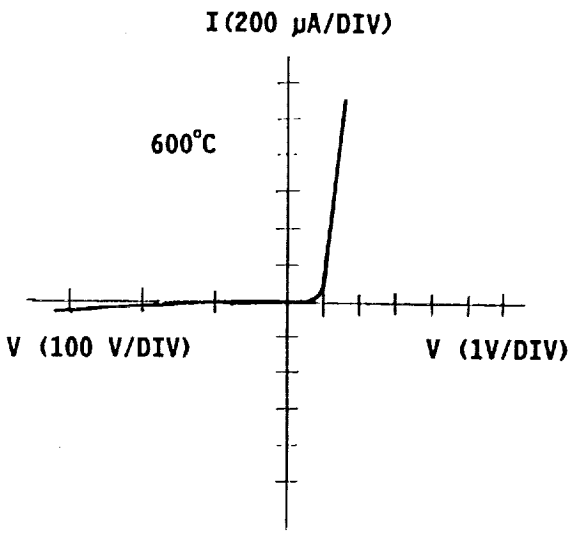
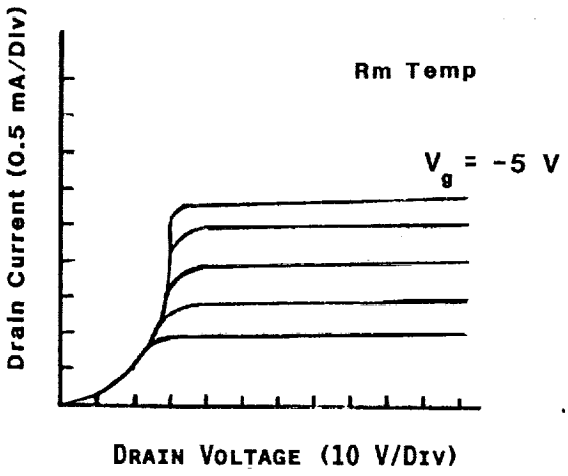


FIG. 3B

FIGURE 3. CURRENT-VOLTAGE (I-V) CURVES FOR A 6H-SiC GROWN JUNCTION DIODE



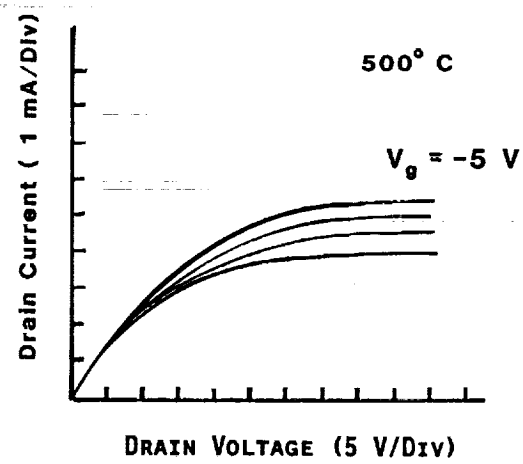


FIGURE 4. CURRENT-VOLTAGE (I-V) CURVES FOR A 6H-SiC DEPLETION-MODE MOSFET