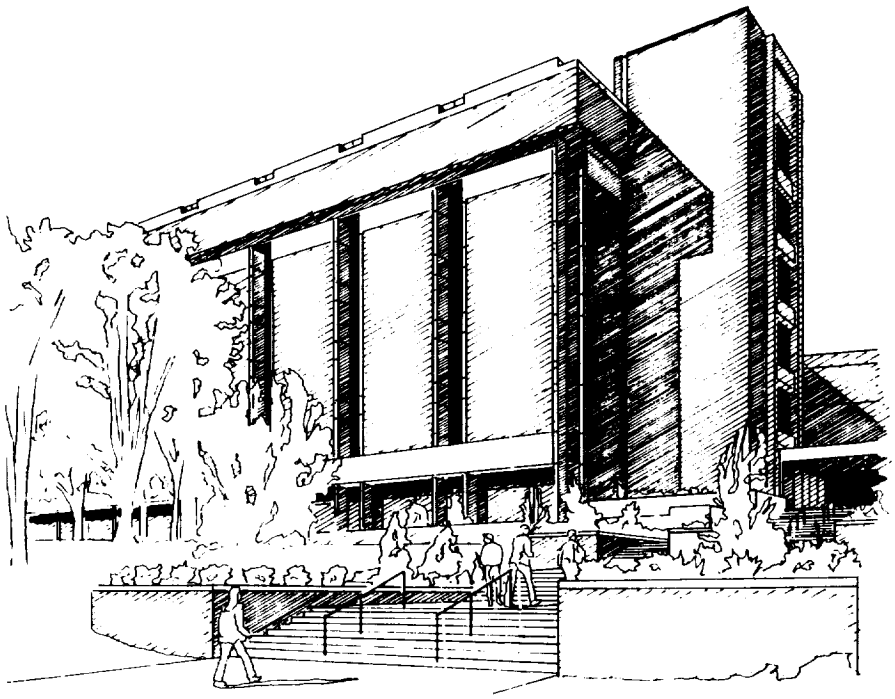

UNIVERSITY OF CINCINNATI
COLLEGE OF ENGINEERING

FINAL TECHNICAL REPORT

NASA COOPERATIVE AGREEMENT

NCC-167

Department of Electrical and Computer Engineering

FINAL TECHNICAL REPORT
NASA COOPERATIVE AGREEMENT NCC-167

Title:	MMIC Integration Technology Investigation
Period:	March 5, 1990 to June 15, 1991
NASA Grants Office:	Ms. Lorene Albergottie Cooperative Agreement & Grants Officer NASA-Lewis Research Center Mail Stop 500-315 21000 Brookpark Road Cleveland, Ohio 44135
Technical Officer: (NASA-LeRC)	Mr. Kurt A. Shalkhauser Dr. Charles A. Raquet Mail Stop 54-8 NASA-Lewis Research Center Cleveland, Ohio 44135
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MMIC Integration Technology Investigation

PERSONNEL ASSOCIATED WITH THE RESEARCH

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2.	Michael D. Biedenbender	Full Time Graduate Student Completed Ph.D. Degree in Electrical Engineering in Feb. 1991 Supported by this cooperative agreement/grant

PART ONE

POWER COMBINER

FOUR-TO-ONE POWER COMBINER FOR 20 GHz PHASED ARRAY ANTENNA USING RADC MMIC PHASE SHIFTERS

The design and microwave simulation of two-to-one and four-to-one microstrip power combiners is described. The power combiners were designed for use in a four element phased array receive antenna subarray at 20 GHz. Four test circuits are described which were designed to enable testing of the power combiner and the four element phased array antenna. Test Circuit 1 enables measurement of the two-to-one power combiner. Test Circuit 2 enables measurement of the four-to-one power combiner. The four element antenna array uses hermetic coaxial feedthroughs indicated in Figure 1 for connection between the antenna patch and the microstrip transmission lines. Test Circuit 3 enables measurement of a four element antenna array without phase shifting MMICs in order to characterize the power combiners with the antenna patch-to-microstrip coaxial feedthroughs. Test Circuit 4 is the four element phased array antenna including the RADC MMIC phase shifters and appropriate interconnects to provide bias voltages and control phase bits.

Several microwave hybrid junctions can be used to divide an input signal from one port into two or more output signals. The same circuits can also be used to produce a single output proportional to the sum of two or more input signals. For a microstrip implementation a Wilkinson power divider (combiner) is one of the easiest to fabricate. Rizzi [1] provides an excellent description of the operation of the Wilkinson power divider. Details from the description by Rizzi are included below to explain how the Wilkinson power divider works.

Figure 2 shows the basic Wilkinson power divider. Two quarter-wave transmission lines are connected to a common port (port 1). The resistor between the other ends of the quarter-wave transmission lines decouples ports 2 and 3. Because of symmetry a signal entering port 1 is divided equally between ports 2 and 3. A signal entering port 2 is isolated from port 3 but can be transmitted to port 1. A signal entering port 3 is isolated from port 2 but not port 1. To match all ports and

obtain isolation between ports 2 and 3 the characteristic impedance of the quarter-wave transmission line should be $2^{0.5}*Z_o$, and the resistor between ports 2 and 3 should be $2Z_o$.

The operation of the Wilkinson power divider can be explained using an even- and odd-mode analysis. In an even- and odd-mode analysis of a linear multiple-port microwave circuit the resulting port voltages are determined for excitation at 2 ports with the same voltage (even-mode excitation) and with voltages 180° out of phase (odd-mode excitation). By superposition of the even- and odd-modes the excitation for one port will cancel and the resulting voltages for excitation at a single port can be determined.

Figure 3 shows a circuit used for an even- and odd-mode analysis of the Wilkinson power divider for a voltage source V_G connected to port 2. For the even-mode excitation points a and b must be at the same potential and no current flows through the resistor R. Points d and c may be open circuited without affecting the even-mode operation. Figure 4 can be used as the equivalent circuit for even-mode analysis. By choosing the characteristic impedance of the quarter-wave line as $2^{0.5}Z_o$ the circuit is matched at ports 2 and 3, and $Z_{2e}=Z_{3e}=Z_o$. The even-mode voltages at the ports are $V_{2e}=V_{3e}=V_G/4$ and $V_{1e}=-j2^{0.5}V_G/4$.

For the odd-mode excitation the potential of points d and c is zero and they can be shorted to ground. Figure 5 can be used as the equivalent circuit for odd-mode analysis. The input to the quarter-wave shorted line is an open circuit and the input impedances for the odd-mode are $Z_{2o}=Z_{3o}=R/2$. For a perfect match $R=2Z_o$ as described above. The odd-mode voltages at the ports are $V_{2o}=V_G/4$, $V_{3o}=-V_G/4$, and $V_{1o}=0$.

Superimposing the even- and odd-mode solutions for an input at port 2 yields the following voltages: $V_1=-jV_2/2^{0.5}$, $V_2=V_G/2$, $V_3=0$, and $V_{ab}=V_2 - V_3=V_2=V_G/2$, where V_{ab} is the voltage across the resistor. For one signal at either port 2 or 3 half of the power is dissipated in the resistor and half is delivered to port 1. For the ideal Wilkinson power divider the insertion loss is 3 dB between port 2 and port 1 or between port 3 and port 1. For signals at both ports 2 and 3 a voltage is produced at port 1

proportional to their phasor sum, where $V_1 = -j(V_2 + V_3)/2^{0.5}$. The power associated with the phasor difference is dissipated in the resistor.

The design of the basic Wilkinson power divider can be made easier by including half-wave extensions of the resistive element terminations. Figure 6 shows the design used in Test Circuits 1 through 4 for the Wilkinson power divider. The design in Figure 6 includes the half-wave extension in the manner described by Abita [2]. The half-wave extensions improve the design by greatly reducing the parasitic coupling that would otherwise occur between the quarter-wave sections for the layout of Figure 2. The half-wave extensions shown in Figure 6 also provide additional means for adjustment of the circuit characteristics if desired. One disadvantage resulting from the half-wave extensions is the larger area required.

The Wilkinson power divider design shown in Figure 6 was determined using commercially available software. For the original design of the power divider and simulation of Test Circuits 1, 2, and 3 Touchstone version 1.7 from EESof was used on an IBM AT personal computer. The frequency range for the power divider design was based on the frequency range expected for the MMIC phase shifters. The center frequency expected for the MMIC phase shifters was 19.7 GHz, and the frequency range expected was 19.4 to 19.9 GHz. The design of the power divider shown in Figure 6 was optimized over the frequency range from 18 to 21 GHz.

The substrate dielectric to be used in the fabrication of Test Circuit 1 is 99.6% purity Al_2O_3, which has a dielectric constant of 9.95 ± 0.02 and a loss tangent of 0.0002. The dielectric thickness specified for all test circuits is ten mils. The conductor thickness specified is 1.5 μm (0.06 mils) of gold. For a 50Ω characteristic impedance the conductor width for the 10 mil Al_2O_3 substrate is 9.06 mils. For a $2^{0.5}*50\Omega$ characteristic impedance the conductor width is 3.62 mils. In Figure 6 and in all test circuits the above microstrip widths are rounded off to 9.0 and 3.6 mils. A minimum conductor width of 2.0 mils is

specified for the half-wave extensions, resulting in a characteristic impedance of about 83Ω.

The Touchstone program can optimize the values desired for S parameters or other microwave properties by adjusting the widths and lengths of designated microstrip transmission line sections. During the optimization of the power divider design the above conductor widths (w50=9.0 mils, w14=3.6 mils, and w12r=2.0 mils in Figure 6) were kept constant and the lengths of the quarter- and half-wave sections (l14, l12ra, and l12rb in Figure 6) were varied. The resulting lengths for the quarter- and half-wave sections were within 5% of the nominal values expected at the center frequency of the MMIC phase shifters.

The power divider design indicated in Figure 6 can withstand significant changes in the value of the thin film isolation resistor and still provide return losses and isolations less than -15 dB, with essentially unchanged insertion losses. Based on fabrication capabilities suggested by manufacturers, a tolerance of ±10% was specified for the 100Ω thin film isolation resistor in all four test circuits. If the deposited thin film resistance cannot meet the ±10 tolerance, laser trimming is to be used to obtain the correct resistance of 100Ω. Microwave simulations of Test Circuits 1, 2, and 3 are included for the nominal 100Ω thin film resistance as well as the ±10% tolerances described above.

Table 1 lists the programs used to simulate Test Circuits 1, 2, and 3, as well as the isolation resistance used during the simulation. The results to be shown below from the programs in Table 1 were determined using Touchstone version 2.1 on a SunSparc 1 workstation. Touchstone version 2.1 uses a different microstrip model [3] to determine the effects of dispersion than used in Touchstone version 1.7 [4]. The difference in microstrip models resulted in some changes in the S parameters compared to those originally calculated, but the return losses and isolations always remained below -15 dB, and the insertion losses were virtually unchanged.

Figure 7 shows the drawing used to specify the design of Test Circuit 1. Test Circuit 1 enables measurement of the two-to-one Wilkinson power divider design indicated in Figure 6. For

all test circuits Detail A specifies the Wilkinson power divider design indicated in Figure 6. Test Circuit 1 consists of a 1 inch square alumina substrate. Touchstone program pdivt1a is included in the Appendix as an example of the program used to simulate Test Circuit 1 with the nominal 100Ω isolation resistance.

Figures 8, 9, and 10 show the S parameters simulated for Test Circuit 1 with the nominal 100Ω isolation resistor (pdivt1a), the +10% or 110Ω resistor (pdivt1b), and the -10% or 90Ω resistor (pdivt1c), respectively. For all three figures the worst return loss (S_{22}) is -19.9 dB, and the worst isolation (S_{32}) simulated is -20.2 dB. The simulated insertion loss (S_{21}) is about -3.6 dB and varies less than 0.1 dB with frequency or isolation resistance. The ideal insertion loss for a Wilkinson power divider is -3 dB.

Figure 11 shows the drawing used to specify the design of Test Circuit 2. Test Circuit 2 enables measurement of the four-to-one power combiner which consists of series connected two-to-one Wilkinson power dividers indicated in Figure 6 and in Detail A of Figure 11. Test Circuits 2, 3, and 4 all use a 2.59 inch by 3 inch alumina substrate. The substrate size was determined by external connectors for control of the MMIC phase shifters, and will be discussed below for Test Circuit 4. For Test Circuits 2, 3, and 4 the output microstrip is the same and extends to the substrate edge as shown. In Test Circuit 2 the input microstrip lines were extended to the substrate edge so measurement of the four-to-one power combiner can be done. Touchstone program pdivt2a is included in the Appendix as an example of the program used to simulate Test Circuit 2 with the nominal 100Ω isolation resistance.

Figures 12 through 17 show the S parameters simulated for Test Circuit 2. For Test Circuits 2 and 3 there are 5 S parameters possible without repeated values. S_{11} corresponds to the output return loss; S_{22} corresponds to the return loss at any of the four input ports; S_{21} corresponds to the insertion loss between any of the four input ports and the output port; S_{32} corresponds to the isolation between inputs of the same Wilkinson

power dividers; and S_{42} corresponds to the isolation between inputs not connected to the same Wilkinson power divider. Because Touchstone only plots four parameters at a time, two figures are necessary to show the five S parameters for the simulation with the nominal 100Ω resistor (Figures 12 and 13), the +10% or 110Ω resistor (Figures 14 and 15), and the -10% or 90Ω resistor (Figures 16 and 17).

The worst return loss (S_{11}) simulated is -21.9 dB. The worst isolation between inputs of the same Wilkinson power divider (S_{32}) is -18.1 dB. The worst isolation between inputs of different Wilkinson power divider (S_{42}) is -27.6 dB. The insertion loss (S_{21}) is about -7.7 dB, and again varies less than 0.1 dB with frequency or isolation resistance. The ideal insertion loss expected with the series connected Wilkinson power dividers is -6 dB.

Figure 18 shows the drawing used to specify the design of Test Circuit 3. Test Circuit 3 enables measurement of a four element antenna array without phase shifting MMICs in order to characterize the antenna patch-to-microstrip coaxial feedthroughs. The coaxial feedthroughs were indicated in the Feedthrough Cross-Section drawing in Figure 1. The coaxial feedthroughs are also indicated below in the Assembly Drawing for Test Circuit 4 shown in Figure 26. The spacing of the patch antennas and feedthroughs is one inch in Test Circuits 3 and 4.

The Touchstone simulation of Test Circuit 3 does not consider the effects of the feedthroughs or patch antennas, and is essentially the simulation used for Test Circuit 2 with shorter microstrip input lines. Touchstone program pdivt3a is included in the Appendix as an example of the program used to simulate Test Circuit 3 with the nominal 100Ω isolation resistance.

Figures 19 through 24 show the S parameters simulated for Test Circuit 3. Figures 19 and 20 show simulations for the nominal 100Ω resistor. Figures 21 and 22 show simulations for the +10% or 110Ω resistor. Figures 23 and 24 show simulations for the -10% or 90Ω resistor.

The worst return loss (S_{11}) simulated is -21.4 dB. The worst isolation between inputs of the same Wilkinson power divider (S_{32}) is -17.0 dB. The worst isolation between inputs of different Wilkinson power dividers (S_{42}) is -26.4 dB. The insertion loss (S_{21}) is about -7.3 dB, and varies less than 0.1 dB with variations in frequency or isolation resistance.

Figure 25 shows Test Circuit 4. Test Circuit 4 is the four element phased array receive antenna subarray and includes the MMIC phase shifters and interconnects to provide bias voltages and control phase bits. Figure 26 indicates the Assembly Drawing of Test Circuit 4. The MMIC phase shifters are inserted in the MMIC cavities shown in Figures 25 and 26. The spacing of the bias lines indicated at the MMIC cavities corresponds to the bonding pad layout on the MMIC for the various bias lines and control bits. The bias lines on the alumina substrate are to be connected to external control circuitry using a 3M printed circuit board layout card-edge connector (part # 3415). The spacings required for the card-edge connector determine the arrangement of the bias lines at the edge of the alumina substrate, as well as the overall substrate size for Test Circuit 4.

Test Circuit 4 is a phased array antenna subarray demonstration circuit to show a total system operation of the various individual components including the patch antennas, coaxial feedthroughs, the RADC MMIC phase shifters, microstrip transmission lines and power combining circuitry, dc bias line interconnections, printed circuit board card edge connectors, and external control circuitry. For a space qualified mission a smaller subarray size with reduced area for dc bias line interconnections and smaller connectors would be necessary.

References

[1] P.A. Rizzi, Microwave Engineering Passive Circuits, pp. 365-367, Prentice-Hall, Inc., 1988.

[2] J.L. Abita, "Wilkinson Combiner with an Additional Degree of Freedom," pp. 3-5, Touchstone Users Group.

[3] M. Kirshning and R.H. Jansen, Electronics Letters, Jan. 18, 1982.

[4] W.J. Getsinger, "Measurement and Modeling of the Apparent Characteristic Impedance of Microstrip," Microwave Theory and Tech., vol. MTT-31, Aug. 1983.

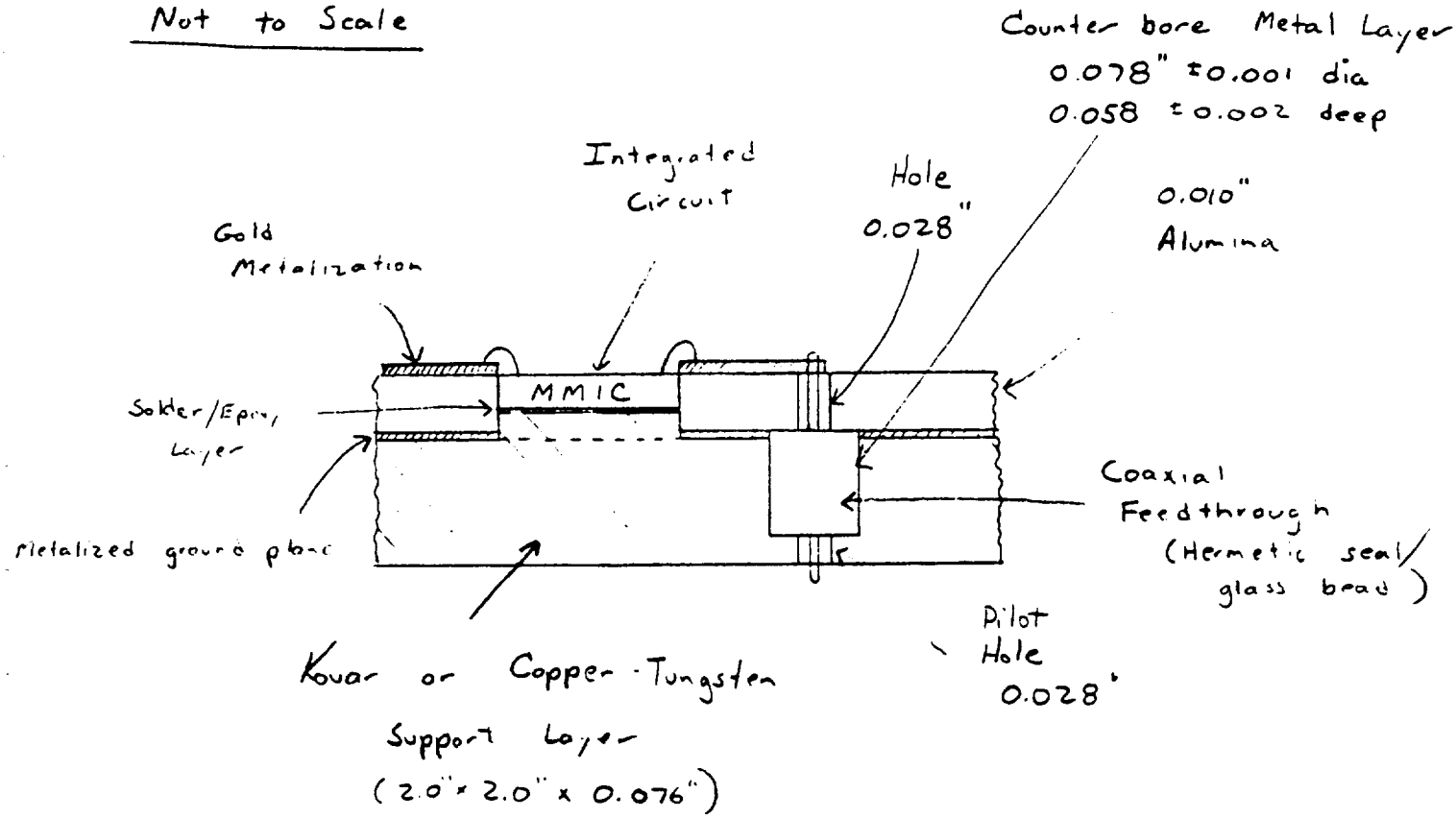
Table 1

Touchstone Programs Used to Simulate Test Circuits 1, 2, and 3

Program	Test Circuit Simulated	Isolation Resistance (Ω)
pdivt1a	1	100
pdivt1b	1	110
pdivt1c	1	90
pdivt2a	2	100
pdivt2b	2	110
pdivt2c	2	90
pdivt3a	3	100
pdivt3b	3	110
pdivt3c	3	90

4/29/90
KAS

Not to Scale



NASA/LeRC 20-GHz Receive Element

Feedthrough Cross-section

FIGURE 1

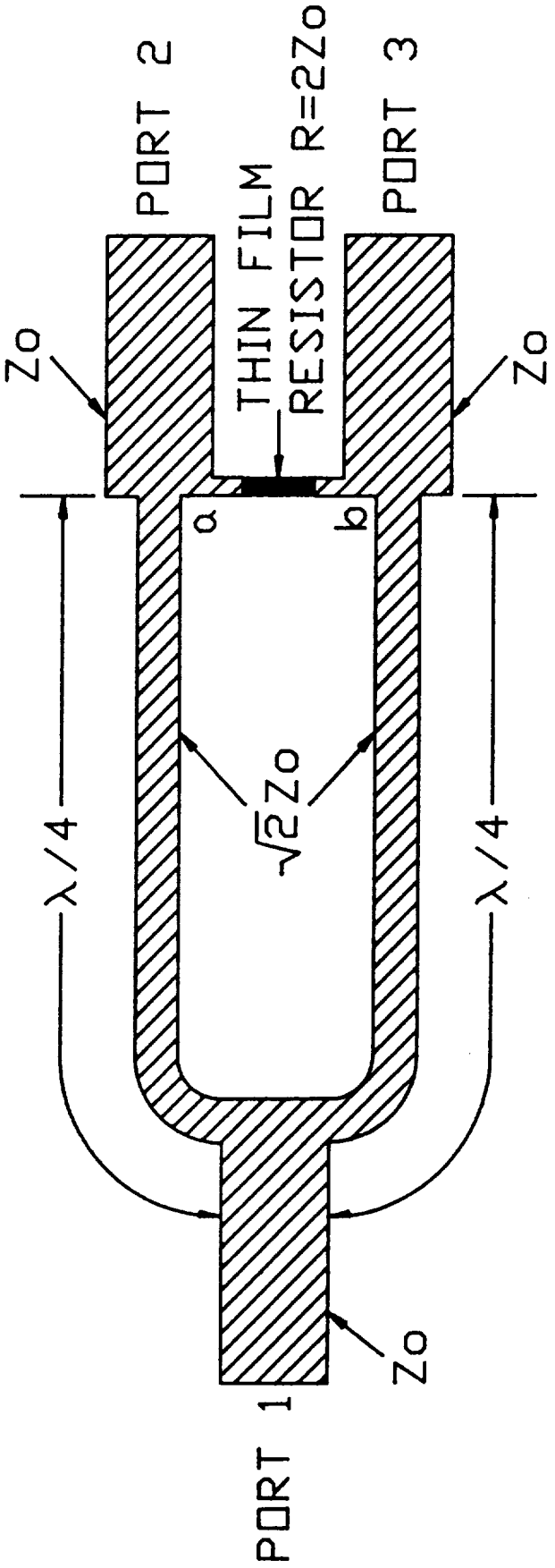

PORT 2
THIN FILM
RESISTOR R=2Zo
PORT 3
Zo
Zo
a
b
λ/4
√2Zo
λ/4
PORT 1
Zo

FIGURE 2

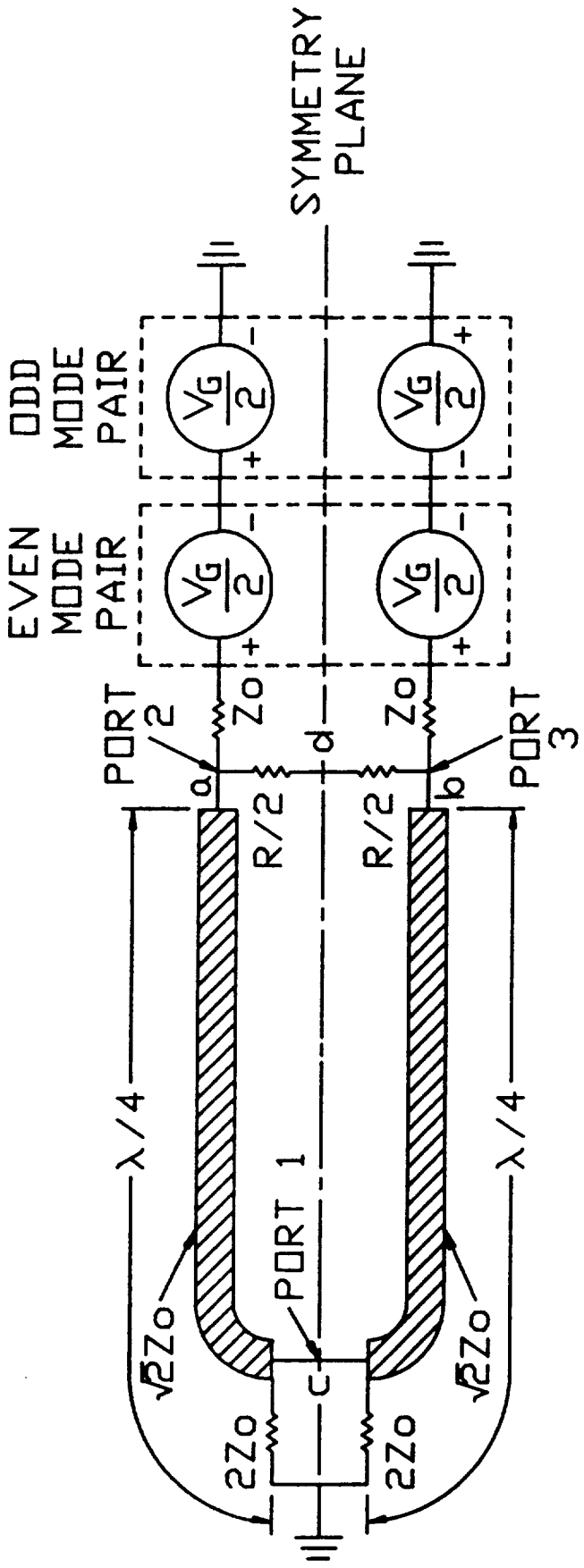

SYMMETRY PLANE
ODD MODE PAIR
EVEN MODE PAIR
VG/2
PORT 2
PORT 3
PORT 1
Zo
d
a
b
c
R/2
λ/4
√2Zo
2Zo

FIGURE 3

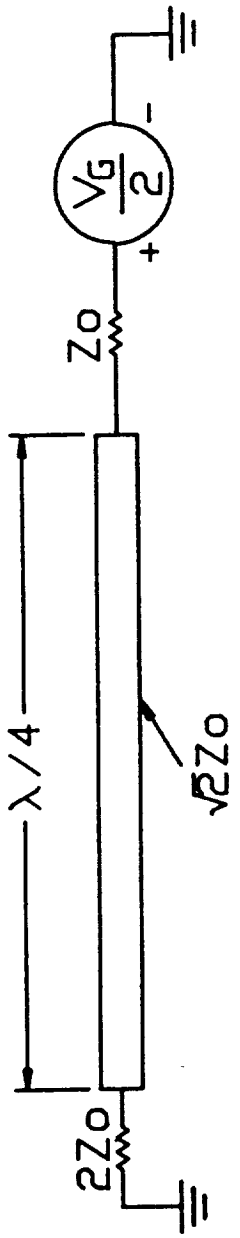


FIGURE 4

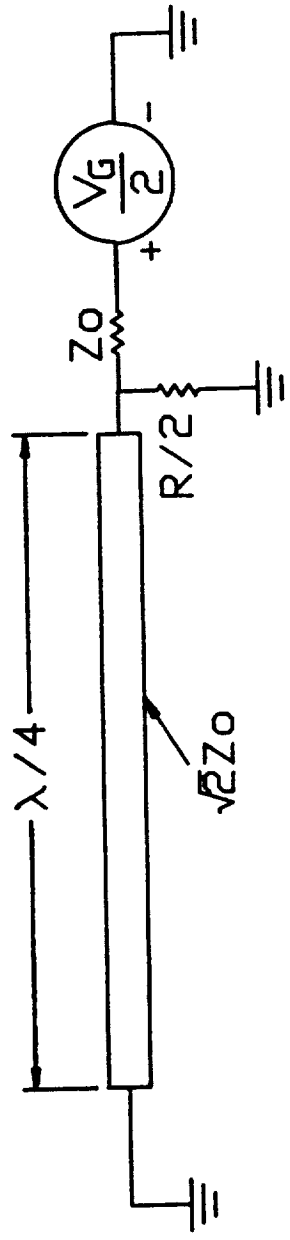


FIGURE 5

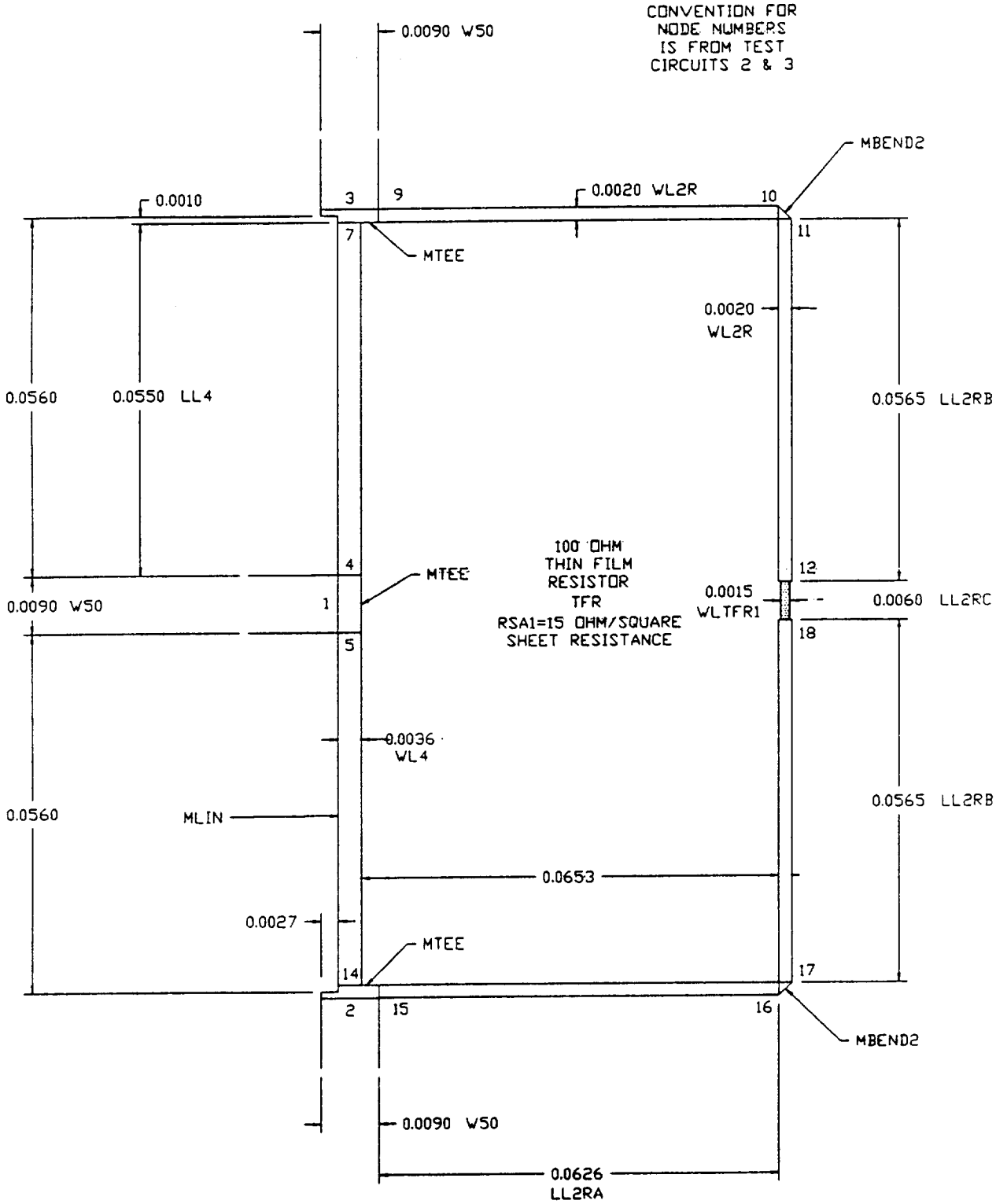
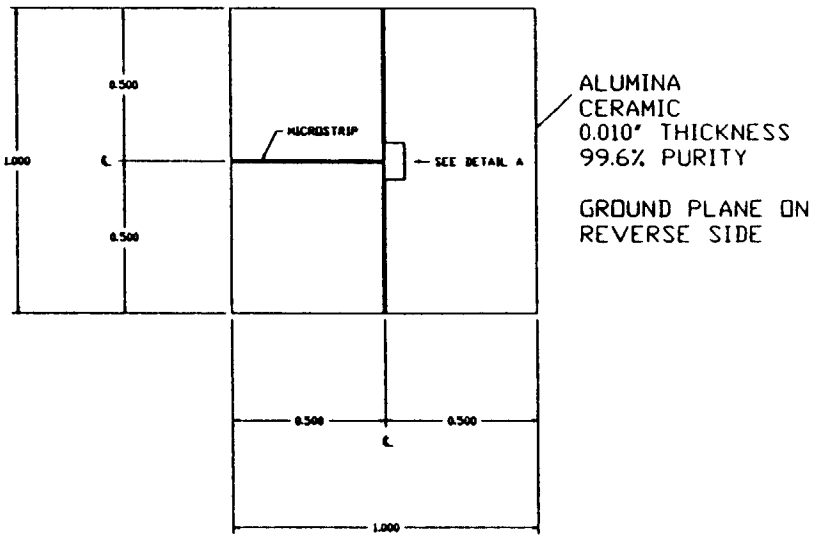

CONVENTION FOR
NODE NUMBERS
IS FROM TEST
CIRCUITS 2 & 3
0.0090 W50
MBEND2
0.0010
3
9
0.0020 WL2R
10
7
MTEE
11
0.0020
WL2R
0.0560
0.0550 LL4
0.0565 LL2RB
100 OHM
THIN FILM
RESISTOR
TFR
RSA1=15 OHM/SQUARE
SHEET RESISTANCE
4
MTEE
12
0.0090 W50
1
0.0015
WLTFR1
0.0060 LL2RC
5
18
0.0036
WL4
0.0560
MLIN
0.0565 LL2RB
0.0653
0.0027
MTEE
14
17
2
15
16
MBEND2
0.0090 W50
0.0626
LL2RA

FIGURE 6

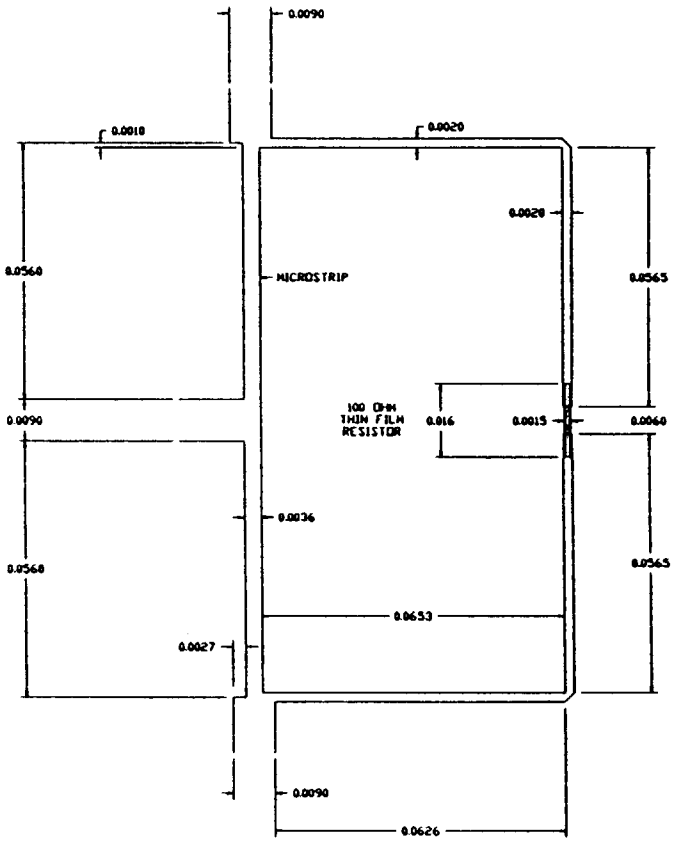
FIGURE 7

TOP SURFACE TOPOLOGY



ALUMINA
CERAMIC
0.010" THICKNESS
99.6% PURITY

GROUND PLANE ON
REVERSE SIDE



DETAIL A

SEE ATTACHED SPECIFICATION
FOR FABRICATION INSTRUCTIONS
ALL DIMENSIONS IN INCHES

NASA TEST CIRCUIT 1

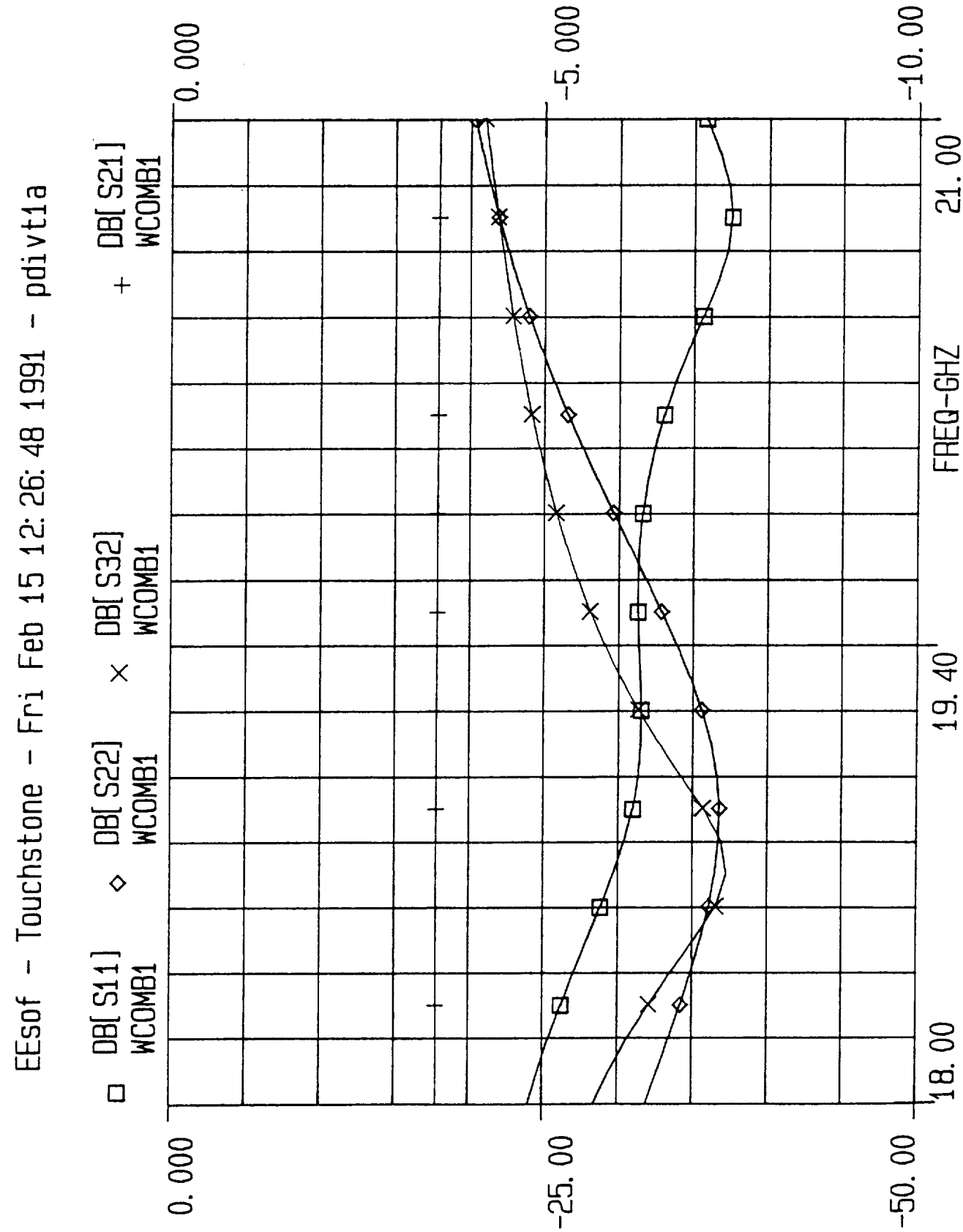

EEsof - Touchstone - Fri Feb 15 12:26:48 1991 - pdivt1a
□ DB[S11] WCOMB1
◇ DB[S22] WCOMB1
× DB[S32] WCOMB1
+ DB[S21] WCOMB1
0.000
-5.000
-10.00
0.000
-25.00
-50.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 8

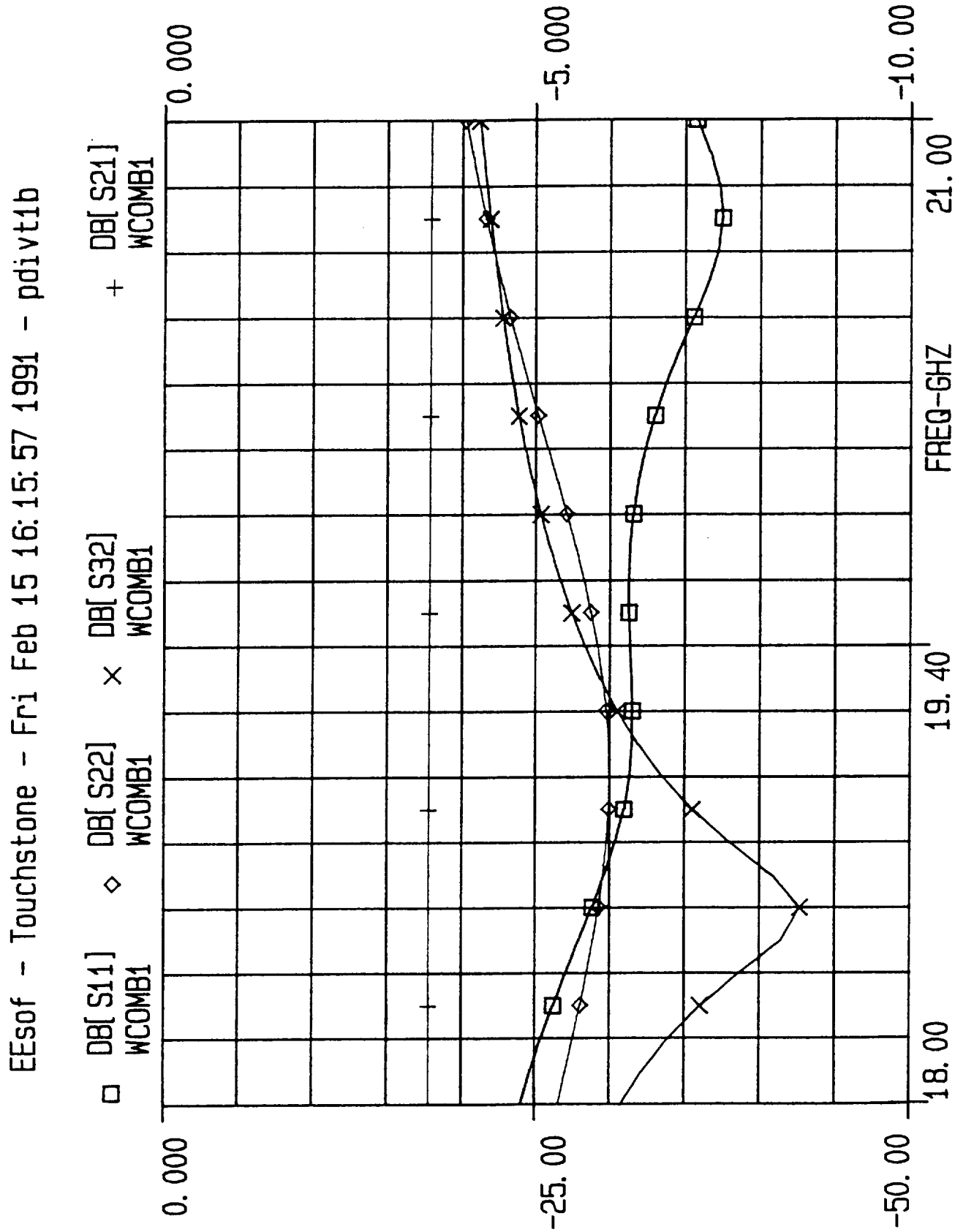

EEsof - Touchstone - Fri Feb 15 16:15:57 1991 - pdivt1b
DB[S11] WCOMB1
DB[S22] WCOMB1
DB[S32] WCOMB1
DB[S21] WCOMB1
0.000
-5.000
-10.00
0.000
-25.00
-50.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 9

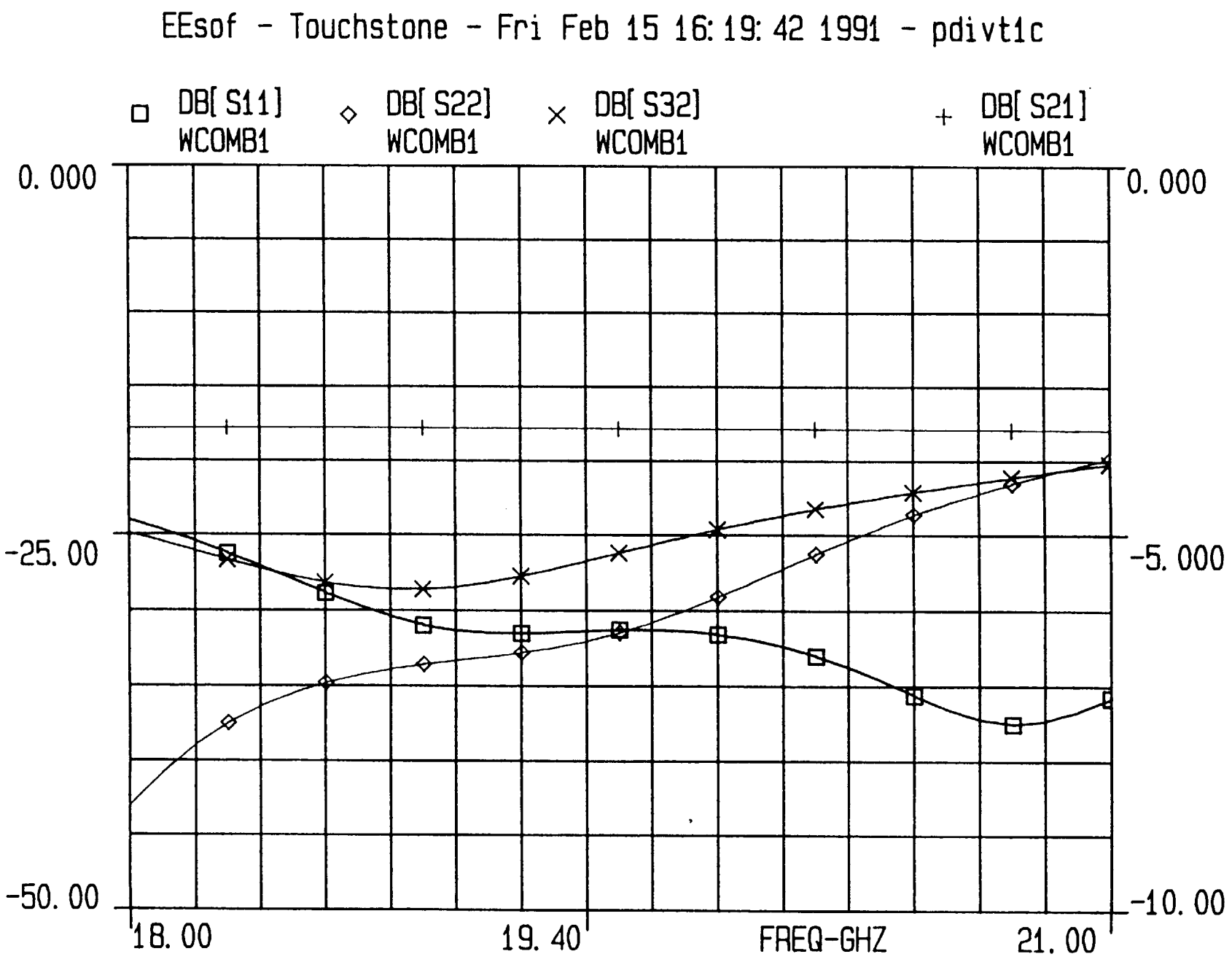

EEsof - Touchstone - Fri Feb 15 16:19:42 1991 - pdivt1c
DB[S11]
WCOMB1
DB[S22]
WCOMB1
DB[S32]
WCOMB1
DB[S21]
WCOMB1
0.000
-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
FREQ-GHZ
21.00

FIGURE 10

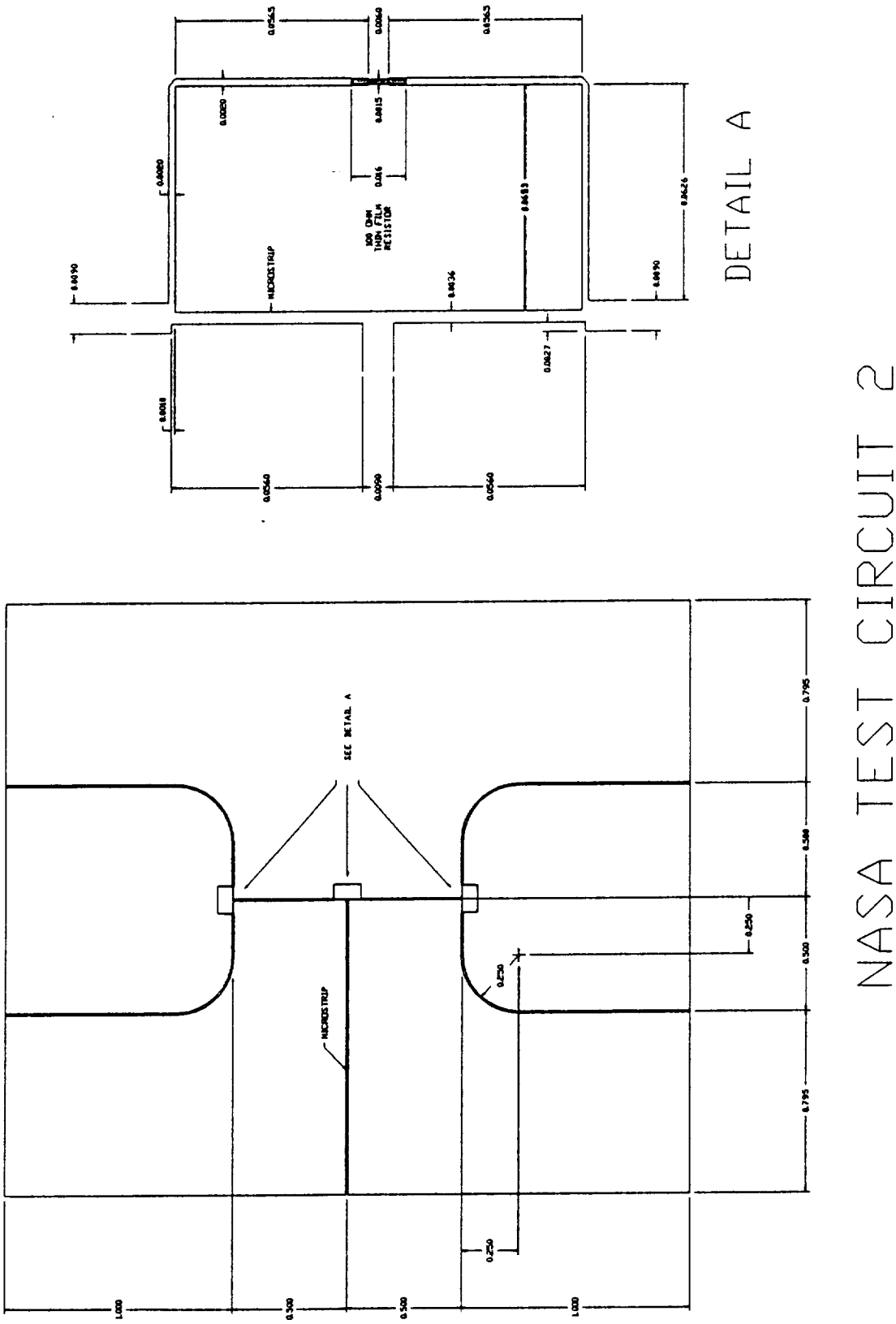


FIGURE 11

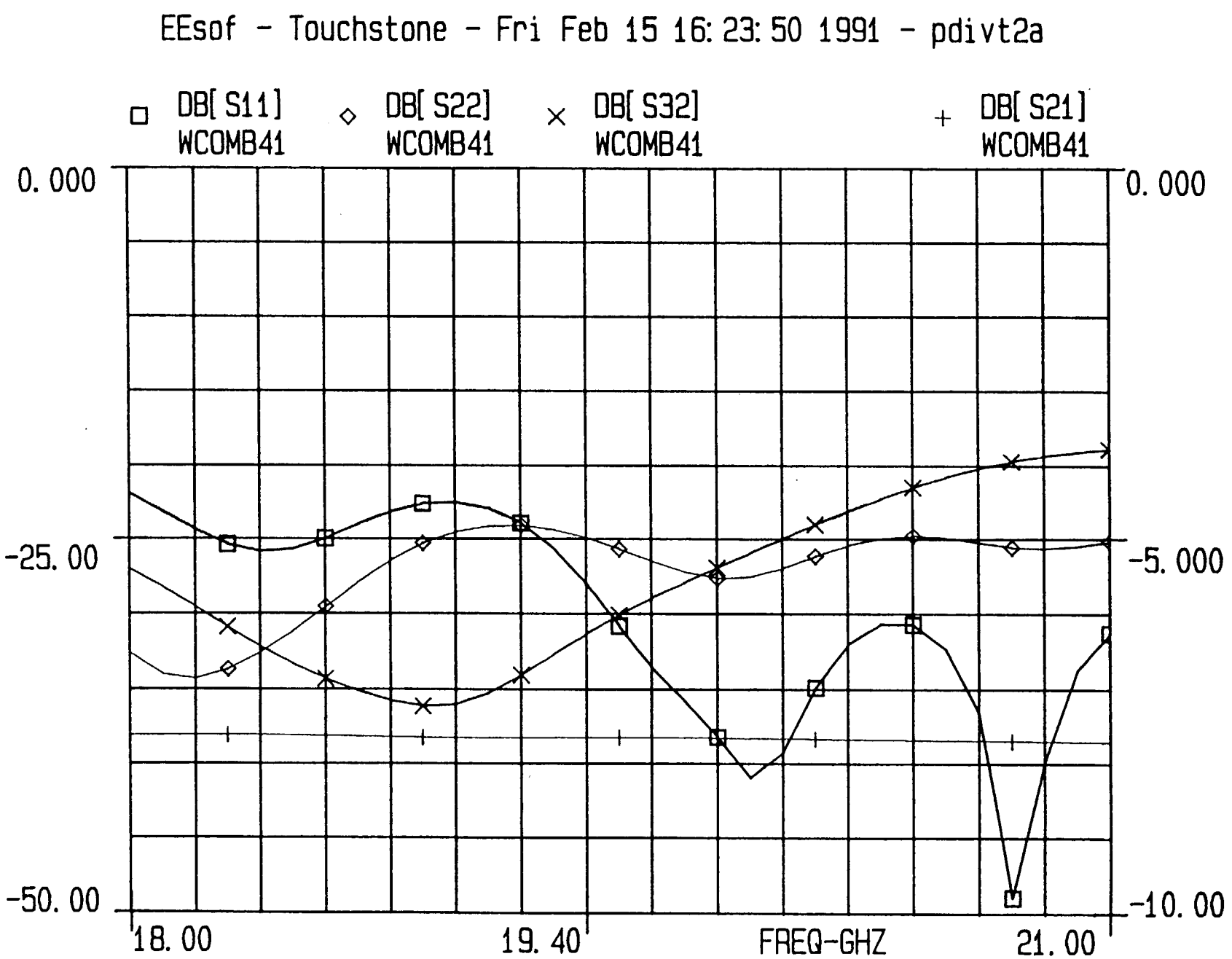

EEsof - Touchstone - Fri Feb 15 16:23:50 1991 - pdivt2a
DB[S11]
WCOMB41
DB[S22]
WCOMB41
DB[S32]
WCOMB41
DB[S21]
WCOMB41
0.000
-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
FREQ-GHZ
21.00

FIGURE 12

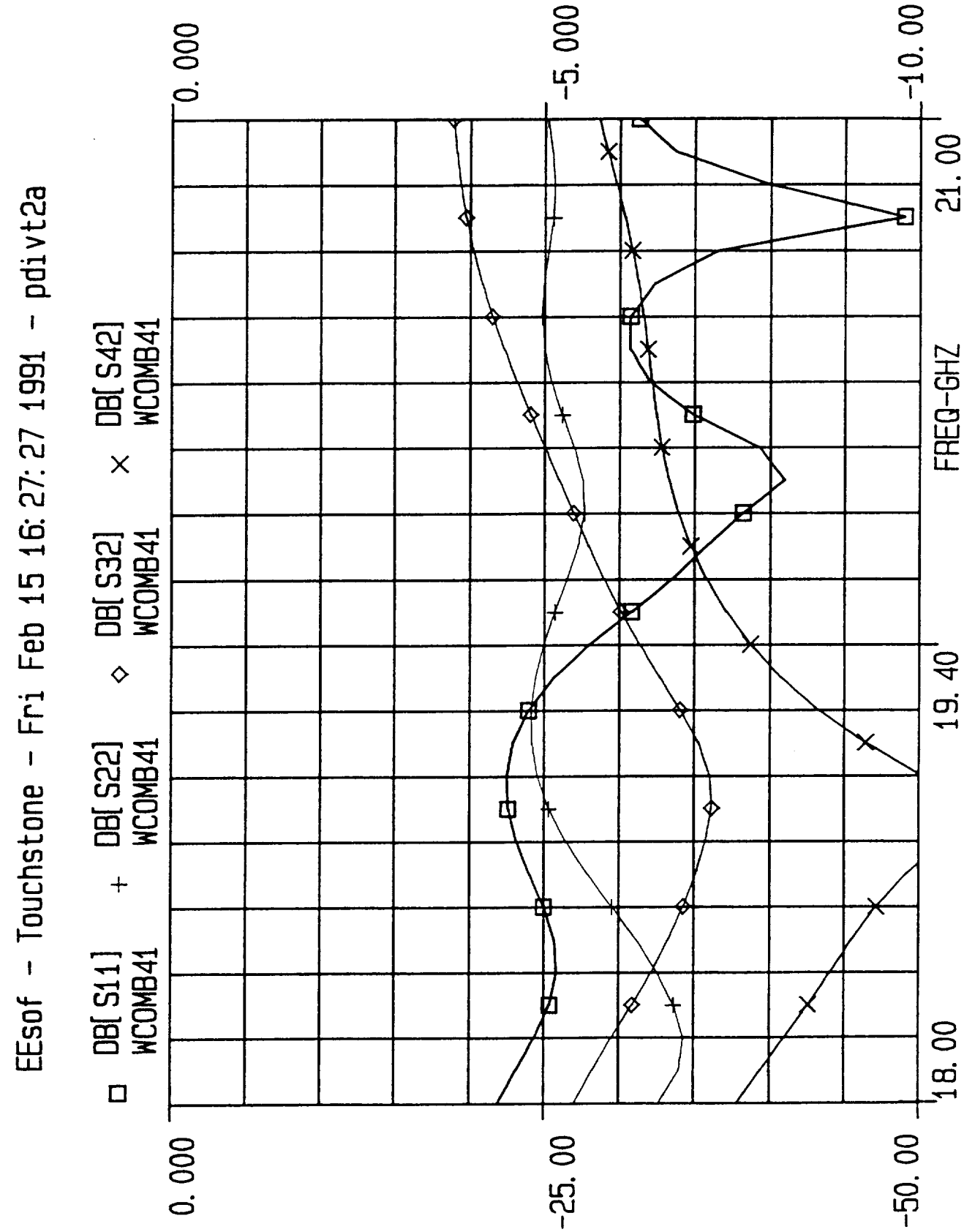

EEsof - Touchstone - Fri Feb 15 16:27:27 1991 - pdivt2a
DB[S11] WCOMB41
DB[S22] WCOMB41
DB[S32] WCOMB41
DB[S42] WCOMB41
0.000
-5.000
-10.00
0.000
-25.00
-50.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 13

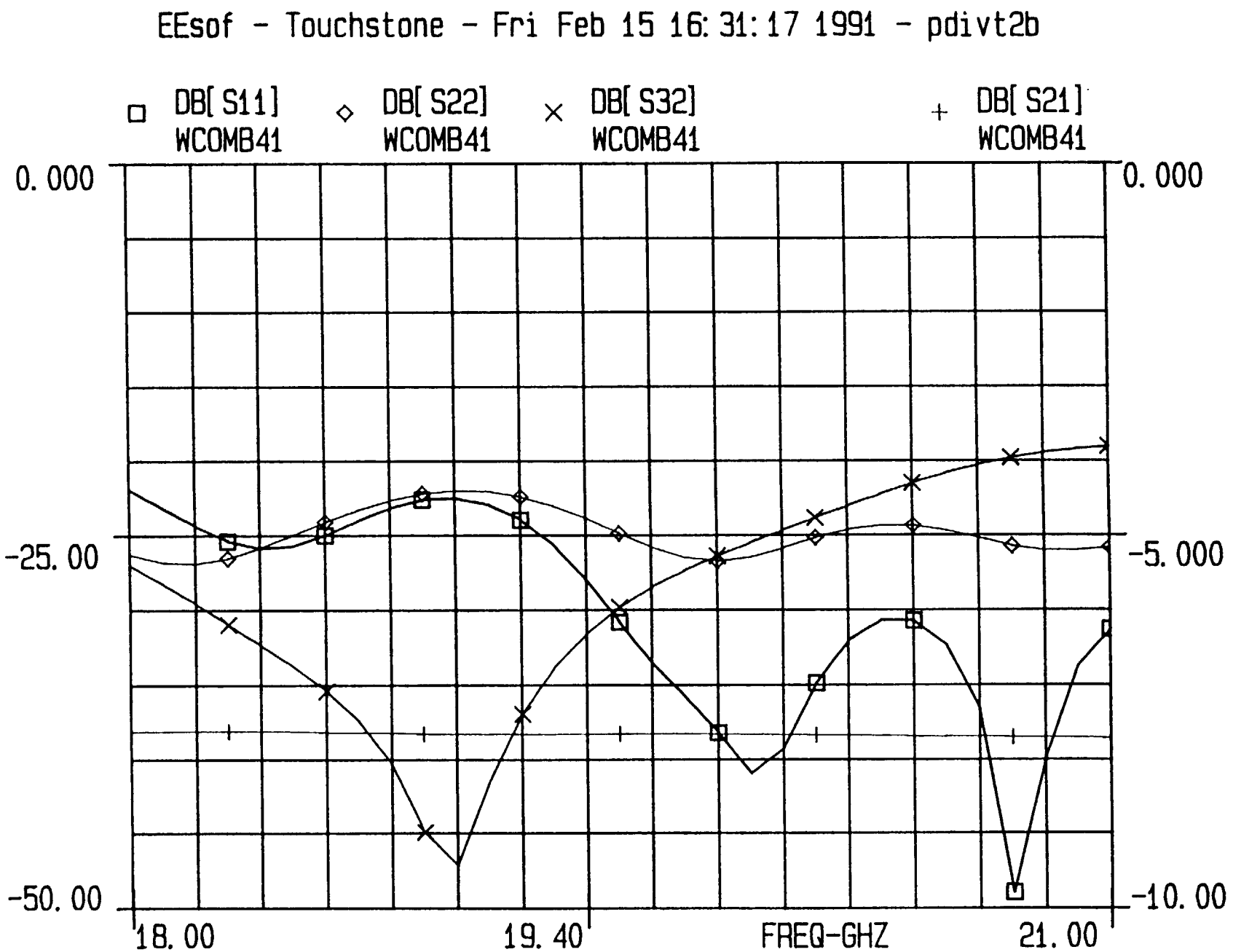

EEsof - Touchstone - Fri Feb 15 16:31:17 1991 - pdivt2b
DB[S11]
WCOMB41
DB[S22]
WCOMB41
DB[S32]
WCOMB41
DB[S21]
WCOMB41
0.000
-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
FREQ-GHZ
21.00

FIGURE 14

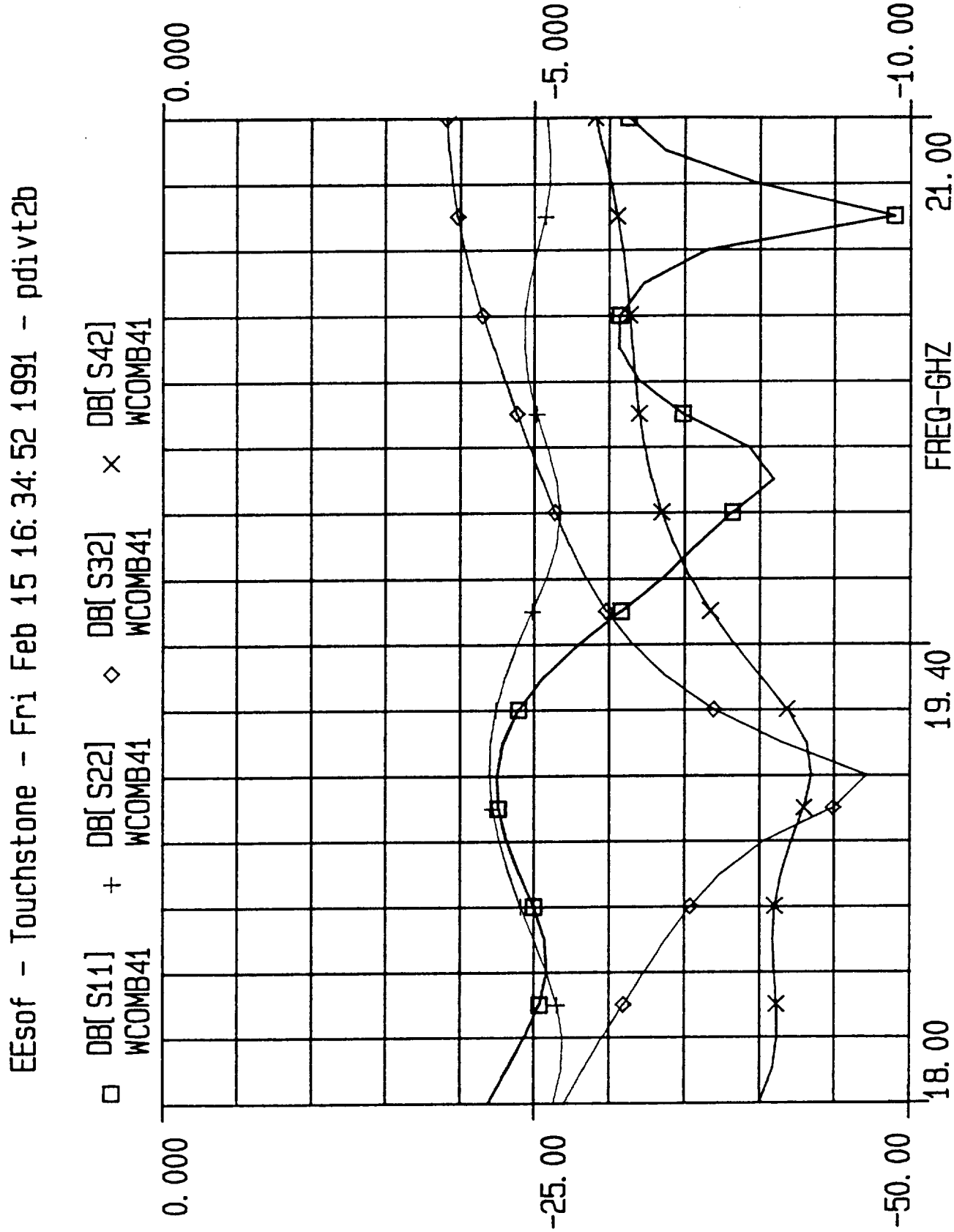

EEsof - Touchstone - Fri Feb 15 16:34:52 1991 - pdivt2b
DB[S11] WCOMB41
DB[S22] WCOMB41
DB[S32] WCOMB41
DB[S42] WCOMB41
0.000
-5.000
-10.00
0.000
-25.00
-50.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 15

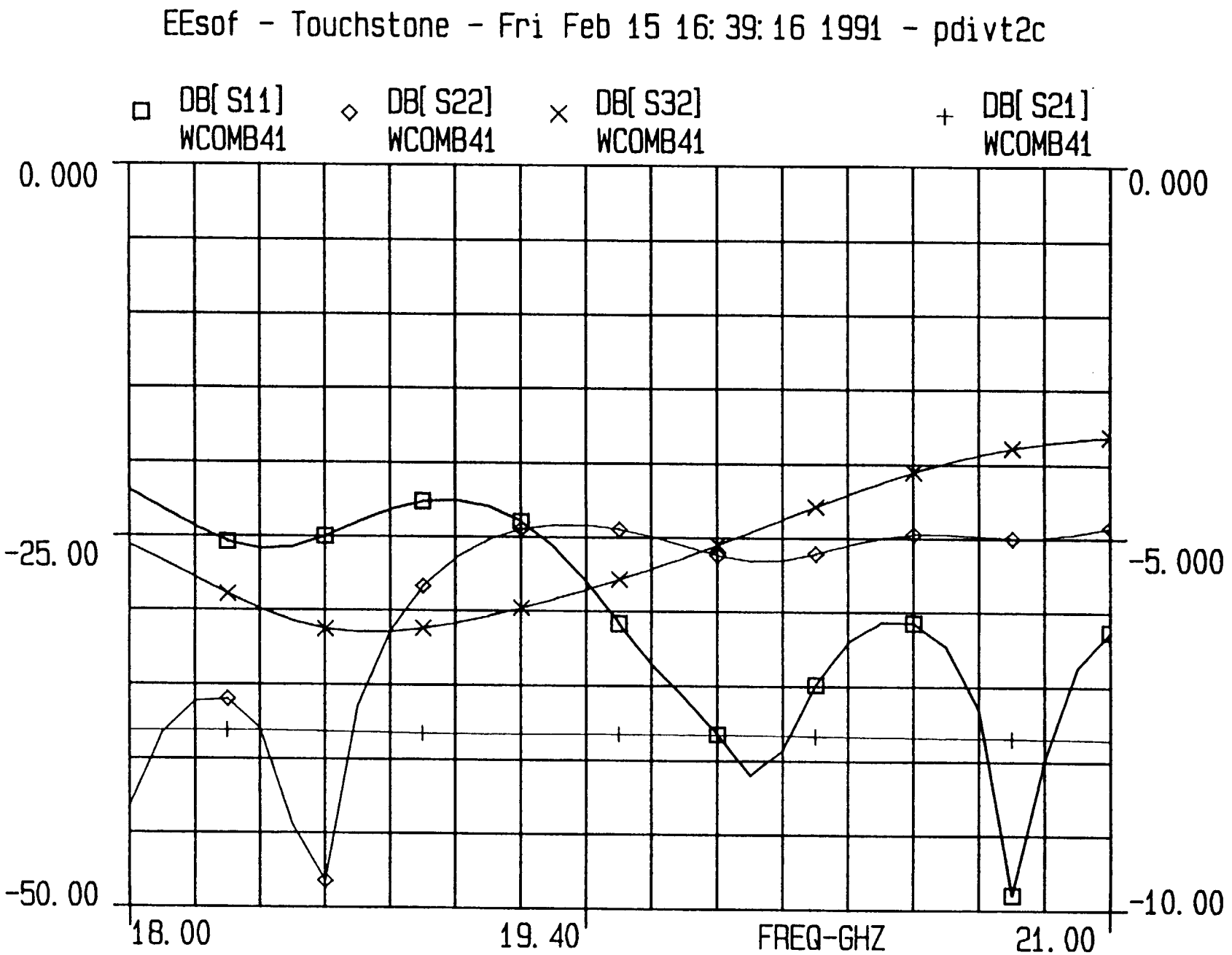

EEsof - Touchstone - Fri Feb 15 16:39:16 1991 - pdivt2c
DB[S11]
WCOMB41
DB[S22]
WCOMB41
DB[S32]
WCOMB41
DB[S21]
WCOMB41
0.000
-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
FREQ-GHZ
21.00

FIGURE 16

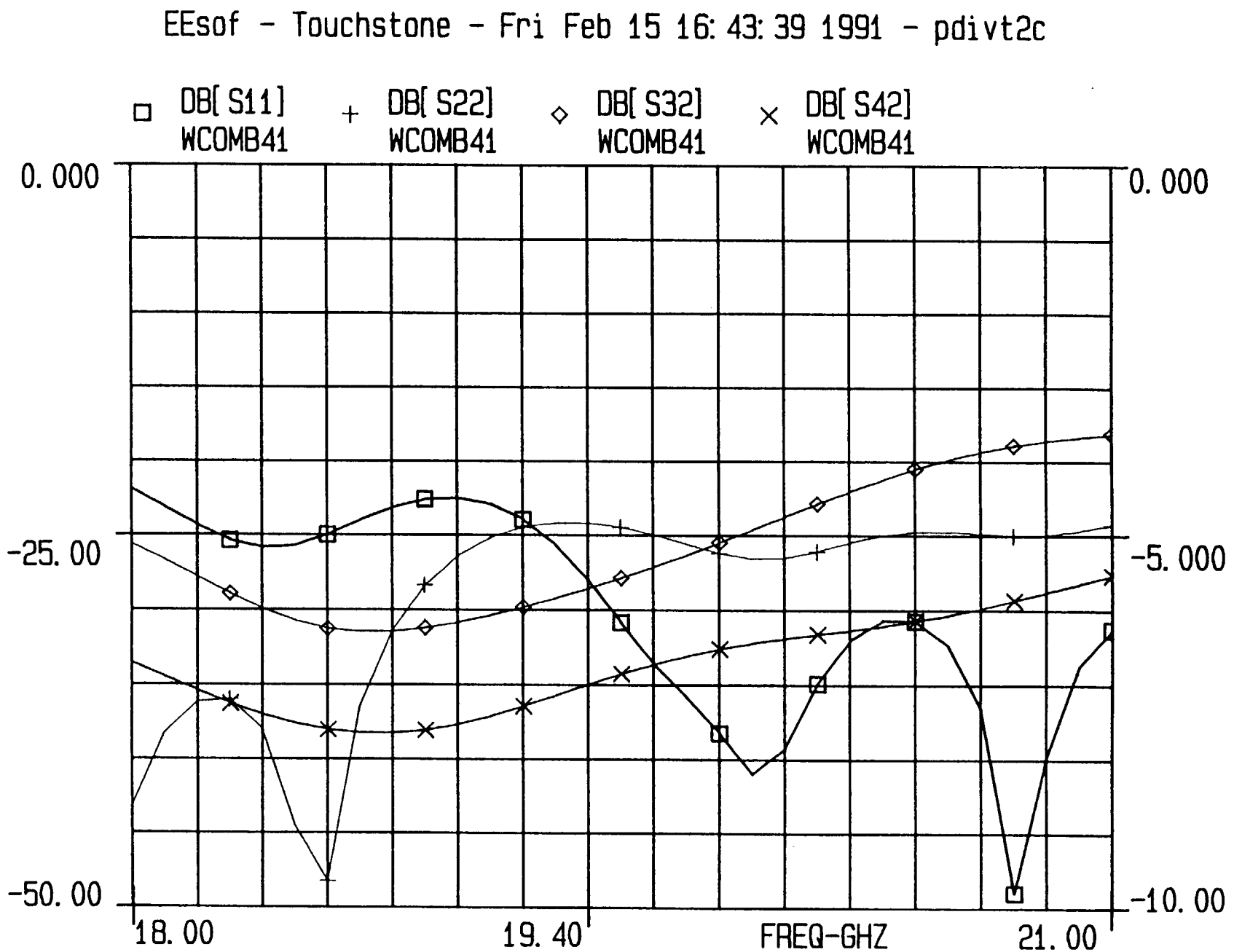
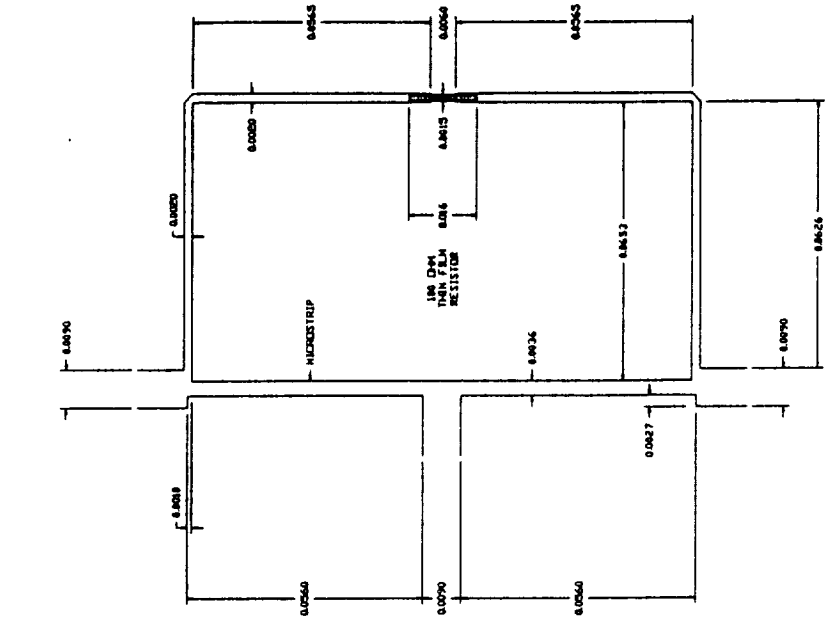

EEsof - Touchstone - Fri Feb 15 16:43:39 1991 - pdivt2c
DB[S11] WCOMB41
DB[S22] WCOMB41
DB[S32] WCOMB41
DB[S42] WCOMB41
0.000
-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 17



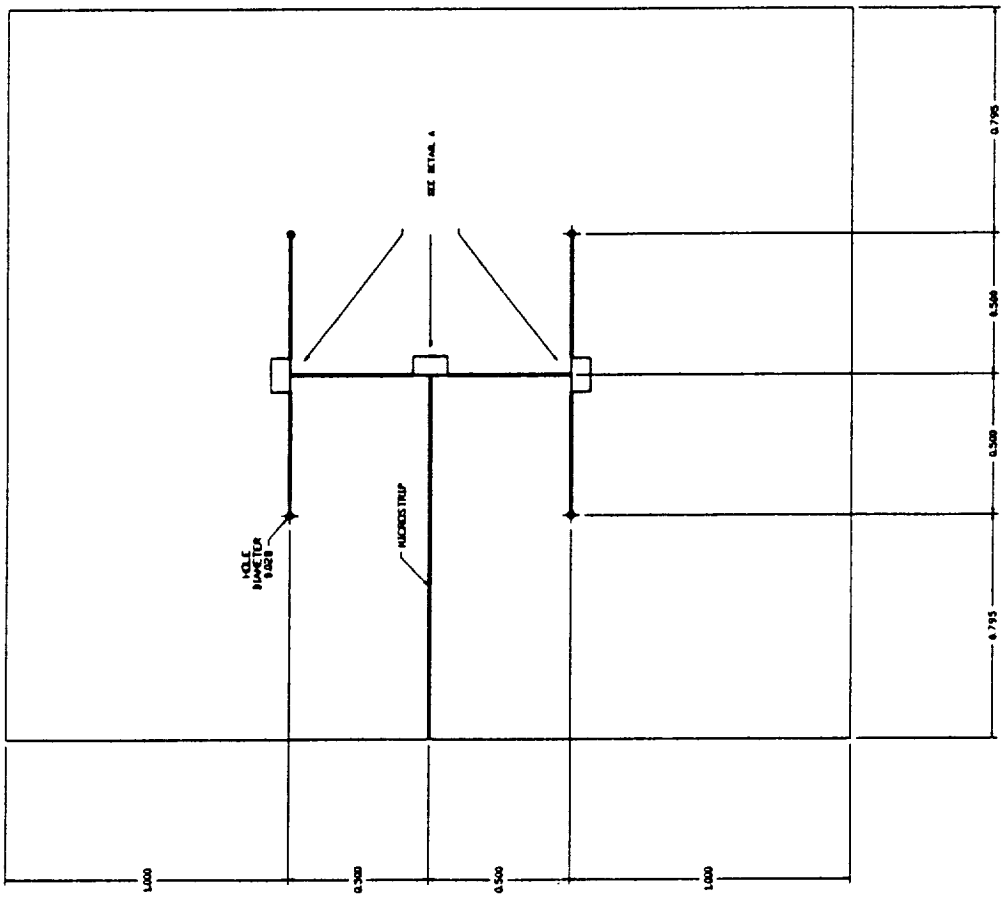


FIGURE 18

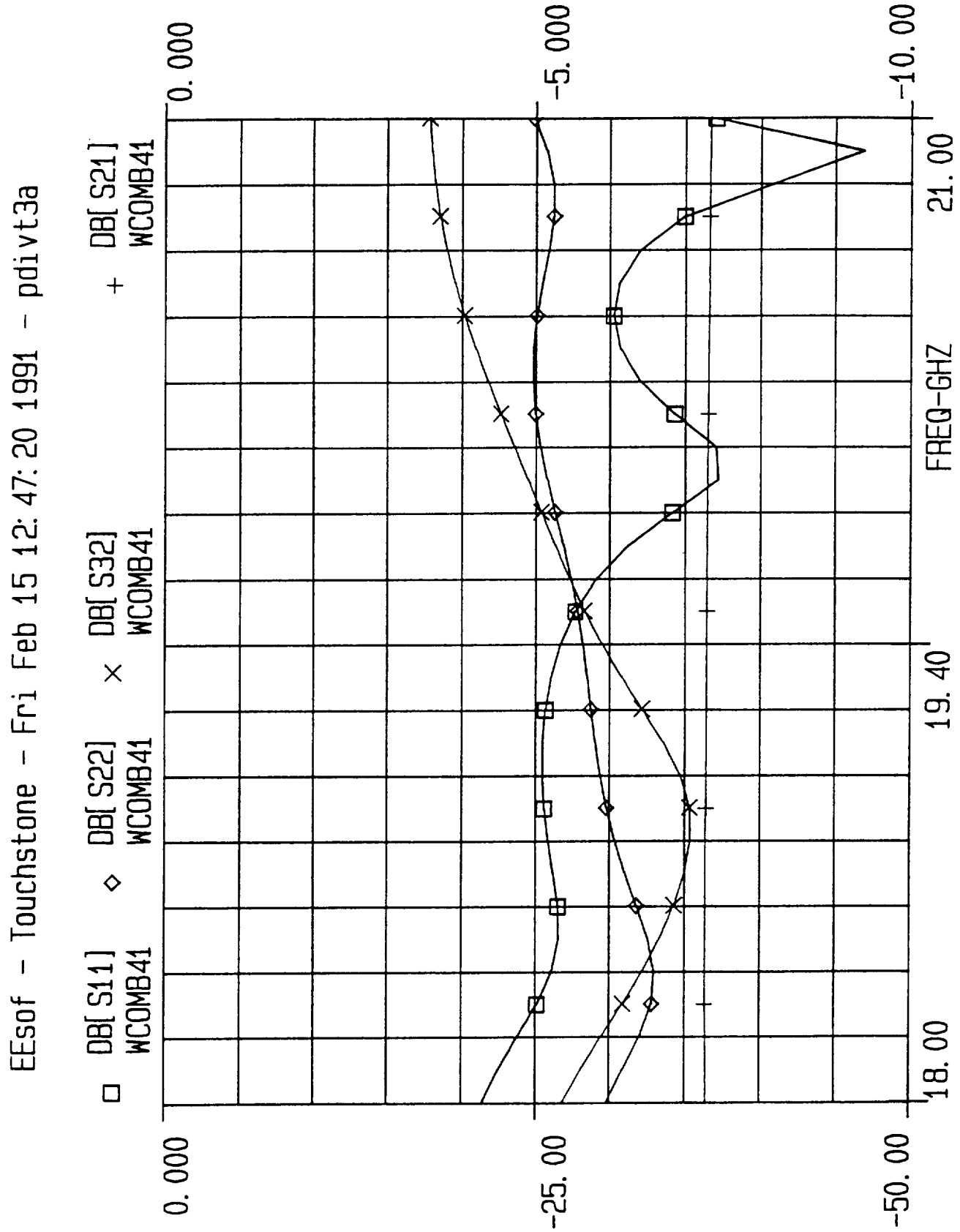

EEsof - Touchstone - Fri Feb 15 12:47:20 1991 - pdivt3a
□ DB[S11] WCOMB41
◇ DB[S22] WCOMB41
× DB[S32] WCOMB41
+ DB[S21] WCOMB41
0.000
-5.000
-10.00
0.000
-25.00
-50.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 19

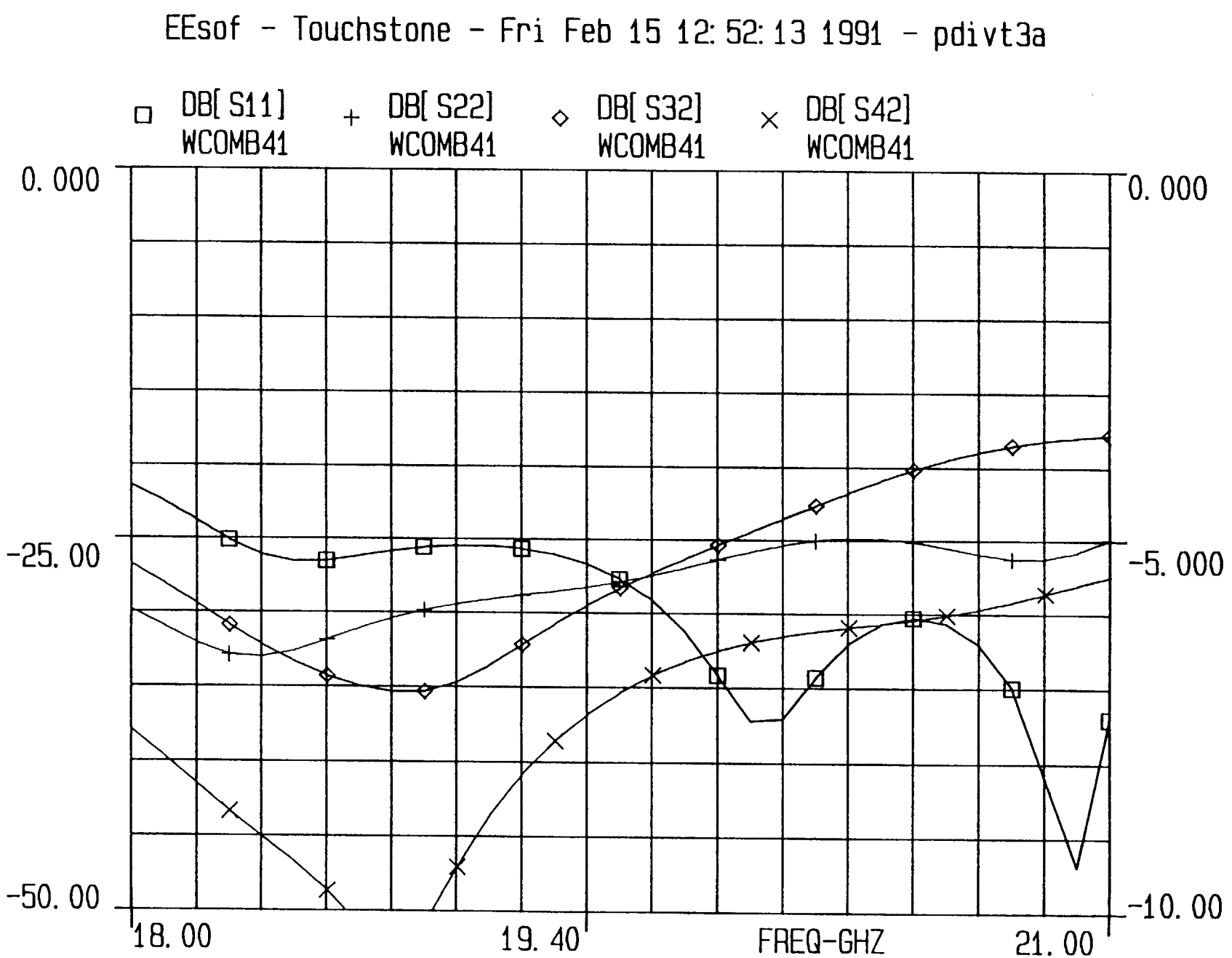

EEsof - Touchstone - Fri Feb 15 12:52:13 1991 - pdivt3a
DB[S11]
WCOMB41
DB[S22]
WCOMB41
DB[S32]
WCOMB41
DB[S42]
WCOMB41
0.000
-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 20

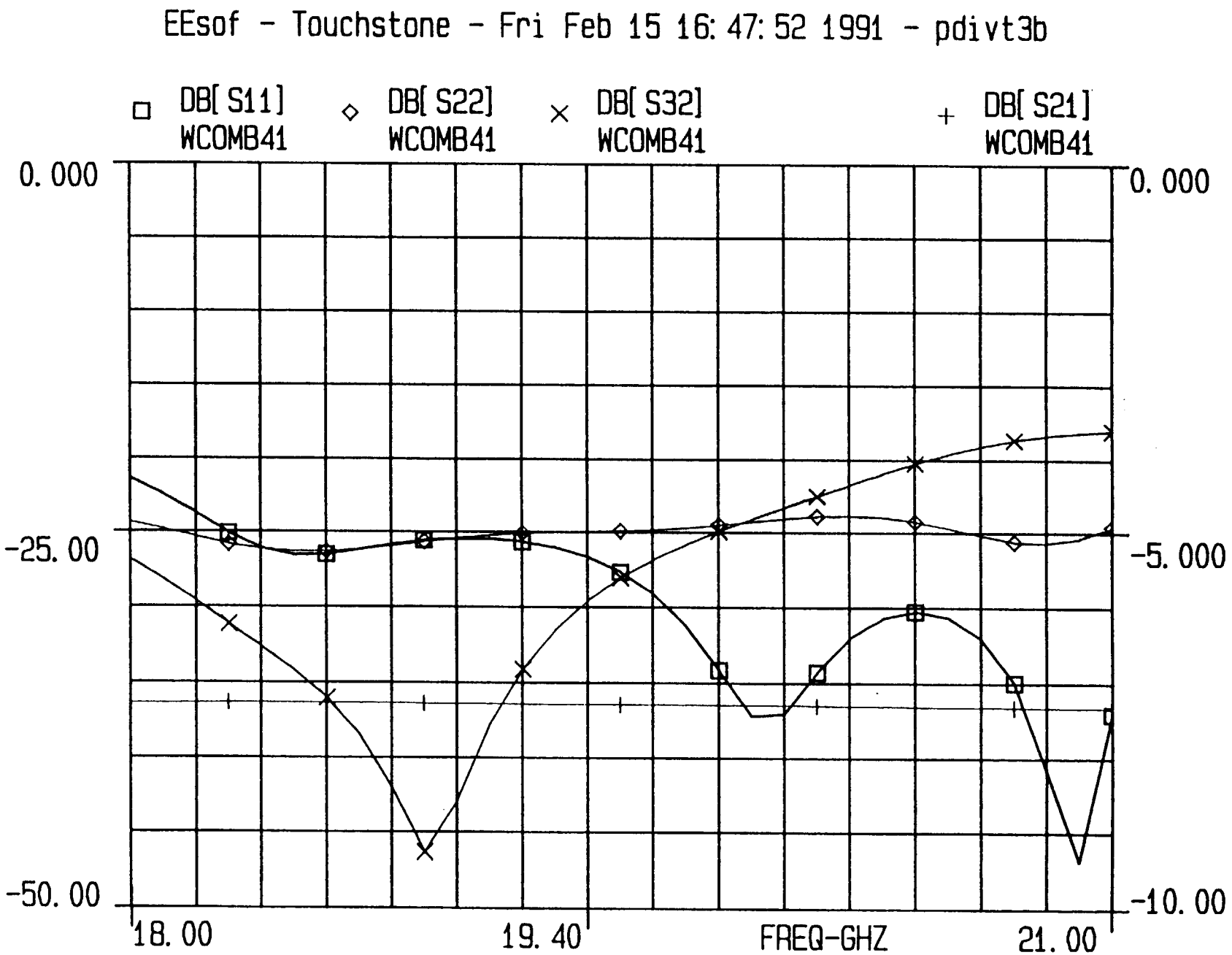

EEsof - Touchstone - Fri Feb 15 16:47:52 1991 - pdivt3b
DB[S11] WCOMB41
DB[S22] WCOMB41
DB[S32] WCOMB41
DB[S21] WCOMB41
0.000
-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 21

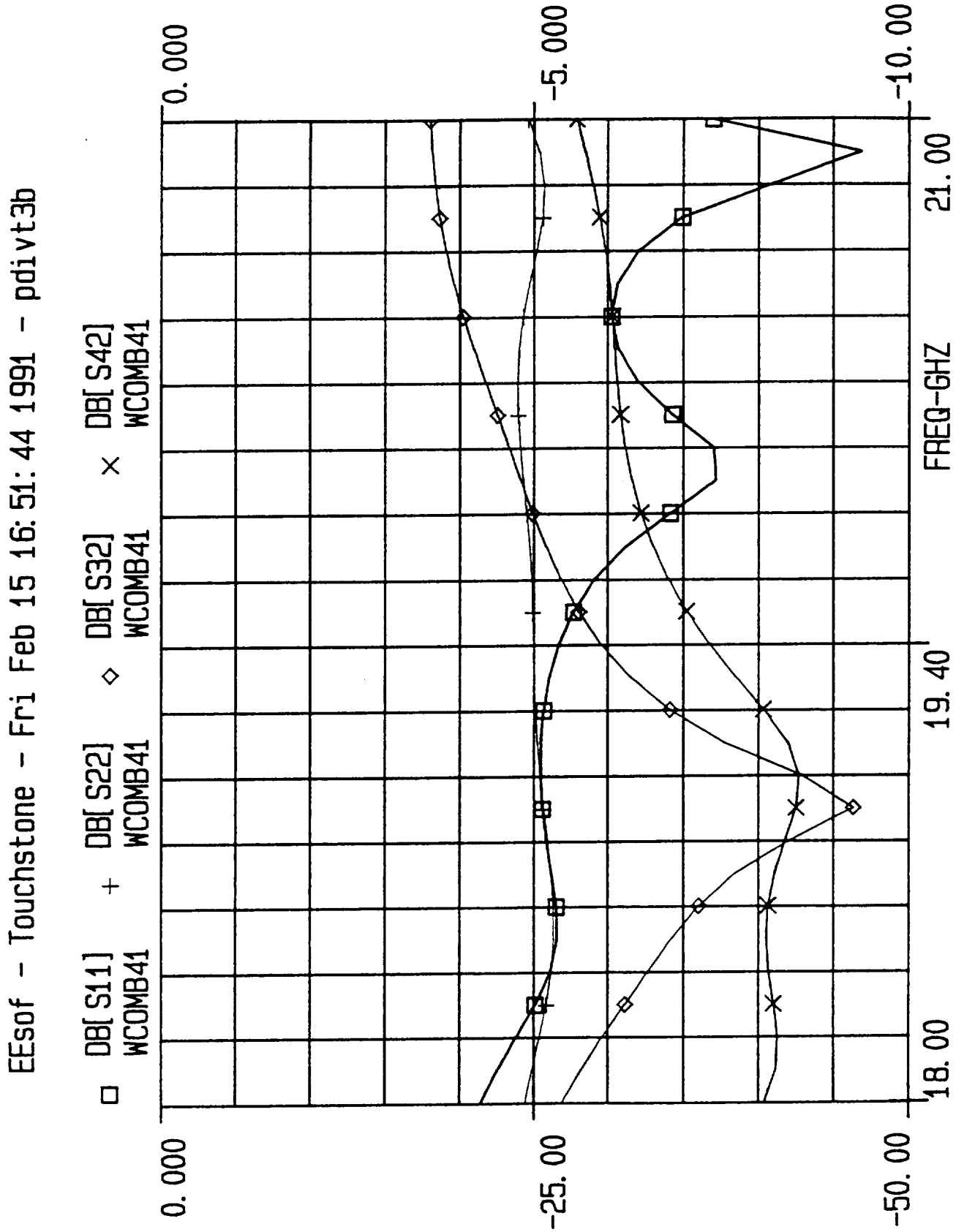

EEsof - Touchstone - Fri Feb 15 16:51:44 1991 - pdivt3b
DB[S11] WCOMB41
DB[S22] WCOMB41
DB[S32] WCOMB41
DB[S42] WCOMB41
0.000
-5.000
-10.00
0.000
-25.00
-50.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 22

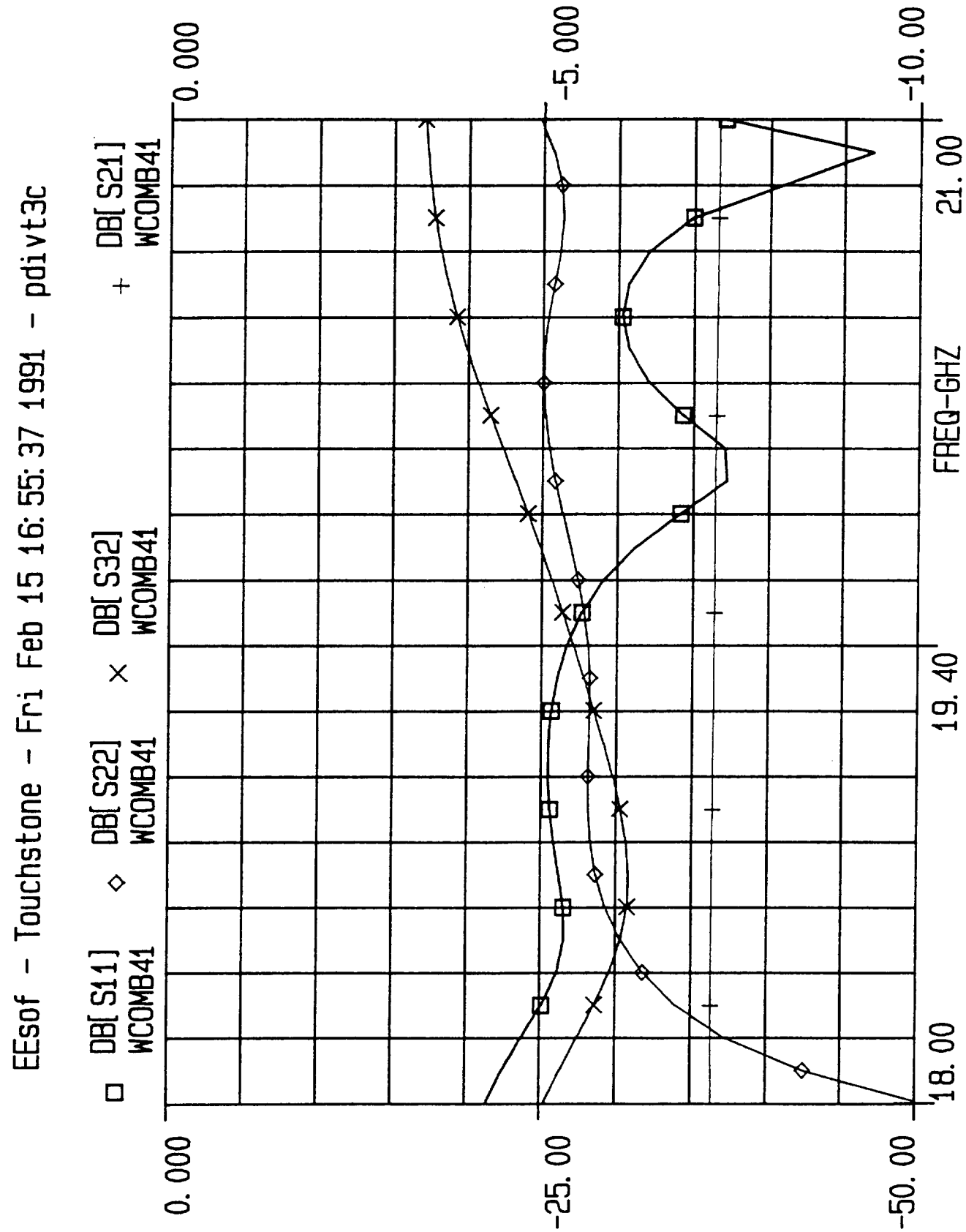

EEsof - Touchstone - Fri Feb 15 16:55:37 1991 - pdivt3c
DB[S11] WCOMB41
DB[S22] WCOMB41
DB[S32] WCOMB41
DB[S21] WCOMB41
0.000
-5.000
-10.00
0.000
-25.00
-50.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 23

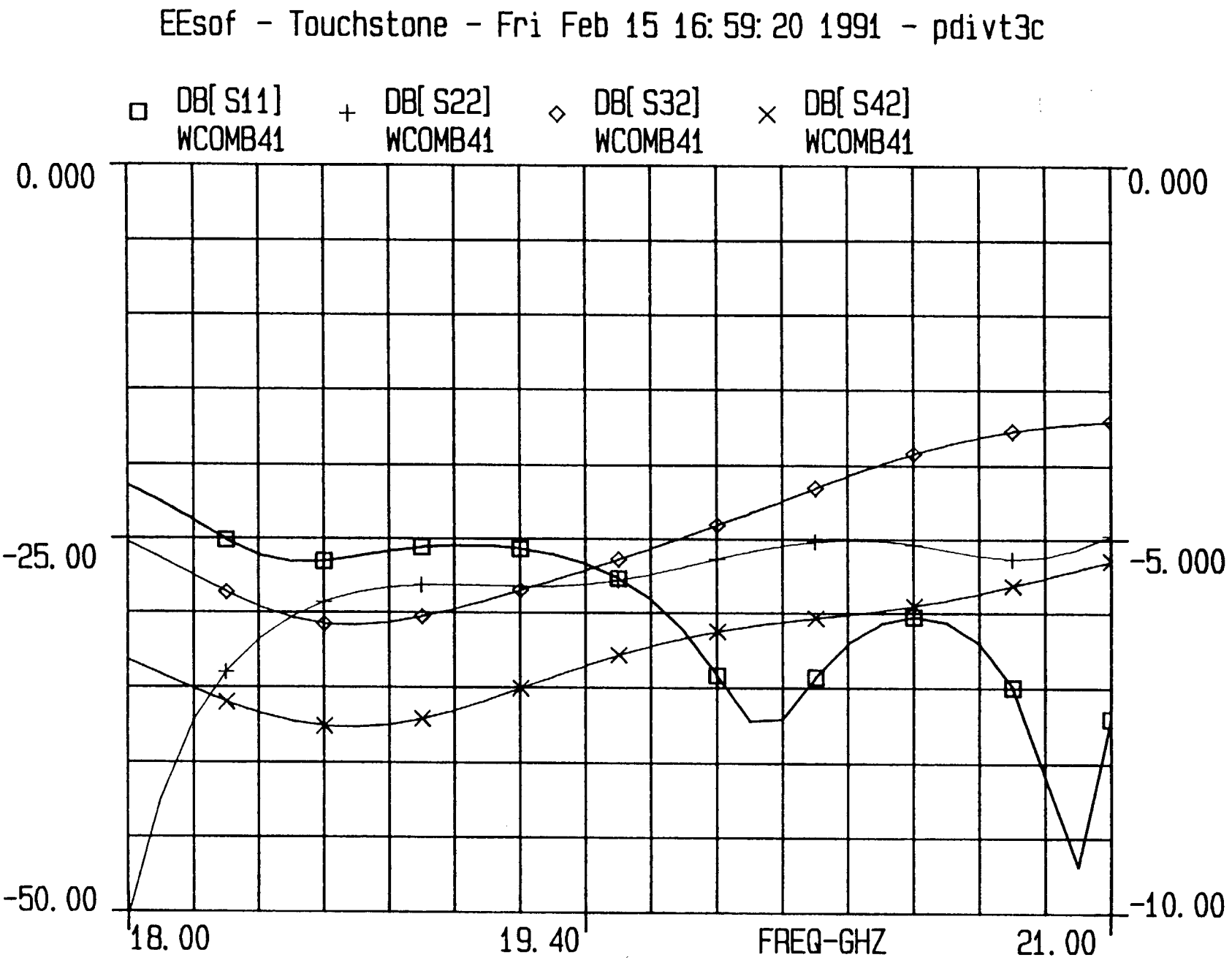

EEsof - Touchstone - Fri Feb 15 16:59:20 1991 - pdivt3c
DB[S11] WCOMB41
DB[S22] WCOMB41
DB[S32] WCOMB41
DB[S42] WCOMB41
0.000
-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
FREQ-GHZ
21.00

FIGURE 24

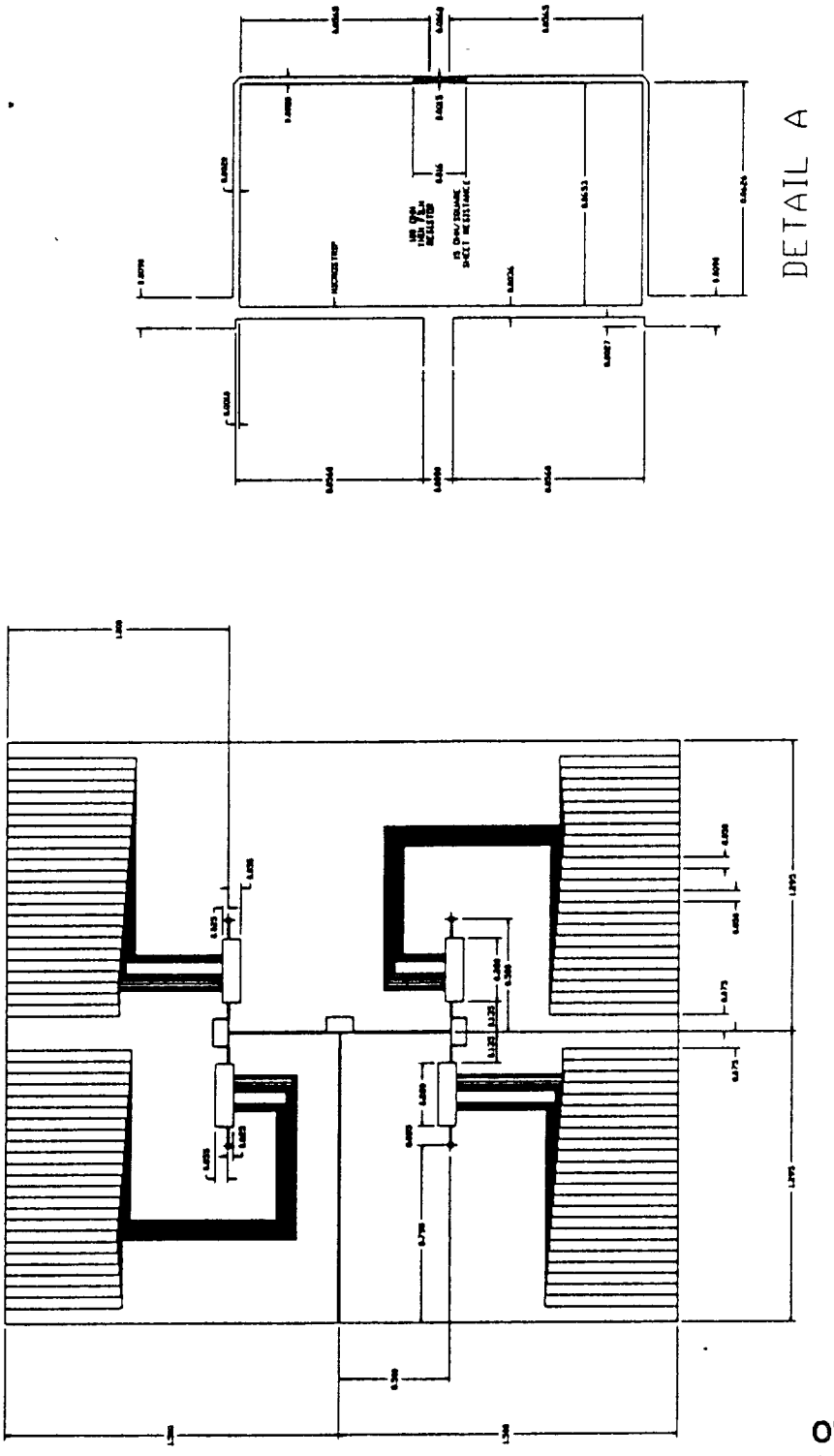


FIGURE 25

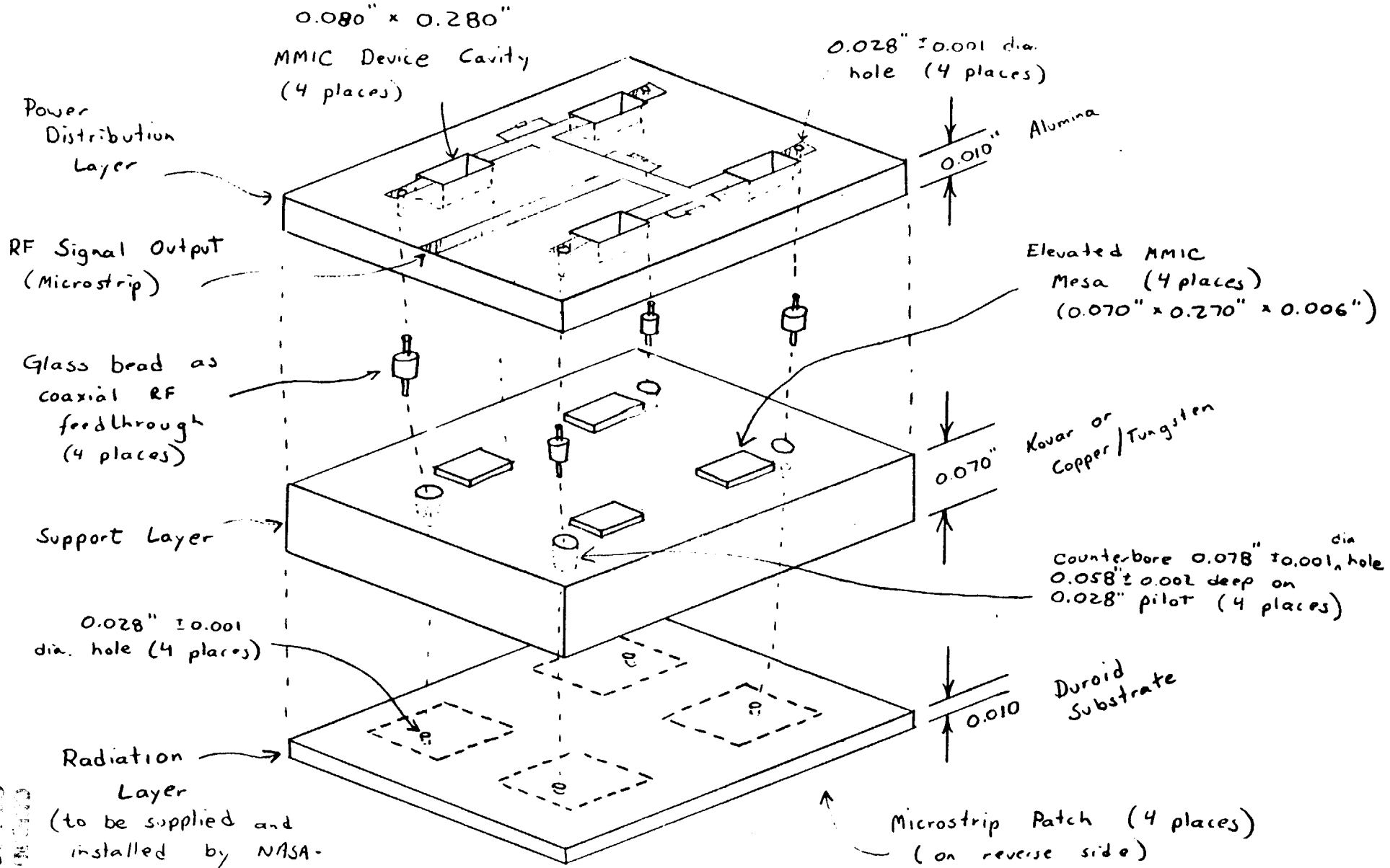


FIGURE 26

NASA/LeRC 20-GHz Receive Element
Assembly Drawing

```
Touchstone Sr. (TM) Ver. 2.100.108.2  Config. (100 20936 5 5100923E 8015 0 4319E)
             pdivt1a.ckt    Fri Feb  8 16:32:13 1991

!
!       File: pdivt1a.ckt
!       Mike Biedenbender 2/8/91
!       description:  Touchstone simulation for Test Circuit 1
!        2:1 Wilkinson power combiner designed for 20 GHz
!        99.6% purity alumina
!        No laser trimming of the thin film isolation resistor
!        Simulation for nominal 25 ohm/square sheet resistance to
!        provide 100 ohm isolation resistor
!
!               !Default Units
dim
  freq ghz
  res oh
  ind nh
  cap pf
  lng mil
  time ps
  cond /oh
  ang deg
!
!               !Define variables for microstrip widths and lengths
!
var
  w50=9.00      !50 ohm transmission line width
  wl4=3.60      !sqrt(2)*50 ohm transmission line width
  wl2r=2.00     !minimum width allowed for half-wave lines to isolation resistor
!
  wltfr1=1.5    !actual width of the thin film isolation resistor
!
  wltfr2=1.5    !nominal width of the thin film isolation resistor
  l14=55        !length of the quarter-wave sqrt(2)*50 ohm trans. line
  l12ra=62.6    !length of the trans. line perpendicular to the thin film res
  rsa=25        !nominal sheet resistance of the thin film resistor
  rsa1=25       !actual sheet resistance of the thin film resistor
!
!               !Define equations to determine additional trans line lengths,
!               !length of thin film resistor
!
eqn
  l12rc=(100*wltfr2)/rsa        !length of the thin film resistor
!
! wltfr1=wltfr2*rsa1/rsa        !determines the length of the thin film
!                               !resistor if laser trimming is used
!
  l12rb=(w50/2) + l14 - ((50*wltfr2)/rsa)       !trans line length to tfr
!
!
ckt
!
!               !Define dielectric and conductor parameters
!
  msub er=9.9 h=10 t=0.06 rho=1 rgh=0
  tand tand=0.0002
```

```
!

Touchstone Sr. (TM) Ver. 2.100.108.2  Config. (100 20936 5 5100923E 8015 0 4319E)
             pdivtla.ckt    Fri Feb  8 16:32:13 1991

!               !Define Test Circuit 1  -  wcomb1
!
  mlin 1 6 w^w50 l=498.2          !trans line from combiner output to edge of
!                                 !Test Circuit 1
  mlin 3 8 w^w50 l=438.5          !trans line from combiner input to edge
  mlin 2 13 w^w50 l=438.5         !trans line from combiner input to edge
  mtee 4 5 6 w1^w14 w2^w14 w3^w50
  mlin 4 7 w^w14 l^l14            !quarter wave trans line
  mlin 5 14 w^w14 l^l14           !quarter wave trans line
  mtee 7 8 9 w1^w14 w2^w50 w3^w12r
  mtee 13 14 15 w1^w50 w2^w14 w3^w12r
  mlin 9 10 w^w12r l^l12ra        !trans line perpendicular to isolation tfr
  mlin 15 16 w^w12r l^l12ra       !trans line perpendicular to isolation tfr
!
  mbend2 10 11 w^w12r
  mbend2 16 17 w^w12r
!
  mlin 11 12 w^w12r l^l12rb       !trans line connected to isolation tfr
  mlin 17 18 w^w12r l^l12rb       !trans line connected to isolation tfr
!
  tfr 12 18 w^wltfr1 l^l12rc rs^rsa1 f=0        !thin film isolation resistor
!
  def3p 1 2 3 wcomb1    !end of definition for Test Circuit 1
!
!               !Specify output parameters to determine
!
out
  wcomb1 db[s11] gr1
  wcomb1 db[s21] gr1a
  wcomb1 db[s22] gr1
  wcomb1 db[s32] gr1
!
!               !Define frequency range for sweeping and optimization
!
freq
  sweep 18 21 0.1
!
!               !Define grids for display
!
grid
  range 18 21 0.2
  gr1 -50 0 5
  gr1a -10 0 1
!
!               !Optimization used to determine quarter-wave transmission line
!               !length and width, length of isolation trans lines
!               !To optimize, w14, l14, and l12ra must be made variable
!               !Example: change l14=55 to l14 # 40 55 80
!
opt
  range 18 21
  wcomb1 db[s22] < -15 1
  wcomb1 db[s32] < -15 1
  wcomb1 db[s12] > -3.2 1
```

```
Touchstone Sr. (TM) Ver. 2.100.108.2  Config. (100 20936 5 5100923E 8015 0 4319E)
             pdivt2a.ckt    Fri Feb 15 15:01:50 1991

!       FILE:PDIVT2A.CKT
!       Mike Biedenbender 2/12/91
!       description:    Touchstone simulation for Test Circuit 2
!        4:1 power combiner for 4 element array without RADC 20 GHz MMICs
!        2:1 Wilkinson power combiner designed for 20 GHz
!        Input microstrip lines extend to edge of substrate to measure
!        characteristics of 4:1 combiner
!        99.6% purity alumina
!        No laser triming of the thin film isolation resistor
!        Simulation for nominal 25 ohm/square sheet resistance to
!        provide 100 ohm isolation resistor
!
!               !Default units
DIM
  FREQ GHZ
  RES OH
  IND NH
  CAP PF
  LNG MIL
  TIME PS
  COND /OH
  ANG DEG
!
!               !Define variables for microstrip widths and lengths
!
VAR
!
  W50=9.00      !50 ohm transmission line width
  WL4=3.60      !sqrt(2)*50 ohm transmission line width
  WL2R=2        !minimum width alowed for half-wave lines to isolation resistor
!
  WLTFR1 #0.1 1.5 3                !WIDTH USED IN ACTUAL RESISTOR
!
  WLTFR2=1.5    !nominal width of the thin film isolation resistor
  LL4=55        !length of the quarter-wave sqrt(2)*50ohm trans line
  LL2RA=62.6    !length of the trans line perpendicular to the thin film res
  RSA=25        !nominal sheet resistance of the thin film resistor
  RSA1=25       !actual sheet resistance of the thin film resistor
!
!               !Define equations to determine additional trans line lengths,
!               !length of thin film resistor
!
EQN
  LL2RC=(100*WLTFR2)/RSA        !length of the thin filmn resistor
!
! WLTFR1=WLTFR2*RSA1/RSA        !determines the width of the thin film
!                               !resistor if laser trimming is used
!
  LL2RB=(W50/2) + LL4 - ((50*WLTFR2)/RSA)       !trans line length to tfr
!
!
CKT
!
!               !Define dielectric and conductor parameters
```

```
  MSUB ER=9.9 H=10 T=0.1 RHO=1 RGH=0


Touchstone Sr. (TM) Ver. 2.100.108.2  Config. (100 20936 5 5100923E 8015 0 4319E)
            pdivt2a.ckt    Fri Feb 15 15:01:50 1991

  TAND TAND=0.0002
!
!               !Define Test Circuit 2  -  wcomb
!
  MTEE 4 5 1 W1^WL4 W2^WL4 W3^W50
  MLIN 4 7 W^WL4 L^LL4          !quarter wave trans line
  MLIN 5 14 W^WL4 L^LL4         !quarter wave trans line
  MTEE 7 3 9 W1^WL4 W2^W50 W3^WL2R
  MTEE 2 14 15 W1^W50 W2^WL4 W3^WL2R
  MLIN 9 10 W^WL2R L^LL2RA      !trans line perpendicular to isolation tfr
  MLIN 15 16 W^WL2R L^LL2RA     !trans line perpendicular to isolation tfr
!
  MBEND2 10 11 W^WL2R
  MBEND2 16 17 W^WL2R
!
  MLIN 11 12 W^WL2R L^LL2RB     !trans line connected to isolation tfr
  MLIN 17 18 W^WL2R L^LL2RB     !trans line connected to isolation tfr
!
  TFR 12 18 W^WLTFR1 L^LL2RC RS^RSA1 F=0        !thin film isolation resistor
!
  DEF3P 1 2 3 WCOMB             !End of definition for Wilkinson power combiner
!
!
  MLIN 100 110 W^W50 L=1293.8   !Trans line from output combiner output to
!                               !edge of Test Circuit 2
  WCOMB 110 111 112             !Output 2:1 power combiner
  MLIN 111 120 W^W50 L=436.7    !Trans line from output combiner input to
!                               !input combiner output
  MLIN 112 130 W^W50 L=436.7    !Trans line from output combiner input to
!                               !input combiner output
  WCOMB 120 121 125             !Input 2:1 power combiner
  WCOMB 130 131 135             !Input 2:1 power combiner
!
  MLIN 121 122 W^W50 L=188.5            !Trans lines and curve from
  MCURVE 122 123 W^W50 ANG=90 RAD=250   !input power combiner to edge of
  MLIN 123 101 W^W50 L=750              !Test Circuit 2
!
  MLIN 125 126 W^W50 L=188.5            !Trans lines and curve from
  MCURVE 126 127 W^W50 ANG=-90 RAD=250  !input power combiner to edge of
  MLIN 127 102 W^W50 L=750              !Test Circuit 2
!
  MLIN 131 132 W^W50 L=188.5            !Trans lines and curve from
  MCURVE 132 133 W^W50 ANG=90 RAD=250   !input power combiner to edge of
  MLIN 133 103 W^W50 L=750              !Test Circuit 2
!
  MLIN 135 136 W^W50 L=188.5            !Trans lines and curve from
  MCURVE 136 137 W^W50 ANG=-90 RAD=250  !input power combiner to edge of
  MLIN 137 104 W^W50 L=750              !Test Circuit 2
!
  DEF5P 100 101 102 103 104 WCOMB41A    !Define 5 port combiner
!                                       !End of definition for Test Circuit 2
!
  WCOMB41A 200 201 202 203 204  !Retrieve 5 port combiner
  RES 204 0 R=50                !Terminate a port to make 4 port network
```

```
!                                !to allow Touchstone output calculation


Touchstone Sr. (TM) Ver. 2.100.108.2  Config. (100 20936 5 5100923E 8015 0 4319E)
             pdivt2a.ckt    Fri Feb 15 15:01:50 1991

  DEF4P 200 201 202 203 WCOMB41 !Define 4 port from 4-way combiner
!
!              !Specify output parameters to determine
!
OUT
  WCOMB41 DB[S11] GR1            !Return loss at output combiner output
  WCOMB41 DB[S21] GR1A           !Insertion loss thru 2 Wilkinson combiners
  WCOMB41 DB[S22] GR1            !Return loss at any input port
  WCOMB41 DB[S32] GR1            !Isolation between inputs of same input combiner
  WCOMB41 DB[S42] GR1            !Isolation between inputs of different input
!                                !combiners
!
!               !Define frequency range for sweeping and optimization
!
FREQ
  SWEEP  18 21 0.1               !Center frequency of design is 19.7 GHz
!
!               !Define grids for display
GRID
  RANGE 18 21 0.2
  GR1 -50 0 5
  GR1A -10 0 1
!
OPT
!
!               !Optimization used to determine quarter-wave transmission line
!               !length and width, length of isolation trans lines
!               !To optimize, WL4, LL4, AND LL2RA must be made variable
!               !Example:  change LL4=55 to LL4 # 40 55 80
!
  RANGE 18 21
  WCOMB41 DB[S22] < -15 1
  WCOMB41 DB[S32] < -15 1
  WCOMB41 DB[S11] < -15 1
  WCOMB41 DB[S12] > -6.5 1
```

```
Touchstone Sr. (TM) Ver. 2.100.108.2  Config. (100 20936 5 5100923E 8015 0 4319E)
             pdivt3a.ckt    Tue Feb 12 14:33:01 1991

!       FILE:PDIVT3A.CKT
!       Mike Biedenbender 2/12/91
!       description:    Touchstone simulation for Test Circuit 3
!        4:1 power combiner for 4 element array without RADC 20 GHz
!        MMICs with microstip in place of MMICs up to antenna feedthroughs
!        2:1 Wilkinson power combiner designed for 20 GHz
!        99.6% purity alumina
!        No laser trimming of the thin film isolation resistor
!        Simulation for nominal 25 ohm/square sheet resistance to
!        provide 100 ohm isolation resistor
!
!               !Default Units
DIM
  FREQ GHZ
  RES OH
  IND NH
  CAP PF
  LNG MIL
  TIME PS
  COND /OH
  ANG DEG
!
!               !Define variables for microstrip widths and lengths
!
VAR
  W50=9.00      !50 ohm transmission line width
  WL4=3.60      !sqrt(2)*50 ohm transmission line width
  WL2R=2        !minimum width allowed for half-wave lines to isolation resistor
!
  WLTFR1=1.5    !Actual width of the thin film isolation resistor
!

  WLTFR2=1.5    !nominal width of the thin film isolation resistor
  LL4=55        !length of the qurater-wave sqrt(2)*50 ohm trans. line
  LL2RA=62.6    !length of the trans.line perpendicular to the thin film res
  RSA=25        !nominal sheet resistance of the thin film resistor
  RSA1=25       !actual sheet resistance of the thin film resistor
!
!               !Define equations to determine additional trans line lengths,
!               !length of thin film resistor
!
EQN
  LL2RC=(100*WLTFR2)/RSA        !length of the thin film resistor
!
! WLTFR1=WLTFR2*RSA1/RSA        !determines the length of the thin film
!                               !resistor if laser trimming is used
!
  LL2RB=(W50/2) + LL4 - ((50*WLTFR2)/RSA)       !trans line length to tfr
!
!
CKT
!
!               !Define dielectric and conductor parameters
  MSUB ER=9.9 H=10 T=0.06 RHO=1 RGH=0
```

```
  TAND TAND=0.0002


Touchstone Sr. (TM) Ver. 2.100.108.2  Config. (100 20936 5 5100923E 8015 0 4319E)
            pdivt3a.ckt    Tue Feb 12 14:33:01 1991

!
!               !Define Test Circuit 3  - wcomb
!
  MTEE 4 5 1 W1^WL4 W2^WL4 W3^W50
  MLIN 4 7 W^WL4 L^LL4          !quarter wave trans line
  MLIN 5 14 W^WL4 L^LL4         !quarter wave trans line
  MTEE 7 3 9 W1^WL4 W2^W50 W3^WL2R
  MTEE 2 14 15 W1^W50 W2^WL4 W3^WL2R
  MLIN 9 10 W^WL2R L^LL2RA      !trans line perpendicular to isolation tfr
  MLIN 15 16 W^WL2R L^LL2RA     !trans line perpendicular to isolation tfr
!
  MBEND2 10 11 W^WL2R
  MBEND2 16 17 W^WL2R
!
  MLIN 11 12 W^WL2R L^LL2RB     !trans line connected to isolation tfr
  MLIN 17 18 W^WL2R L^LL2RB     !trans line connected to isolation tfr
!
  TFR 12 18 W^WLTFR1 L^LL2RC RS^RSA1 F=0        !thin film isolation resistor
!
  DEF3P 1 2 3 WCOMB             !End of definition for Wilkinson power combiner
!
!
  MLIN 100 110 W^W50 L=1293.2   !Trans line from output combiner output to
!                               !edge of Test Circuit 3
  WCOMB 110 111 112             !Output 2:1 power combiner
  MLIN 111 120 W^W50 L=436.7    !Trans line from output combiner input to
!                               !input combiner output
  MLIN 112 130 W^W50 L=436.7    !Trans line from output combiner input to
!                               !input combiner output
  WCOMB 120 121 122             !Input 2:1 power combiner
  WCOMB 130 131 132             !Input 2:1 power combiner
  MLIN 121 101 W^W50 L=438.5    !Trans line from input power combiner to
!                               !edge of Test Circuit 3
  MLIN 122 102 W^W50 L=438.5    !Trans line from input power combiner to
!                               !edge of Test Circuit 3
  MLIN 131 103 W^W50 L=438.5    !Trans line from input power combiner to
!                               !edge of Test Circuit 3
  MLIN 132 104 W^W50 L=438.5    !Trans line from input power combiner to
!                               !edge of Test Circuit 3
  DEF5P 100 101 102 103 104 WCOMB41A    !Define 5 port combiner
!                                       !End of definition for Test Circuit 3
!
  WCOMB41A 200 201 202 203 204  !Retrieve 5 port combiner
  RES 204 0 R=50                !Terminate a port to make 4 port network
!                               !to allow Touchstone output calculation
  DEF4P 200 201 202 203 WCOMB41 !Define 4 port from 4-way combiner
!
!               !Specify output parameters to determine
!
OUT
  WCOMB41 DB[S11] GR1           !Return loss at output combiner output
  WCOMB41 DB[S21] GR1A          !Insertion loss thru 2 Wilkinson combiners
  WCOMB41 DB[S22] GR1           !Return loss at any input port
  WCOMB41 DB[S32] GR1           !Isolation between inputs of same input combiner
```

```
  WCOMB41 DB[S42] GR1           !Isolation between inputs of different input


Touchstone Sr. (TM) Ver. 2.100.108.2  Config. (100 20936 5 5100923E 8015 0 4319E)
             pdivt3a.ckt     Tue Feb 12 14:33:01 1991

!                               !combiners
!
!               !Define frequency range for sweeping and optimization
!
FREQ
  SWEEP 18 21 0.1               !Center Freq of design is 19.7 GHz
!
!               !Define grids for display
!
GRID
  RANGE 18 21 0.2
  GR1 -50 0 5
  GR1A -10 0 1
!
!               !Optimization used to determine quarter-wave transmission line
!               !length and width, length of isolation trans lines
!               !To optimize, wl4, ll4, and ll2ra must be made variable
!               !Example:  change ll4=55 to ll4 # 40 55 80
!
OPT
  RANGE 18 21
  WCOMB41 DB[S22] < -15 1
  WCOMB41 DB[S32] < -15 1
  WCOMB41 DB[S11] < -15 1
  WCOMB41 DB[S12] > -6.5 1
```

PART TWO

TESTING OF

INDIUM PHOPHIDE DEVICES

Submicron Gate InP Power MISFET's With Improved Output Power Density at 18 and 20 GHz

M.D. Biedenbender and V.J. Kapoor

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ABSTRACT

Presented here are the microwave characteristics at 18 and 20 GHz of submicron gate indium phosphide (InP) metal-insulator-semiconductor field-effect transistors (MISFET's) for high output power density applications. InP power MISFET's were fabricated with 0.7 μm gate lengths, 0.2 mm gate widths, and drain-source spacings of 2, 3, or 5 μm. The output power density was investigated as a function of drain-source spacing. The best output power density and gain were obtained for drain-source spacings of 3 μm. At 18 GHz output power densities of 1.59 W/mm with a gain of 3.47 dB and a power-added efficiency of 20.0% were obtained for a drain-source spacing of 3 μm. At 20 GHz output power densities of 1.20 W/mm with a gain of 3.17 dB and a power-added efficiency of 13.6% were obtained for a drain-source spacing of 3 μm. The output power density is 2.7 times greater than has previously been measured for InP MISFET's at 18 and 20 GHz, and the power-added efficiency has also been increased. The output power density is also 50% better than recently reported for comparable gate width pseudomorphic HEMT's at 20 GHz. The power gain was stable to within 3.0% over 12 hours, and the drain current variation during the same time was less than 5%.

I. Introduction

Indium phosphide (InP) is a compound semiconductor with several material properties which make InP metal-insulator-semiconductor field-effect transistors (MISFET's) especially suited for power amplification at microwave and millimeter-wave frequencies. InP FET's should operate at higher frequencies than gallium arsenide (GaAs) FET's due to the higher peak and saturation electron velocities of InP. InP is better for high-power applications since it has a 30% higher breakdown field and lower ionization coefficients compared to GaAs and a 55% higher room temperature thermal conductivity compared to GaAs [1].

The insulated gate of a MISFET also has several advantages for power amplification. Gate leakage current is virtually eliminated and larger positive gate voltages may be used, which provide both charge accumulation for higher channel current as well as higher gate-source and gate-drain breakdown voltages.

The disadvantage of an insulated gate on InP has been the dc drain current drift with time, which has been widely examined. Shokrani and Kapoor [2] have examined gate insulators with reduced dc drain current drift for InP power MISFET's, and drift mechanisms have been reviewed by Wager et al. [3]. The InP MISFET output power at microwave frequencies has been demonstrated to be more stable than the dc drain current [4].

The promise offered by InP MISFET material and device properties has been realized by record power densities in both the microwave and millimeter-wave region. Messick et al. [4] have demonstrated 4.5 W/mm at 9.7 GHz for InP MISFET's on n-type epitaxial layers using a 1.4 μm gate length and a total gate width of 1 mm. Biedenbender, Kapoor, Messick, and Nguyen [5] and Shokrani et al. [6] have reported 2.4 and 2.7 W/mm, respectively, at 9.7 GHz for an all ion-implanted version of the above device. Others have reported lower output power densities from InP MISFET's with gate lengths from 1.2 to 0.3 μm at frequencies up to 30 GHz [7-10]. The microwave

performance of power FET's is affected by the device size, especially the gate length and the drain-source or drain-gate spacing [11]. However, no investigation of the microwave properties as a function of the drain-source spacing has been reported for InP power MISFET's.

Presented here are the microwave results from a new 0.7 μm gate length InP power MISFET. The new design uses a submicron gate length for operation at high microwave frequencies and drain-source spacings of 2, 3, or 5 μm to compare the effect of device size on output power. Current-voltage (I-V) characteristics are given at dc as well as power measurements at 18 and 20 GHz including output power density, power gain, and power-added efficiency (η_{add}) as function of drain-source spacing. The output power density, power gain, and power-added efficiency at 20 GHz as a function of drain voltage are presented. The variation of power gain and drain current as a function of time is also examined.

II. Experimental

Figure 1 shows a schematic cross section of a submicron gate InP MISFET. The InP MISFET design was based on the structure recently reported by the authors [5]. The InP MISFET's investigated in this work had gate lengths of 0.7 μm. The gate length was reduced compared to the previous structure [5] to provide higher transconductance and power gain for better operation at higher frequencies [12]. The length of the channel recess was 1 μm. The new MISFET design included three devices with drain-source spacings (L_{DS}) of 2, 3, or 5 μm. The InP MISFET's with L_{DS}=5 μm were included since these devices have been reported to provide record output power densities at 9.7 GHz [4]. A drain-source spacing of 5 μm is also similar to values used for GaAs MESFET's to provide good breakdown voltages and high reliability at 15 GHz [12] as well as high total output power at 20 GHz [13]. The L_{DS}=2 and 3 μm devices were included since at higher frequencies lower gate-source and gate-drain parasitics are often necessary despite the lower breakdown voltages possible as device size decreases [11].

The total gate width of the devices was 0.2 mm. Two individual gates with a width of 100 μm were connected in parallel to obtain the total gate width of 0.2 mm. An individual gate width of 100 μm was used to minimize the gain degradation that can occur for large widths as frequency increases. The same individual gate width has recently been reported for pseudomorphic power HEMT's at 20 GHz [14]. A large average spacing of 114 μm between individual gates was used to allow enough room for wire bonds to the individual drain and gate regions. The large gate-to-gate spacing provides the benefit of a low thermal impedance and minimizes the temperature rise [15]. The devices were designed with ten 100 μm wide gates and several gate bonding pads available to provide various total gate widths of up to 1 mm [4]. The total area of each device was 0.5 mmX1.4 mm.

The starting substrate material used for InP MISFET's was a 2-in-diameter semi-insulating (Fe-doped) InP wafer. The surface orientation of the substrate was <100> with a 2° misorientation to the closest <110> directions. Initial cleaning of the InP was done using a sequence of trichloroethylene, acetone, and methanol for degreasing. After degreasing the InP was rinsed in deionized H_2O (DI H_2O) followed by a solution of 1:1 DI H_2O:HF for surface oxide removal, and a final DI H_2O rinse and nitrogen blow dry. Additional details of the InP cleaning procedure have been previously described by Valco, Kapoor, Biedenbender, et al. [16,17].

The InP layers used for the fabrication of the MISFET's have been grown by low pressure metal organic vapor phase epitaxy (MOVPE) in a commercial AIXTRON AIX 200 horizontal reactor as widely used for industrial compound semiconductor production. The design and the variety of processes for which this reactor type have been applied are described elsewhere [18].

A 0.3 μm thick n-type epitaxial layer with a carrier concentration of $3x10^{17}$ cm^{-3} was grown directly on the semi-insulating substrate by MOVPE without an unintentionally doped buffer layer as shown in Fig. 1. As precursors for the preparation of the InP epitaxial layer trimethylindium (TMIn) and 100% concentrated phosphide (PH_3) were used. For n-type doping silicon was incorporated in the layers by introducing diluted SiH_4 (2% in SiH_4) as a source material into the growth atmosphere. The TMIn was transported from a stainless steel cylinder thermostated at 17 C. The cylinder was electronically pressure controlled for extremely stable evaporation rates. The carrier gas in the reaction cell was Pd diffused H_2.

All gas flows were accurately controlled by electronic mass flow controllers and pneumatically operated valves. For extremely sharp interface formation all precursors were switched by a zero dead volume high speed vent/run switching manifold.

For obtaining highly pure and uniform semiconductor layers on large substrate surfaces the application of low pressure growth processes with high gas velocities have been proven to be advantageous. The reactor included an electronic control unit for the chamber pressure. The present work has been performed on a static susceptor.

For obtaining pure and uniform InP layers the growth temperature was adjusted at 600 C, the reactor pressure was held at 15 Torr, and the total flow rates were adjusted to achieve a gas velocity of 2.2 m/sec. The growth rate for the bulk layer was 2.5 μm/hr at a TMIn pressure of 3 mTorr and a V/III ratio of 500. At the target doping for the epitaxial layer, $3x10^{17}$ cm^{-3}, the electron mobility at 77 K was 5000 $cm^2/Vsec$. The crystalline properties of the grown layer were excellent, as shown by a FWHM of less than 15" of the <004> Bragg reflection line in the DCXD spectrum. The surface morphology was featureless in optical microscopy.

Figure 2 illustrates cross sections of the fabrication sequence for the InP MISFET's. Step A of Fig. 2 shows photolithography for the mesa isolation etch. Mesa etching was done using 10 wt.% HIO_3 in DI H_2O. Step B of Fig. 2 shows the source and drain ohmic contacts. The metal patterns were defined by a liftoff technique. The ohmic contacts consisted of a 1500 Å Au:Ge layer and a 1000 Å Au overlayer alloyed at 405 C for 1½ min. Step C of Fig. 2 shows the active channel gate recess. A photoresist mask was used during etching in 30:1 DI H_2O:HBr with 1 drop of H_2O_2 for each 20 ml of solution.

Step D of Fig. 2 shows the silicon dioxide gate insulator deposition. The silicon dioxide was deposited at 250 C using a Technics Planar-Etch II-A plasma reactor, operated at 13.56 MHz with automatic matching. The flow rates used during deposition were 55 sccm nitrous oxide and 23 sccm silane, and the deposition pressure was 350 mTorr. The rf power used was 50 W, corresponding to a power density of 85 mW/cm^2. The details of silicon dioxide deposition on InP have been reported by Shokrani and Kapoor [2]. After deposition the gate insulator was annealed at 300 C for 1 hr in pure H_2.

A 1000 Å gate insulator thickness was reported by Biedenbender, Kapoor, Messick, and Nguyen [5] for a 1.4 μm gate length InP power MISFET at 9.7 GHz. A thinner dielectric can be expected for smaller gate lengths and higher frequencies. A gate insulator thickness of 700 Å has been used by Gardner et al. [9] up to 20 GHz and by Saunier et al. [10] at 30 GHz. The gate insulator thickness used in this investigation was 630 Å. The saturation current density was measured to be ≈1 A/mm after the gate recess and gate insulator deposition and anneal. Saunier et al. [10] have reported the same saturation current density for millimeter-wave operation.

Step E of Fig. 2 shows the gate metal and submicron lithography for the InP MISFET's. The submicron lithography was a variation of the multi-level portable-conformable-mask technique [19]. A thick bottom resist (≈1.1 μm) was used to planarize the gate region. A 1000 Å layer of SiO_2 was deposited on the bottom resist by e-beam evaporation. Finally, a thin (≈2000 Å) resist was spun on the e-beam oxide. The thin top imaging resist was exposed using a 0.5 μm mask and developed. The pattern was transferred to the e-beam SiO_2 using a CF_4/O_2 plasma etch. Because of the isotropic nature of the plasma used the feature size obtained in the SiO_2 layer increased to 0.7 μm. The bottom resist was opened using an oxygen plasma, and the remaining e-beam oxide layer defined the gate during a subsequent metal evaporation and liftoff. The gate metal was 200 Å Ti and 4000 Å Au. Bonding pads to the submicron gates were patterned in a separate, conventional liftoff lithography and were also Ti/Au.

Step F of Fig. 2 shows openings etched in the SiO_2 to the source and drain contact regions. A 4000 Å Au overlayer was deposited in the openings to assist the current handling of the devices and to ensure easy wire bonding. The InP samples were thinned to ~100 m to decrease the thermal impedance of the devices, and were scribed into individual MISFET's. A 200 Å Ti layer and a 4000 Å Au overlayer were deposited on the sample back to aid heat dissipation.

Microwave power measurements for the completed InP MISFET's were obtained using a test fixture with microstrip input and output circuits shown in Fig. 3. The dc bias was applied through an rf choke consisting of a high impedance transmission line in series with low impedance radial stubs. The rf choke was designed for bias currents up to 1.5 A. External chip capacitors across microstrip gaps were used as dc blocks near the test fixture input and output. The circuit design was optimized using commercially available software from 20 to 40 GHz for a wide range of operation. To accommodate the range of device impedances resulting from different drain-source sizes and operation at different frequencies, impedance matching was done empirically using external metal stubs close to the transistor.

The microstrip circuits were epoxied to a gold-plated brass block. The transistors were mounted on a metal ridge between the input and output circuits. Electrical connections to the gate and drain were made by 1 mil diameter wire bonds to the input and output microstrips, respectively. An electrically and thermally conductive silver-loaded epoxy was used for mounting the device and electrical connection to the source. Electrical connections between the test fixture microstrip and measurement system were made using 2.4 mm coax to microstrip launchers with a frequency range up to 50 GHz. Figure 3 shows the test fixture with the coax-to-microstrip launchers. Figure 4 shows a test fixture with a mounted transistor.

A calibration fixture to account for test fixture insertion loss was made with a microstrip through line in place of the transistor. Power measurements of InP MISFET's reported below have been corrected for the minimum calibration fixture insertion loss measured using external tuning at 18 and 20 GHz.

III. Results

Figure 5 shows a typical I-V characteristic for an InP power MISFET with L_{DS}=2 μm and W=0.2 mm. The gate voltage ranges from 0 to -10 V in 1 V steps. The extrinsic transconductance is at least 75 mS/mm for gate voltages greater than -4 V. The zero gate voltage saturation current is ≈1 A/mm at a drain voltage of 5 V. The transconductance and current density are representative values for all devices. For L_{DS}=3 and 5 μm the saturation drain voltage increases as expected with device size to ≈3.8 and ≈4.1 V, respectively. As reported elsewhere, the InP MISFET channel current can not be pinched off in the normal curve tracer dc sweeping mode [2,4,6,10]. However, previous results have shown the channel can be pinched off using a curve tracer which applies the gate voltage in 80 μsec pulses [4,5,10]. Similar decreases in drain current using pulsed gate voltages compared to dc sweeping have also been reported for GaAs power MESFET's [20].

The drain-source breakdown voltages for the I-V measurements in Fig. 5 are 6 V for L_{DS}=2 and 3 μm and 8 V for L_{DS}=5 μm. These voltages are comparable to the 6 V drain bias reported by Saunier et al. [10] for 30 GHz devices with L_{DS}=1.5 μm and a drain current density of 1 A/mm. However, they are lower than the drain voltages of 9 to 18 V reported for other InP MISFET's between 4 and 20 GHz with drain current densities of 70 to 660 mA/mm [4-10]. The gate-drain and gate-source breakdown voltages are >25 V for all devices.

Figures 6a and 6b show measurements at 18 and 20 GHz, respectively, of output power density, power-added efficiency, and power gain as a function of L_{DS}. The gate width is 0.2 mm and the gate voltage is zero for all measurements. At both frequencies the output power density and power gain for conditions used to obtain high output power are best for L_{DS}=3 μm, second for L_{DS}=2 μm, and lowest for L_{DS}=5 μm.

In Fig. 6a at 18 GHz for L_{DS}=2 μm the input power, drain voltage, and drain current density are 21.55 dBm, 6.0 V, and 603 mA/mm, respectively. For L_{DS}=3 μm the input power, drain

voltage, and drain current density are 21.55 dBm, 7.0 V, and 625 mA/mm, respectively. For L_{DS}=5 μm the input power, drain voltage, and drain current density are 19.55 dBm, 7.0 V, and 589 mA/mm, respectively. The output power density for all device sizes is greater than previous measurements for InP MISFET's at 18 GHz [9]. For L_{DS}=3 μm the output power density is up to 1.59 W/mm, which is better by a factor of 2.7. The total output power (up to 318 mW) is comparable to the total powers obtained from larger gate width InP MISFET's at these frequencies [9]. The power-added efficiencies of 23.0 and 20.0% for the L_{DS}=2 and 3 μm devices, respectively, are also improvements for InP MISFET's measured at 18 GHz. The power-added efficiency for L_{DS}=5 m is 12.7% and is less than the value of 15.7% previously achieved at 18 GHz [9].

In Fig. 6b at 20 GHz for L_{DS}=2 μm the input power, drain voltage, and drain current density are 18.63 dBm, 5.6 V, and 690 mA/mm, respectively. For L_{DS}=3 μm the input power, drain voltage, and drain current density are 20.64 dBm, 7.0 V, and 654 mA/mm, respectively. For L_{DS}=5 μm the input power, drain voltage, and drain current density are 19.65 dBm, 6.0 V, and 603 mA/mm. At 20 GHz the L_{DS}=5 μm device has a low power gain less than 2 dB. However, there is over 3 dB gain for the L_{DS}=3 and 2 μm devices, which again have output power densities better than has been reported for larger gate width InP MISFET's providing comparable total output power (up to 240 mW) at 20 GHz [9]. For L_{DS}=3 μm the output power density is up to 1.20 W/mm, which is again better by a factor of 2.7 compared to previous measurements at 20 GHz. For L_{DS}=3 μm η_{add} is improved to 13.6%. At 23 GHz the best gain that could be obtained for any of the devices was only 2.1 dB.

The reason for the best output power being available for L_{DS}=3 μm is probably due to the tradeoff between lower parasitics for smaller devices and higher breakdown voltages for bigger devices. Although parasitics are lower for L_{DS}=2 μm, the drain voltage is higher for L_{DS}=3 μm. At 18 GHz the output power is less for L_{DS}=5 μm even though the drain voltage is the same as for L_{DS}=3 μm. At 20 GHz the maximum

drain voltage decreases for L_{DS}=5 μm and power gain and output power are low.

Figure 7 shows microwave power measurements at 20 GHz of output power density, power gain, and power-added efficiency as a function of drain voltage. The measurements are for a device with W=0.2 mm and L_{DS}=3 μm. The maximum output power density at 20 GHz is 1.20 W/mm, with a corresponding gain of 3.17 dB and power-added efficiency of 13.6%. The input power is 20.6 dBm; it is the highest examined at 20 GHz for this device and the gain in Fig. 7 is compressed for all drain voltages. The power gain, P_{out}, and η_{add} all increase with drain voltage. At 18 GHz the same device had a maximum output power density of 1.59 W/mm, with a corresponding gain of 3.47 dB and power-added efficiency of 20.0% for a drain voltage of 7.0 V and P_{in}=21.6 dBm.

The drain current decreases with increasing microwave input power as has been previously observed for InP MISFET's [4,5,10]. The saturation current density for the device in Fig. 7 at 18 and 20 GHz is 654 mA/mm for P_{in}=20.6 dBm and a drain voltage of 7.0 V. The decrease in drain current with P_{in} has been attributed to a change in the charge status of states near the InP-insulator interface [4,5], although a mechanism for the response of such states at the high frequencies involved is yet to be developed. Another possible cause for the decreased current is the nonlinear output characteristics that can occur as the device is driven into compression [21]. The lower drain current results in higher drain-source breakdown voltages compared to dc values. The maximum drain voltages that can be used with rf power applied are 8 V for L_{DS}=2 or 3 μm and 9 V for L_{DS}=5 μm. When high drain voltages are used to obtain maximum output power, a high input power must also be applied for a low drain current. Reducing P_{in} while a high drain voltage is applied results in increased current and thermal breakdown of the transistor. The change in drain current limits the range of P_{in} for measurements of P_{out} versus P_{in} under constant bias conditions.

Figure 8 shows the power gain and drain current variation over a 12 hour period. The measurements are at 18 GHz for a L_{DS}=3 μm device. The microwave input power was set to an initial value of 15.66 dBm. The gate voltage was 0 V. At t=0 sec the drain voltage was changed from 1.5 V to 5.5 V. The gain and drain current density at t=0 sec were 3.60 dB and 721 mA/mm, respectively. The microwave power source had a power variation of 0.15 dB during the measurement time, so the power gain variation is shown instead of the output power variation to eliminate the effect of the input power variation. The power gain was stable to within 3.0%, which corresponds to an overall change of 0.13 dB. The drain current showed an initial increase of 2.0% and later decreases of as much as 2.4%. The power gain stability is slightly less than the output power stability of 2% over 167 hours previously reported for 1.4 μm gate length power MISFET's [4]. However, the drain current change is better than the value of 10% observed for the 1.4 μm gate length MISFET's [4].

IV. Summary

InP power MISFET's were fabricated with a 0.7 μm gate length. Different device sizes were examined with gate widths of 0.2 mm and drain-source spacings of 2, 3, and 5 μm. Current-voltage measurements at dc indicated extrinsic transconductances of up to 75 mS/mm. The drain-source breakdown voltages were 6 to 8 V. The gate-source and gate-drain breakdown voltages were >25 V. Power measurements at 18 and 20 GHz showed output power densities up to 2.7 times greater than previously observed at these frequencies for InP MISFET's, and power-added efficiency was also improved. At 18 GHz for a drain-source spacing of 3 μm the output power was 318 mW (1.59 W/mm) with a gain of 3.47 dB and a power-added efficiency of 20.0%. At 20 GHz for a drain-source spacing of 3 μm the output power was 240 mW (1.20 W/mm) with a gain of 3.17 dB and a power-added efficiency of 13.6%. The output power density for the 0.2 mm gate width InP MISFET's here is 50% greater than the value of 0.8 W/mm recently reported at 20 GHz for 0.15 mm gate width pseudomorphic HEMT's with 0.25 μm gate lengths [14].

The best output power density and gain were obtained for drain-source spacings of 3 μm. The maximum drain voltage was lower for 2 μm drain-source space devices as was the gain and output power density. Devices with a 5 μm drain-source space had lower gain and output power density despite comparable maximum drain voltages to the 3 μm drain-source space devices. The power gain was stable to within 3.0% over 12 hours. The drain current variation was less than 5% during the same time period.

The gain was less than 3 dB and the output power density was low for gate widths greater than 0.2 mm. The total output power of the InP MISFET's here may be improved if the drain-source breakdown voltage can be increased through optimization of the device processing. Although excellent output power densities and power-added efficiencies have been achieved for gate widths of 0.2 mm, the maximum drain voltages that can be

used are relatively low compared to most other InP MISFET's. Several parameters including the drain saturation current resulting from the gate recess, channel thickness, and channel doping density could be investigated to increase the drain-source breakdown voltages for the InP MISFET's here. Higher breakdown voltages may provide even better output power density and enhance the operation of larger gate width InP MISFET's for higher total power. The total output power may also be improved through the use of a different device topology for better power combining, such as air bridge connections and source vias commonly used in commercial devices.

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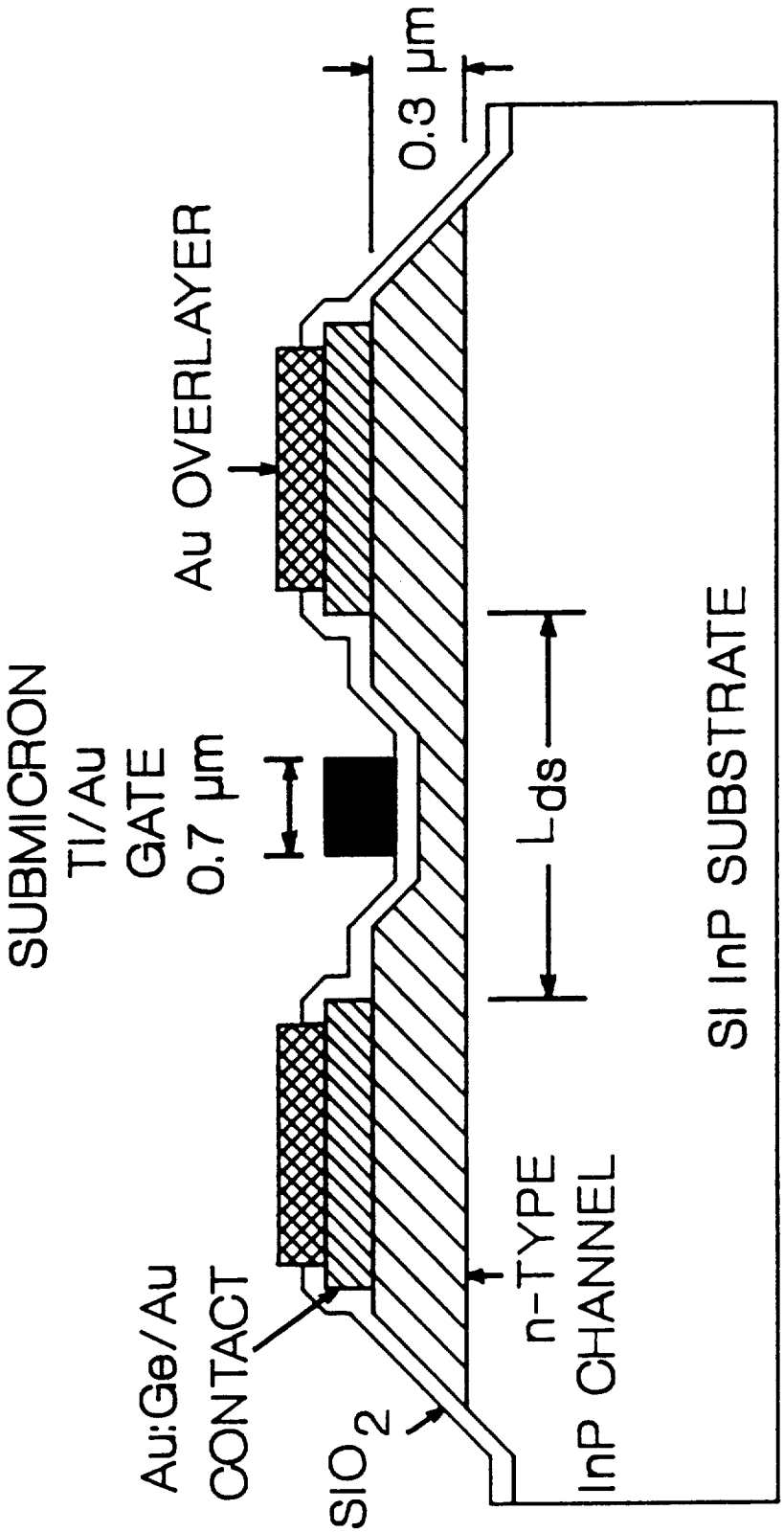
Figures


0.3 μm
Au OVERLAYER
SUBMICRON
Ti/Au
GATE
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Lds
SI InP SUBSTRATE
Au:Ge/Au
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SiO2
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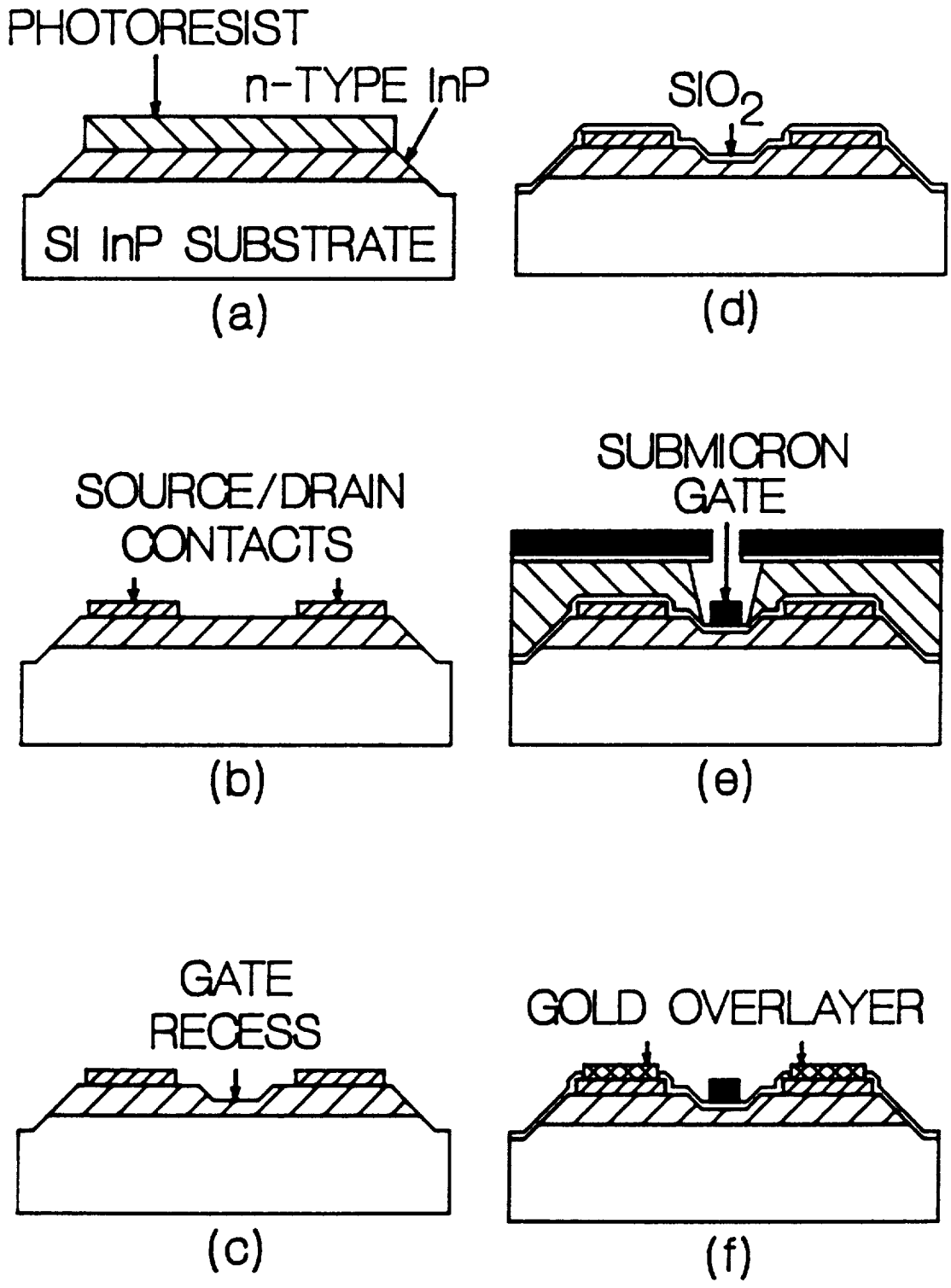
InP CHANNEL

FIGURE 1


PHOTORESIST
n-TYPE InP
SI InP SUBSTRATE
(a)
SIO2
(d)
SOURCE/DRAIN
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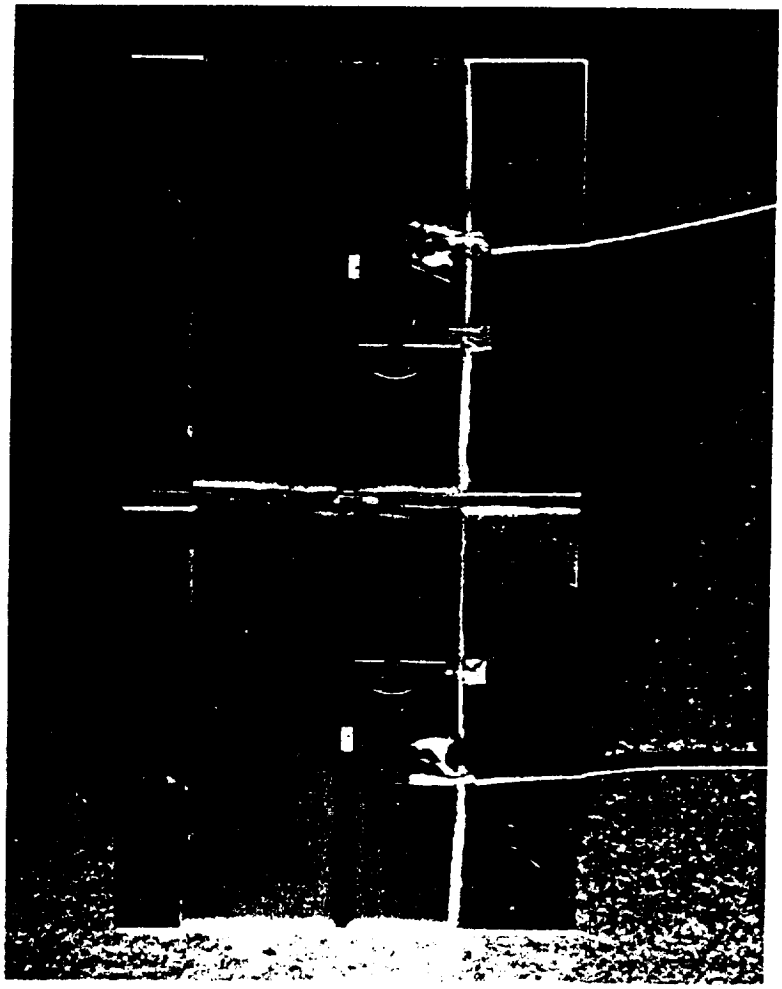
GATE
RECESS
(c)
GOLD OVERLAYER
(f)

FIGURE 2



NASA
C-90-11398

FIGURE 3

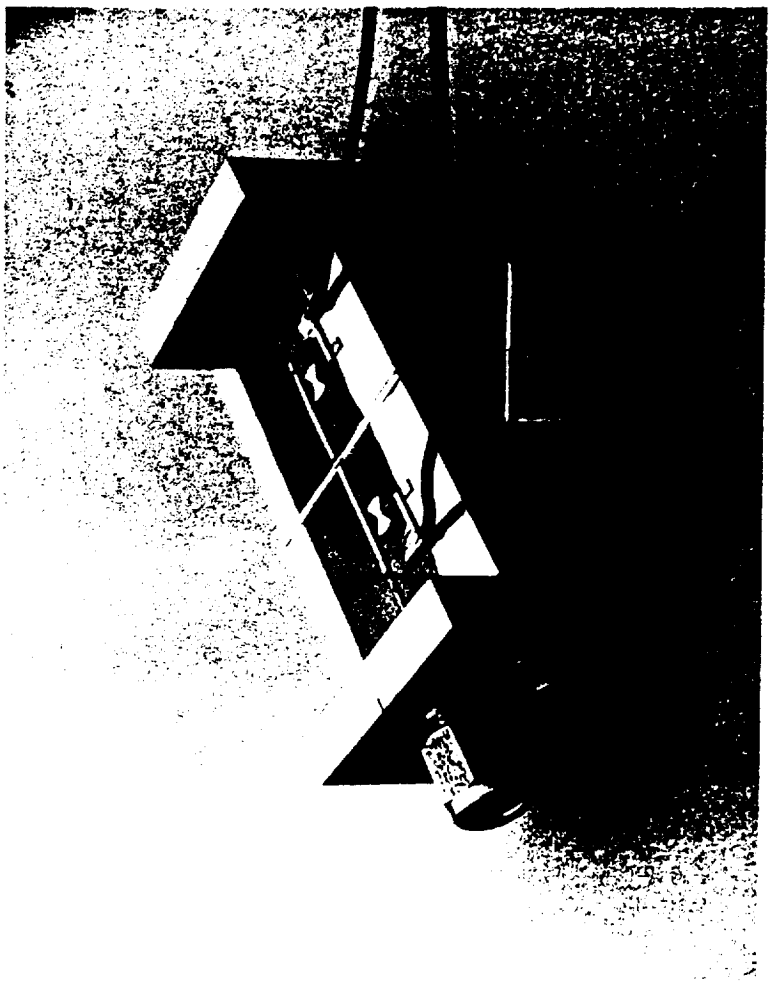


FIGURE 4

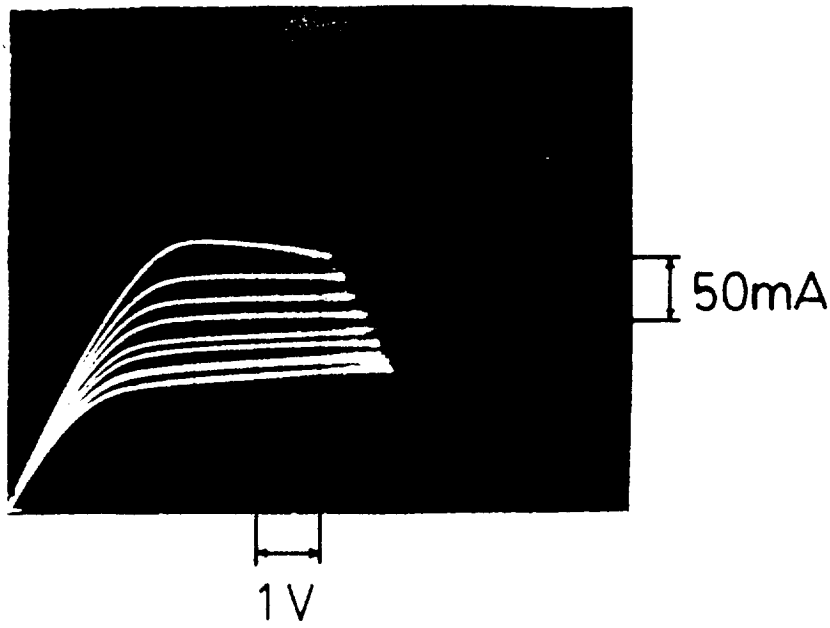


FIGURE 5

(a)
18 GHz
DRAIN-SOURCE SPACING (μm)
POWER GAIN (dB)
OUTPUT POWER DENSITY (W/mm)
POWER-ADDED EFFICIENCY (%)
(b)
20 GHz
DRAIN-SOURCE SPACING (μm)
POWER GAIN (dB)
OUTPUT POWER DENSITY (W/mm)
POWER-ADDED EFFICIENCY (%)

FIGURE 6

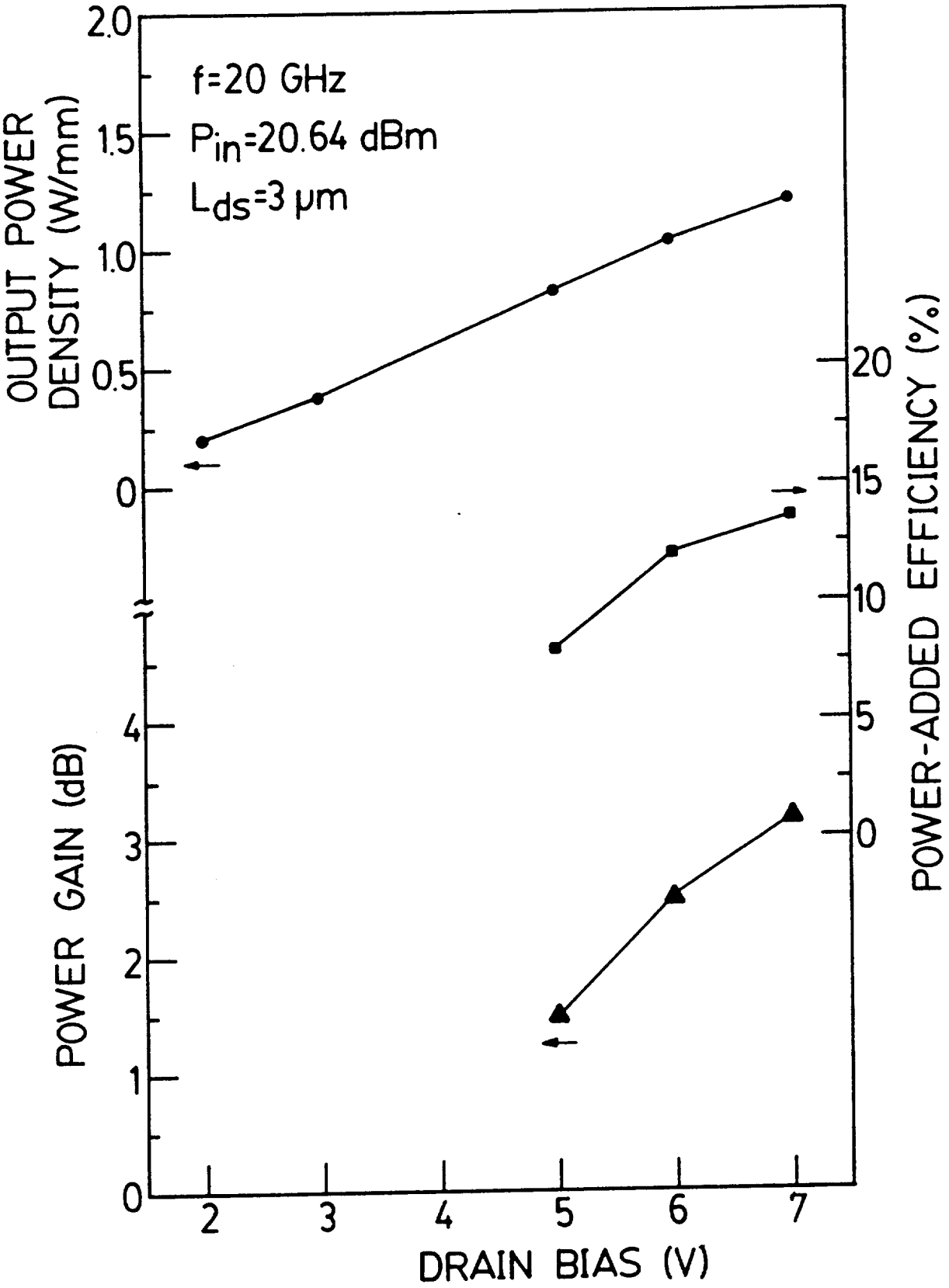

f=20 GHz
P_{in}=20.64 dBm
L_{ds}=3 μm
OUTPUT POWER DENSITY (W/mm)
POWER GAIN (dB)
POWER-ADDED EFFICIENCY (%)
DRAIN BIAS (V)
2.0
1.5
1.0
0.5
0
4
3
2
1
0
20
15
10
5
0
2
3
4
5
6
7

FIGURE 7

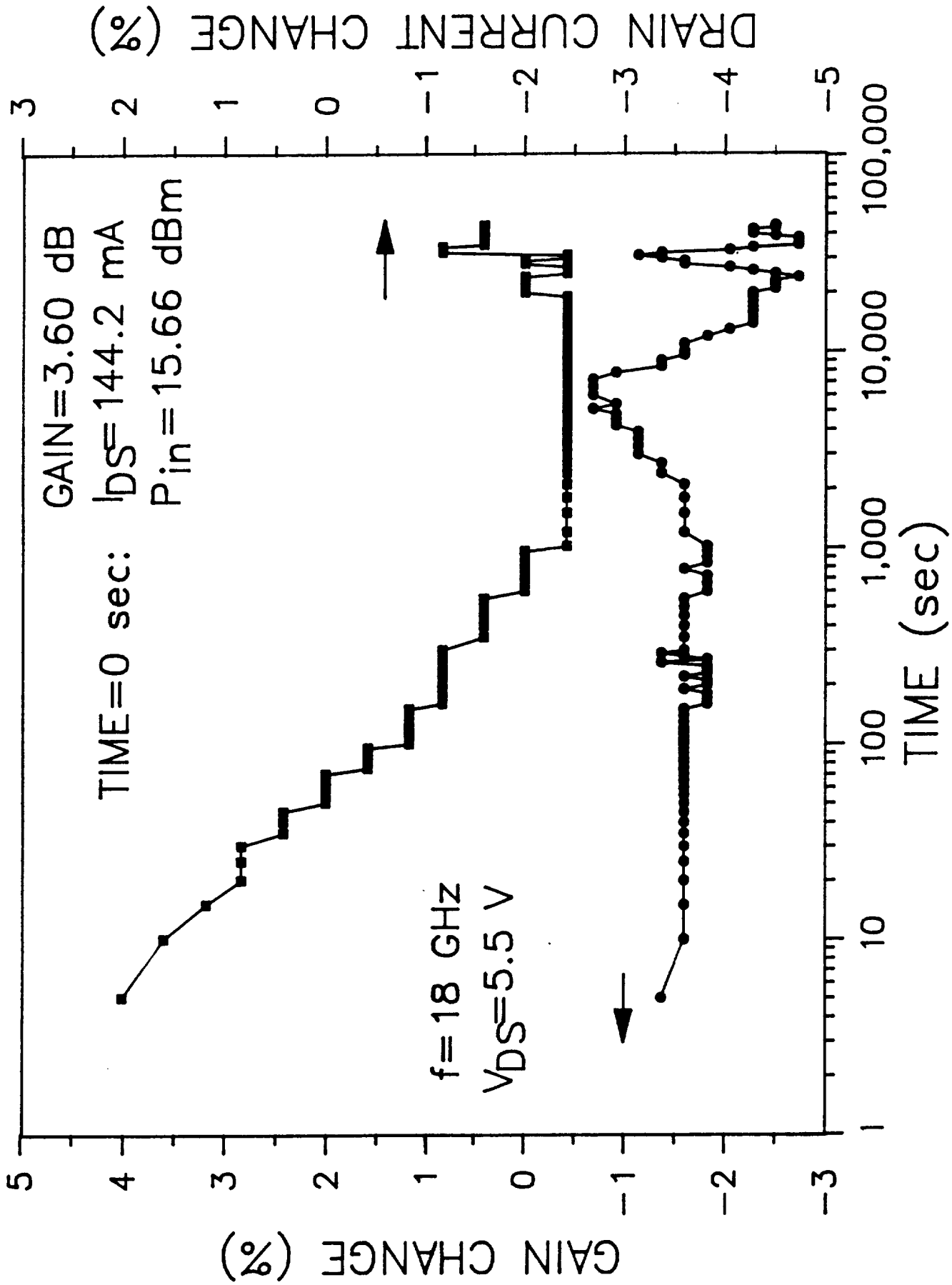

GAIN CHANGE (%)
DRAIN CURRENT CHANGE (%)
TIME (sec)
TIME=0 sec: I_{DS}=144.2 mA
P_{in}=15.66 dBm
GAIN=3.60 dB
f=18 GHz
V_{DS}=5.5 V

FIGURE 8