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PART ONE

POWER COMBINER

FOUR-TO-ONE POWER COMBINER FOR 20 GHz PHASED ARRAY ANTENNA USING RADC MMIC PHASE SHIFTERS

The design and microwave simulation of two-to-one and four-to-one microstrip power combiners is described. The power combiners were designed for use in a four element phased array receive antenna subarray at 20 GHz. Four test circuits are described which were designed to enable testing of the power combiner and the four element phased array antenna. Test Circuit 1 enables measurement of the two-to-one power combiner. Test Circuit 2 enables measurement of the four-to-one power combiner. The four element antenna array uses hermetic coaxial feedthroughs indicated in Figure 1 for connection between the antenna patch and the microstrip transmission lines. Test Circuit 3 enables measurement of a four element antenna array without phase shifting MMICs in order to characterize the power combiners with the antenna patch-to-microstrip coaxial feedthroughs. Test Circuit 4 is the four element phased array antenna including the RADC MMIC phase shifters and appropriate interconnects to provide bias voltages and control phase bits.

Several microwave hybrid junctions can be used to divide an input signal from one port into two or more output signals. The same circuits can also be used to produce a single output proportional to the sum of two or more input signals. For a microstrip implementation a Wilkinson power divider (combiner) is one of the easiest to fabricate. Rizzi [1] provides an excellent description of the operation of the Wilkinson power divider. Details from the description by Rizzi are included below to explain how the Wilkinson power divider works.

Figure 2 shows the basic Wilkinson power divider. Two quarter-wave transmission lines are connected to a common port (port 1). The resistor between the other ends of the quarter-wave transmission lines decouples ports 2 and 3. Because of symmetry a signal entering port 1 is divided equally between ports 2 and 3. A signal entering port 2 is isolated from port 3 but can be transmitted to port 1. A signal entering port 3 is isolated from port 2 but not port 1. To match all ports and obtain isolation between ports 2 and 3 the characteristic impedance of the quarter-wave transmission line should be $2^{0.5}*Z_o$, and the resistor between ports 2 and 3 should be $2Z_o$.

The operation of the Wilkinson power divider can be explained using an even- and odd-mode analysis. In an even- and odd-mode analysis of a linear multiple-port microwave circuit the resulting port voltages are determined for excitation at 2 ports with the same voltage (even-mode excitation) and with voltages 180° out of phase (odd-mode excitation). By superposition of the even- and odd-modes the excitation for one port will cancel and the resulting voltages for excitation at a single port can be determined.

Figure 3 shows a circuit used for an even- and odd-mode analysis of the Wilkinson power divider for a voltage source V_G connected to port 2. For the even-mode excitation points a and b must be at the same potential and no current flows through the resistor R. Points d and c may be open circuited without affecting the even-mode operation. Figure 4 can be used as the equivalent circuit for even-mode analysis. By choosing the characteristic impedance of the quarter-wave line as $2^{0.5}Z_o$ the circuit is matched at ports 2 and 3, and $Z_{2e}=Z_{3e}=Z_o$. The even-mode voltages at the ports are $V_{2e}=V_{3e}=V_G/4$ and $V_{1e}=-j2^{0.5}V_G/4$.

For the odd-mode excitation the potential of points d and c is zero and they can be shorted to ground. Figure 5 can be used as the equivalent circuit for odd-mode analysis. The input to the quarter-wave shorted line is an open circuit and the input impedances for the odd-mode are $Z_{2o}=Z_{3o}=R/2$. For a perfect match $R=2Z_o$ as described above. The odd-mode voltages at the ports are $V_{2o}=V_G/4$, $V_{3o}=-V_G/4$, and $V_{1o}=0$.

Superimposing the even- and odd-mode solutions for an input at port 2 yields the following voltages: $V_1=-jV_2/2^{0.5}$, $V_2=V_G/2$, $V_3=0$, and $V_{ab}=V_2 - V_3=V_2=V_G/2$, where V_{ab} is the voltage across the resistor. For one signal at either port 2 or 3 half of the power is dissipated in the resistor and half is delivered to port 1. For the ideal Wilkinson power divider the insertion loss is 3 dB between port 2 and port 1 or between port 3 and port 1. For signals at both ports 2 and 3 a voltage is produced at port 1 proportional to their phasor sum, where $V_1 = -j(V_2 + V_3)/2^{0.5}$. The power associated with the phasor difference is dissipated in the resistor.

The design of the basic Wilkinson power divider can be made easier by including half-wave extensions of the resistive element terminations. Figure 6 shows the design used in Test Circuits 1 through 4 for the Wilkinson power divider. The design in Figure 6 includes the half-wave extension in the manner described by Abita [2]. The half-wave extensions improve the design by greatly reducing the parasitic coupling that would otherwise occur between the quarter-wave sections for the layout of Figure 2. The half-wave extensions shown in Figure 6 also provide additional means for adjustment of the circuit characteristics if desired. One disadvantage resulting from the half-wave extensions is the larger area required.

The Wilkinson power divider design shown in Figure 6 was determined using commercially available software. For the original design of the power divider and simulation of Test Circuits 1, 2, and 3 Touchstone version 1.7 from EESof was used on an IBM AT personal computer. The frequency range for the power divider design was based on the frequency range expected for the MMIC phase shifters. The center frequency expected for the MMIC phase shifters was 19.7 GHz, and the frequency range expected was 19.4 to 19.9 GHz. The design of the power divider shown in Figure 6 was optimized over the frequency range from 18 to 21 GHz.

The substrate dielectric to be used in the fabrication of Test Circuit 1 is 99.6% purity Al_2O_3, which has a dielectric constant of 9.95 ± 0.02 and a loss tangent of 0.0002. The dielectric thickness specified for all test circuits is ten mils. The conductor thickness specified is 1.5 μm (0.06 mils) of gold. For a 50Ω characteristic impedance the conductor width for the 10 mil Al_2O_3 substrate is 9.06 mils. For a $2^{0.5}*50\Omega$ characteristic impedance the conductor width is 3.62 mils. In Figure 6 and in all test circuits the above microstrip widths are rounded off to 9.0 and 3.6 mils. A minimum conductor width of 2.0 mils is specified for the half-wave extensions, resulting in a characteristic impedance of about 83Ω.

The Touchstone program can optimize the values desired for S parameters or other microwave properties by adjusting the widths and lengths of designated microstrip transmission line sections. During the optimization of the power divider design the above conductor widths (w50=9.0 mils, w14=3.6 mils, and w12r=2.0 mils in Figure 6) were kept constant and the lengths of the quarter- and half-wave sections (114, 112ra, and 112rb in Figure 6) were varied. The resulting lengths for the quarter- and half-wave sections were within 5% of the nominal values expected at the center frequency of the MMIC phase shifters.

The power divider design indicated in Figure 6 can withstand significant changes in the value of the thin film isolation resistor and still provide return losses and isolations less than -15 dB, with essentially unchanged insertion losses. Based on fabrication capabilities suggested by manufacturers, a tolerance of ±10% was specified for the 100Ω thin film isolation resistor in all four test circuits. If the deposited thin film resistance cannot meet the ±10 tolerance, laser trimming is to be used to obtain the correct resistance of 100Ω. Microwave simulations of Test Circuits 1, 2, and 3 are included for the nominal 100Ω thin film resistance as well as the ±10% tolerances described above.

Table 1 lists the programs used to simulate Test Circuits 1, 2, and 3, as well as the isolation resistance used during the simulation. The results to be shown below from the programs in Table 1 were determined using Touchstone version 2.1 on a SunSparc 1 workstation. Touchstone version 2.1 uses a different microstrip model [3] to determine the effects of dispersion than used in Touchstone version 1.7 [4]. The difference in microstrip models resulted in some changes in the S parameters compared to those originally calculated, but the return losses and isolations always remained below -15 dB, and the insertion losses were virtually unchanged.

Figure 7 shows the drawing used to specify the design of Test Circuit 1. Test Circuit 1 enables measurement of the two-to-one Wilkinson power divider design indicated in Figure 6. For all test circuits Detail A specifies the Wilkinson power divider design indicated in Figure 6. Test Circuit 1 consists of a 1 inch square alumina substrate. Touchstone program pdivt1a is included in the Appendix as an example of the program used to simulate Test Circuit 1 with the nominal 100Ω isolation resistance.

Figures 8, 9, and 10 show the S parameters simulated for Test Circuit 1 with the nominal 100Ω isolation resistor (pdivt1a), the +10% or 110Ω resistor (pdivt1b), and the -10% or 90Ω resistor (pdivt1c), respectively. For all three figures the worst return loss (S_{22}) is -19.9 dB, and the worst isolation (S_{32}) simulated is -20.2 dB. The simulated insertion loss (S_{21}) is about -3.6 dB and varies less than 0.1 dB with frequency or isolation resistance. The ideal insertion loss for a Wilkinson power divider is -3 dB.

Figure 11 shows the drawing used to specify the design of Test Circuit 2. Test Circuit 2 enables measurement of the four-to-one power combiner which consists of series connected two-to-one Wilkinson power dividers indicated in Figure 6 and in Detail A of Figure 11. Test Circuits 2, 3, and 4 all use a 2.59 inch by 3 inch alumina substrate. The substrate size was determined by external connectors for control of the MMIC phase shifters, and will be discussed below for Test Circuit 4. For Test Circuits 2, 3, and 4 the output microstrip is the same and extends to the substrate edge as shown. In Test Circuit 2 the input microstrip lines were extended to the substrate edge so measurement of the four-to-one power combiner can be done. Touchstone program pdivt2a is included in the Appendix as an example of the program used to simulate Test Circuit 2 with the nominal 100Ω isolation resistance.

Figures 12 through 17 show the S parameters simulated for Test Circuit 2. For Test Circuits 2 and 3 there are 5 S parameters possible without repeated values. S_{11} corresponds to the output return loss; S_{22} corresponds to the return loss at any of the four input ports; S_{21} corresponds to the insertion loss between any of the four input ports and the output port; S_{32} corresponds to the isolation between inputs of the same Wilkinson power dividers; and S_{42} corresponds to the isolation between inputs not connected to the same Wilkinson power divider. Because Touchstone only plots four parameters at a time, two figures are necessary to show the five S parameters for the simulation with the nominal 100Ω resistor (Figures 12 and 13), the +10% or 110Ω resistor (Figures 14 and 15), and the -10% or 90Ω resistor (Figures 16 and 17).

The worst return loss (S_{11}) simulated is -21.9 dB. The worst isolation between inputs of the same Wilkinson power divider (S_{32}) is -18.1 dB. The worst isolation between inputs of different Wilkinson power divider (S_{42}) is -27.6 dB. The insertion loss (S_{21}) is about -7.7 dB, and again varies less than 0.1 dB with frequency or isolation resistance. The ideal insertion loss expected with the series connected Wilkinson power dividers is -6 dB.

Figure 18 shows the drawing used to specify the design of Test Circuit 3. Test Circuit 3 enables measurement of a four element antenna array without phase shifting MMICs in order to characterize the antenna patch-to-microstrip coaxial feedthroughs. The coaxial feedthroughs were indicated in the Feedthrough Cross-Section drawing in Figure 1. The coaxial feedthroughs are also indicated below in the Assembly Drawing for Test Circuit 4 shown in Figure 26. The spacing of the patch antennas and feedthroughs is one inch in Test Circuits 3 and 4.

The Touchstone simulation of Test Circuit 3 does not consider the effects of the feedthroughs or patch antennas, and is essentially the simulation used for Test Circuit 2 with shorter microstrip input lines. Touchstone program pdivt3a is included in the Appendix as an example of the program used to simulate Test Circuit 3 with the nominal 100Ω isolation resistance.

Figures 19 through 24 show the S parameters simulated for Test Circuit 3. Figures 19 and 20 show simulations for the nominal 100Ω resistor. Figures 21 and 22 show simulations for the +10% or 110Ω resistor. Figures 23 and 24 show simulations for the -10% or 90Ω resistor.

The worst return loss (S_{11}) simulated is -21.4 dB. The worst isolation between inputs of the same Wilkinson power divider (S_{32}) is -17.0 dB. The worst isolation between inputs of different Wilkinson power dividers (S_{42}) is -26.4 dB. The insertion loss (S_{21}) is about -7.3 dB, and varies less than 0.1 dB with variations in frequency or isolation resistance.

Figure 25 shows Test Circuit 4. Test Circuit 4 is the four element phased array receive antenna subarray and includes the MMIC phase shifters and interconnects to provide bias voltages and control phase bits. Figure 26 indicates the Assembly Drawing of Test Circuit 4. The MMIC phase shifters are inserted in the MMIC cavities shown in Figures 25 and 26. The spacing of the bias lines indicated at the MMIC cavities corresponds to the bonding pad layout on the MMIC for the various bias lines and control bits. The bias lines on the alumina substrate are to be connected to external control circuitry using a 3M printed circuit board layout card-edge connector (part # 3415). The spacings required for the card-edge connector determine the arrangement of the bias lines at the edge of the alumina substrate, as well as the overall substrate size for Test Circuit 4.

Test Circuit 4 is a phased array antenna subarray demonstration circuit to show a total system operation of the various individual components including the patch antennas, coaxial feedthroughs, the RADC MMIC phase shifters, microstrip transmission lines and power combining circuitry, dc bias line interconnections, printed circuit board card edge connectors, and external control circuitry. For a space qualified mission a smaller subarray size with reduced area for dc bias line interconnections and smaller connectors would be necessary.

References

[1] P.A. Rizzi, Microwave Engineering Passive Circuits, pp. 365-367, Prentice-Hall, Inc., 1988.

[2] J.L. Abita, "Wilkinson Combiner with an Additional Degree of Freedom," pp. 3-5, Touchstone Users Group.

[3] M. Kirshning and R.H. Jansen, Electronics Letters, Jan. 18, 1982.

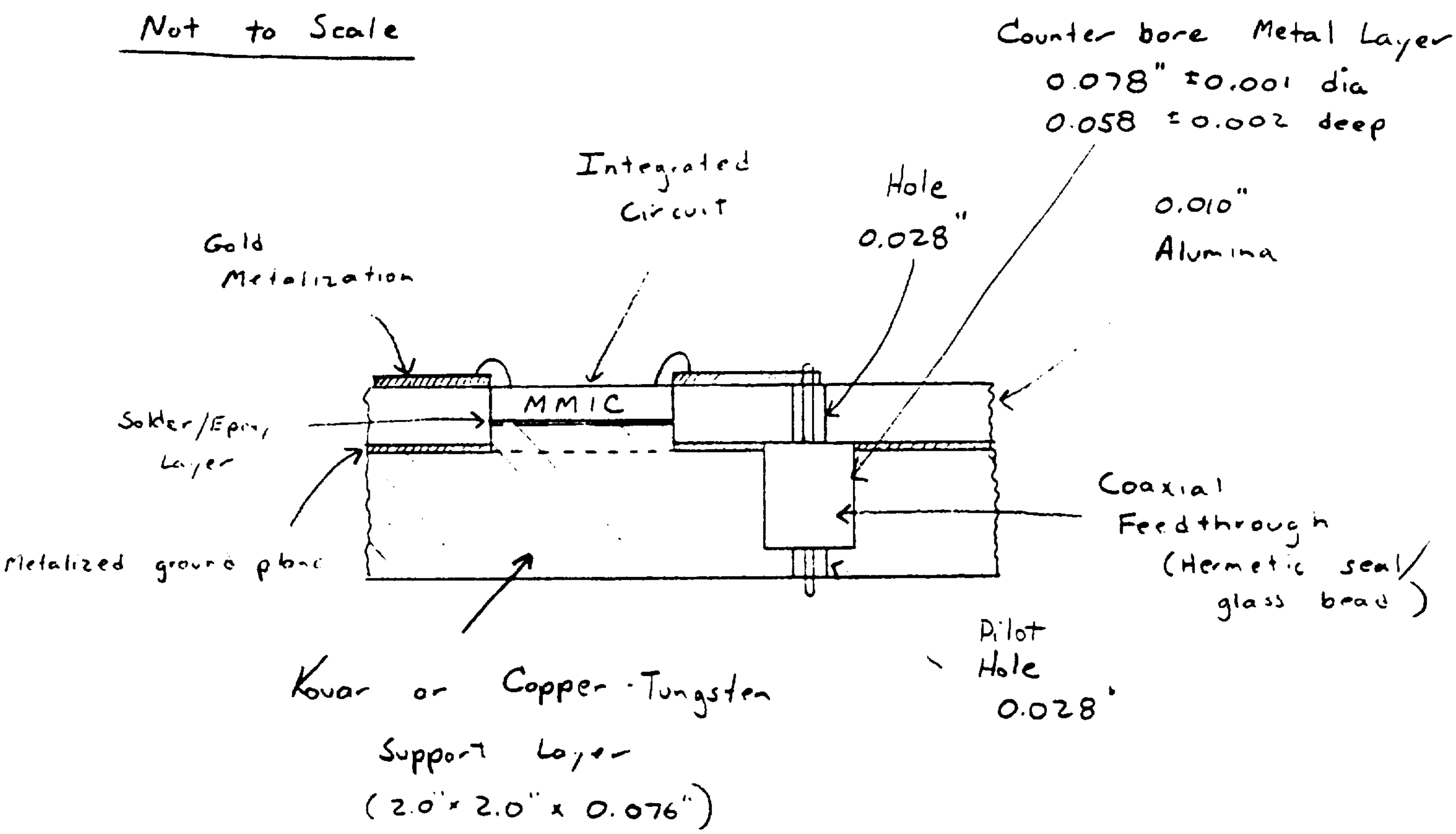
[4] W.J. Getsinger, "Measurement and Modeling of the Apparent Characteristic Impedance of Microstrip," Microwave Theory and Tech., vol. MTT-31, Aug. 1983.

Table 1

Touchstone Programs Used to Simulate Test Circuits 1, 2, and 3

Program	Test Circuit Simulated	Isolation Resistance (Ω)
pdivt1a	1	100
pdivt1b	1	110
pdivt1c	1	90
pdivt2a	2	100
pdivt2b	2	110
pdivt2c	2	90
pdivt3a	3	100
pdivt3b	3	110
pdivt3c	3	90

6/29/90
KAS



NASA / LeRC 20-GHz Receive Element

Feedthrough Cross-section

FIGURE 1

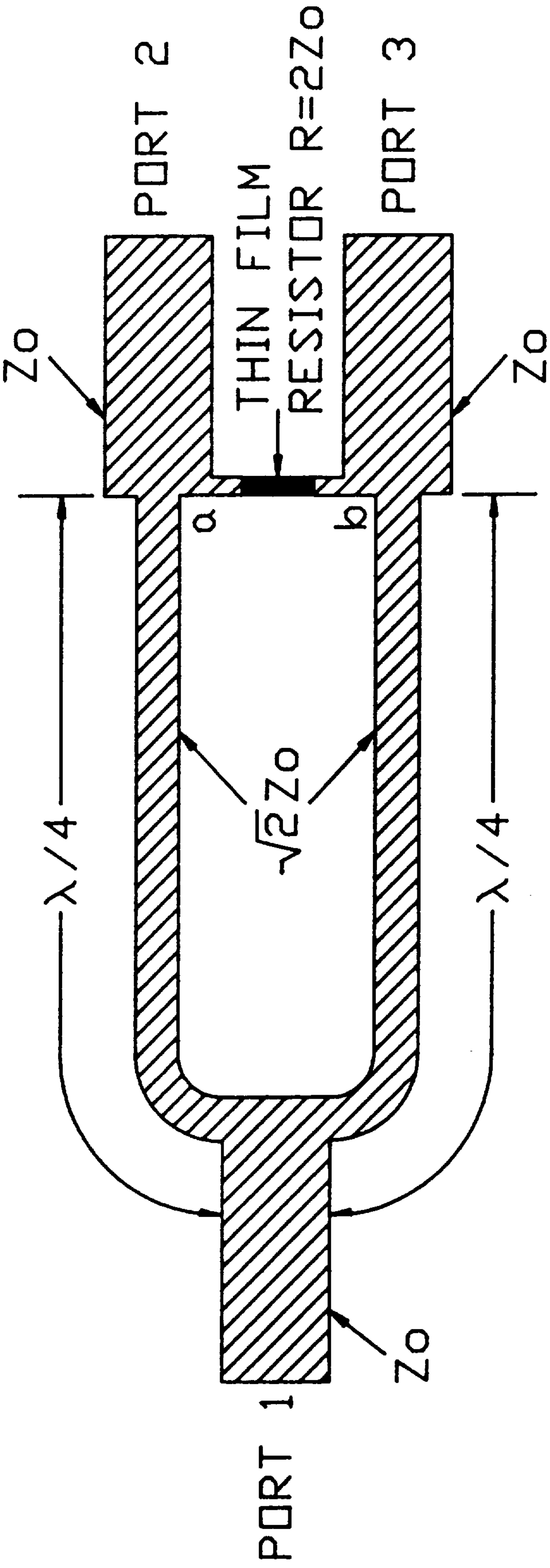

PORT 2
THIN FILM
RESISTOR R=2Zo
PORT 3
Zo
Zo
a
b
λ/4
√2Zo
λ/4
Zo
PORT 1

FIGURE 2

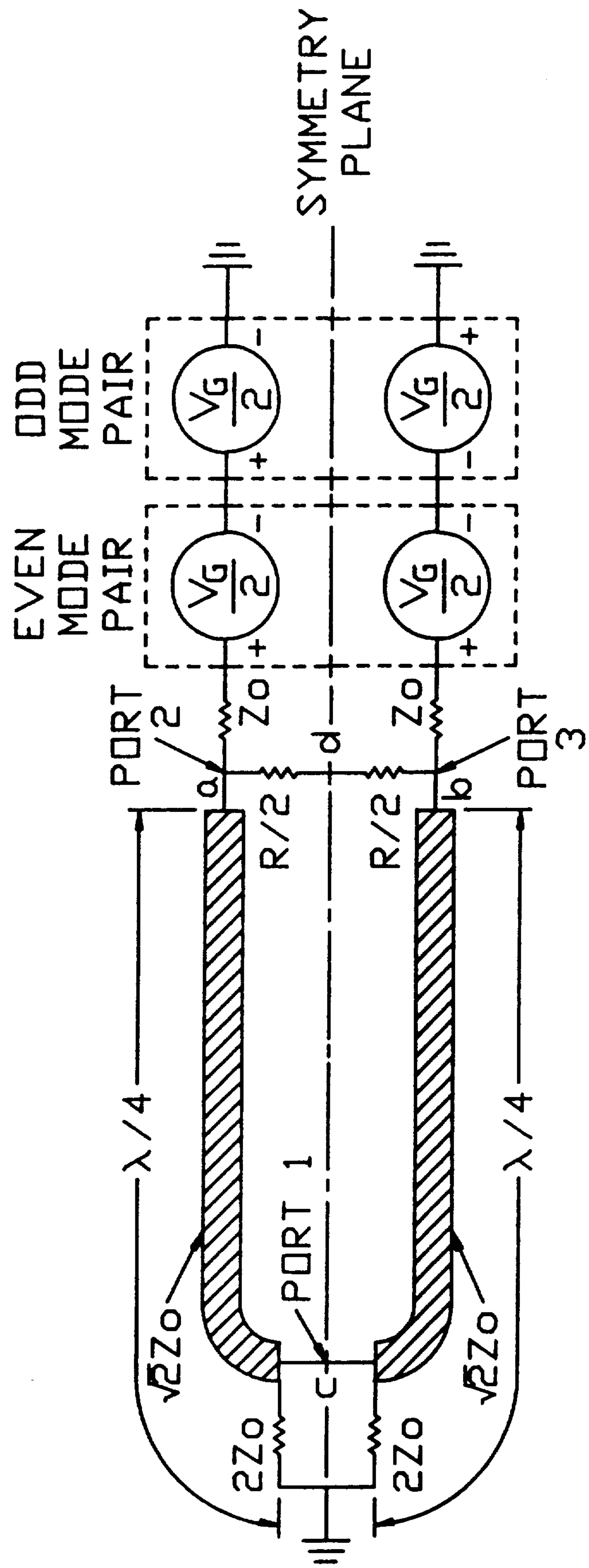

SYMMETRY PLANE
ODD MODE PAIR
EVEN MODE PAIR
$\frac{V_G}{2}$
+
-
PORT 2
PORT 3
PORT 1
Zo
R/2
a
b
c
d
λ/4
√2Zo
2Zo

FIGURE 3

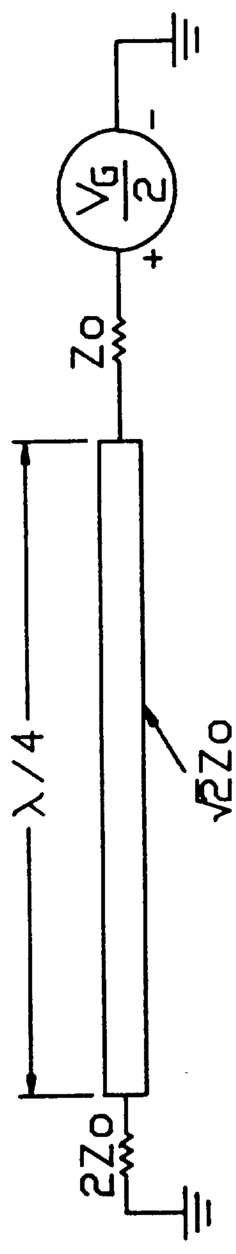


FIGURE 4

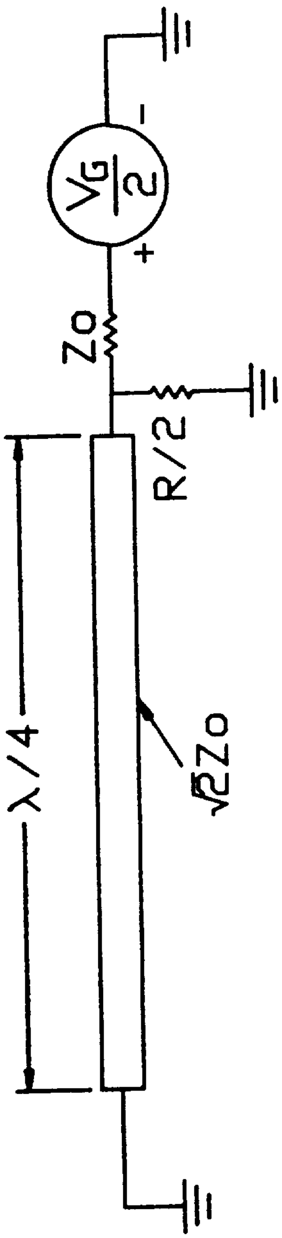


FIGURE 5

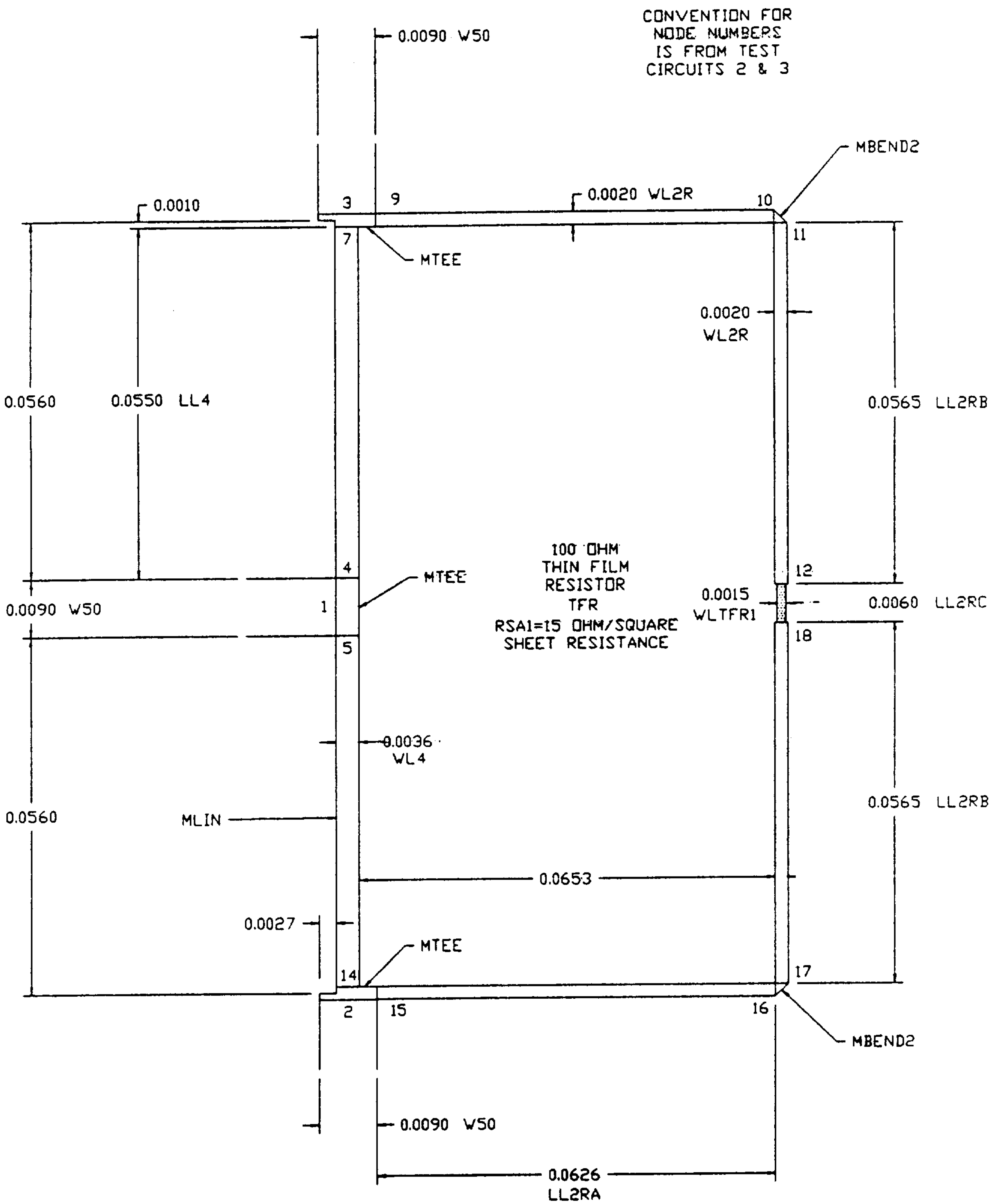

CONVENTION FOR NODE NUMBERS IS FROM TEST CIRCUITS 2 & 3
0.0090 W50
MBEND2
0.0010
3
9
0.0020 WL2R
10
11
7
MTEE
0.0020
WL2R
0.0560
0.0550 LL4
0.0565 LL2RB
100 OHM
THIN FILM
RESISTOR
TFR
RSA1=15 OHM/SQUARE
SHEET RESISTANCE
4
MTEE
12
0.0015
WLTFR1
0.0060 LL2RC
0.0090 W50
1
5
18
0.0036
WL4
0.0560
MLIN
0.0565 LL2RB
0.0653
0.0027
MTEE
14
17
2
15
16
MBEND2
0.0090 W50
0.0626
LL2RA

FIGURE 6

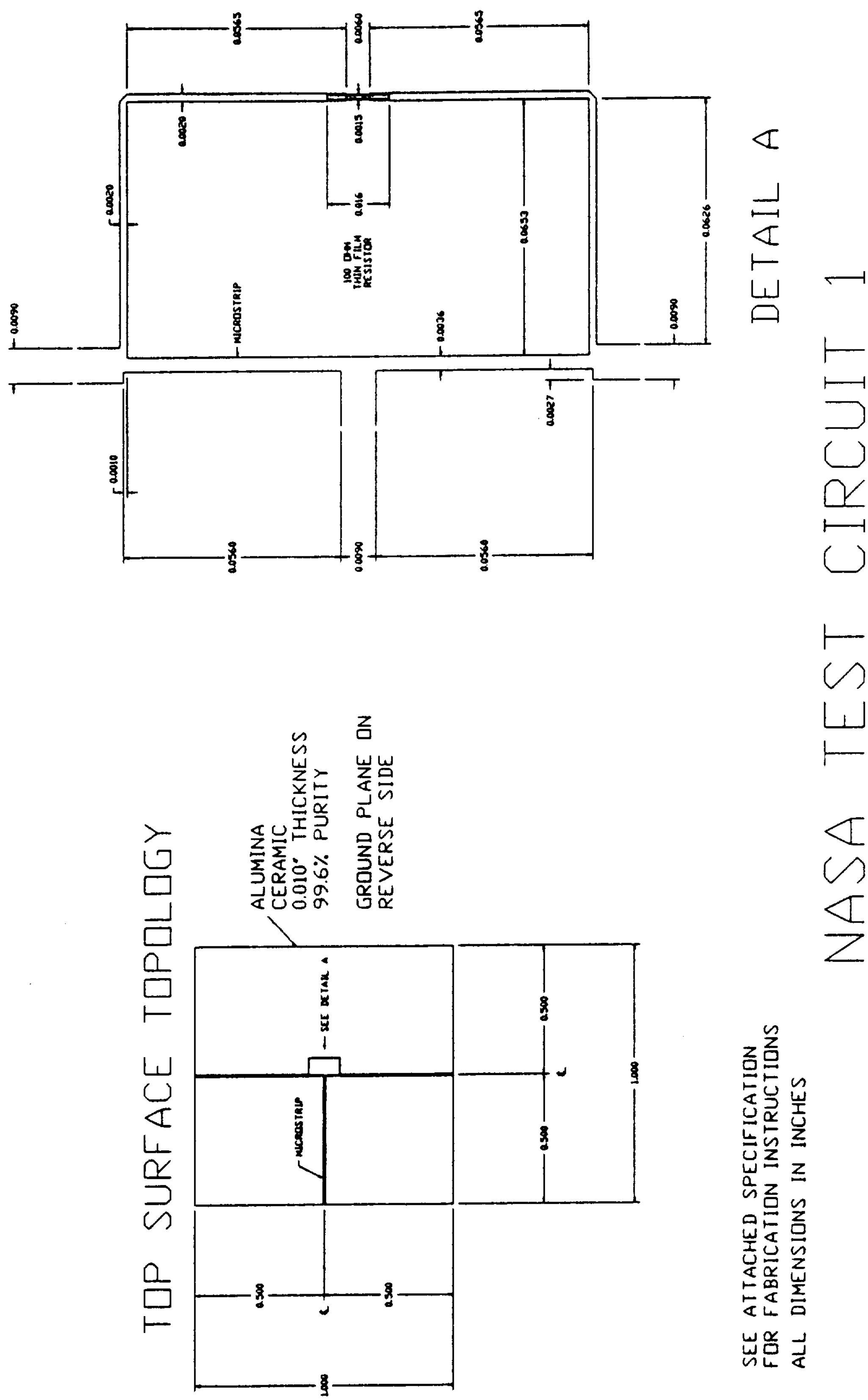
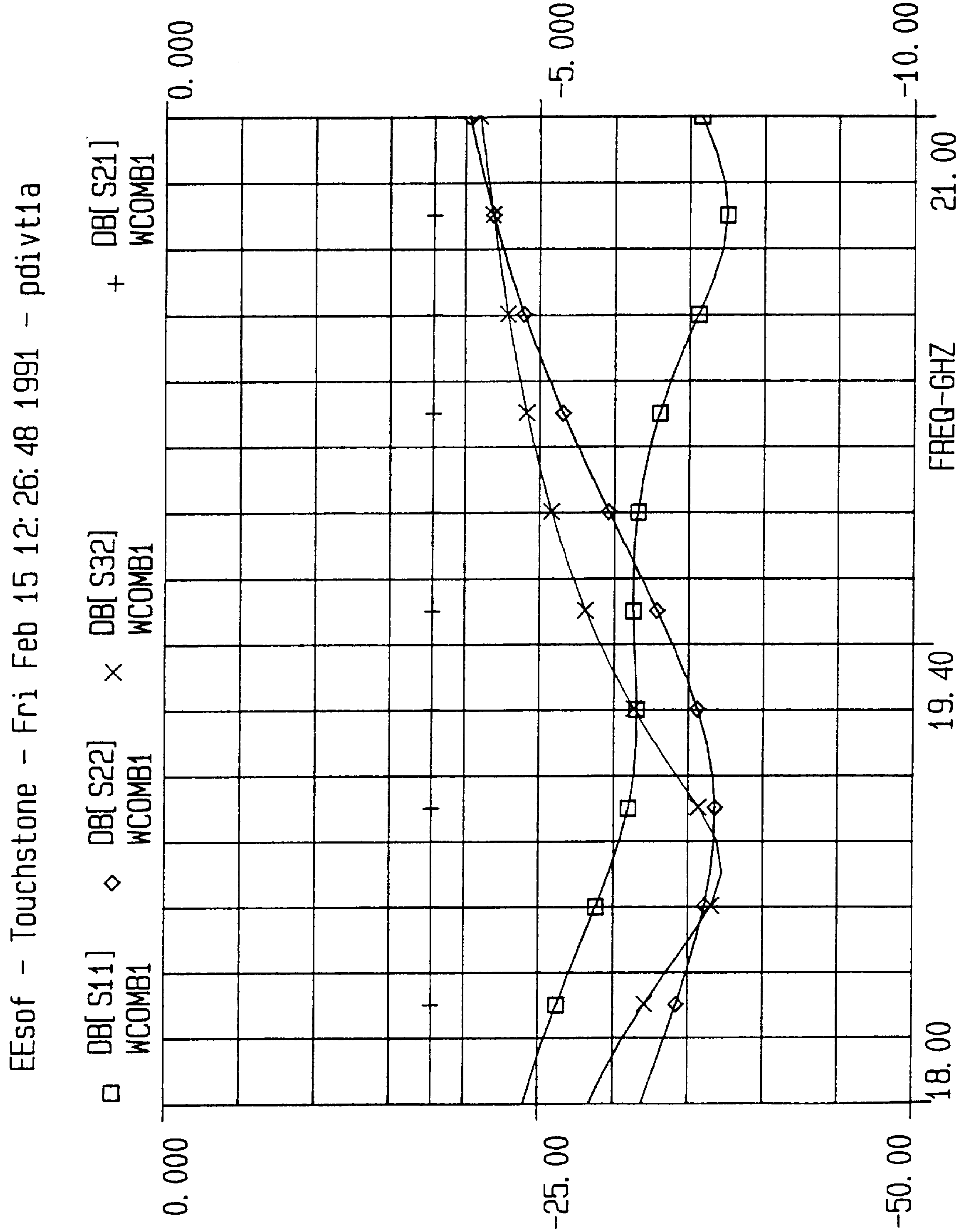

NASA TEST CIRCUIT 1
TOP SURFACE TOPOLOGY
ALUMINA
CERAMIC
0.010" THICKNESS
99.6% PURITY
GROUND PLANE ON
REVERSE SIDE
SEE DETAIL A
MICROSTRIP
SEE ATTACHED SPECIFICATION
FOR FABRICATION INSTRUCTIONS
ALL DIMENSIONS IN INCHES
DETAIL A
100 OHM
THIN FILM
RESISTOR

FIGURE 7



EEsof - Touchstone - Fri Feb 15 12:26:48 1991 - pdivt1a
DB[S11] WCOMB1
DB[S22] WCOMB1
DB[S32] WCOMB1
DB[S21] WCOMB1
0.000
-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 8

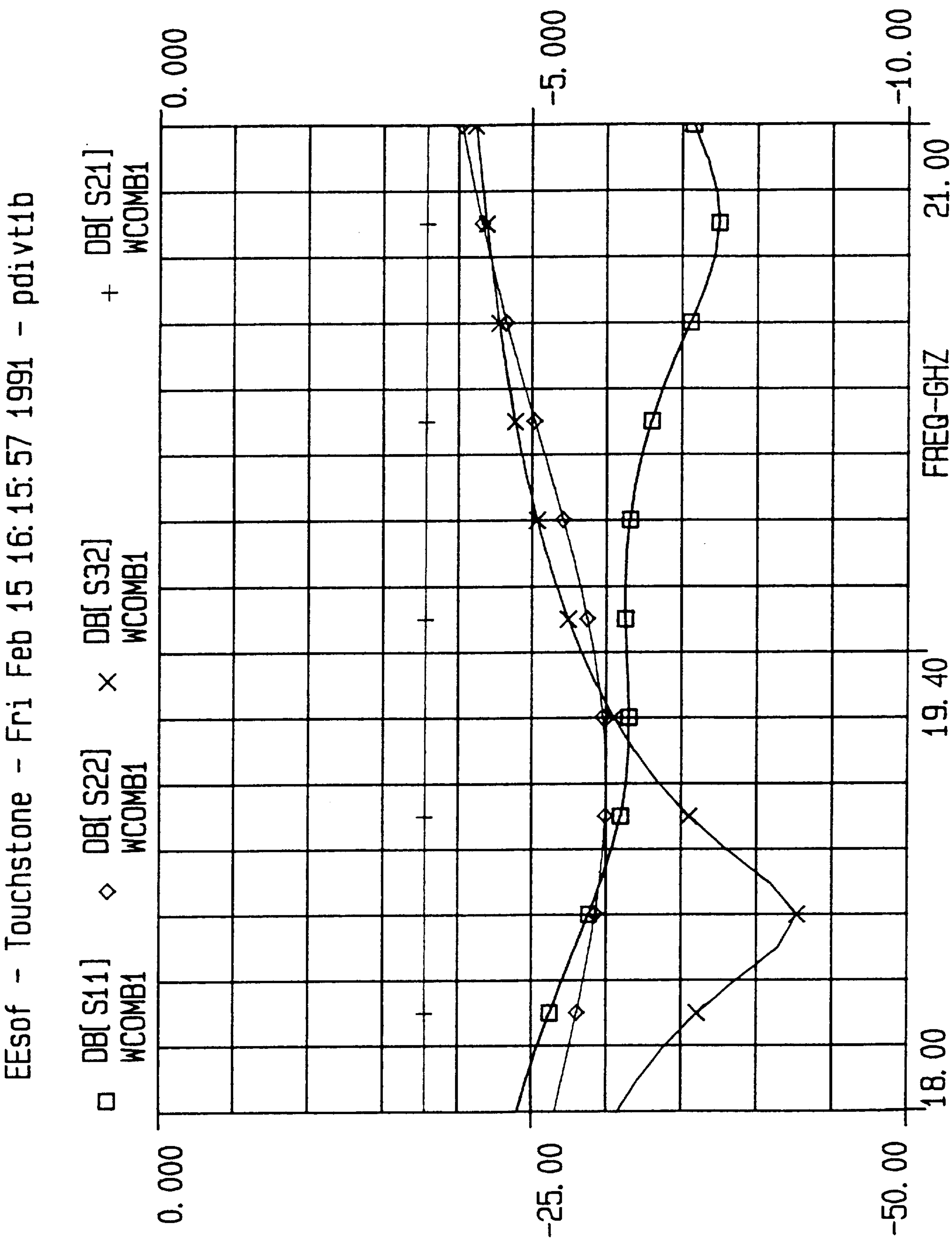

EEsof - Touchstone - Fri Feb 15 16:15:57 1991 - pdivt1b
DB[S11] WCOMB1
DB[S22] WCOMB1
DB[S32] WCOMB1
DB[S21] WCOMB1
0.000
-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 9

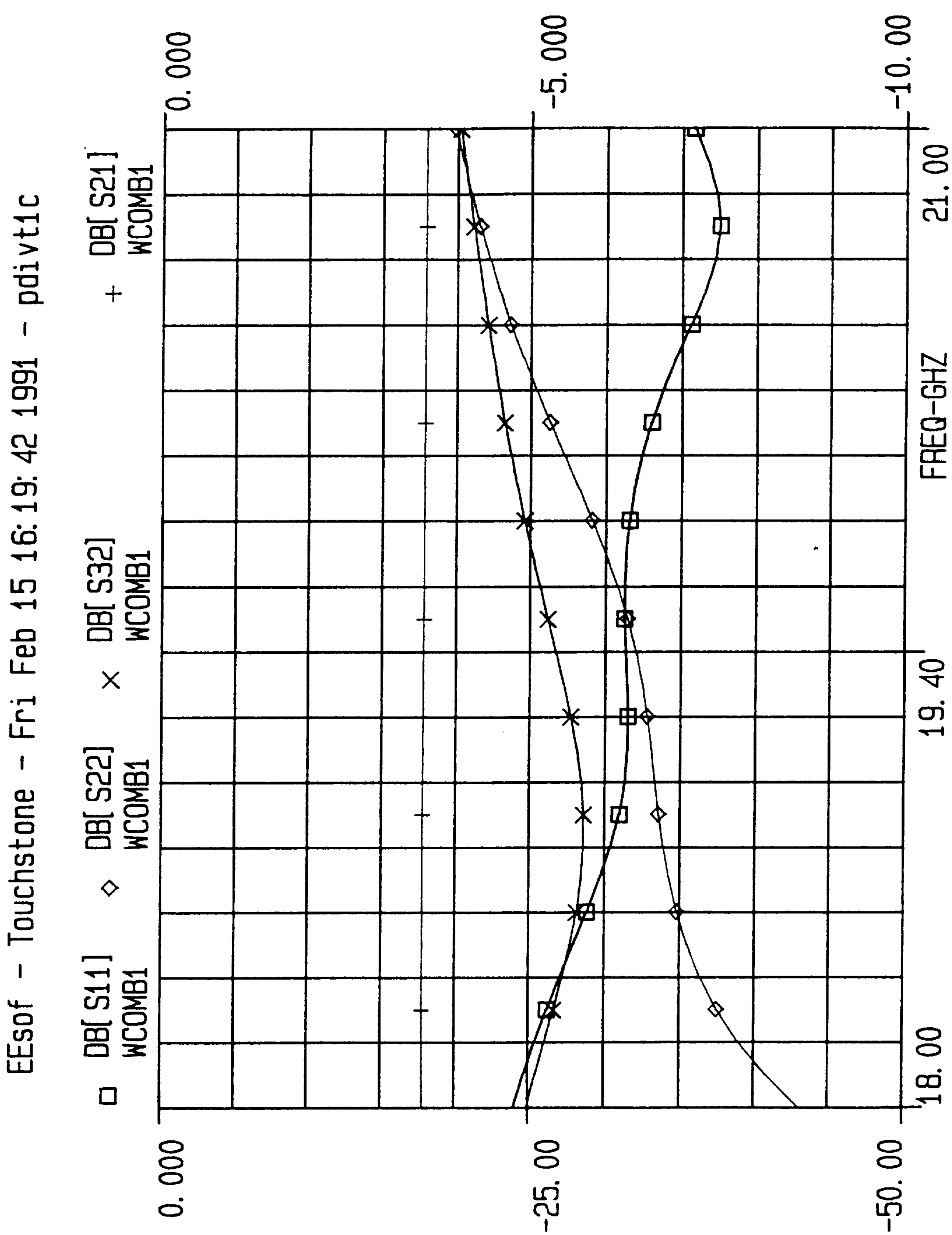

EEsof - Touchstone - Fri Feb 15 16:19:42 1991 - pdivt1c
DB[S11] WCOMB1
DB[S22] WCOMB1
DB[S32] WCOMB1
DB[S21] WCOMB1
0.000
-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 10

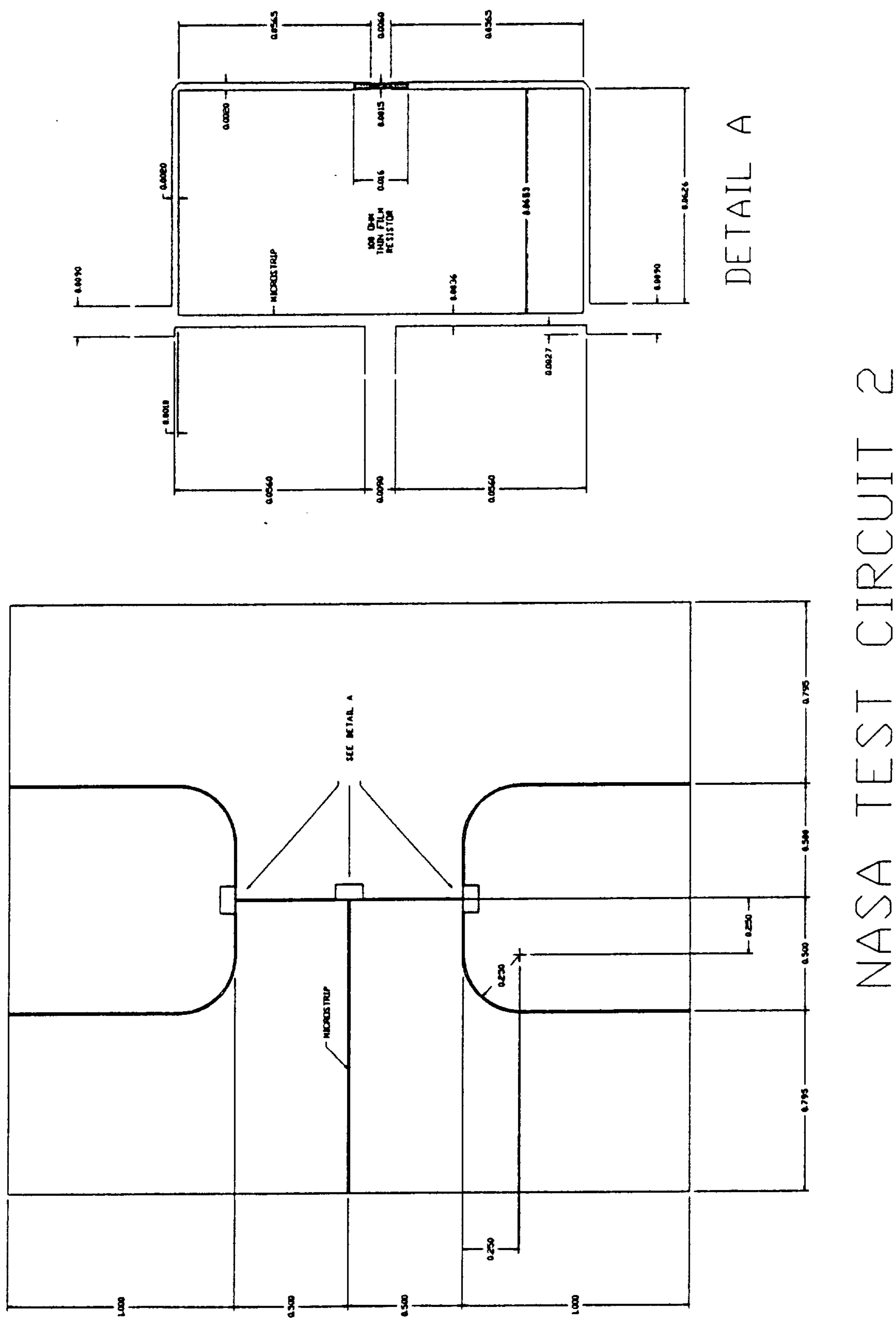
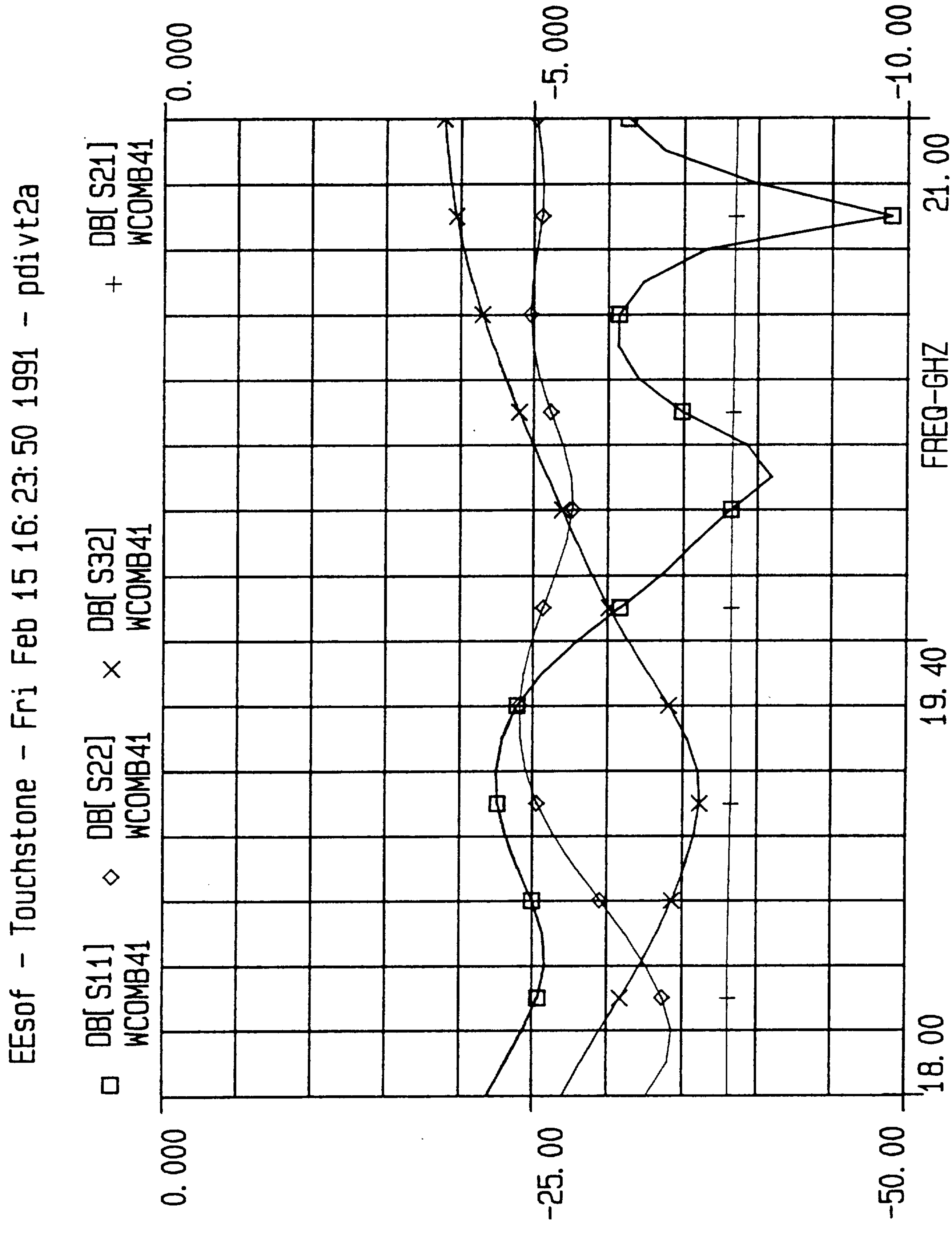

NASA TEST CIRCUIT 2
DETAIL A
SEE DETAIL A
MICROSTRIP
100 OHM THIN FILM RESISTOR

FIGURE 11


EEsof - Touchstone - Fri Feb 15 16:23:50 1991 - pdivt2a
DB[S11] WCOMB41
DB[S22] WCOMB41
DB[S32] WCOMB41
DB[S21] WCOMB41
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-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 12

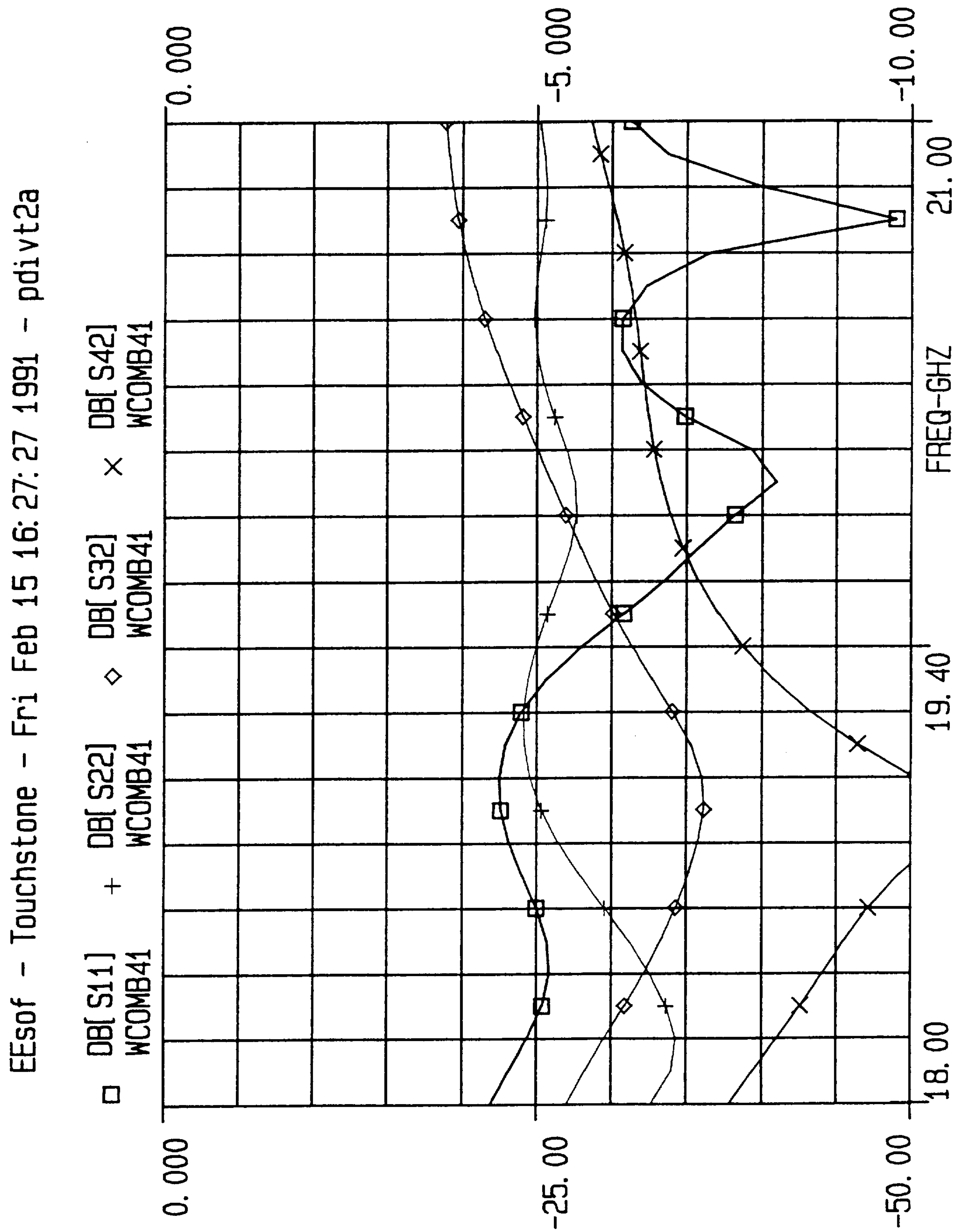

EEsof - Touchstone - Fri Feb 15 16:27:27 1991 - pdivt2a
DB[S11] WCOMB41
DB[S22] WCOMB41
DB[S32] WCOMB41
DB[S42] WCOMB41
0.000
-5.000
-10.00
0.000
-25.00
-50.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 13

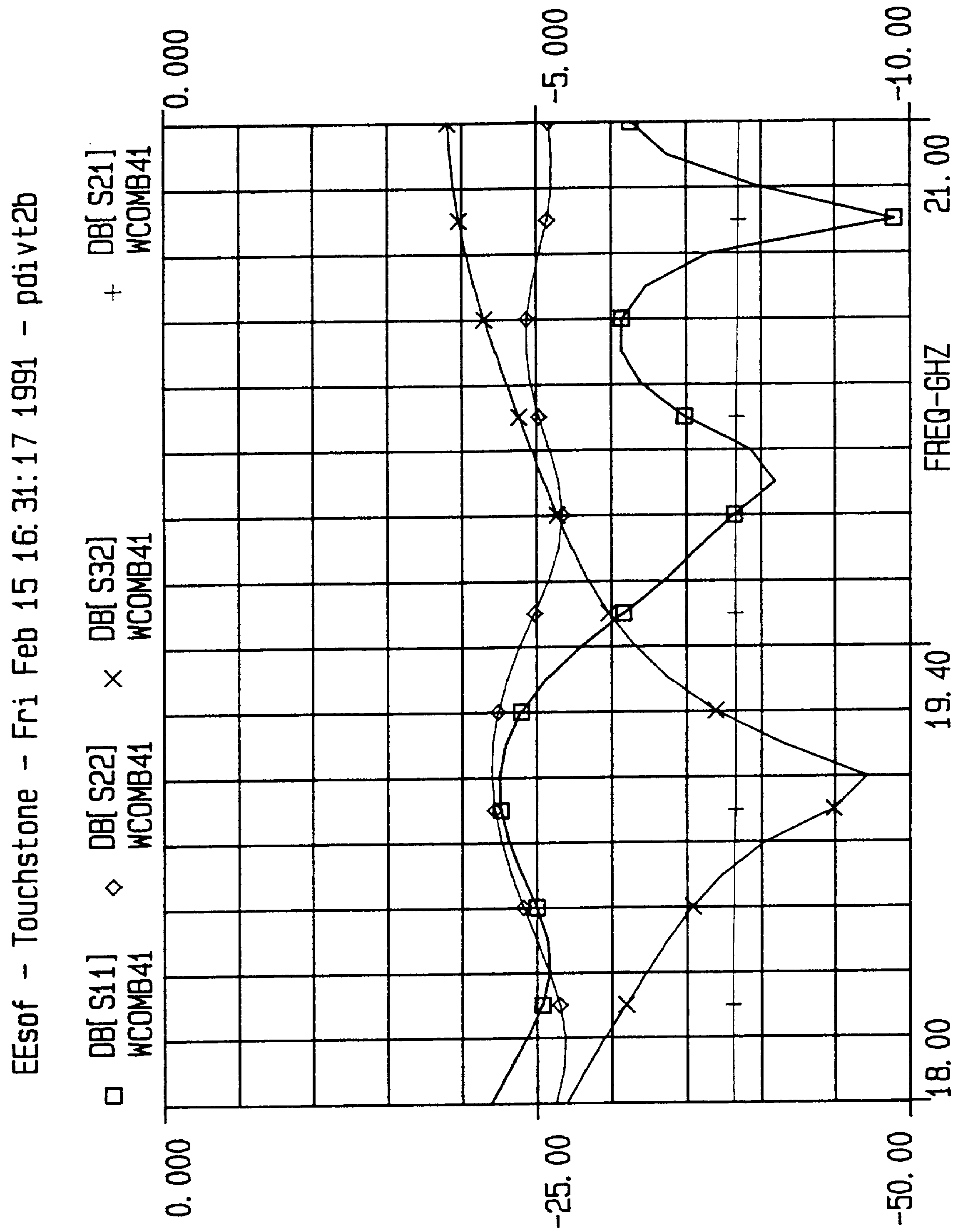
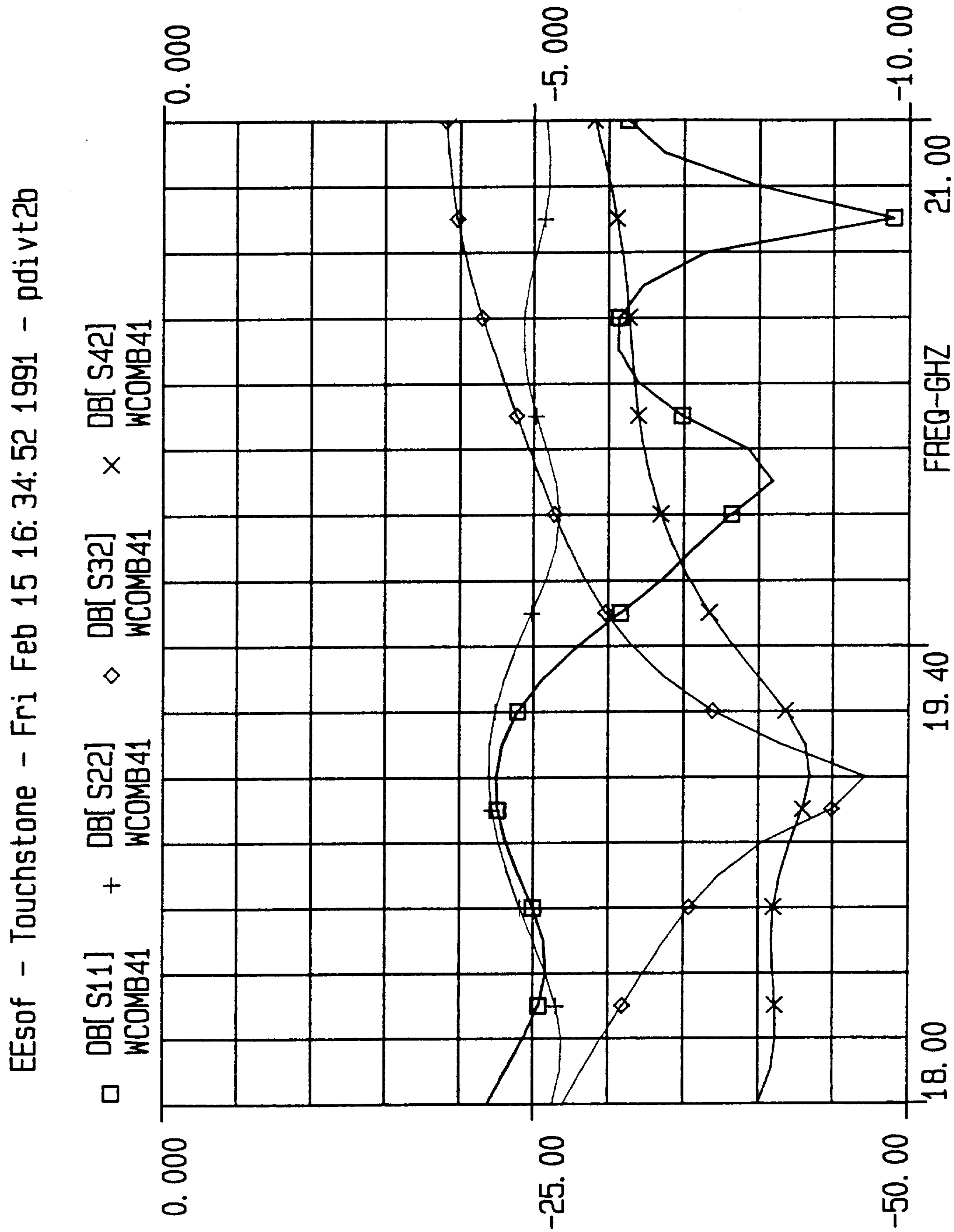

EEsof - Touchstone - Fri Feb 15 16:31:17 1991 - pdivt2b
DB[S11] WCOMB41
DB[S22] WCOMB41
DB[S32] WCOMB41
DB[S21] WCOMB41
0.000
-5.000
-10.00
0.000
-25.00
-50.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 14


EEsof - Touchstone - Fri Feb 15 16:34:52 1991 - pdivt2b
DB[S11] WCOMB41
DB[S22] WCOMB41
DB[S32] WCOMB41
DB[S42] WCOMB41
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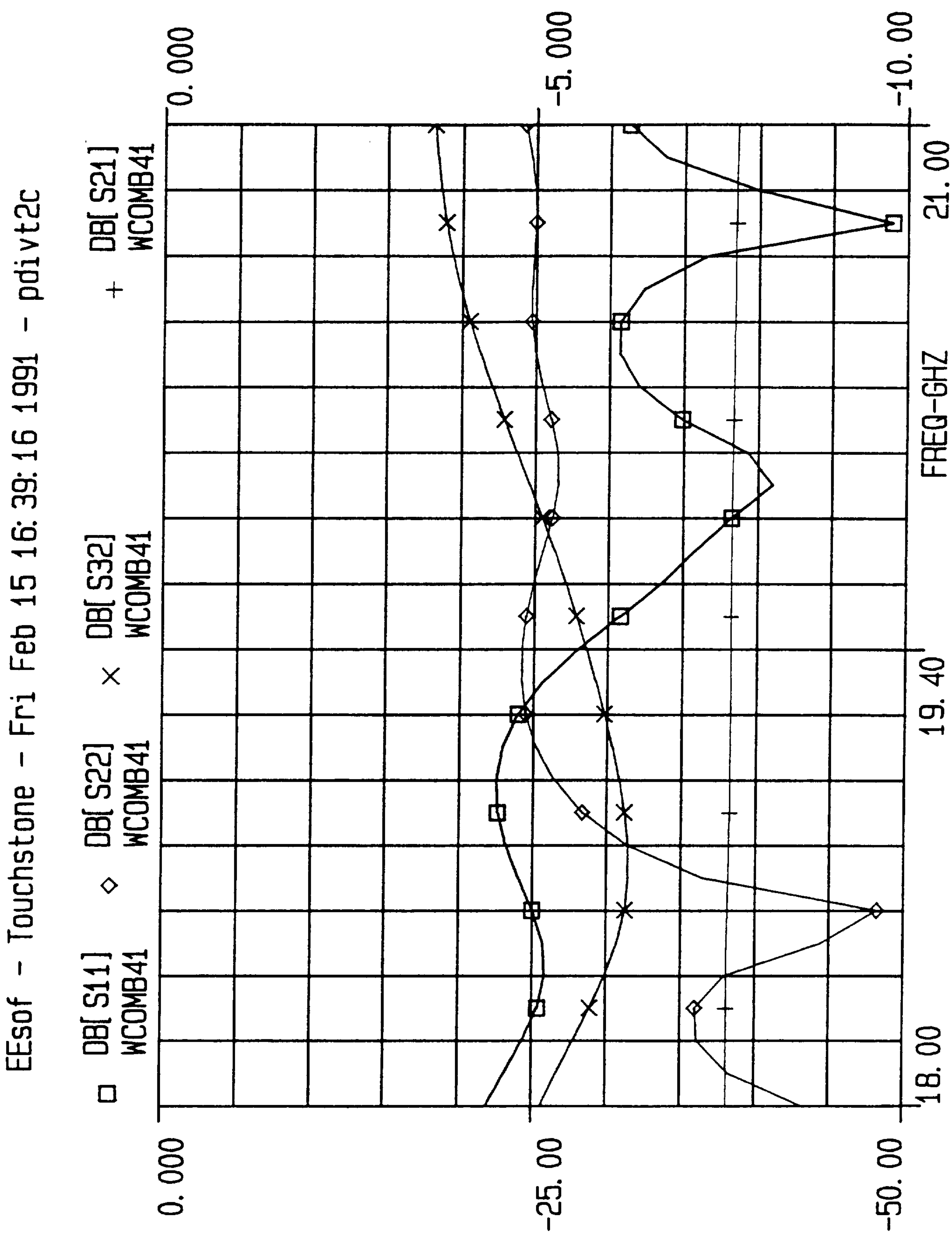
-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 15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DB[S32] WCOMB41
DB[S21] WCOMB41
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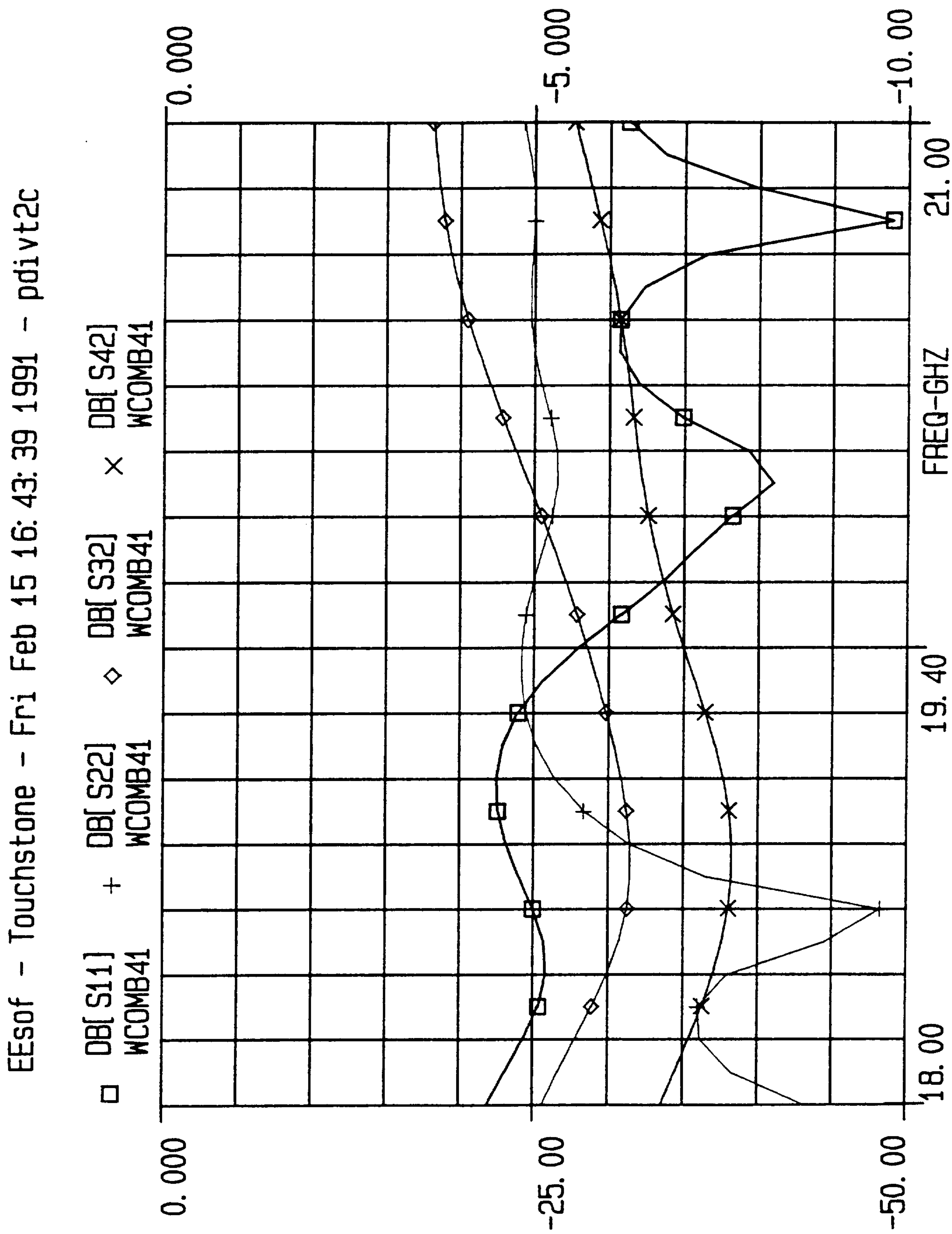
-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 16


EEsof - Touchstone - Fri Feb 15 16:43:39 1991 - pdivt2c
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DB[S22] WCOMB41
DB[S32] WCOMB41
DB[S42] WCOMB41
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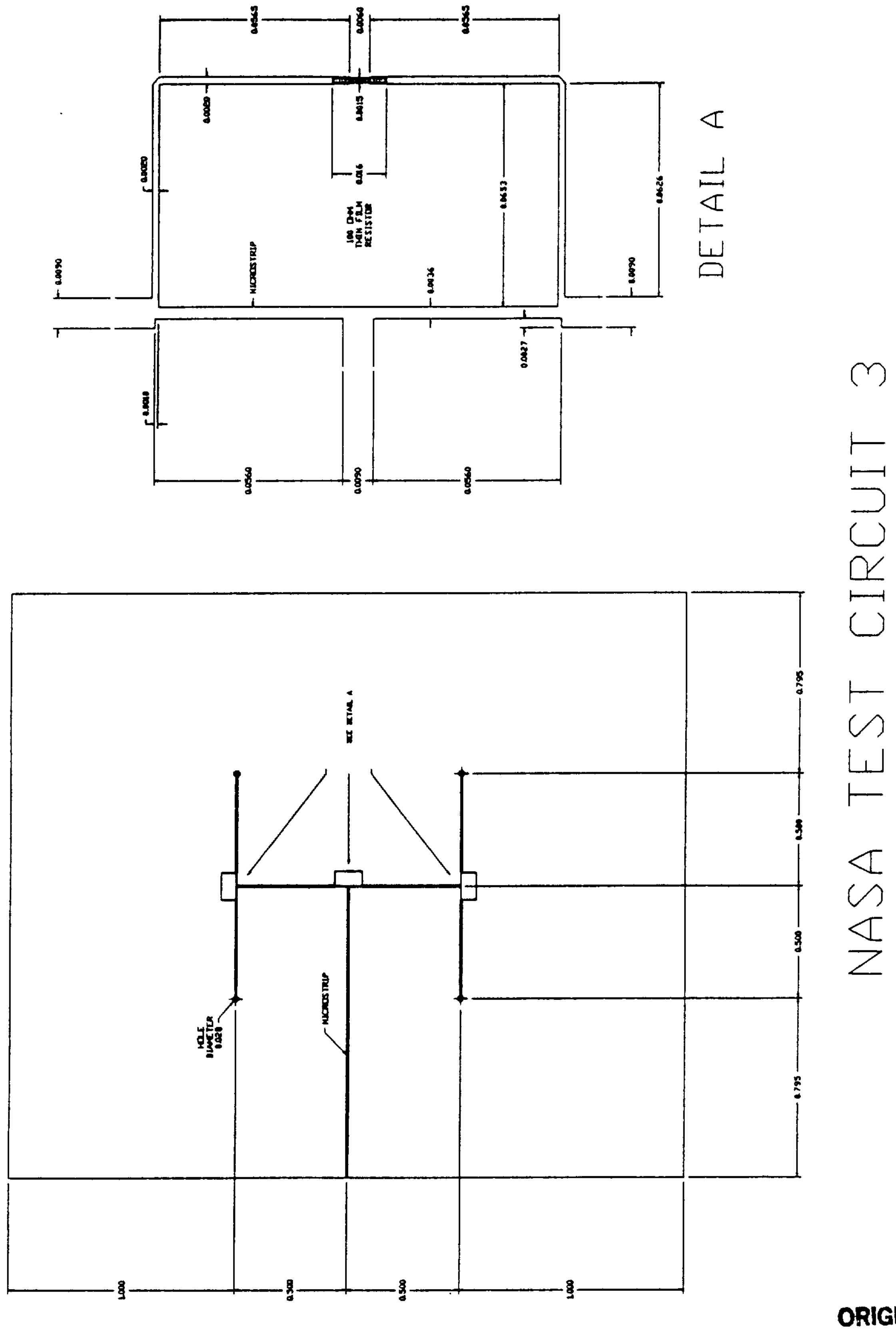
-5.000
-10.00
21.00
FREQ-GHZ
19.40
18.00
0.000
-25.00
-50.00

FIGURE 17



ORIGINAL PAGE IS
OF POOR QUALITY

FIGURE 18

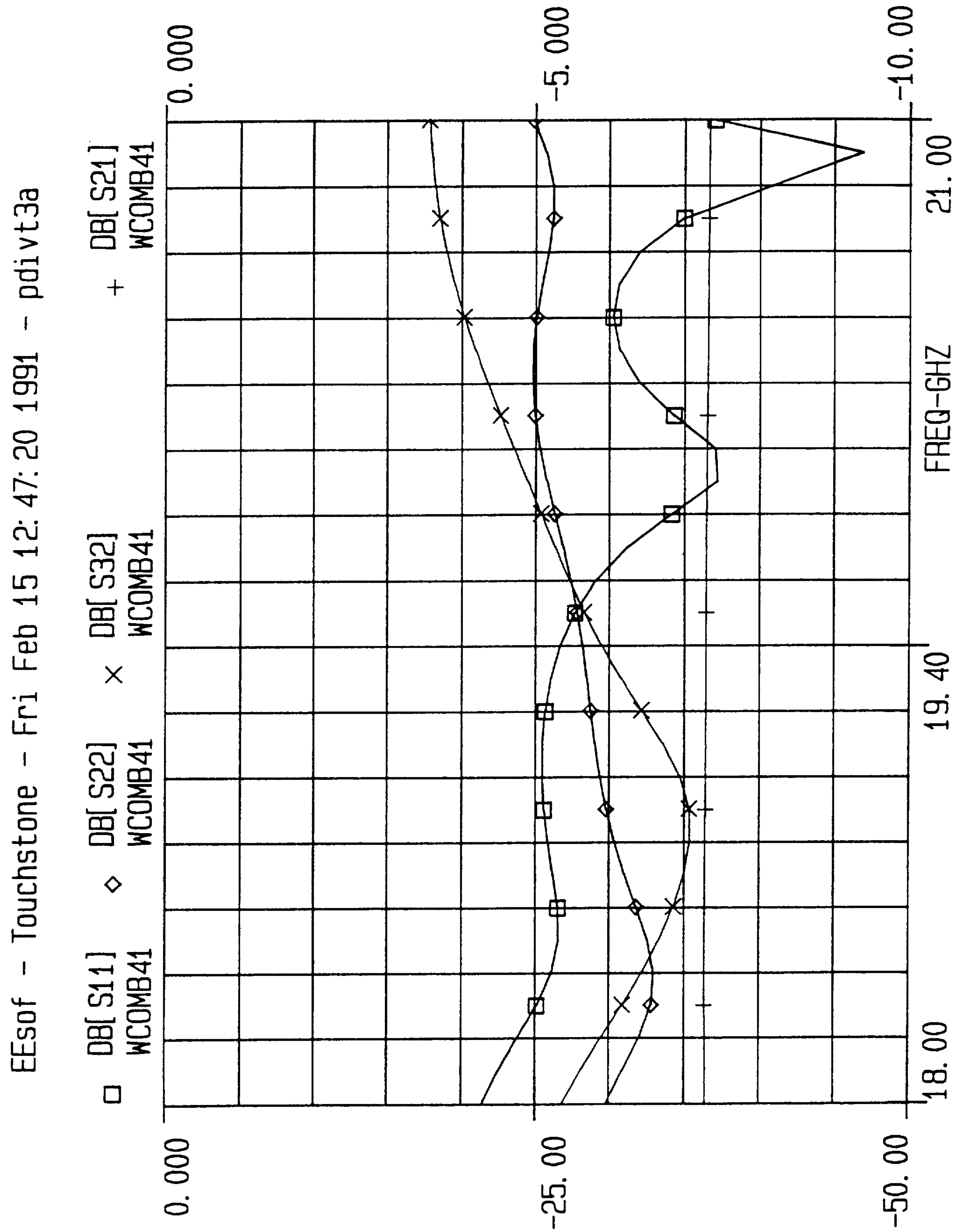

EEsof - Touchstone - Fri Feb 15 12:47:20 1991 - pdivt3a
DB[S11] WCOMB41
DB[S22] WCOMB41
DB[S32] WCOMB41
DB[S21] WCOMB41
0.000
-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 19

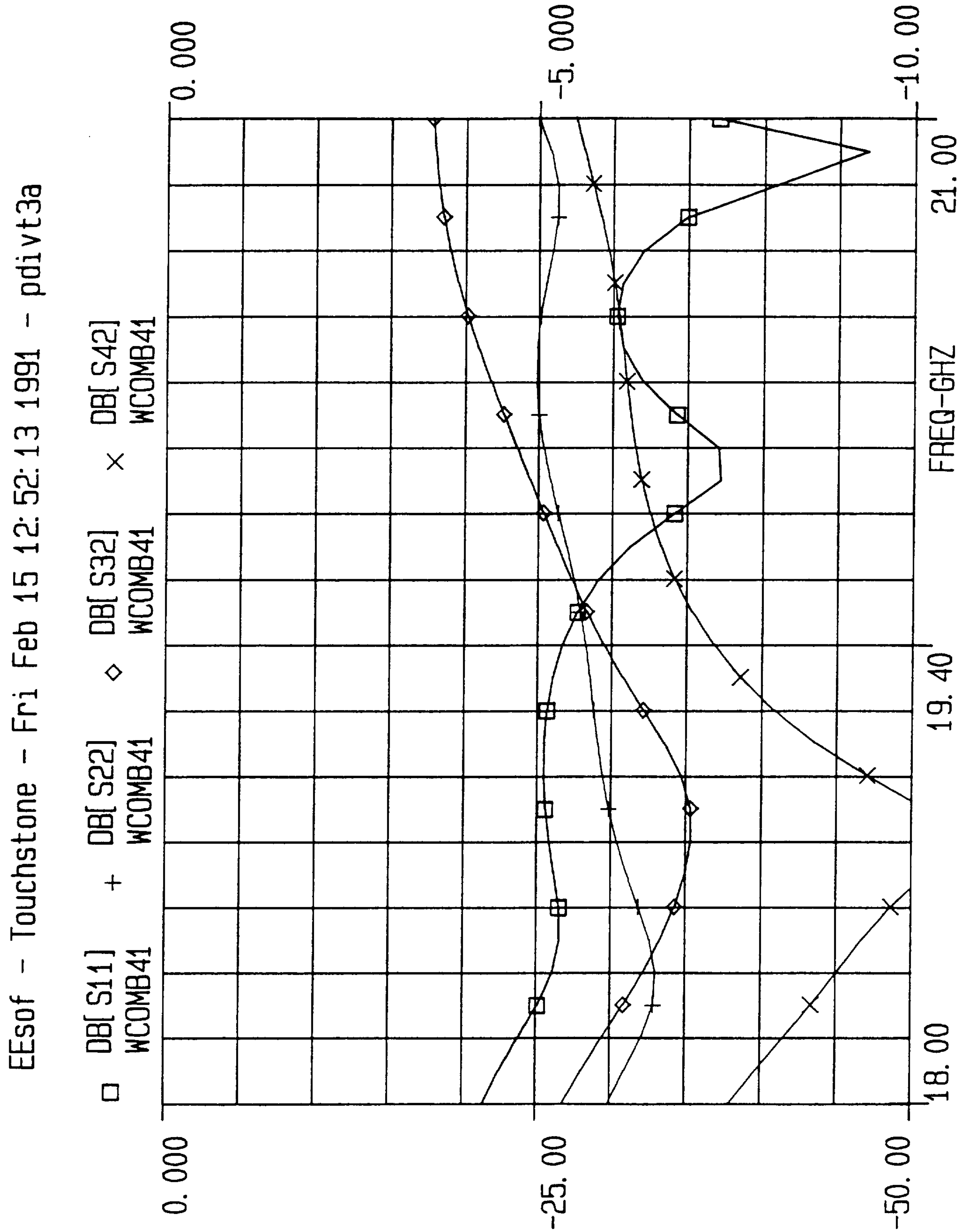

EEsof - Touchstone - Fri Feb 15 12:52:13 1991 - pdivt3a
DB[S11] WCOMB41
DB[S22] WCOMB41
DB[S32] WCOMB41
DB[S42] WCOMB41
0.000
-5.000
-10.00
0.000
-25.00
-50.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 20

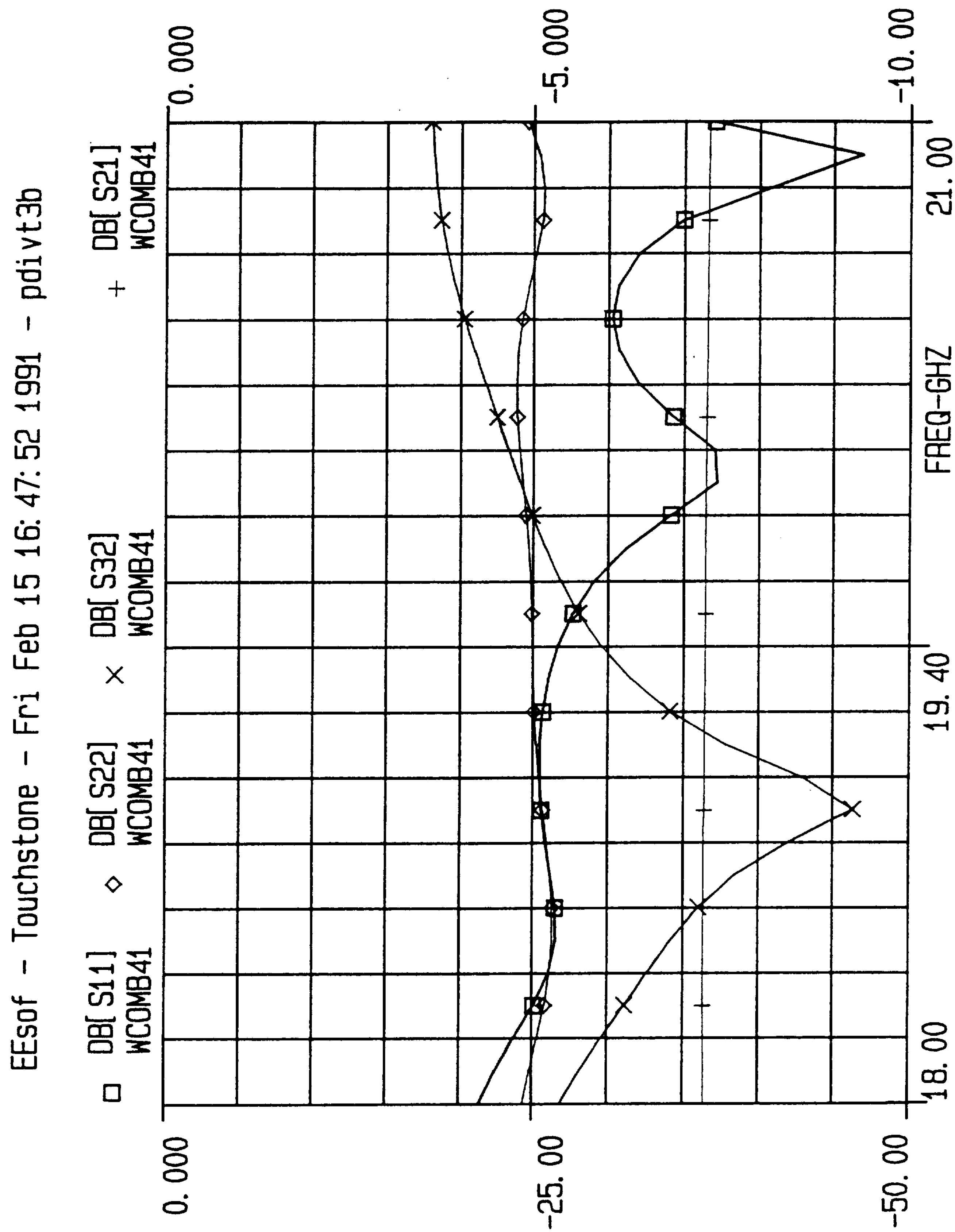
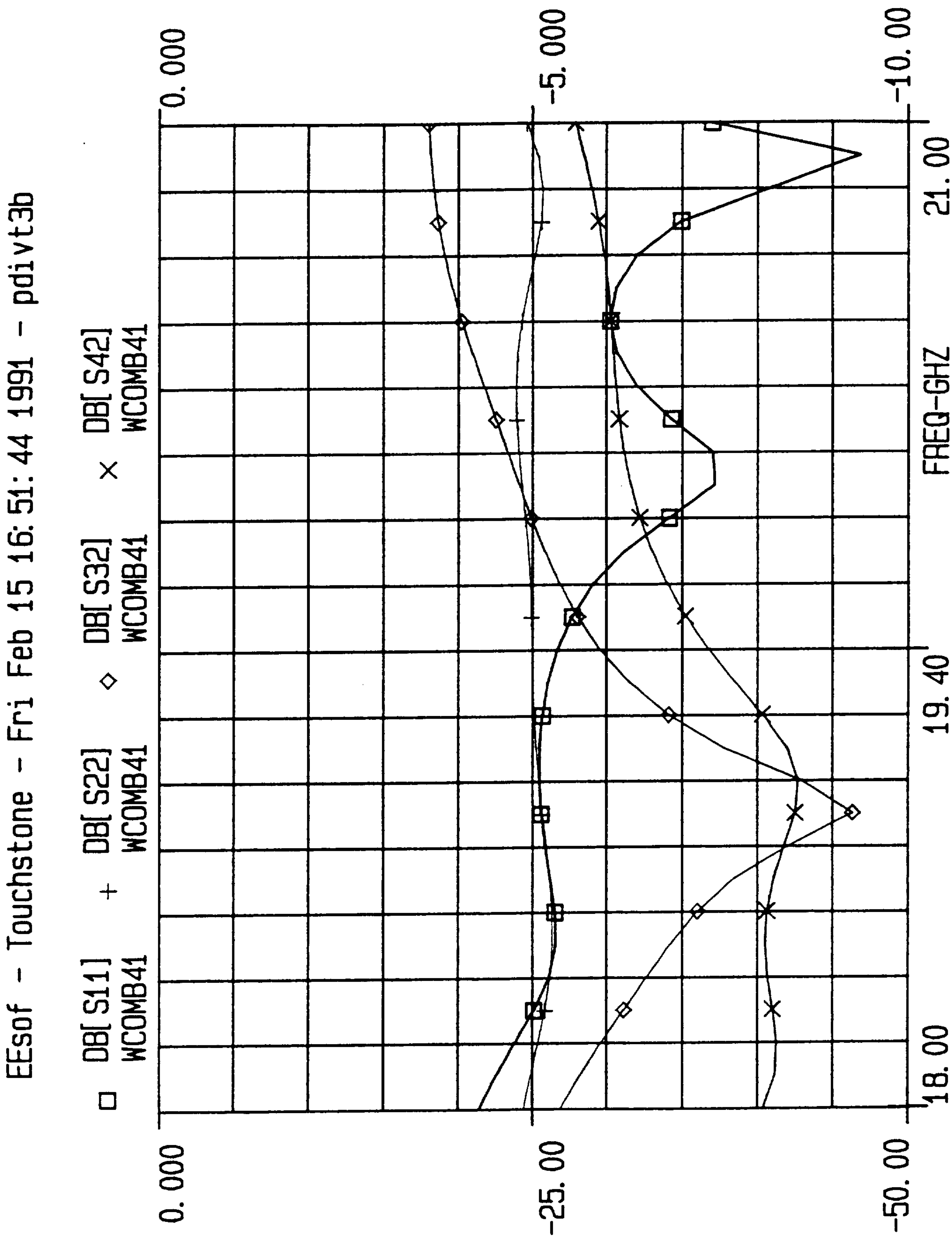
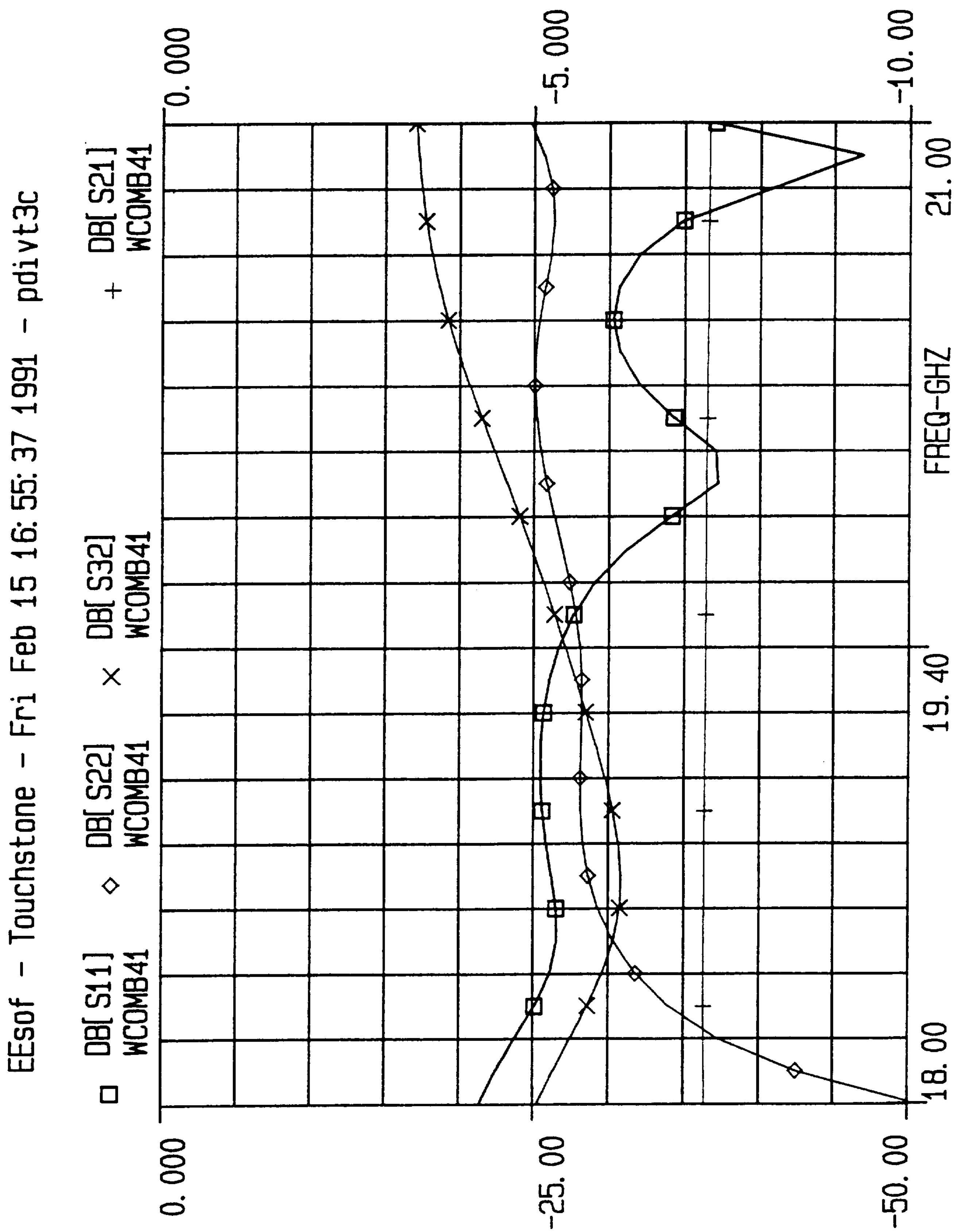

EEsof - Touchstone - Fri Feb 15 16:47:52 1991 - pdivt3b
□ DB[S11] WCOMB41
◇ DB[S22] WCOMB41
× DB[S32] WCOMB41
+ DB[S21] WCOMB41
0.000
-5.000
-10.00
0.000
-25.00
-50.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 21



EEsof - Touchstone - Fri Feb 15 16:51:44 1991 - pdivt3b
DB[S11] WCOMB41
DB[S22] WCOMB41
DB[S32] WCOMB41
DB[S42] WCOMB41
0.000
-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 22



EEsof - Touchstone - Fri Feb 15 16:55:37 1991 - pdivt3c
DB[S11] WCOMB41
DB[S22] WCOMB41
DB[S32] WCOMB41
DB[S21] WCOMB41
0.000
-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 23

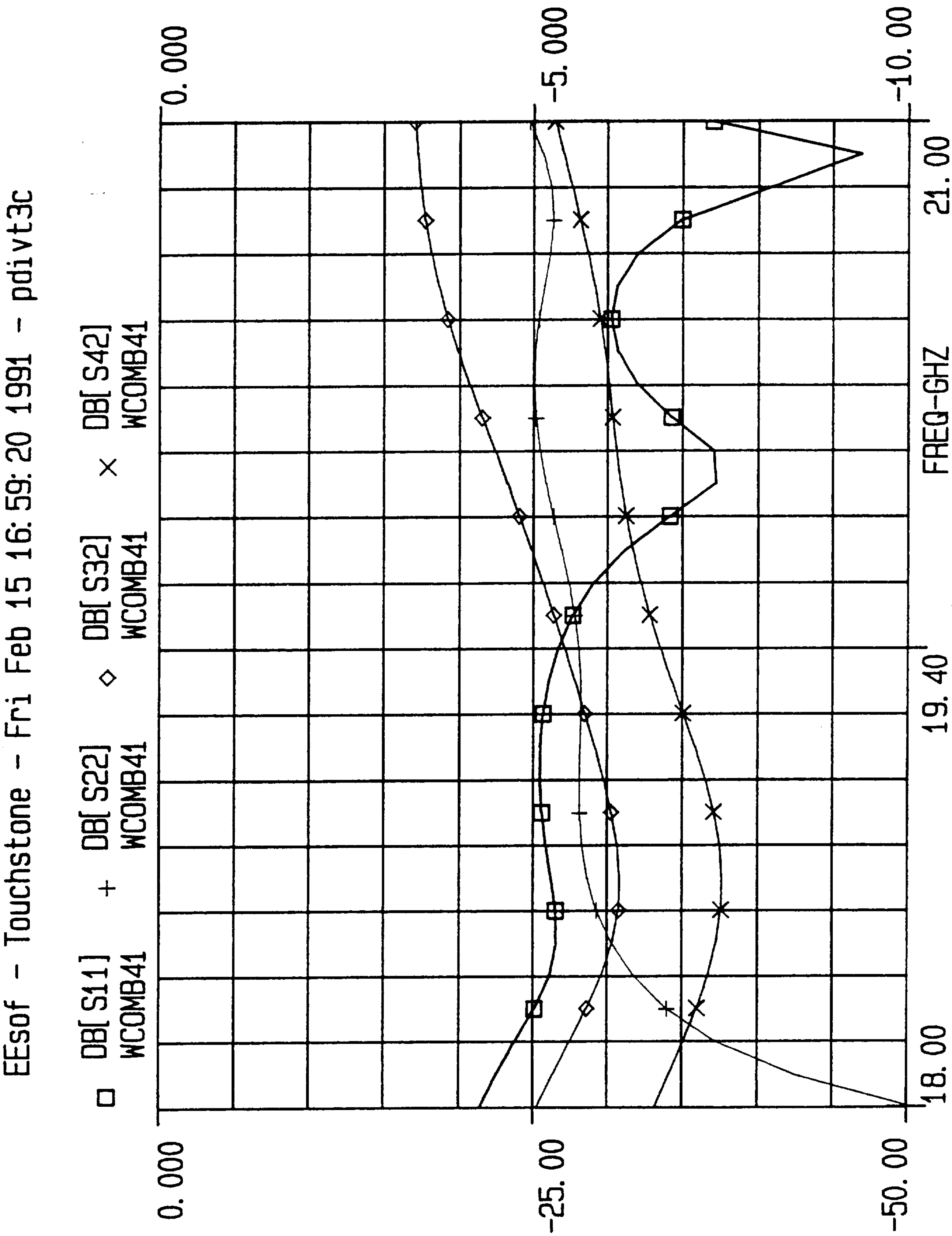
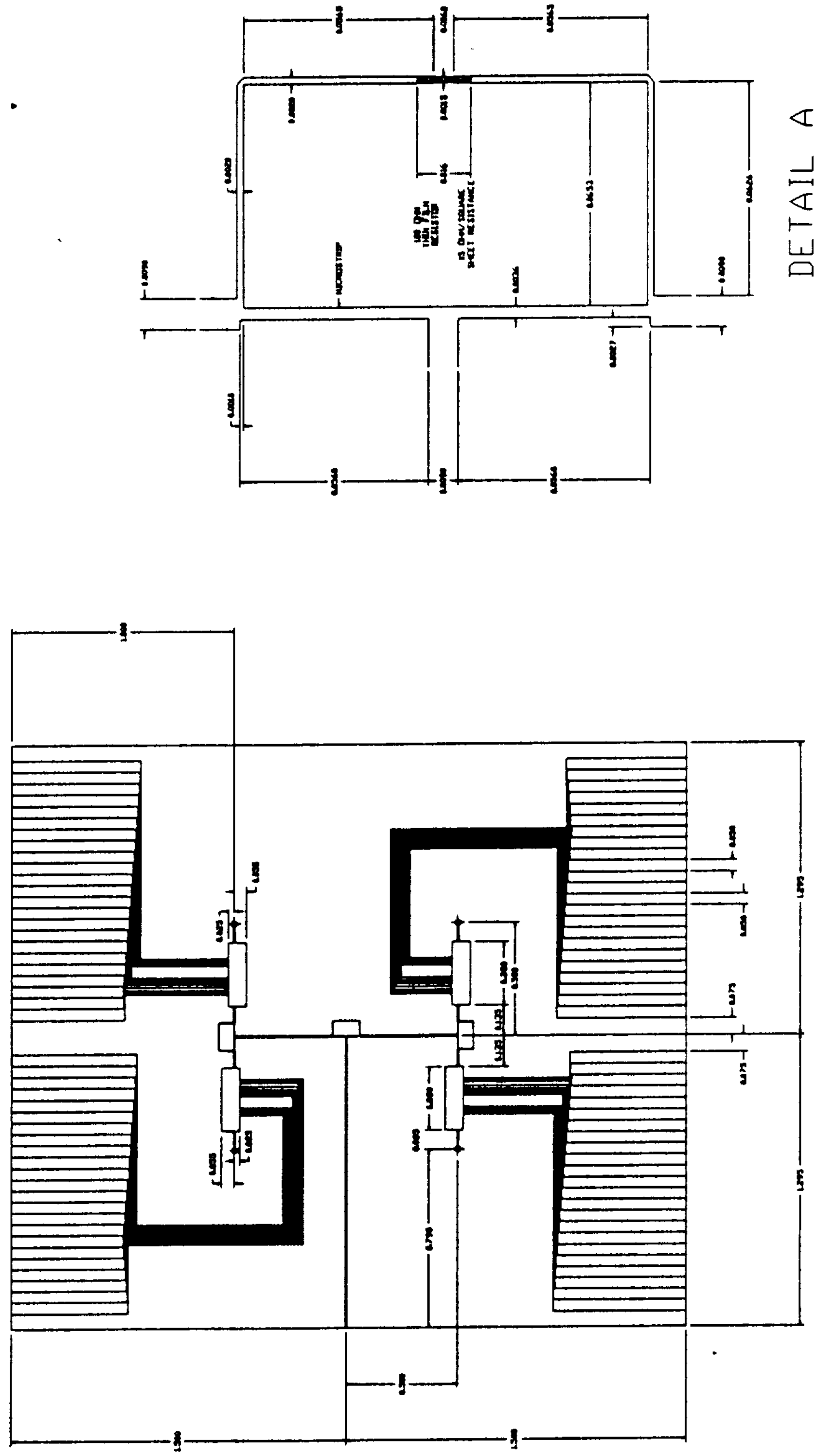

EEsof - Touchstone - Fri Feb 15 16:59:20 1991 - pdivt3c
DB[S11] WCOMB41
DB[S22] WCOMB41
DB[S32] WCOMB41
DB[S42] WCOMB41
0.000
-25.00
-50.00
0.000
-5.000
-10.00
18.00
19.40
21.00
FREQ-GHZ

FIGURE 24



ORIGINAL PAGE IS OF POOR QUALITY

FIGURE 25

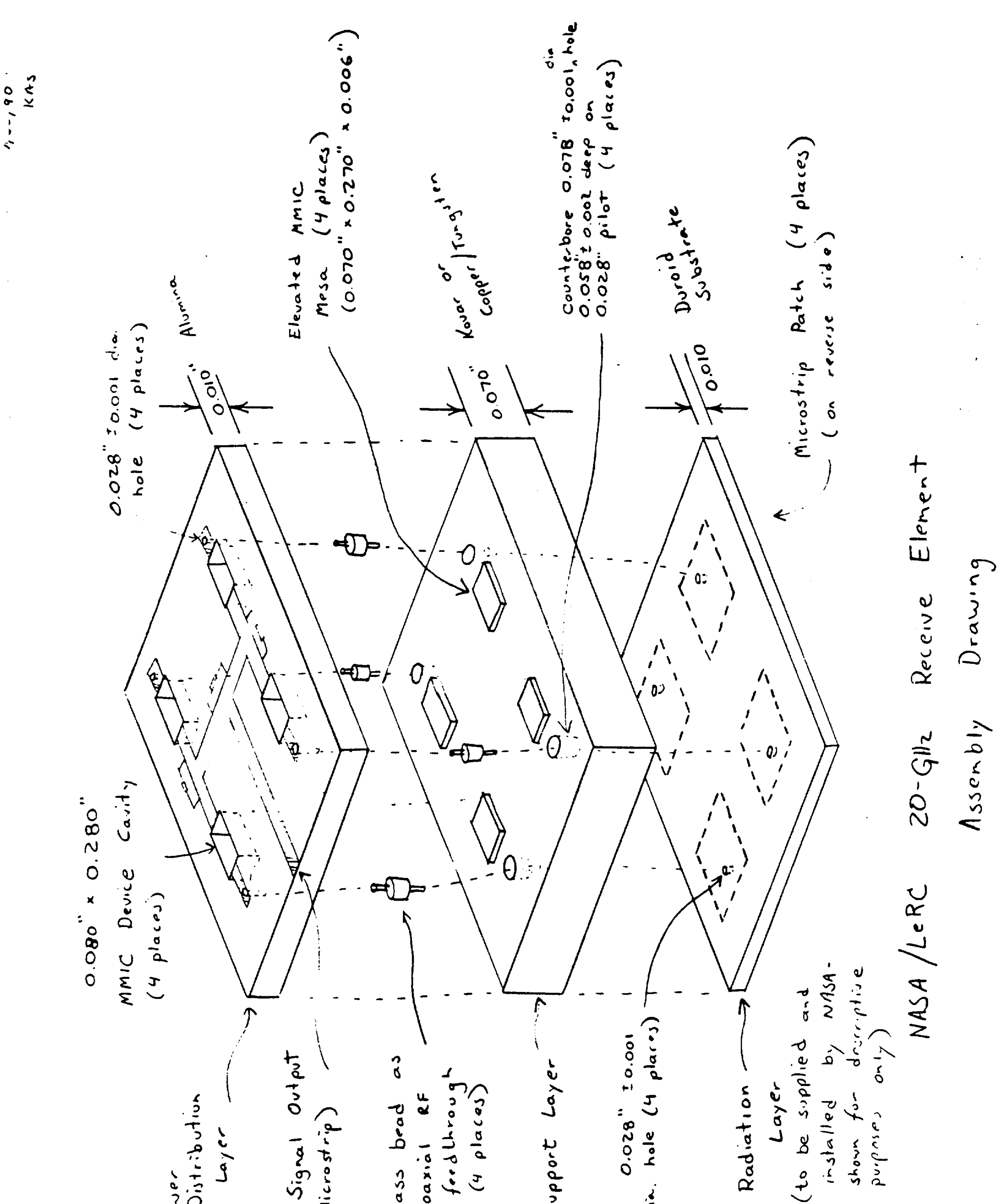

0.080" × 0.280"
MMIC Device Cavity
(4 places)
0.028" ±0.001 dia. hole (4 places)
0.010"
Alumina
Elevated MMIC Mesa (4 places)
(0.070" × 0.270" × 0.006")
0.070"
Kovar or Copper/Tungsten
Counterbore 0.078" ±0.001 dia hole
0.058" ±0.002 deep on
0.028" pilot (4 places)
Duroid Substrate
0.010
Microstrip Patch (4 places)
(on reverse side)
Power Distribution Layer
RF Signal Output (Microstrip)
Glass bead as coaxial RF feedthrough (4 places)
Support Layer
0.028" ±0.001 dia. hole (4 places)
Radiation Layer
(to be supplied and installed by NASA-shown for descriptive purposes only)
NASA/LeRC 20-GHz Receive Element
Assembly Drawing

FIGURE 26

```
Touchstone Sr. (TM) Ver. 2.100.108.2  Config. (100 20936 5 5100923E 8015 0 4319E)
            pdivtla.ckt    Fri Feb  8 16:32:13 1991

!
!       File: pdivtla.ckt
!       Mike Biedenbender 2/8/91
!       description:  Touchstone simulation for Test Circuit 1
!        2:1 Wilkinson power combiner designed for 20 GHz
!        99.6% purity alumina
!        No laser trimming of the thin film isolation resistor
!        Simulation for nominal 25 ohm/square sheet resistance to
!        provide 100 ohm isolation resistor
!
!                  !Default Units
dim
  freq ghz
  res oh
  ind nh
  cap pf
  lng mil
  time ps
  cond /oh
  ang deg
!
!                  !Define variables for microstrip widths and lengths
!
var
  w50=9.00         !50 ohm transmission line width
  wl4=3.60         !sqrt(2)*50 ohm transmission line width
  wl2r=2.00        !minimum width allowed for half-wave lines to isolation resistor
!
  wltfrl=1.5       !actual width of the thin film isolation resistor
!
  wltfr2=1.5       !nominal width of the thin film isolation resistor
  ll4=55           !length of the quarter-wave sqrt(2)*50 ohm trans. line
  ll2ra=62.6       !length of the trans. line perpendicular to the thin film res
  rsa=25           !nominal sheet resistance of the thin film resistor
  rsal=25          !actual sheet resistance of the thin film resistor
!
!                  !Define equations to determine additional trans line lengths,
!                  !length of thin film resistor
!
eqn
  ll2rc=(100*wltfr2)/rsa        !length of the thin film resistor
!
! wltfrl=wltfr2*rsal/rsa        !determines the length of the thin film
!                               !resistor if laser trimming is used
!
  ll2rb=(w50/2) + ll4 - ((50*wltfr2)/rsa)      !trans line length to tfr
!
!
ckt
!
!                  !Define dielectric and conductor parameters
!
  msub er=9.9 h=10 t=0.06 rho=1 rgh=0
  tand tand=0.0002
```

```
!

Touchstone Sr. (TM) Ver. 2.100.108.2  Config. (100 20936 5 5100923E 8015 0 4319E)
              pdivtla.ckt    Fri Feb  8 16:32:13 1991

!               !Define Test Circuit 1  -  wcombl
!
  mlin 1 6 w^w50 l=498.2          !trans line from combiner output to edge of
!                                 !Test Circuit 1
  mlin 3 8 w^w50 l=438.5          !trans line from combiner input to edge
  mlin 2 13 w^w50 l=438.5         !trans line from combiner input to edge
  mtee 4 5 6 w1^wl4 w2^wl4 w3^w50
  mlin 4 7 w^wl4 l^ll4            !quarter wave trans line
  mlin 5 14 w^wl4 l^ll4           !quarter wave trans line
  mtee 7 8 9 w1^wl4 w2^w50 w3^wl2r
  mtee 13 14 15 w1^w50 w2^wl4 w3^wl2r
  mlin 9 10 w^wl2r l^ll2ra        !trans line perpendicular to isolation tfr
  mlin 15 16 w^wl2r l^ll2ra       !trans line perpendicular to isolation tfr
!
  mbend2 10 11 w^wl2r
  mbend2 16 17 w^wl2r
!
  mlin 11 12 w^wl2r l^ll2rb       !trans line connected to isolation tfr
  mlin 17 18 w^wl2r l^ll2rb       !trans line connected to isolation tfr
!
  tfr 12 18 w^wltfrl l^ll2rc rs^rsal f=0        !thin film isolation resistor
!
  def3p 1 2 3 wcombl    !end of definition for Test Circuit 1
!
!               !Specify output parameters to determine
!
out
  wcombl db[s11] grl
  wcombl db[s21] grla
  wcombl db[s22] grl
  wcombl db[s32] grl
!
!               !Define frequency range for sweeping and optimization
!
freq
  sweep 18 21 0.1
!
!               !Define grids for display
!
grid
  range 18 21 0.2
  grl -50 0 5
  grla -10 0 1
!
!               !Optimization used to determine quarter-wave transmission line
!               !length and width, length of isolation trans lines
!               !To optimize, wl4, ll4, and ll2ra must be made variable
!               !Example: change ll4=55 to ll4 # 40 55 80
!
opt
  range 18 21
  wcombl db[s22] < -15 1
  wcombl db[s32] < -15 1
  wcombl db[s12] > -3.2 1
```

```
Touchstone Sr. (TM) Ver. 2.100.108.2  Config. (100 20936 5 5100923E 8015 0 4319E)
             pdivt2a.ckt    Fri Feb 15 15:01:50 1991

!       FILE:PDIVT2A.CKT
!       Mike Biedenbender 2/12/91
!       description:    Touchstone simulation for Test Circuit 2
!        4:1 power combiner for 4 element array without RADC 20 GHz MMICs
!        2:1 Wilkinson power combiner designed for 20 GHz
!        Input microstrip lines extend to edge of substrate to measure
!        characteristics of 4:1 combiner
!        99.6% purity alumina
!        No laser triming of the thin film isolation resistor
!        Simulation for nominal 25 ohm/square sheet resistance to
!        provide 100 ohm isolation resistor
!
!               !Default units
DIM
  FREQ GHZ
  RES OH
  IND NH
  CAP PF
  LNG MIL
  TIME PS
  COND /OH
  ANG DEG
!
!               !Define variables for microstrip widths and lengths
!
VAR
!
  W50=9.00      !50 ohm transmission line width
  WL4=3.60      !sqrt(2)*50 ohm transmission line width
  WL2R=2        !minimum width alowed for half-wave lines to isolation resistor
!
  WLTFR1 #0.1 1.5 3                  !WIDTH USED IN ACTUAL RESISTOR
!
  WLTFR2=1.5    !nominal width of the thin film isolation resistor
  LL4=55        !length of the quarter-wave sqrt(2)*50ohm trans line
  LL2RA=62.6    !length of the trans line perpendicular to the thin film res
  RSA=25        !nominal sheet resistance of the thin film resistor
  RSA1=25       !actual sheet resistance of the thin film resistor
!
!               !Define equations to determine additional trans line lengths,
!               !length of thin film resistor
!
EQN
  LL2RC=(100*WLTFR2)/RSA        !length of the thin filmn resistor
!
! WLTFR1=WLTFR2*RSA1/RSA        !determines the width of the thin film
!                               !resistor if laser trimming is used
!
  LL2RB=(W50/2) + LL4 - ((50*WLTFR2)/RSA)       !trans line length to tfr
!
!
CKT
!
!               !Define dielectric and conductor parameters
```

```
MSUB ER=9.9 H=10 T=0.1 RHO=1 RGH=0


Touchstone Sr. (TM) Ver. 2.100.108.2  Config. (100 20936 5 5100923E 8015 0 4319E)
            pdivt2a.ckt    Fri Feb 15 15:01:50 1991

 TAND TAND=0.0002
!
!              !Define Test Circuit 2  -  wcomb
!
 MTEE 4 5 1 W1^WL4 W2^WL4 W3^W50
 MLIN 4 7 W^WL4 L^LL4           !quarter wave trans line
 MLIN 5 14 W^WL4 L^LL4          !quarter wave trans line
 MTEE 7 3 9 W1^WL4 W2^W50 W3^WL2R
 MTEE 2 14 15 W1^W50 W2^WL4 W3^WL2R
 MLIN 9 10 W^WL2R L^LL2RA       !trans line perpendicular to isolation tfr
 MLIN 15 16 W^WL2R L^LL2RA      !trans line perpendicular to isolation tfr
!
 MBEND2 10 11 W^WL2R
 MBEND2 16 17 W^WL2R
!
 MLIN 11 12 W^WL2R L^LL2RB      !trans line connected to isolation tfr
 MLIN 17 18 W^WL2R L^LL2RB      !trans line connected to isolation tfr
!
 TFR 12 18 W^WLTFR1 L^LL2RC RS^RSA1 F=0       !thin film isolation resistor
!
 DEF3P 1 2 3 WCOMB              !End of definition for Wilkinson power combiner
!
!
 MLIN 100 110 W^W50 L=1293.8    !Trans line from output combiner output to
!                               !edge of Test Circuit 2
 WCOMB 110 111 112              !Output 2:1 power combiner
 MLIN 111 120 W^W50 L=436.7     !Trans line from output combiner input to
!                               !input combiner output
 MLIN 112 130 W^W50 L=436.7     !Trans line from output combiner input to
!                               !input combiner output
 WCOMB 120 121 125              !Input 2:1 power combiner
 WCOMB 130 131 135              !Input 2:1 power combiner
!
 MLIN 121 122 W^W50 L=188.5             !Trans lines and curve from
 MCURVE 122 123 W^W50 ANG=90 RAD=250    !input power combiner to edge of
 MLIN 123 101 W^W50 L=750               !Test Circuit 2
!
 MLIN 125 126 W^W50 L=188.5             !Trans lines and curve from
 MCURVE 126 127 W^W50 ANG=-90 RAD=250   !input power combiner to edge of
 MLIN 127 102 W^W50 L=750               !Test Circuit 2
!
 MLIN 131 132 W^W50 L=188.5             !Trans lines and curve from
 MCURVE 132 133 W^W50 ANG=90 RAD=250    !input power combiner to edge of
 MLIN 133 103 W^W50 L=750               !Test Circuit 2
!
 MLIN 135 136 W^W50 L=188.5             !Trans lines and curve from
 MCURVE 136 137 W^W50 ANG=-90 RAD=250   !input power combiner to edge of
 MLIN 137 104 W^W50 L=750               !Test Circuit 2
!
 DEF5P 100 101 102 103 104 WCOMB41A     !Define 5 port combiner
!                                       !End of definition for Test Circuit 2
!
 WCOMB41A 200 201 202 203 204   !Retrieve 5 port combiner
 RES 204 0 R=50                 !Terminate a port to make 4 port network
```

```
!                                !to allow Touchstone output calculation


Touchstone Sr. (TM) Ver. 2.100.108.2  Config. (100 20936 5 5100923E 8015 0 4319E)
             pdivt2a.ckt    Fri Feb 15 15:01:50 1991

  DEF4P 200 201 202 203 WCOMB41 !Define 4 port from 4-way combiner
!
!               !Specify output parameters to determine
!
OUT
  WCOMB41 DB[S11] GR1            !Return loss at output combiner output
  WCOMB41 DB[S21] GR1A           !Insertion loss thru 2 Wilkinson combiners
  WCOMB41 DB[S22] GR1            !Return loss at any input port
  WCOMB41 DB[S32] GR1            !Isolation between inputs of same input combiner
  WCOMB41 DB[S42] GR1            !Isolation between inputs of different input
!                                !combiners
!
!               !Define frequency range for sweeping and optimization
!
FREQ
  SWEEP  18 21 0.1               !Center frequency of design is 19.7 GHz
!
!               !Define grids for display
GRID
  RANGE 18 21 0.2
  GR1 -50 0 5
  GR1A -10 0 1
!
OPT
!
!               !Optimization used to determine quarter-wave transmission line
!               !length and width, length of isolation trans lines
!               !To optimize, WL4, LL4, AND LL2RA must be made variable
!               !Example:  change LL4=55 to LL4 # 40 55 80
!
  RANGE 18 21
  WCOMB41 DB[S22] < -15 1
  WCOMB41 DB[S32] < -15 1
  WCOMB41 DB[S11] < -15 1
  WCOMB41 DB[S12] > -6.5 1
```

```
Touchstone Sr. (TM) Ver. 2.100.108.2  Config. (100 20936 5 5100923E 8015 0 4319E)
              pdivt3a.ckt    Tue Feb 12 14:33:01 1991

!        FILE:PDIVT3A.CKT
!        Mike Biedenbender 2/12/91
!        description:    Touchstone simulation for Test Circuit 3
!         4:1 power combiner for 4 element array without RADC 20 GHz
!         MMICs with microstip in place of MMICs up to antenna feedthroughs
!         2:1 Wilkinson power combiner designed for 20 GHz
!         99.6% purity alumina
!         No laser trimming of the thin film isolation resistor
!         Simulation for nominal 25 ohm/square sheet resistance to
!         provide 100 ohm isolation resistor
!
!                !Default Units
DIM
  FREQ GHZ
  RES OH
  IND NH
  CAP PF
  LNG MIL
  TIME PS
  COND /OH
  ANG DEG
!
!                !Define variables for microstrip widths and lengths
!
VAR
  W50=9.00       !50 ohm transmission line width
  WL4=3.60       !sqrt(2)*50 ohm transmission line width
  WL2R=2         !minimum width allowed for half-wave lines to isolation resistor
!
  WLTFR1=1.5     !Actual width of the thin film isolation resistor
!

  WLTFR2=1.5     !nominal width of the thin film isolation resistor
  LL4=55         !length of the qurater-wave sqrt(2)*50 ohm trans. line
  LL2RA=62.6     !length of the trans.line perpendicular to the thin film res
  RSA=25         !nominal sheet resistance of the thin film resistor
  RSA1=25        !actual sheet resistance of the thin film resistor
!
!                !Define equations to determine additional trans line lengths,
!                !length of thin film resistor
!
EQN
  LL2RC=(100*WLTFR2)/RSA         !length of the thin film resistor
!
! WLTFR1=WLTFR2*RSA1/RSA         !determines the length of the thin film
!                                !resistor if laser trimming is used
!
  LL2RB=(W50/2) + LL4 - ((50*WLTFR2)/RSA)       !trans line length to tfr
!
!
CKT
!
!                !Define dielectric and conductor parameters
  MSUB ER=9.9 H=10 T=0.06 RHO=1 RGH=0
```

```
  TAND TAND=0.0002


Touchstone Sr. (TM) Ver. 2.100.108.2  Config. (100 20936 5 5100923E 8015 0 4319E)
             pdivt3a.ckt    Tue Feb 12 14:33:01 1991

!
!               !Define Test Circuit 3  - wcomb
!
  MTEE 4 5 1 W1^WL4 W2^WL4 W3^W50
  MLIN 4 7 W^WL4 L^LL4          !quarter wave trans line
  MLIN 5 14 W^WL4 L^LL4         !quarter wave trans line
  MTEE 7 3 9 W1^WL4 W2^W50 W3^WL2R
  MTEE 2 14 15 W1^W50 W2^WL4 W3^WL2R
  MLIN 9 10 W^WL2R L^LL2RA      !trans line perpendicular to isolation tfr
  MLIN 15 16 W^WL2R L^LL2RA     !trans line perpendicular to isolation tfr
!
  MBEND2 10 11 W^WL2R
  MBEND2 16 17 W^WL2R
!
  MLIN 11 12 W^WL2R L^LL2RB     !trans line connected to isolation tfr
  MLIN 17 18 W^WL2R L^LL2RB     !trans line connected to isolation tfr
!
  TFR 12 18 W^WLTFR1 L^LL2RC RS^RSA1 F=0        !thin film isolation resistor
!
  DEF3P 1 2 3 WCOMB             !End of definition for Wilkinson power combiner
!
!
  MLIN 100 110 W^W50 L=1293.2   !Trans line from output combiner output to
!                               !edge of Test Circuit 3
  WCOMB 110 111 112             !Output 2:1 power combiner
  MLIN 111 120 W^W50 L=436.7    !Trans line from output combiner input to
!                               !input combiner output
  MLIN 112 130 W^W50 L=436.7    !Trans line from output combiner input to
!                               !input combiner output
  WCOMB 120 121 122             !Input 2:1 power combiner
  WCOMB 130 131 132             !Input 2:1 power combiner
  MLIN 121 101 W^W50 L=438.5    !Trans line from input power combiner to
!                               !edge of Test Circuit 3
  MLIN 122 102 W^W50 L=438.5    !Trans line from input power combiner to
!                               !edge of Test Circuit 3
  MLIN 131 103 W^W50 L=438.5    !Trans line from input power combiner to
!                               !edge of Test Circuit 3
  MLIN 132 104 W^W50 L=438.5    !Trans line from input power combiner to
!                               !edge of Test Circuit 3
  DEF5P 100 101 102 103 104 WCOMB41A    !Define 5 port combiner
!                                       !End of definition for Test Circuit 3
!
  WCOMB41A 200 201 202 203 204  !Retrieve 5 port combiner
  RES 204 0 R=50                !Terminate a port to make 4 port network
!                               !to allow Touchstone output calculation
  DEF4P 200 201 202 203 WCOMB41 !Define 4 port from 4-way combiner
!
!               !Specify output parameters to determine
!
OUT
  WCOMB41 DB[S11] GR1           !Return loss at output combiner output
  WCOMB41 DB[S21] GR1A          !Insertion loss thru 2 Wilkinson combiners
  WCOMB41 DB[S22] GR1           !Return loss at any input port
  WCOMB41 DB[S32] GR1           !Isolation between inputs of same input combiner
```

```
  WCOMB41 DB[S42] GR1           !Isolation between inputs of different input

Touchstone Sr. (TM) Ver. 2.100.108.2  Config. (100 20936 5 5100923E 8015 0 4319E)
             pdivt3a.ckt    Tue Feb 12 14:33:01 1991

!                                    !combiners
!
!               !Define frequency range for sweeping and optimization
!
FREQ
  SWEEP 18 21 0.1                    !Center Freq of design is 19.7 GHz
!
!               !Define grids for display
!
GRID
  RANGE 18 21 0.2
  GR1 -50 0 5
  GR1A -10 0 1
!
!               !Optimization used to determine quarter-wave transmission line
!               !length and width, length of isolation trans lines
!               !To optimize, w14, l14, and l12ra must be made variable
!               !Example:  change l14=55 to l14 # 40 55 80
!
OPT
  RANGE 18 21
  WCOMB41 DB[S22] < -15 1
  WCOMB41 DB[S32] < -15 1
  WCOMB41 DB[S11] < -15 1
  WCOMB41 DB[S12] > -6.5 1
```