PART TWO

TESTING OF

INDIUM PHOPHIDE DEVICES

Submicron Gate InP Power MISFET's With Improved Output Power Density at 18 and 20 GHz

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ABSTRACT

Presented here are the microwave characteristics at 18 and 20 GHz of submicron gate indium phosphide (InP) metal-insulator-semiconductor field-effect transistors (MISFET's) for high output power density applications. InP power MISFET's were fabricated with 0.7 μm gate lengths, 0.2 mm gate widths, and drain-source spacings of 2, 3, or 5 μm. The output power density was investigated as a function of drain-source spacing. The best output power density and gain were obtained for drain-source spacings of 3 μm. At 18 GHz output power densities of 1.59 W/mm with a gain of 3.47 dB and a power-added efficiency of 20.0% were obtained for a drain-source spacing of 3 μm. At 20 GHz output power densities of 1.20 W/mm with a gain of 3.17 dB and a power-added efficiency of 13.6% were obtained for a drain-source spacing of 3 μm. The output power density is 2.7 times greater than has previously been measured for InP MISFET's at 18 and 20 GHz, and the power-added efficiency has also been increased. The output power density is also 50% better than recently reported for comparable gate width pseudomorphic HEMT's at 20 GHz. The power gain was stable to within 3.0% over 12 hours, and the drain current variation during the same time was less than 5%.

I. Introduction

Indium phosphide (InP) is a compound semiconductor with several material properties which make InP metal-insulator-semiconductor field-effect transistors (MISFET's) especially suited for power amplification at microwave and millimeter-wave frequencies. InP FET's should operate at higher frequencies than gallium arsenide (GaAs) FET's due to the higher peak and saturation electron velocities of InP. InP is better for high-power applications since it has a 30% higher breakdown field and lower ionization coefficients compared to GaAs and a 55% higher room temperature thermal conductivity compared to GaAs [1].

The insulated gate of a MISFET also has several advantages for power amplification. Gate leakage current is virtually eliminated and larger positive gate voltages may be used, which provide both charge accumulation for higher channel current as well as higher gate-source and gate-drain breakdown voltages.

The disadvantage of an insulated gate on InP has been the dc drain current drift with time, which has been widely examined. Shokrani and Kapoor [2] have examined gate insulators with reduced dc drain current drift for InP power MISFET's, and drift mechanisms have been reviewed by Wager et al. [3]. The InP MISFET output power at microwave frequencies has been demonstrated to be more stable than the dc drain current [4].

The promise offered by InP MISFET material and device properties has been realized by record power densities in both the microwave and millimeter-wave region. Messick et al. [4] have demonstrated 4.5 W/mm at 9.7 GHz for InP MISFET's on n-type epitaxial layers using a 1.4 μm gate length and a total gate width of 1 mm. Biedenbender, Kapoor, Messick, and Nguyen [5] and Shokrani et al. [6] have reported 2.4 and 2.7 W/mm, respectively, at 9.7 GHz for an all ion-implanted version of the above device. Others have reported lower output power densities from InP MISFET's with gate lengths from 1.2 to 0.3 μm at frequencies up to 30 GHz [7-10]. The microwave

performance of power FET's is affected by the device size, especially the gate length and the drain-source or drain-gate spacing [11]. However, no investigation of the microwave properties as a function of the drain-source spacing has been reported for InP power MISFET's.

Presented here are the microwave results from a new 0.7 μm gate length InP power MISFET. The new design uses a submicron gate length for operation at high microwave frequencies and drain-source spacings of 2, 3, or 5 μm to compare the effect of device size on output power. Current-voltage (I-V) characteristics are given at dc as well as power measurements at 18 and 20 GHz including output power density, power gain, and power-added efficiency (η_{add}) as function of drain-source spacing. The output power density, power gain, and power-added efficiency at 20 GHz as a function of drain voltage are presented. The variation of power gain and drain current as a function of time is also examined.

II. Experimental

Figure 1 shows a schematic cross section of a submicron gate InP MISFET. The InP MISFET design was based on the structure recently reported by the authors [5]. The InP MISFET's investigated in this work had gate lengths of 0.7 μm. The gate length was reduced compared to the previous structure [5] to provide higher transconductance and power gain for better operation at higher frequencies [12]. The length of the channel recess was 1 μm. The new MISFET design included three devices with drain-source spacings (L_{DS}) of 2, 3, or 5 μm. The InP MISFET's with L_{DS}=5 μm were included since these devices have been reported to provide record output power densities at 9.7 GHz [4]. A drain-source spacing of 5 μm is also similar to values used for GaAs MESFET's to provide good breakdown voltages and high reliability at 15 GHz [12] as well as high total output power at 20 GHz [13]. The L_{DS}=2 and 3 μm devices were included since at higher frequencies lower gate-source and gate-drain parasitics are often necessary despite the lower breakdown voltages possible as device size decreases [11].

The total gate width of the devices was 0.2 mm. Two individual gates with a width of 100 μm were connected in parallel to obtain the total gate width of 0.2 mm. An individual gate width of 100 μm was used to minimize the gain degradation that can occur for large widths as frequency increases. The same individual gate width has recently been reported for pseudomorphic power HEMT's at 20 GHz [14]. A large average spacing of 114 μm between individual gates was used to allow enough room for wire bonds to the individual drain and gate regions. The large gate-to-gate spacing provides the benefit of a low thermal impedance and minimizes the temperature rise [15]. The devices were designed with ten 100 μm wide gates and several gate bonding pads available to provide various total gate widths of up to 1 mm [4]. The total area of each device was 0.5 mmX1.4 mm.

The starting substrate material used for InP MISFET's was a 2-in-diameter semi-insulating (Fe-doped) InP wafer. The surface orientation of the substrate was <100> with a 2° misorientation to the closest <110> directions. Initial cleaning of the InP was done using a sequence of trichloroethylene, acetone, and methanol for degreasing. After degreasing the InP was rinsed in deionized H_2O (DI H_2O) followed by a solution of 1:1 DI H_2O:HF for surface oxide removal, and a final DI H_2O rinse and nitrogen blow dry. Additional details of the InP cleaning procedure have been previously described by Valco, Kapoor, Biedenbender, et al. [16,17].

The InP layers used for the fabrication of the MISFET's have been grown by low pressure metal organic vapor phase epitaxy (MOVPE) in a commercial AIXTRON AIX 200 horizontal reactor as widely used for industrial compound semiconductor production. The design and the variety of processes for which this reactor type have been applied are described elsewhere [18].

A 0.3 μm thick n-type epitaxial layer with a carrier concentration of $3x10^{17}$ cm^{-3} was grown directly on the semi-insulating substrate by MOVPE without an unintentionally doped buffer layer as shown in Fig. 1. As precursors for the preparation of the InP epitaxial layer trimethylindium (TMIn) and 100% concentrated phosphide (PH_3) were used. For n-type doping silicon was incorporated in the layers by introducing diluted SiH_4 (2% in SiH_4) as a source material into the growth atmosphere. The TMIn was transported from a stainless steel cylinder thermostated at 17 C. The cylinder was electronically pressure controlled for extremely stable evaporation rates. The carrier gas in the reaction cell was Pd diffused H_2.

All gas flows were accurately controlled by electronic mass flow controllers and pneumatically operated valves. For extremely sharp interface formation all precursors were switched by a zero dead volume high speed vent/run switching manifold.

For obtaining highly pure and uniform semiconductor layers on large substrate surfaces the application of low pressure growth processes with high gas velocities have been proven to be advantageous. The reactor included an electronic control unit for the chamber pressure. The present work has been performed on a static susceptor.

For obtaining pure and uniform InP layers the growth temperature was adjusted at 600 C, the reactor pressure was held at 15 Torr, and the total flow rates were adjusted to achieve a gas velocity of 2.2 m/sec. The growth rate for the bulk layer was 2.5 μm/hr at a TMIn pressure of 3 mTorr and a V/III ratio of 500. At the target doping for the epitaxial layer, $3x10^{17}$ cm^{-3}, the electron mobility at 77 K was 5000 $cm^2/Vsec$. The crystalline properties of the grown layer were excellent, as shown by a FWHM of less than 15" of the <004> Bragg reflection line in the DCXD spectrum. The surface morphology was featureless in optical microscopy.

Figure 2 illustrates cross sections of the fabrication sequence for the InP MISFET's. Step A of Fig. 2 shows photolithography for the mesa isolation etch. Mesa etching was done using 10 wt.% HIO_3 in DI H_2O. Step B of Fig. 2 shows the source and drain ohmic contacts. The metal patterns were defined by a liftoff technique. The ohmic contacts consisted of a 1500 Å Au:Ge layer and a 1000 Å Au overlayer alloyed at 405 C for 1½ min. Step C of Fig. 2 shows the active channel gate recess. A photoresist mask was used during etching in 30:1 DI H_2O:HBr with 1 drop of H_2O_2 for each 20 ml of solution.

Step D of Fig. 2 shows the silicon dioxide gate insulator deposition. The silicon dioxide was deposited at 250 C using a Technics Planar-Etch II-A plasma reactor, operated at 13.56 MHz with automatic matching. The flow rates used during deposition were 55 sccm nitrous oxide and 23 sccm silane, and the deposition pressure was 350 mTorr. The rf power used was 50 W, corresponding to a power density of 85 mW/cm^2. The details of silicon dioxide deposition on InP have been reported by Shokrani and Kapoor [2]. After deposition the gate insulator was annealed at 300 C for 1 hr in pure H_2.

A 1000 Å gate insulator thickness was reported by Biedenbender, Kapoor, Messick, and Nguyen [5] for a 1.4 μm gate length InP power MISFET at 9.7 GHz. A thinner dielectric can be expected for smaller gate lengths and higher frequencies. A gate insulator thickness of 700 Å has been used by Gardner et al. [9] up to 20 GHz and by Saunier et al. [10] at 30 GHz. The gate insulator thickness used in this investigation was 630 Å. The saturation current density was measured to be ≈1 A/mm after the gate recess and gate insulator deposition and anneal. Saunier et al. [10] have reported the same saturation current density for millimeter-wave operation.

Step E of Fig. 2 shows the gate metal and submicron lithography for the InP MISFET's. The submicron lithography was a variation of the multi-level portable-conformable-mask technique [19]. A thick bottom resist (≈1.1 μm) was used to planarize the gate region. A 1000 Å layer of SiO_2 was deposited on the bottom resist by e-beam evaporation. Finally, a thin (≈2000 Å) resist was spun on the e-beam oxide. The thin top imaging resist was exposed using a 0.5 μm mask and developed. The pattern was transferred to the e-beam SiO_2 using a CF_4/O_2 plasma etch. Because of the isotropic nature of the plasma used the feature size obtained in the SiO_2 layer increased to 0.7 μm. The bottom resist was opened using an oxygen plasma, and the remaining e-beam oxide layer defined the gate during a subsequent metal evaporation and liftoff. The gate metal was 200 Å Ti and 4000 Å Au. Bonding pads to the submicron gates were patterned in a separate, conventional liftoff lithography and were also Ti/Au.

Step F of Fig. 2 shows openings etched in the SiO_2 to the source and drain contact regions. A 4000 Å Au overlayer was deposited in the openings to assist the current handling of the devices and to ensure easy wire bonding. The InP samples were thinned to ~100 m to decrease the thermal impedance of the devices, and were scribed into individual MISFET's. A 200 Å Ti layer and a 4000 Å Au overlayer were deposited on the sample back to aid heat dissipation.

Microwave power measurements for the completed InP MISFET's were obtained using a test fixture with microstrip input and output circuits shown in Fig. 3. The dc bias was applied through an rf choke consisting of a high impedance transmission line in series with low impedance radial stubs. The rf choke was designed for bias currents up to 1.5 A. External chip capacitors across microstrip gaps were used as dc blocks near the test fixture input and output. The circuit design was optimized using commercially available software from 20 to 40 GHz for a wide range of operation. To accommodate the range of device impedances resulting from different drain-source sizes and operation at different frequencies, impedance matching was done empirically using external metal stubs close to the transistor.

The microstrip circuits were epoxied to a gold-plated brass block. The transistors were mounted on a metal ridge between the input and output circuits. Electrical connections to the gate and drain were made by 1 mil diameter wire bonds to the input and output microstrips, respectively. An electrically and thermally conductive silver-loaded epoxy was used for mounting the device and electrical connection to the source. Electrical connections between the test fixture microstrip and measurement system were made using 2.4 mm coax to microstrip launchers with a frequency range up to 50 GHz. Figure 3 shows the test fixture with the coax-to-microstrip launchers. Figure 4 shows a test fixture with a mounted transistor.

A calibration fixture to account for test fixture insertion loss was made with a microstrip through line in place of the transistor. Power measurements of InP MISFET's reported below have been corrected for the minimum calibration fixture insertion loss measured using external tuning at 18 and 20 GHz.

III. Results

Figure 5 shows a typical I-V characteristic for an InP power MISFET with L_{DS}=2 μm and W=0.2 mm. The gate voltage ranges from 0 to -10 V in 1 V steps. The extrinsic transconductance is at least 75 mS/mm for gate voltages greater than -4 V. The zero gate voltage saturation current is ≈1 A/mm at a drain voltage of 5 V. The transconductance and current density are representative values for all devices. For L_{DS}=3 and 5 μm the saturation drain voltage increases as expected with device size to ≈3.8 and ≈4.1 V, respectively. As reported elsewhere, the InP MISFET channel current can not be pinched off in the normal curve tracer dc sweeping mode [2,4,6,10]. However, previous results have shown the channel can be pinched off using a curve tracer which applies the gate voltage in 80 μsec pulses [4,5,10]. Similar decreases in drain current using pulsed gate voltages compared to dc sweeping have also been reported for GaAs power MESFET's [20].

The drain-source breakdown voltages for the I-V measurements in Fig. 5 are 6 V for L_{DS}=2 and 3 μm and 8 V for L_{DS}=5 μm. These voltages are comparable to the 6 V drain bias reported by Saunier et al. [10] for 30 GHz devices with L_{DS}=1.5 μm and a drain current density of 1 A/mm. However, they are lower than the drain voltages of 9 to 18 V reported for other InP MISFET's between 4 and 20 GHz with drain current densities of 70 to 660 mA/mm [4-10]. The gate-drain and gate-source breakdown voltages are >25 V for all devices.

Figures 6a and 6b show measurements at 18 and 20 GHz, respectively, of output power density, power-added efficiency, and power gain as a function of L_{DS}. The gate width is 0.2 mm and the gate voltage is zero for all measurements. At both frequencies the output power density and power gain for conditions used to obtain high output power are best for L_{DS}=3 μm, second for L_{DS}=2 μm, and lowest for L_{DS}=5 μm.

In Fig. 6a at 18 GHz for L_{DS}=2 μm the input power, drain voltage, and drain current density are 21.55 dBm, 6.0 V, and 603 mA/mm, respectively. For L_{DS}=3 μm the input power, drain

voltage, and drain current density are 21.55 dBm, 7.0 V, and 625 mA/mm, respectively. For L_{DS}=5 μm the input power, drain voltage, and drain current density are 19.55 dBm, 7.0 V, and 589 mA/mm, respectively. The output power density for all device sizes is greater than previous measurements for InP MISFET's at 18 GHz [9]. For L_{DS}=3 μm the output power density is up to 1.59 W/mm, which is better by a factor of 2.7. The total output power (up to 318 mW) is comparable to the total powers obtained from larger gate width InP MISFET's at these frequencies [9]. The power-added efficiencies of 23.0 and 20.0% for the L_{DS}=2 and 3 μm devices, respectively, are also improvements for InP MISFET's measured at 18 GHz. The power-added efficiency for L_{DS}=5 m is 12.7% and is less than the value of 15.7% previously achieved at 18 GHz [9].

In Fig. 6b at 20 GHz for L_{DS}=2 μm the input power, drain voltage, and drain current density are 18.63 dBm, 5.6 V, and 690 mA/mm, respectively. For L_{DS}=3 μm the input power, drain voltage, and drain current density are 20.64 dBm, 7.0 V, and 654 mA/mm, respectively. For L_{DS}=5 μm the input power, drain voltage, and drain current density are 19.65 dBm, 6.0 V, and 603 mA/mm. At 20 GHz the L_{DS}=5 μm device has a low power gain less than 2 dB. However, there is over 3 dB gain for the L_{DS}=3 and 2 μm devices, which again have output power densities better than has been reported for larger gate width InP MISFET's providing comparable total output power (up to 240 mW) at 20 GHz [9]. For L_{DS}=3 μm the output power density is up to 1.20 W/mm, which is again better by a factor of 2.7 compared to previous measurements at 20 GHz. For L_{DS}=3 μm η_{add} is improved to 13.6%. At 23 GHz the best gain that could be obtained for any of the devices was only 2.1 dB.

The reason for the best output power being available for L_{DS}=3 μm is probably due to the tradeoff between lower parasitics for smaller devices and higher breakdown voltages for bigger devices. Although parasitics are lower for L_{DS}=2 μm, the drain voltage is higher for L_{DS}=3 μm. At 18 GHz the output power is less for L_{DS}=5 μm even though the drain voltage is the same as for L_{DS}=3 μm. At 20 GHz the maximum

drain voltage decreases for L_{DS}=5 μm and power gain and output power are low.

Figure 7 shows microwave power measurements at 20 GHz of output power density, power gain, and power-added efficiency as a function of drain voltage. The measurements are for a device with W=0.2 mm and L_{DS}=3 μm. The maximum output power density at 20 GHz is 1.20 W/mm, with a corresponding gain of 3.17 dB and power-added efficiency of 13.6%. The input power is 20.6 dBm; it is the highest examined at 20 GHz for this device and the gain in Fig. 7 is compressed for all drain voltages. The power gain, P_{out}, and η_{add} all increase with drain voltage. At 18 GHz the same device had a maximum output power density of 1.59 W/mm, with a corresponding gain of 3.47 dB and power-added efficiency of 20.0% for a drain voltage of 7.0 V and P_{in}=21.6 dBm.

The drain current decreases with increasing microwave input power as has been previously observed for InP MISFET's [4,5,10]. The saturation current density for the device in Fig. 7 at 18 and 20 GHz is 654 mA/mm for P_{in}=20.6 dBm and a drain voltage of 7.0 V. The decrease in drain current with P_{in} has been attributed to a change in the charge status of states near the InP-insulator interface [4,5], although a mechanism for the response of such states at the high frequencies involved is yet to be developed. Another possible cause for the decreased current is the nonlinear output characteristics that can occur as the device is driven into compression [21]. The lower drain current results in higher drain-source breakdown voltages compared to dc values. The maximum drain voltages that can be used with rf power applied are 8 V for L_{DS}=2 or 3 μm and 9 V for L_{DS}=5 μm. When high drain voltages are used to obtain maximum output power, a high input power must also be applied for a low drain current. Reducing P_{in} while a high drain voltage is applied results in increased current and thermal breakdown of the transistor. The change in drain current limits the range of P_{in} for measurements of P_{out} versus P_{in} under constant bias conditions.

Figure 8 shows the power gain and drain current variation over a 12 hour period. The measurements are at 18 GHz for a L_{DS}=3 μm device. The microwave input power was set to an initial value of 15.66 dBm. The gate voltage was 0 V. At t=0 sec the drain voltage was changed from 1.5 V to 5.5 V. The gain and drain current density at t=0 sec were 3.60 dB and 721 mA/mm, respectively. The microwave power source had a power variation of 0.15 dB during the measurement time, so the power gain variation is shown instead of the output power variation to eliminate the effect of the input power variation. The power gain was stable to within 3.0%, which corresponds to an overall change of 0.13 dB. The drain current showed an initial increase of 2.0% and later decreases of as much as 2.4%. The power gain stability is slightly less than the output power stability of 2% over 167 hours previously reported for 1.4 μm gate length power MISFET's [4]. However, the drain current change is better than the value of 10% observed for the 1.4 μm gate length MISFET's [4].

IV. Summary

InP power MISFET's were fabricated with a 0.7 μm gate length. Different device sizes were examined with gate widths of 0.2 mm and drain-source spacings of 2, 3, and 5 μm. Current-voltage measurements at dc indicated extrinsic transconductances of up to 75 mS/mm. The drain-source breakdown voltages were 6 to 8 V. The gate-source and gate-drain breakdown voltages were >25 V. Power measurements at 18 and 20 GHz showed output power densities up to 2.7 times greater than previously observed at these frequencies for InP MISFET's, and power-added efficiency was also improved. At 18 GHz for a drain-source spacing of 3 μm the output power was 318 mW (1.59 W/mm) with a gain of 3.47 dB and a power-added efficiency of 20.0%. At 20 GHz for a drain-source spacing of 3 μm the output power was 240 mW (1.20 W/mm) with a gain of 3.17 dB and a power-added efficiency of 13.6%. The output power density for the 0.2 mm gate width InP MISFET's here is 50% greater than the value of 0.8 W/mm recently reported at 20 GHz for 0.15 mm gate width pseudomorphic HEMT's with 0.25 μm gate lengths [14].

The best output power density and gain were obtained for drain-source spacings of 3 μm. The maximum drain voltage was lower for 2 μm drain-source space devices as was the gain and output power density. Devices with a 5 μm drain-source space had lower gain and output power density despite comparable maximum drain voltages to the 3 μm drain-source space devices. The power gain was stable to within 3.0% over 12 hours. The drain current variation was less than 5% during the same time period.

The gain was less than 3 dB and the output power density was low for gate widths greater than 0.2 mm. The total output power of the InP MISFET's here may be improved if the drain-source breakdown voltage can be increased through optimization of the device processing. Although excellent output power densities and power-added efficiencies have been achieved for gate widths of 0.2 mm, the maximum drain voltages that can be

used are relatively low compared to most other InP MISFET's. Several parameters including the drain saturation current resulting from the gate recess, channel thickness, and channel doping density could be investigated to increase the drain-source breakdown voltages for the InP MISFET's here. Higher breakdown voltages may provide even better output power density and enhance the operation of larger gate width InP MISFET's for higher total power. The total output power may also be improved through the use of a different device topology for better power combining, such as air bridge connections and source vias commonly used in commercial devices.

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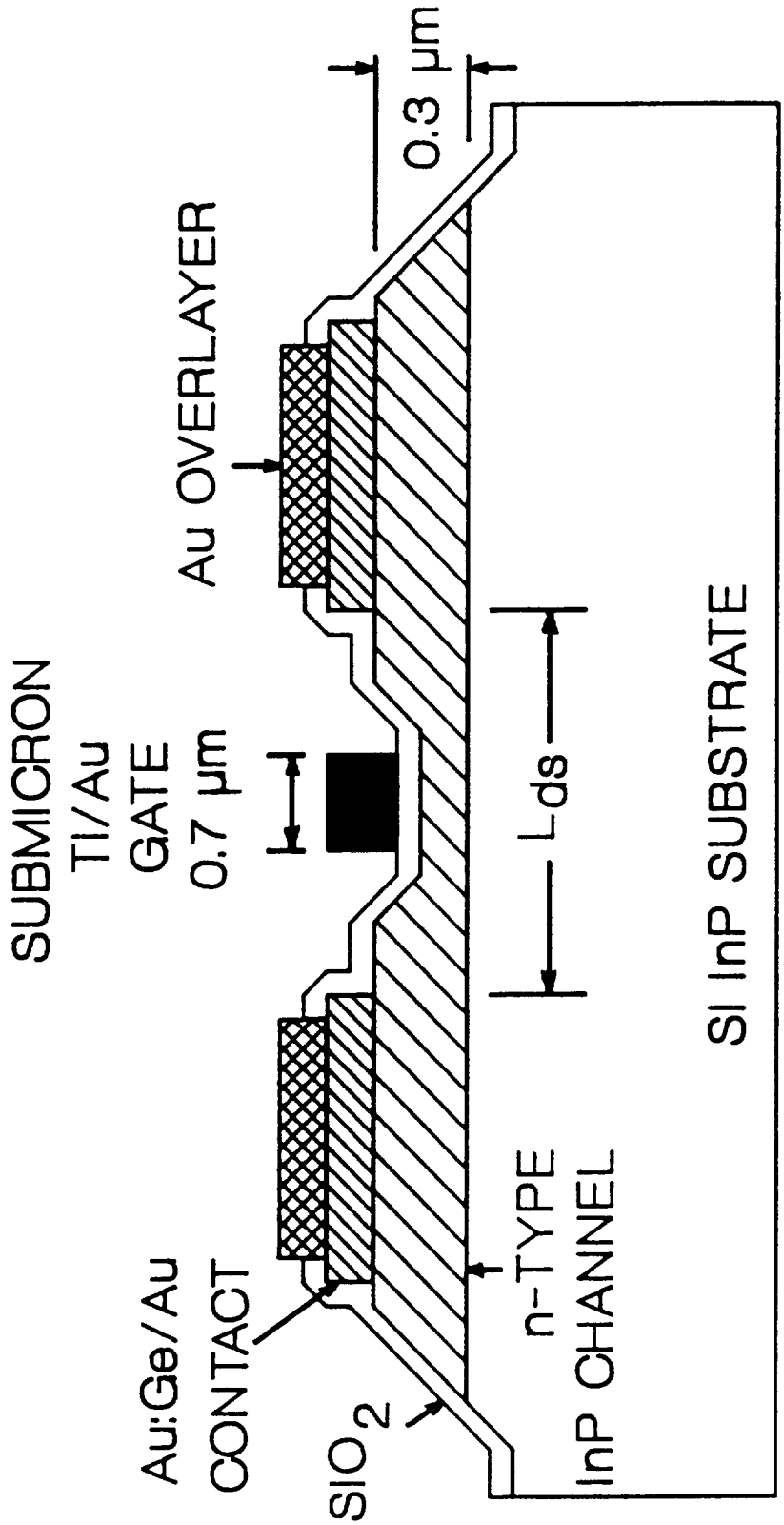
Figures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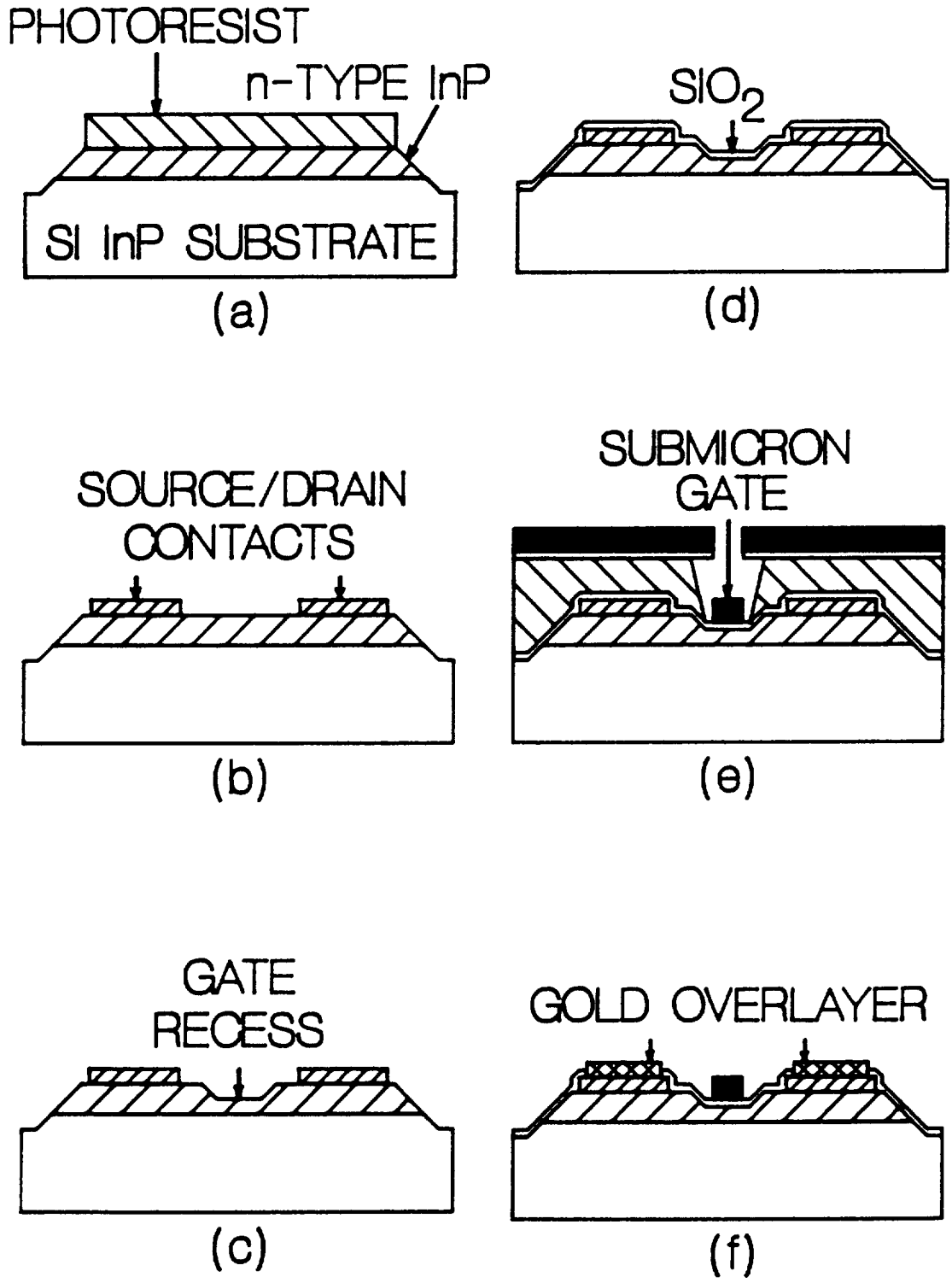
InP CHANNEL

FIGURE 1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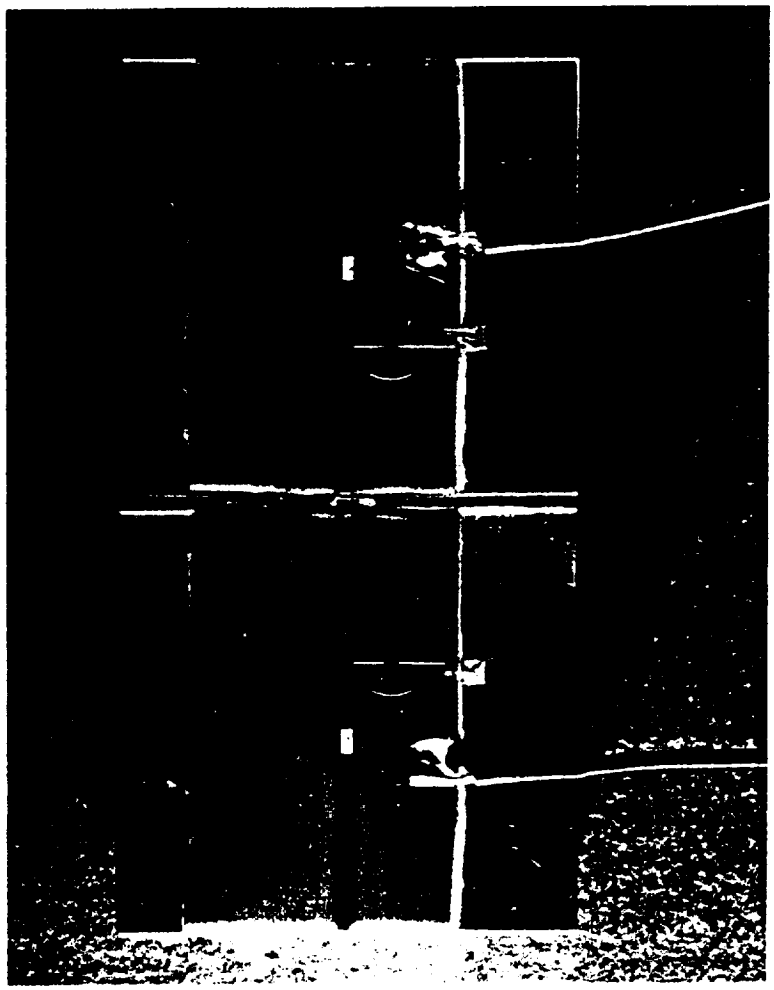
GOLD OVERLAYER
(f)

FIGURE 2



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C-90-11398

FIGURE 3

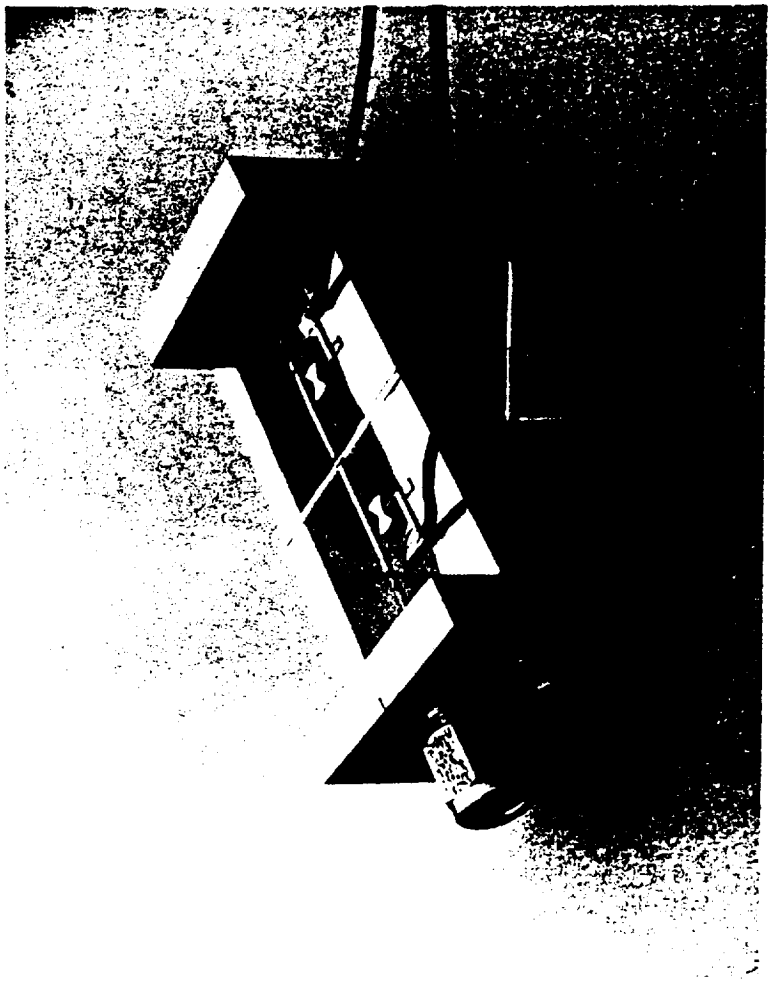

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FIGURE 4

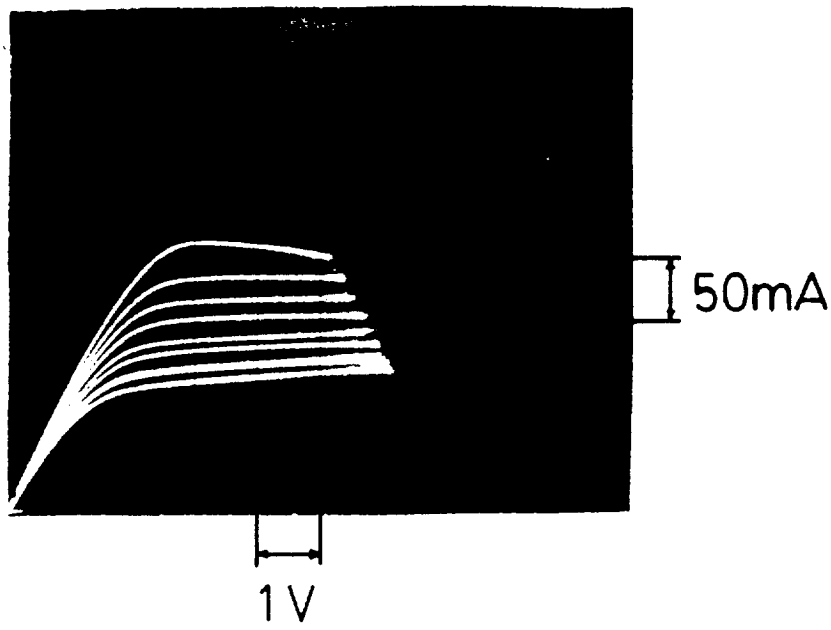

FIGURE 5

(b)
20 GHz
DRAIN-SOURCE SPACING (μm)
POWER GAIN (dB)
OUTPUT POWER DENSITY (W/mm)
POWER-ADDED EFFICIENCY (%)
(a)
18 GHz
DRAIN-SOURCE SPACING (μm)
POWER GAIN (dB)
OUTPUT POWER DENSITY (W/mm)
POWER-ADDED EFFICIENCY (%)

FIGURE 6

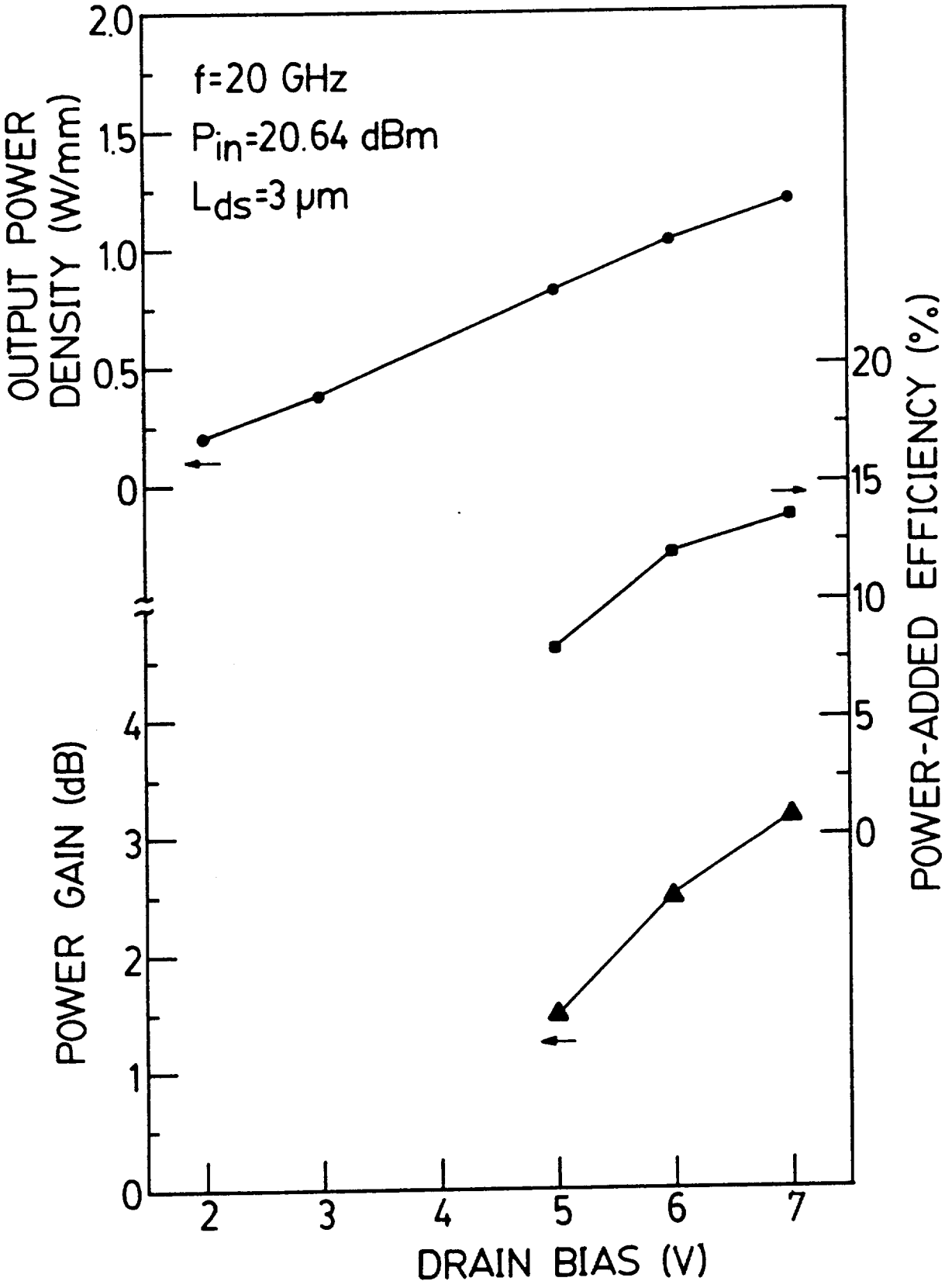
f=20 GHz
P_{in}=20.64 dBm
L_{ds}=3 μm
OUTPUT POWER DENSITY (W/mm)
POWER GAIN (dB)
POWER-ADDED EFFICIENCY (%)
DRAIN BIAS (V)
2.0
1.5
1.0
0.5
0
4
3
2
1
0
20
15
10
5
0
2
3
4
5
6
7

FIGURE 7

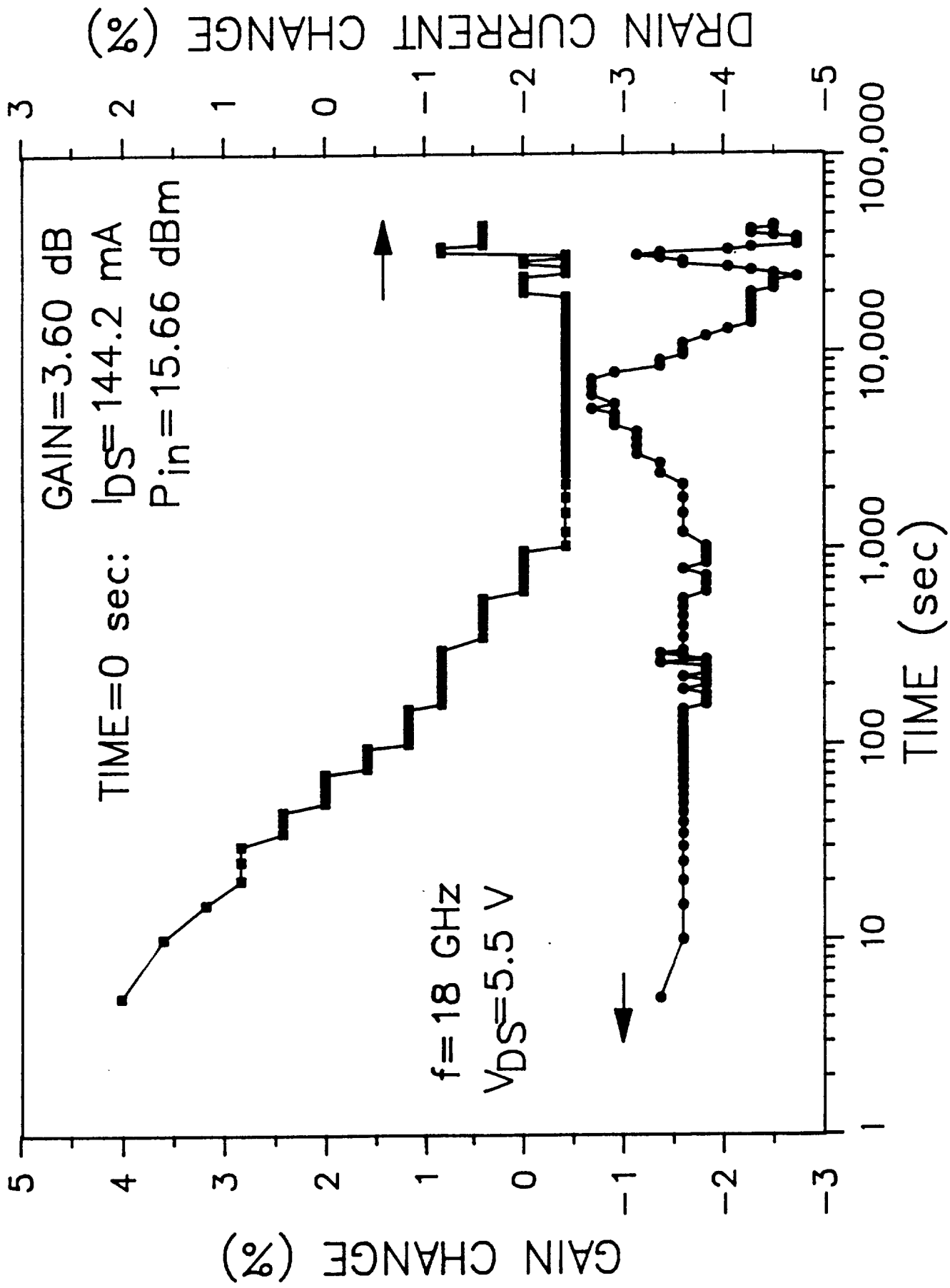
GAIN CHANGE (%)
DRAIN CURRENT CHANGE (%)
TIME (sec)
TIME=0 sec: I_{DS}=144.2 mA
P_{in}=15.66 dBm
GAIN=3.60 dB
f=18 GHz
V_{DS}=5.5 V

FIGURE 8