NASA Contractor Report

PART I

# System and Component Design and Test of a 10 HP, 18,000 RPM AC Dynamometer Utilizing a High Frequency AC Voltage Link

Contract No. NAG3-940
Final Report

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# Chapter 1
# Introduction

## 1.1 Objective of This Research

The first and most important objective of this research concerns the design, construction and testing of a second generation three phase to three phase power converter system and field oriented induction machine drive based upon "Pulse Density Modulated" (PDM) converters utilizing a 20 kHz parallel resonant high frequency AC link. This link enables the implementation of a high speed, 10 hp (7.46 kW) squirrel cage induction machine to operate as a fast response AC Dynamometer. When this machine is operated as an AC-generator, it can feed back power to the 60 Hz utility at unity power factor via this converter system and reach speeds up to 18,000 rpm by use of field weakening thereby making high speed machine tests possible. Furthermore, bidirectional power flow capability of the system offers full 4-quadrant operation for the induction machine.

The second objective of this research is to review the design and testing of the first generation three phase to three phase converter system and the field oriented induction machine drive based upon use of PDM converters and 20 kHz parallel resonant HF ac link. The objective is also to discuss its limitations to achieve the proposed power levels mentioned in the preceding paragraph and finally to compare both the first and second generation systems.

The third objective of this research is to conduct several series of tests on the samples of "MOS Controlled Thyristors" (MCT) for use as switching devices and to investigate their feasibility for use in the converter system mentioned above wherein a zero voltage switching scheme is used. However, the presence of a high turn-on voltage requirement for the MCTs in zero voltage switching applications, determined by means of these tests, led us to the search for utilization of other devices for this application.

Several other interesting research results were determined during the course of construction and during the tests of the second generation converter and they are included here in this report.

## 1.2 Summary of the Report

Hard and soft switching test results conducted with one of the samples of first generation MCTs and similar but more troublesome test results with several different samples of second generation MCTs are reported in Chapter 2. A simple chopper circuit is used to investigate the basic switching characteristics of MCT under hard switching and various types of resonant circuits are used to determine the soft switching characteristics of MCT under both zero voltage and zero current switching.

In Chapter 3, firstly the operation principles of a Pulse Density Modulated Converter (PDMC) for 3Ø (three phase) to 3Ø two-step power conversion via parallel resonant High Frequency (HF) AC link is reviewed. Later, the details for the selection of power switches and other power components required for the construction of the power circuit for the second generation 3Ø to 3Ø converter system is discussed. The problems encountered in the first generation system, in the selection of the new power components, and in the second generation system are presented. The solutions and suggestions to these problems are also discussed.

In Chapter 4, the design and performance of the first generation 3Ø to 3Ø power converter system and field oriented induction motor drive based upon a 3 kVA, 20 kHz parallel resonant HF ac link is described. Low harmonic current both at the input and output, unity power factor operation of input and bidirectional power flow capability of the system are shown via both computer and experimental results.

Chapter 5 describes the work completed on the construction and testing of the second generation converter and field oriented induction motor drive based upon specifications for a 10 hp (7.5 kW) squirrel cage dynamometer and a 20 kHz parallel resonant HF ac link. The induction machine is designed to deliver 10 hp or 7.46 kW when operated as an AC-Dynamo with power fed back to the source through the converter. The results presented in Chapter 5 reveal that the proposed power level requires additional energy storage elements to overcome difficulties with a peak link voltage variation problem that limits reaching to desired power level.

Chapter 6 briefly describes the power level test of the second generation converter after the addition of extra energy storage elements to the HF link. The importance of the source voltage level to achieve a better current regulation for the source side PDM converter is also briefly discussed. The power levels achieved in the motoring mode of operation shows that the proposed power levels in generating mode of operation (operation as an AC Dynamometer) can also be easily achieved if there were no mechanical speed limitation to drive the induction machine at the proposed power level. Since speeds up to 18,000 rpm can be achieved by use of field weakening, high speed machine tests up to 10 hp becomes possible via this system.

Chapter 7 reviews the report and presents conclusions concerning the important aspects of this report and gives recommendations for possible future work.

# Chapter 2

# Testing of MOS-Controlled Thyristors

The MOS-Controlled Thyristor (MCT) is a strong candidate for the power semiconductor switch to be used in a 20 kHz resonant link power conversion system. To verify the characteristics of the MCT operating as a switch, two series of tests were conducted. One test was carried out during late 1987 and studied the initial batch of MCTs which became available. The other test which used a second generation type device was conducted during late 1989 and the early 1990 period. This chapter reports the results of both of these series of tests. Section 2.1 mainly covers the earlier test results and Section 2.2 covers more recent test results. Several circuits were built with MCT's and different type of tests were carried conducted to determine the switching capability of the device. One of the tests is a simple chopper circuit to investigate the basic switching characteristics of MCT under hard switching. The other circuits are various types of resonant circuits to determine the soft switching characteristics of the MCT. The tests to determine the soft switching characteristics of MCT cover both zero voltage and zero current switching tests.

## 2.1 Test Results of First Generation Devices

### 2.1.1 Basic Principle of MCT Switching

The MCT used in the test was the complementary type whose equivalent circuit schematic of unit cell is shown in Fig. 2.1 The basic principle of turn-on and off can be described as follows [1-10].

There are several ways to turn-on the device. The most useful method is to use the built-in "on-FET" which is effectively connected between the emitter and collector of the upper transistor in Fig. 2.1. Driving the gate of this on-FET with -5.V. or -7 V. (-12 V. is recommended) with respect to anode turns-on the bottom NPN transistor with its drain current. This, in turn, triggers the SCR and causes the MCT to turn-on.

The same gate terminal is used to turn-off the MCT by applying a positive voltage. The gate voltage is referenced to the anode of the MCT. Driving the "off-FET" shown in Fig. 2.1 with +10 V. (+15 V. is recommended) with respect to the anode turns it on. Turned-on of the off-FET establishes an active short circuit between the emitter and base of the upper transistor. All the current is diverted to the off-FET and bypasses the p-n junction of the upper transistor causing the turn-off of the MCT.

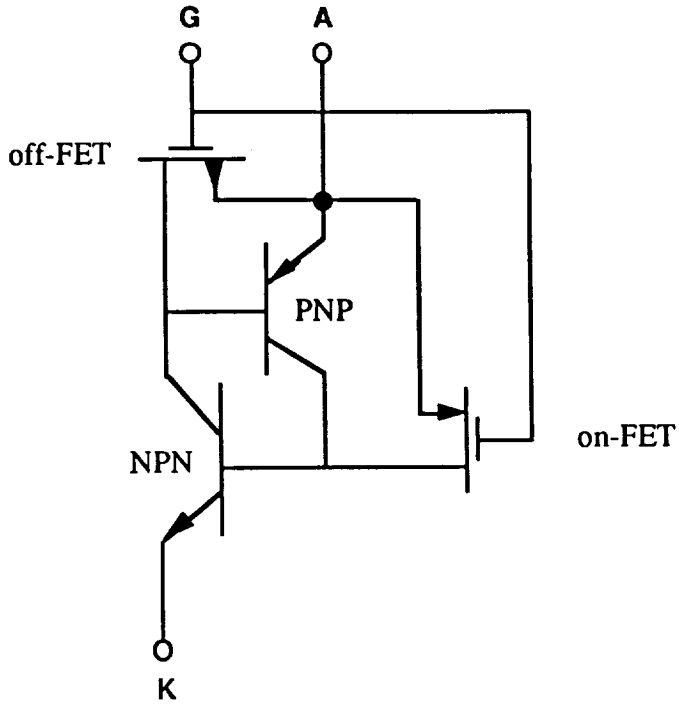



Fig. 2.1 Circuit Schematic of Typical MCT Unit Cell.

The main features of the MCT can be summarized as follows [1-10]:

- Gate turn-on and turn-off capability.
- Combines the fast switching property of MOSFET with high power rating of SCR.
- Turn-on and off time equal or less than the Gate Turn-Off Thyristor (GTO).
- Very low forward voltage drop compared to other semiconductor power switches.
- Much greater current density than most other semiconductor power switches.
- Low power gate drive requirements are similar to a MOSFET.
- Is an asymmetric device, but possible to build in symmetric form for bilateral voltage blocking.

### 2.1.2 Hard Switching Characteristics of MCT

To understand the basic switching characteristics of the device, the circuit shown in Fig. 2.2 was constructed. The circuit is a simple DC-chopper circuit, which regulates DC power into a load. The gating amplifier circuit to turn-on and off the MCT shown in Fig. 2.3 was designed and used for the entire test including other kinds of power circuit

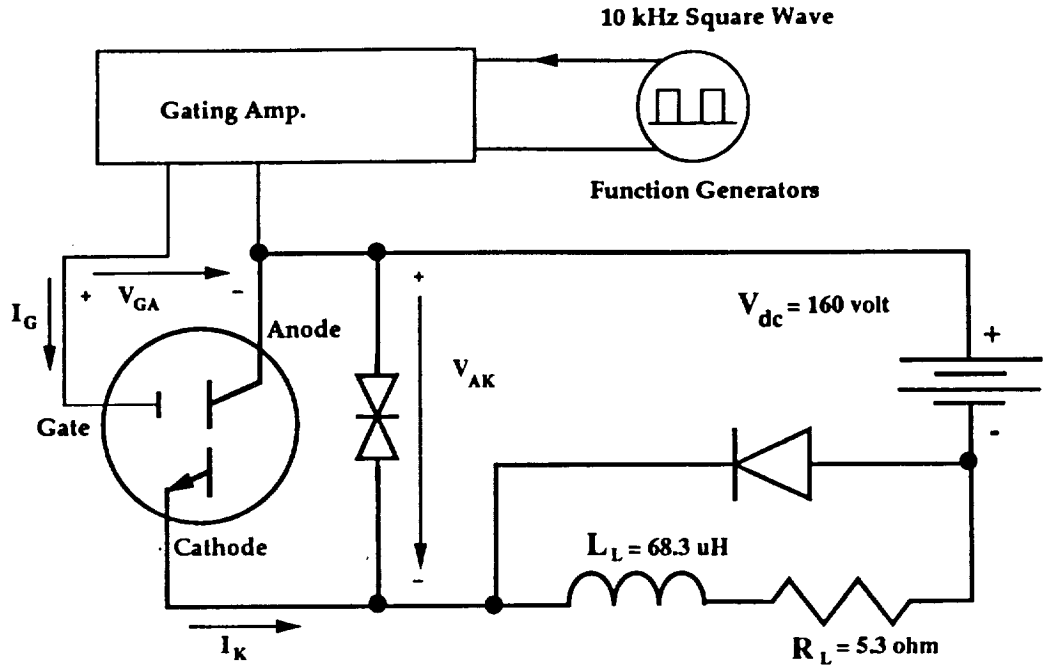



Fig. 2.2 Chopper Circuit Utilizing MCT Switch.

arrangements. In this gating amplifier circuit an opto-isolator is used in order to isolate the control and the power circuit. Also, the power supply of the gating amplifier was constructed with a different ground from that of control power supply. To turn-on the MCT, a negative voltage should be applied to the gate with respect to anode, and to turn it off, a positive voltage is needed. The voltage and current waveforms of the gating circuit are shown in Figs. 2.4 to 2.6. Note that the current is almost a spike which has a peak value around 2.5 A. and a period of about 250 nsec. In the experimental procedure, about -7 V. is applied to the gate with respect to the anode to turn-on the device and to turn it off +12 V. is applied. In Figs. 2.5 and 6, the fall time and rise time of the gate voltage are about 300 nsec.

The overall operation of the chopper circuit is clearly shown in Fig. 2.7, where the switching frequency is 10 kHz. Because of the inductance of the load, the current increases exponentially for the on period of the the MCT. A magnified view of Fig. 2.7 at the instant of turn-on of the MCT is shown in Fig. 2.8. From the figure, it can be seen that the rise time of the MCT is about 360 nsec whereas in Fig. 2.9 which is the case of turn-off, the fall time is about 1.5 μsec. Delay times at at the instant of turn-on and off are

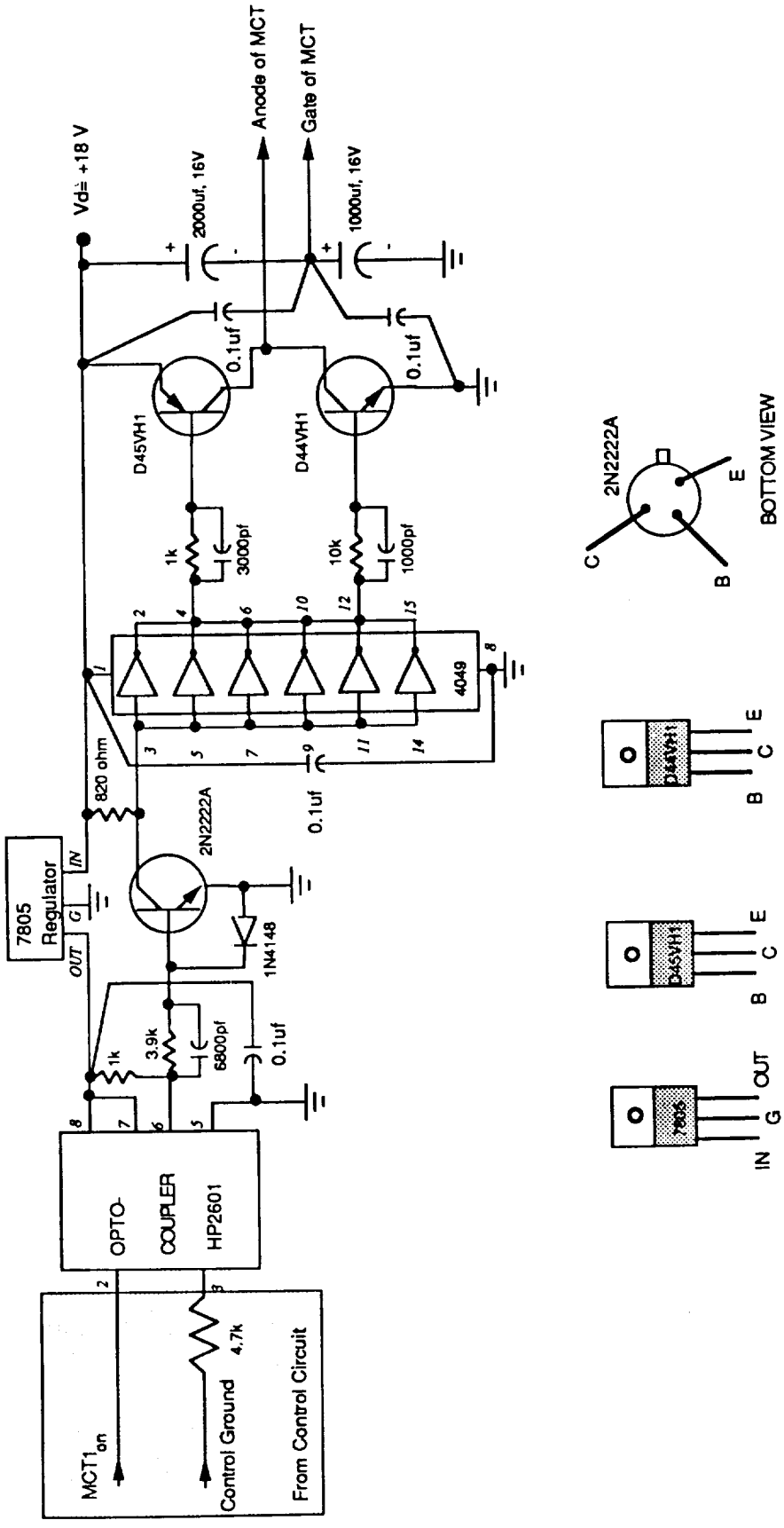



Fig. 2.3 Gating Amplifier Circuit for MCT.

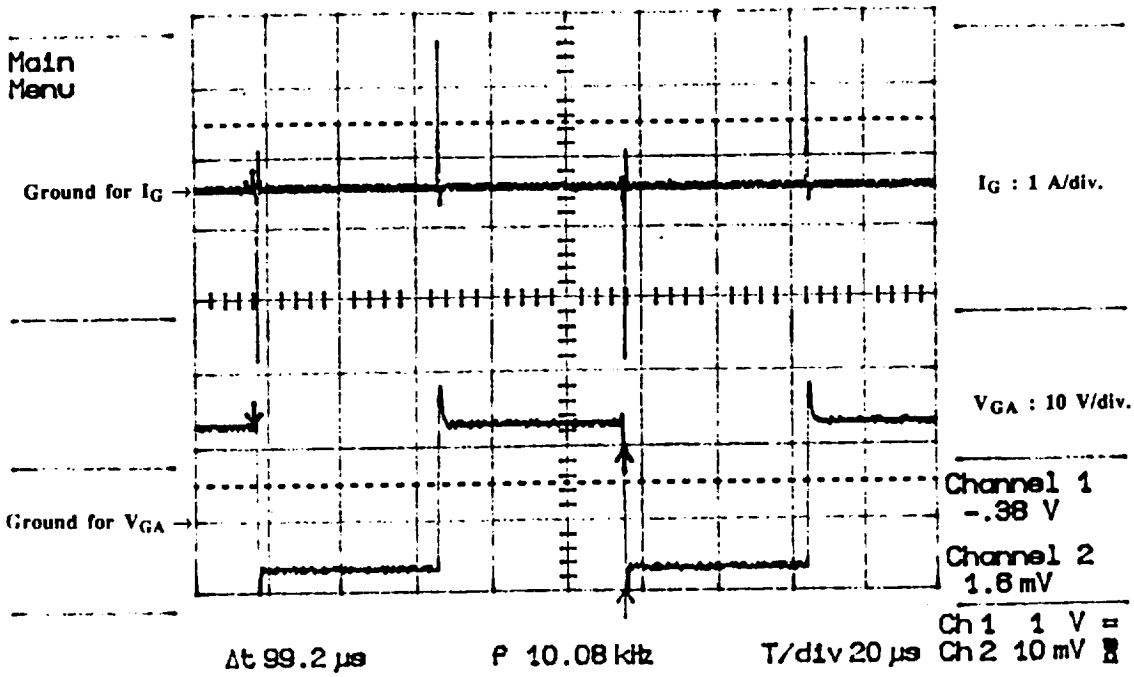



Fig. 2.4. Current and Voltage of Gating Circuit. Top Trace: MCT Gate Current: $I_G$ : 1 A/div. Bottom Trace: MCT Gate to Anode Voltage: $V_{GA}$ : 10 V/div. Time/div: 20 μsec.

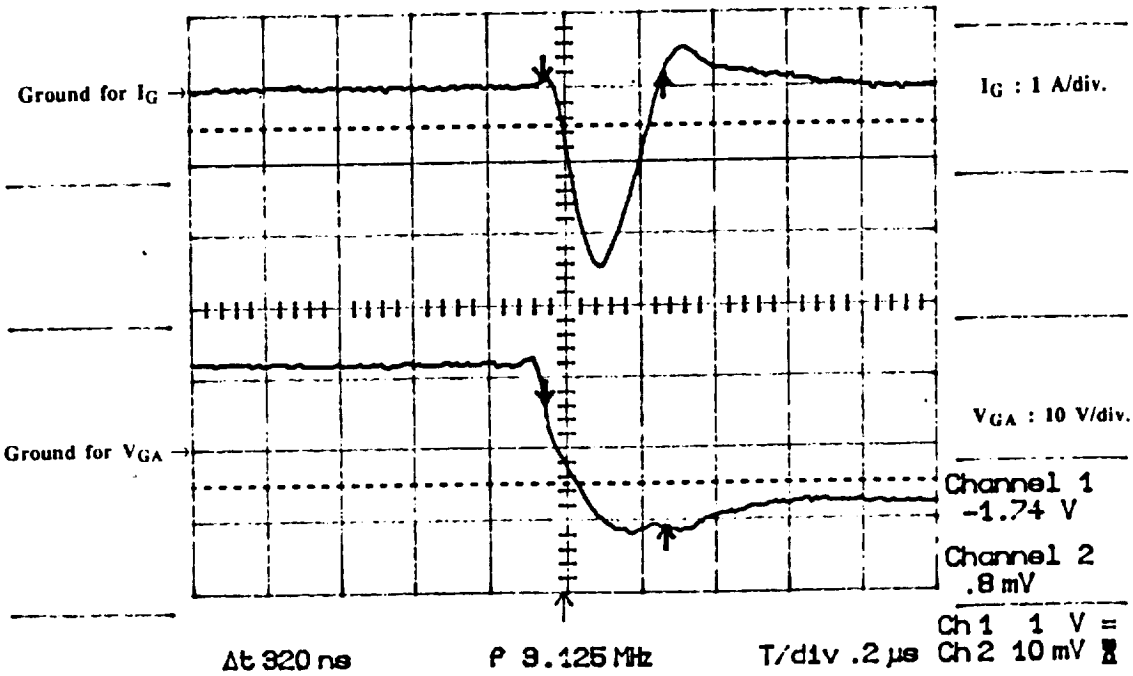



Fig. 2.5. Gating Characteristics During Turn-on. Top Trace: MCT Gate Current: $I_G$ : 1 A/div. Bottom Trace: MCT Gate to Anode Voltage: $V_{GA}$ : 10 V/div. Time/div: 200 nsec.

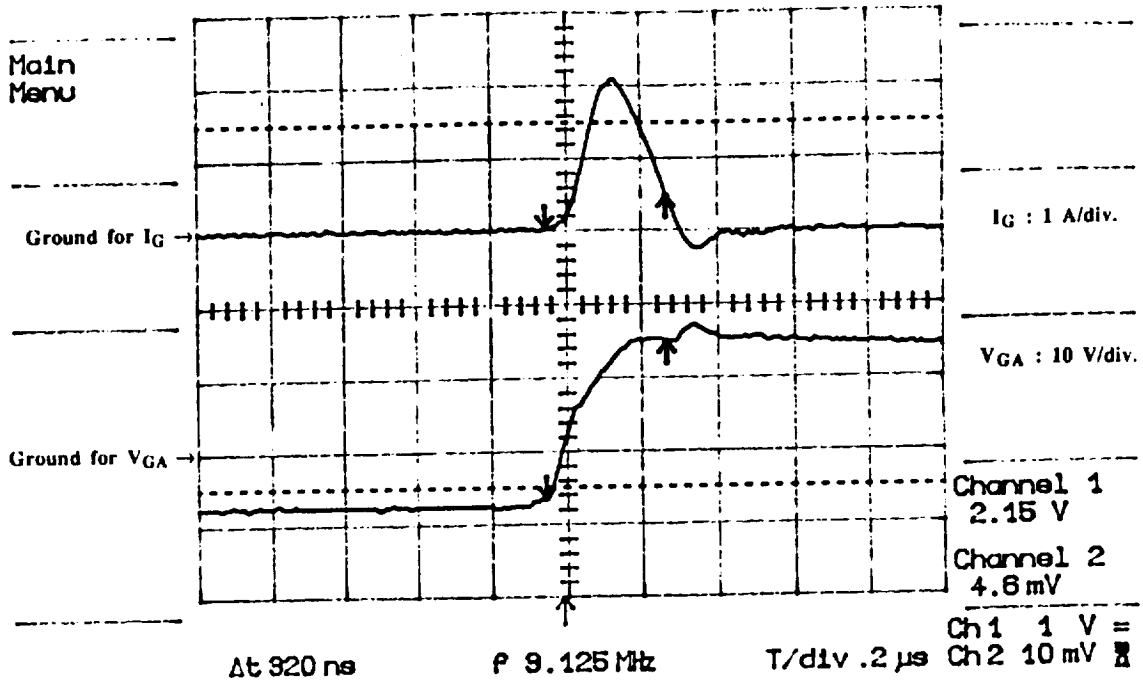



Fig. 2.6. Gating Characteristics During Turn-off. Top Trace: MCT Gate Current: $I_G$ : 1 A/div. Bottom Trace: MCT Gate to Anode Voltage: $V_{GA}$ : 10 V/div. Time/div: 200 nsec.

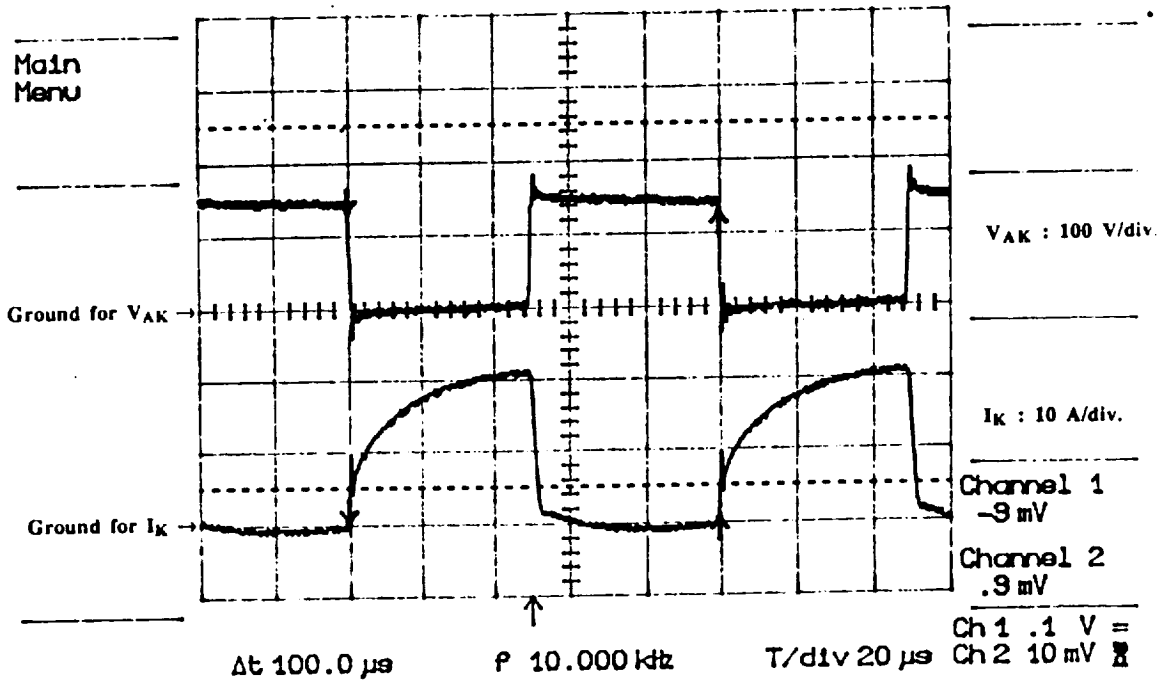



Fig. 2.7. Showing Overall Operation of Device in Chopper Circuit. Top Trace: MCT Anode to Cathode Voltage: $V_{AK}$ : 100 V/div. Bottom Trace: MCT Cathode Current: $I_K$ : 10 A/div. Time/div: 20 µsec.

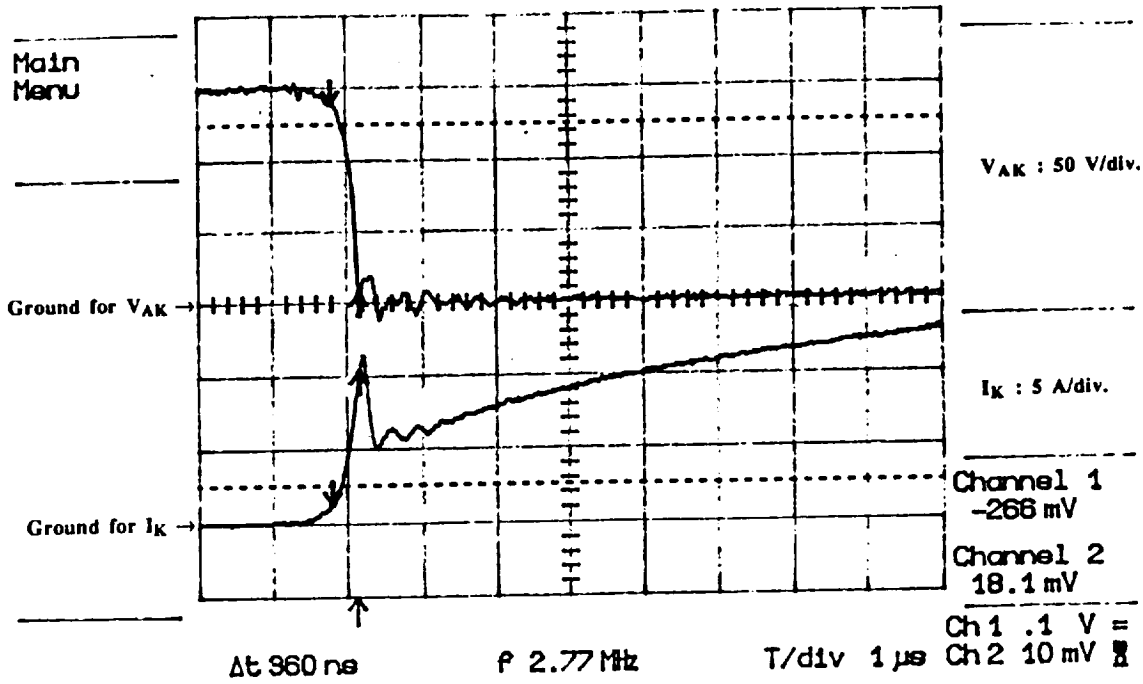



Fig. 2.8. Turn-on Characteristics of MCT Operating in Chopper Circuit. Top Trace: MCT Anode to Cathode Voltage: $V_{AK}$ : 50 V/div. Bottom Trace: MCT Cathode Current: $I_K$ : 5 A/div. Time/div: 1 μsec.

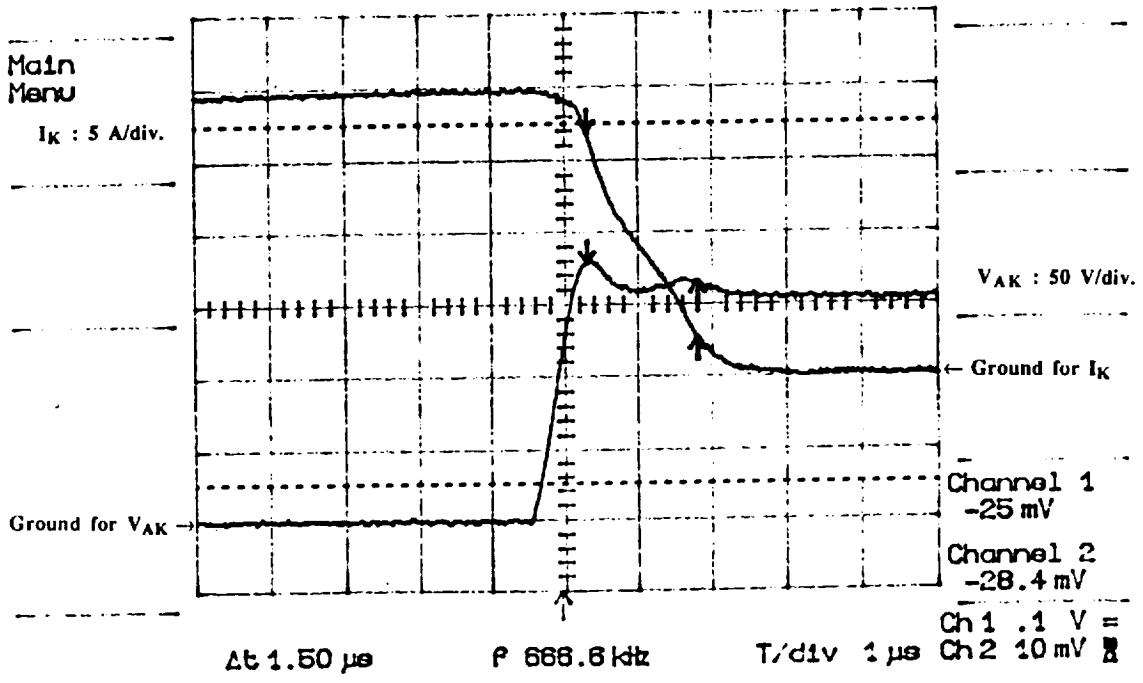



Fig. 2.9. Turn-off Characteristics of MCT Operating in Chopper Circuit. Top Trace: MCT Cathode Current: $I_K$ : 5 A/div. Bottom Trace: MCT Anode to Cathode Voltage: $V_{AK}$ : 50 V/div. Time/div: 1 μsec.

shown respectively in Figs. 2.10 and 2.11 . From these figures, it can be observed that the delay time at turn-on is 720 nsec and at turn-off is 520 nsec.

### 2.1.3 Zero Current Switching Characteristics of MCT

The zero current switching characteristics of the MCT were investigated by means of the resonant circuit shown in Fig. 2.12 [11]. The circuit is a typical Parallel Output Series Resonant inverter which generates single phase 20 kHz voltage from a DC source. In this circuit, the MCT turns on at zero current instants and turns off at zero voltage and zero current. A typical output voltage waveform across the load is shown in Fig. 2.13 with a current waveform which flows through a switch. The output voltage is 20 kHz sinusoidal waveform with small harmonic content. In Fig. 2.14, turn-on and off of the MCT are shown, indicating the point where negative current flows through the feedback diode of the MCT. In the control circuit, the turn-off signal is generated when the current starts to flow in the negative direction. A detailed view of turn-on of the MCT is shown in Fig. 2.15, where it is shown that the MCT current increases after the device voltage decreases. The turn-on time is approximately 700 nsec. In Fig. 2.16 turn-off of the MCT is shown under conditions where the MCT turns off at zero voltage and zero current. Due to the resonance of the circuit, when the current starts to flow in the negative direction, the feedback diode turns on and a small negative voltage corresponding to the forward voltage drop of the diode is applied to the anode-cathode terminals of the MCT. At the same time the gate control circuit generates the turn-off signal for the other MCT. From the bottom trace of Fig. 2.16, the change-over instant of current flow from the MCT to the diode during the period where the voltage across the switch changes its polarity can be followed. The gate signal for the MCT and the voltage across the device are shown in Fig. 2.17. If this figure is compared to Fig. 2.14, it is clear that a gate signal for turn off is generated when the current begins to change its polarity from positive to negative.

### 2.1.4 Zero Voltage Switching Characteristics of MCT

Generally, in order to turn-on an MCT, some positive voltage should exist across the anode to cathode of the device. This voltage, the so called 'threshold voltage', might be a problem in zero voltage switching when no voltage exits across the device at turn-on. To verify this problem, the circuit shown in Fig. 2.18 was built and tested. In this circuit, two switches operate in complementary fashion and the inductor current becomes a sawtooth

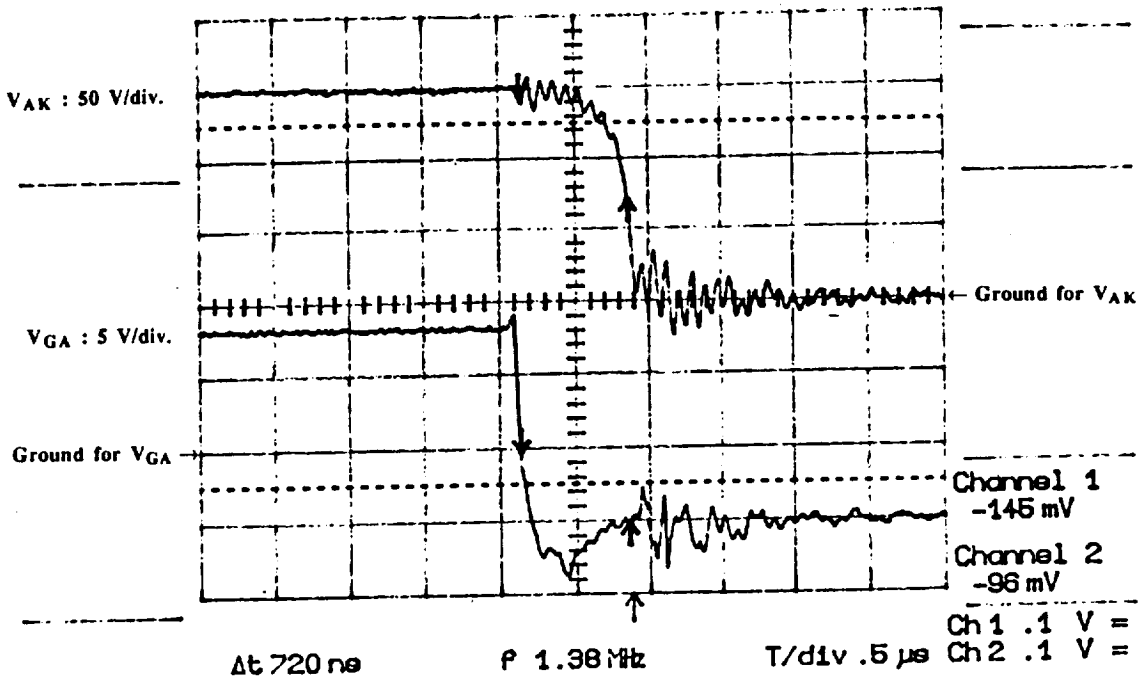



Fig. 2.10. Showing Turn-on Delay of MCT. Top Trace: MCT Anode to Cathode Voltage: $V_{AK}$ : 50 V/div. Bottom Trace: MCT Gate Anode Voltage: $V_{GA}$ : 5 V/div. Time/div: 500 nsec.

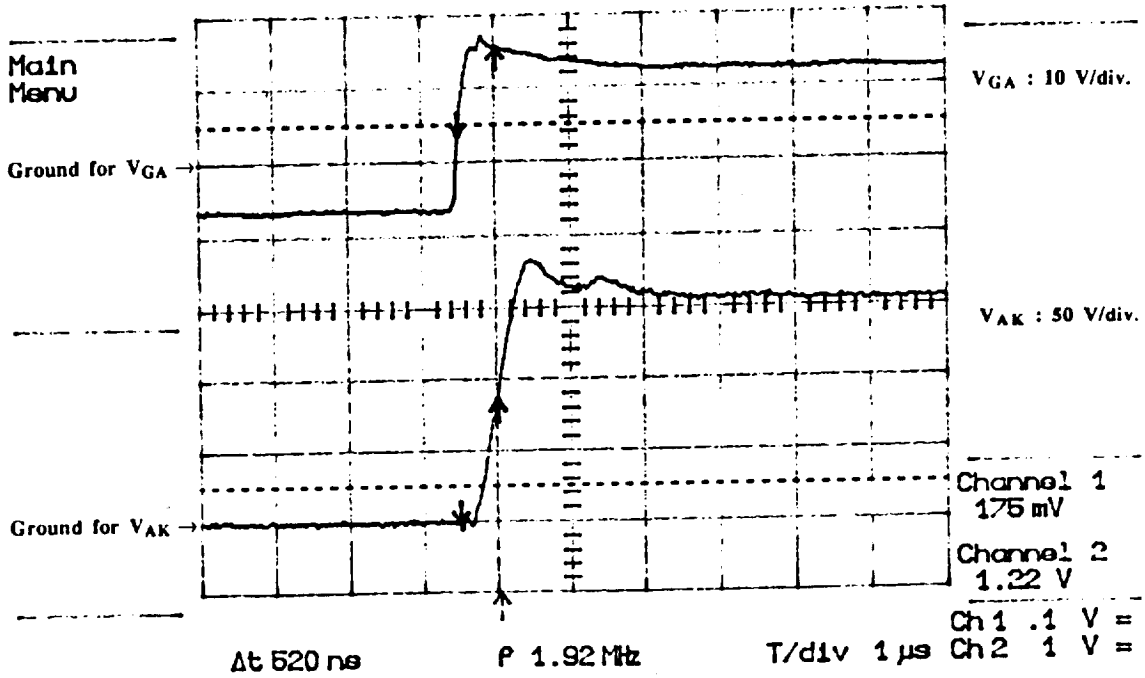



Fig. 2.11. Showing Turn-off Delay of MCT. Top Trace: MCT Gate to Anode Voltage: $V_{GA}$ : 10 V/div. Bottom Trace: MCT Anode to Cathode Voltage of MCT: $V_{AK}$ : 50 V/div. Time/div: 1μsec.

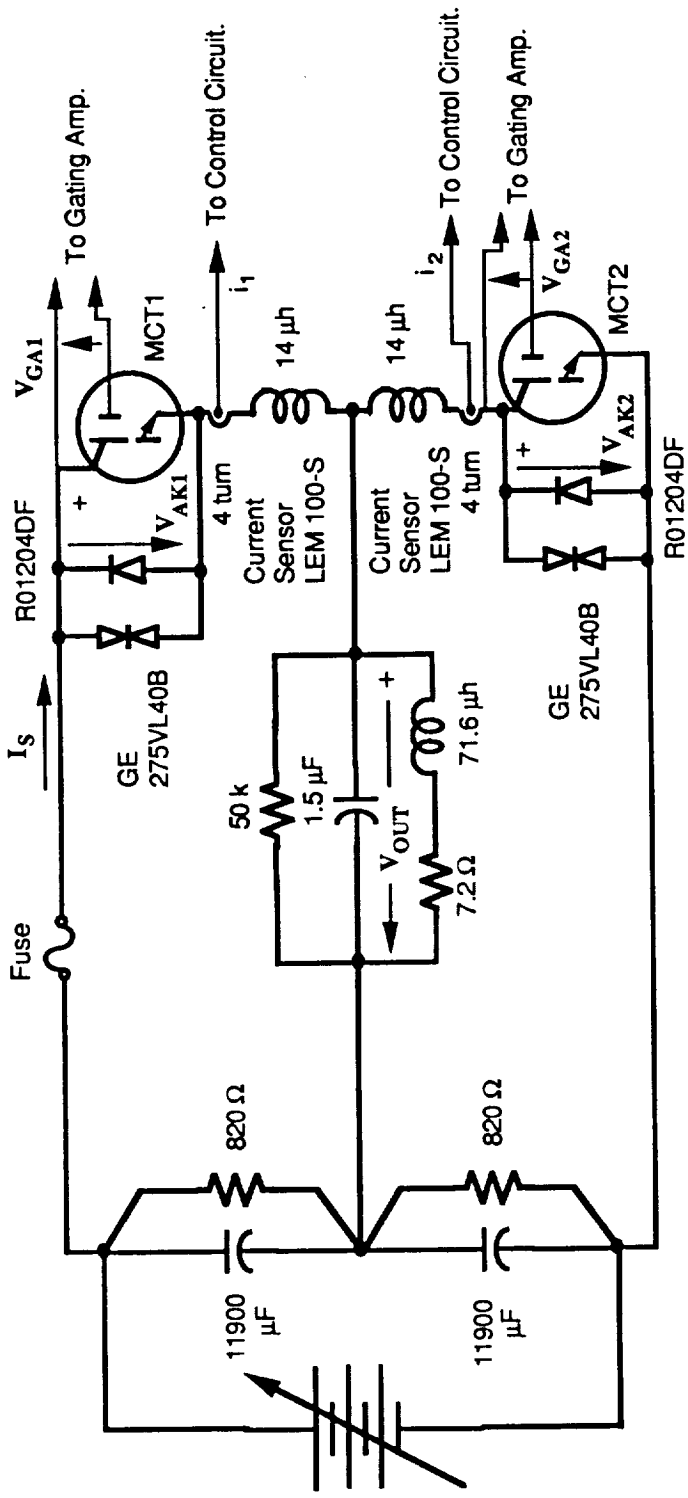



Fig. 2.12 Parallel Output-Series Resonant (POSR) Circuit for Soft Zero Current Switching of MCT.

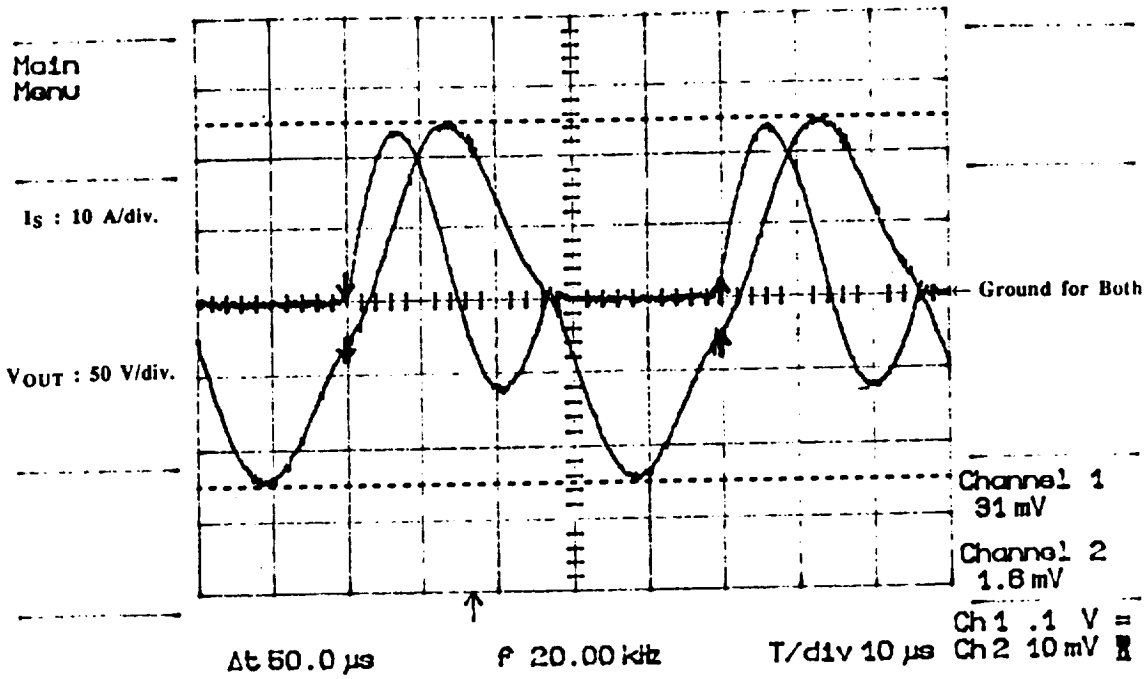



Fig. 2.13. Output Voltage and Switched Current in POSR Circuit. Top Left Trace: Upper Branch Switched Current: $I_S$ : 10 A/div. Bottom Left Trace: Output Voltage: $V_{OUT}$ : 50 V/div. Time/div: 10 µsec.

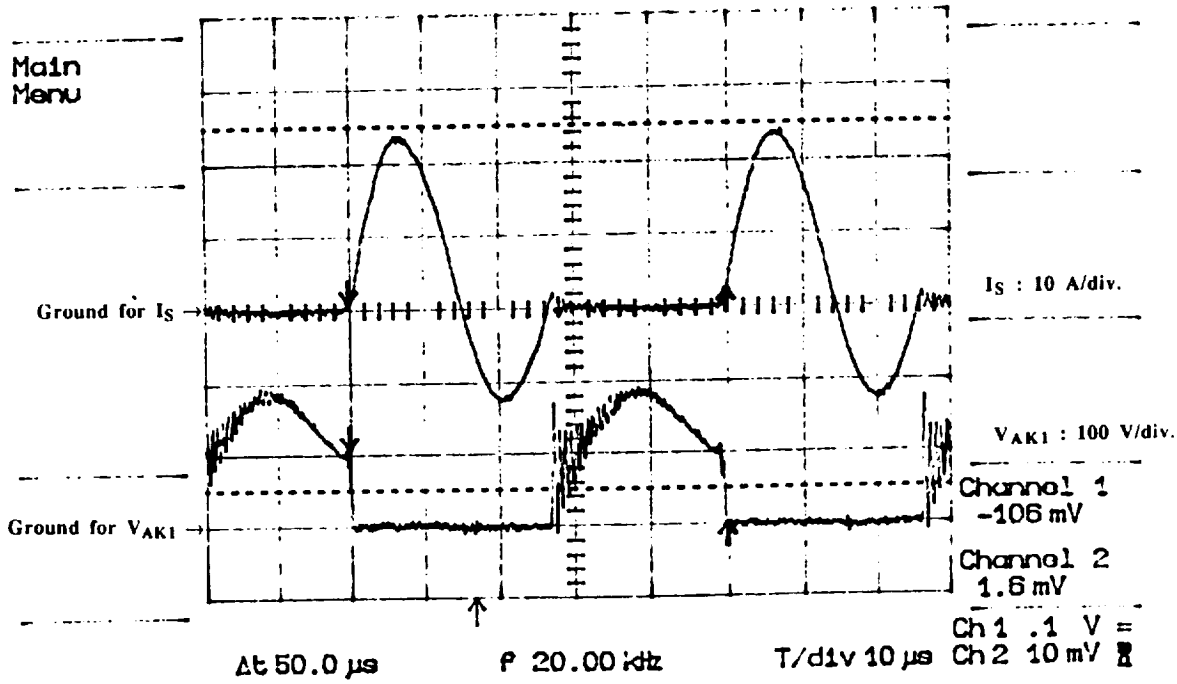



Fig. 2.14. Turn-on and Turn-off of MCT in POSR Circuit. Top Trace: Upper Branch Switched Current: $I_S$ : 10 A/div. Bottom Trace: Upper MCT Anode to Cathode Voltage: $V_{AK1}$ : 100 V/div. Time/div: 10 µsec.

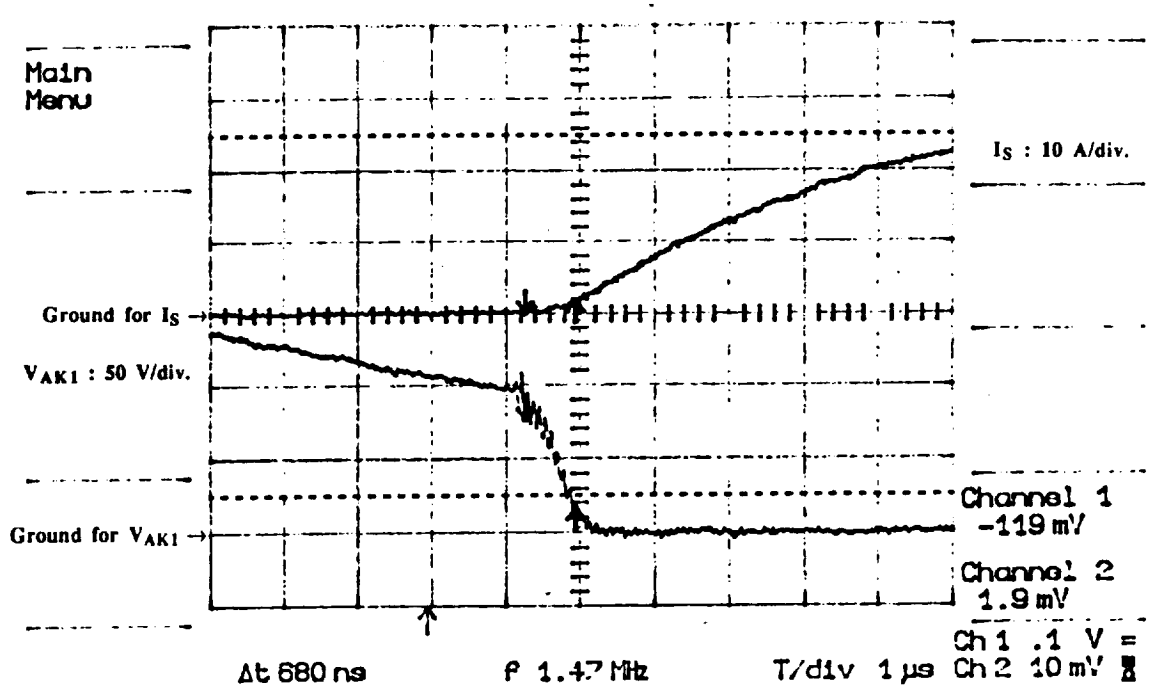



Fig. 2.15. Turn-on Characteristic of MCT with Soft Zero Current Switching. Top Trace: Upper Branch Switched Current: $I_S$ : 10 A/div. Bottom Trace: Upper MCT Anode to Cathode Voltage: $V_{AK1}$ : 50 V/div. Time/div: 1 µsec.

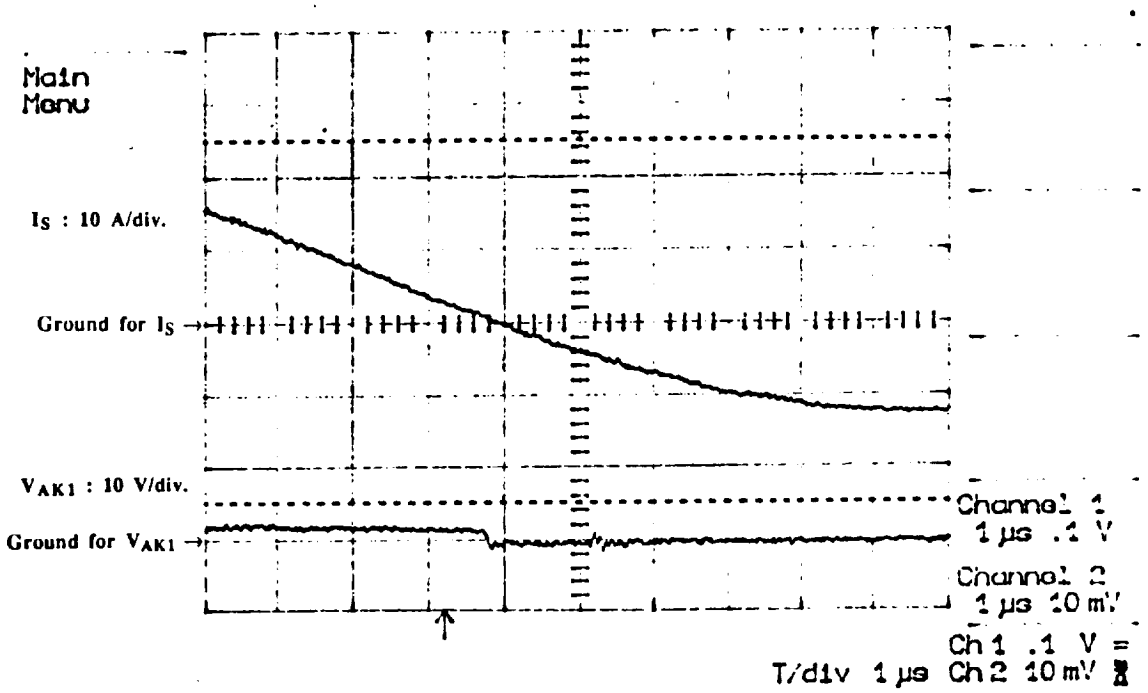



Fig. 2.16. Turn-off Characteristic of MCT with Soft Zero Current Switching.Top Trace: Upper Branch Switched Current: $I_S$ : 10 A/div. Bottom Trace: Upper MCT Anode to Cathode Voltage: $V_{AK1}$ : 10 V/div. Time/div: 1 µsec.

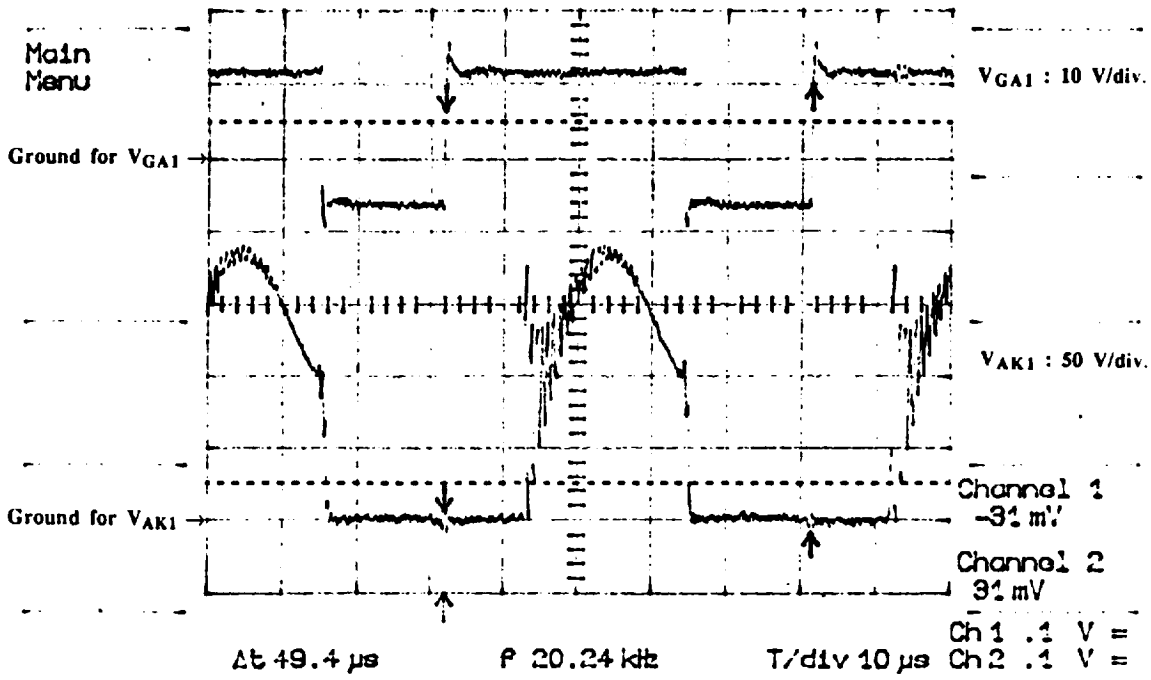
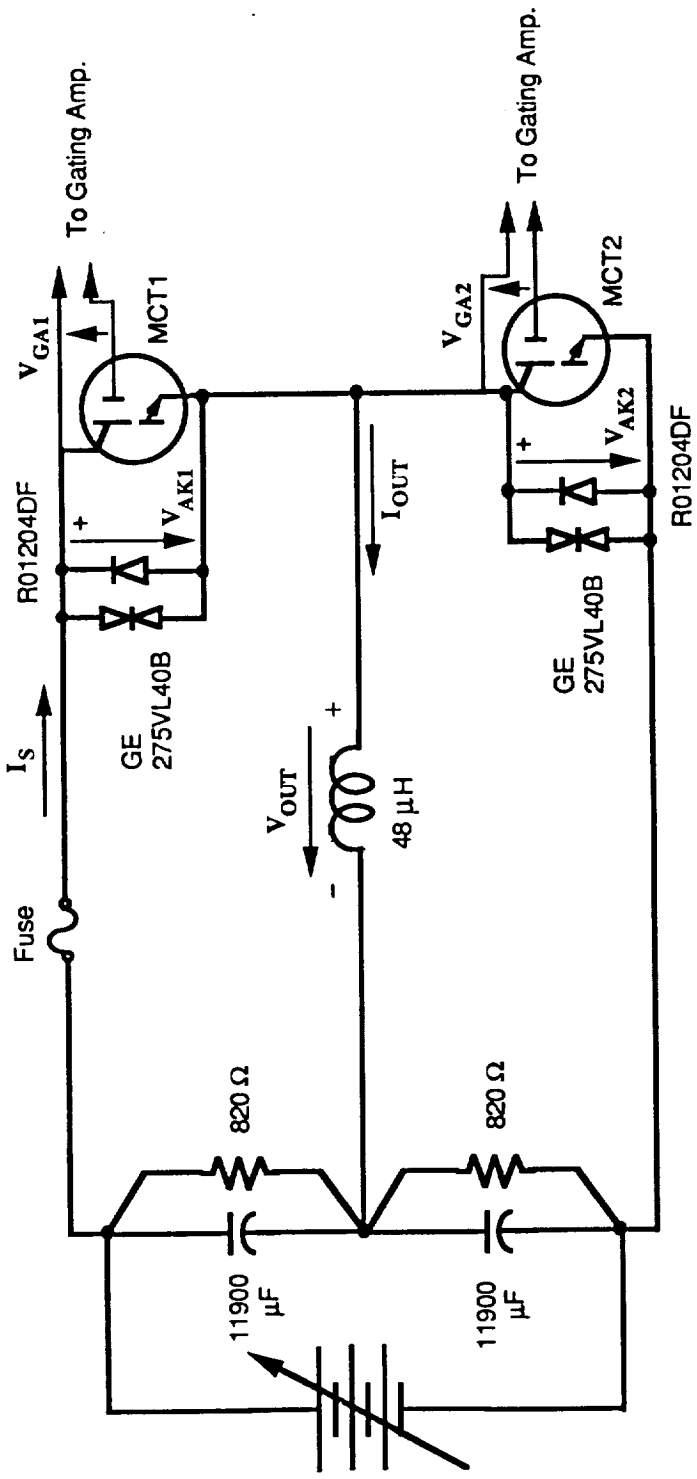



Fig. 2.17. Gating Signal and Device Voltage During Turn-on and Turn-off. Top Trace: Upper MCT Gate to Anode Voltage: $V_{GA1}$ : 10 V/div. Bottom Trace: Upper MCT Anode to Cathode Voltage: $V_{AK1}$ : 50 V/div. Time/div: 10 μsec.




Designed By Seung Ki Sul

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Fig. 2.18. Zero Voltage Switching Test Circuit

waveform. The typical output voltage and current waveforms at 20 kHz operating frequency are shown in Fig. 2.19.

The output voltage waveform clearly shows a glitch in every half cycle. These glitches result from the fact that the switch can not turn on at zero voltage. This fact is even more clear in Figs. 2.20 and 21, where the current and voltage waveforms of the switch are shown. From Fig. 2.20 it can be seen that the turn-off of the MCT has no problem but the turn-on of the device has some difficulty. When the current starts to change the direction from negative to positive, the MCT should carry a positive current immediately because the gating signal for turn-on is already applied across the gate terminals of MCT, which is shown in Fig. 2.21. However, it is clear that the MCT does not turn on immediately. This fact demonstrates that the MCT needs some voltage from anode to cathode for it to turn-on. A detailed view of turn-on of the MCT is shown in Fig. 2.22. Note that it takes about 1.2 μsec and requires about 90 V. between anode and cathode for the MCT to go into full conduction. The same figure shows the change-over of the current from diode to MCT indicating a change in the forward voltage drop of the switch as expected.

Even though the manufacturer of the MCT gives low 'threshold voltage' values around 6 to 7 V, it appears that an MCT requires considerably more voltage across its anode and cathode to turn-on at zero voltage the switching applications. It has been reported that this voltage requirement depends upon the current rating of the on-FET of MCT [7]. Higher current ratings are required for the on-FET of the MCT to reach the necessary PNPN regenerative operation for hard conduction at low anode-cathode voltages. This means in order to achieve turn-on of the MCT at low anode-cathode voltages, the current rating of the on-FET of the MCT should be raised. Hence, application of an MCT in a 20 kHz resonant power conversion system utilizing zero voltage switching scheme appears to be questionable [12]. If the MCT requires the same amount of high voltage to turn-on, it might take several μsec for the device to turn-on since a 20 kHz link voltage waveform has a smaller voltage rise (dv/dt) across the device compared to the sharp turn-on voltage in Fig. 2.22. During this period since both of the devices in any branch of the converter will be OFF, current at the low frequency side will increase the snubber capacitor voltages across the devices. This, in turn, could speed up the turn-on process at the expense of having continuous voltage spikes. The sizes of these spikes and the possible effects on the control circuit boards could be studied and, if desired, further research can be pursued to determine the behavior of such devices with a resonant link application.

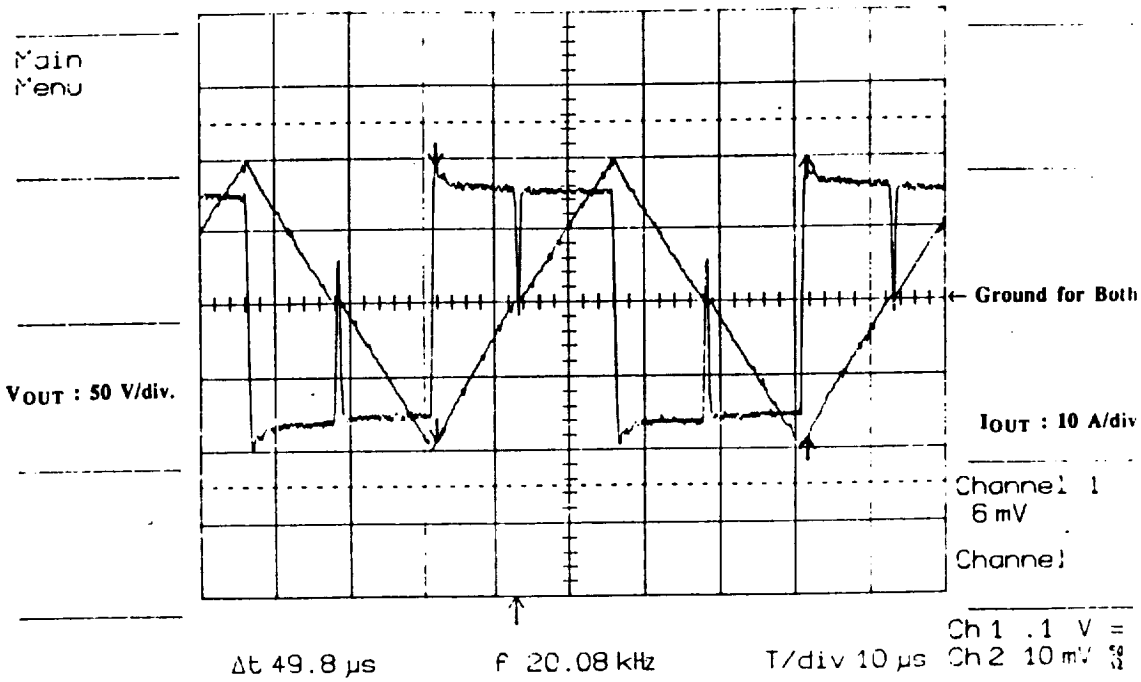


Fig. 2.19. Output Voltage and Current of Zero Voltage Test Circuit Utilizing an MCT. Squarewave Waveform: Output Voltage: $V_{OUT}$ : 50 V/div. Saw-tooth Waveform: Output Current: $I_{OUT}$ : 10 A/div. Time/div: 10 μsec.

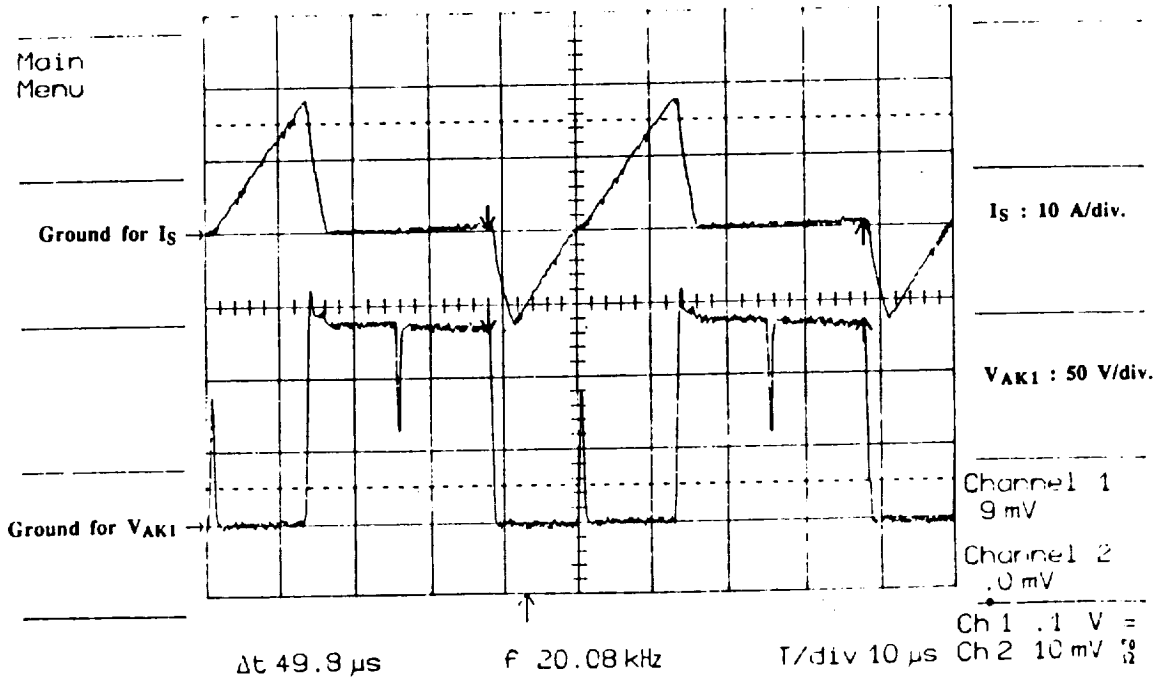


Fig. 2.20. Voltage and Current of MCT Operating in Zero Voltage Test Circuit. Top Trace: Upper Branch Switched Current: $I_S$ : 10 A/div. Bottom Trace: Upper MCT Anode to Cathode Voltage: $V_{AK1}$ : 50 V/div. Time/div: 10 μsec.

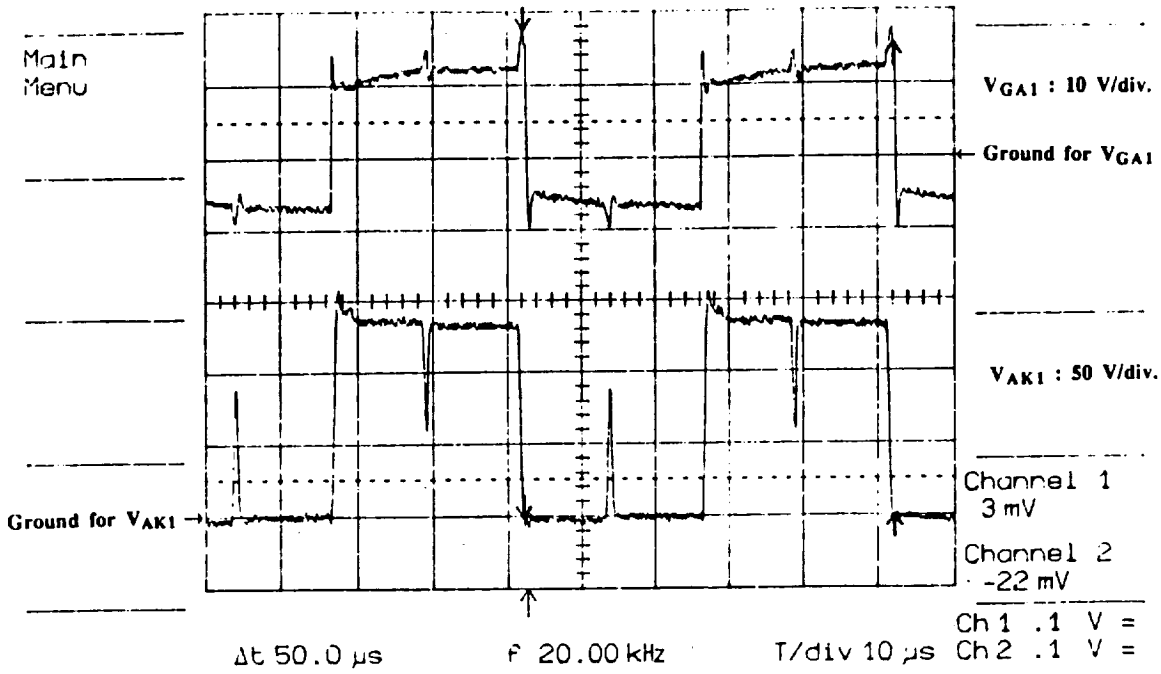


Fig. 2.21. Gating Signal and MCT Voltage Operating in Zero Voltage Test Circuit. Top Trace: Upper MCT Gate to Anode Voltage: $V_{GA1}$ : 10 V/div. Bottom Trace: Upper MCT Anode to Cathode Voltage: $V_{AK1}$ : 50 V/div. Time/div: 10 μsec.

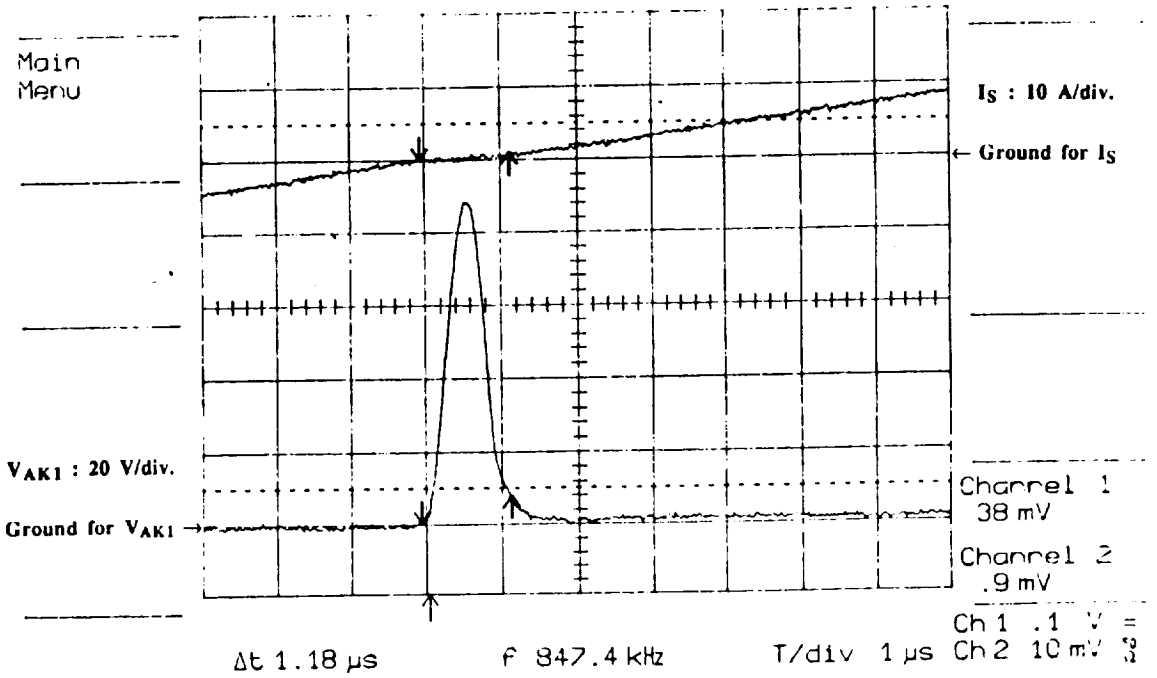


Fig. 2.22. Magnified View of Fig. 2.20 During Current Reversal Instant. Top Trace: Upper Branch Switched Current: $I_S$ : 10 A/div. Bottom Trace: Upper MCT Anode to Cathode Voltage: $V_{AK1}$ : 20 V/div. Time/div: 1 μsec.

### 2.1.5 Measurement of Saturation Voltage.

During the tests the saturation voltage was monitored during the DC conduction period wherein the device is continually conducting. The voltage was measured with a high accuracy Digital Volt Meter. The relation between the saturation voltage and the conduction current is shown in Fig. 2.23. Note that the voltage is only 1.2 V. at 25 A. indicating a very low forward conduction drop.

## 2.2 Test Results of Second Generation Devices

The more recent 80-90 tests are carried out for very short time intervals such as 10-20 msec which is enough to determine the switching characteristics of MCT. The reason for this time interval is to reduce the ratings of the components used in the test power circuits.

A new MCT gate drive chip was also tested for the first time in our lab and found to have some disabilities. After determining that this chip would be useful for our tests, a additional MCT gate drive unit which was developed based the earlier tests was again fabricated with some additional changes to meet the gating requirements of new MCT devices.

Even though faster slew rates for the gate-anode voltage transitions were obtained than the recommended values, the new devices were determined to have problems in "turn-on" and some of them during "turn-off". Even when the device voltage slew rate is reduced at turn-off to prevent turn-off failure, some devices continued to fail to turn-off.

### 2.2.1 MCT Gating Logic and Gate Drive Circuit

The first tests are initiated with the new MCT gate drive chip. The circuit schematic of this gate drive along with the gating logic circuit is given in Fig. 2.24. As mentioned several problems are encountered while using this new MCT gate drive chip. These problems are observed while testing the MCT in a DC-chopper circuit whose schematic is given in Fig. 2.25. One of these problems is an increase in voltage spikes in the gate-anode voltage waveform for increasing operating voltages. This behavior can be witnessed from Figs. 2.26 and 2.27. The operating voltage of the chopper circuit in Fig. 2.26 is only 55 $V_{dc}$, the amplitudes of the spikes were as large as 30 V, whereas in Fig. 2.27, the operation voltage is 75 $V_{dc}$ and the amplitude of the spikes are around 40 V. Another

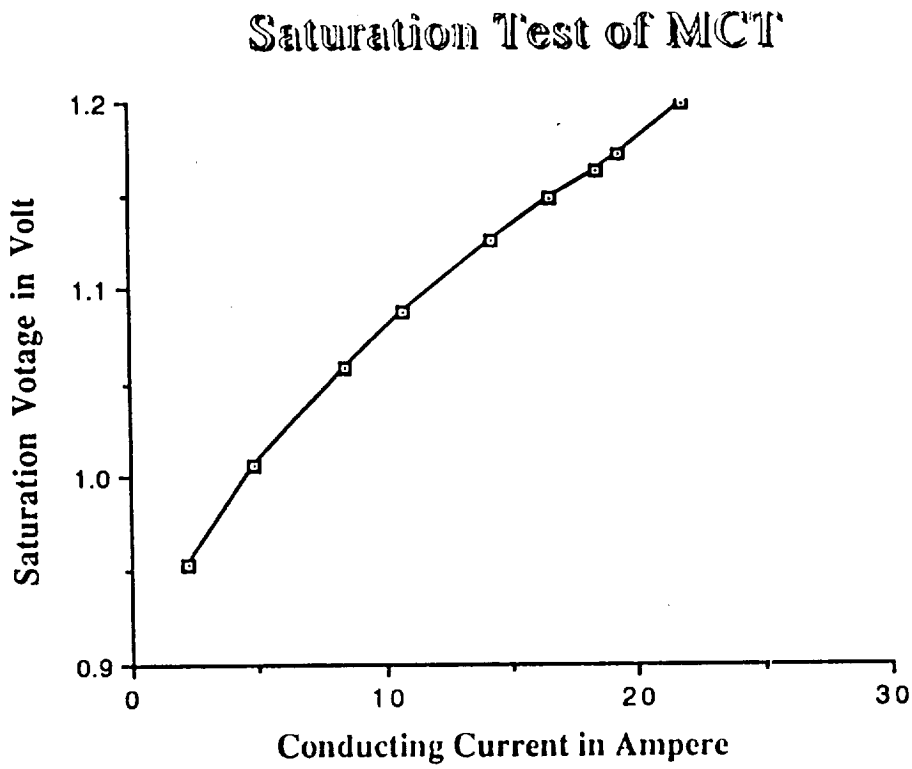


Fig. 2.23. MCT Saturation Voltage versus Conduction Current.

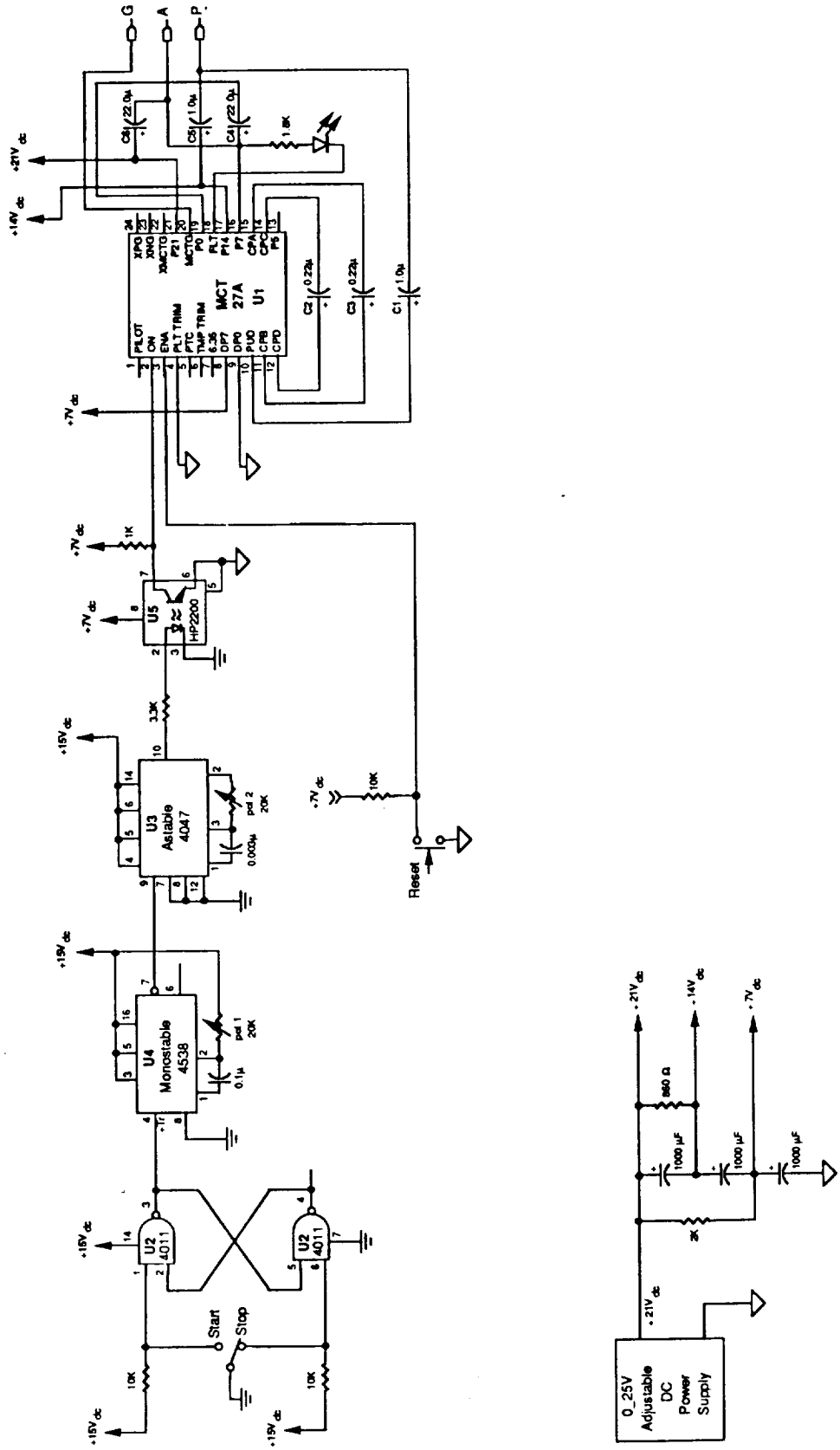


Fig. 2.24 Gating Logic and Gate Drive Unit Utilizing New MCT Drive Chip for the test of Second Generation MCTs.

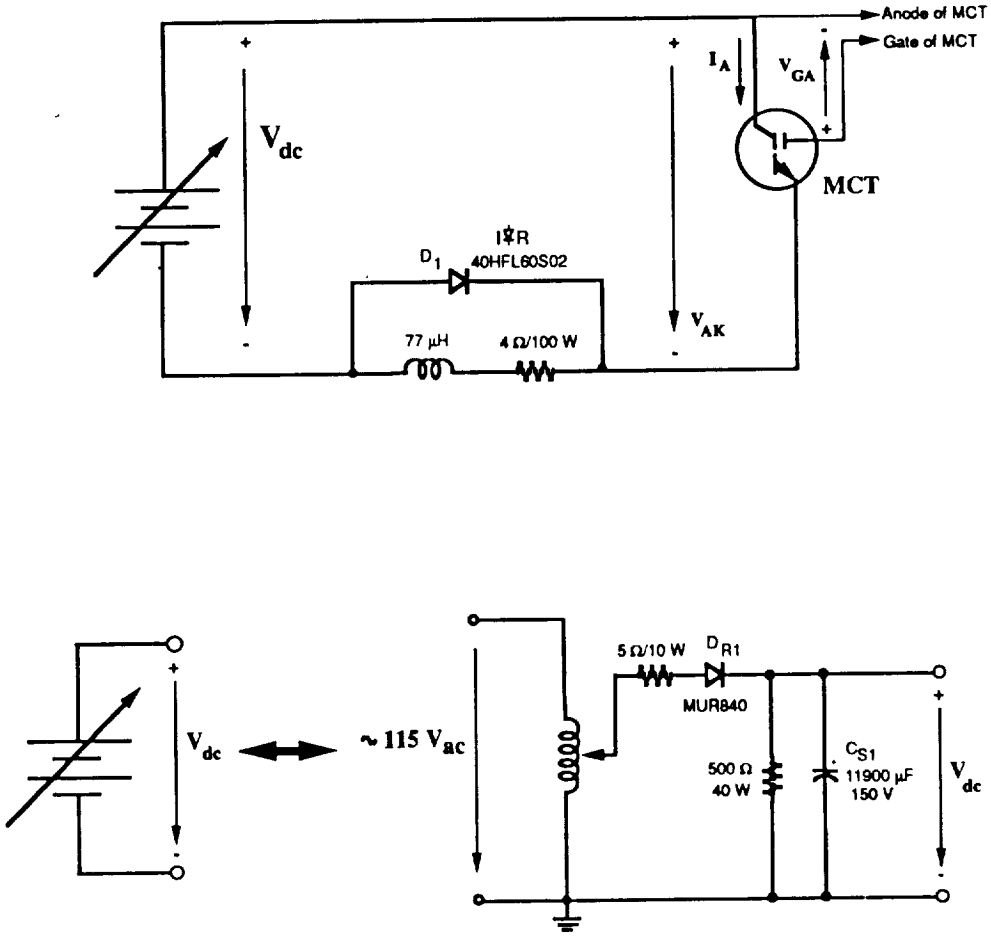


Fig. 2.25 DC Chopper Circuit Schematic for the Determination of Hard Switching Characteristics of Second Generation MCTs.

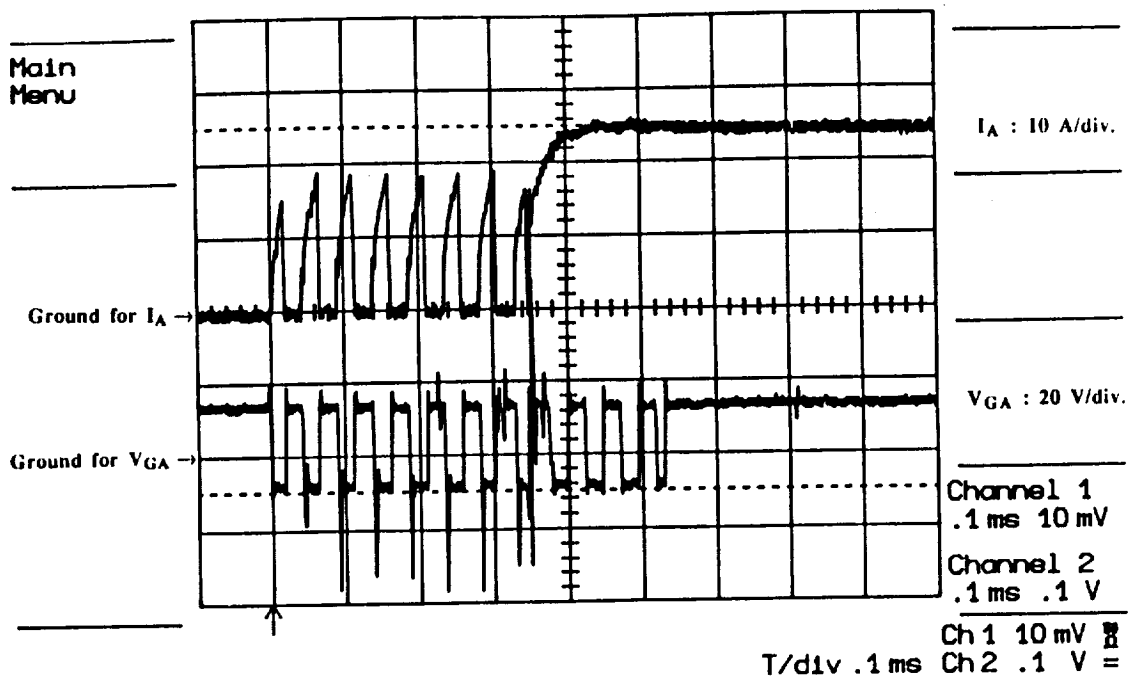


Fig. 2.26. Illustrating Spikes and Unwanted Notches in the Gate to Anode Voltage with the New Drive Chip in Operation. Trace Also Illustrates a Turn-off Failure of the MCT. Top Trace: MCT Anode Current: $I_A$ : 10 A/div. Bottom Trace: MCT Gate to Anode Voltage: $V_{GA}$ : 20 V/div. Time/div: 100 µsec.

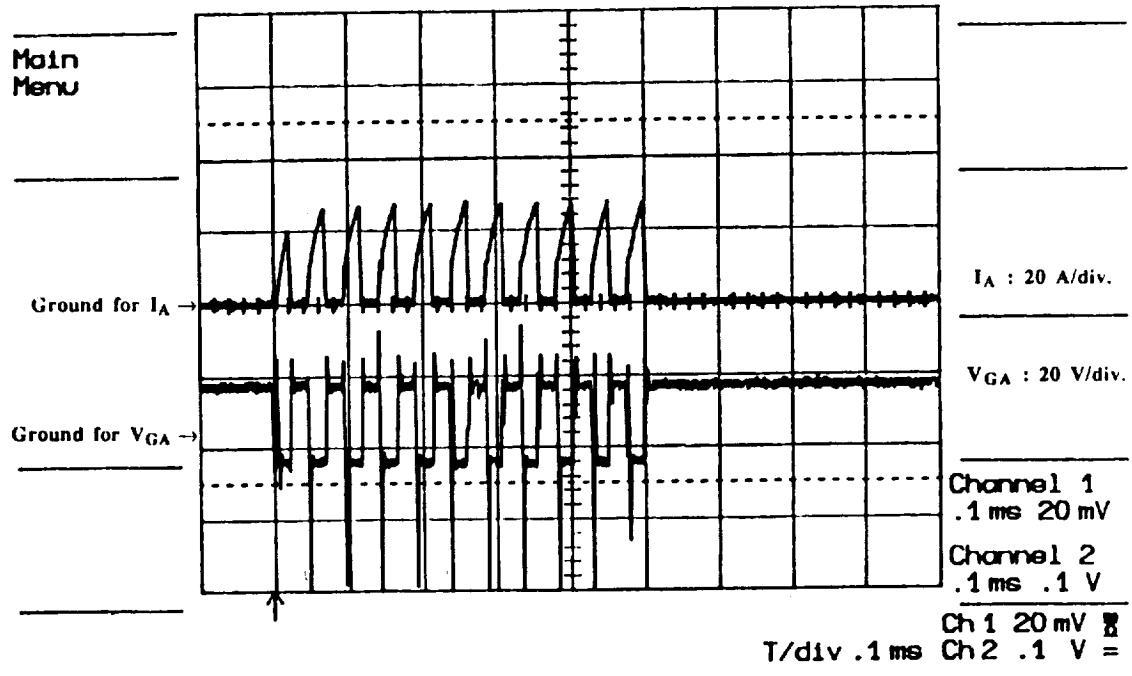


Fig. 2.27. Showing Increasing Spikes in the Gate to Anode Voltage with Increasing Operating Voltage. Top Trace: MCT Anode Current: $I_A$ : 20 A/div. Bottom Trace: MCT Gate to Anode Voltage: $V_{GA}$ : 20 V/div. Time/div: 100 µsec.

problem that was discovered was the unwanted notches in the gate-anode voltage waveforms. Even though the gating logic signal commands one mode of operation such as "on" or "off" , the gate-anode voltage waveform carries the wrong information due to the notches. In severe case these notches even cause the MCT to change its conducting state. One example of this kind is given in Fig. 2.28 with an operating voltage of 14 $V_{dc}$. The unwanted notches are circled so that they are seen more clearly. The same type of event can be observed also from Fig. 2.26 where the operating voltage is 55 $V_{dc}$. Figures 2.26 and 2.28 also reveal very clear turn-off problems for the MCT. Once the MCT turns-on, it does not turn-off when it is commanded. With the proper selection of the operating voltage and the resistor value in the power circuit, around a 25 A. maximum MCT current is obtained even in the turn-off failure case. Fortunately, since all the MCTs are rated for currents larger than 45 A. it was not likely for the MCT to be damaged with the selected current range.

It is worthwhile to mention the point of connection of the P_ terminal in Fig. 2.24. Specifically, the waveforms in Fig. 2.28 are taken while this P_ terminal is connected to the minus terminal of MCT, that is the cathode. The current waveform in this figure reveals that the MCT has a long current tail after turn-off with this type of connection. Figures 2.26 and 2.27 do not reveal this type of current tail since the P_ terminal is not connected to the cathode of the MCT. Therefore, the remainder of the test was carried out without connecting the P_ terminal to the cathode of the MCT, i.e. it was just left open.

Several trials of solutions to remove the spikes in the gate-anode voltage and the unwanted notches did not improve the situation. Hence, the gate drive unit was replaced with a specially designed unit with some minor changes for the first generation gate driver to meet the new recommendations. This gate drive unit along with the gating logic is given in Fig. 2.29. For the devices tested last year, the recommended gate drive voltages were -5 V or -7 V for turn-on and +10 V to +15 V for turn-off with a 200 nsec rise time. However, for the new devices, while the turn-on recommendations changed to -7 V or -15 V., turn-off recommendations remained the same.

With the new gate drive unit we did not experience any spike or notch problems. However, the turn-off problem remained unsolved. Since the gate drive requirements were more than adequately satisfied with our redesigned gate driver, it was believed that the possible reason for continued turn-off failure was due to the rate of change of device voltage. In other words, a very high dV/dt device voltage rate retriggers he MCT before it turns-off. With the utilization of modified version of last years gate drive unit this behavior can be observed from Fig. 2.30. This figure clearly shows the absence of spike or notch problem a failure to turn-off is apparent. To overcome the turn-off failure problem a turn-

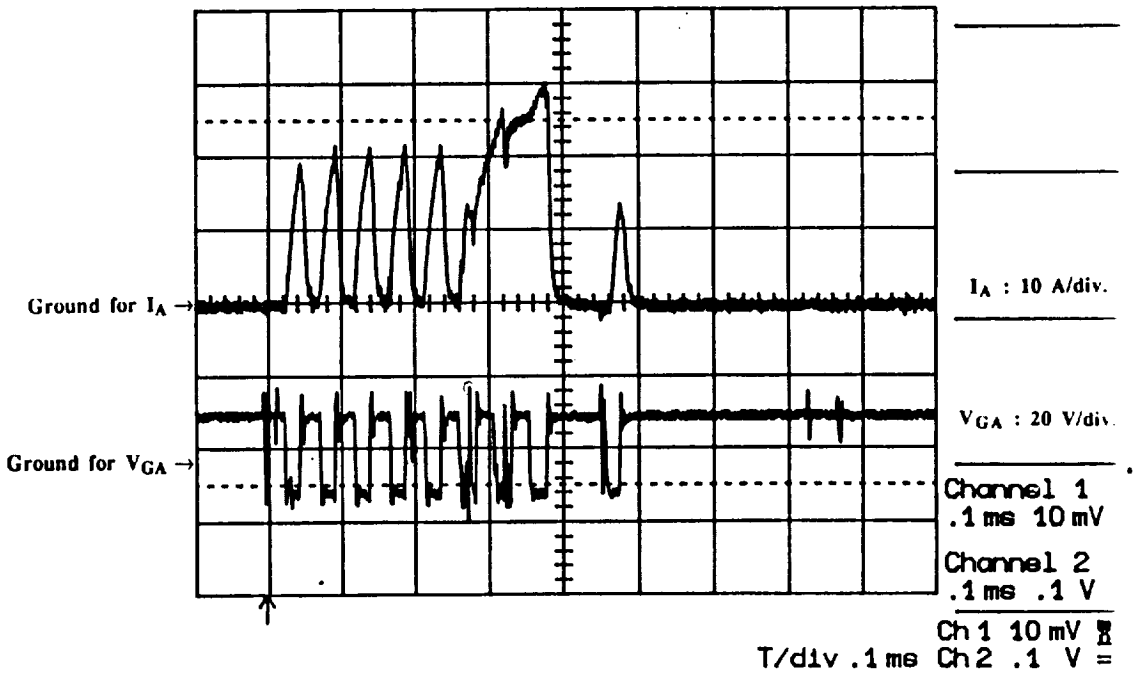


Fig. 2.28. Showing Unwanted Notches in the Gate to Anode Voltage and Illustrating Turn-off Failure of MCT. Top Trace: MCT Anode Current: $I_A$ : 10 A/div. Bottom Trace: MCT Gate to Anode Voltage: $V_{GA}$ : 20 V/div. Time/div: 100 μsec.

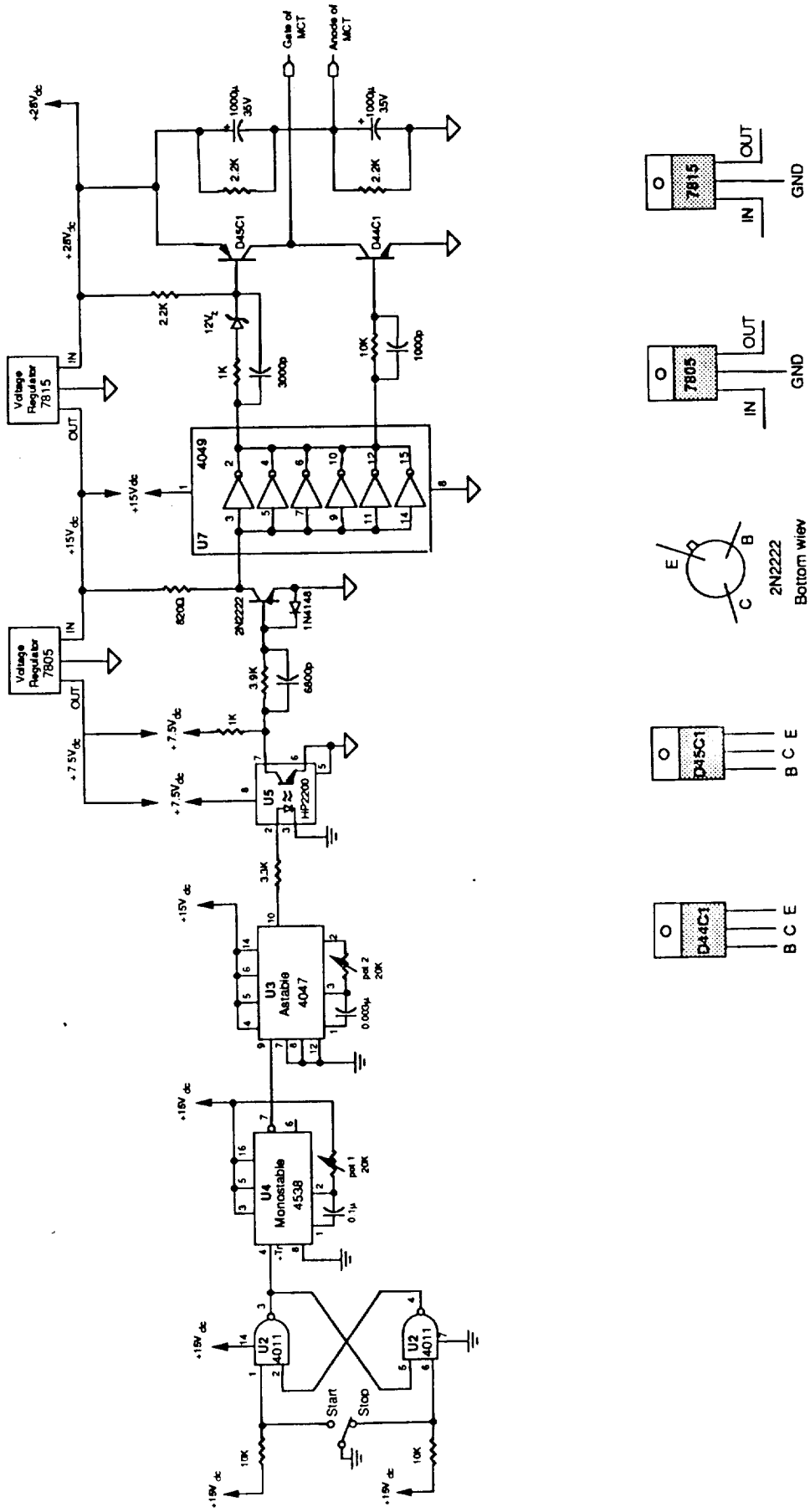


Fig. 2.29. Utilization of Gate Drive Unit Used For Test of First Generation Devices Showing Additional Modifications to Satisfy New Gate Drive Requirement.

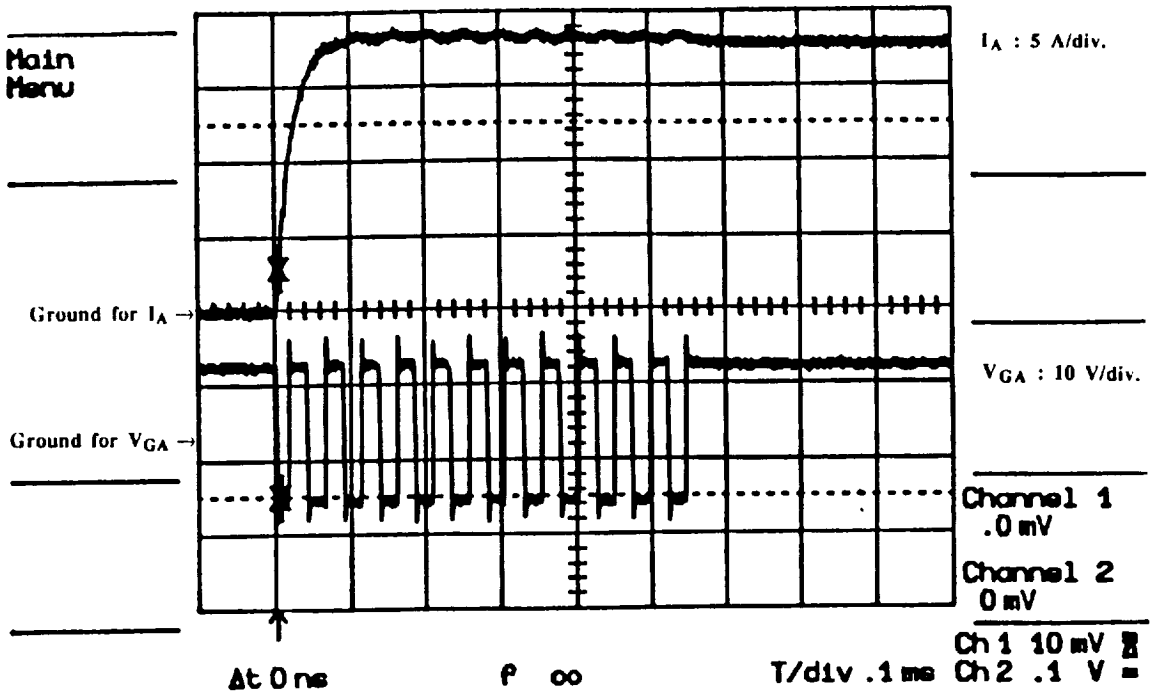


Fig. 2.30. Illustrating Clean Gate to Anode Voltage with New Gate Drive Unit but Showing Continued Existence of Turn-off Failure. Top Trace: MCT Anode Current: $I_A$ : 5 A/div. Bottom Trace: MCT Gate to Anode Voltage: $V_{GA}$ : 10 V/div. Time/div: 100 µsec.

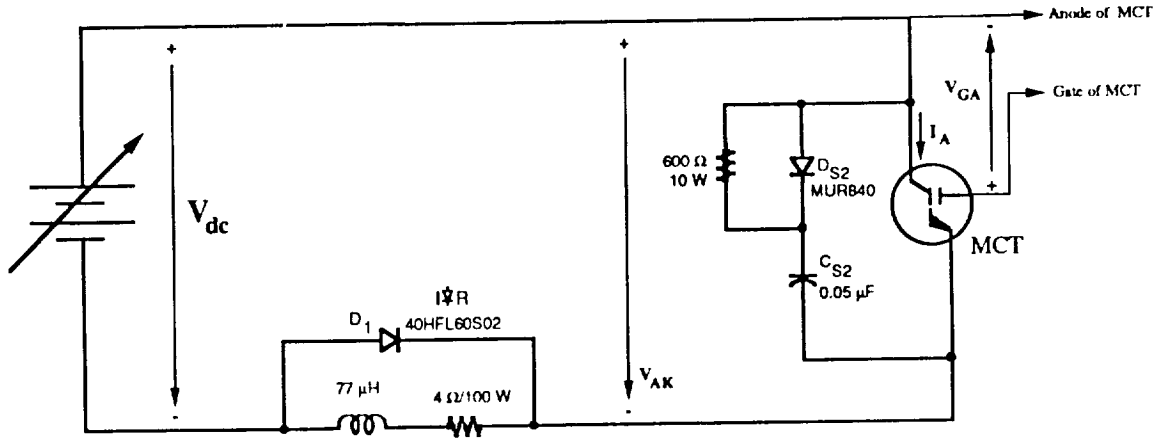


Fig. 2.31 DC Chopper Circuit Schematic for the Determination of Hard Switching Characteristics of Second Generation MCTs with Turn-off Snubber Added in Parallel with the MCT.

off snubber was added across the MCT terminals so that the rate of change of device voltage could be reduced at turn-off. The power circuit layout of DC-chopper circuit with turn-off snubber is given in Fig. 2.31. After the addition of a turn-off snubber the following dv/dt rates were recorded with increasing operating voltages; 77 V./μs for 34 V. operation, 88 V./μs for 52 V. operation and 128 V./μs for 70 V. operation. Continuous successful operation could be maintained with the addition of the snubber.

### 2.2.2 Hard Switching Characteristics of Second Generation MCT

Fig. 2.31 shows the power circuit layout of DC chopper circuit used to determine the hard switching characteristics of second generation MCT. This test is carried out at a 20 kHz operating frequency. One reason for turn-off failures encountered might well be due to this high operating frequency.

During the test, high voltage spikes are observed during turn-off of the device. These spikes are essentially due to the stray inductance of the wiring layout of the power circuit. Fortunately, the voltage ratings of MCTs are on the order of 1400 V. and operating voltage is at around 150 V. so that devices were not lost. Also, only the switching characteristics of the device were of concern at this point so that these spikes were not examined carefully. Turn-on and turn-off of the second generation MCT is given in Fig. 2.32. Here, one can observe that the spikes at turn-off are more than twice the value of the operating voltage itself.

The turn-on gating characteristic of an MCT is given in Fig. 2.33. This figure reveals that the MCT gate anode voltage has a 250 nsec fall time from +12.5 V. to -12.5 V. The device requires a negative gate current of amplitude 2 A. for about 400 ns for turn-on. The large spike in the gate-anode voltage which appears almost 1μs after reaching -12.5 V. is an induced voltage at turn-on most probably due to turn-off snubber discharge.

Turn-on delay of the MCT corresponding to the time gate signal is applied to the time 10% of the current is reached is pictured with Fig. 2.34. This figure reveals almost a 1 μs turn-on delay. The reason for the spike in the gate anode voltage is the same as before. To determine the total turn-on time of the MCT the rise time of the device current is also needed. The rise time is defined to be the time from 10% to 90% of the device current during turn-on. This time is pictured with Fig. 2.35. The rise time in this figure is approximately 250 ns. Hence, together with turn-on delay this result reveals a 1.25 μs total turn-on time for the device.

The turn-off gating characteristic of the second generation MCT is given in Fig. 2.36. As can be seen from the figure about a 100 ns rise time exists from -12.5 to +12.5

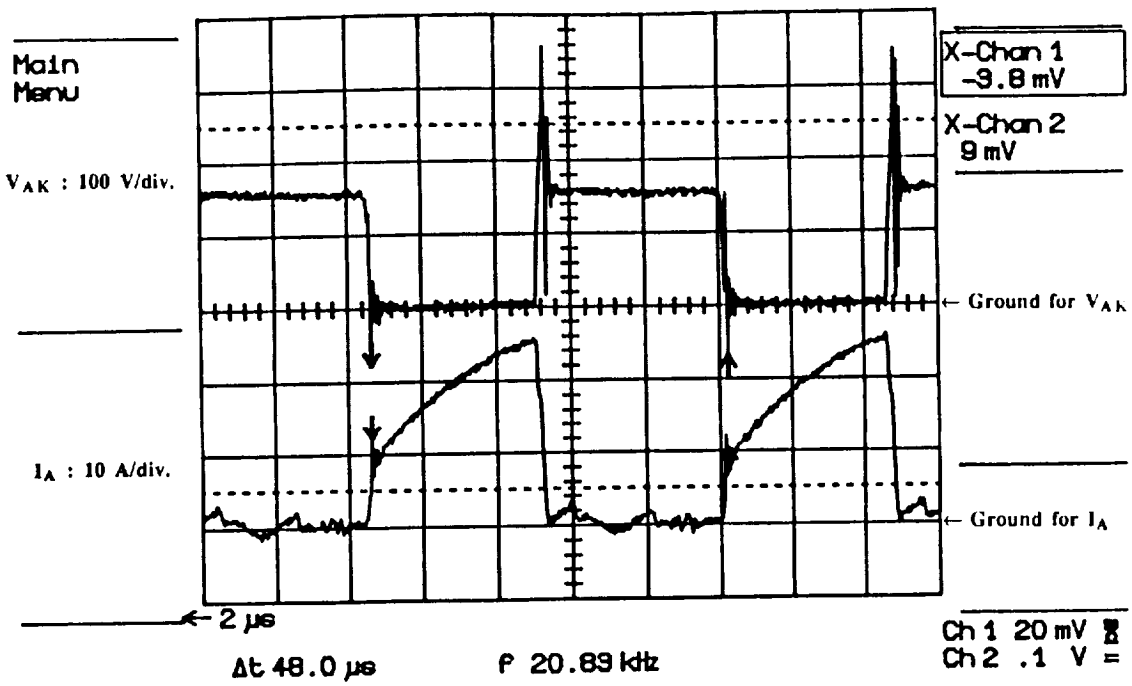


Fig. 2.32. Turn-on and off of the Second Generation MCT Showing High Voltage Spikes Across the Device Due to Stray Inductance of the Power Circuit Layout. Top Trace: MCT Anode to Cathode Voltage: $V_{AK}$ : 100 V/div. Bottom Trace: MCT Anode Current: $I_A$ : 10 A/div. Time/div: 10 µsec.

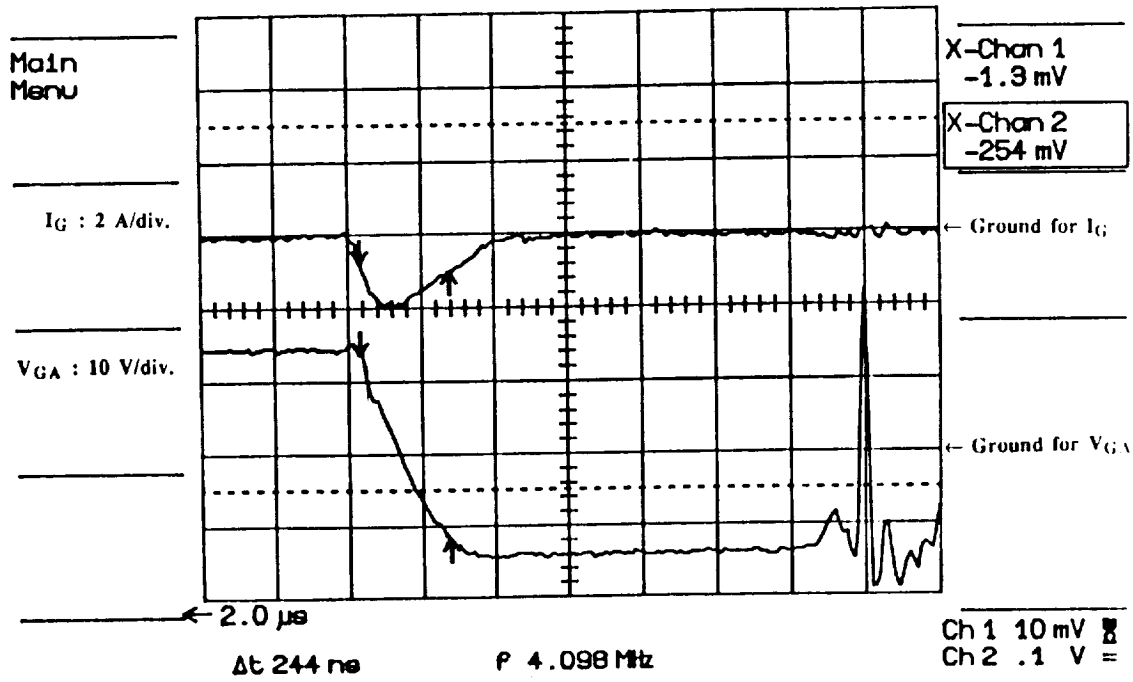


Fig. 2.33. Turn-on Gating Characteristics of the Second Generation MCT Showing High Voltage Spike in the Gate to Anode Voltage Due to Induced Voltage at the Turn-on Instant of the MCT. Top Trace: MCT Gate Current: $I_G$ : 2 A/div. Bottom Trace: MCT Gate to Anode Voltage: $V_{GA}$ : 10 V/div. Time/div: 200 nsec.

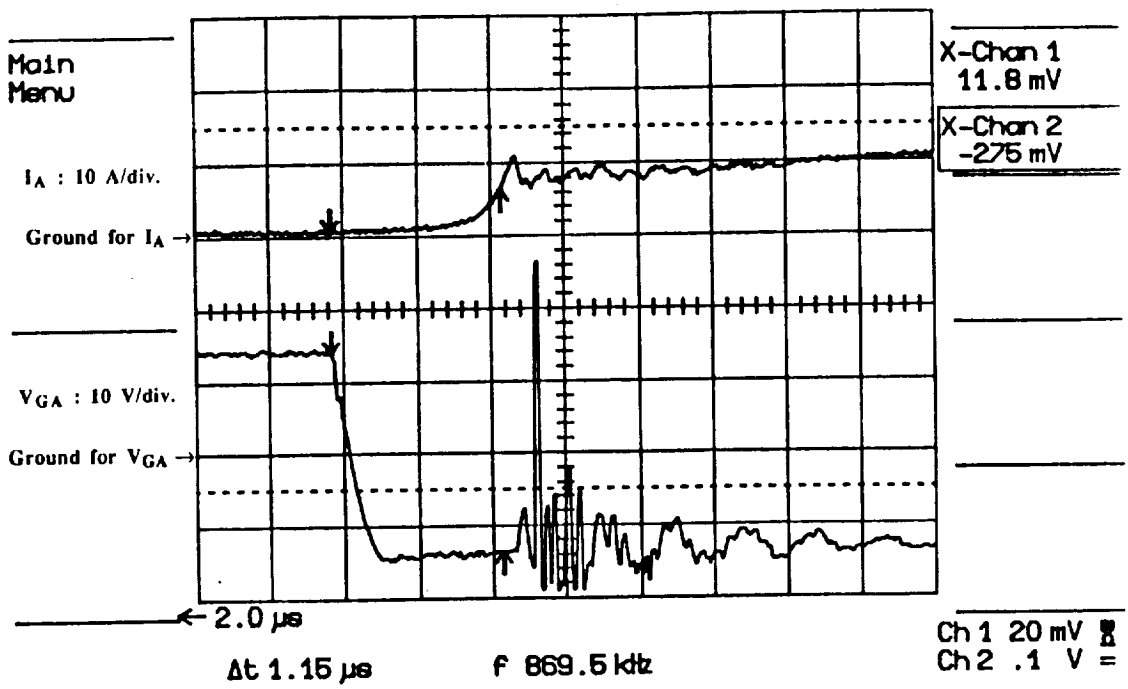


Fig. 2.34. Showing Turn-on Delay of the Second Generation MCT Indicating Voltage Spike in the Gate to Anode Voltage Due to Induced Voltage at the Instant of Turn-on of the MCT. Top Trace: MCT Anode Current: $I_A$ : 10 A/div. Bottom Trace: MCT Gate to Anode Voltage: $V_{GA}$ : 0 V/div. Time/div: 500 nsec.

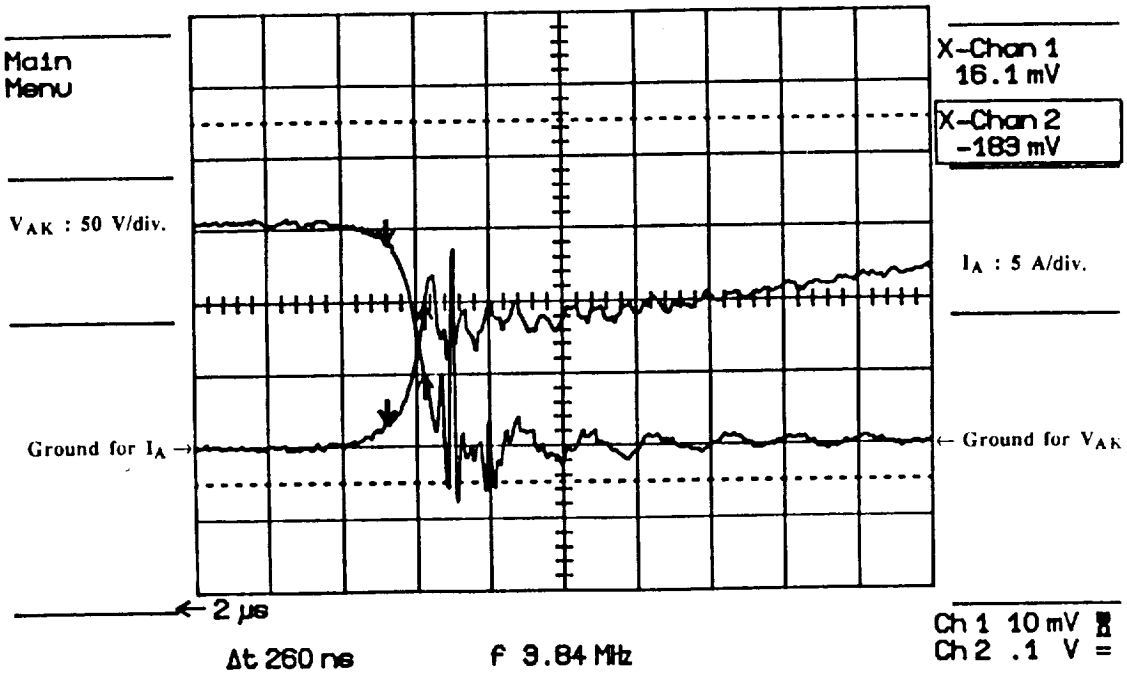


Fig. 2.35. Showing Rise Time of the Second Generation MCT. Top Left Trace: MCT Anode to Cathode Voltage: $V_{AK}$ : 50 V/div. Bottom Left Trace: MCT Anode Current: $I_A$ : 5 A/div. Time/div: 500 nsec.

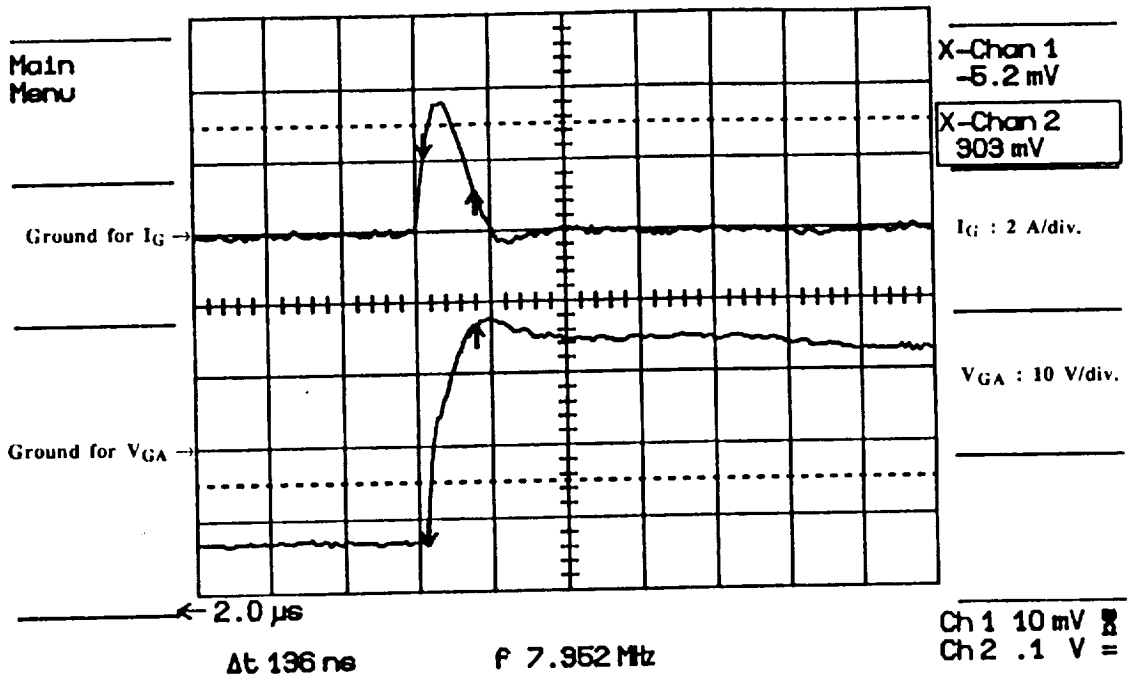


Fig. 2.36. Turn-off Gating Characteristics of the Second Generation MCT. Top Trace: MCT Gate Current: $I_G$ : 2 A/div. Bottom Trace: MCT Gate to Anode Voltage: $V_{GA}$ : 10 V/div. Time/div: 200 nsec.

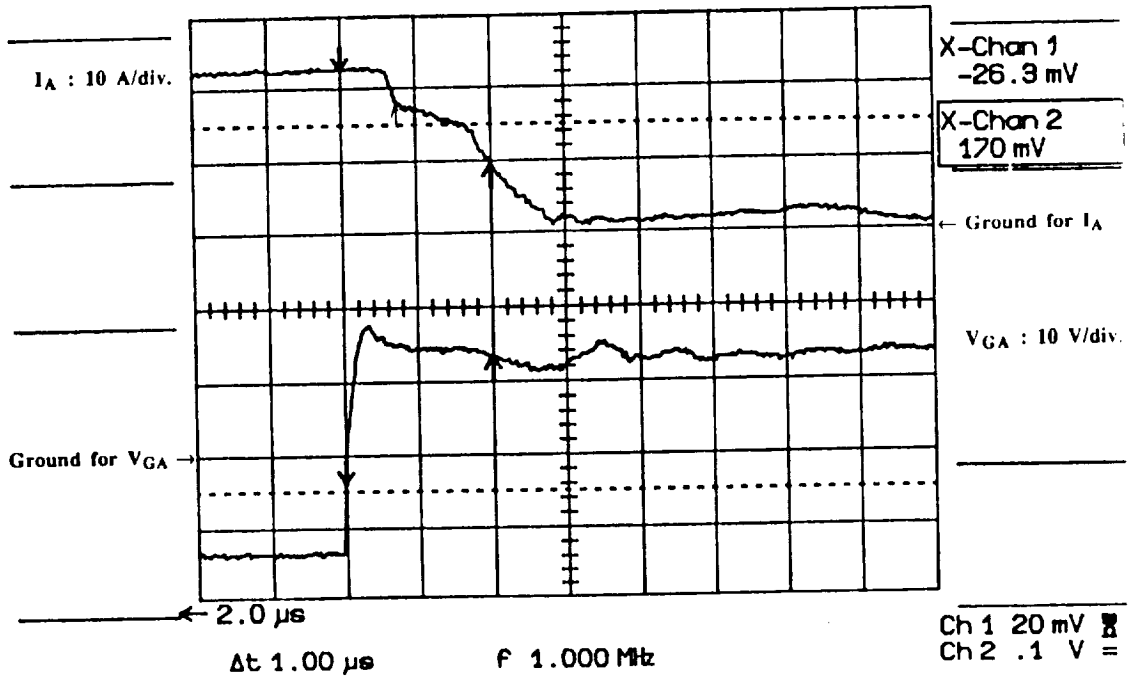


Fig. 2.37. Illustrating Turn-off Delay of the Second Generation MCT.Top Trace: MCT Anode Current: $I_A$ : 10 A/div. Bottom Trace: MCT Gate to Anode Voltage: $V_{GA}$ : 10 V/div. Time/div: 500 nsec.

for the gating voltage. This indicates a 250 V/μs dv/dt for gate voltage at turn-off. The recommended gate drive from the previous data of the first generation device is 200 ns rise time from -5 V or -7 V to +10 V or +15 V at turn-off which implies a max 100 V/μs dv/dt for the gate drive. Thus, the measured dv/dt is considerably faster than the recommended value. Figure 2.36 reveals that the MCT requires a positive gate current of amplitude close to 4 A for about 200 ns for good turn-off.

Figure 2.37 shows the turn-off delay or storage time of the MCT. The turn-off delay is defined to be the time interval from the time the gate signal is applied to the time 90% of current is reached. This time can be determined from Fig. 2.37 to be about 350 ns. Since there is a turn-off snubber, some of the current is diverted to the snubber circuit at the beginning of the turn-off instant which is the reason for the high droop in the MCT current observed at the beginning of turn-off. However, later when the snubber capacitor is charged, the slope is reduced and returned to the normal value. The fall time of the device current is defined to be from 90% to 10% of the value prior to turn-off and from Fig 2.38 corresponds to approximately 1.0 μs. Hence, a total 1.35μsec turn-off time exists for the MCT whose characteristics were measured.

An overview of turn-on and off of an MCT during hard switching is given in Fig. 2.39. The device current and the gating signal is shown for condition corresponding to about 20 kHz and 150 V operation. Unfortunately, hard switching tests of the TO-3 case MCT devices could not be carried out because of their built-in problems associated with the case. In particular, when the gate drive is connected to their gate to anode, the turn-off gate anode voltage drops to zero from +12.5 V. and a low frequency oscillation develops with increasing operating voltage. This behavior can be observed from Fig. 2.40 and its magnified version shown in Fig. 2.41. The operating voltage for this case is about 23 V. Thinking that the gate anode terminals might be specified wrongly, we repeated the test by changing gate anode terminals. This time even though the gate anode voltage remained reasonable, the current through the device was clearly abnormal. This behavior is pictured with Fig. 2.42 for 13 V. operation.

At this point, it is useful to compare the hard switching test results of MCT with the results taken from the earlier tests results. Table 2.1 has been prepared for this purpose. It is important to note again that the major difference between these two test is that a turn-off snubber utilization in the second generation test. In the earlier tests no snubber circuit was used.

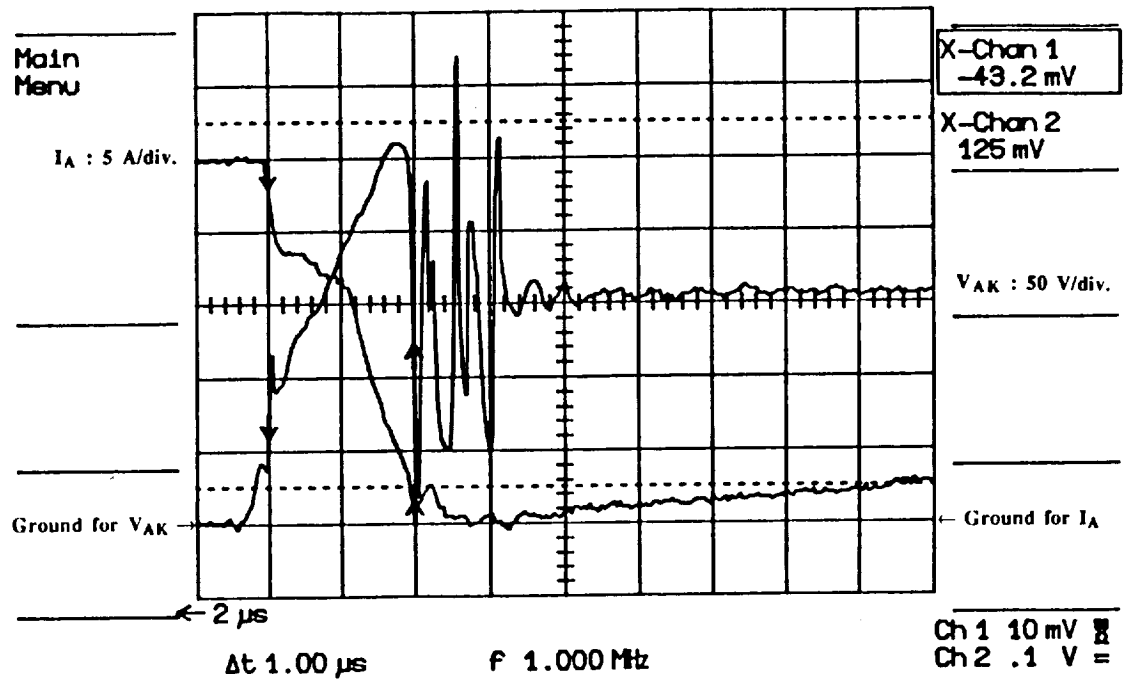


Fig. 2.38. Trace Showing Fall Time of the Second Generation MCT Current Indicating Ringing and Spikes in the Device Voltage Due to Stray Inductance and Capacitances. Top Left Trace: MCT Anode Current: $I_A$ : 5 A/div. Bottom Left Trace: MCT Anode to Cathode Voltage: $V_{AK}$ : 50 V/div. Time/div: 500 nsec.

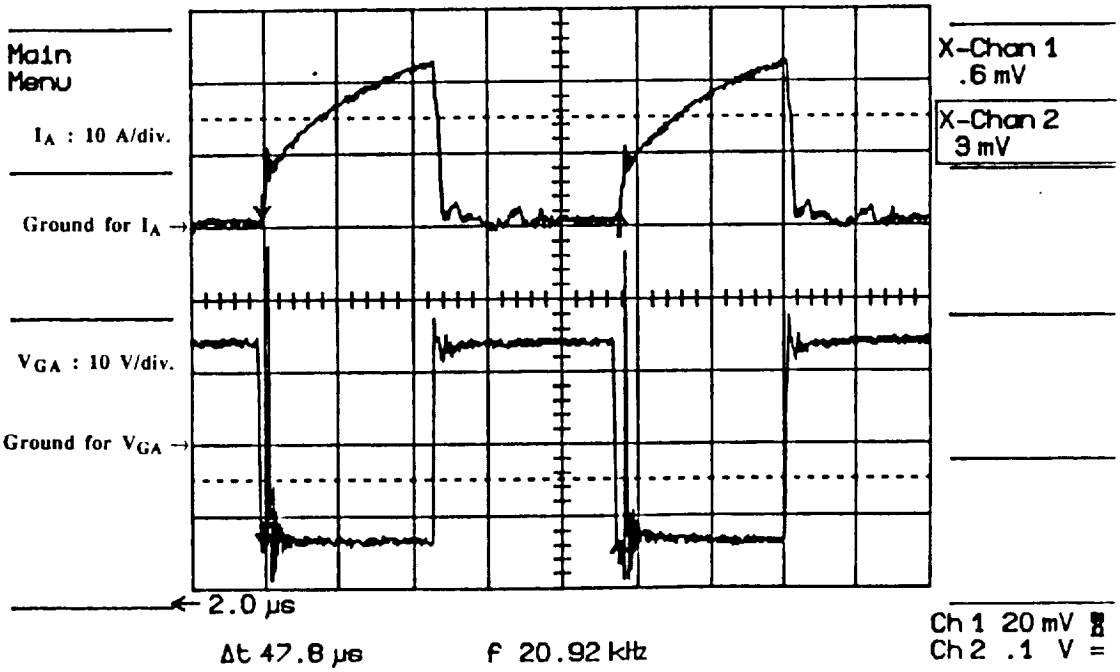


Fig. 2.39. Trace Showing Overall Second Generation MCT Behavior During Turn-on and Turn-off. Top Trace: MCT Anode Current: $I_A$ : 10 A/div. Bottom Trace: MCT Gate to Anode Voltage: $V_{GA}$ : 10 V/div. Time/div: 10µsec.

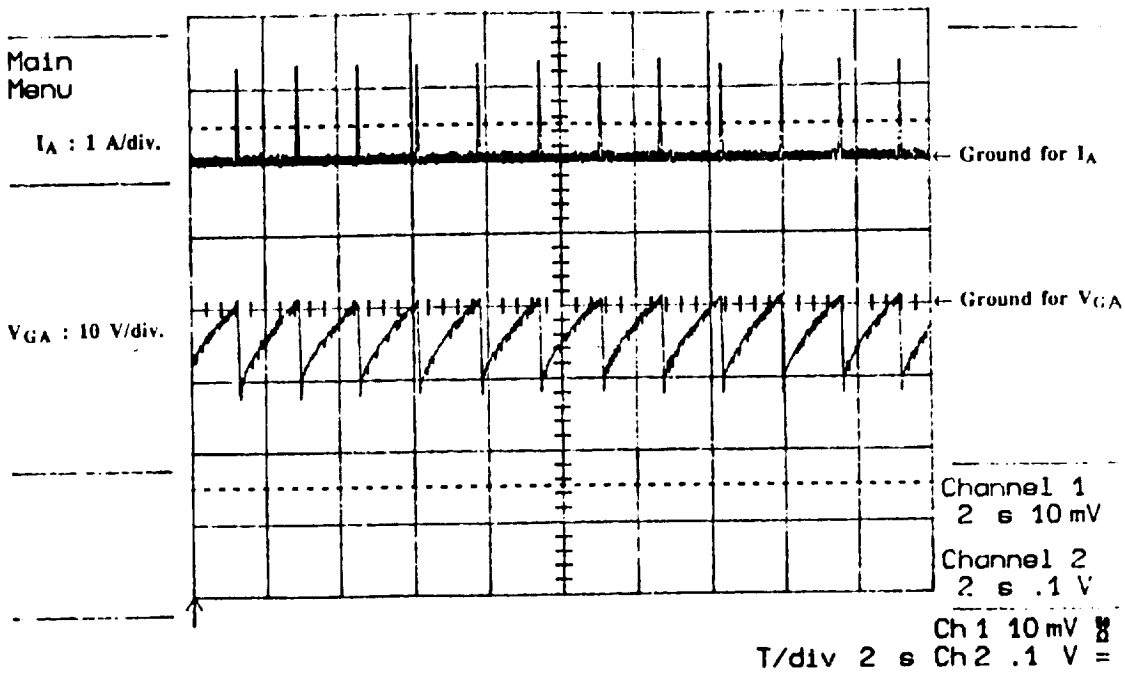


Fig. 2.40. Showing Test of MCT Device Mounted in a TO-3 Package. Top Trace: MCT Anode Current: $I_A$ : 1 A/div. Bottom Trace: MCT Gate to Anode Voltage: $V_{GA}$ : 10 V/div. Time/div: 2 sec.

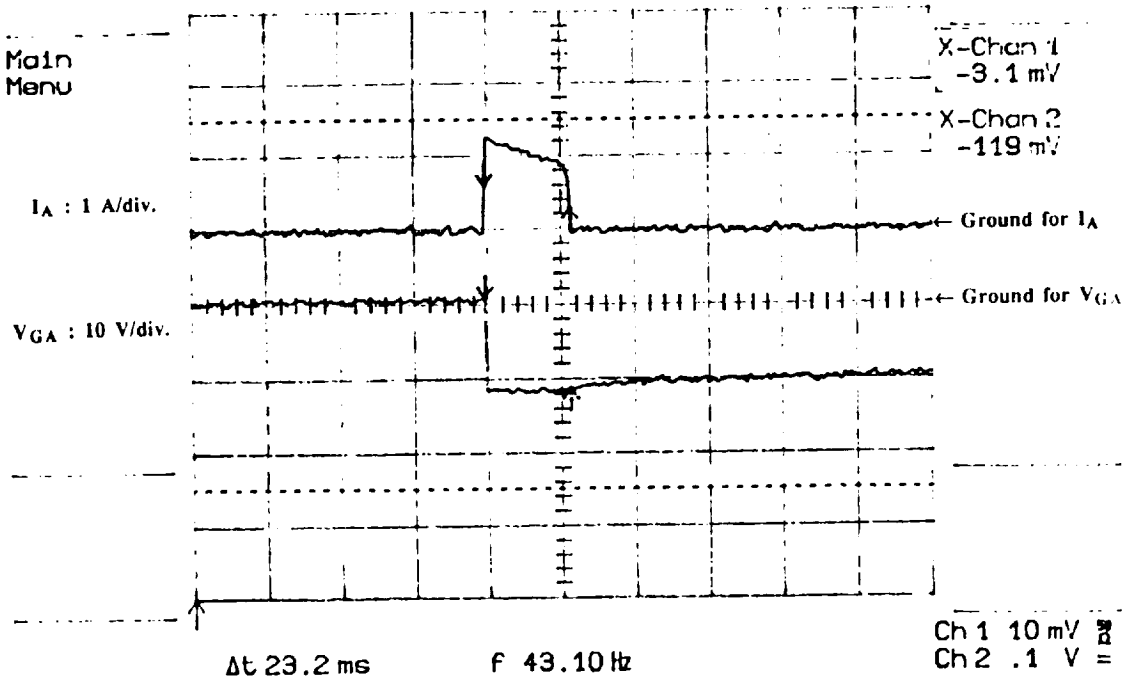


Fig. 2.41. Magnified View of Fig. 2.40 Illustrating Slow Rise in the Gate to Anode Voltage. Top Trace: MCT Anode Current: $I_A$ : 1 A/div. Bottom Trace: MCT Gate to Anode Voltage: $V_{GA}$ : 10 V/div. Time/div: 20 msec.

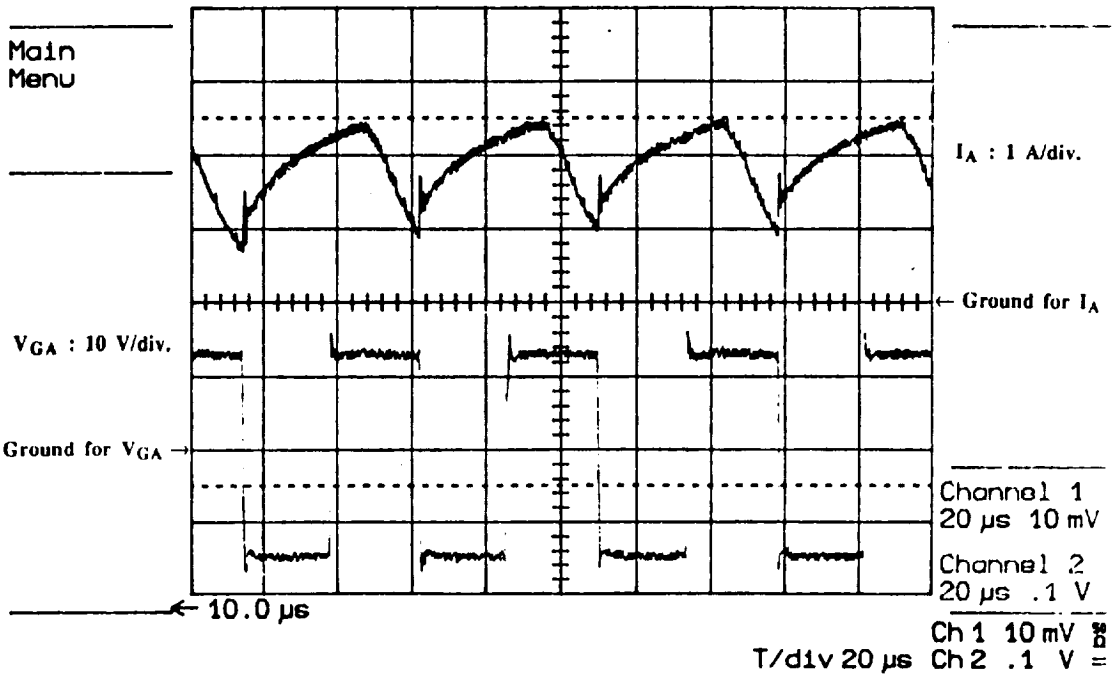


Fig. 2.42. Test of Device in TO-3 Case with Reverse Voltage Applied from Gate to Anode. Top Trace: MCT Anode Current: $I_A$ : 1 A/div. Bottom Trace: MCT Gate to Anode Voltage: $V_{GA}$ : 10 V/div. Time/div: 20 µsec.

| PARAMETERS | | | First Generation MCT | Second Generation MCT |
|---|---|---|---|---|
| Gating Signal | Current | ON | -2.2 A | -2 A |
| | | OFF | 2.1 A | 3.5 A |
| | Voltage | ON | 12 V → -6 V | 12.5 V → -12.5 V |
| | | OFF | -6 V → 12 V | -12.5 V → 12.5 V |
| | Duration | ON | 320 ns | 250 ns |
| | | OFF | 320 ns | 100 ns |
| Switching Speed | Turn on Delay | | 720 ns | 1.0 µs |
| | Rise time | | 360 ns | 250 ns |
| | Turn off Delay | | 520 ns | 1.0 µs |
| | Fall Time | | 1.5 µs | 350 ns |

Table 2.1. Comparison of Hard Switching Test Result for the First and Second Generation MCT Devices.

### 2.2.3 Zero Voltage Switching Characteristics of Second Generation MCT

In general, the discussion of Section 2.1.4 especially the last paragraph also applies for the second generation device. A similar series of tests, discussed in Section 2.1.4 were also carried out for the new MCTs. In the first series of tests, the simple circuit given in Fig. 2.43 was used The operating frequency was chosen to be 10 kHz and the frequency was governed by an astable multivibrator. Capacitors paralleled to the devices in this figure are used to reduce the dv/dt at turn-off of MCTs to prevent possible turn-off failure due to a high dv/dt rating. Due to the double gate drive unit requirement, another isolated gate drive unit had to be built for this purpose. Figure 2.44 shows the entire gating circuit schematic required for this test.

During our first trial run, testing with 60 V. operating voltage, the lower MCT failed to turn-off as can be seen from Fig. 2.45. Figure 2.46 shows related gate anode voltages for both devices. By comparing Figs. 2.45 and 2.46 one can determine that initially current builds up in the upper MCT. When the turn-off command is given to the upper MCT, this current diverts to the anti parallel diode connected to the lower MCT. When the turn-on command is given to the lower MCT, the current builds up in this device, yet, when the turn-off command is given, it does not turn-off at all. Even operation of the fast acting fuse does not save the MCT.

The damaged MCT led us to take more complicated preventive measures against turn-off failures. Figure 2.47 shows the revised power circuit layout for the zero voltage switching test. The logic of the protection circuit is as follows. Protection inductors are chosen accordingly to prevent the rapid change in the current if a shoot through occurs. During normal operation, the currents through these inductors are almost constant and do not affect the operation of the circuit significantly. When the related MCT in the upper or lower loop is turned off, the stored energy in the protection inductor is circulated through the paralleled free wheeling diode. If a shoot through occurs because of a turn off failure of one device, this shoot through current can not increase rapidly because of the protection inductors, during this incident "over current" is detected with a current LEM sensor and power darlingtons are commanded to turn-off before the MCTs are damaged. Even the fuses are sized to blow earlier than the MCTs because of the continuous but low sloped shoot through current. The operation of protection circuit is shown in Figs. 2.48 and 2.49 with the damaged MCT. The protection now operates much faster for increased operating voltages because "over current" level is reached quickly. Figures 2.48 and 2.49 show this behavior. This damaged device is numbered as 18AU30A.

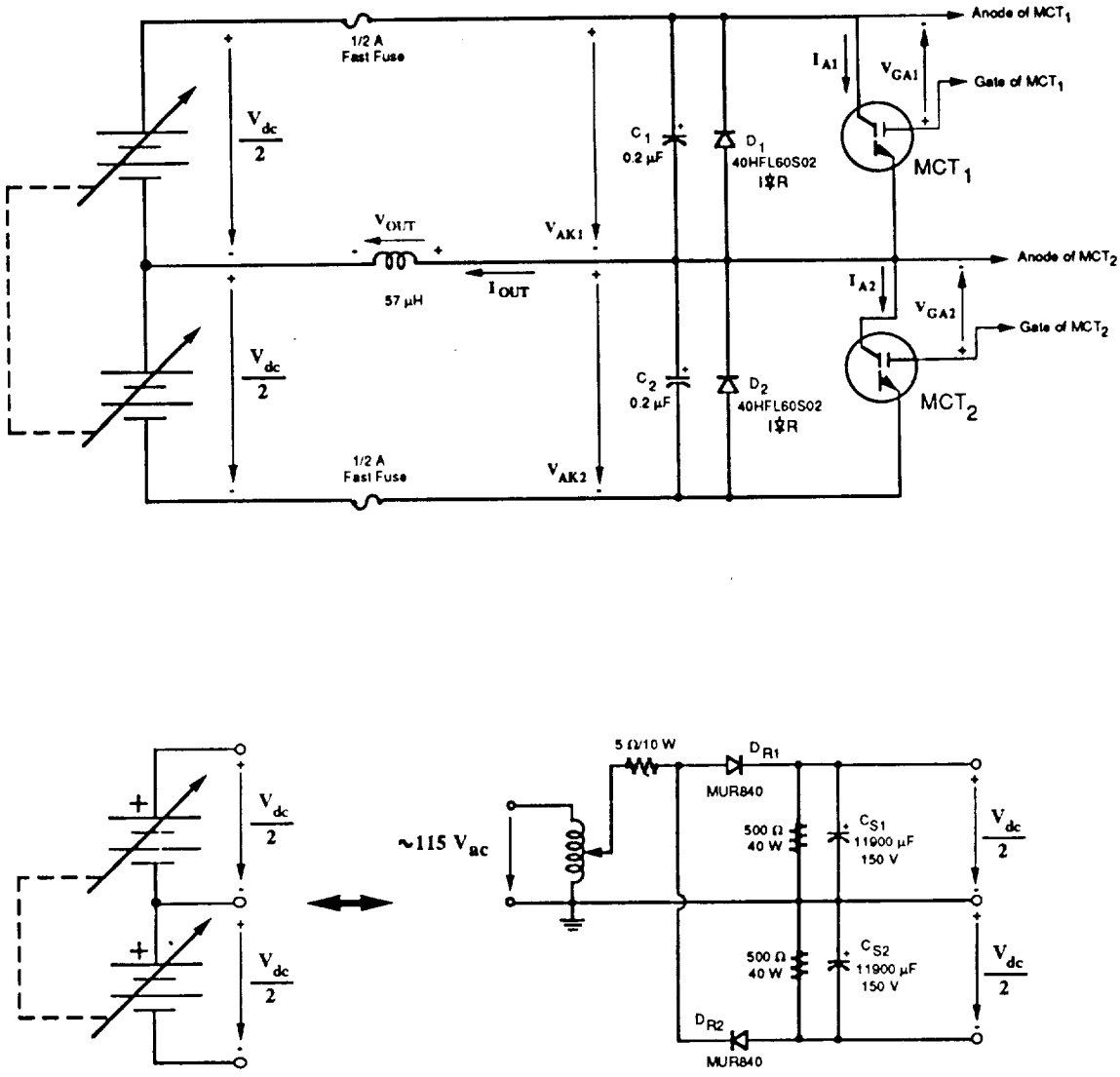


Fig. 2.43. Power Circuit Layout for Zero Voltage Switching Tests for the Second Generation MCTs.

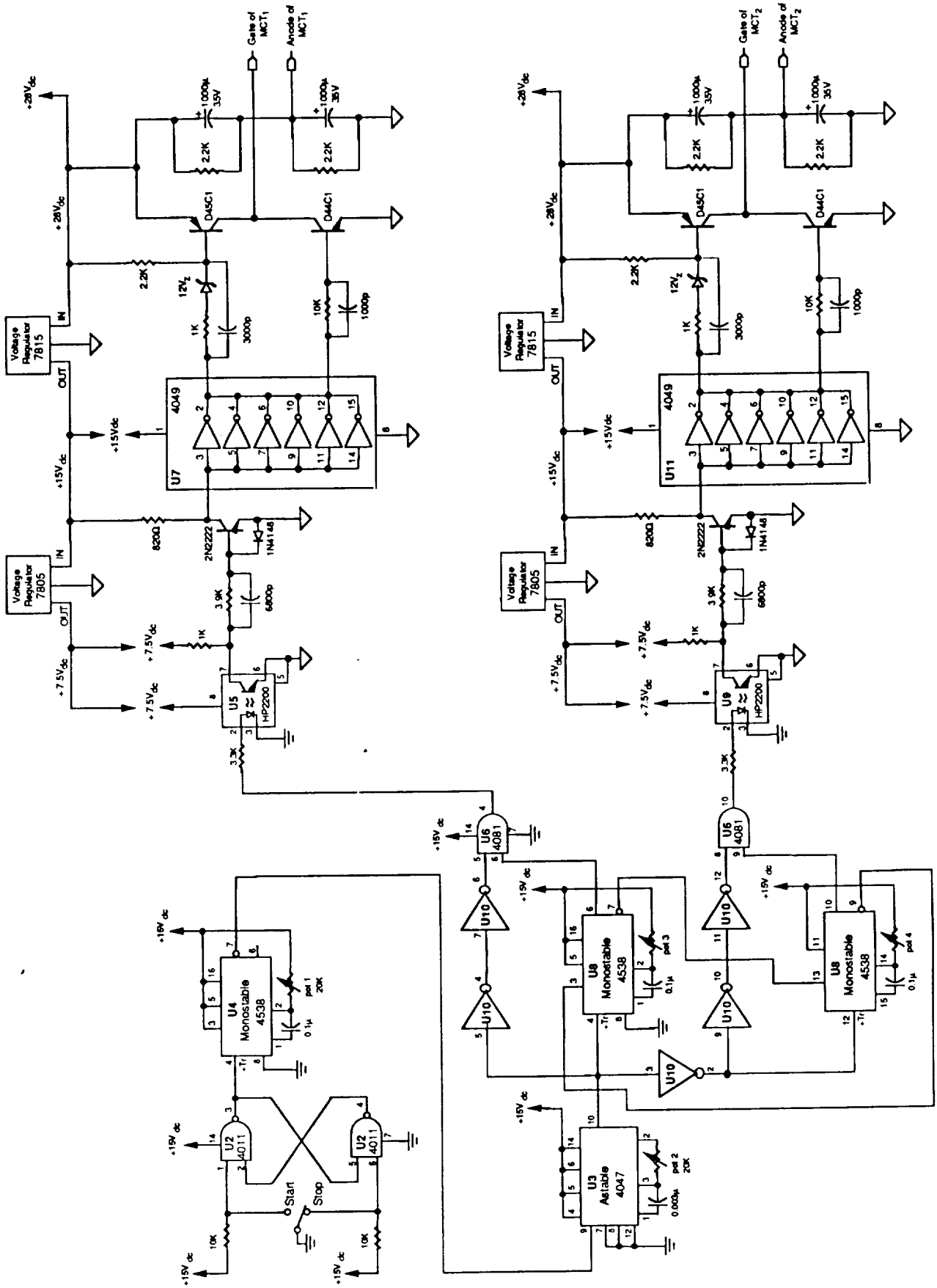


Fig. 2.44. Isolated Gate Drive Units Together with Their Gating Logic Units Used for the Soft Voltage and Current Switching Tests of the Second Generation MCTs.

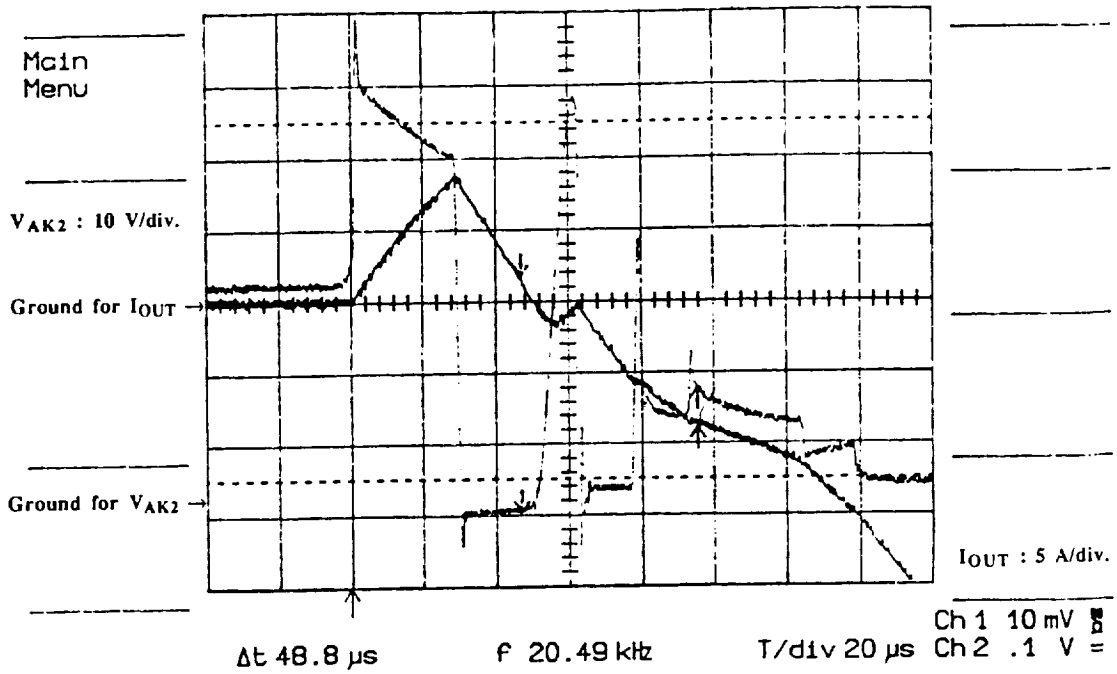


Fig. 2.45. Lower MCT (18AU30A) Voltage and Current Illustrating Instant of Device Failure. Top Left Trace: Lower MCT Anode to Cathode Voltage: $V_{AK}$ : 10 V/div. Bottom Left Trace: Output (Inductor) Current: $I_{OUT}$ : 5 A/div. Time/div: 20 μsec.

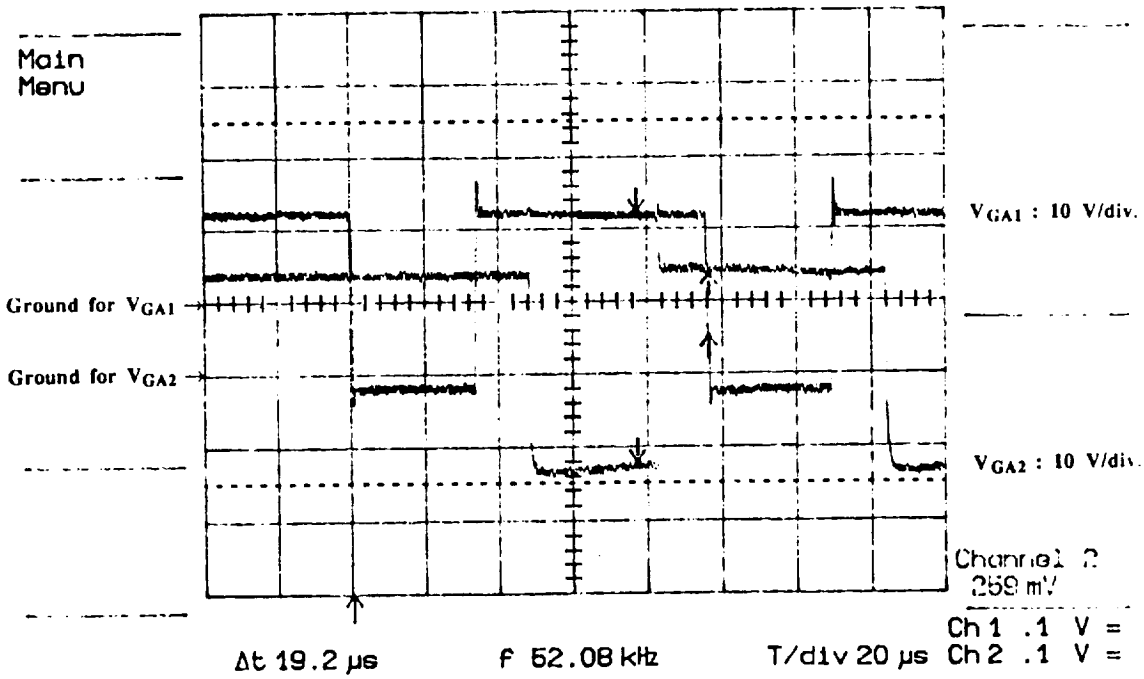


Fig. 2.46 Related Gate Drive Signals Corresponding to Fig. 2.45 During Device Failure. Top Trace: Upper MCT Gate to Anode Voltage: $V_{GA1}$ : 10 V/div. Bottom Trace: Lower MCT Gate to Anode Voltage: $V_{GA2}$ : 10 V/div. Time/div: 20 μsec.

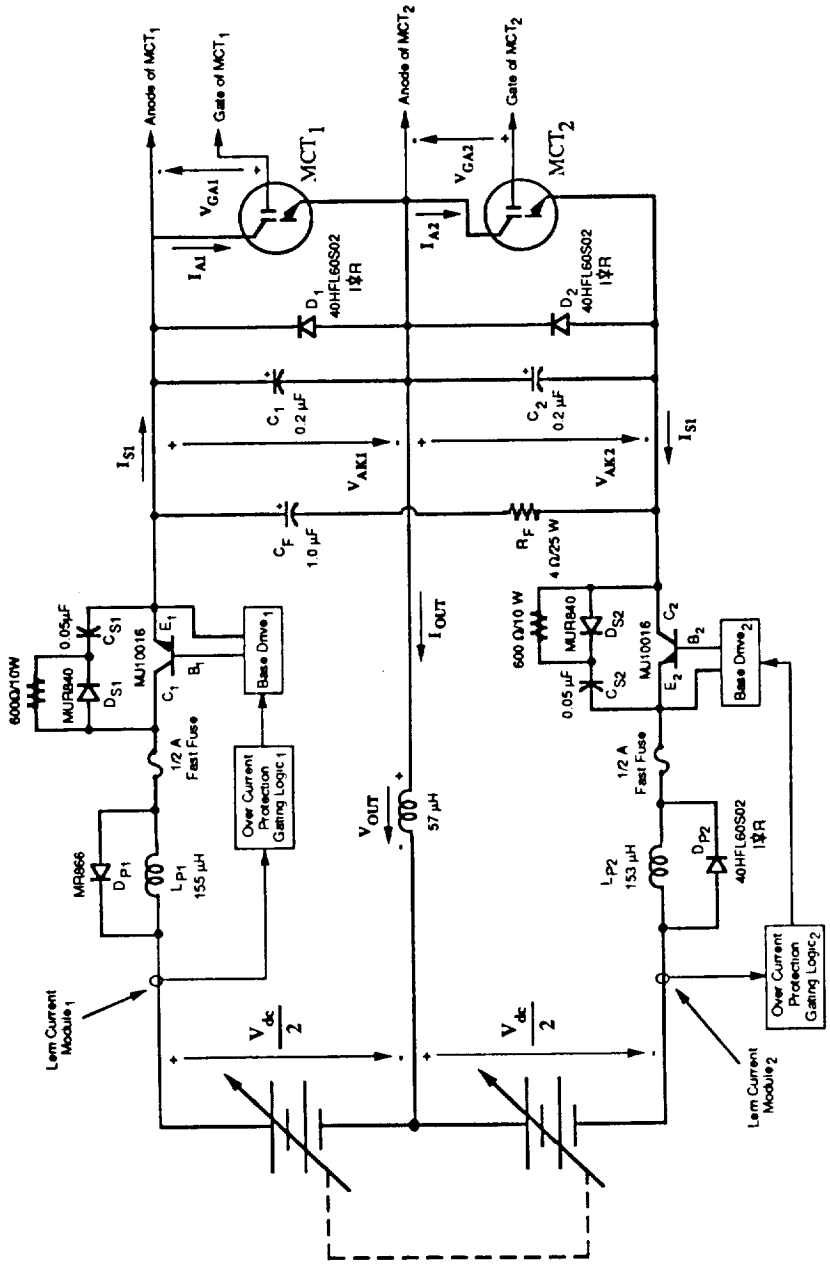


Fig. 2.47. Zero Voltage Switching Power Circuit Layout for the Second Generation MCTs Together with Improved Protection Circuit.

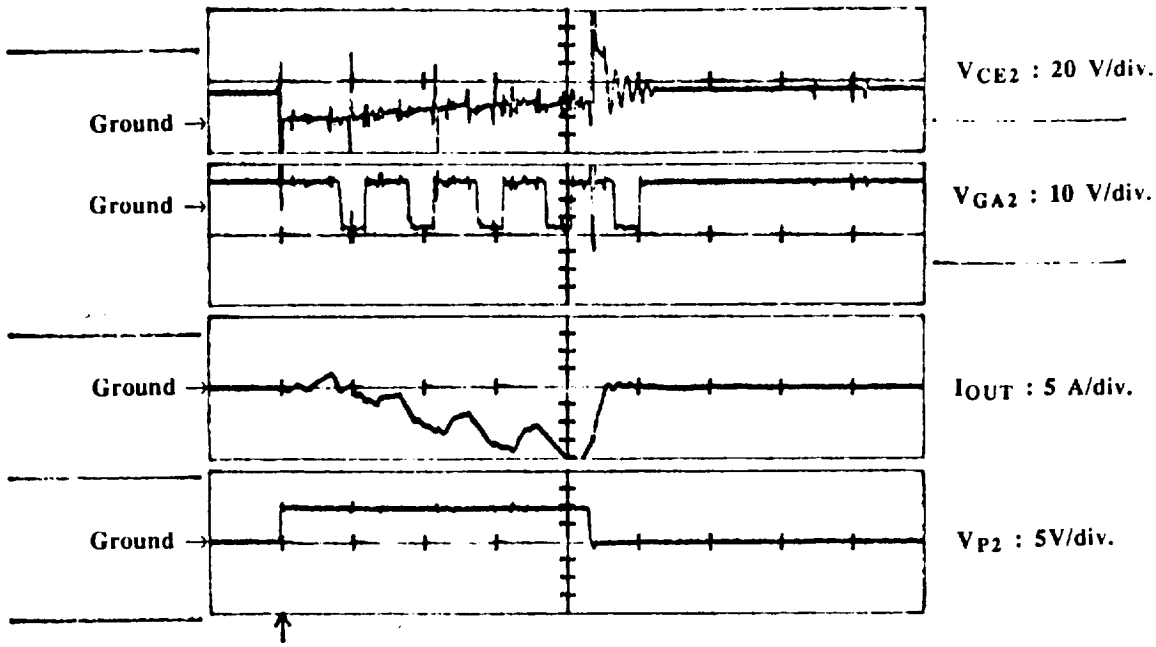


Fig. 2.48. Testing of Protection Circuit with the Failed MCT Device (18AU30A) Still in Place in the Circuit. From the Top Respectively: Lower Protection Transistor Collector to Emitter Voltage: $V_{CE2}$ : 20 V/div. Lower (Defected) MCT's Gate to Anode Voltage: $V_{GA2}$ : 10 V/div. Output (Inductor) Current: $I_{OUT}$ : 5 A/div. Protection Signal That Activates the Lower Protection Transistor: $V_{P2}$ : 5V/div. Time/div: 100 µsec.

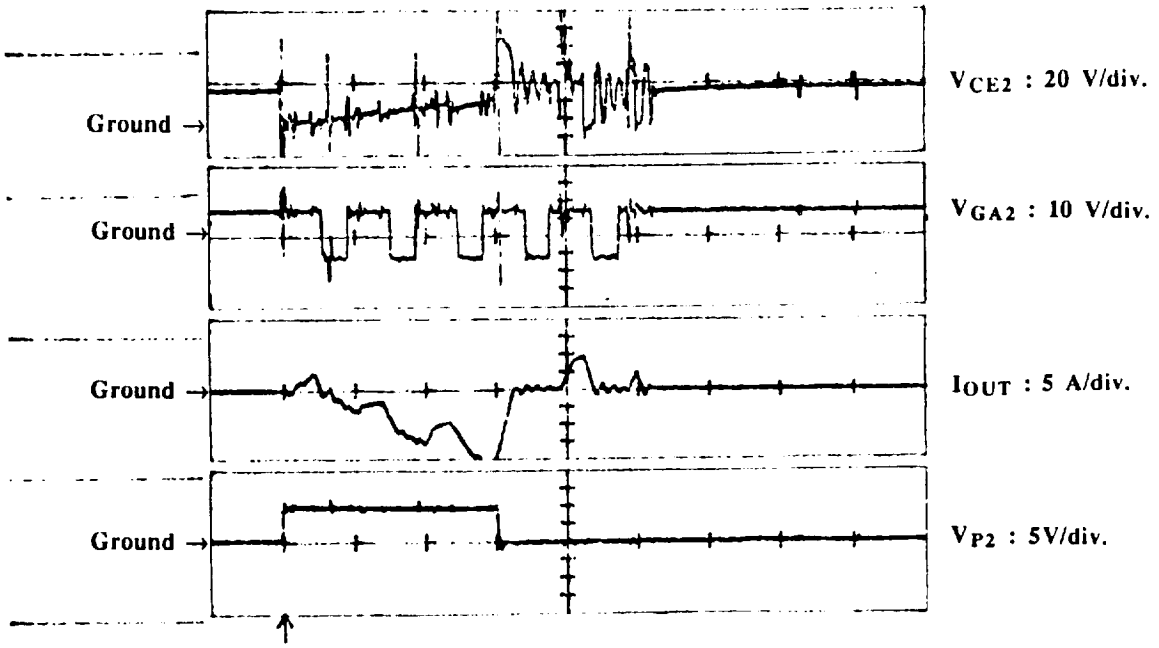


Fig. 2.49. Testing of Protection Circuit with Failed Device in Place Using a High Operating Voltage. From the Top Respectively: Lower Protection Transistor Collector to Emitter Voltage: $V_{CE2}$ : 20 V/div. Lower (Defected) MCT's Gate to Anode Voltage: $V_{GA2}$ : 10 V/div. Output (Inductor) Current: $I_{OUT}$ : 5 A/div. Protection Signal That Activates the Lower Protection Transistor: $V_{P2}$ : 5V/div. Time/div: 100 µsec.

Fig. 2.50 shows another problem, this time a turn-on failure problem of a newly replaced lower MCT. This device is numbered as 14AU28. After confirming that we have devices which does not show any failure, we have proceeded to determine the zero voltage switching characteristics of MCT.

At a 70 volt operating voltage the upper MCT requires 40 V. across its anode-cathode before it turns-on. Similarly the lower MCT requires 50 V. to turn-on. These requirements can be seen from Figs. 2.51 and 2.52 respectively. In these figures first droop in the device voltage is due to the turn-on requirement of the other MCT and the second droop is due to the voltage drop across the protection inductor. It is interesting to note that the turn-on requirement increases with increasing operating voltage. For example, in the records taken during the test, this requirement goes up to about 58 V. for the upper MCT and about 82 V. for the lower MCT at 130 V. operating voltage. The entire test was completed at a 152 V. operating voltage. The turn-on requirements for this operation is about 75 V. for the upper device and almost 105 V. for the lower MCT. Figures 2.53 and 2.54 are related to these requirements respectively. In these figures the upper and lower branch currents are again shown. Since it was not possible to go to higher operating voltages, wit is not known how much voltage will the MCTs require to turn-on at these high operating voltages.

In Fig. 2.55, the gate-anode voltage versus device voltage of lower MCT is given. It is apparent that the gate-anode voltage is quite affected due to induced voltages with the switching action of the MCTs. Fig. 2.56 shows the output voltage and the output current of the resonant circuit.

The next three figures represents tests for three additional new MCTs. Two of them at their first trial showed turn-off failure at a 76 V. operating voltage. Figure 2.57 and 2.58 show these turn-off failures which correspond to devices numbered 14AP30A and 14AP30C respectively. The last cut-off instants in the currents in these figures are due to the protection circuit operation. Figure 2.59 shows the turn-on characteristics to a device which did not fail numbered 18BP34 which requires least voltage to turn-on among the remaining MCTs with around 45 V. required at a 152 V. operating voltage.

Table. 2.2 is prepared to compare the turn-on voltage requirements of the different MCTs for the zero voltage switching scheme.

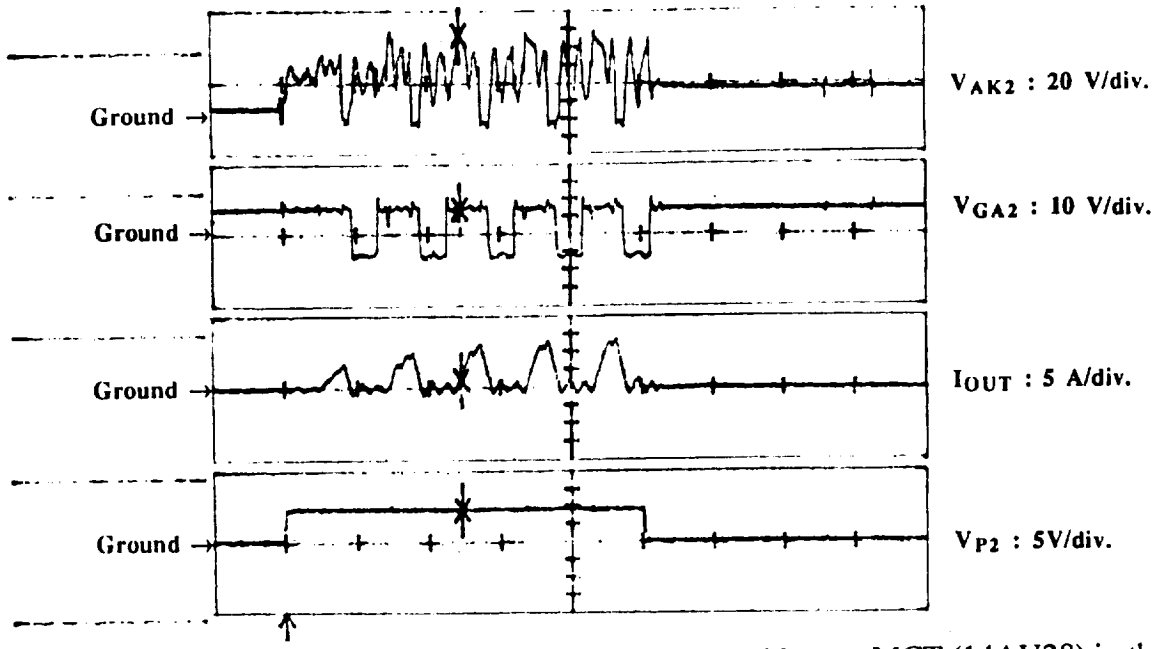


Fig. 2.50. Turn-on Failure Record of the Newly Replaced Lower MCT (14AU28) in the Circuit of 2.47. From the Top Respectively: Lower MCT Anode to Cathode Voltage: $V_{AK2}$ : 20 V/div. Lower MCT Gate to Anode Voltage: $V_{GA2}$ : 10 V/div. Output (Inductor) Current: $I_{OUT}$ : 5 A/div. Protection Signal That Activates the Lower Protection Transistor: $V_{P2}$ : 5V/div. Time/div: 100 µsec.

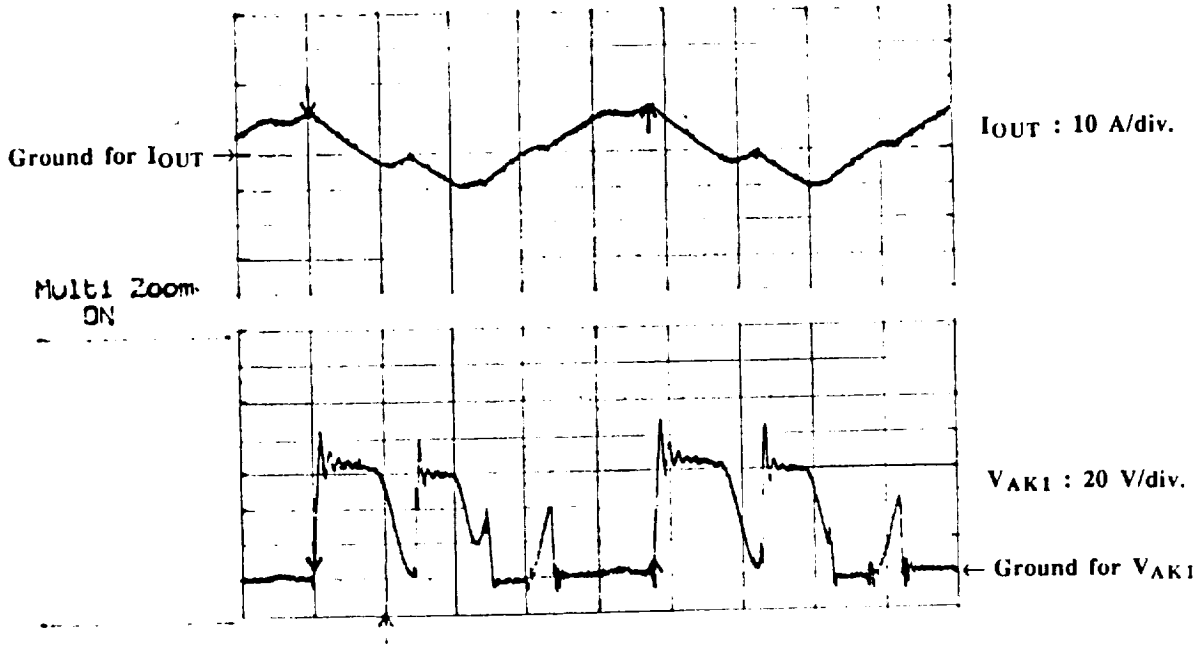


Fig. 2.51. Turn-on Voltage Requirement of Upper MCT (14AU34A) During Zero Voltage Switching for an Operating DC Voltage of 70 V. Top Trace: Output (Inductor) Current: $I_{OUT}$ : 10 A/div. Bottom Trace: Upper MCT Anode to Cathode Voltage: $V_{AK1}$ : 20 V/div. Time/div: 20 µsec.


Fig. 2.52. Turn-on Voltage Requirement of Lower MCT (14AU30B) During Zero Voltage Switching. The Operating DC Voltage is 70 V. Top Trace: Output (Inductor) Current: $I_{OUT}$ : 10 A/div. Bottom Trace: Lower MCT Anode to Cathode Voltage: $V_{AK2}$ : 20 V/div. Time/div: 20 µsec.

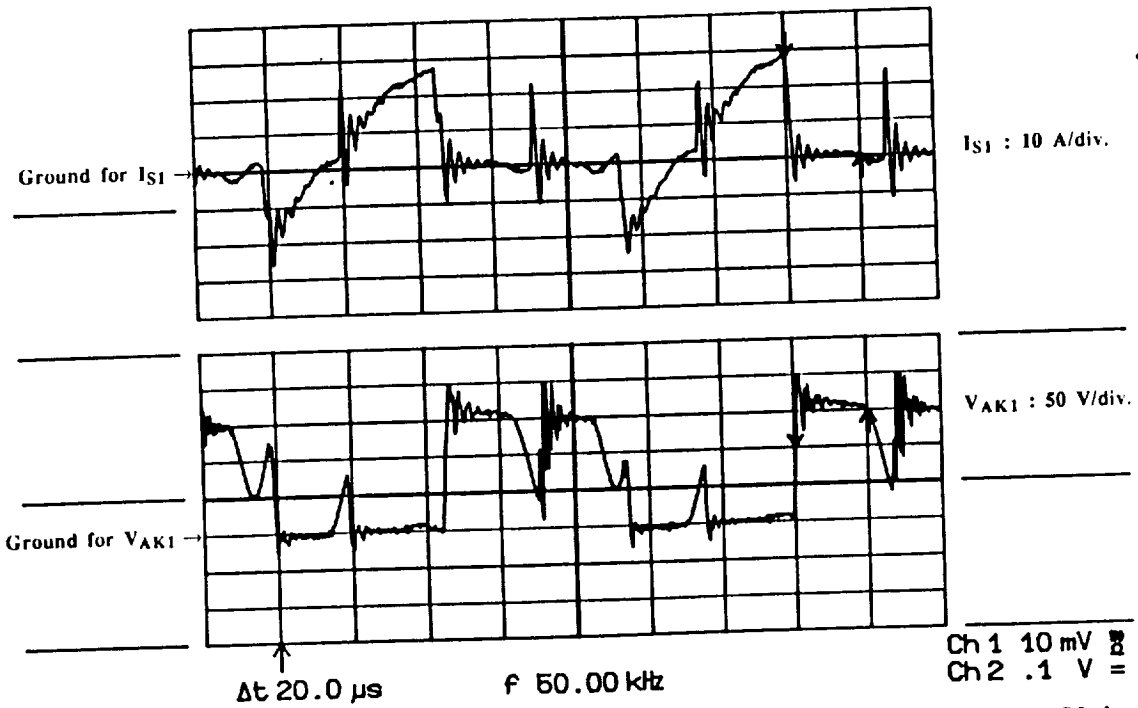


Fig. 2.53. Showing Upper Device Voltage and Switched Current During Zero Voltage Switching Indicating the Turn-on Voltage Requirement of the Upper MCT (14AU34A) for an Operating DC Voltage of 152 V. Top Trace: Upper Branch Switched Current: $I_{S1}$ : 10 A/div. Bottom Trace: Upper MCT Anode to Cathode Voltage: $V_{AK1}$ : 50 V/div. Time/div: 20 µsec.

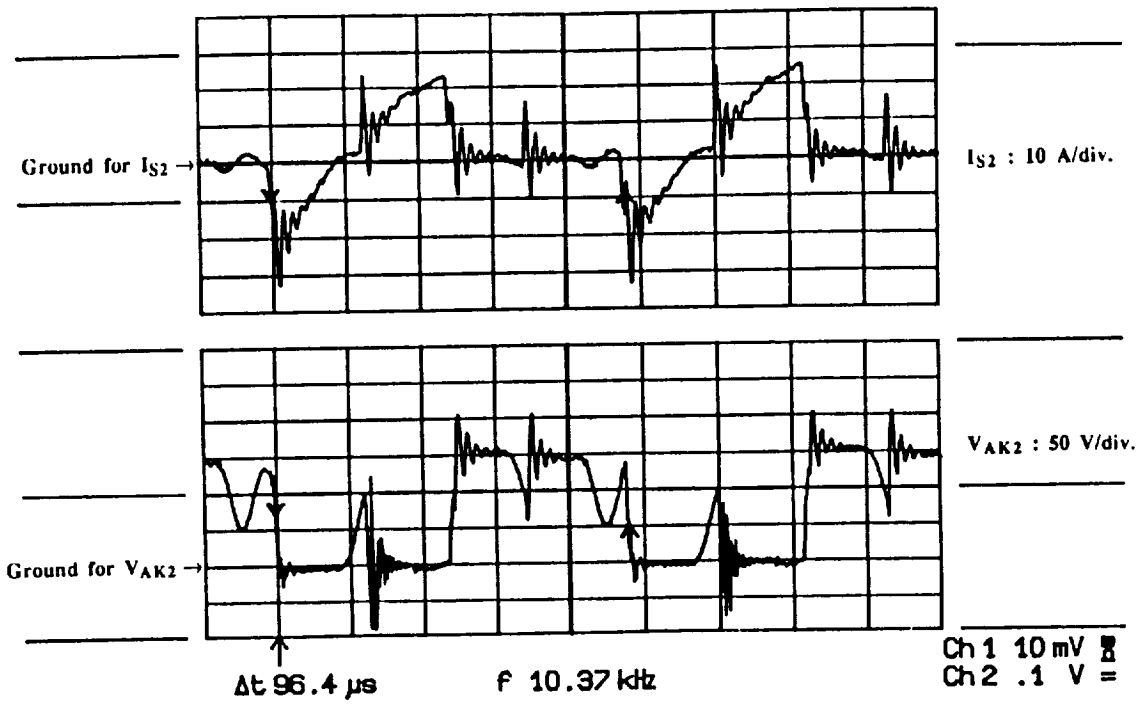


Fig. 2.54. Showing Lower Device Voltage and Current During Zero Voltage Switching Indicating the Turn-on Voltage Requirement of the Lower MCT (14AU30B) for an Operating DC Voltage of 152 V. Top Trace: Lower Branch Switched Current: $I_{S2}$ : 10 A/div. Bottom Trace: Lower MCT Anode to Cathode Voltage: $V_{AK2}$ : 50 V/div. Time/div: 20 μsec.

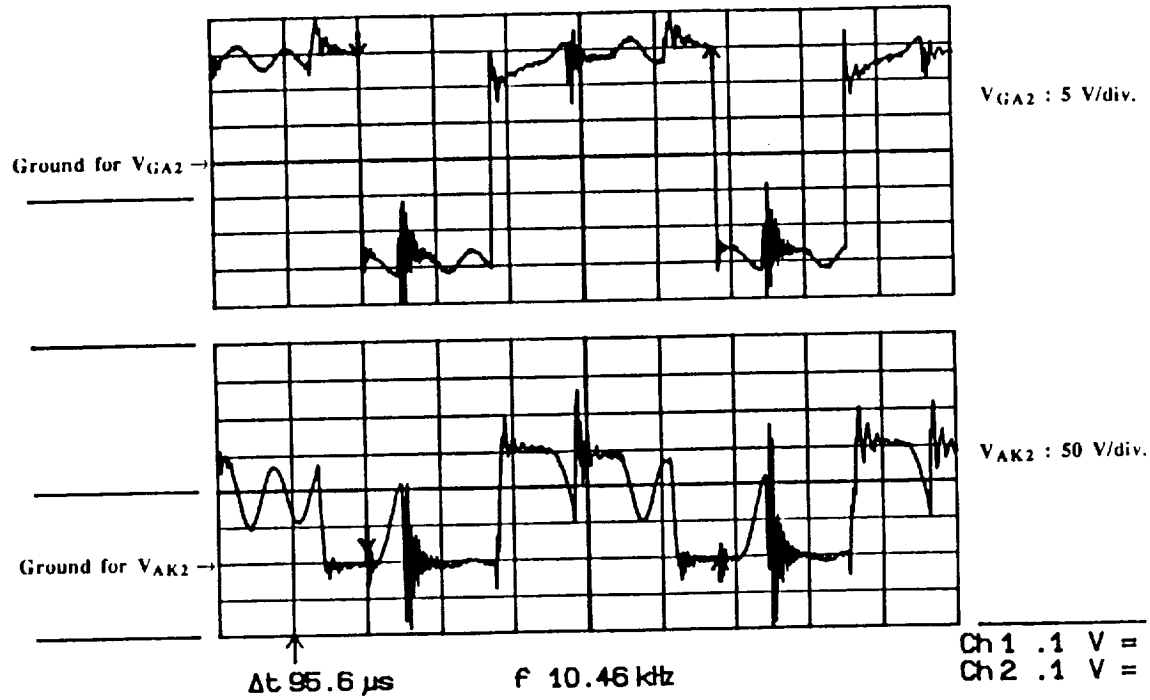


Fig. 2.55. Illustrating Overall Behavior of Device Gate to Anode and Anode to Cathode Voltage During Zero Voltage Switching. Top Trace: Lower MCT Gate to Anode Voltage: $V_{GA2}$ : 5 V/div. Bottom Trace: Lower MCT Anode to Cathode Voltage: $V_{AK2}$ : 50 V/div. Time/div: 20 μsec.

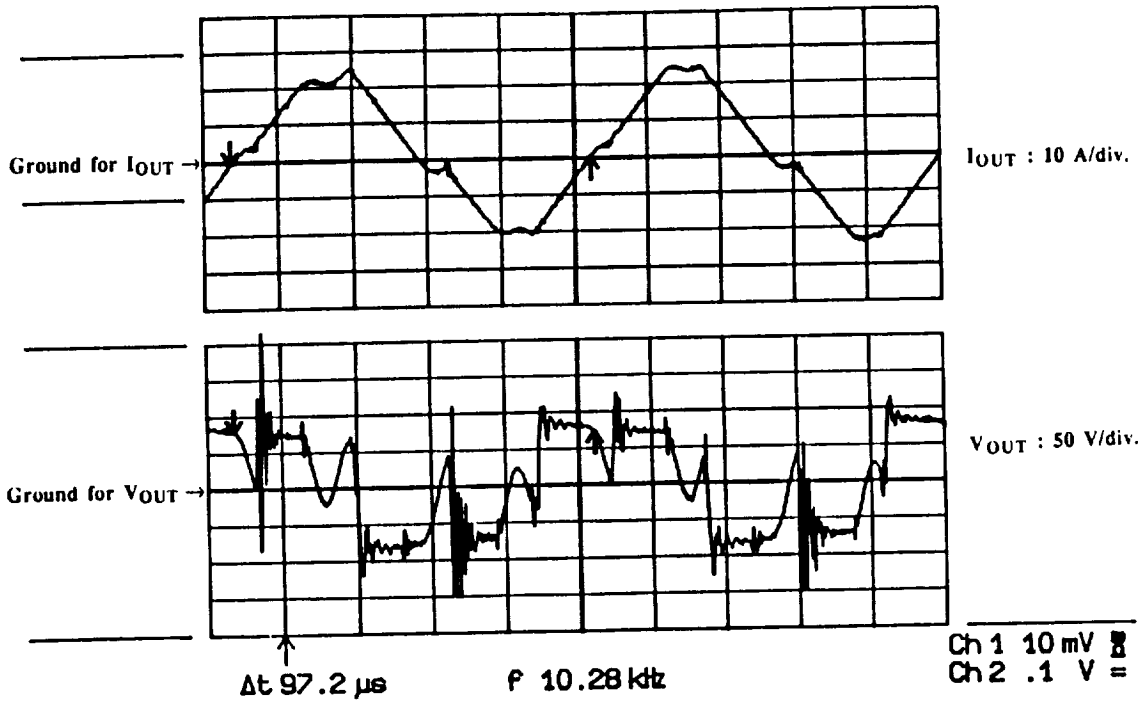


Fig. 2.56. Illustrating Overall Behavior of Output Voltage and Current Waveforms in Soft Zero Voltage Switching Circuit. Top Trace: Output (Inductor) Current: $I_{OUT}$ : 10 A/div. Bottom Trace: Output (Inductor) Voltage: $V_{OUT}$ : 50 V/div. Time/div: 20 μsec.

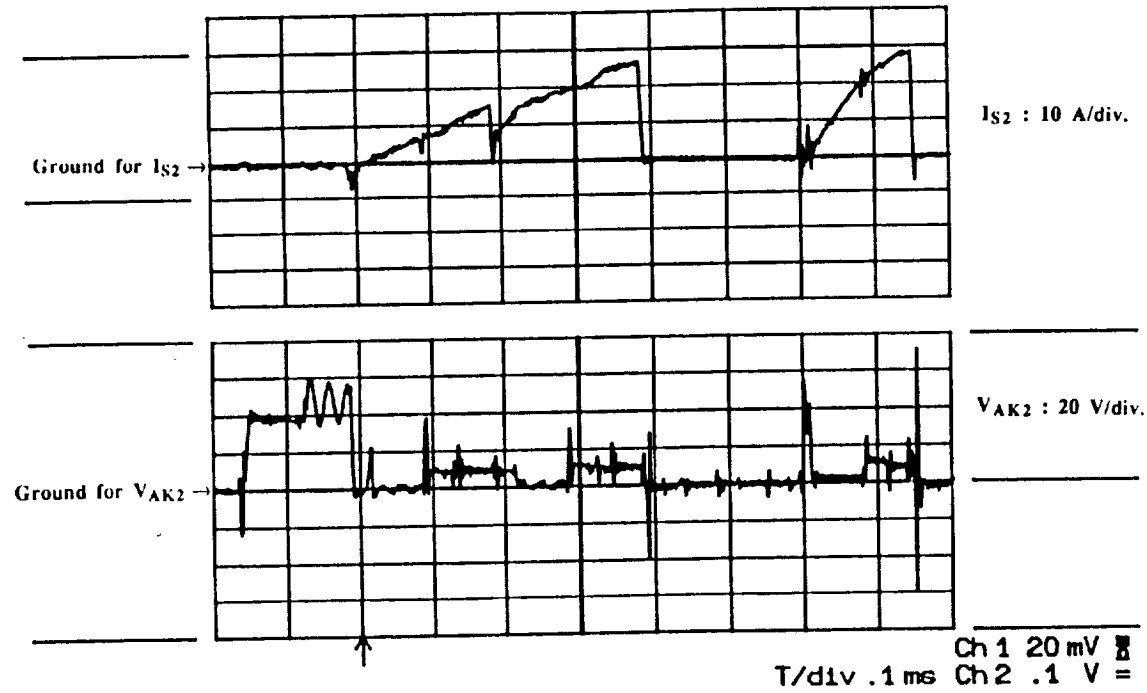


Fig. 2.57. Test of MCT 14AP30A in Lower Branch of Circuit Documenting Turn-off Failure of Device with Protection Circuit of Fig. 2.47 in Operation. Top Trace: Lower Branch Switched Current: $I_{S2}$ : 10 A/div. Bottom Trace: Lower MCT Anode to Cathode Voltage: $V_{AK2}$ : 20 V/div. Time/div: 100 μsec.

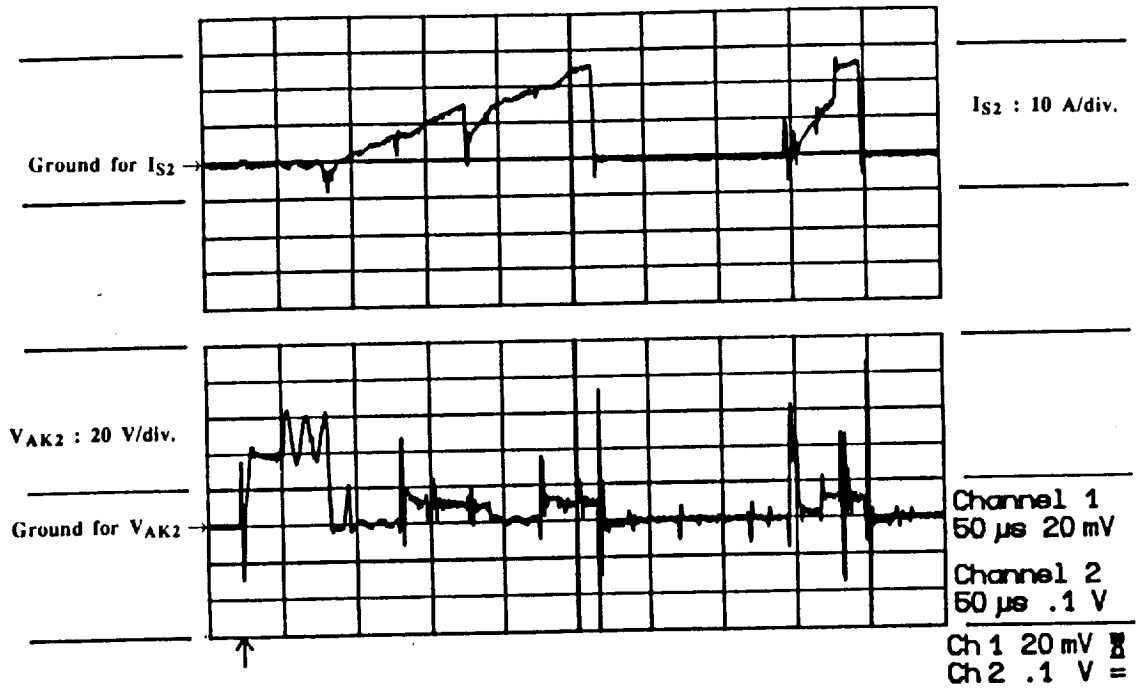


Fig. 2.58. Test of MCT 14AP30C in Lower Branch of Circuit Documenting Turn-off Failure of Device with Protection Circuit of Fig. 2.47 in Operation. Top Trace: Lower Branch Switched Current: $I_{S2}$ : 10 A/div. Bottom Trace: Lower MCT Anode to Cathode Voltage: $V_{AK2}$ : 20 V/div. Time/div: 100 µsec.

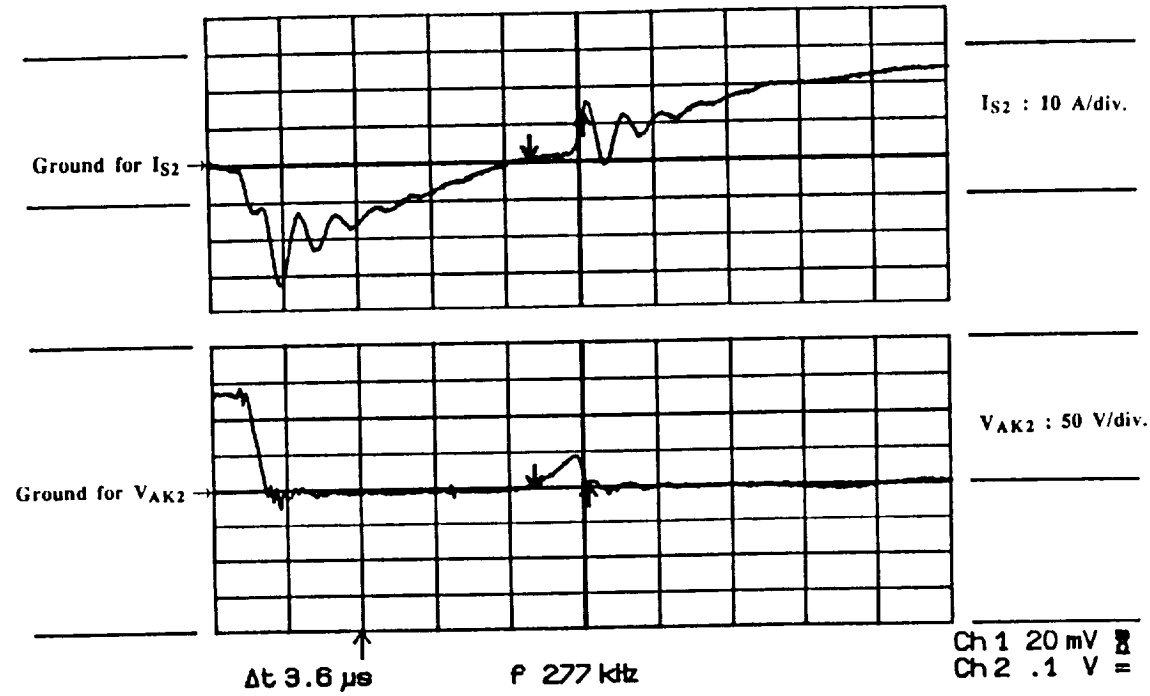


Fig. 2.59. Test of MCT 18BP34 in Lower Branch of Circuit Showing Performance of the Best Device for the Same Operating Conditions as Figs. 2.57 and 2.58. Top Trace: Lower Branch Switched Current: $I_{S2}$ : 10 A/div. Bottom Trace: Lower MCT Anode to Cathode Voltage: $V_{AK2}$ : 50 V/div. Time/div: 5 µsec.

| | | Operating Voltage | Turn on Voltage Requirement at Zero Voltage Switching |
|---|---|---|---|
| **First Generation MCT** | | 150 V | 90 V |
| **Second Generation MCTs** | **14AU34A** | 70 V | 40 V |
| | | 130 V | 58 V |
| | | 152 V | 75 V |
| | **14AU30B** | 70 V | 50 V |
| | | 130 V | 82 V |
| | | 152 V | 105 V |
| | **18BP34** | 152 V | 45 V |

Table 2.2. Comparison of Turn-on Voltage Requirements for Zero Voltage Switching.

### 2.2.4 Zero Current Switching Characteristics of Second Generation MCT

The zero current switching characteristics of MCTs were investigated with the circuit given in Fig. 2.60. This circuit appears to be very complicated because the same protection circuit was used as in the zero voltage switching test. Since, in a practical circuit, exact zero current switching is difficult to accomplish, the switching performance when the current switching instant is off by certain percentage was also investigated.

The operating or clock frequency was chosen to be 10 kHz and governed by an astable multivibrator. The resonant circuit parameters were chosen accordingly. The operating voltage level was 150 V. Since the tests were carried out for approximately 10 cycles, no extra gating logic was arranged to switch at the exact zero current. Therefore, the clock and resonant frequencies were observed together so as to match the signals by adjusting the clock frequency. Hence, at each step of changing the clock frequency, the turn-on signals for complementary operating MCTs had to be readjusted to make sure that the MCTs never receive turn-on signals at the same time and establish a shoot through.

Figure 2.61 shows an overview of total cycles of operating in this mode. It is worthwhile to mention here that the glitches in the gate anode voltage waveform of the lower MCT, the second figure from the top, are due to the voltage isolator that was used in the lab. It can be noticed that there is almost no glitch at the other gate anode voltage waveform because a different channel of the voltage isolator was used. This other channel of isolator was used to measure the gate anode voltage containing frequent glitches and the situation was verified to be due to the voltage isolator. The large droop in the device anode-cathode voltage during the off period is because of the protection inductor voltage drop.

Figure 2.62 shows the resonant circuit inductor current and lower MCT anode cathode voltage. This figure clearly shows the zero current switching of the device even though it is not switching as an exact zero instant. Figure 2.63 shows the corresponding gating signal and device voltage. From this figure one can determine that the device voltage stays at zero for about 4 μsec after a turn-off command is given. This result is due to the conduction of the anti-parallel diode connected to the same device. The conduction of this diode continues until the complementary MCT is turned-on and the current is diverted to that MCT. Figure 2.64 shows this behavior more clearly since the lower device voltage and lower branch current are pictured together. A magnified view of this figure around the turn-off instant of the device is given in Fig. 2.65. While the negative current is carried by the anti-parallel diode, the device voltage remains at zero even though the turn-off

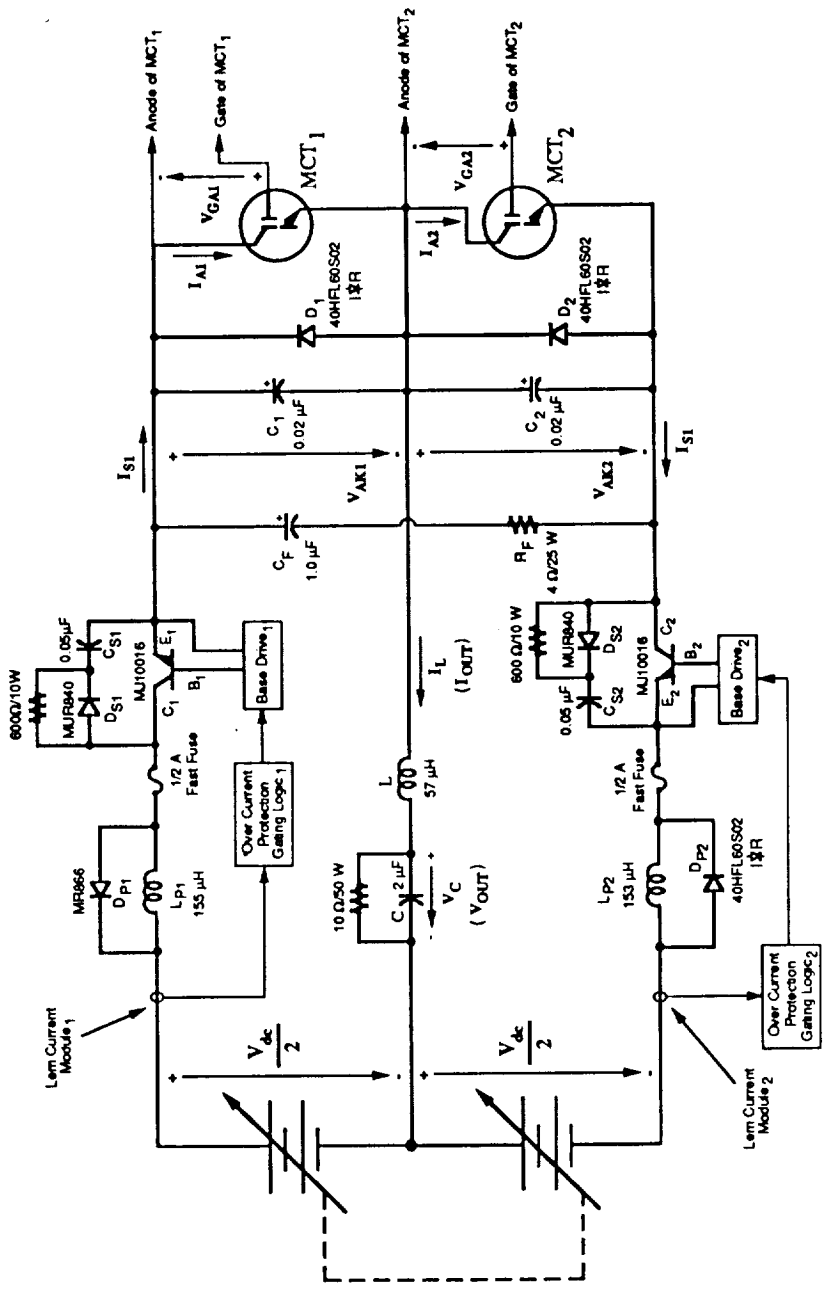


Fig. 2.60 Zero Current Switching Circuit Layout for the Second Generation MCTs Including Improved Protection Circuit.

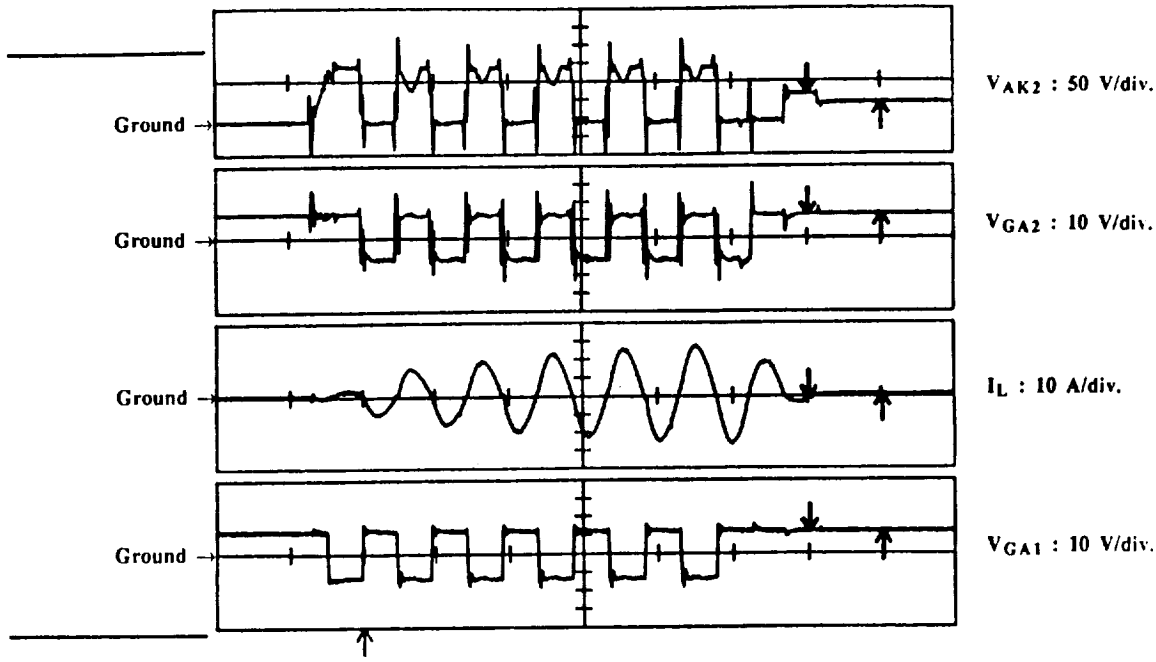


Fig. 2.61. Overall Behavior of Device Operation During Zero Current Switching Operation. From the Top Respectively: Lower MCT Anode to Cathode Voltage: $V_{AK2}$ : 50 V/div. Lower MCT Gate to Anode Voltage: $V_{GA2}$ : 10 V/div. Resonant Inductor (Output) Current: $I_L$ : 10 A/div. Upper MCT Gate to Anode Voltage: $V_{GA1}$ : 10 V/div. Time/div: 100 µsec.

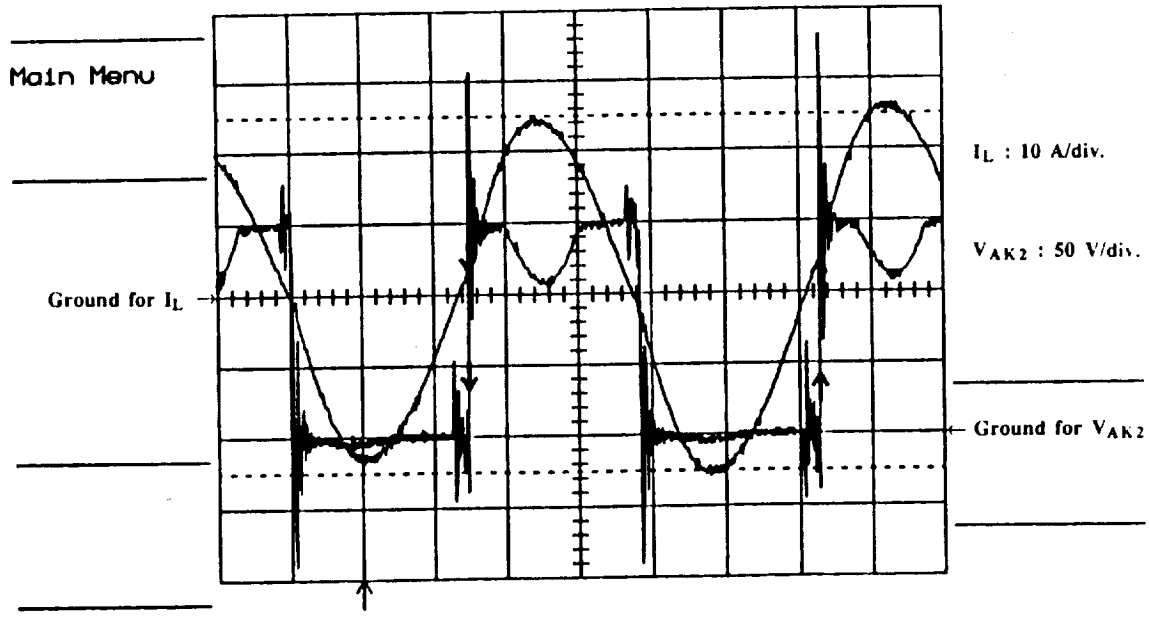


Fig. 2.62. Resonant Circuit Inductor (Output) Current and Lower Device Anode to Cathode Voltage During Zero Current Switching with Second Generation Device. Sinusoidal Waveform: Resonant Inductor (Output) Current: $I_L$ : 10 A/div. The other Waveform: Lower MCT Anode to Cathode Voltage: $V_{AK2}$ : 50 V/div. Time/div: 20 µsec.

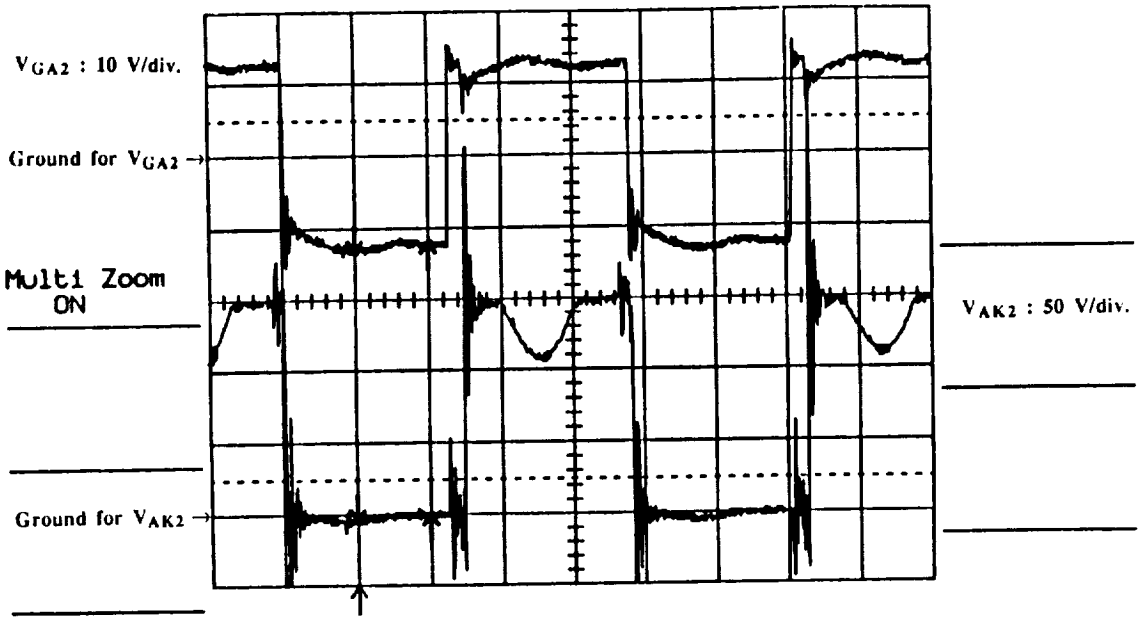


Fig. 2.63. Lower Device Gate to Anode and Anode to Cathode Voltage During Zero Current Switching with Second Generation Device. Top Trace: Lower MCT Gate to Anode Voltage: $V_{GA2}$ : 10 V/div. Bottom Trace: Lower MCT Anode to Cathode Voltage: $V_{AK2}$ : 50 V/div. Time/div: 20 μsec.

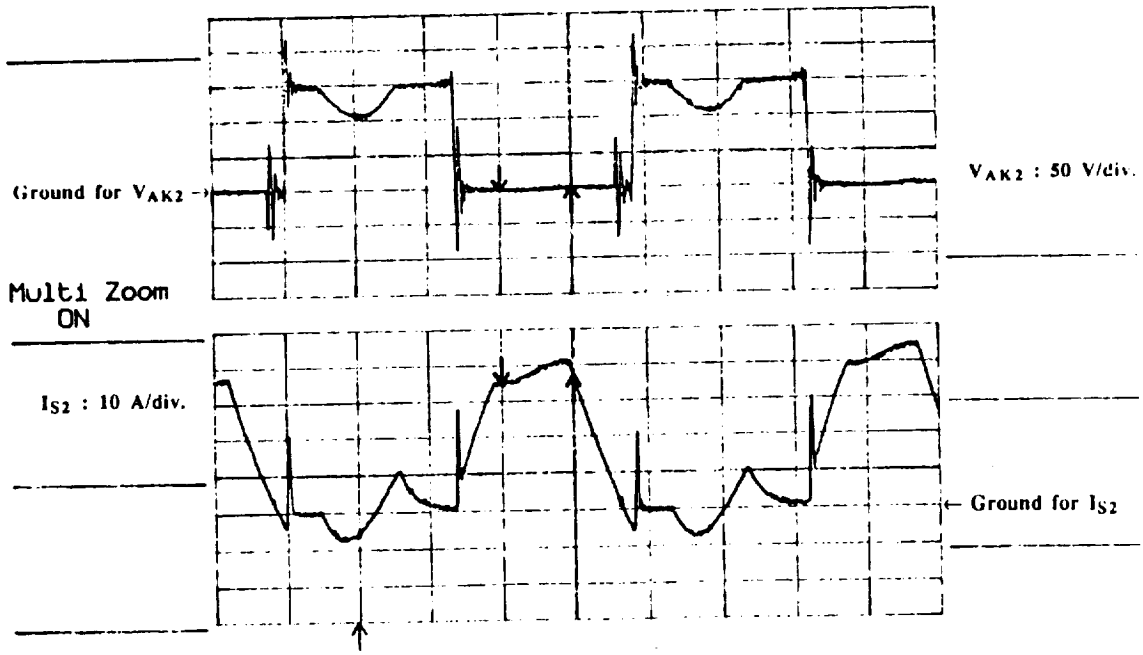


Fig. 2.64. Lower Device Anode to Cathode Voltage and Switched Current in Zero Current Switching. Top Trace: Lower MCT Anode to Cathode Voltage: $V_{AK2}$ : 50 V/div. Bottom Trace: Lower Branch Switched Current: $I_{S2}$ : 10 A/div. Time/div: 20 μsec.

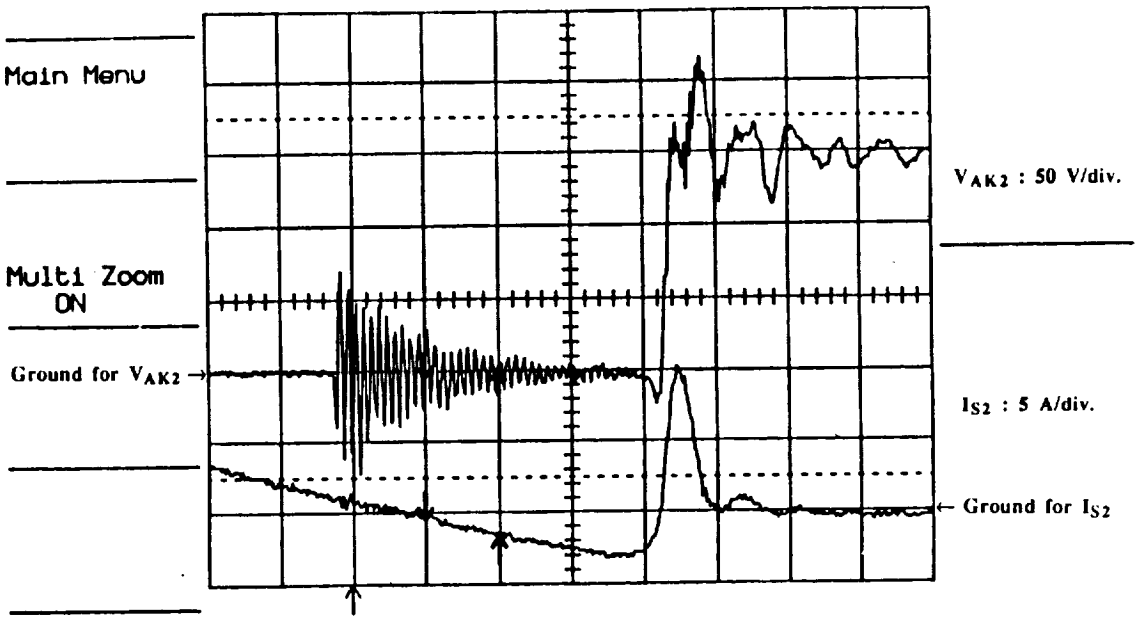


Fig. 2.65. Magnified View of Turn-off of Second Generation MCT in Zero Current Switching. Long Delay in Turn-off of the Lower Device is Due to the Turn-on Delay of the Upper Device on the Circuit. Top Trace: Lower MCT Anode to Cathode Voltage: $V_{AK2}$ : 50 V/div. Bottom Trace: Lower Branch Switched Current: $I_{S2}$ : 5 A/div. Time/div: 1 μsec.

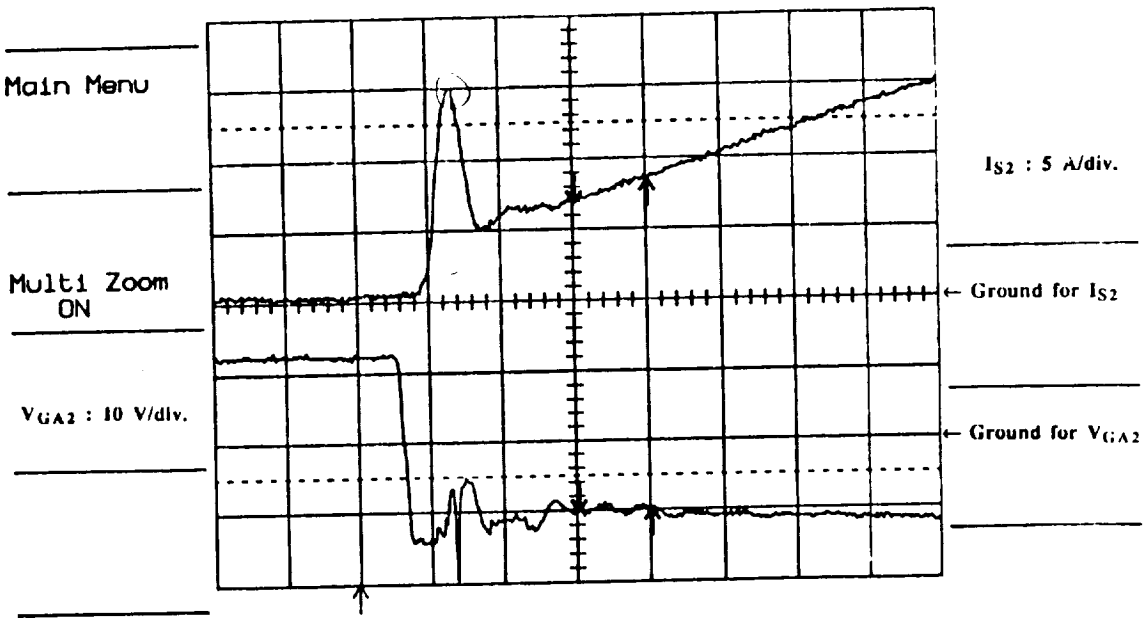


Fig. 2.66. Magnified View of Turn-on of Second Generation MCT in Zero Current Switching. Top Trace: Lower Branch Switched Current: $I_{S2}$ : 5 A/div. Bottom Trace: Lower MCT Gate to Anode Voltage: $V_{GA2}$ : 10 V/div. Time/div: 1 μsec.

command is given. The spike in the current when the other MCT is turned-on is due to the reverse recovery of lower branch diode.

Turn-on of the MCT is given in Figs. 2.66 and 2.67. The current spike just after the turn-on is again due to the reverse recovery of the diode connected to the complementary device. The inductor current and the output voltage of the resonant circuit is shown in Fig. 2.68. The output voltage versus device voltage is given in Fig. 2.69.

### 2.2.5 Non Zero Current Switching for Zero Current Switching Scheme

In order to determine the switching characteristics of the second generation MCT when zero current switching is 10% from the exact zero current switching, two tests were carried out at frequencies above and below the resonant frequency. The resonant frequency for this portion of the test was about 10 kHz. Operating above resonance at 11 kHz switching frequency again draws attention to the turn-on voltage requirement problem of the MCT. Figure 2.70 shows a good example of this type of problem. Let it should be remembered that to turn the MCT on it is necessary to apply a negative gate anode voltage. As can seen from the figure, when the turn-on gate pulse is applied, the voltage across the device is already zero because of the conducting anti-parallel diode. When the current changes its direction, normally the MCT should take over the current since it is already commanded on. However, since the MCT requires a certain amount of voltage before it turns-on, it takes time for the device to turn-on. Hence, problems with high device losses could be encountered in current resonant link converters is the zero current instant is not accurately determined.

For operating frequencies below the resonant frequency, no problems were experienced. Figure 2.71 shows this type of operation at approximately 9.7 kHz operating frequency.

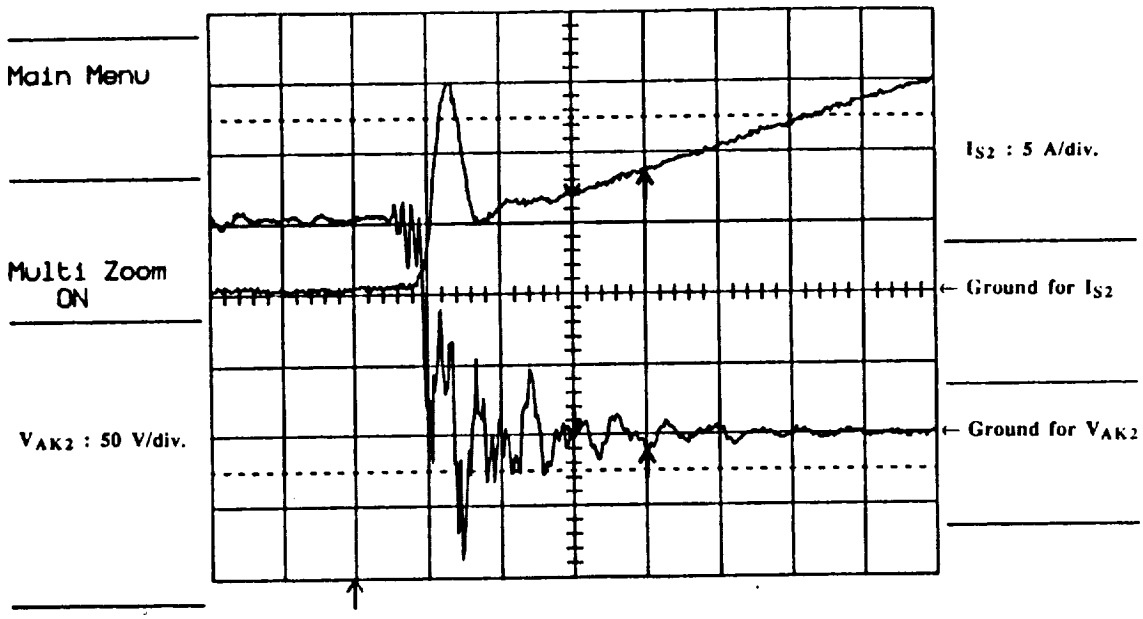


Fig. 2.67. Another Picture Showing Magnified View of Turn-on of Second Generation MCT in Zero Current Switching. Top Trace: Lower Branch Switched Current: $I_{S2}$ : 5 A/div. Bottom Trace: Lower MCT Anode to Cathode Voltage: $V_{AK2}$ : 50 V/div. Time/div: 1 μsec.

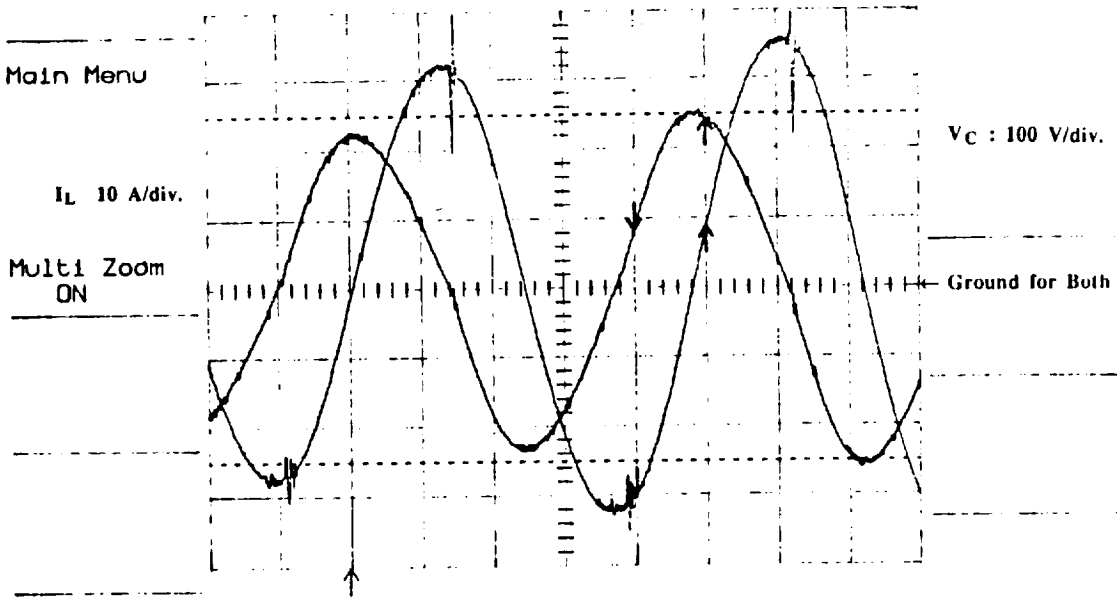


Fig. 2.68. Output Voltage and Current Waveforms for Zero Current Switching Circuit Shown in Fig. 2.60 where the Second Generation MCTs are Utilized. Higher Amplitude Waveform: Resonant Capacitor (Output) Voltage: $V_C$ : 100 V/div. Lower Amplitude Waveform: Resonant Inductor (Output) Current: $I_L$ : 10 A/div. Time/div: 20 μsec.

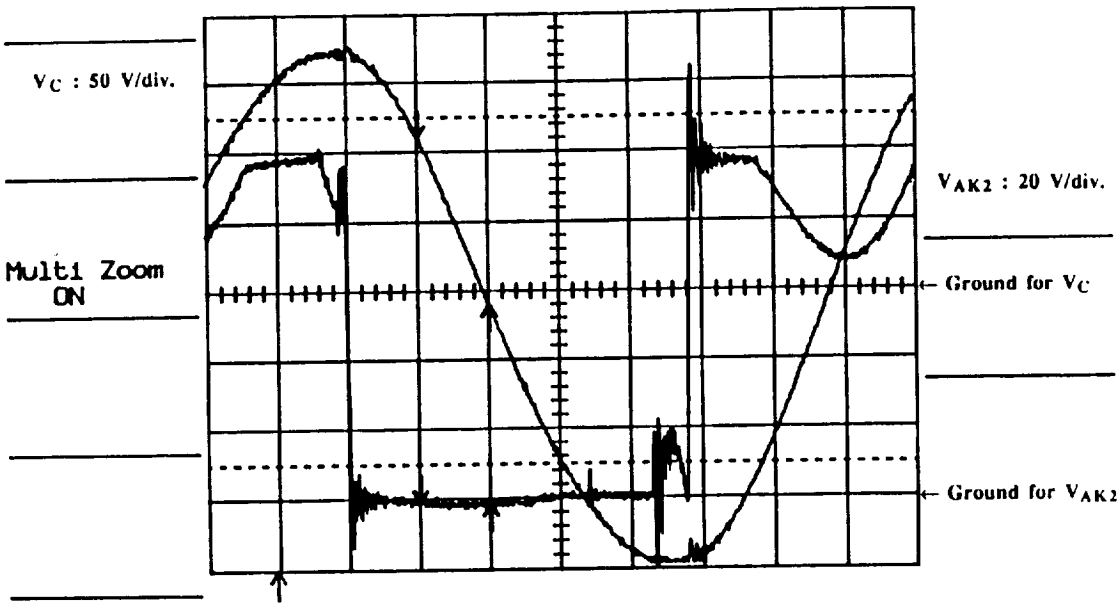


Fig. 2.69. Showing the Lower MCT Device Voltage Versus Output Voltage for Zero Current Switching Circuit. Sinusoidal Waveform: Resonant Capacitor (Output) Voltage: $V_C$ : 50 V/div. The Other Waveform: Lower MCT Anode to Cathode Voltage: $V_{AK2}$ : 20 V/div. Time/div: 10 µsec.

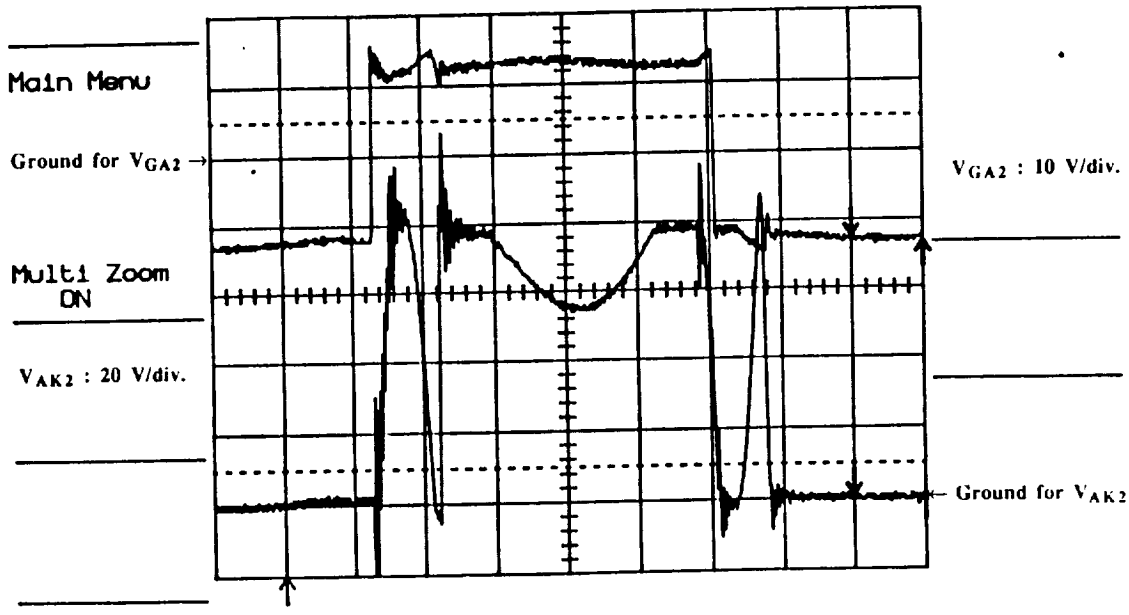


Fig. 2.70. Non-Zero Current Switching for a Switching Frequency of Approximately 10% Greater than the Resonant Frequency Required for True Zero Current Switching. Top Trace: Lower MCT Gate to Anode Voltage: $V_{GA2}$ : 10 V/div. Bottom Trace: Lower MCT Anode to Cathode Voltage: $V_{AK2}$ : 20 V/div. Time/div: 10 µsec.

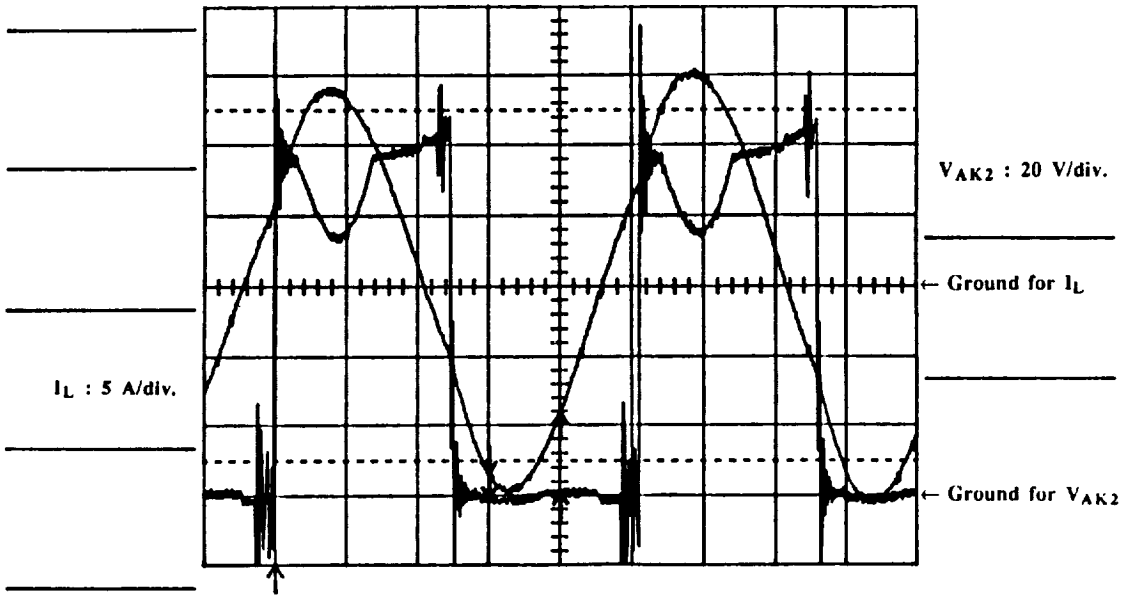


Fig. 2.71. Non-Zero Current Switching for a Switching Frequency of Approximately 5% Less than the Resonant Frequency Required for True Zero Current Switching. Sinusoidal Trace: Resonant Inductor (Output) Current: $I_L$ : 5 A/div. The Other Trace: Lower MCT Anode to Cathode Voltage: $V_{AK2}$ : 20 V/div. Time/div: 20 μsec.

## 2.3. References


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# Chapter 3

# PDM Converter and Component Considerations

In this chapter the operation principles of a Pulse Density Modulated Converter (PDMC) for three phase (3Ø) to three phase two-step power conversion via parallel resonant High Frequency (HF) AC link is reviewed. Since the power rating of the previous system has been upgraded and increased in rating, details for the selection of the power switches and other power components required for the new power circuit encompassing a complete 3Ø to 3Ø power converter system is discussed throughout Sections 3.2 to 3.4. Problems encountered in the previous low power system, in the selection of the new power components, and in the new system are presented in the same sections. The solutions and suggestions to these problems for the new system are also discussed.

## 3.1. Review of Operating Principles

In this Section the operating principle of a Direct ON-OFF current regulated single phase PDMC operating from a DC source via parallel resonant HF AC Link is reviewed to ease the understanding of operating principle for a 3Ø-PDMC. Later, the principle of operation of a Direct ON-OFF current regulated 3Ø-PDMC operating from a 3Ø source/load via parallel resonant HF AC Link is reviewed.

### 3.1.1 Review of Principles of Operation of a Single Phase Full Bridge PDM Converter

It is possible to view the Single Phase PDMC Bridge Operation operating from a Parallel Resonant HF AC Link from two different perspectives. In the first perspective, a voltage synthesization technique is utilized where the DC or single phase low frequency AC voltages are synthesized from an existing Parallel Resonant HF AC Link. The current at the DC or low frequency side is a dependent variable and determined by the load and synthesized voltage. With this technique, a given reference voltage is synthesized with either half cycles of the HF Link voltage or the zero voltage state by the switching action of the PDMC. This perspective is quite extensively covered in references [1,2,3]. The maximum level of the DC or the peak of the low frequency AC voltage that can be synthesized using a full bridge power circuit is given, on the average as

$$V_{dc}^{max} = V_{LF\ AC}^{max\ peak} = \frac{2V_{HF}}{\pi} \qquad 3.1.1$$

The second perspective utilizes a current regulation technique whereby the DC or single phase low frequency AC current is regulated by means of the switching action of the single phase PDMC and interaction occurs between the Parallel Resonant HF AC Link and the DC or low frequency AC through a line side filter inductor. In this technique, the synthesized DC or low frequency AC voltage is a dependent variable and determined by the switching action of the single phase PDMC. The line filter inductor shown in Fig. 3.1 determines the size of the ripple current imposed on the DC or low frequency AC current and allows energy to be stored and dumped when required. This perspective is partly covered in references [1,2] and extensively in [4,5].

It is important to mention that the switches used in the Single Phase PDMC Bridge should have bidirectional voltage blocking capability since the HF Link is a Parallel Resonant AC Link. Similarly, they should have bidirectional current carrying capability both for bidirectional power flow through a DC supply and for synthesizing low frequency AC signals.

### 3.1.2 Operating Principle of Single Phase Full Bridge PDM Converter

In this case it is useful to consider the second technique whereby current regulation is utilized to establish and maintain the Parallel Resonant HF AC Link from a DC voltage supply. As simulated in the computer and shown experimentally in the references mentioned above, power flow control and maintenance of the HF Link can be managed mainly by controlling the line filter inductor current at the DC side. As shown in Fig. 3.1, the gating logic of the switches in the Single Phase PDMC Bridge are determined by measured and reference currents.

The reference current is basically generated according to the required power of the load, the operational losses of the Source Side and the Load Side PDMC and the HF Link. If the source does not supply sufficient power when required by the load and the losses, the HF Link peak voltage tends to decrease. At this time, the appropriate switches which dump more energy from the source to the link should be selected for the next half cycle of the HF link. This case requires an increase in the reference current and in the dumped energy from source to link. The appropriate switches which do this job as quickly as possible are the ones that enable the HF Link voltage to support the positive DC side line inductor current. The choice of the switches is subject to change depending on the polarity

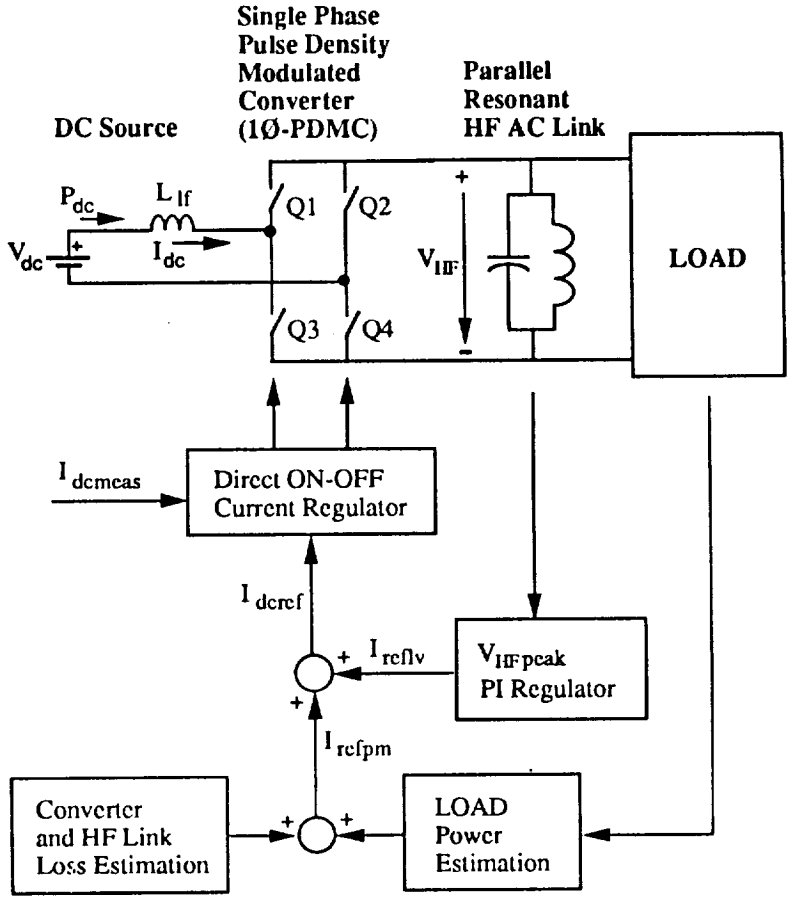



Fig. 3.1. Block Diagram of Direct ON-OFF Current Regulated Single Phase PDMC Operating from a DC Source and Parallel Resonant HF AC Link.

of the HF Link voltage. If the polarity of the link voltage is positive, switches Q2 and Q3 are appropriate, and if negative, Q1 and Q4. Similarly, when excessive power is dumped to the HF Link, the HF Link peak voltage increases. This case requires a decrease both in the reference current and in the energy dumped from the source to the link. Therefore, as opposed to the previous case, in this case the appropriate switches are the ones that enable the HF Link voltage to impede the positive DC side line inductor current. That is to say, if the polarity of the link voltage is positive the switches Q1 and Q4 are selected, if negative Q2 and Q3.

In the preceding two paragraphs, a power flow from the source side to the load side is assumed. This type of power flow direction can be referred to as a positive power flow. The two cases above can then be summarized as follows:

1. $I_{ref}$ is positive and $|I_{measured}| < |I_{ref}|$ :Supporting polarity of $V_{HF}$ is selected (-)
2. $I_{ref}$ is positive and $|I_{measured}| > |I_{ref}|$ : Impeding polarity of $V_{HF}$ is selected (+)

The first case corresponds to a reduction, and the second case to an increase in the peak link voltage for positive power flow operation.

When the negative power flow is assumed, the load side is in a position to deliver power to the HF Link and the source side to absorb excess power. The HF Link peak voltage increases when more power is delivered than the DC supply is already absorbing. This case requires the selection of the HF link voltage polarity that supports the negative DC side line inductor current. In this way, more power is absorbed in the next half cycle of the link by the DC supply. This means that Q1 and Q4 should be chosen for positive and Q2 and Q3 for negative polarity of the link voltage.

Similarly, the HF Link peak voltage decreases when less power is delivered than the DC supply is already absorbing. In this case selection of the HF link voltage polarity that impedes negative DC side line inductor current is necessary. In this manner, less power is absorbed in the next half cycle of the link by the DC supply. This means that one should choose Q2 and Q3 for positive and Q1 and Q4 for negative polarity of the link voltage.

The two cases in these preceding two paragraphs can be summarized as follows:

3. $I_{ref}$ is negative and $|I_{measured}| < |I_{ref}|$: Supporting polarity of $V_{HF}$ is selected (+)
4. $I_{ref}$ is negative and $|I_{measured}| > |I_{ref}|$: Impeding polarity of $V_{HF}$ is selected (-)

The first case corresponds to an increase, and the second case to a decrease in the peak link voltage for negative power flow operation.

The size of the DC voltage supply, peak value of the HF Link voltage, size of the line inductor and the switching pattern determine the size of the ripple current imposed on the DC line current. The size of the ripple current can be reduced at the expense of slower system response to the rapidly varying peak link voltage.

The technique explained above is known as "Direct ON-OFF, sigma modulator or Bang-Bang Controller." In this controller there is no integration involved in the regulation of the DC current. Figure 3.2 shows the implementation of this Direct ON-OFF Controller for the Single Phase PDM Converter case. If an additional integrator is involved in the regulation, then the controller is known as "Integral Controller or delta modulation"[1,2]. If additional complexity of the controller is not a problem, the so called "Mode Controller" which minimizes a cost function is even possible. More detailed discussions about these controllers can be found in references [4,5].

### 3.1.3 Review of Theory Pertaining to a Three Phase Full Bridge PDM Converter

Again operation of the three phase full bridge PDM converter can be divided to two categories. The first category utilizes a voltage regulation technique where 3Ø-low frequency AC voltages are synthesized from an existing Parallel Resonant HF AC Link. The currents on the low frequency side are dependent variables and determined by the load and the synthesized voltages. A given set of balanced low frequency reference voltages are synthesized using either half cycles of the HF Link voltage or the zero voltage state by the switching action of the 3Ø-PDM converter. This perspective is extensively covered in references [1,2,3]. The maximum level of the peak low frequency AC line to line voltage that can be synthesized using a three phase full bridge power converter is given, on average as

$$V_{\text{LF AC ll}}^{\text{max peak}} = \frac{2V_{HF}}{\pi} \qquad 3.1.2$$

and the maximum level of the peak low frequency AC line to neutral voltage can be derived from the above formula by simply dividing this equation by $\sqrt{3}$ as follows

$$V_{\text{LF AC ln}}^{\text{max peak}} = \frac{2V_{HF}}{\sqrt{3}\pi} \qquad 3.1.3$$

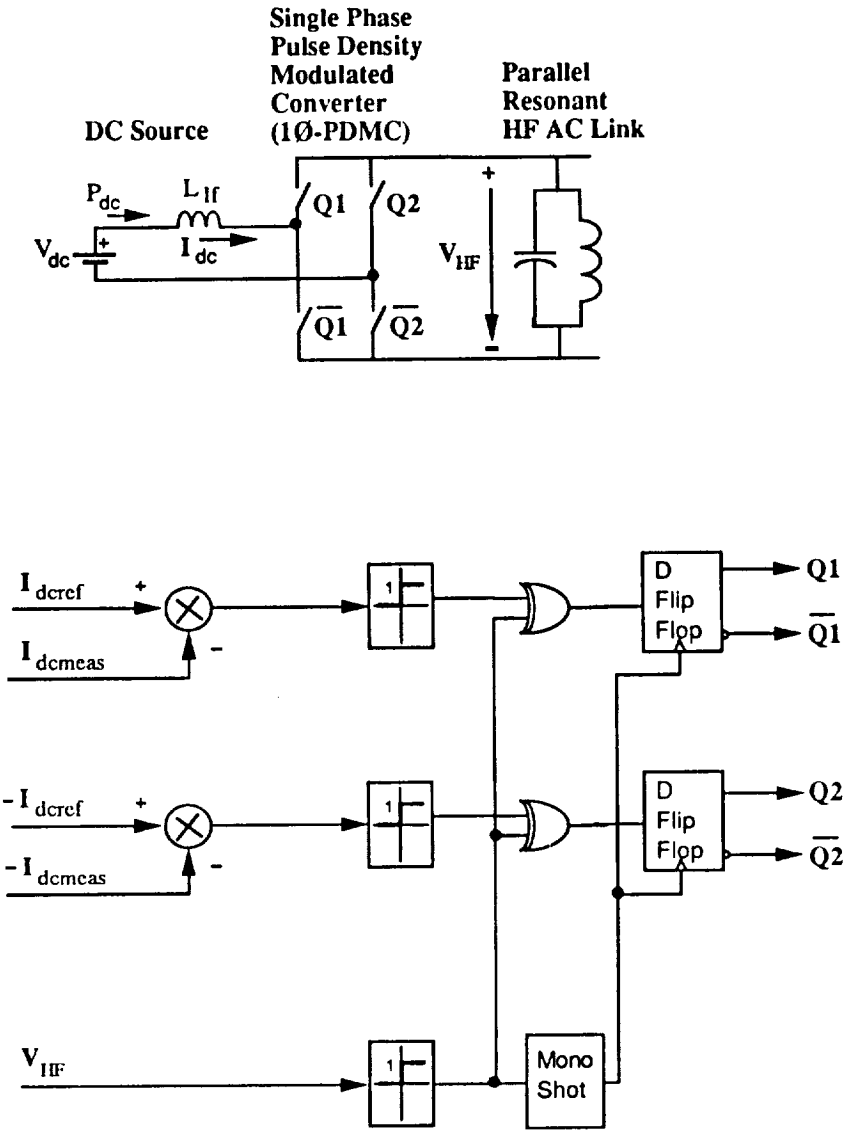



Fig. 3.2. Direct ON-OFF Current Regulator for Single Phase PDMC.

It is worthwhile to note that the derivation of the above two formulas in references [1,2,3] are done with the assumption of using a half bridge power circuit. That is, HF link voltage is split into two equivalent portions and the midpoint of this equivalent resonant circuit and the neutral point of the 3Ø AC side are assumed to be the same. Therefore the values given here and in references 1-3 are not same.

The second category utilizes a current regulation technique where 3Ø-low frequency AC currents are regulated with the switching action of 3Ø-PDMC and the interaction between the Parallel Resonant HF AC Link and 3Ø-low frequency AC source through line side filter inductors. In this technique, synthesized 3Ø-low frequency AC voltages are dependent variables and determined by the switching action of 3Ø-PDM converter and the Parallel Resonant HF AC Link voltage polarities. The line filter inductors shown in Fig. 3.3 determines the size of the ripple currents imposed on the 3Ø-low frequency AC currents and allows energy to be stored and dumped when required. It should not be forgotten however that the size of the ripple current can be reduced at the expense of slower system response to the fast varying peak link voltage. This second perspective is covered extensively in reference [6].

A similar type of current regulation technique is used even for variable frequency type of 3Ø loads operating from Parallel Resonant HF AC Link via 3Ø-PDMC Bridges as covered in references [4,5] for a Load Side PDMC.

The switches used in these 3Ø-PDMC Bridges must again have bidirectional voltage blocking capability since the HF Link is a Parallel Resonant AC Link. Similarly they should have bidirectional current carrying capability because the currents are alternating and bidirectional power flow operation is required.

### 3.1.4 Principle of Operation of a Three Phase Full Bridge PDM Converter

As in the Single Phase PDMC Bride case the second perspective concerning operation of a 3Ø-PDMC Bridge is convenient for conceptualizing the behavior its behavior. In this case, the Parallel Resonant HF AC Link must be established and maintained when operating from a 3Ø-60Hz utility grid. Once the operating principle is established for a Single Phase PDMC Bridge operating from a DC supply, it is then easier to understand the operating principle for the 3Ø-PDMC Bridge when the source is a 3Ø-60Hz utility grid.

As shown in Ref 6 both by means of computer simulation and experimentally, power flow control and maintenance of the HF Link is managed mainly by controlling the line filter inductor currents on the 3Ø-60Hz utility grid side of the converter. As shown in

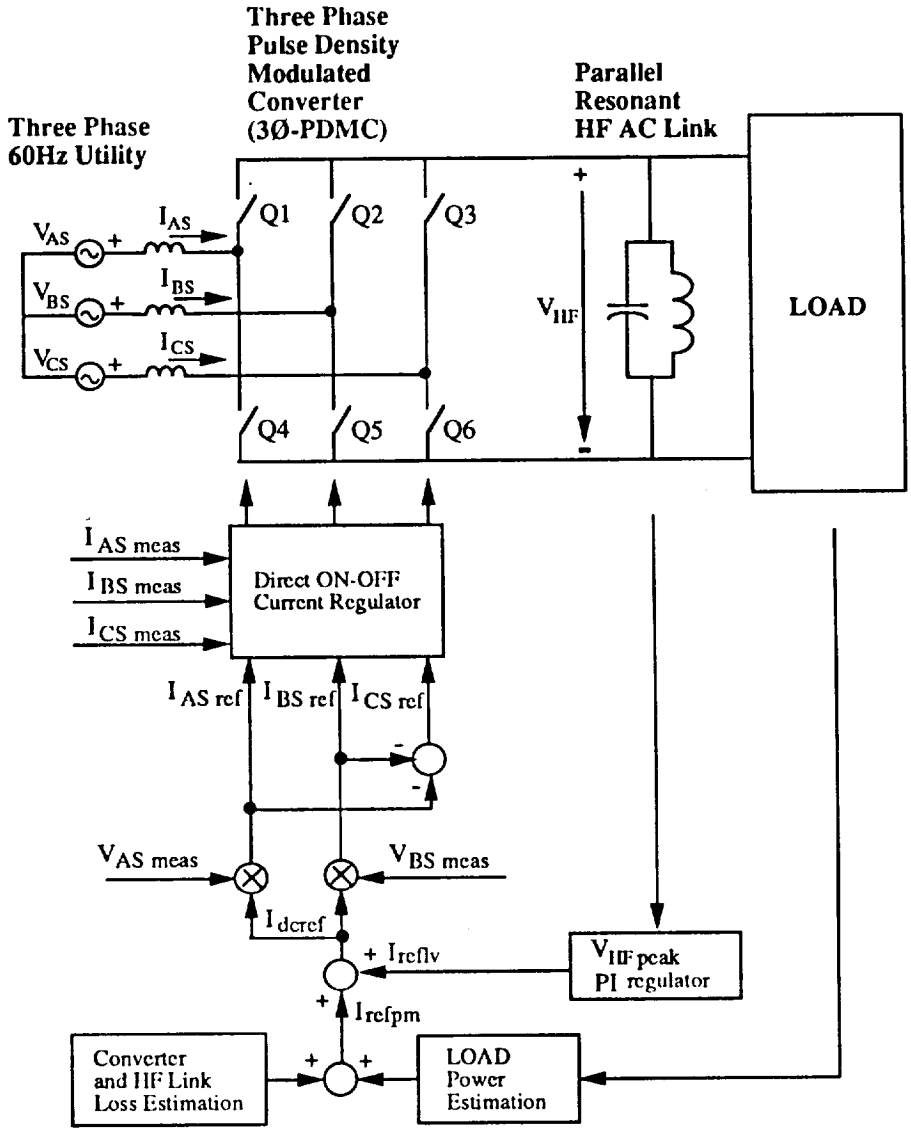



Fig. 3.3. Block Diagram of Direct ON-OFF Current Regulated 3Ø-PDMC Operating from 3Ø-60 Hz Utility at Unity Power Factor and Parallel Resonant HF AC Link.

Fig. 3.3, the gating logic of the switches in the 3Ø-PDMC Bridge are determined by comparing measured and reference currents. The direct type of ON-OFF Current Control Technique is covered here because of its simplicity. The reference phase currents are generated through the multiplication of source phase voltages with a DC reference current whose components are determined by the required load power, the operational losses of the source side and load side PDM converter and the HF Link.

For positive power flow, the link voltage reduces when instantaneous power is less than the total average power required by the load and operating losses of the converters and the link. At this time, the amplitudes of all the 3Ø source side reference currents are increased on an instantaneous basis by an increase in the DC reference to dump more energy from the source to the link during the next half cycle of the HF link. Hence, depending on the instantaneous values of these reference and the measured currents and the polarity of the HF Link voltage, gating signals for the 3Ø-PDMC switches are generated. These 3Ø reference currents can be either polarity and have different instantaneous values. However, their sum must add to zero for a balanced 3Ø set of currents. If any of the reference phase currents are positive and measured current is less than this value, the link voltage that supports the measured current (with its polarity) is reflected to that phase in the related branch of the 3Ø-PDMC Bridge. There are three other alternatives for the combination of the reference and measured currents of 3Ø source. If all of these four combinations can be tabulated the following set of conditions is obtained:

1. $I_{ref}$ is positive and $|I_{measured}| < |I_{ref}|$: Supporting polarity of $V_{HF}$ is selected (-)
2. $I_{ref}$ is positive and $|I_{measured}| > |I_{ref}|$ : Impeding polarity of $V_{HF}$ is selected (+)
3. $I_{ref}$ is negative and $|I_{measured}| < |I_{ref}|$ : Supporting polarity of $V_{HF}$ is selected (+)
4. $I_{ref}$ is negative and $|I_{measured}| > |I_{ref}|$ : Impeding polarity of $V_{HF}$ is selected (-)

It is important to note that any of these four reference and measured current combinations could exist for any phase of the 3Ø AC source. These four combinations cover all possible operating conditions including bidirectional power flow.

For positive power flow, the peak link voltage increases when instantaneous power is more than the total average power as required by the load and losses in the converters and the link. In this case, the DC reference command is decreased causing the amplitudes of the 3Ø reference currents to decrease. The reference and the measured currents take shape according to their initial values and switching action of the 3Ø-PDMC whose rules are given above. For negative power flow, the peak link voltage reduces when instantaneous power is less than the total average power absorbed by the source, and

increases when it is more than this value. Similar arguments are valid for the 3Ø reference and measured currents.

The maximum size of the ripple current depends heavily on the size of the line inductor, the peak of both the link and source phase voltages and the switching pattern of the converter. As stated earlier it should not be forgotten that the size of the ripple current can always be reduced at the expense of slower system response to the fast varying peak link voltage.

To aid in understanding the operational principles of the Direct ON-OFF Current Regulated 3Ø-PDMC Bridge, a computer simulation trace is given in Table 3.1. In this simulation, the peak value of the source side low frequency line to line voltage is 170 V, the peak value of the HF Link Voltage is 500 V, and the line inductor value is 1 mH per phase. It is illustrative to examine Table 3.1 together with Fig. 3.3. Note for example, that at the end of assumed first half cycle of the HF Link, the source side phase A actual current is -1.96 A; and the reference current is 1.16 A. The desired reference current flows in the positive direction, whereas the actual current flows in the negative direction. The actual current should clearly be forced towards its reference value. If the positive polarity of $V_{HF}$ is reflected to phase A of the source by selecting switch Q1 in the coming half cycle, the actual current will continue to flow in the negative direction and it will even increase in amplitude. The opposite effect, however, is required. Therefore, it is necessary to select switch Q4 which would reflect the negative polarity of the link voltage to phase A of the source in the coming half cycle which will then force the actual current towards its reference. That explains why the negative polarity is circled under column Q4 for the next cycle switch selection. With this switch selected, phase A source current reaches 1.9 A at the end of the second half cycle of the link and at this time the actual current exceeds its reference, which is 1.7 A at the same instant. Since the actual current is now greater than its reference, it is necessary to reduce the current in the next half cycle. In order to achieve this result, it is necessary to reflect a positive polarity of $V_{HF}$ to this phase. Since the link voltage changes its polarity every half cycle, the switch Q4 will again do this job. Hence, switch Q4 is selected for the third cycle as shown at the end of the second row of $I_{as}$.

Similar arguments are carried out for the other phases of the source. It can be seen in Table 3.1 that the sum of the 3Ø currents either for actual or reference sums to zero at any particular instant because balanced 3Ø sets of currents are assumed in the simulation.

This type of current regulation technique is again known as a "Direct ON-OFF or Bang-Bang Controller." No integration is involved in regulating 3Ø currents. Figure 3.4 shows an implementation of such a Direct ON-OFF Controller for the 3Ø-PDMC case. More detailed discussions, comparisons and the trade-offs among Direct ON-OFF, Integral

| Needed Information for Switch Selection | | | | Next Half Cycle Switch Selection (Circled) | |
|---|---|---|---|---|---|
| | Assumed Half Cycle of the HF Link | Actual Current in Amps | Reference Current in Amps | S1 | S4 |
| $I_{as}$ | 1st half cycle | -1.96 | 1.16 | + | ⊖ |
| | 2nd half cycle | 1.90 | 1.70 | − | ⊕ |
| | 3rd half cycle | -0.10 | 2.40 | + | ⊖ |
| | 4th half cycle | 1.70 | 1.09 | − | ⊕ |
| | 5th half cycle | ..... | ..... | + | − |
| | 6th half cycle | ..... | ..... | − | + |
| | 7th half cycle | ..... | ..... | + | − |
| | Assumed Half Cycle of the HF Link | Actual Current in Amps | Reference Current in Amps | S2 | S5 |
| $I_{bs}$ | 1st half cycle | -7.26 | -9.39 | ⊕ | − |
| | 2nd half cycle | -9.00 | -9.60 | − | ⊕ |
| | 3rd half cycle | -10.70 | -9.80 | + | ⊖ |
| | 4th half cycle | -8.40 | -10.30 | − | ⊕ |
| | 5th half cycle | ..... | ..... | + | − |
| | 6th half cycle | ..... | ..... | − | + |
| | 7th half cycle | ..... | ..... | + | − |
| | Assumed Half Cycle of the HF Link | Actual Current in Amps | Reference Current in Amps | S3 | S6 |
| $I_{cs}$ | 1st half cycle | 9.23 | 8.23 | ⊕ | − |
| | 2nd half cycle | 7.00 | 7.80 | ⊖ | + |
| | 3rd half cycle | 10.80 | 7.40 | ⊕ | − |
| | 4th half cycle | 6.75 | 9.26 | ⊖ | + |
| | 5th half cycle | ..... | ..... | + | − |
| | 6th half cycle | ..... | ..... | − | + |
| | 7th half cycle | ..... | ..... | + | − |

Table 3.1. Example of Switch Selection Pattern for Direct ON-OFF Current Regulated 3Ø-PDMC Operating from 3Ø-60 Hz Utility and Parallel Resonant HF AC Link. (Selected switches are circled; Positive and negative signs at the right hand two columns show the polarity of $V_{HF}$ which will be reflected to the related source side phase when the specified switch is selected for the next half cycle of the HF Link.)

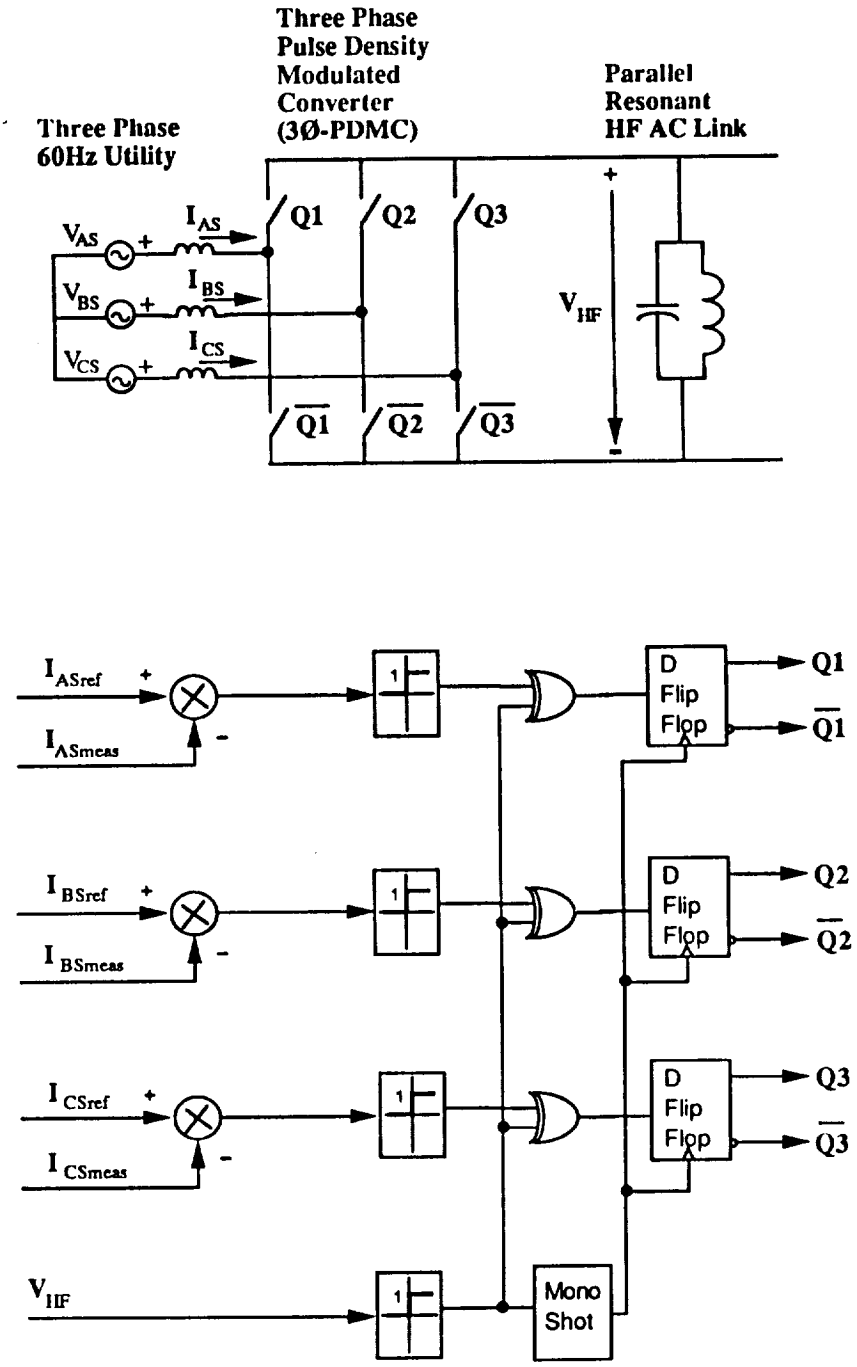



Fig. 3.4. Direct ON-OFF Current Regulator for 3Ø-PDMC

and Mode Controllers can be found in Refs. 4,5, and 6.

## 3.2 Power Switch Selection

It has already been shown that a 3Ø-PDM Converter Bridge operating from a Parallel Resonant HF AC Link employing bidirectional power flow requires bilateral switches. Since there are no manufactured bilateral switches for the time being, these switches still have to be implemented from unidirectional devices. As suggested and discussed in Ref. [1], some of these switch configurations are shown in Fig. 3.5.

Among the devices manufactured, only the thyristor (SCR) has a built-in bidirectional voltage blocking capability. No solid state switches except the low performance triac has bidirectional current carrying capability. Therefore, only the SCR can be directly paralleled to configure a bilateral switch as in Fig. 3.5.a. However, since SCRs do not have gate turn-off capability, either forced commutation or natural commutation by means of the Parallel Resonant HF AC Link should be incorporated. A detailed discussion about the utilization of naturally commutated SCRs utilizing a zero voltage switching scheme can be found in Ref. [1].

It is well known that the Gate Turn-off Thyristor (GTO) also does not have a reverse voltage blocking capability. This device behaves essentially as a resistor which does not conduct significant current when reverse voltage is applied across the anode and cathode. Therefore, it can not be paralleled to configure a bilateral device as in the case of the SCR. Thus, to include reverse voltage blocking capability for AC switching, an additional diode must necessarily be included with the GTO [7,8]. To include both bidirectional current carrying and voltage blocking capability, one of the switch configurations b, c or d in Fig. 3.5 is required. The only difference is to replace the transistor type of devices with GTOs and simply replace the anode-cathode connections with collector-emitter connections respectively.

With other devices such as power darlingtons, Bipolar Junction Transistors (BJTs) and Insulated Gate Bipolar Transistors (IGBTs), and Mos-Controlled Thyristors (MCTs), again the switch configurations shown in Fig. 3.5.b, c and d are required because these devices have neither bidirectional voltage blocking nor bidirectional current carrying capabilities. It should be noted that there are a number of trade-offs between the configurations in Fig. 3.5.b, c and d. These trade-offs are discussed at the end of Section 3.2.2 in summarized form.

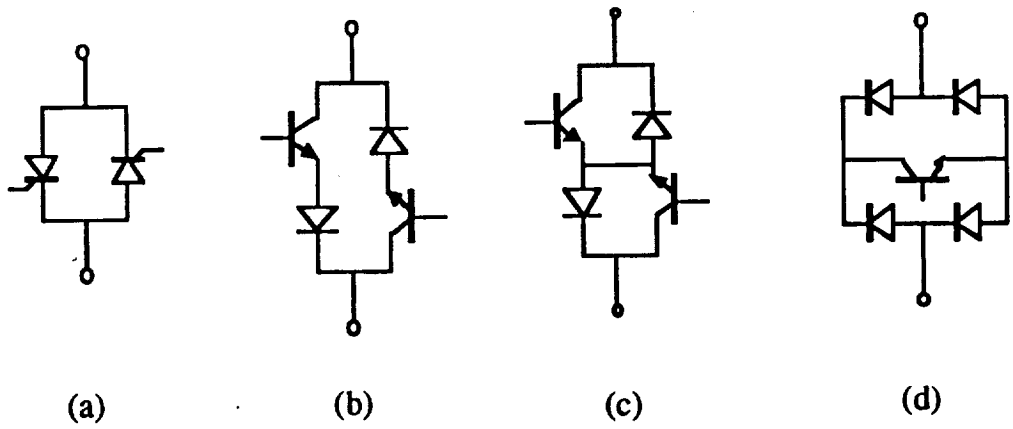



Fig. 3.5. Bilateral Switch Configurations.

As the desired power transfer level increases, it is well known that the bilateral device stresses also increase. The system reported in references [1-6], is a relatively low power converter system which can handle a maximum of about 2 kW power transfer from the source to load. In the latest phase of the study, a 7.5 kW converter was constructed to supply power to a AC Induction Motor dynamometer load rated at 3Ø, 300 Hz, 6 poles, 7.46 kW (10 hp), 230 V ,and 32 A. If this machine is to be operated via 3Ø-PDM converter operating from a Parallel Resonant HF AC Link, the power switches as well as the base drive units consequently had to be upgraded.

### 3.2.1 Review of Bilateral Switches Used Previously

The bilateral switch configuration used in previous years' investigations is shown in Fig. 3.5.c. In this case the switches used to configure the bilateral switch are two-stage power darlingtons. These switches have built-in anti-parallel diodes. They require no additional diode at the expense of non-alterable reverse recovery behavior. The key characteristics of an individual two-stage power darlington transistor, MJ10016, are given by Motorola in Table 3.2. As seen in Table 3.2, the total maximum turn-off time is given as 3.5 μsec for the 20 A. collector and 1 A. base current case. Approximately a 10 A. base current would be needed to achieve the same turn-off time with a 50 A. collector current as specified in the ON characteristics.

The design of the base drive units, designed for use with the previous 2 kW prototype, are capable of supplying only a 1 A base drive current so that a maximum 20 A collector current can be achieved without extensive modification. Unfortunately the base drive units were already bulky with substantial cooling needed even at no load. Also the

| | |
|---|---|
| OFF Characteristics | $V_{CEO(sus)}$=500 V |
| ON Characteristics | $I_C$=50 $A_{dc}$ , $I_B$=10 $A_{dc}$, $V_{CE(sat)}$=5.0 $V_{dcmax}$<br>$I_C$=20 $A_{dc}$ , $I_B$=1 $A_{dc}$ , $V_{CE(sat)}$=2.2 $V_{dcmax}$ |
| Diode Forward Drop | $I_F$=20 $A_{dc}$ , $V_F$=2.5 $V_{dctyp}$ and 5.0 $V_{dcmax}$ |
| Switching Characteristics | Max delay time $t_d$=0.3 µsec<br>Max rise Time $t_r$=1.0 µsec<br>Max storage Time $t_s$=2.5 µsec<br>Max fall Time $t_f$=1.0 µsec |

Table 3.2. The Key Characteristics of MJ10016 Two-Stage Bipolar Power Darlington Transistor Manufactured by Motorola Used in the Initial Prototype.

darlington drivers were found unsuitable for a high frequency drive because of the large stray capacitance of the 60 Hz isolation transformer. Finally, the constant base drive current (which is independent of the load current) resulted in a variable turn-off time as can be noted from Figs. 3.6 and 3.7. That is, the device has a short turn-off time when it operates in or close to the active region (loaded conditions), and has a long turn-off time when it operates in heavy saturation (light load conditions). This type of behavior can be observed from Figs. 3.6 and 3.7. The turn-off times of the devices for zero voltage switching operating in 3Ø-PDMC must adjusted for the longest turn-off times for safe operation since interrupting the output current would produce a large voltage spike across the device. Figure 3.6 corresponds to operation with a heavy saturation case. Since the devices have long turn-off times for heavy saturation cases and turn-off times are adjusted for the longest possible turn-off time, there is almost no voltage spike in Fig. 3.6. On the other hand, Fig. 3.7 still corresponds to a saturated case, but not as heavy as in Fig. 3.6. In this case the devices have a shorter turn-off times causing early turn-offs. These early turn-offs causes the voltage spikes encountered in Fig. 3.7.

In experiments conducted to determine the the maximum turn-off times of these devices when heavily saturated, it was discovered that the turn-off times reach 7-9 µsec levels. Figure 3.8 confirms this delay condition. To reduce the turn-off times of these devices, Baker Clamp circuits are used with the bilateral switch as shown in Fig. 3.9. With the use of clamp circuits, the devices are pushed to operate in the quasi-saturation region and the turn-off times of the devices are reduced from 7-9 µsec to around 2 µsec, and even less than that for some cases. Fig. 3.10 shows the turn-off time of a device after Baker Clamp Circuit has been added. Figures. 3.8 and 3.10 can be compared to observe

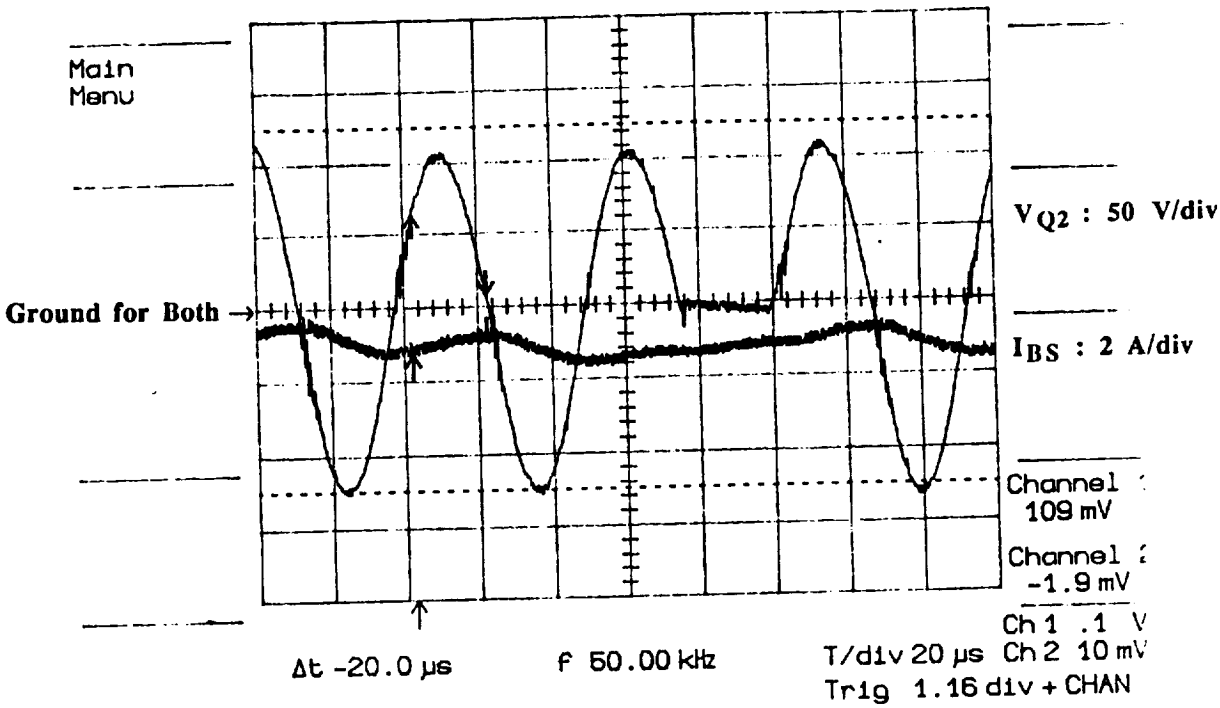



Fig. 3.6. Lightly Loaded Condition for MJ10016 Showing Long Turn-off Times with no Spike in the Bilateral Device Voltage; Bilateral Device Voltage: $V_{Q2}$ : 50 V/div. Phase B Source Current: $I_{BS}$ : 2 A/div. Time/div: 20 μsec.

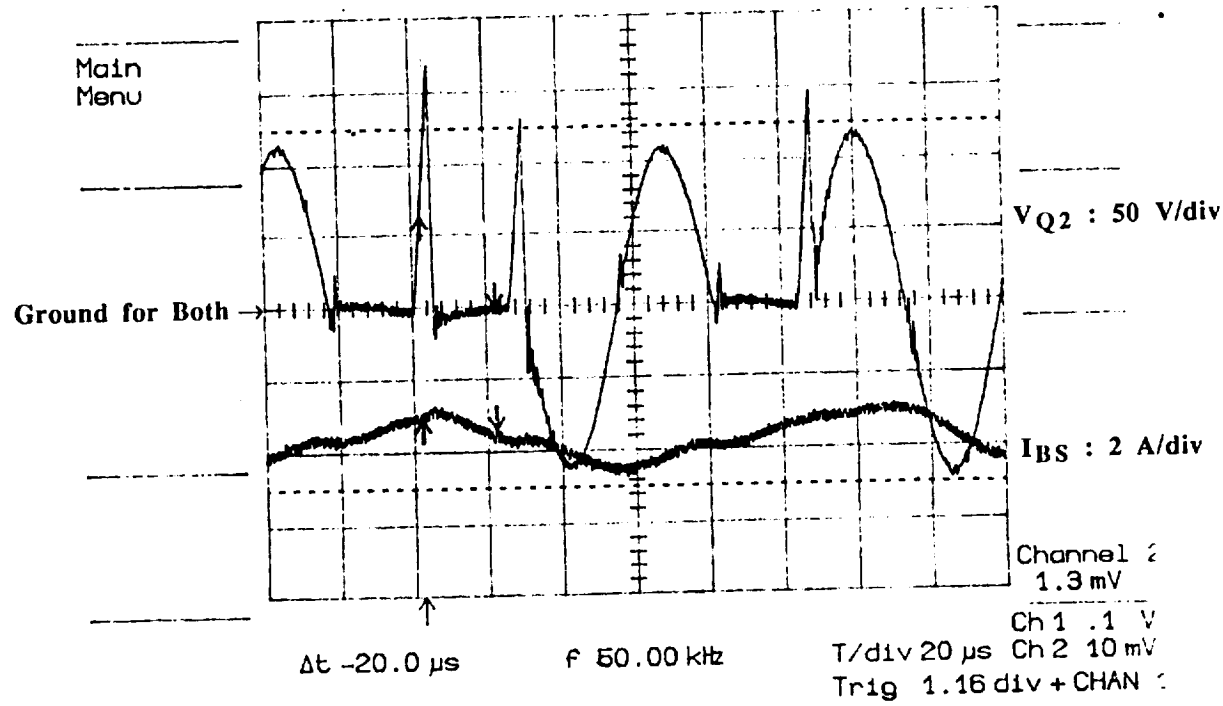



Fig. 3.7. Loaded Condition for MJ10016 Showing Short Turn-off Times with Spikes in the Bilateral Device Voltage; Bilateral Device Voltage: $V_{Q2}$ : 50 V/div. Phase-B Source Current: $I_{BS}$ : 2 A/div. Time/div: 20 μsec.

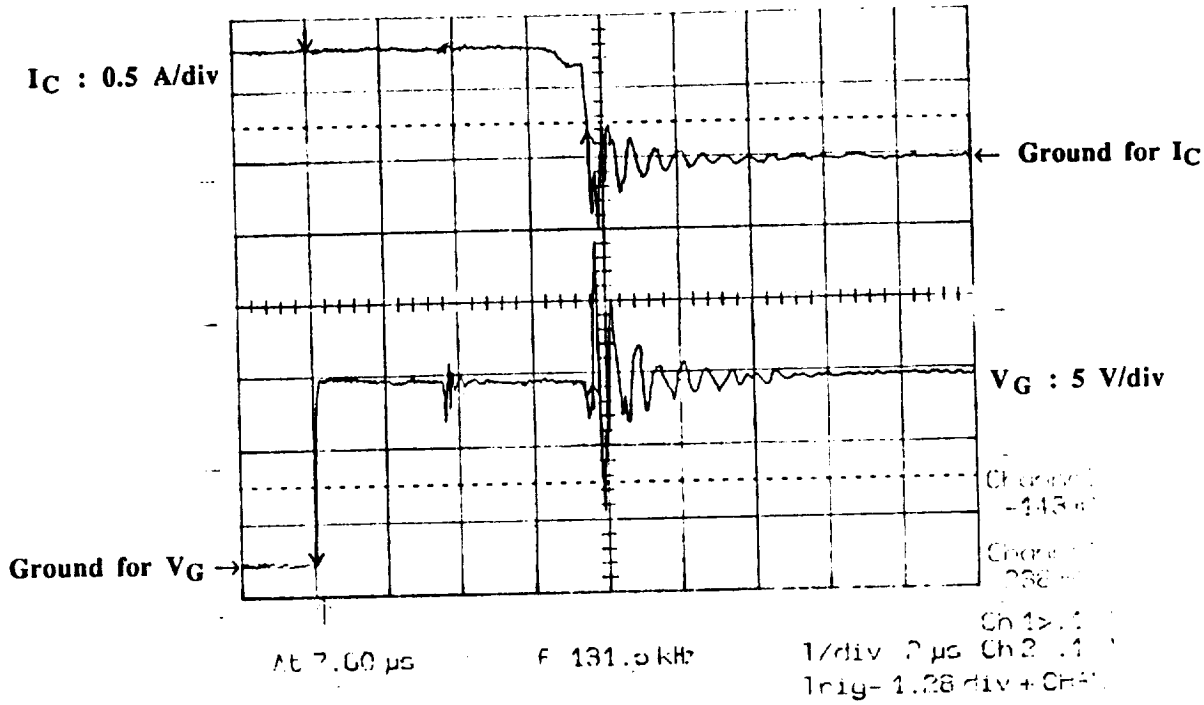



Fig. 3.8. Turn-off Time of MJ10016 Two-Stage Bipolar Power Darlington at Light Load without Baker Clamp Circuit Utilization; Collector Current: $I_C$ : 0.5 A/div. Gating Control Signal: $V_G$ : 5 V/div. Time/div: 2 µsec.

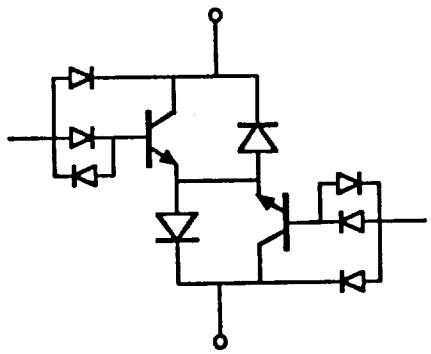


Fig. 3.9. Utilization of Baker Clamp Circuits for the Bilateral Switch Configuration in Fig. 3.5.c.

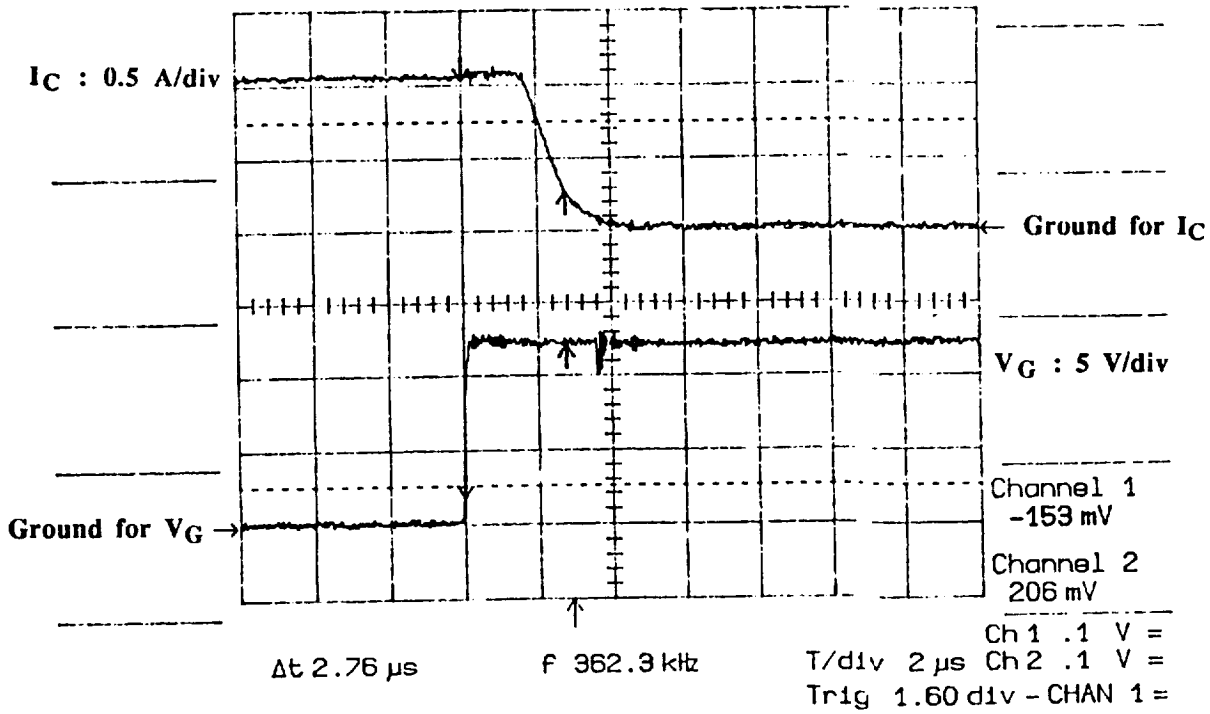



Fig. 3.10. Turn-off Time of MJ10016 Two-Stage Bipolar Power Darlington at Light Load with Baker Clamp Circuit Utilization; Collector Current: $I_C$ : 0.5 A/div. Gating Control Signal: $V_G$ : 5 V/div. Time/div: 2 μsec.

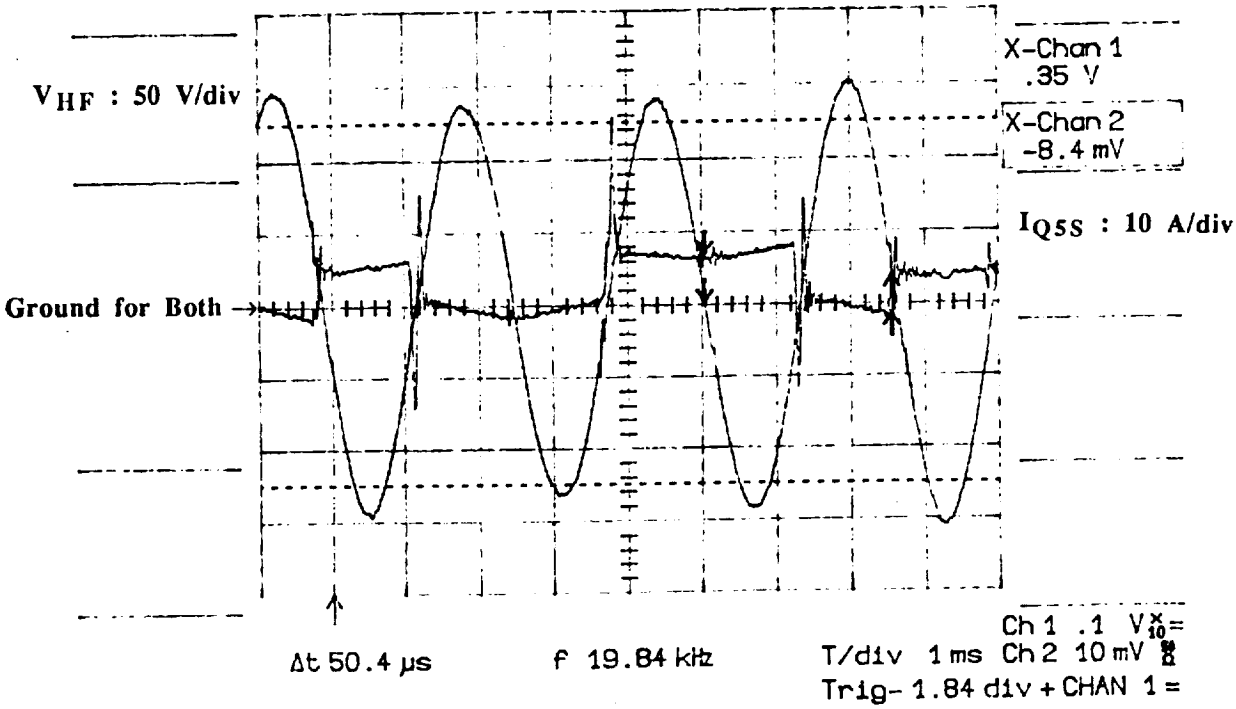



Fig. 3.11. Current Spikes due to the Reverse Recovery Problem of Built-in Anti-Parallel Diodes in MJ10016 Two-Stage Bipolar Power Darlingtons. Sinusoidal Trace: HF Link Voltage: $V_{HF}$ : 50 V/div. The Other Trace: Bilateral Device Current: $I_{QSS}$ : 10 A/div. Time/div: 20 μsec.

the difference between the turn-off times before and after the Baker Clamp Circuit is used.

Another problem encountered with the MJ10016 darlington when operated in 3Ø PDM converter bridges configuration is the reverse recovery problem of the built-in anti-parallel diode. These diodes causes high current spikes during their reverse recovery periods probably because they have relatively large stored charge to recover and they are fast recovery types. The size of these current spikes sometimes reaches to more than three times its normal conduction current. This behavior for a case of 40 kHz switching frequency, can be observed from Fig. 3.11 indicating a spike reaching 26 A for a case in which 7 A is the normal device current. To overcome this problem, a saturable inductor was designed to reduce the size of these spikes by reducing the di/dt of the current. Unfortunately, this in turn delays the reverse recovery period of the diode since the same amount of charge must be recovered. This saturable inductor shows better performance when facing reverse recovery. If reverse recovery occurs when this inductor is saturated however, it cannot prevent spikes totally. Figures 3.12 and 3.13 show the performance of the saturable inductor for least and most initial saturation respectively. Figure 3.13 corresponds to a case where the inductor is almost saturated and where the spike is not totally prevented but its amplitude is still reduced. These pictures were taken with a peak device current of 7 A. If a saturable inductor is not used, the SOA limit of the device will certainly be affected for high current operations.

If the anti-parallel diode comes in built-in form with the transistor, its reverse recovery characteristic clearly cannot be changed by the user. Hence, it is important for the user of the switch to consider this point in advance and accordingly select the device which will minimize this current spike effect for high current operations. Therefore, if diodes with these properties (fast recovery and low storage charge) are not available in the built-in structure, diodes satisfying these requirements must be selected independently and used externally with transistors that do not have built-in anti-parallel diodes.

The forward voltage drop of the bilateral device configuration in Fig. 3.5.c is composed of two components. One voltage drop is due to the transistor and the other is the diode forward voltage drop. Depending on the individual forward drops of these devices, the conduction losses can be estimated. If the bilateral device configured from MJ10016 is pushed to operate at around 50 A device current range, it will require 10 A of base drive current. The darlington and diode will have a 5 V forward voltage drop each, totalling to 10 V forward drop for the bilateral device. This clearly indicates high conduction losses. Use of Baker Clamp Circuit further reduces the current gain of the device requiring further base current to handle the high collector current operations. However, it also reduces the forward drop of the bilateral device to around 7 V for the 50 A device current range. It

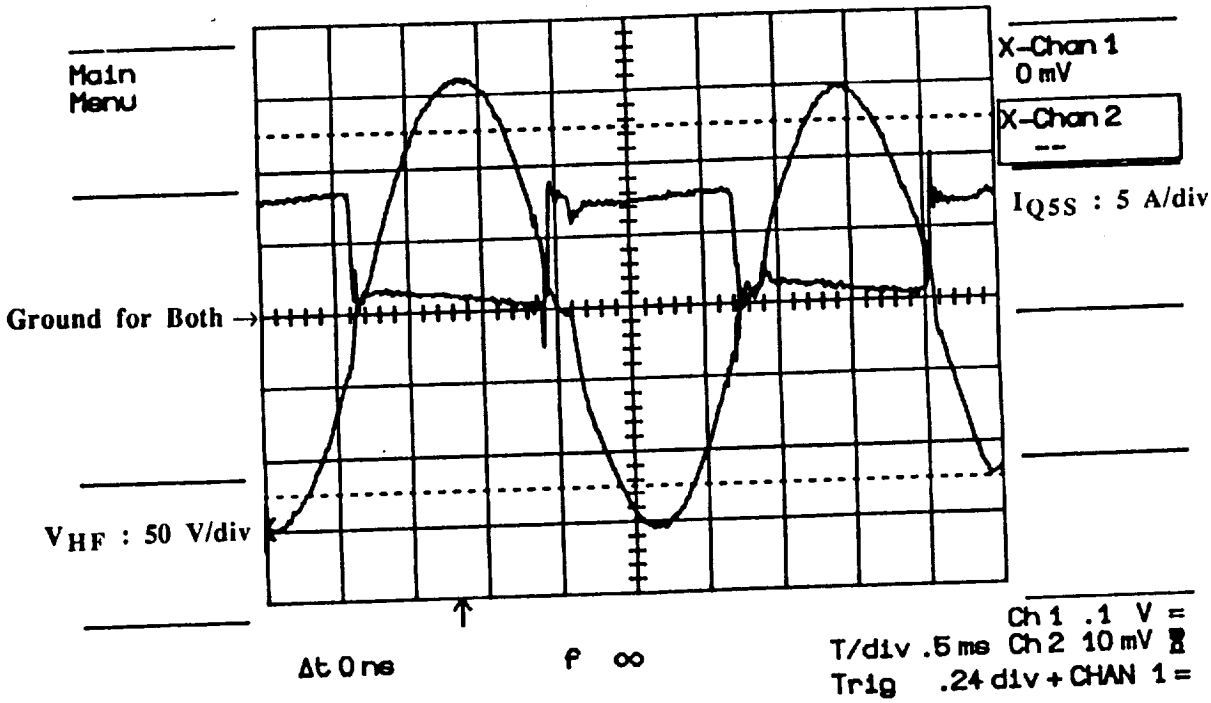



Fig. 3.12. Best Case of Improved Current Spikes after the Utilization of Saturable Inductor to Handle the Reverse Recovery Problem of Built-in Anti-Parallel Diodes in MJ10016. Sinusoidal Trace: HF Link Voltage: $V_{HF}$ : 50 V/div. The Other Trace: Bilateral Device Current: $I_{Q5S}$ : 5 A/div. Time/div: 10 μsec.

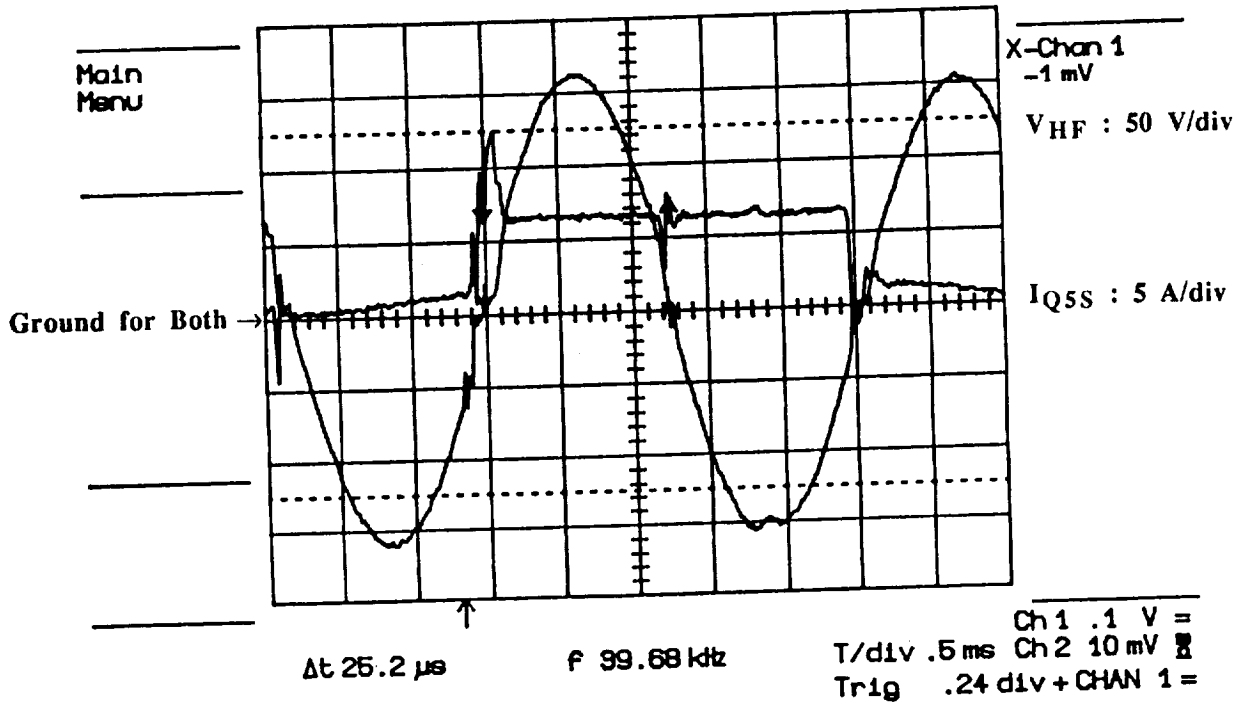



Fig. 3.13. Worst Case of Improved Current Spikes after the Utilization of Saturable Inductor to Handle the Reverse Recovery Problem of Built-in Anti-Parallel Diodes in MJ10016. Sinusoidal Trace: HF Link Voltage: $V_{HF}$ : 50 V/div. The Other Trace: Bilateral Device Current: $I_{Q5S}$ : 5 A/div. Time/div: 10 μsec.

would clearly be risky to push these devices to their limits because of the reasons discussed in the preceding paragraphs.

### 3.2.2 Switch Selection for Upgraded Power Level

From the preceding discussion in upgrading the power level of the 3Ø to 3Ø Power Converter System from 3 HP to one rated at 10 HP, the bilateral switch stresses and their ratings should clearly change. In order to satisfactorily supply the 10 HP induction motor dyno bilateral switches of the PDM Converters should operate in the range of blocking 600-650 V and conducting 60-90 A without facing any major safe operating area limitations. These values are estimated considering the link voltage variations which inevitably occur and the possible current spikes which exist during the reverse recovery periods of the devices.

Triple stage power darlingtons were available for the desired voltage and current ratings but unfortunately have long turn-off times for a 40 kHz switching frequency. For example, a 1200 V, 75 A Bipolar Transistor Module manufactured by Fuji [9] has a maximum total turn-off time of 17 μsec. Therefore, the turn-off command must be given 17 μsec in advance of the zero crossing of link voltage to achieve zero voltage turn-off. Since the half cycle of the HF AC Link at 20 kHz is 25 μsec and the turn-off times of these type of devices change with varying device currents, their utilization in this application is would be very difficult. In particular, if general purpose base drive units are used to drive these devices would be most likely the case, the problems associated with those drive units bring extra drawbacks.

Other devices which are reasonably fast in the required power range are GTOs, IGBTs and MCTs. One of the fastest GTOs available in the range of 1200 V, 90 A is offered by Hitachi. This device has a forward voltage drop of 2.8 V at 90 A, a turn-off time of 4.5 μsec and a turn-on time of 3 μsec. With the assumption of 2 V forward voltage drop of the diode used for bidirectional voltage blocking capability, the total bidirectional device forward drop becomes around 5 V for a switch configuration as shown in Fig. 3.5.b and c and about 7 V for a configuration as in Fig. 3.5.d. The turn-off time of the GTO greatly depends on the level of the current carried by the device. An example is given in reference [8] indicating that if an anode current of 5 A is turned off by extracting 1 A gate current, the storage and the fall times may be as long as 2.5 μsec and 2 μsec respectively. Whereas if the same 5 A anode current is switched off by extracting 5 A gate current, the storage and the fall times reduce to 0.5 μsec and 0.25 μsec respectively. Because a constant amount of current will be extracted from the gate of the GTO, turn-off

times will change depending on the level of current carried by the device. The GTOs will turn-off early for anode currents close to zero, and will turn-off late for anode currents far from zero. Since 3Ø low frequency currents change in time between their zero and peak, the level of the currents carried by the devices will change substantially during their switching at high frequency and zero voltage. Since the prediction of the turn-off times are constant and made in advance of the zero crossings and accommodates the longest turn-off times, these devices again can cause voltage spikes across the bilateral switches for early turn-off. In addition to this, GTOs require relatively high power for their gate drive units.

In general, IGBTs form the best choice for a suitable switch for a resonant converter of this rating. A 1000 V and 75 A IGBT manufactured by AEG is stated to have a forward voltage drop of 3 V at 75 A, a turn-off time of 0.9 μsec and a turn-on time of 0.5 μsec. Hence, with these characteristics, the IGBTs are much superior to the Bipolar Power Darlingtons and better than the GTOs mentioned above for the power range and operating frequency considered. With a device this fast, even if the turn-off times vary depending on the level of the current, the variation is limited to 1 μsec which this is very small compared to the 25 μsec half cycle of the link. Therefore, the effect of voltage spikes are very much reduced in this case. Bilateral device forward voltage drop is the same as in GTO case mentioned in the previous paragraph. The base drive units of the IGBTs are very compact and require very low power.

Another that is potentially useful is the MCT. A 1000 V and 300 A MCT device reported in reference [8] has a forward voltage drop of less than 1.61 V at 300 A anode current, a turn-off time of less than 1.28 μsec and a turn-on time of less than 0.5 μsec. The lower forward voltage drop of the MCT looks even better than the IGBT. Assuming again a 2 V forward drop for the diode used to add bidirectional voltage blocking capability, the total bilateral device forward drop becomes less than 3.61 V for the configuration in Fig. 3.5.b and c and 5.61 V for the configuration in Fig. 3.5.c. These relatively low forward drops help decrease conduction losses. The MCT is similar to the IGBT in that it requires a low energy gate drive unit. The primary drawback of the MCT comes in zero voltage switching applications. From the measurements made on Chapter 2 it appears that the MCT requires a certain amount of voltage across its anode-cathode terminals before it turns-on. It is interesting that this voltage varies considerably from device to device. It is reported that this voltage depends on the current rating of the on-FET of the MCT [10]. Higher current ratings are required for the on-FET of the MCT to reach the PNPN regenerative operation at low anode-cathode voltages. This means that in order to achieve turn-on of the MCT at low anode-cathode voltages, the current rating of the on-FET of the MCT should be raised. However, raising the on-FET current implies an

increase in the required gating energy. In this application, since switching occurs at the zero crossings of the high frequency AC Link voltage, turn-on of the MCT takes time because it waits for the link voltage to reach the desired voltage. During this period since both of the devices in any branch of the PDMC Bridge will be OFF, current in the low frequency side will increase the snubber capacitor voltages and will cause voltage spikes across the bilateral devices. This in turn will speed up the turn-on process at the expense of having voltage continuous spikes. The sizes of those spikes and the possible effects on the control circuit boards can be studied and, if desired, further research can be pursued to see the operation of these devices in PDMC Bridges. The MCTs on the other hand do not have any problem with a zero current switching schemes [11]. For this reason they seem to be one of the best candidates for applications using zero current switching.

When we compare all of the devices presently available, the IGBTs appear to be the most suitable for this application. The MCTs are not convenient for zero voltage switching scheme, Bipolar Power Darlingtons have very long and variable turn-off times, and the IGBTs are relatively much faster than the GTOs and do not have variable turn-off times as the GTOs does. Table 3.3 summarizes the overall issues involved.

The choice of a bilateral switch configuration as in Fig. 3.5.b or c leads to the following requirements:

- 24 unilateral switches, no additional diodes for built-in anti-parallel versions, thereby living with the reverse recovery current spikes of the built-in diodes, or
- 24 unilateral switch, 24 low storage and fast recovery power diodes without built-in anti-parallel versions, providing low reverse recovery current spikes,
- 24 base drive units,
- One unilateral switch forward voltage drop plus one diode forward voltage drop for the total bilateral device forward voltage drop.

The choice of a bilateral switch configuration as in Fig. 3.5.d leads to the following requirements:

- 12 unilateral switches, 48 low storage and fast recovery power diodes, providing low reverse recovery current spikes for the diodes,
- 12 base drive units, advantage of reduced complexity and number of base drive unit requirement with increased reliability,

| | Triple-Stage Bipolar Power Darlington | GTO | IGBT | MCT |
|---|---|---|---|---|
| Typical Turn-off Time | 17 µsec | 4.5 µsec | 0.9 µsec | 1.28 µsec |
| Typical Turn-on Time | 3 µsec | 3.0 µsec | 0.5 µsec | 0.50 µsec |
| Forward Voltage Drop | 2.8V@75A | 2.8V@90A | 3V@75A | 1.61V@300A |
| Turn-on at Zero Voltage | ok | might have problems | ok | problems |
| Gate Drive Requirement | medium power gate drive requirement | very high gate current is required for turn-off (28A) | low power and compact gate drive requirement | low power and compact gate drive requirement |
| Dependence of Turn-off Times on Current Level for Constant Base Current | heavily and effectively dependent | relatively less dependent | almost independent | almost independent |

Table 3.3. 1000-1200 V, 75-90 A Semiconductor Power Switch Comparison for 40 kHz Switching Frequency.

- One unilateral switch forward voltage drop plus two diode forward voltage drop for the total bilateral device forward voltage drop, disadvantage of increased conduction losses due to extra diode forward voltage drop.

In summary, the second configuration given with Fig. 3.5.d was selected as the bilateral switch configuration for the new 7.5 kVA dual converter. This configuration was chosen to reduce the complexity, building cost and time of the system at the expense of having an extra diode forward voltage drop. The IGBT used as a unilateral switch was selected for the upgraded power version for the system. The key characteristics of the IGBTs and external diodes to configure a new bilateral switch are given in Table 3.3. The forward voltage drop of this bilateral switch is measured in a DC chopper test conducted at 20 kHz and found to be approximately 7 V. Figure 3.14 shows a confirmation of this result.

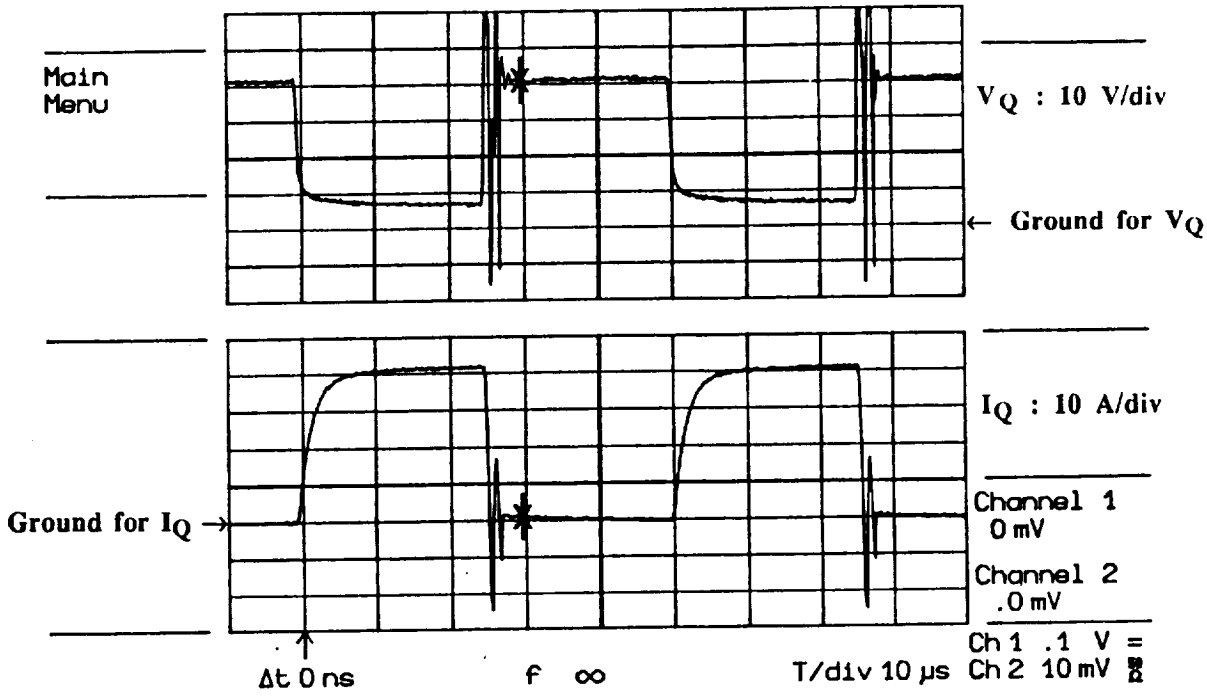



Fig. 3.14. Forward Voltage Drop of New Bilateral Device Configured from an IGBT and a Diode Bridge Around it as in Configuration Fig. 3.5.d; Bilateral Device Voltage: $V_Q$ : 10 V/div. Bilateral Device Current: $I_Q$ : 10 A/div. Time/div: 10 μsec.

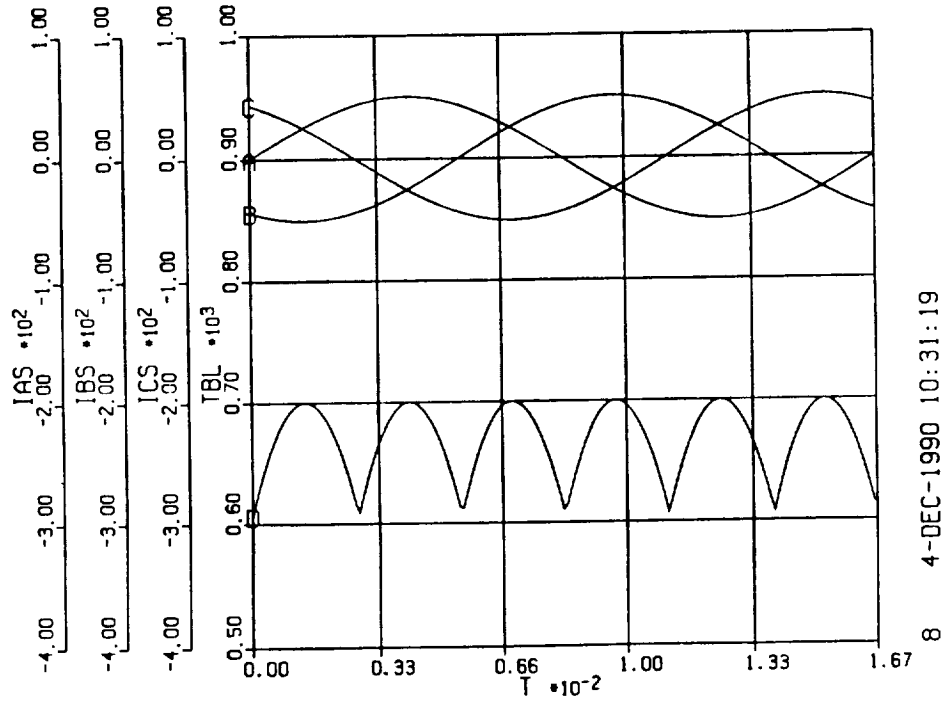



Fig. 3.15. Conduction Loss Variation of 3Ø-PDMC Operating at 35 A rms (50 A peak) 3Ø-60 Hz Line Current with a 7 V Forward Voltage Drop for each Bilateral Switch; Top Three Traces: Phase A, B and C Line Currents: $I_{AS}$, $I_{BS}$, $I_{CS}$ : 100 A/div. Bottom Trace: Total Bridge Loss (Conduction Loss Variation of 3Ø-PDMC): TBL: 100 W/div. Time/div: 3.33 msec.

### 3.2.3 Conduction Losses of 3Ø PDM Converters

When calculating the conduction losses of the converter bridge it should be recalled from Section 3.1.2 that at least 3 bilateral switches should be in conduction at any time to carry the 3Ø low frequency side currents. The maximum instantaneous conduction losses will occur during the peak of the low frequency current of any phase. If we assume that the maximum peak of the low frequency current of any phase for the load side PDM Converter is 50 A., then for 3Ø currents to add to zero a total of 50 A should be carried by the other two phases in the reverse polarity. This suggests a maximum instantaneous conduction losses of

50 A x 5 V+ I-50 AI x 5 V=500 W for the switch configuration in Fig. 3.5.b or c

and

50 A x 7 V+ I-50 AI x 7 V=700 W for the switch configuration in Fig. 3.5.d

for the load side PDM converter bridge where 5 V and 7 V are the forward voltage drops of the bilateral devices utilizing IGBTs..

The source side current is determined by active power required by the load and losses, source voltage and unity power factor. Once the peak source side current is determined, the maximum instantaneous source side PDM converter conduction losses can be estimated similar to the above case.

Simulation results have demonstrated that the difference between the maximum and the minimum values of instantaneous conduction losses is great. For example, the variation of the instantaneous conduction losses of the 3Ø-PDM converter bridge operating from 60 Hz, 50 A peak perfect sinusoidal currents is shown in Fig. 3.15. Since perfect sinusoids are assumed, this figure does not account for the high frequency ripple currents superimposed on the low frequency currents. In the simulation, since the switch configuration of Fig. 3.5.d is assumed, the 7 V forward voltage drop is used in the calculation of the instantaneous conduction losses of the bridge. The total instantaneous conduction losses of the 3Ø-PDM converter bridge is defined as Total Bridge Losses, TBL, in the Fig. 3.15. As can be seen from the figure, the maximum value of the conduction losses reaches 700 W as calculated above and the minimum value does not drop below 600 W for a 50 A current amplitude. Therefore, we can roughly assume a 650 W total average conduction losses for the bridge operating at a 50 A peak (amplitude) current. Of course, when the peak value of this low frequency current reduces, the total average conduction losses of the bridge reduce proportionally.

### 3.2.4 Stray Inductance Effect of New Bilateral Switch

Since the current level increases with increasing power level of the system, the stray inductance of the selected bilateral device configuration is crucial to the main unilateral switch, namely the IGBT, in terms of its Safe Operating Area (SOA) limits. In particular, the energy stored in the stray inductance of the configuration should not raise the voltage across the main device beyond the value permitted by its SOA limits when it is turned-off. Before the new configuration was utilized in the two PDMC Bridges, the stray inductance effect of this configuration was tested by means of a DC chopper. No snubber capacitor was used during the test. Tests were conducted at 10 and 20 kHz switching frequencies with half duty cycle operation, with currents reaching 75 amperes. Figure 3.16 shows the circuit schematic of the DC Chopper Circuit used to test the bilateral device. To test only the bilateral switch stray inductance effect, the freewheeling diode across the load was connected in such a manner so as to reduce the stray inductance of the power lines. The same gating logic circuit used during the MCT tests was again used.

The voltage spikes encountered due to stray inductance when the device is turned-off were recorded and given in Table 3.4 for different operating conditions. These values are the most pessimistic values because examination of the current and voltage is not done at exactly the same time instant. For example, the peak current value which is turned-off might have already reduced to a lesser value when the voltage spike peak was reached. Figure 3.17 was obtained from the data given in Table 3.4 and it is easier to follow the unilateral device stress from this figure. This figure reveals progressively more device stress for higher frequencies of operation. This is, in effect, fortunate because SOA limitations become more strict as the operating frequencies reduce. Another characteristic observed was that the device stresses increase for inductive loads. Figures 3.18 and 3.19 show the two individual cases from Table 3.4. One shows the results of a 10 kHz resonant link frequency and the other is at a 20 kHz operating frequency. Both cases show turn-offs for around 75 A device current for an inductive load case.

The information given in Table 3.5 is derived from the SOA characteristic curves of the IGBT device used to configure the switch. Since the data presented in Table 3.4 is a very pessimistic one, comparing the information given in Table 3.4 to the limits given in Table 3.5 is also the quite pessimistic. This comparison shows, however, that when operating at 10 kHz and 20 kHz with duty cycles the device remains within the SOA limits.

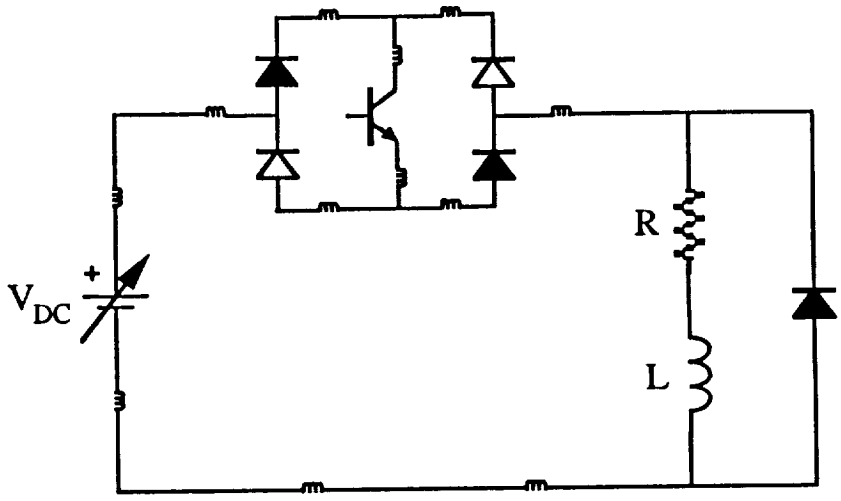



Fig. 3.16. DC-Chopper Circuit for Stray Inductance Effect Measurement of the New Bilateral Switch Configuration.

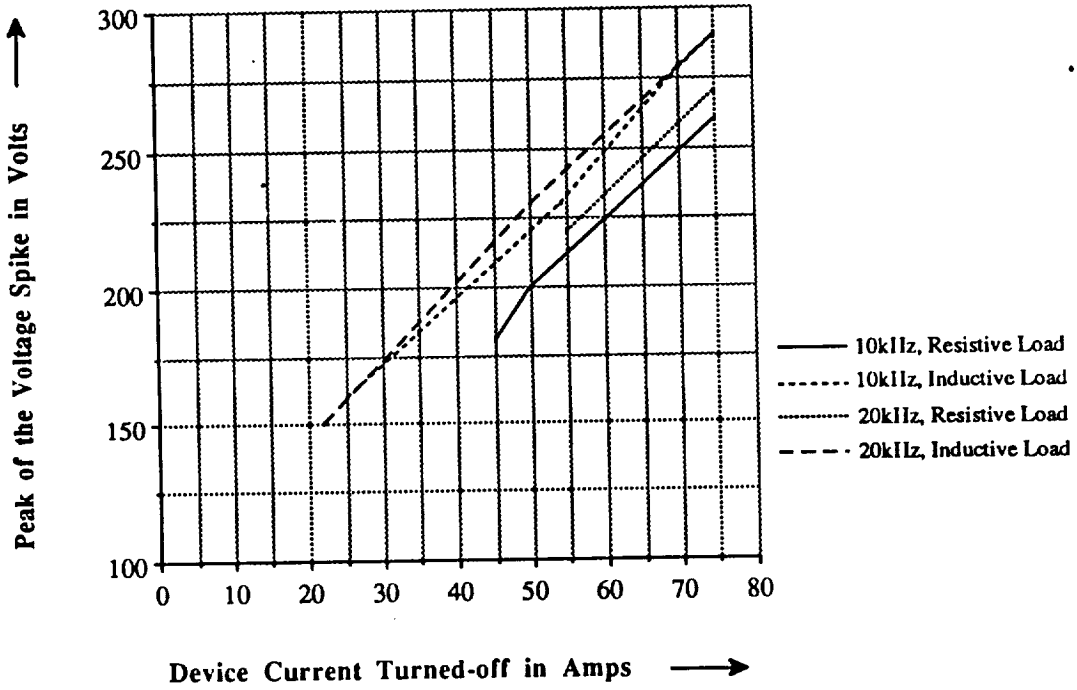



Fig. 3.17. Voltage Spikes at Turn-offs of IGBT Due to Stray Inductance of New Bilateral Switch Configuration.

| OPERATING CONDITIONS | RESISTIVE LOAD | | INDUCTIVE LOAD | |
|---|---|---|---|---|
| | Peak Current Value Switched-off (A) | Peak Voltage Spike Occuring at turn-off (V) | Peak Current Value Switched-off (A) | Peak Voltage Spike Occuring at turn-off (V) |
| 10 kHz 0.5 Duty Cycle 50µsec Current Pulse | 45 | 180 | 25 | 160 |
| | 50 | 200 | 54 | 230 |
| | 75 | 260 | 75 | 290 |
| 20 kHz 0.5 Duty Cycle 25µsec Current Pulse | 55 | 220 | 22 | 150 |
| | 75 | 270 | 50 | 230 |
| | 75 | 300 (extra stray) | 75 | 290 |

Table 3.4. Voltage Spikes at Turn-offs of IGBT Due to Stray Inductance of New Bilateral Switch Configuration.

| Allowed Maximum Voltage at Specified Current Levels | Pulse Width of the Current in µsecs |
|---|---|
| 370V at 75A | 50 µsec |
| 550V at 50A | 50 µsec |
| 230V at 75A | 100 µsec |
| 350V at 50A | 100 µsec |
| 70V at 75A | 1 msec |
| 100V at 50A | 1 msec |

Table 3.5. Safe Operating Area (SOA) Limits of IGBT at Various Current Levels and Pulse Widths (Operating Frequencies).

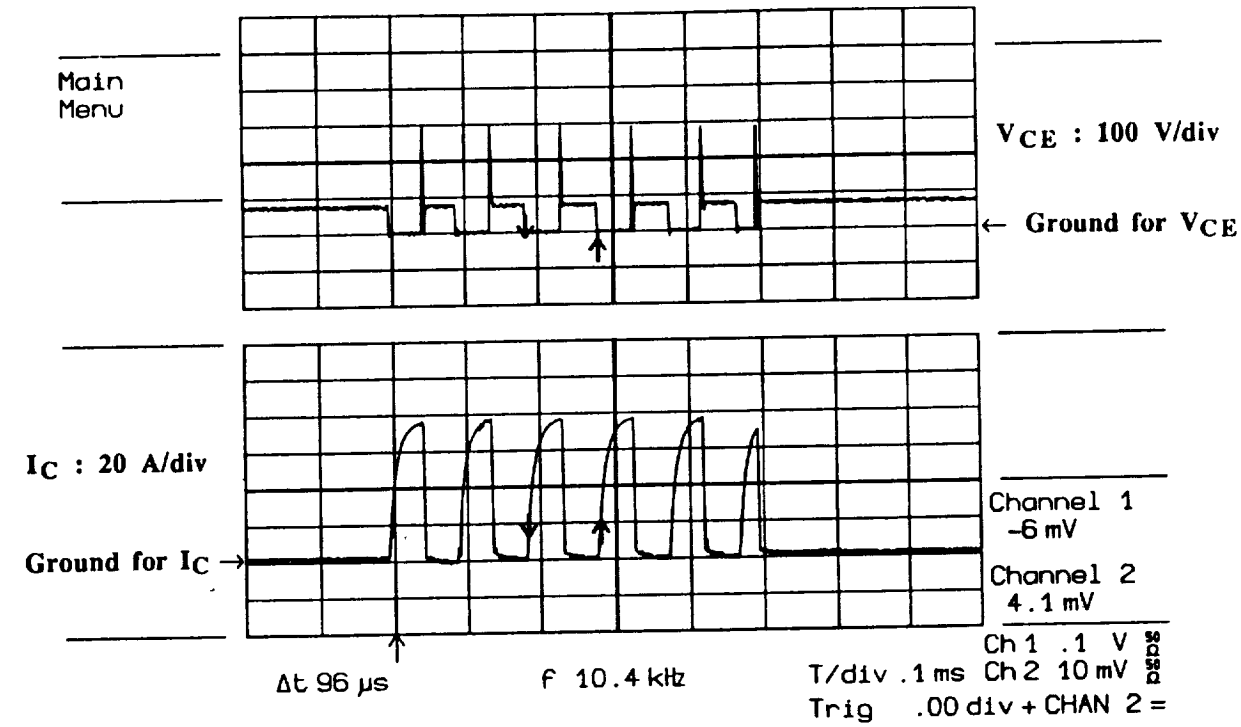



Fig. 3.18. Example Case for the Data in Fig.3.17 with 10 kHz Half Duty Cycle Operation and Switching-off Approximately 75 A Collector Current; IGBT Collector-Emitter Voltage: $V_{CE}$ : 100 V/div. IGBT Collector Current: $I_C$ : 20 A/div. Time/div: 100 μsec.

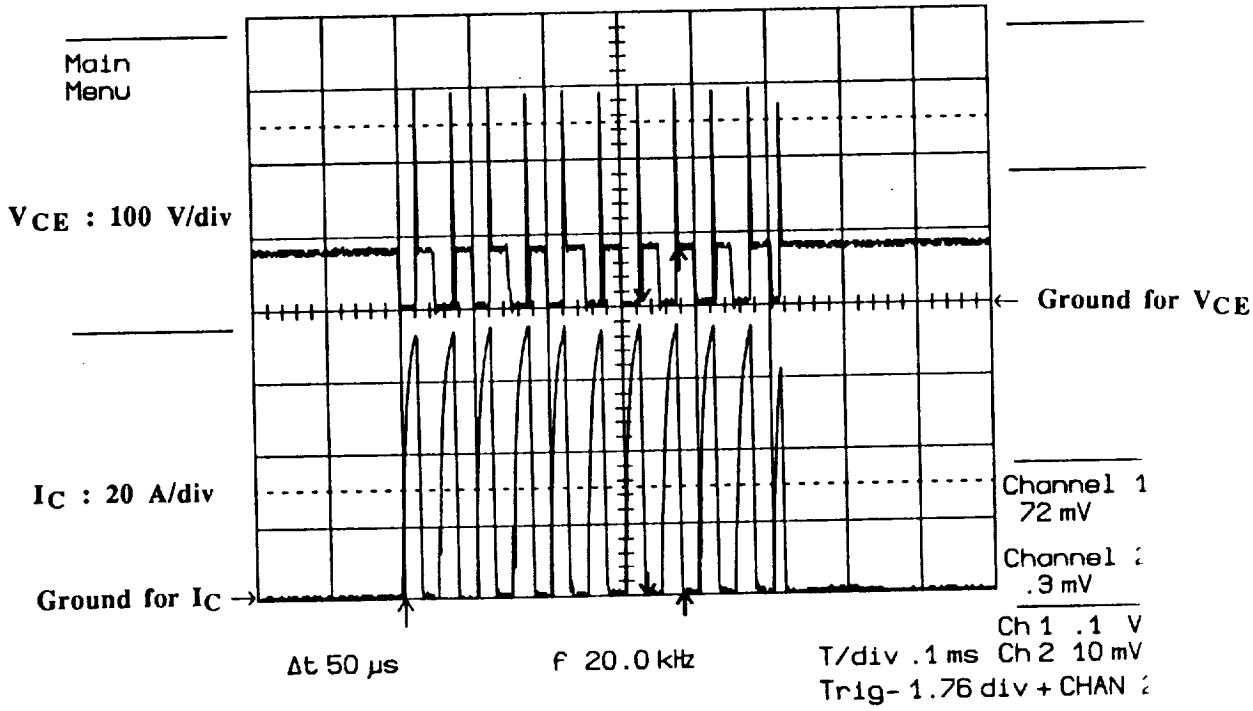



Fig. 3.19. Another Example Case for the Data in Fig.3.17 with 20 kHz Half Duty Cycle Operation and Switching-off Approximately 75 A Collector Current; IGBT Collector-Emitter Voltage: $V_{CE}$ : 100 V/div. IGBT Collector Current: $I_C$ : 20 A/div. Time/div: 100 μsec.

The length of the wire which is used to configure the bilateral switch was intentionally increased 6.5 inches to see the effect of additional stray inductance. This was done for a resistive load at 75 A and 20 kHz operating frequency with a one-half duty cycle. As seen from the Table 3.4, the additional stray inductance from the 6.5 inches of wire brings only a 30 V extra voltage spike for the same operating condition. To reduce the stray inductance of the bilateral switch as much as possible, the length of the wire was reduced almost by 8 inches further from its original version.

Our concern for our application is to know the possible maximum pulse width of the device current since long current pulses mean low frequency operations for the device and SOA limitations become more strict as the frequency of operation reduces. In other words, the maximum number of 20 kHz half cycles in which the bilateral switch stays in conduction is very important. If the same switch stays in conduction for four half cycles of the 20 kHz Link, this corresponds to a 100 μsec current pulse for the device. Similarly if the device stays in conduction for 10 half cycles, it means the equivalent of a 250 μsec current pulse. Since it is not known in advance the maximum number of half cycles of the high frequency link that a bilateral switch can stay in conduction, safe operation of the IGBTs in this application heavily depends on the maximum possible pulse width along with the amplitude of the current during turn-off. Figure 5.29 can be referred to at this point to obtain an insight to the maximum possible pulse width. In this figure, the bilateral device stays in conduction for almost 20 half cycles of 20 kHz link suggesting an equivalent pulse width of about 500 μsec with a current amplitude of around 30 A. Figure 5.33 shows a magnified view of turn-off after approximately 20 half cycles of conduction. The second trace from the top shows the unilateral device (IGBT) voltage stress. After turn-off no voltage spikes of dramatic size due to stray inductance are observed. If the device current (last figure from the top in Fig. 5.33) is compared with the device voltage (second figure from the top in Fig. 5.33) and to the SOA limitations of IGBT in Table 3.5, it becomes clear that safe operation of the IGBT as unilateral device can be obtained for all practical operating conditions..

### 3.2.5 Snubber Circuits for Old and New Power Circuits

The value of the snubber capacitor can be chosen depending on the maximum peak value of the low frequency side current and the turn-on and turn-off times of the switches utilized in the bilateral switch configuration. As mentioned earlier, the bilateral switch configuration of Fig 3.5.c and the devices MJ10016 (two-stage bipolar power darlingtons) were used in the power circuit of the earlier 3 kVA system. In this case the maximum

device current that achievable with the available general purpose base drive units (capable of supplying 1 A base current) was 20 A. This current was basically the maximum peak value of the low frequency side current. Before the turn-off times were improved by using Baker Clamps, the turn-off time was between 7 to 9 μsec. Since variable turn-off times will impose variable voltage spikes, the worst possible case (earliest turn-off case) was considered in the selection of the snubber capacitors. If 20 A is the maximum assumed peak value of the low frequency side current and the 7 μsec is taken as the maximum period that both bilateral devices stay off together, and the maximum permitted voltage spike during this period is selected to be 300 V, then the snubber capacitor which must be placed across each individual bilateral device can be calculated as

$$C_S = \frac{i_C\, dt}{dV} = \frac{(20A/2) \times 7\ \mu sec}{300\ V} = 0.2333\ \mu F$$

Here it is assumed that the low frequency side current is shared by two snubber capacitors. Snubber capacitors were placed across the bilateral devices as shown in Fig 3.20 for the first generation 3 kVA system configuration. After the turn-off times were improved by using Baker Clamp Circuits, the potential open circuit interval was reduced to around 2 μsec. Thus, with a reduced turn-off time, the size of the snubber capacitor can also be reduced. Assuming that early turn-off causes both bilateral device in one branch of the bridge to stay off for a maximum of 1 μsec in this case, the size of the snubber capacitor reduces to $C_S$=0.0333 μF for the same maximum current and voltage spike considered in the calculation of above snubber capacitor. Since the energy stored in the snubber capacitor is dissipated as switching losses in the incoming devices when they turn-on. Therefore, it is clearly advantageous to keep the voltage spikes down to reduce the switching losses.

In the case of the second generation 10 kVA system, the bridge circuit of Fig. 3.5.d was selected as the new bilateral switch configuration and 1000 V-75 A IGBTs switching faster than 1 μsec were used. Hence, the snubber capacitors in the new power circuit of 3Ø-PDMC Bridge were rated according to the current that these IGBTs will carry and the turn-off time of these devices. As a first step, the snubber capacitors were placed across the collector-emitters of the IGBTs in each branch of the bridge as shown in Fig. 3.21. In this system, the maximum peak value of the low frequency side current can be assumed to be around 50 A. If the maximum time duration that both devices in one branch of the bridge remain off is assumed to be 0.5 μsec and if the maximum spike allowed at the end of this period is chosen to be 300 V, then the snubber capacitor in this case is calculated to

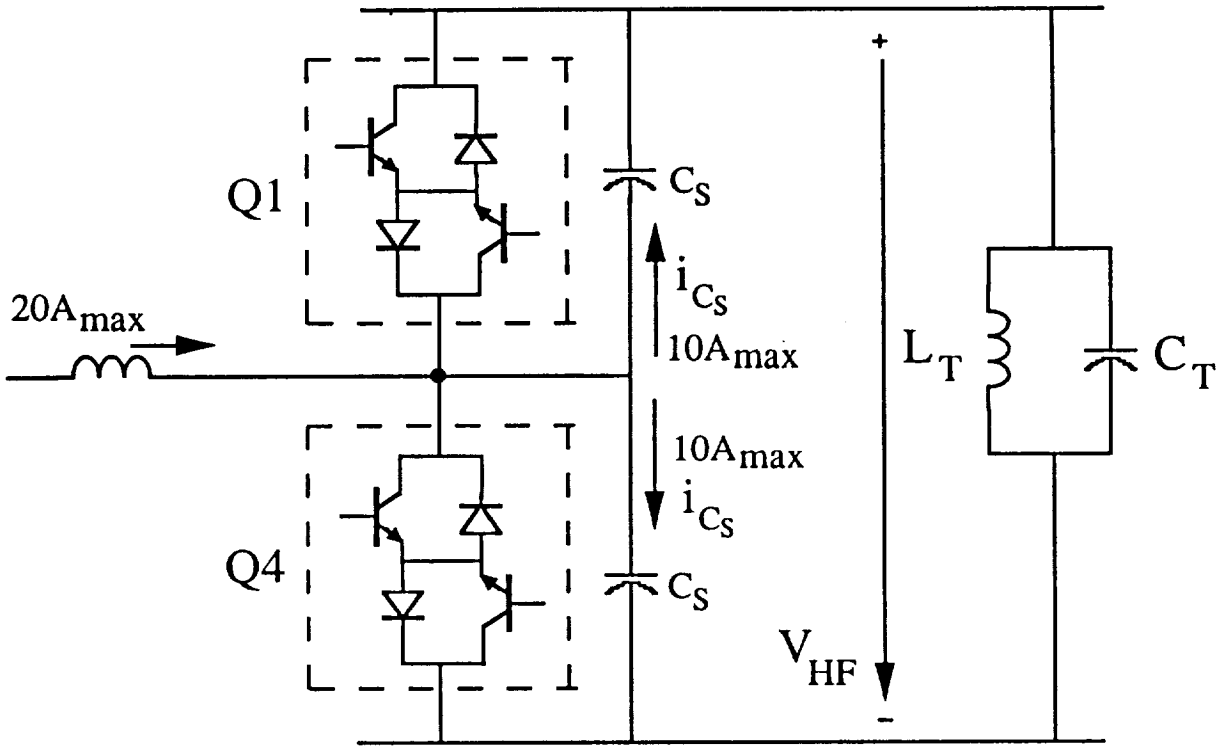



Fig. 3.20. Snubber Circuit Consideration for the Bilateral Switch Configured from MJ10016 Two-Stage Power Darlingtons with Configuration in Fig. 3.5.c and Utilized in the PDMC Structure as Above.

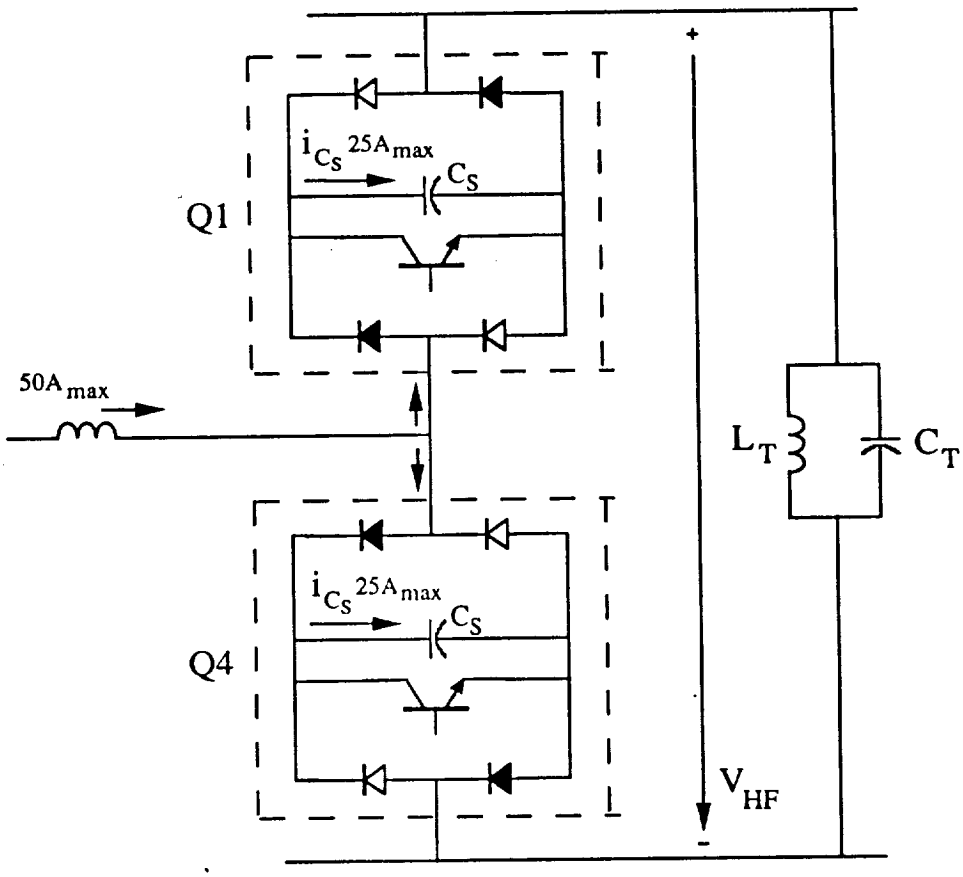



Fig. 3.21. Snubber Circuit Consideration for the Bilateral Switch Configured from an IGBT and a Diode Bridge Utilized in the PDMC Structure as above (Snubber Capacitors are Placed Across the Collector-Emitter of IGBTs).

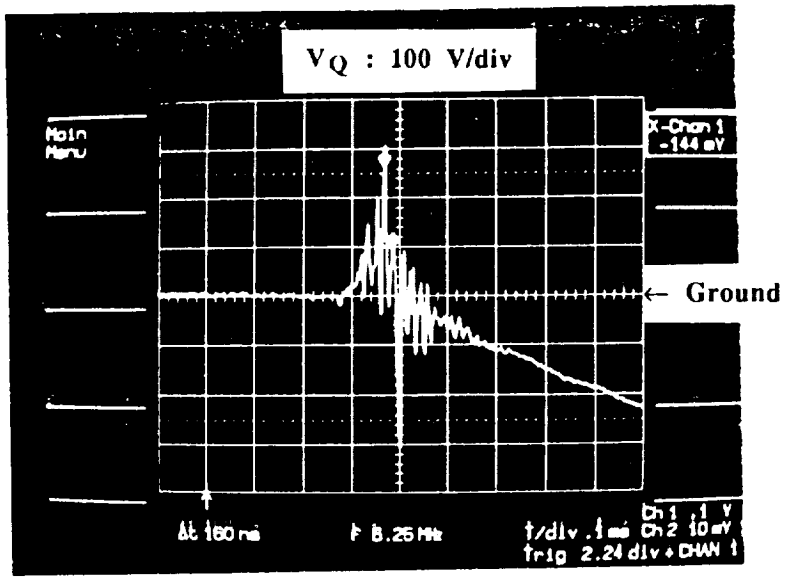
be only $C_S$=0.08333 μF. The location of the snubber capacitors shown in Fig 3.21, however, caused very high frequency oscillations in the bilateral device voltages during the switching instants. This behavior can be observed from Figs. 3.22.a and b. This high frequency ringing was sufficiently sever to affect the operation of the entire system by inducing voltage spikes into the control board signals. Misinformation was mixed into the encoder and slip signals and prevented normal functioning of the Field Orientation Control boards.

Fortunately, when the snubber capacitors were removed from across the collector-emitter of the device and placed across the entire bilateral device as shown in Fig. 3.23 the amplitudes of the very high frequency ringing was greatly reduced. Resulting samples from the bilateral device voltages after the change of location of the snubber capacitors are given in Figs. 3.24.a and b. These wave forms can be compared to those in Figs. 3.22.a and b so that the difference before and after the change can be appreciated. This dramatic reduction in very high frequency ringing in the bilateral device voltage also removed the problems related to the malfunctioning of the system control boards.

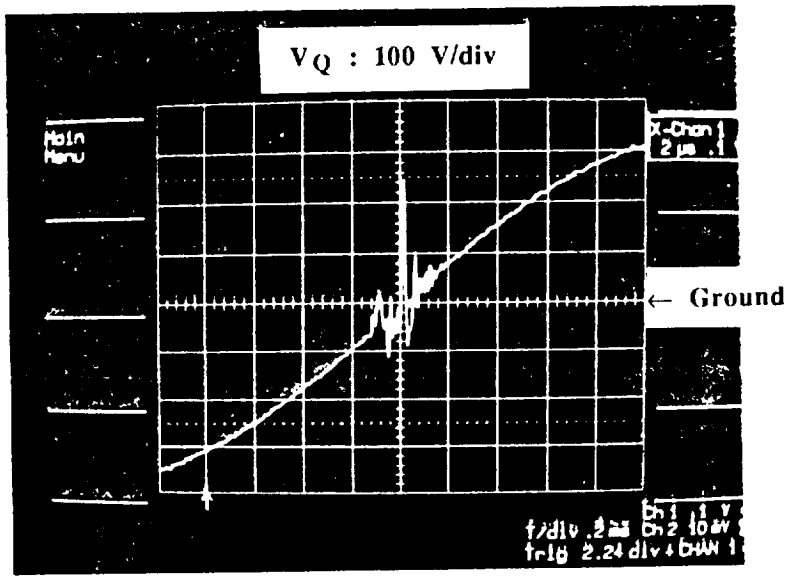
## 3.3. Source Side Line Filter Inductor Considerations

The line filter inductances used between the 3Ø-60 Hz utility grid and the line side 3Ø-PDM converter bridge, shown in Fig 3.2, are utilized mainly to limit the rate of the current change within the switching periods. The inductors used in the earlier investigation were rated for 15 Arms at 60 Hz operation with a ripple current 6 A peak to peak allowed. The inductance of these inductors were 1.5 mH per phase. As the power rating of the 3Ø to 3Ø power converter system increases, the need for line filter inductors with high current rating also rises. For the increased power range considered, inductors had to be rated approximately 35 Arms. Magnetic-core inductors were first used in the experimental system, each of them having three different taps for three different inductor values. Information concerning each of these individual inductors are given in Table 3.6.

As a first step, the Tap 2 values of the three inductors were selected for the proposed line filter inductances. Later, to obtain faster system response, they were changed to their Tap 3 values at the expense of having higher peak to peak current ripple imposed on the low frequency currents. In the experimental tests, it was observed that link voltage variation plays a very important role as the power transfer level is increased. Because only average power matching on either side of the line side converter can be




(a)




(b)

Fig. 3.22. Showing Very High Frequency and Large Amplitude Ringing During Zero Voltage Switching Instants when the Snubber Capacitors are Placed Across the Collector-Emitter of the IGBTs as in Fig. 3.21; Bilateral Device Voltage: $V_Q$ : 100 V/div. Time Scale for Trace (a): 1 µsec/div. Time Scale for Trace (b): 2 µsec/div.

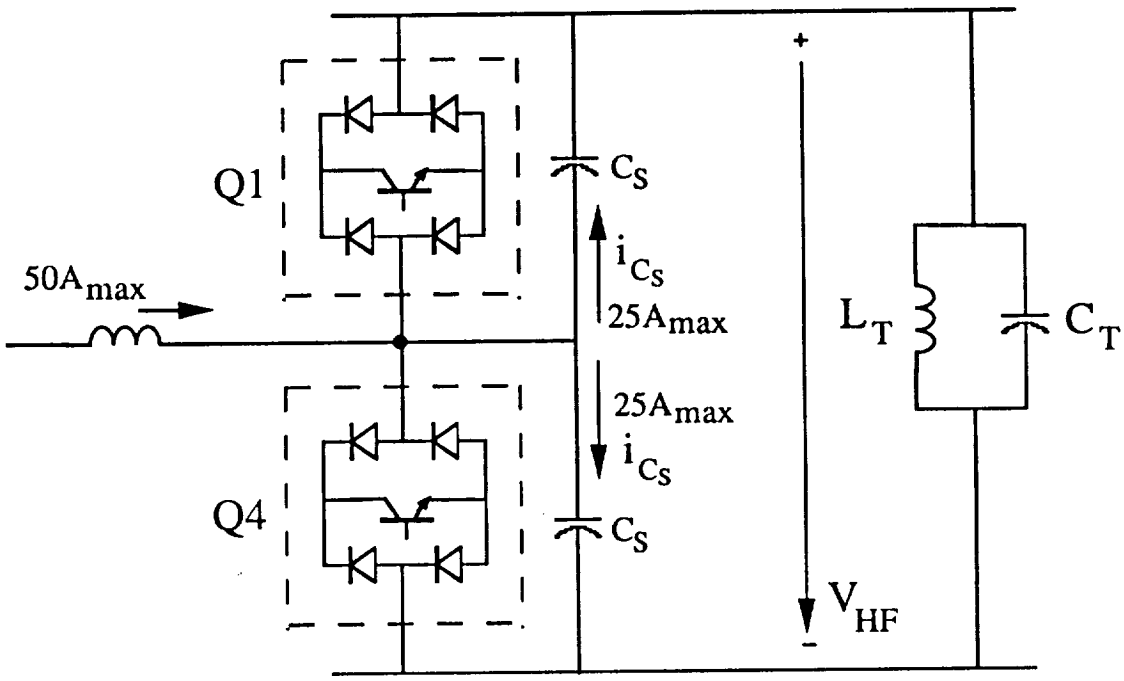
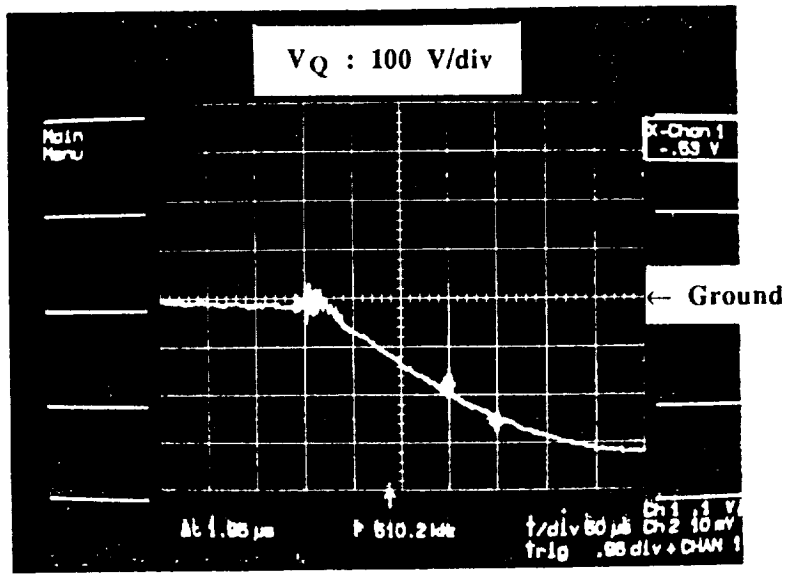
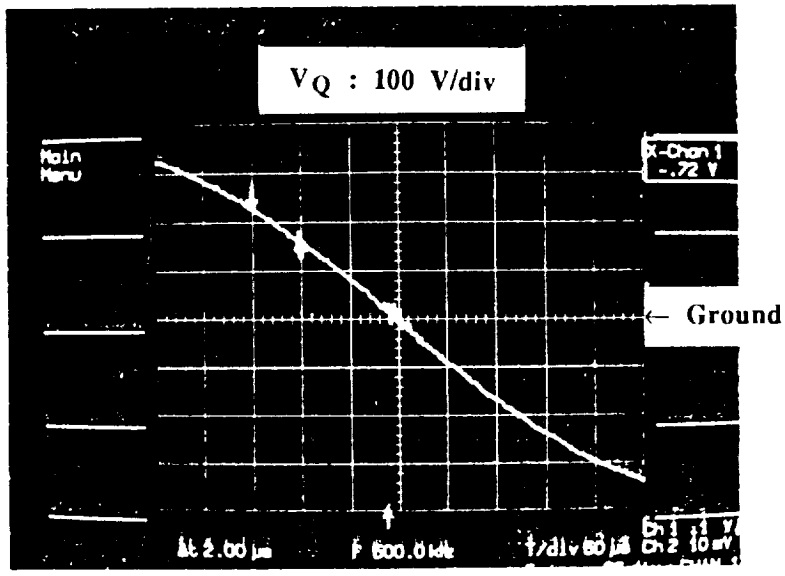



Fig. 3.23. Snubber Circuit Consideration for the Bilateral Switch Configured from an IGBT and a Diode Bridge Utilized in the PDMC Structure as Above (Snubber Capacitors are Placed Across the Bilateral Devices Themselves).




(a)




(b)

Fig. 3.24. Reduced Ringing During Zero Voltage Switching Instants When the Snubber Capacitors are Placed Across the Bilateral Devices as in Fig. 3.23. Bilateral Device Voltage: $V_Q$ : 100 V/div. Time Scale for Trace (a) and (b): 2 μsec/div.

| | | |
|---|---|---|
| Inductor $L_1$ | Tap1 (B015) | 2.850 mH, 111.0 mΩ |
| | Tap2 (B030) | 1.406 mH, 53.0 mΩ |
| | Tap3 (B050) | 922 μH, 35.2 mΩ |
| Inductor $L_2$ | Tap1 (B015) | 2.850 mH, 110.0 mΩ |
| | Tap2 (B030) | 1.400 mH, 52.3 mΩ |
| | Tap3 (B050) | 919 μH, 35.2 mΩ |
| Inductor $L_3$ | Tap1 (B015) | 2.690 mH, 115.8 mΩ |
| | Tap2 (B030) | 1.330 mH, 53.8 mΩ |
| | Tap3 (B050) | 872 μH, 35.5 mΩ |

Table 3.6. Key Specifications for the Source Side Line Filter Inductors Rated for Around 35 Arms Line Currents.

satisfied by the controller, and instantaneous power is not equal to the average, the difference between instantaneous and average power must be handled by the storage capacity of the tank circuit. For low power transfer levels, the existing tank circuit storage capacity is satisfactory. However, for high power transfer levels it is not. When the storage capacity of the tank circuit becomes unsatisfactory, the link voltage variation then becomes a problem. The PI link voltage regulator (which is, in fact, a minor regulation control loop) changes the reference currents to keep the peak link voltage at its desired reference value. However, the response of the system heavily depends on the line filter inductor values. An increased value of the source side line filter inductors reduces peak to peak ripple current imposed on the low frequency currents and improves the filtering process. However, increasing the inductance makes the response of the system slower for sudden and fast reference current changes due to link voltage variation resulting in a trade off to determine the optimum line side inductance.

## 3.4 Resonant Link Tank Circuit Inductor Design Considerations

Another alternative and better solution to the link voltage variation problem is to simply increase the energy storage capacity of the link tank circuit. For high current levels reaching up to 200 A peak flowing through the link tank circuit inductor and with 20 kHz operation, it is a critical question whether this inductor be an air-core litz wire or a

magnetic-core litz wire inductor. In most high frequency applications litz wire is used to reduce the eddy currents since losses in normal copper wire would be much higher at such frequencies. Therefore, the normal copper wire is not considered for the construction of the link tank circuit inductor. The size, weight, cost, leakage flux and losses were chosen as the major factors in the selection of this inductor.

In the first generation 3 kVA system two tank circuits were used. The inductor used in one of these tank circuits was magnetic-core litz wire which had a value of 22.5 μH and a 120 A peak current carrying capability. The other was a air-core litz wire inductor which had a value of again 22.5 μH and a 150 A peak current carrying capability. Because the current rating of the magnetic-core, litz wire inductor was underrated for 550 V peak link voltage operation at 20 kHz, it was not used in the new upgraded power level system but was replaced by an air-core litz wire inductor.

### 3.4.1 Air-Core Litz Wire Inductors

The litz wire used in the construction of the air-core inductor has an outer diameter of very close to 1 cm (0.39 inches). The inductor is constructed with 23 turns with an average core diameter of 11 cm (4.33 inches). A length of 26 feet of litz wire was required to construct the air-core inductor. A sketch of the rough shape of the inductor is shown in Fig 3.25. Cooling of the inductor was accomplished by means of a fan. The chart given in Table 3.7 is compiled from a litz wire catalog. According to this chart, the litz wire used in the construction of the inductor fits best part number NELD2660/36SPDN. As seen in the chart, this wire size has a DC resistance of $0.173*10^{-3}\Omega$/ft. Calculations showed that at 20 kHz operation, the AC resistance of this specific litz wire does not increase more than 6% beyond its DC value. Considering the AC resistance, the total resistance at 20kHz becomes $0.183\Omega*10^{-3}$/ft. This value causes a copper loss of 3.66 W/ft at a 200 A peak (142 Arms) inductor current @20kHz. Since 26 feet of wire is used, the total copper loss is 95.16 W at a total weight of 5.928 lbs (weight/length is 0.228 lbs/ft). As expected, while the cross-section area of the litz wire increases, the diameter of each turn will also increase and the required length of the wire for the same 23 turns will increase. In tandem with size, the weight and the cost will increase and the total copper losses of the air-core inductor will reduce. Even though the reduction in the total copper losses does not drop to 2/3 the previous value, the total weight of the inductor increases almost 3 times. The trade-offs are presented together with more details in Table 3.8.

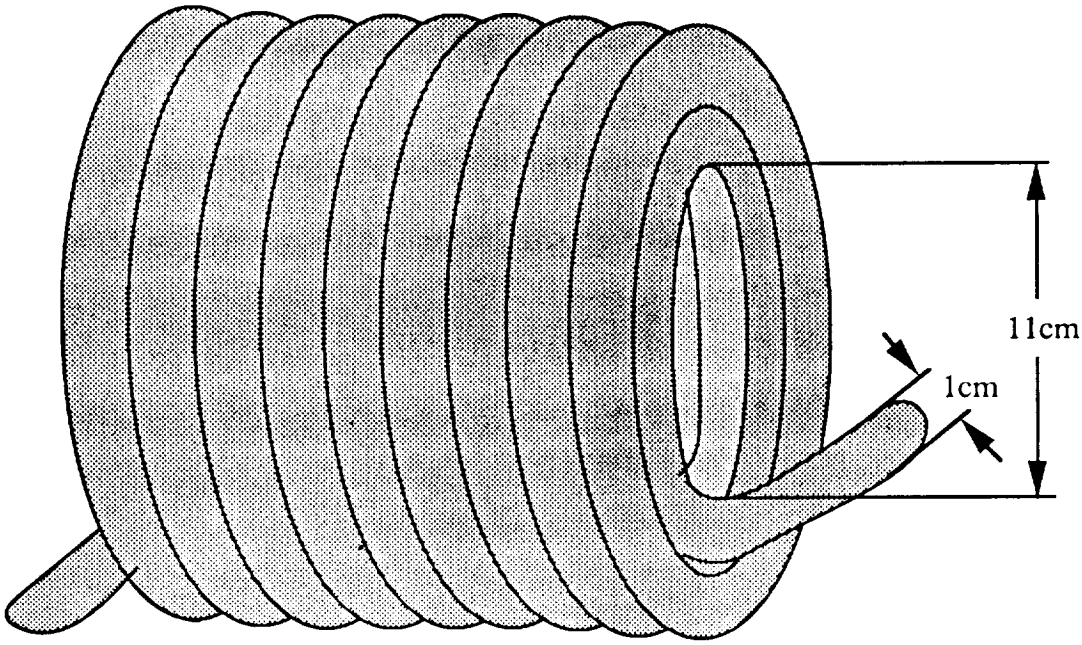



Fig. 3.25. Showing the 22.5 μH, 150 A peak Air-Core Litz Wire Resonant Tank Circuit Inductor.

| New England Part Number | Equivalent Wire Gage | Circular Mil Area | Number of Strands | Strand Wire Gage | Outer Diameter (inches) | DC resistance (Ω / ft) | Weight (lbs/ ft) |
|---|---|---|---|---|---|---|---|
| NELD2660/36SPDN | 2 | 66,500 | 2,660 | 36 | 0.370 | $0.173 * 10^{-3}$ | 0.228 |
| NELD3360/36SPSNB | 1 | 84,000 | 3,360 | 36 | 0.548 | $0.140 * 10^{-3}$ | 0.318 |
| NELD4320/36SPSNB | 1/0 | 108,000 | 4,320 | 36 | 0.655 | $0.109 * 10^{-3}$ | 0.420 |
| NELD5400/36SPSNB | 2/0 | 135,000 | 5,400 | 36 | 0.728 | $0.087 * 10^{-3}$ | 0.522 |

Table 3.7. Litz Wire Information for Resonant Tank Circuit Inductor Design Considerations for 200 A peak and 20 kHz of Opeartion.

| New England Part Number | AC resistance (Ω/ ft) @20kHz | Total AC resistance (Ω) | Cupper loss W/FT @200Apeak | Total Cupper Loss (W) @200Apeak | Total Weight (lbs) |
|---|---|---|---|---|---|
| NELD2660/36SPDN | $0.183 * 10^{-3}$ | $4.758 * 10^{-3}$/26ft | 3.66 | 95.16/26ft | 5.928 /26ft |
| NELD3360/36SPSNB | $0.148 * 10^{-3}$ | $4.144 * 10^{-3}$/28ft | 2.96 | 82.88/28ft | 8.904 /28ft |
| NELD4320/36SPSNB | $0.116 * 10^{-3}$ | $3.596 * 10^{-3}$/31ft | 2.32 | 71.92 /31ft | 13.020 /31ft |
| NELD5400/36SPSNB | $0.092 * 10^{-3}$ | $3.220 * 10^{-3}$/35ft | 1.84 | 64.40 /35ft | 18.270 /35ft |

Table 3.8. Loss and Weight Information of 22.5 μH Air-Core Litz Wire Inductor Designs for 200 Apeak and 20 kHz of Operation. (Designs with Different Gage of Litz Wires)

### 3.4.2 Magnetic-Core Litz Wire Inductors

In order to provide an alternative to the relatively high loss air core inductor the design of a magnetic core inductor was also considered. Figure 3.26 gives an idea about how magnetic-core, litz wire inductors are constructed using low loss Moly Permalloy Powder (MPP) cores. The number and size of MPP cores, their permeability and number of turns of the litz wire wound through the windows of these cores basically determines the value of inductance.

Equation 3.2.1 was used to calculate the number of cores required to design an inductor of desired value. The number of cores basically determines the total cross section of the magnetic circuit depending on the individual core cross section area.

$$x = \frac{L\ l}{\mu_0\ \mu_r\ N^2\ A} \qquad 3.2.1$$

where
- x : Number of cores required
- L : Desired value of inductor (H)
- l : Magnetic path length of the core (cm)
- $\mu_0$: Permeability of air ($4\pi 10^{-9}$ in H/cm)
- $\mu_r$ : Relative permeability of selected core
- N : Number of turns of litz wire
- A : Individual core cross sectional area ($cm^2$)

When constructing the same link inductor using low permeability MPP cores large window area cores should be used because of the large cross section area of the litz wire needed to carry about 200 Apeak current. For a core like this selected from the "Magnetics" catalog [12], the available largest possible window area MPP cores with part numbers through 55867-55869 have an inner diameter of 1.888 inches. This means that the core window can handle only 7 turns of litz wire numbered NELD3360/36SPSNB. The other physical sizes of these cores are given as: l=20 cm, A=1.77 $cm^2$. The permeability of these cores varies with the part number. The cores have relative permeabilities of 60, 26, 14 for parts numbered 55867-55869 respectively. The inductor value required is 22.5 μH. The appropriate number of cores for each permeability value must be calculated. For example, consider the MPP core which has the lowest relative permeability ($\mu_r$=14) among the 3 cores available of the same size, assuming 7 turns of litz wire. Substituting the values into Equation 3.2.1 we obtain:

Fig. 3.26. Appearance of an MPP-Core Litz Wire Resonant Tank Circuit Inductor.

$$x(\mu_r=14) = \frac{(22.5\ 10^{-6}\text{H})\ (20\text{cm})}{(4\pi 10^{-9}\frac{\text{H}}{\text{cm}})\ (14)\ (7^2)\ (1.77\text{cm}^2)} = 29.49$$

Hence, the number of cores with a relative permeability of 14 and maximum possible number of turns is very large, roughly 30. Each core being 0.638 lbs, the total weight of the 30 cores becomes 19.14 lbs. This leads to quite a costly and heavy inductor.

The maximum flux density of the core design is calculated by using Equation 3.2.2.

$$B_{max} = \frac{E_{rms}}{4.44\ N\ f\ A\ x}\ \text{(Tesla)} = \frac{E_{rms}\ 10^8}{4.44\ N\ f\ A\ x}\ \text{(Gauss)} \qquad 3.2.2$$

where $B_{max}$ : Maximum flux density (Tesla) or (Gauss)

$E_{rms}$ : Applied rms voltage to the winding or inductor (V)

f : Frequency of the applied voltage (Hz)

and the other quantities are the same as described for Equation 3.2.1.

Using this equation for the case of relative permeability of 14 yields

$$B_{max}^{(\mu r=14)} = \frac{E_{rms}\ 10^8}{4.44\ N\ f\ A\ x_{(\mu r=14)}} = \frac{(\frac{550}{\sqrt{2}})\ 10^8}{(4.44)\ (7)\ (20000)\ (1.77)\ (30)} = 1178\ \text{Gauss}$$

Referring to the curves supplied in the "Magnetics" catalog [12], an iron loss of 9W/lbs for 1178 Gauss operation at 20 kHz. Since we have 19.14 lbs weight for a total of 30 cores, this means 172 W iron loss for this particular inductor design. The total loss and weight of the inductor are not limited to the loss and weight of the cores. The seven turns of litz wire wound through the windows of the cores introduces an additional 41.44 W copper loss and 4.45 lbs. weight. Therefore, the total losses and weight of this particular inductor becomes 213.70 W and 23.59 lbs respectively. Reduction of the weight and cost of the magnetic-core inductors, clearly requires higher permeability cores. The trade-off in using higher permeability cores is an increase in iron loss against a decrease in the number of cores, weight and cost.

Repeating the same calculations for an MPP core whose relative permeability is 26 instead of 14 and part number 55868 the following results are obtained:

$x_{(\mu r=26)}$ : 16

| | |
|---|---|
| $B_{max}^{(\mu r=26)}$ | : 2209 Gauss |
| Core Weight | : 10.208 lbs |
| Core Loss | : 25 W/lbs |
| Total Core Losses | : 255 W |
| Litz Wire Weight | : 2.45 lbs |
| Copper Losses | : 22.79 W |

By repeating same procedures for the core which has a relative permeability of 60 and tabulating the results the trade-offs among the magnetic-core litz wire inductors can be compared. Comparison of Tables 3.8 and 3.9 suggests that air-core litz wire inductors always have less losses than their MPP-core litz wire counterparts, and that they are also lighter for the same loss level. The disadvantage of using an air-core litz wire inductor is clearly the large leakage flux circulating around the inductor. In other words, since there is no magnetic path for the flux, all the flux completes its path through the air. This large amount of flux circulating around the inductor could introduce unwanted voltages in the control circuitry and affect system operation.

In conclusion, the air-core litz wire inductor was selected over the MPP magnetic-core litz wire inductor for the second generation prototype. The effect of the large circulating flux of the air-core inductor on the other parts of the circuit was minimized by simply placing the inductor remotely from the power circuit.

Desired value of inductor.....: 22.5μH
Magnetic path length of induvidual core.....: 20cm
Individual core cross section area.....: 1.77cm$^2$
Litz wire used.....: NELD3360/36SPSNB
Assumed number of turns of litz wire.....: 7
Inductor operating voltage.....: 550Vpeak
Operating frequency.....: 20kHz
Permeability of air.....: 4π10$^{-9}$ H/cm

| Relative Core Permeability | Number of Cores Required | Maximum Flux Density (Gauss) | Core Loss (W/lbs) | Core Weight per piece (lbs) | Total Core Weight (lbs) | Total Core Losses (W) | Required lenght of litz wire for 7 turns (ft) | 7 turns of litz wire weight (lbs) | Total Cupper Losses (W) | Total Inductor Weight (lbs) | Total Inductor Losses (W) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 14 | 30 | 1178 | 9 | 0.638 | 19.140 | 172.26 | 14.00 | 4.45 | 41.44 | 23.590 | 213.70 |
| 26 | 16 | 2209 | 25 | 0.638 | 10.208 | 255.20 | 7.70 | 2.45 | 22.79 | 12.658 | 277.99 |
| 60 | 7 | 5049 | 100 | 0.638 | 4.466 | 446.60 | 3.36 | 1.07 | 9.95 | 5.536 | 456.55 |

Table 3.9. Loss and Weight Information of 22.5 μH MPP-Core Litz Wire Inductor Designs for 200 Apeak and 20 kHz of Operation. (Designs with Different Permeability Cores)

## 3.5 References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# Chapter 4

# Performance of First Generation High Frequency Link Induction Motor Drive

## 4.1 Introduction

In this chapter the design and performance of a complete three phase to three phase converter system and field oriented induction motor drive based upon a 3 kVA, 20 kHz ac link is described. By using same converter for the ac input side as well as the output load side, it is shown that power can be transferred in either direction. It is also shown that with the use of a current regulator both power flow on the link and the link voltage amplitude can be regulated. In addition, by suitable feedback control, the power factor at the input to the converter can be adjusted to unity. Both computer and experimental results show unity power factor operation, low harmonic current both in the input and output of the system, and bidirectional power flow capability.

With recent advances in power electronics, variable speed operation of an ac machine by use of frequency changers has now become a well established technology. The most widely used and highly developed frequency changers are the Six Step and Pulse Width Modulated (PWM) inverters which synthesize variable frequency and variable voltage ac output from a dc input. These inverters utilize a dc voltage link which is obtained by rectifying and filtering the utility source voltages.

An important factor behind the wide spread use of the dc voltage link has been the ease and effectiveness by which the energy storage function, essential for decoupling the source from load, can be implemented in a dc link. Electrolytic capacitors provide low cost, high density energy storage in the dc voltage link of a voltage source inverter. However, this type of dc link based power conversion system has several inherent limitations. One important drawback is the excessive switching loss and device stress which occur during switching intervals. As a result, the typical switching frequency in medium size 10-50 kW PWM inverters is, at best, 5 kHz. Because of the relatively low switching frequency it is difficult to realize dramatic gains in important system attributes such as faster system response, increased output frequency, improved power densities and reduction in audible and electrical noise particularly when the motor is operating at high speeds. Another difficulty worth mentioning is the presence of the rectifier bridge which is used to obtain dc from the ac voltage source. Conventional full bridge rectifiers inject

considerable low-order harmonics into the utility grid. In addition, the power flow is unidirectional, and regenerative operation of the system is possible only with considerable added expense.

In this chapter, the design and performance of a complete three phase to three phase converter system based upon a 20 kHz ac link is described. By using same converter for the ac input side as well as the output load side, power can be readily transferred in either direction. At present, this type of topology requires twelve bidirectional switches, so that it appears to be a costly system. However, with the development of new power devices such as MOS-Controlled thyristor it is anticipated that cost effective, bi-directional devices will soon become available. Hence, this type of converter holds promise as a means for obtaining unity power factor and low harmonic current on the source side of a frequency converter as well as providing fast response with high efficiency, no acoustic and markedly reduced electrical noise at the output.

## 4.2 Overall System Description

The overall first generation system is shown in Fig. 4.1 wherein two converters are connected through a 20 kHz resonant link. The link voltage is supported by a parallel resonant tank circuit. Each switch of the converter has the capability of bi-directional current flow and bi-directional voltage blocking. The source side converter is nominally tied to the utility grid through interface inductors but since these inductors are small they may not be necessary if sufficient source impedance exists. The load side converter is connected directly to an induction machine without added capacitive filtering. The current of source side converter is controlled by a link voltage regulator which regulates the link voltage by balancing the active power flow between the source and load. The current regulator at each converter regulates current in magnitude and phase. The power estimator provides an estimate of the current value of active power to the voltage regulator by calculating the average load power and the system losses based upon measurement of the current operating condition. The induction machine is controlled by a current regulated field oriented controller equipped with a speed regulation loop.

## 4.3 Link Voltage Regulation

For cost reasons the energy storage capacity of the link tank circuit must clearly be constructed to be smaller than the dc capacitor in a dc voltage link. In order to achieve a similar voltage ripple of the link would require an ac capacitor of hundreds of microfarads.

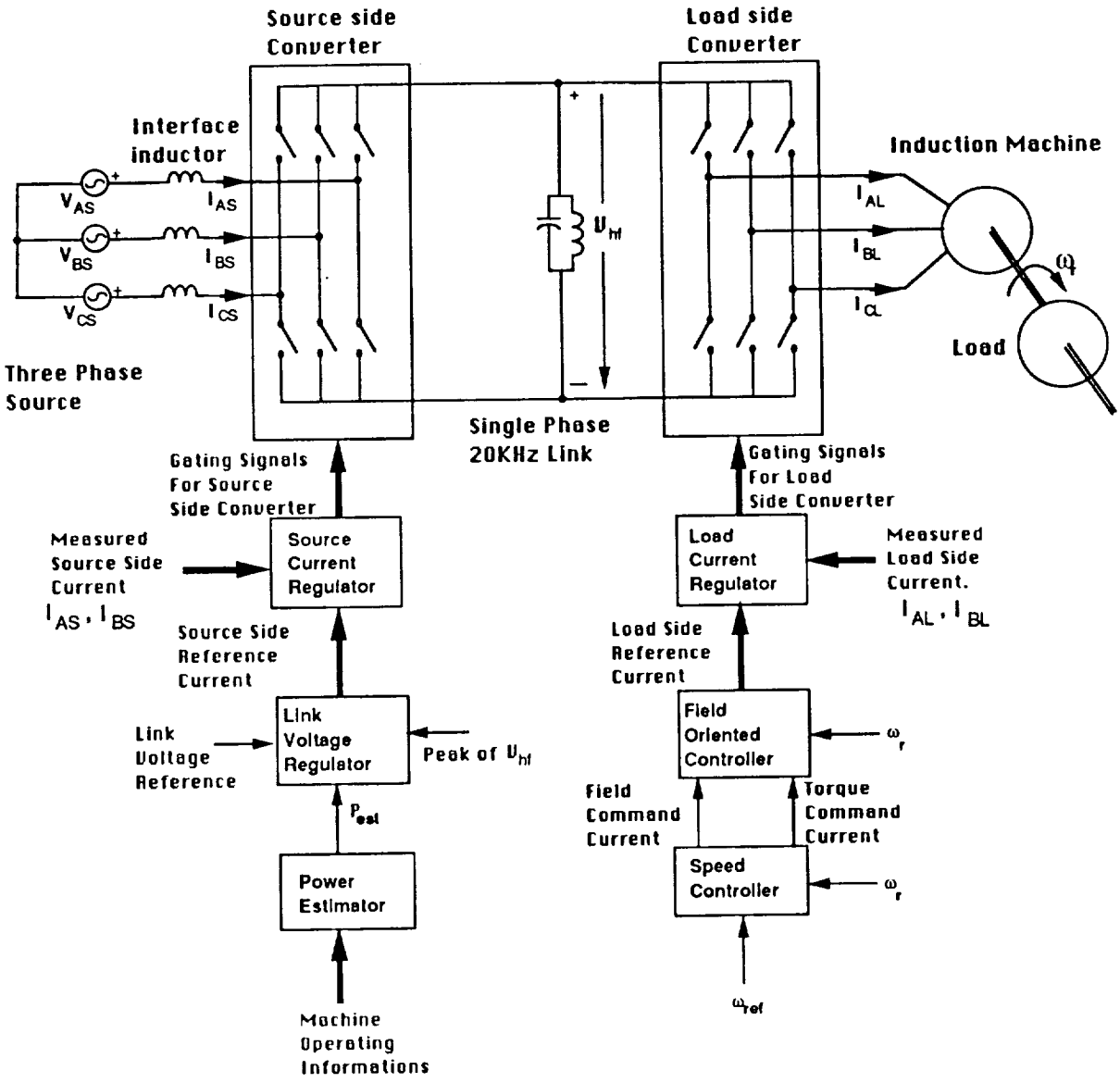



Fig. 4.1. Power Circuit and System Control Block Diagram

Hence, power balance between the load and source must be done actively. The ideal method for balancing the power flow between source and load is to measure the instantaneous power delivered to the load and system losses and deliver this exact power to the tank circuit by the source side converter. However, such an instantaneous power matching control appears to be impossible because of the difference in the source and load frequency and voltage. The best approach for handling the power balancing problem is to attempt power balance only on an average basis. The instantaneous power unbalance must then be handled by tank circuit at the cost of link voltage variations.

Fortunately, a moderate variation of link voltage is not a severe problem because the power converter connected source or load has the capability of fast regulation and the current in the source and load can be controlled as desired even in the presence of high frequency link voltage fluctuations. A small or moderate variation will, perhaps, only produce slightly more harmonic content in output current. A large variation of link voltage could, however, creates more severe problems. In particular, if the voltage is instantaneously below the minimum voltage needed to synthesize the desired reference command, the actual signal will not be able to follow the reference suggesting the possibility of control instability.

Probably the most elegant approach to measure power is measure the power by means of d,q components. That is by the equation,

$$P = \frac{3}{2}(v_d i_d + v_q i_q)$$

In this case both the voltage and current must be measured. Since the voltage waveform has wide band harmonics due to the modulation scheme elimination of the harmonics requires that the cutoff frequency of the filter be set at several hundreds of Hertz. This restriction implies several hundreds of microseconds of time delay. To suppress the link voltage variation within an acceptable level, this time delay may be critical or else the capacity of the tank circuit should be increased.

The simplest approach for obtaining average power information is to measure the power delivered to the induction machine using a low pass filter. However, with this method, time delays resulting from the low pass filter are also inevitable. Thus, during the delay time the difference in average power must be covered by the energy storage capacity of the tank circuit. This observation, in turn, implies a degradation in the link voltage regulation.

Another method to obtain average power is to estimate the power with information derived from the reference currents of the induction machine which are, in turn, available

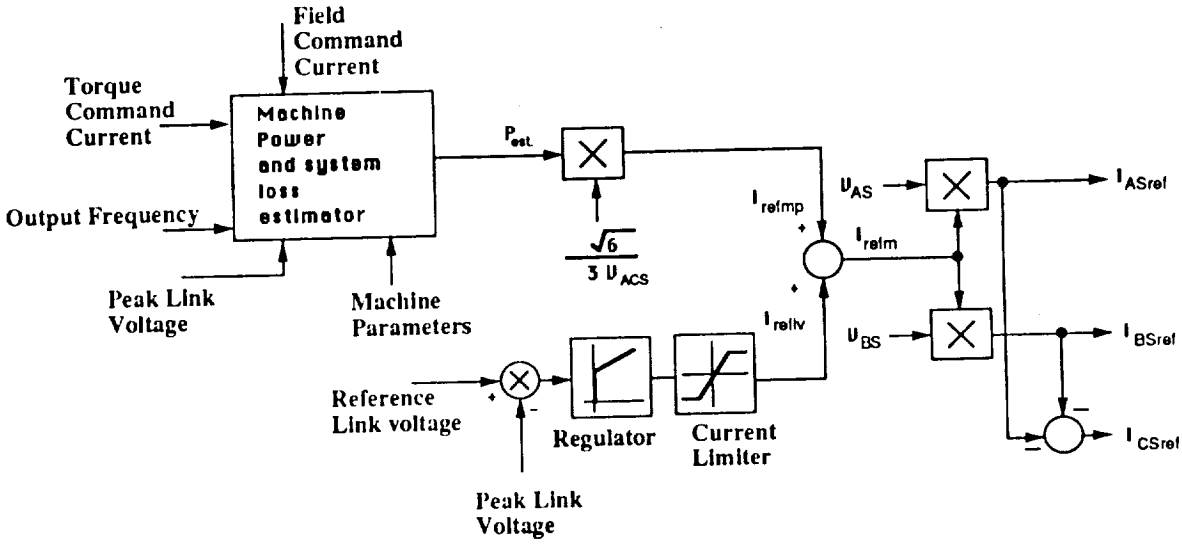
from the field oriented controller used to control the induction machine. If the current regulation is perfect and if the machine parameters do not change and are known, the average machine power can be estimated without any time delay and without any measurement. In practice, of course, there are always differences between the actual currents and their references. Moreover, the parameters of the machine change according to flux level and operating temperature so that some error between estimated power and the actual power is inevitable. However, these errors can be compensated by using a voltage regulating loop as a minor loop. More detailed descriptions concerning the voltage control loop and power calculator can be found in Refs. [1] and [2].

A block diagram of the voltage regulator and power estimator is shown in Fig. 4.2, in which the source power factor is controlled as unity. The source power factor can be controlled by shifting the phase of the reference current command so long as average power balance is maintained. Hence, the input power factor can be easily programmed to be leading or lagging as desired. In the figure, the magnitude of the reference current is the sum of the value from the power estimator and the value from the link voltage regulator. The phase of the reference current is controlled according to the source voltage.

## 4.4 Transient Behavior of Resonant Link

A computer simulation trace illustrating link voltage build-up is shown in Figs. 4.3.a and b. It can be noted that the energy from the source is pumped to the resonant tank circuit and the tank voltage gradually increases to the given reference value. After overshooting the voltage settles down to the reference value. In the simulation, the reference voltage is 500 volts and the parameters of the tank circuit are 22.5 μh, 3 μf, and 0.01 Ω. Resistance is incorporated to account for losses in the resonant tank circuit. After settling down, it can be noted that the source current is almost zero, supplying only the losses of the system.

Another simulation result illustrating the operating characteristics of the system as a whole is shown in Fig. 4.4. In this simulation it is assumed that 3 HP induction machine is operating in the steady state at 40 Hz with rated torque. It can be observed that the link voltage amplitude is reasonably well regulated. The phase A source current reveals unity power factor operation and indicates only very high frequency harmonics. The synthesized load current is nearly sinusoidal, and has virtually no harmonics less than 40 kHz. It is clear that the parameters of the resonant tank circuit should be traded off with the cost and performance of the system. A larger tank size can clearly provide better voltage regulation




$V_{AS}$ , $V_{BS}$ : Line to neutral instantaneous source voltage

$V_{ACS}$ : Line to line rms source voltage

Fig. 4.2. Block Diagram of Voltage Regulator.

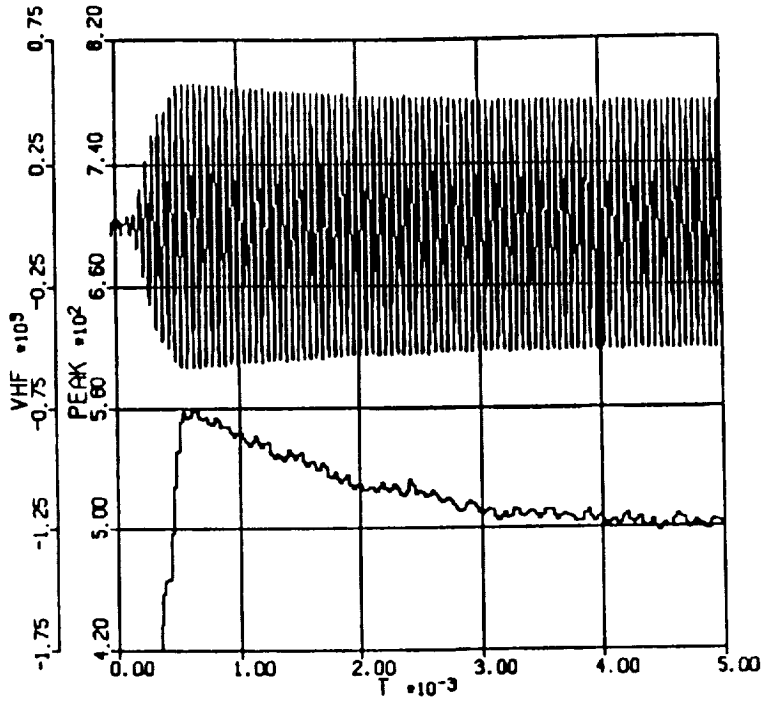



Fig. 4.3.a. Simulation Result of High Frequency Link Voltage Build-up. Top Trace: Link Voltage: $V_{HF}$ : 500 V/div. Bottom Trace: Peak of the Link Voltage: PEAK : 80 V/div. Time/div: 1msec.

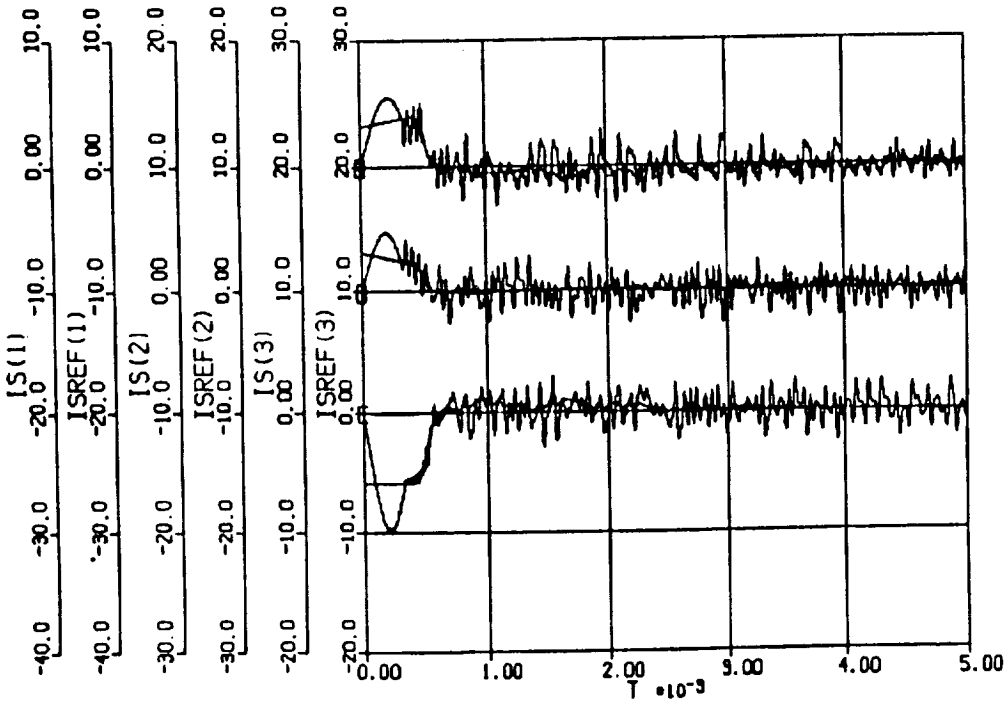



Fig. 4.3.b. Simulation Result of High Frequency Link Voltage Build-up. From the Top Respectively; Phase A Source Current and Its Reference: $I_S(1)$, $I_{SREF}(1)$: 10 A/div. Phase B Current and Its Reference: $I_S(2)$, $I_{SREF}(2)$: 10 A/div. Phase C Current and Its Reference: $I_S(3)$, $I_{SREF}(3)$: 10 A/div. Time/div: 1msec.

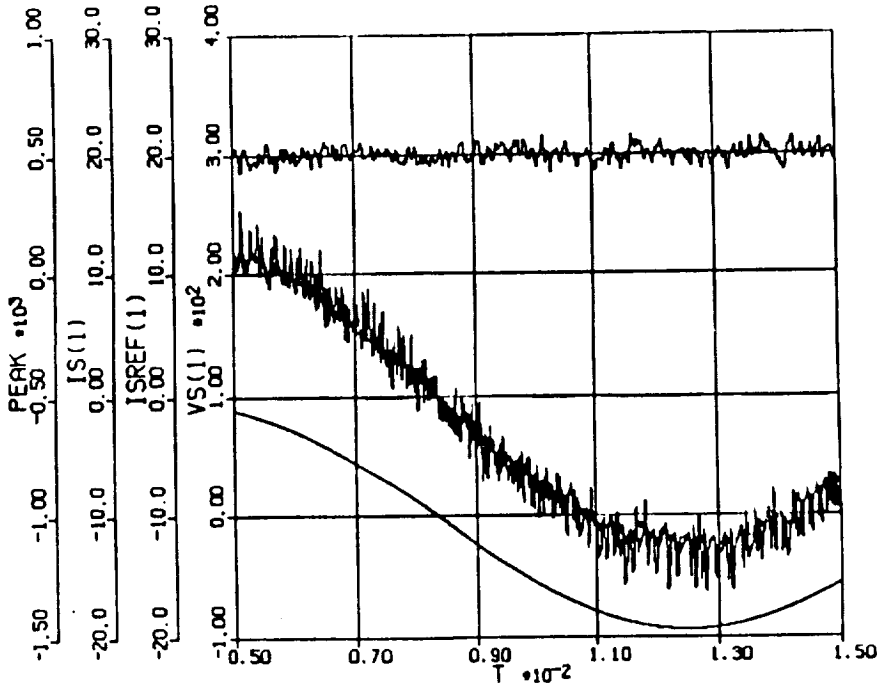



Fig. 4.4.a. Simulation Result of Operating Characteristics of the System. From the Top Respectively; Peak Link Voltage: PEAK : 500 V/div. Phase A Source Current and Its Reference: $I_S(1)$, $I_{SREF}(1)$: 10 A/div. Phase A Source Voltage: $V_S(1)$ : 100 V/div. Time/div: 2msec.

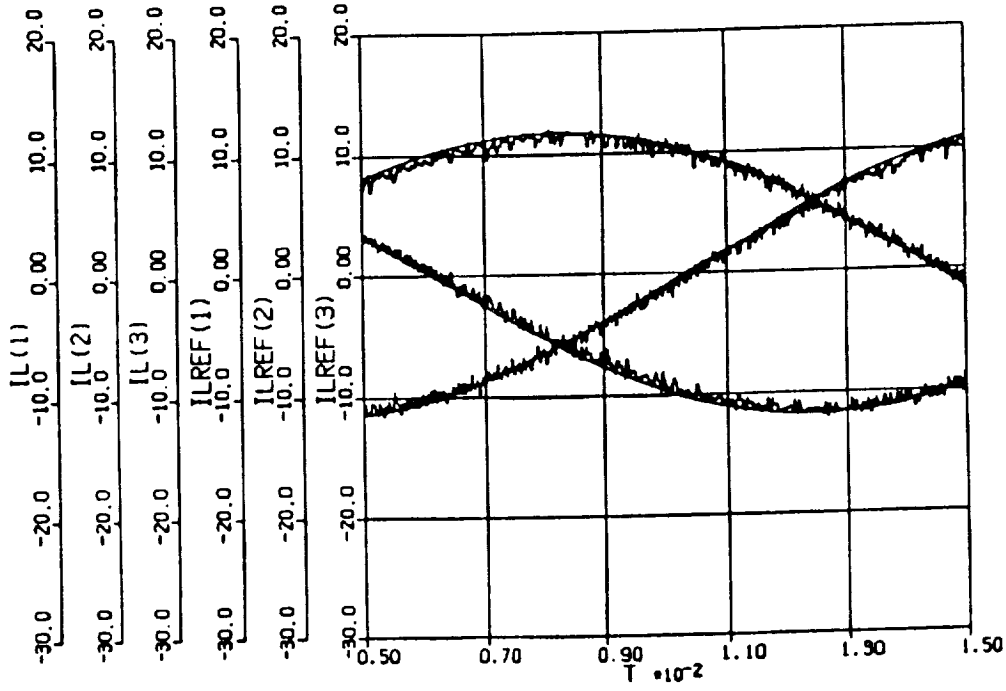



Fig. 4.4.b. Simulation Taces Showing Operating Characteristics of the System. Phase A, B and C Load Current and Corresponding References; $I_L(1)$, $I_{LREF}(1)$, $I_L(2)$, $I_{LREF}(2)$, $I_L(3)$, $I_{LREF}(3)$: 10 A/div. Time/div: 2msec.

at the expense of bulkier components and increased cost.

## 4.5 Current Regulator

In the case of a resonant link system, the current regulator most widely used is the Pulse Density Modulator or Delta modulator [3, 4, 5]. In general, both types of regulators are essentially the identical. In the above simulation the Pulse Density Modulator was used for the current regulator. Pulse density modulation performs very well in most cases except for cases of low load inductance or when synthesizing fairly high frequency output. Recently, the authors have reported a new type of current regulator, termed a *mode selection controller* [1, 2]. The mode selection controller operates on-line to select the switching pattern for the next switching mode which will minimize a given error function based upon the predicted values of voltage and current at the next switching instant. This type of current regulator can be extended to the control of a complete bidirectional double bridge system. Mode selection is very effective and easy to apply especially as a source side current regulator, where the source voltage and current can be easily measured and independent of system operating conditions. Also, by utilizing mode selection the controller can simultaneously regulate the current as well as the link voltage. In this particular case the required error function is shown to be simply the sum of the absolute error of each phase current plus that of the link voltage.

The performance of the mode selection controller as a source current regulator is shown in Fig. 4.5.a and b for the case of link voltage build up. In these traces all parameters are identical with the case of Fig. 4.3 except for the current regulator. By comparing Fig.4.3 and 5 it can be noted that the voltage overshoot is decreased and the current ripple is also attenuated. Thus, the overall performance has clearly been improved.

## 4.6 Experimental Results

The system shown in Fig. 4.1 has been constructed and thoroughly tested in the laboratory. The Speed Controller of Fig. 4.1 is a conventional proportional and integral regulator, and the indirect current regulated field orientation algorithm has been used to implement field oriented controller. The Current Regulator of both the line side and load side converters employ the Pulse Density Modulation principle. The link voltage regulator, speed controller and power estimator were implemented by analog circuits.

The inductors used on the source side are 1.5 mh, ferrite core, Litz wire inductors. In the experimental set-up two resonant tank circuits were used. The parameters of each

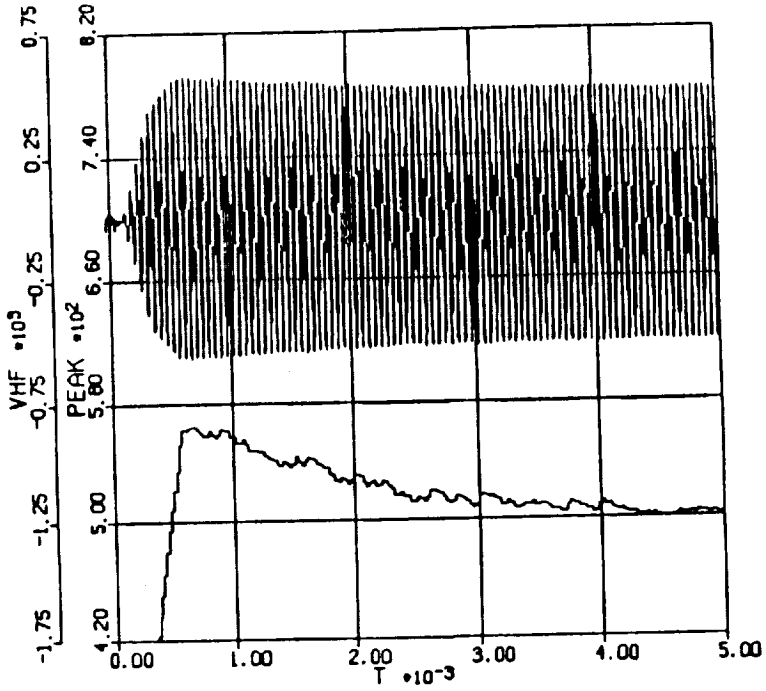



Fig. 4.5.a. Simulation Result Showing High Frequency Link Voltage Build-up with Mode Controller as Source Current Regulator. Top Trace: Link Voltage: $V_{HF}$ : 500 V/div. Bottom Trace: Peak of the Link Voltage: PEAK : 80 V/div. Time/div: 1msec.

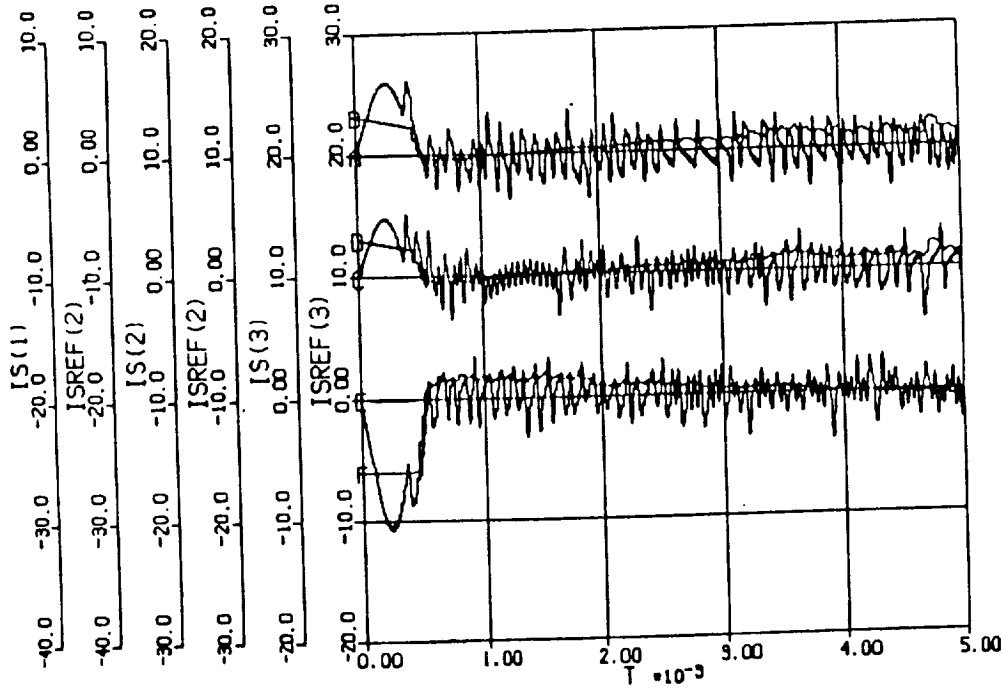



Fig. 4.5.b. Simulation Result of High Frequency Link Voltage Build-up with Mode Controller as Source Current Regulator. From the Top Respectively; Phase A Source Current and Its Reference: $I_S(1)$, $I_{SREF}(1)$: 10 A/div. Phase B Current and Its Reference: $I_S(2)$, $I_{SREF}(2)$: 10 A/div. Phase C Current and Its Reference: $I_S(3)$, $I_{SREF}(3)$: 10 A/div. Time/div: 1msec.

tank are 3 μF and 22.5 μH. Two power transistors were used as a bidirectional power switch and were connected as shown in Fig. 4.6 [6]. Typical voltage and current wave

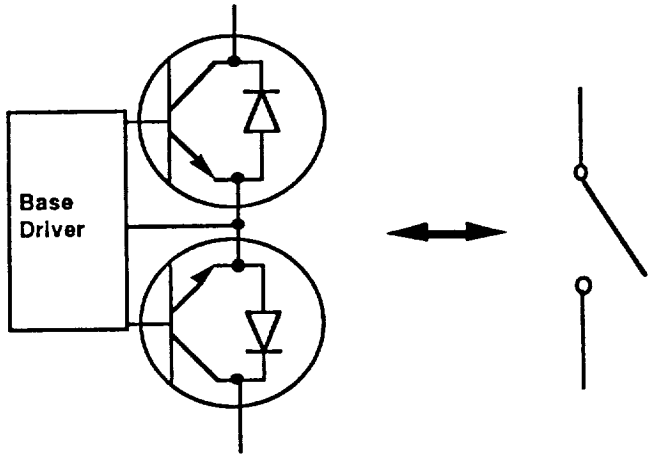



Fig. 4.6. Implementation of Bidirectional Switch.

forms across a switch during normal operation is shown in Fig. 4.7. As expected, the switching occurs only at the zero crossing points of the link voltage. As a load a 3 Hp, 4 pole, and 60 Hz induction machine was employed and the machine was mechanically coupled to a 7.5 kw dc machine to apply torque to the induction machine in the positive or negative direction.

### 4.6.1 Link Voltage Build-up

An experimental result during controlled voltage build-up is shown in Fig. 4.8. The trace of the peak of the link voltage reveals smooth and well controlled behavior. Initially, the trace of the phase A current shows a sharp increase to store energy in the inductor. After build-up the current shows a sinusoidal variation which is in phase with phase A source voltage. The difference between experimental results and simulation results is due to the difference in the loss of the modeled and actual system. In the simulation the loss component was too small compared to the real system since all of the loss components

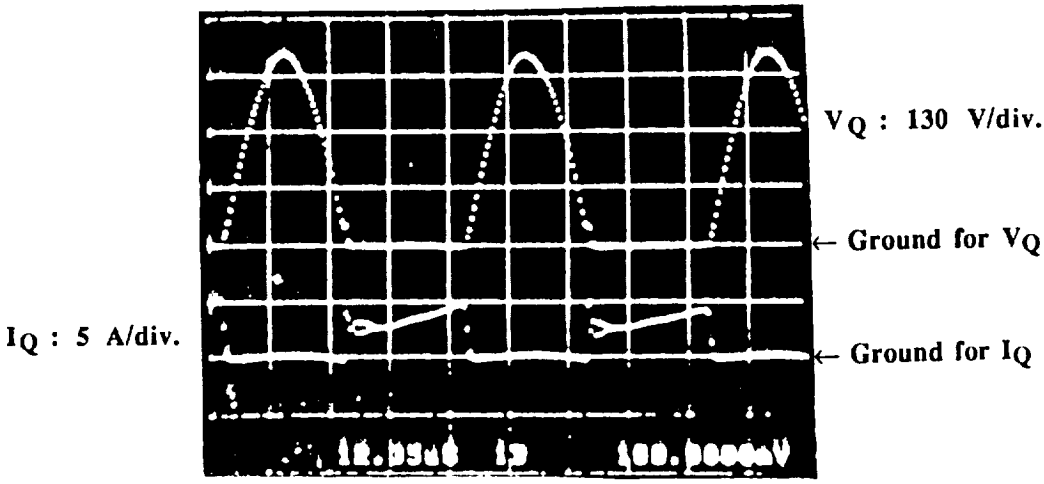



Fig. 4.7. Voltage and Current Waveform Across a Bidirectional Switch. Top Trace: Voltage Across Switch: $V_Q$ : 130 V/div. Bottom Trace: Current Across Switch: $I_Q$ : 5 A/div. Time/div: 12.35 μsec.

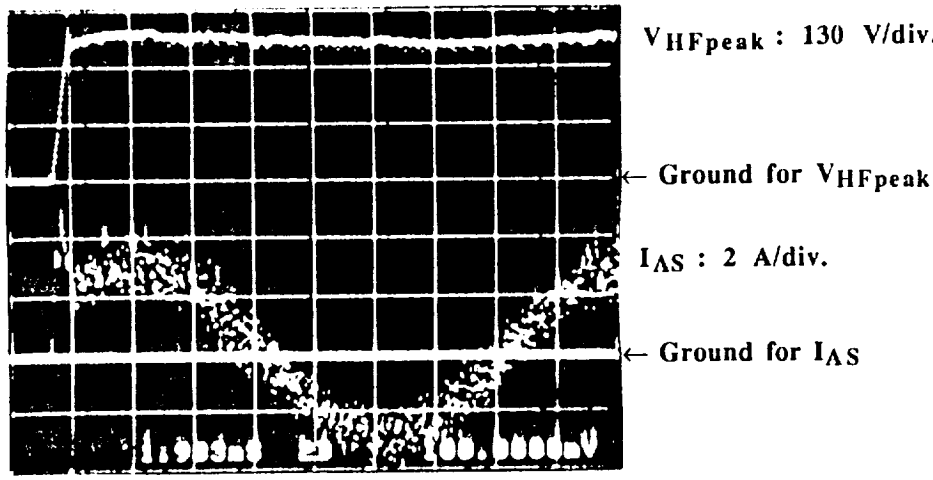



Fig. 4.8. Peak of the High Frequency Link Voltage and Phase A Source Current Waveform During Link Voltage Build-up. Top Trace: Peak of Link Voltage: $V_{HFpeak}$ : 130 Volts/div. Bottom trace: Phase A Source Current: $I_{AS}$ : 2 A/div. Time/div: 1.983 msec.

were not modelled. The real system has some losses associated with the power switch, source side inductor and resonant tank inductor.

### 4.6.2 Dynamic Performance of Field Oriented Controller

The test results illustrating performance of the field oriented controller is shown in Figs. 4.9 and 10. In Fig. 4.9.a, because of large inertia of the dc machine coupled to the induction machine, it takes several seconds to accomplish the speed change. While not clearly shown due to the large time scale, Fig. 4.9.a shows the variation of the power of the system. Before the transient the source supplies only the loss of the system including the mechanical loss. During the deceleration time the mechanical energy is converted to electrical energy. Hence, the current of the source rapidly decreases. When the machine begins to accelerate in negative direction, the current increases rapidly to supply the accelerating energy. A trace of the phase A machine current in Fig. 4.9.b clearly shows the change of the frequency as well as the phase. As shown in Fig. 4.9.b, the link voltage was well regulated during speed reversal. Figure 4.10 shows the system response of the same amount of speed change but this time without the coupled dc machine. The speed reversal was carried out within several tenths of a second. Both test results demonstrate good dynamic performance of the field oriented control incorporated with high frequency link power conversion system.

### 4.6.3 Unity Power Factor Operation

In Figs. 4.11 and 12, the steady state characteristics of the system are shown during motoring and generating operation of the induction machine. In motoring operation, shown in Fig. 4.11, the source supplies all the losses of the system and the mechanical energy of the induction machine. The trace of the phase A of the source current is in phase with phase A of the source voltage, which clearly demonstrates unity power factor operation. The trace of the peak of the link voltage demonstrates reasonable regulation. During generating operation shown in Fig. 4.12, the energy generated by the induction machine supplies all losses and the excess energy transfers to the source. Between phase-A source voltage and the corresponding current there is 180° phase difference. The phase difference means that the source takes the energy from the system with unity power factor. The link voltage regulation for generating operation is poorer than that for motoring operation because of a slight mismatch of the parameters of the power estimator.

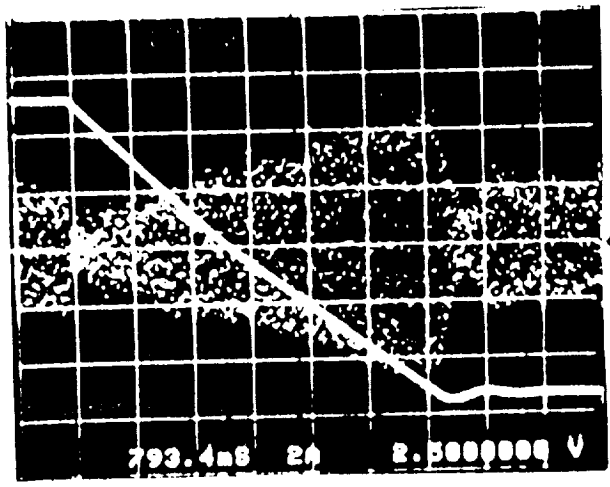



Fig. 4.9.a. Response of the Field Oriented Control Utilizing High Frequency Link Power Conversion. Top Left Trace: Mechanical Rotational Speed: n : 190 rpm/div. The Other Trace: Phase A Source Current: $I_{AS}$ : 5 A/div. Time/div: 793.4 msec.

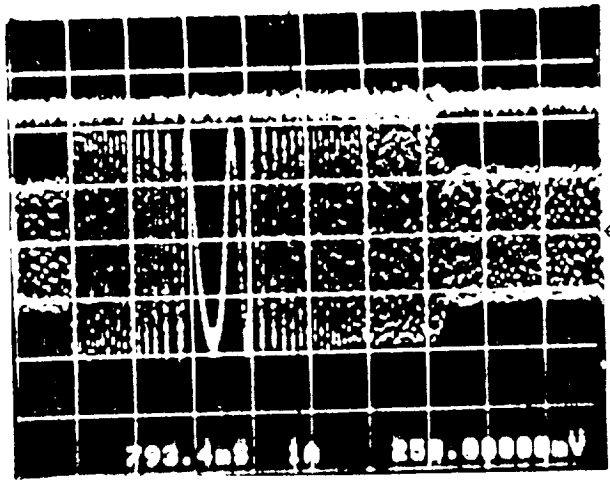



Fig. 4.9.b. Response of the Field Oriented Control with High Frequency Link Power Conversion. Top trace: Peak Value of the Link Voltage: $V_{HFpeak}$ : 130 V/div. Bottom Trace: Induction Machine Phase A Current: $I_{AL}$ : 5 A/div. Time/div: 793.4 msec.

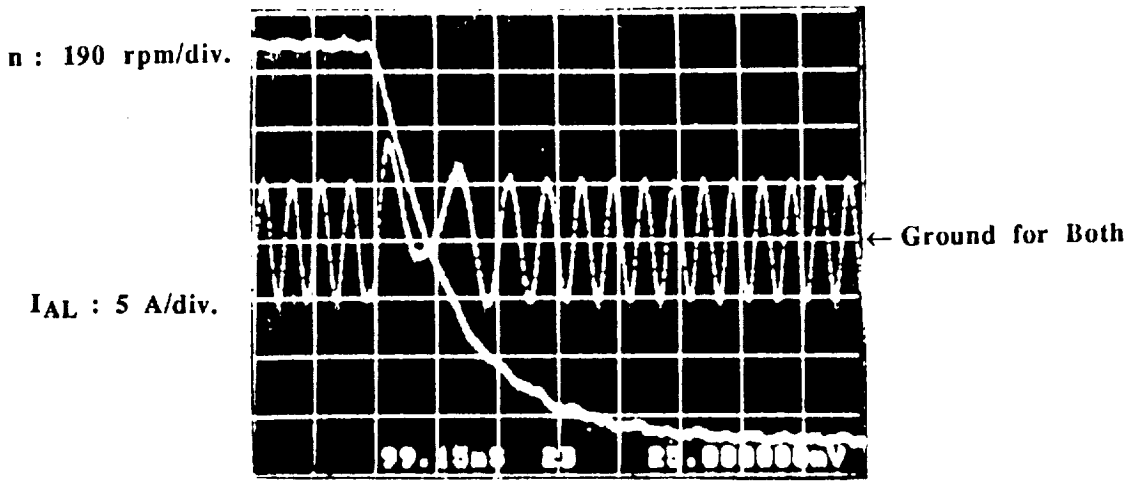



Fig. 4.10. Response of the Field Oriented Control with High Frequency Link Power Conversion without DC Machine Coupled. Top Left Trace: Mechanical Rotational Speed: n : 190 rpm/div. The Other Trace: Phase A Induction Machine Current: $I_{AL}$ : 5 A/div. Time/div: 99.15 msec.

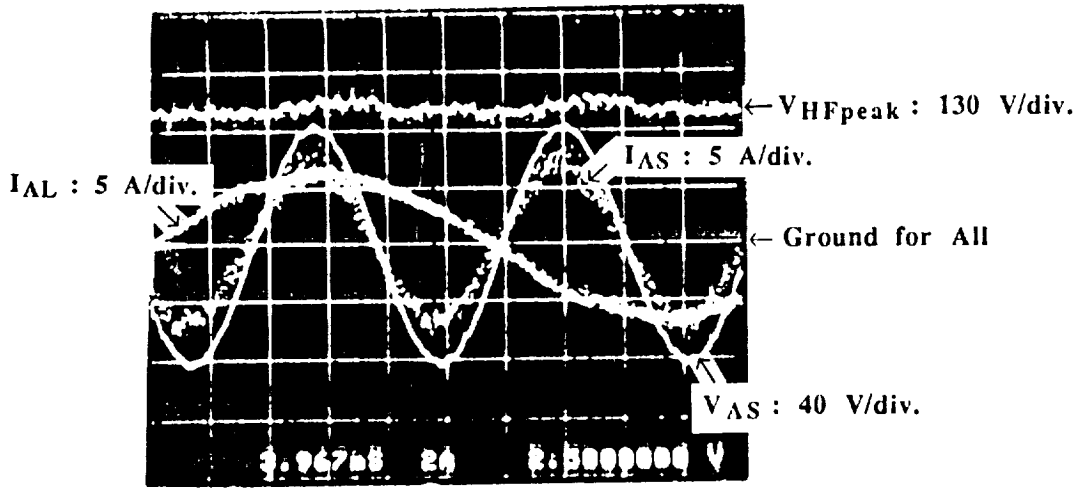



Fig. 4.11. Waveforms Showing Unity Power Factor Operation of the System During Motoring Operation. Top Trace: Peak of the Link Voltage: $V_{HFpeak}$ : 130 V/div. Bigger Amplitude and Higher Frequency Sinusoidal Waveform: Phase A Source Voltage: $V_{AS}$ : 40 V/div. Smaller Amplitude and Higher Frequency Sinusoidal Waveform: Phase A Source Current: $I_{AS}$ : 5 A/div. Lower Amplitude and Lower Frequency Sinusoidal Waveform: Phase A Induction Machine Current: $I_{AL}$ : 5 A/div. Time/div: 3.967 msec.

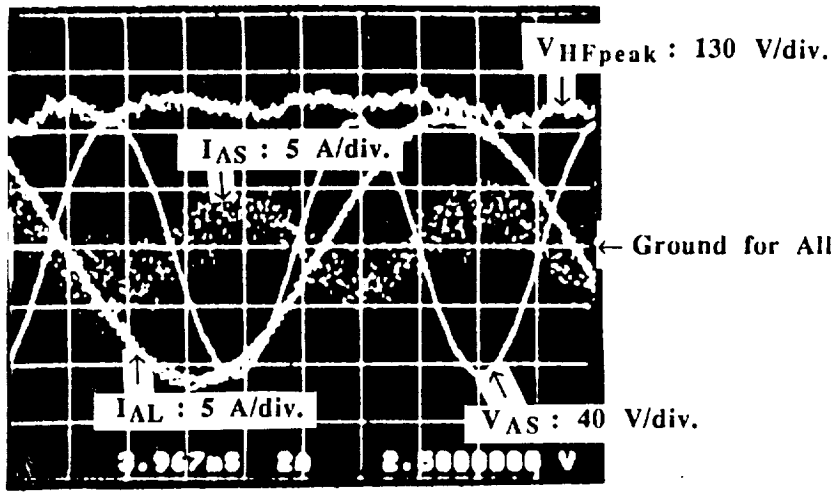



Fig. 4.12. System Traces Showing Unity Power Factor Operation of the System During Regeneration. Top Trace: Peak of the Link Voltage: $V_{HFpeak}$ : 130 V/div. Bigger Amplitude and Higher Frequency Sinusoidal Waveform: Phase A Source Voltage: $V_{AS}$ : 40 V/div. Smaller Amplitude and Higher Frequency Sinusoidal Waveform: Phase A Source Current: $I_{AS}$ : 5 A/div. Lower Amplitude and Lower Frequency Sinusoidal Waveform: Phase A Induction Machine Current: $I_{AL}$ : 5 A/div. Time/div: 3.967 msec.

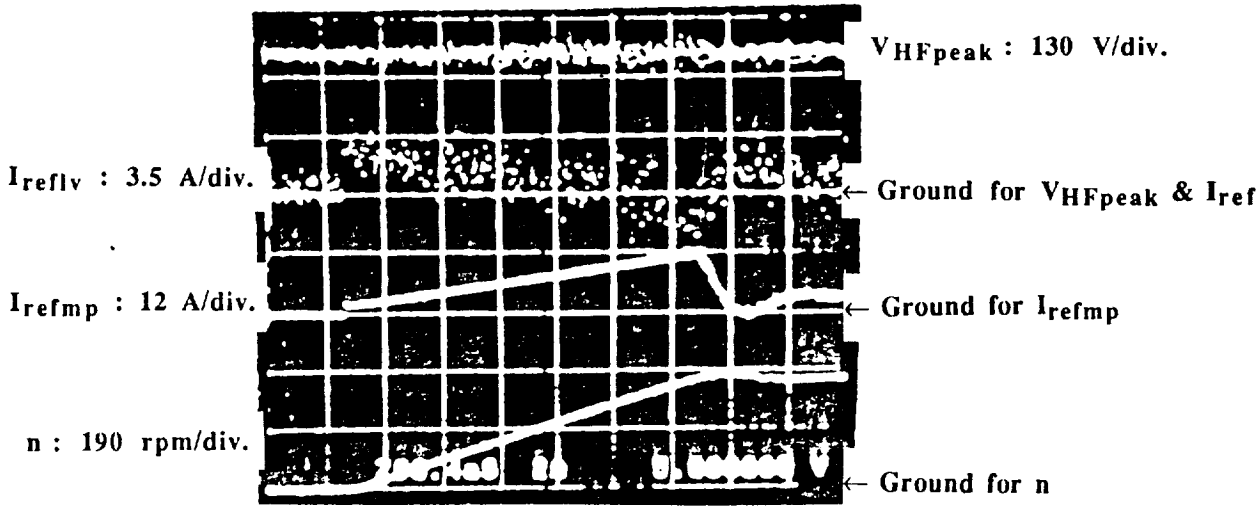



Fig. 4.13. Operation of Power Matching Controller and Voltage Regulator. From the Top Respectively; Peak Value of the Link Voltage: $V_{HFpeak}$ : 130 V/div. Magnitude of Reference Current from Voltage Regulator: $I_{reflv}$ : 3.5 A/div. Magnitude of Reference Current from Power Estimator: $I_{refmp}$ : 12 A/div. Mechanical Rotational Speed: n : 190 rpm/div. Time/div: 793.4 msec.

### 4.6.4 Power Matching Controller

As mentioned before, the high frequency link system has no great reservoir of energy so that the power balance between source and load should be actively controlled. The behavior of the power estimation controller is shown in Fig. 4.13. During the starting of the induction machine the magnitude of the reference current from estimated power ($I_{refmp}$) was gradually increased, and after settling of the speed, the magnitude decreased to a small value to supply only the losses of the system. The reference current from voltage regulator, which is a minor loop, deviates around zero. By comparing the magnitude of the current it can be seen that the major part of the magnitude of the source reference current comes from the power estimator. The test result clearly explains the operation of the voltage regulator including the power estimator shown in Fig. 4.2.

### 4.6.5 Current Regulation

The characteristics of the current regulator employing Pulse Density Modulation are shown in Fig. 4.14 and 15. In the case of the source current regulation the reference of the source current itself has some ripples to regulate link voltage and power matching control. The actual current still accurately follows its reference. The load current reference is almost a ripple free sinusoidal wave during steady state operation of the induction machine. Hence, the actual current shows almost the same trace with its reference. It should be noted that during the operation of the system there was no acoustic noise from the power conversion system because of its high switching frequency.

## 4.7 Conclusions

In this chapter a three phase to three phase power conversion topology based upon a 20 kHz single phase voltage link was demonstrated. To demonstrate hardware feasibility of the system and to verify the simulation results, an experimental system was built and tested. The simulation results and experimental results agree and exhibit very good load current regulation as well as unity power factor operation of the source side current. Also, the system was shown to have inherent bidirectional power flow capability. The system could prove to be a viable alternative to conventional dc link systems in near future when bidirectional power semiconductor switches become readily available.

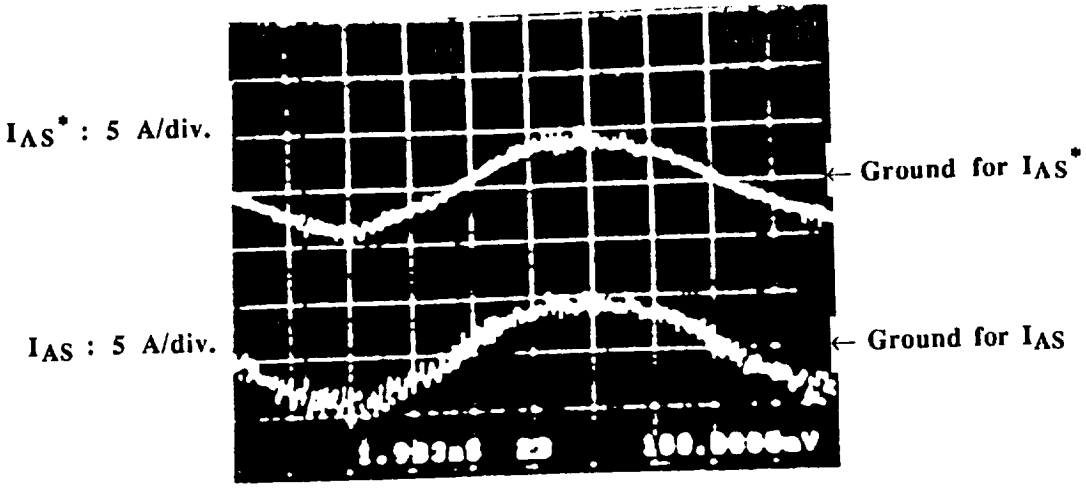



Fig. 4.14. System Performance Showing Source Side Current Regulation. Top Trace: Reference of Phase A Source Current: $I_{AS}^*$ : 5 A/div. Bottom Trace: Phase A Source Current: $I_{AS}$ : 5 A/div. Time/div: 1.983 msec.

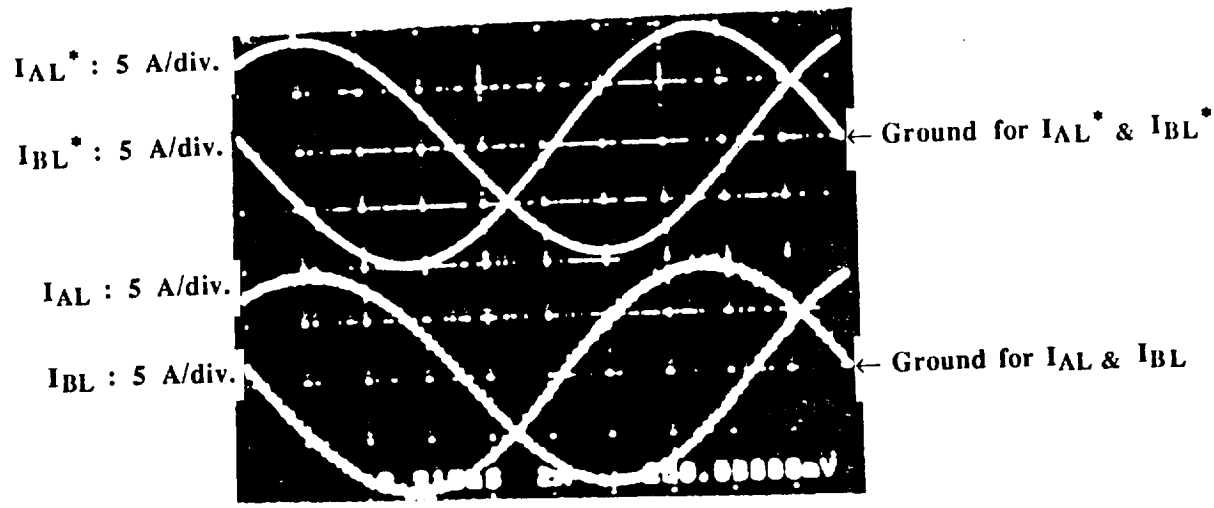



Fig. 4.15. Oscilloscope Traces Showing Load Side Current Regulation. Top Trace: References for Phase A and B Induction Machine Currents: $I_{AL}^*$ & $I_{BL}^*$ : 5 A/div. Bottom Trace: Phase A and B Induction Machine Current: $I_{AL}$ & $I_{BL}$ : 5 A/div. Time/div: 9.915 msec.

## 4.8 References

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2. S.K. Sul and T.A. Lipo,"Field Oriented Control of an Induction Machine in a High Frequency Link Power System", IEEE Power Electronics Specialists Conference, Kyoto, Japan, April 1988.

3. P.K. Sood and T.A. Lipo,"Power Conversion Distribution System Using a Resonant High-Frequency AC Link", IEEE Trans. Ind. Appl. Soc.., October 1986, pp. 533-541.

4. P.K. Sood, "High Frequency Link Power Conversion System", Ph.D. Thesis, University of Wisconsin-Madison, January 1987.

5. M. Kheraluwala and D.M. Divan,"Delta Modulation Strategies for Resonant Link Inverters", IEEE Power Electronics Specialists Conference, Blacksburg, Virginia, pp. 271-278, June 1987.

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# Chapter 5

# Performance of 7.5 kW Second Generation System Operating as a Dynamometer

## 5.1 Introduction

This chapter describes the work completed on the testing of the 10 hp (7.5 kW) squirrel cage dynamometer. The name plate ratings of this induction machine are 3Ø, 300 Hz, 6 poles, 6,000 RPM, 10 hp, 230 V, 32 A as shown in Table 5.1. The machine is designed to deliver 10 hp or 7.46 kW when operated as an AC-Dynamo with power fed back to the source through the converter. Speeds up to 18,000 rpm can be achieved by use of field weakening.

## 5.2 Description of Overall Experimental System

As a final task of the overall investigation into high frequency link power conversion, a higher power version of the same system described in Chapter 4 was designed, built and tested for permanent laboratory use as a high speed dynamometer. The proposed power level of the upgraded system was selected to be 10 hp at 6000 rpm with a 3 to 1 field weakening range extending high speed operation to 18,000 rpm. The rating of the machine was chosen according to NASA specifications consistent with the speed limits imposed by the use of conventional greased bearings. The source side voltage and current and the peak link voltage values was chosen to enable an operation over this power range with readily available solid state switches. To synthesize 230 V rms line to line voltage from a parallel resonant high frequency AC Link, the peak link voltage according to the Equation 3.1.2 was rated at 511 V. This rating allows a maximum of 325.3 V line to line peak low frequency synthesized voltage which is equivalent to maximum of 230 V line to line rms.

As the first experimental task of this portion of the project, a series of tests were performed to first determine the parameters of the 10 hp, 6000 rpm induction machine. The resulting parameters are listed in Table 5.1 in summarized form.

In order to perform the tests, a DC-Dynamometer operating in the motoring mode was used to load the induction machine. The name plate rating of this machine is given in

**Name Plate Ratings of Induction Machine:**

3 phase (3Ø), 10 hp (7.46 kW), 230 V, 32 A, 300 Hz, 6 poles

6000 rpm @ no load, 5957 rpm @ rated torque

Δ-Connected Stator Winding, Squirrel Cage Rotor

Designed to Operate at 900 Hz (18,000 rpm) with Field Weakening

**Equivalent Circuit Parameters:**

$r_{1dc}$ =0.195 Ω

$r_2'$ =0.10482 Ω

$r_M$ =240 Ω @ 300 Hz and 40.411 Ω @ 60 Hz

$L_{l1} = L_{2l}'$=0.6796 mH with Measurement at 60 Hz

$L_M$ =11.149 mH at 300 Hz and 10.888 mH at 60 Hz

$L_M$ =11.149 mH at 300 Hz and 10.888 mH at 60 Hz

$S_R$ =0.0072 @ 230 $V_{ll}$/300 Hz V/f Ratio and Rated Torque Operation

$S_R$ =0.0358 @ 46 $V_{ll}$/60 Hz V/f Ratio and Rated Torque Operation

**Per Unit Equivalent Circuit Parameters:**

$r_{1dc}$=0.015664 pu

$r_2'$ =0.00842 pu

$r_M$ =19.278 pu @ 300 Hz and 3.246 pu @ 60 Hz

$X_{l1}=X_{l2}'$=0.1029 pu @ 300 Hz and 0.02058 pu @ 60 Hz

$X_M$=1.6848 pu @ 300 Hz and 0.32973 pu @ 60 Hz

**Per Unit Base Quantities:**

$V_{BASE}$=230 V

$I_{BASE}=32A/\sqrt{3}$=18.475 A

$Z_{BASE}=V_{BASE}/I_{BASE}$=12.449 Ω

Table 5.1. Name Plate Ratings and Equivalent Circuit Parameters of Special Purpose Squirrel Cage Induction Machine Used as High Speed Dynamometer

Table 5.2. The rated speed of this DC-Dynamometer is specified as 4000 rpm. This top speed was one of the highest speed range DC-Dynamometers available in the lab capable of loading the induction machine to a power close to the induction machine power rating. Since the rated speed of the induction machine is 6000 rpm there was, unfortunately, no machine available in our lab that could operate at these speed ranges and load/drive this induction machine at its maximum power point.

**Name Plate Ratings of DC Machine:**

Armature Voltage: 250/230 Volts

Armature Current: 22 Amps

Speed: 1250/4000 rpm

Power: Absorbs 8 hp

Power: Delivers 5 hp

Table 5.2. Name Plate Ratings of DC-Dynamometer Coupled to the Induction Machine for Purpose of Testing

An Indirect Field Orientation Controller (FOC) which was previously designed in the WisPERC laboratory [1,2] was adopted to control the induction machine. The operating principle of Field Oriented Control utilizing a PDM (pulse density modulated) converter is explained in reference [3]. Both the source and the load side 3Ø low frequency portions of the PDM Converters are current regulated and link voltage regulation is used as a minor loop on the source side converter. A detailed description of operating principle of current regulation scheme for the 3Ø PDM Converters has been given in Section 3.1. The overall operating principle of this system is explained in Chapter 4.

### 5.2.1 Description of the New Power Circuit

A block diagram of the power circuit of the overall system is shown in Fig. 5.1. Initially, a 3Ø Auto Transformer was used to be able to initiate system starts at low voltage levels when necessary. Later, the output of this 3Ø Auto Transformer was set to 178 V line to line rms for normal operation. This is value corresponds to a 511 V peak link voltage with zero source current references while the load side PDM converter is not in

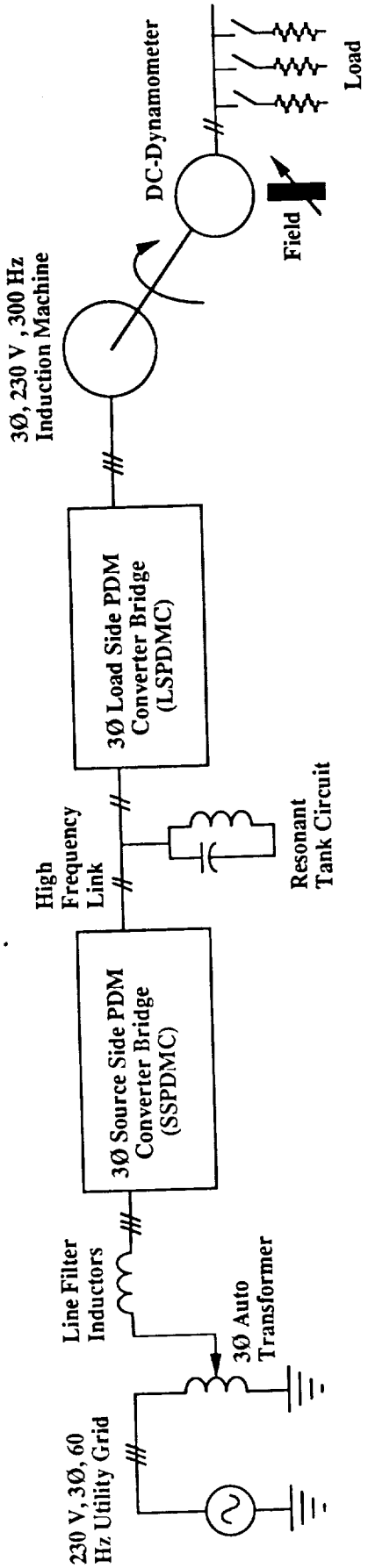


Fig. 5.1. Power Circuit Block Diagram of Overall System.

operation. For the initial measurements only one of the two tank circuits of the first generation converter was used. It is apparent that there is a need to increase the number of tank circuits to increase the energy storage capacity for high power level operation. The size of the link tank circuit was later changed to realize the full rating of the dyno.

A detailed power circuit diagram of this 3Ø to 3Ø upgraded power conversion system operating via a parallel resonant high frequency link is shown in Figs. 5.2.a and b. Components used in the power circuit are labelled on the figure and their characteristic values are given in Table 5.3.a and b. The current and voltage conventions used in the measurements are also shown in the figure.

| Component | Circuit Symbol | Key Specifications and Comments |
|---|---|---|
| Insulated Gate Bipolar Transistors (IGBTs) | $T1_S$ - $T6_S$<br>$T1_L$ - $T6_L$ | $I_C$=75 A, $V_{CES}$=1000 V, $V_{CEsat}$=3 V<br>AEG Part #: F75A1000K |
| Fast Recovery Power Diodes | $D1_S$ - $D23_S$ (odds)<br>$D2_S$ - $D24_S$ (evens)<br>$D1_L$ - $D23_L$ (odds)<br>$D2_L$ - $D24_L$ (evens) | $I_{FAVM}$=72 A,$I_{FRMS}$=160 A,$V_{RRM}$=1200V<br>$V_F$=1.7 V @ $I_F$=150 A<br>BBC Part # for odds : DSDI71-12A<br>BBC Part # for evens: DSD71-12A |
| Snubber Capacitors | $C_{S1}$ - $C_{S6}$<br>$C_{L1}$ - $C_{L6}$ | 0.094 µF, 1200 $V_{DC}$<br>Two 0.047 µF, 1200 VDC in parallel |
| Tank Circuit Inductor | $L_T$ | 22.5 µH, 150 Apeak, Air-core-Litz wire,<br>Air cooled for 200 A peak inductor current |
| Tank Circuit Capacitor | $C_T$ | 3.0 µF, 1000 V pk, 161 Apeak<br>Three GE97F8522FC in parallel |
| Equivalent Impedance of the Tank Circuit | $Z_T=\sqrt{L_T/C_T}$ | 2.7386Ω |

Table 5.3.a. Component Values Used in the Upgraded 3Ø to 3Ø Power Conversion System, Circuit Symbols and Key Specifications.

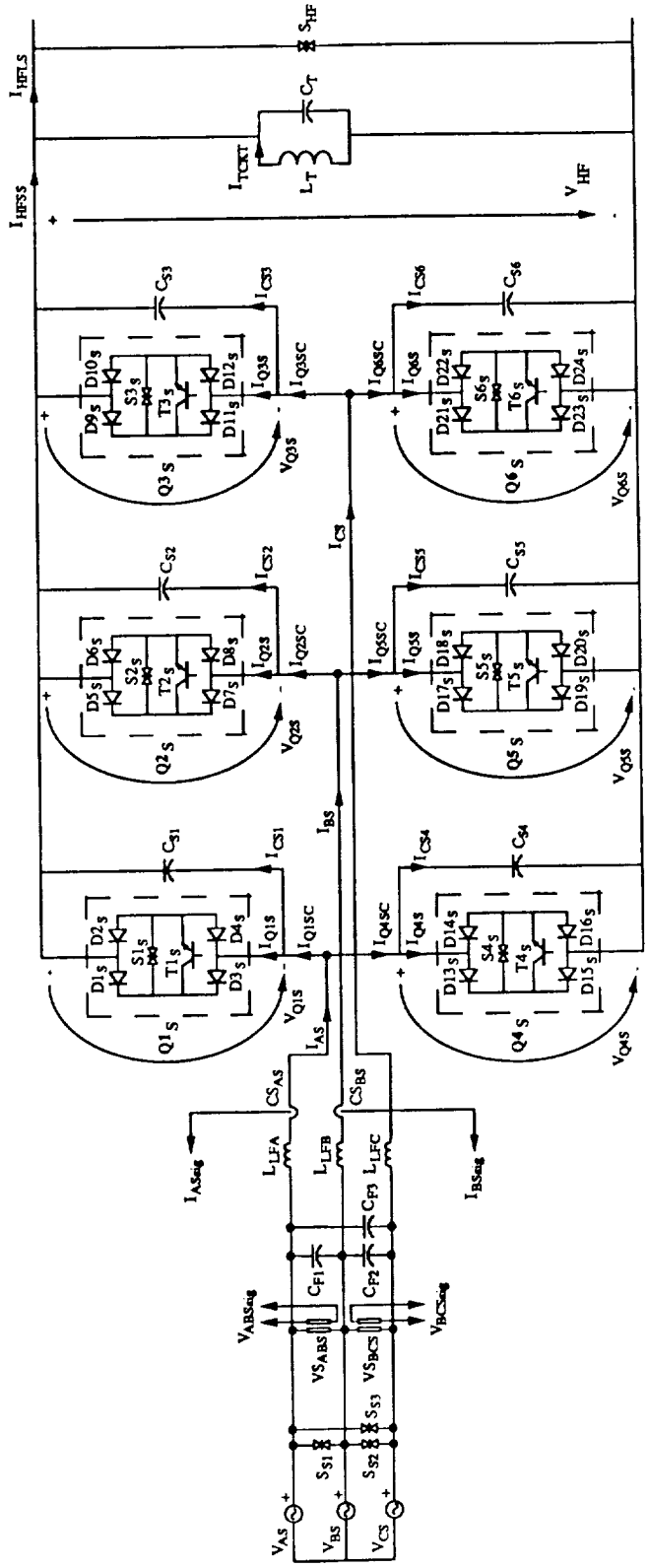


Fig. 5.2.a. Power Circuit Layout and Conventions for the Source Side PDM Converter.

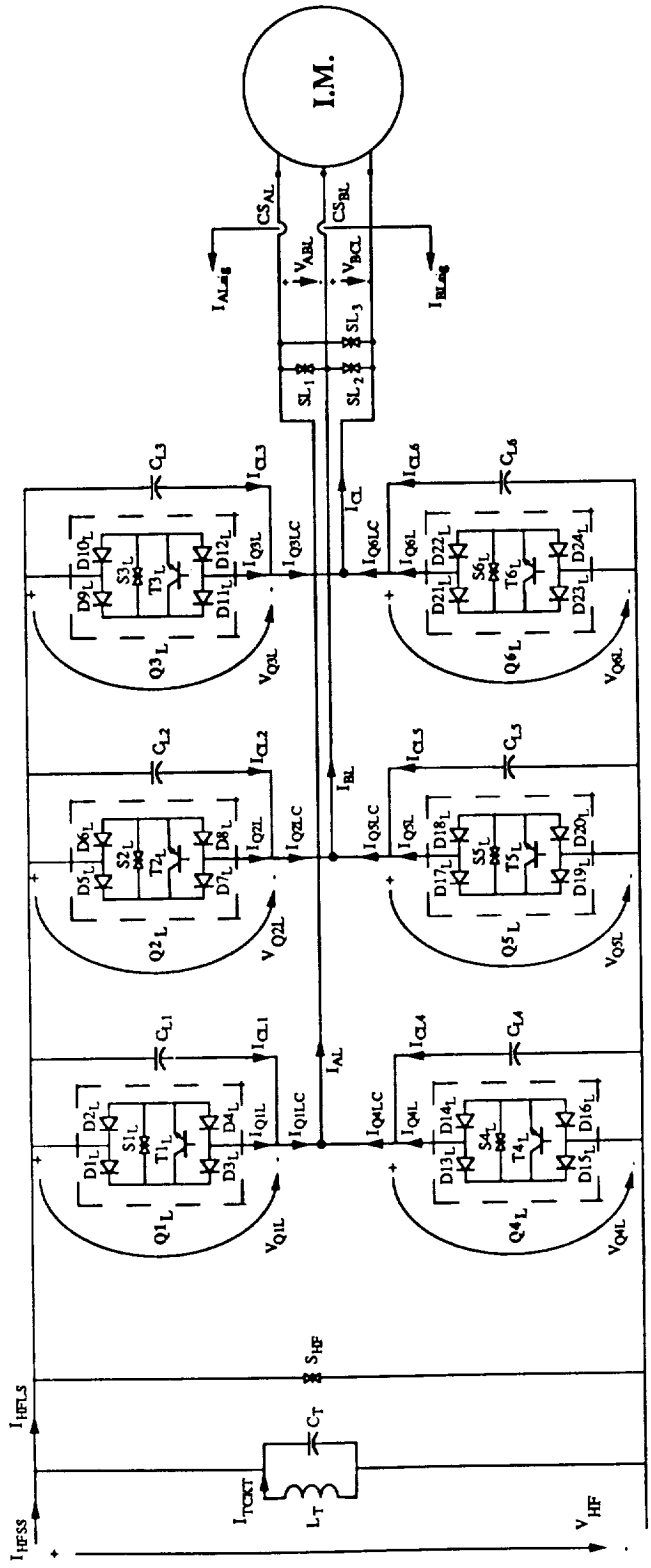


Fig. 5.2.b. Power Circuit Layout and Conventions for the Load Side PDM Converter.

| Component | Circuit Symbol | Key Specifications and Comments |
|---|---|---|
| Surge Suppressors | $S1_S$-$S6_S$, $S1_L$ - $S6_L$ | $V_{surge}$: 560$V_{DC}$,GE part #:V420LA40B |
| | $S_{S1}$ - $S_{S3}$ | $V_{surge}$: 369$V_{DC}$, GE part #:V275LA40B |
| | $S_{L1}$ - $S_{L3}$ | $V_{surge}$: 420 VDC, GE part #:V320LA40B |
| | $S_{HF}$ | $V_{surge}$: 560$V_{DC}$, GE part #:V420LA40B |
| Source Side Filter Capacitors | $C_{F1}$ - $C_{F3}$ | 13.6 μF, 400 $V_{DC}$<br>Two 6.8 μF, 400 $V_{DC}$ in parallel |
| Source Side Line Filter Inductors | $L_{LFA}$ - $L_{LFC}$ | Tap1: 2.85 mH, 100 mΩ, 35 Arms<br>Tap2: 1.4 mH, 53 mΩ, 35 Arms<br>Tap3: 0.9 mH, 35 mΩ, 35 Arms |
| Source Side Current Sensors | $CS_{AS}$ & $CS_{BS}$ | 100 A rms, DC-100 kHz, 1:1000 ratio<br>part #: LEM LT 100-S<br>1 turn is used, generating 5 V for 50 A peak with 100 Ω terminator resistor |
| Load Side Current Sensors | $CS_{AL}$ & $CS_{BL}$ | 80 Arms, DC - 100 kHz, 1:1000 ratio<br>part #: LEM LT 80-P<br>1 turn is used, generating 5 V for 50 A peak with 100 Ω terminator resistor |
| Source Side Voltage Sensors | $VS_{AB}$ & $VS_{BC}$ | 1000 V rms, DC - 100 kHz, 10000: 2000 ratio<br>part #: LEM LV 100/SP5, R1=50 KΩ<br>250 V peak input yields 5 mA peak input, 25 mA peak output and 11.25 V control signal with 450 Ω terminator resistor. |

Table 5.3.b. Component Values Used in the Upgraded 3Ø to 3Ø Power Conversion System, Circuit Symbols and Key Specifications.

### 5.2.2 Description of the Control Circuit

In general, there are two basic control modes for the induction machine. One mode is torque control and the other concerns speed regulation. It is possible to select one of these modes through a manual switch. The reference signal for either mode is manually adjusted by means of a trim pot and it is possible to change its sign with another manual switch for negative torque or speed control. In the torque regulation mode, the torque command is directly applied whereas in the speed regulation mode, the torque command is generated from a PI speed regulated output.

In the torque regulation mode, sufficient load/prime-mover torque must be applied to the shaft of the induction machine in order to be able to operate at the desired torque point. If insufficient load torque is applied to the shaft in the motoring mode, the induction machine could speed-up indefinitely. If insufficient prime-mover torque is applied to the shaft in the generating mode, the expected active power can not be generated and machine will stop.

In the speed regulation mode, the controller regulates the speed as desired by applying required amount of torque up to but not exceeding its limit. Usually this torque limit is set to the rated torque of the machine When a certain speed reference is given, the speed regulator applies the maximum torque command (usually the rated torque) to reach the commanded speed as soon as possible. Once the reference speed is reached only a required amount of torque command determined by the load is applied to the induction machine. For instance, if no load torque is applied, the torque command required after reaching the reference speed corresponds only to the losses and the inertia of the induction machine and the connected DC machine.

### 5.2.3 Power Matching and Link Voltage Regulation

This part of the controller functions as a power matching controller between the source and load. The controller consists of primarily of a power estimator and a link voltage regulator block. Active power estimation of the induction machine is achieved using the torque and flux commands, and rotor speed information. The torque and the flux commands are the commands used by the Field Oriented Controller to control the induction machine via the 3Ø-PDM converter. The losses of the induction machine, high frequency link losses, source and load side PDM converter losses are included in the overall power estimation.

Since only average power matching is done, the PI link voltage regulator exists as an additional minor control loop, but plays an important role in the power matching process

especially when the level of power transferred is increased and the resonant link tank circuit energy storage capacity is not sufficient to supply the instantaneous power demand. For a more detailed discussion of the function of the link voltage regulator, the reader is referred to Section 4.3. A block diagram of this part of the controller was shown in Fig. 4.2. In this controller, a DC reference signal generated from the power estimation and the link voltage regulation loop is used along with the measured line to neutral source voltages to generate 3Ø, 60 Hz source side reference current signals. The estimated power is set to be delivered at unity power factor by just adjusting the phases of the reference current signals generated. This is accomplished by direct multiplication of a DC current amplitude command signal with line to neutral source voltage signals and generates 3Ø, 60 Hz reference current signals in phase with the source voltages for unity power factor operation. The power estimation, matching and the link voltage regulation block diagram was included in the overall control block diagram shown in Fig. 5.3.

### 5.2.4 Field Oriented Controller

As mentioned earlier, an Indirect Field Oriented Controller developed in University of Wisconsin-Madison [1,2] has been adopted to control the induction motor dyno. Once the necessary settings of the Indirect Field Orientation Controller were fixed for the new induction machine, machine can then be controlled by three pieces of information. These are the flux command (usually rated flux command), a desired torque command depending on torque or speed regulation modes, and the field angle information. A block diagram of this Indirect Field Oriented Controller is included in Fig. 5.3. Desired 3Ø reference currents for the induction machine are generated through the Field Orientation Controller.

### 5.2.5 Source Side 3Ø-PDM Controller

Once the 3Ø source side reference current signals are generated from power matching and link voltage regulation loops, these reference currents along with the measured current signals are used for direct ON-OFF current regulation of the source currents through the 3Ø-PDM Converter as explained in Section 3.1.2. This control board is equipped with start/stop, over current protection for 3Ø source currents, over voltage and under voltage protection for the high frequency link voltage, soft starting, and clock signal generation protection circuits. In case of faults, the protection circuit activates a disable command and the gatings are blocked immediately after the first zero crossing of the high frequency link. Unfortunately, this immediate blocking of the gate signals impose

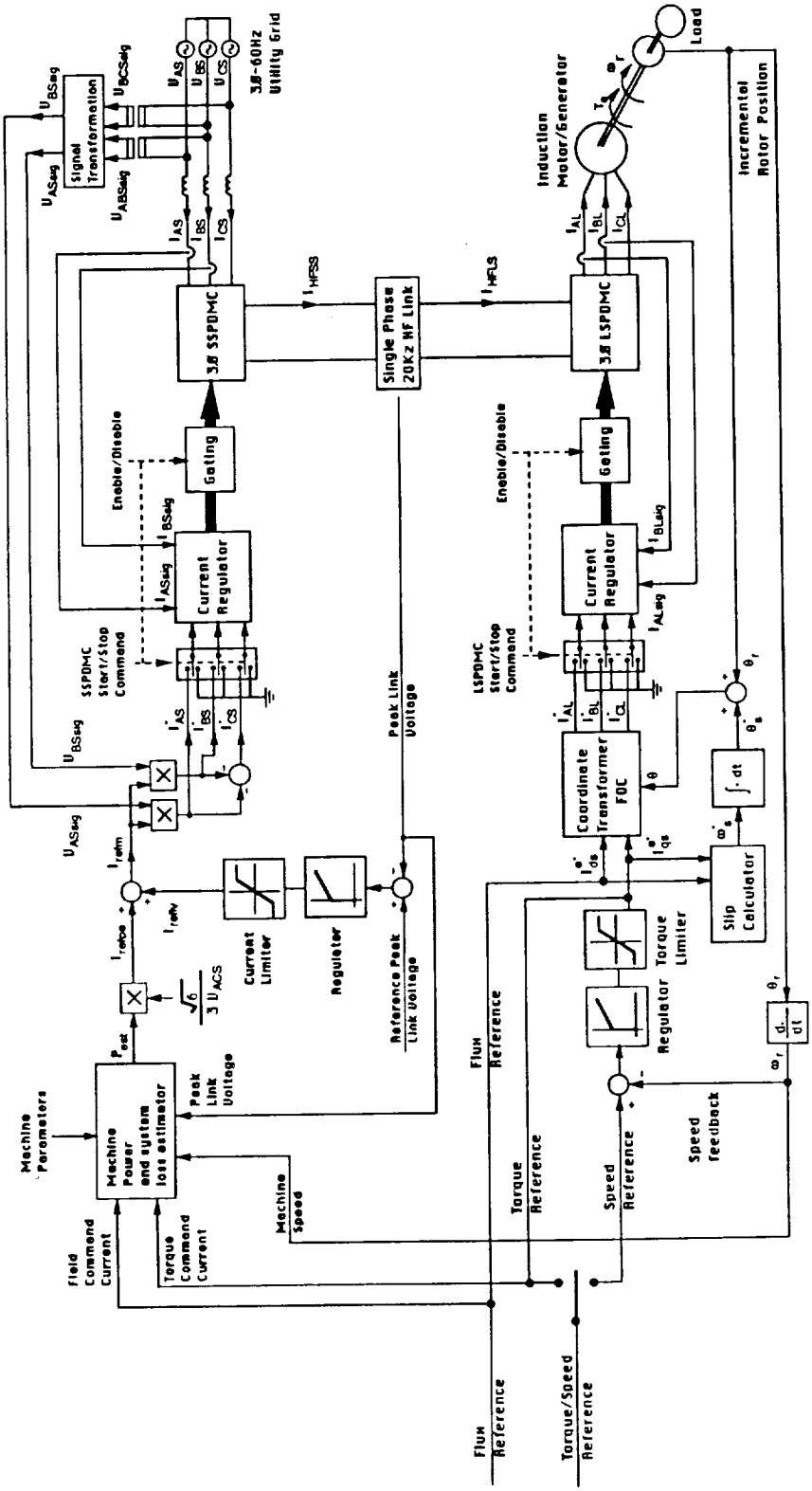


Fig. 5.3. Full Control Block Diagram of 3Ø to 3Ø Power Conversion System Based on Parallel Resonant HF AC Link and Operating From Utility At Unity Power Factor.

voltage spikes across the bilateral devices because of the stored energy in the line inductors. In the current system configuration, this case is still handled with surge suppressors. Normal, in a no fault situation, when the stop command is given, the load side reference currents are set to zero forcing the induction machine currents to zero. Hence, by regulation of these currents close to zero, the voltage spike problem is greatly reduced. Figure 5.3 partly covers the function of this controller in a block diagram form.

### 5.2.6 Load Side 3Ø-PDM Controller

The 3Ø reference current signals generated from an indirect field oriented controller along with the measured induction machine current signals are used for direct ON-OFF current regulation of the induction machine currents through the load side 3Ø-PDM converter. This controller is equipped with over current protection for the induction machine currents, reset and clock signal generation protection circuits, and a soft current stopping circuit for the faults. This circuit blocks the gating of related phases sequentially whenever the related phase current passes through zero. Therefore, it again reduces the voltage spike problem. Again, Fig. 5.3 partly shows the function of this controller in block diagram form.

## 5.3 Test Results and Discussion

### 5.3.1 Test Conditions

The overall system has been tested under a number of different conditions. In the initial test, only the operation of the source side PDM converter was tested. Load side PDM converter operation is not included in this case. This test covers the starting of the source side PDM converter, including link voltage build-up and link voltage regulation. Since the overall system can be considered to be at no load, a 3Ø, 60 Hz source supplies only the operating losses of the SSPDM and the link in this case.

In a second study, the starting and operation of the load side PDM converter was tested with the source side PDM converter in operation. The operating point of the induction machine (load) was determined by the Field Oriented Controller and the load torque applied to the machine. As the power level transferred from the source to the load is increased, the link voltage variation becomes a very important obstacle to operation of the overall system at high power levels. Since only one tank circuit of the first prototype was used during these tests, the tests were initially conducted with a limited power range

corresponding to rated flux, 40% of rated torque and about 30% of rated speed and frequency. At this operating point, the machine draws around 2.76 kW active power including the converter and the link losses at almost unity power factor. In the torque control mode, it is still possible to cover a reasonable wide speed and frequency range by adjusting the field of the DC-dynamometer. For the 10 hp machine under test, the rated flux component of the current was determined to be 21.37 A rms (30.22 A peak) and the rated torque component of the current was 23.47 A rms (33.20 A peak). Since these current values are the line current values and the induction machine is Δ-connected, the flux and the torque components of the winding currents becomes 12.34 A rms (17.45 A peak) and 13.55 A rms (19.16 A peak) respectively.

Various operating characteristics such as link voltage regulation, power matching between the source and the load, zero voltage switching characteristics, determination of device stresses, source and load side current regulation capability, effectiveness of the synthesis of the induction machine voltages from high frequency link half cycle voltages in current regulation mode and their harmonic spectrums as well as other operational features were recorded during these test and will be discussed below.

### 5.3.2 Scaling Between the Real and Control Quantities

Before starting the presentation of the test results, it is useful to discuss first the scaling factors between the real power circuit quantities and their corresponding control circuit signals. These scaling basically are summarized in Figs. 5.4, 5 and 6. In Fig. 5.4, the first figure from the top shows the real source side line to line voltage, the second figure from the top shows its control circuit signal correspondence. Since the source line to line voltage is set to 178 V rms, existence of approximately a 250 V peak in the first figure from the top confirms this value. The source line to line voltage control circuit signals are used to generate the line to neutral versions of those voltages. Only the line to neutral voltages are used in the power estimation process. Therefore, the scaling should be implemented according to synthesized line to neutral quantities. The third figure from the top shows one of these generated line to neutral source voltage control signals. Scaling of the line to neutral voltages roughly gives a factor of 23 indicating that a 6 V line to neutral control signal corresponds to 6x23=138 V actual line to neutral and $\sqrt{3}$x138=239 V actual line to line voltage. Since the second figure from the top is a measurement taken by using the generated line to neutral voltage signals, the total error in obtaining the line to neutral voltage signals can be easily observed by the phase shift between the real and measured line to line voltages. This total error in turn contributes to an error in unity power factor

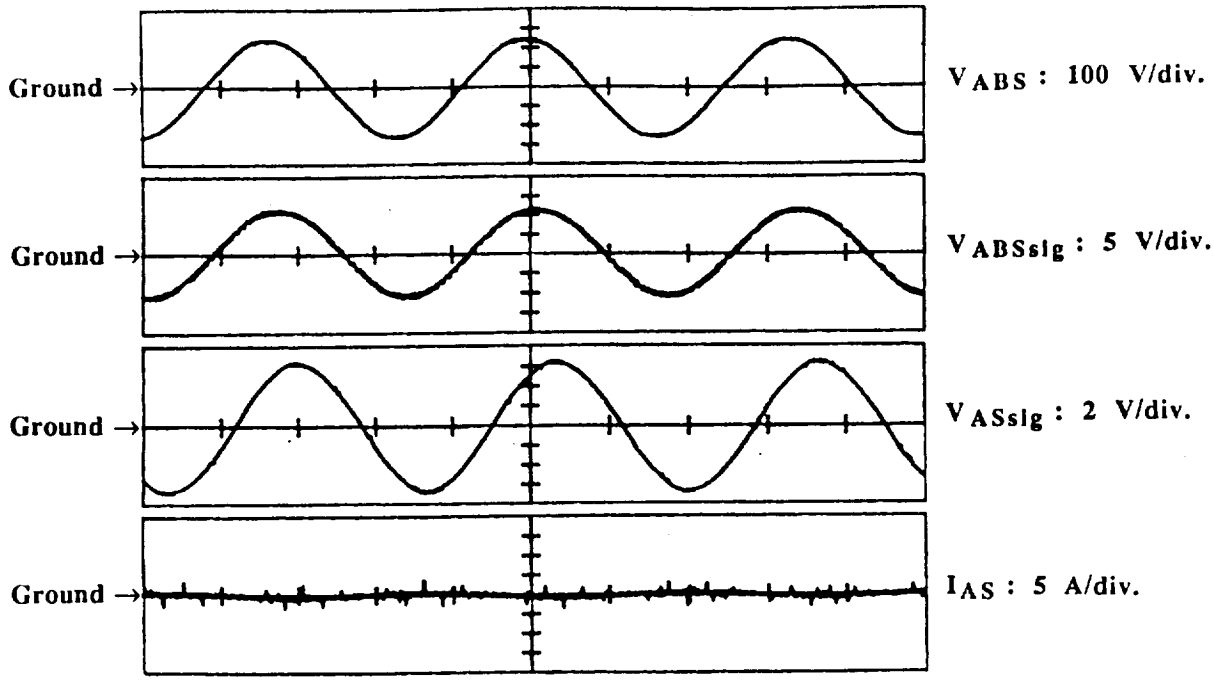


Fig. 5.4. Source Voltage Scaling Between the Real Values and Control Signals. From the Top Respectively; Phase AB Line to Line Source Voltage: $V_{ABS}$ : 100 V/div. Phase AB Line to Line Source Voltage Control Signal: $V_{ABSsig}$ : 5 V/div. Phase A Line to Neutral Source Voltage Control Signal: $V_{ASsig}$ : 2 V/div. Phase A Source Line Current: $I_{AS}$ : 5 A/div. Time/div: 5 msec.

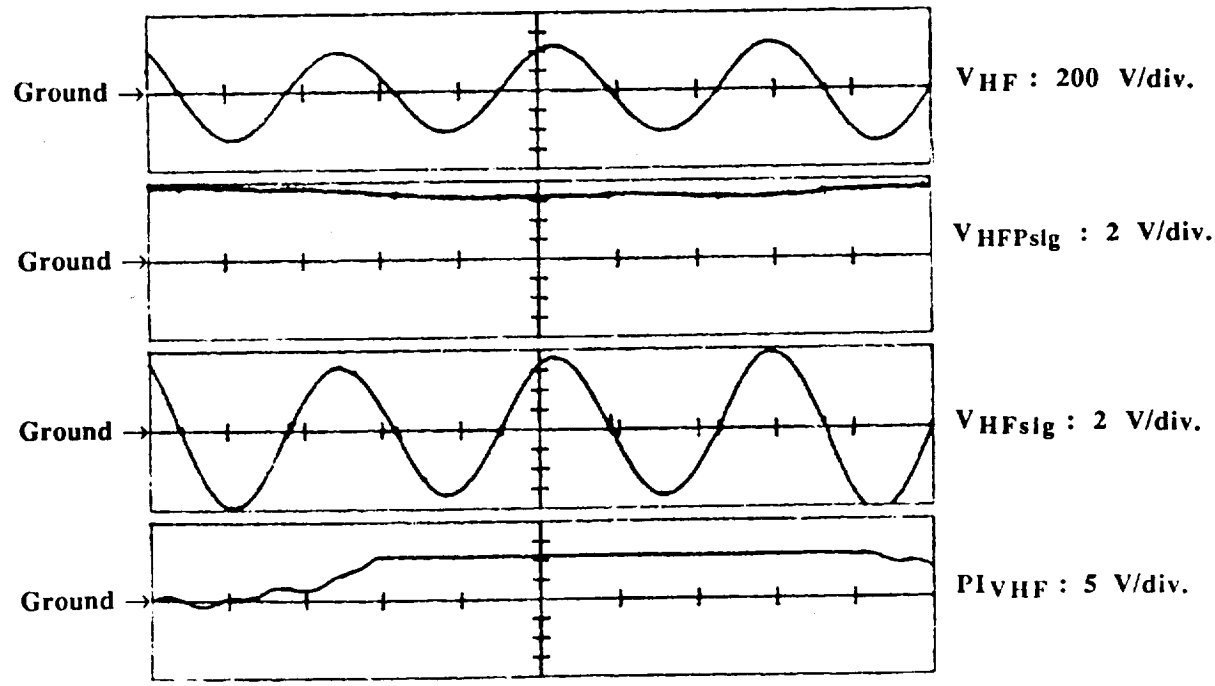


Fig. 5.5. HF Link Voltage Scaling Between the Real Values and Control Signals. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. HF Link Voltage Peak Control Signal: $V_{HFPsig}$ : 2 V/div. HF Link Voltage Control Signal: $V_{HFsig}$ : 2 V/div. HF Peak Link Voltage PI Controller Output: $PI_{VHF}$ : 5 V/div. Time/div: 20 µsec.

operation. The last figure from the top in Fig. 5.4 shows the real source side line current. Since this picture was taken when neither of converter was operating, the current drawn from the source is almost zero. It can be noted that a very small amount of current flows through the filter capacitors placed into the source side.

Figure 5.5 shows, from top, the actual high frequency link voltage, its measured peak signal, the measured signal and the PI link voltage regulator output respectively. The peak link voltage reference was set to around 511 V. Note that when the link voltage drops below its reference, the PI regulator commands an increase and when the link voltage exceeds its reference, the PI regulator commands a decrease in the delivered power from the source. The scaling between the real and measured signals a scale factor of 65 meaning that an 8 V control signal would correspond to 8x65=520 V actual high frequency link voltage.

Figure 5.6 indicates the scaling of the source and load side low frequency currents. The figure was taken under operating conditions wherein the induction machine operates at full rated flux, 40% of rated torque and 30% of rated frequency which corresponds to 90 Hz operation. The fundamental component of line to line rms induction machine voltage synthesized from the high frequency link at this condition is measured to be 71.45 V which satisfies the constant volts per hertz and rated flux constraint for satisfactory operation. The corresponding source side quantities are 60 Hz and 178 V line to line rms. The first two traces from the top in Fig. 5.6 show phase C load side line current with actual and measured (control circuit) signals respectively. Similarly, the last two traces from the top in Fig. 5.6 show phase C source side line current scaling at 60 Hz with actual and control circuit signals respectively. These traces roughly reveal a scaling factor of 10 A per control signal volt for both source and load side currents.

### 5.3.3 Link Voltage Build-up, Regulation, and Operational Characteristics of PDM Converter

Figure 5.7 shows the link voltage build-up and regulation during starting of the source side PDM converter. It can be noted that the link voltage builds-up and, after a small overshoot, settles down and is quite well regulated. The peak link voltage is a little over 500 V. Quite a large circulating current occasionally reaching 175 A peak in the resonant tank circuit can be observed. Since the load side PDM converter is not yet in operation, the peak of the resonant tank circuit current appears almost constant. The source side high frequency link current is about 20 A peak excluding the very instant of starting. Normally, it was observed that once the peak link voltage settles down, the required

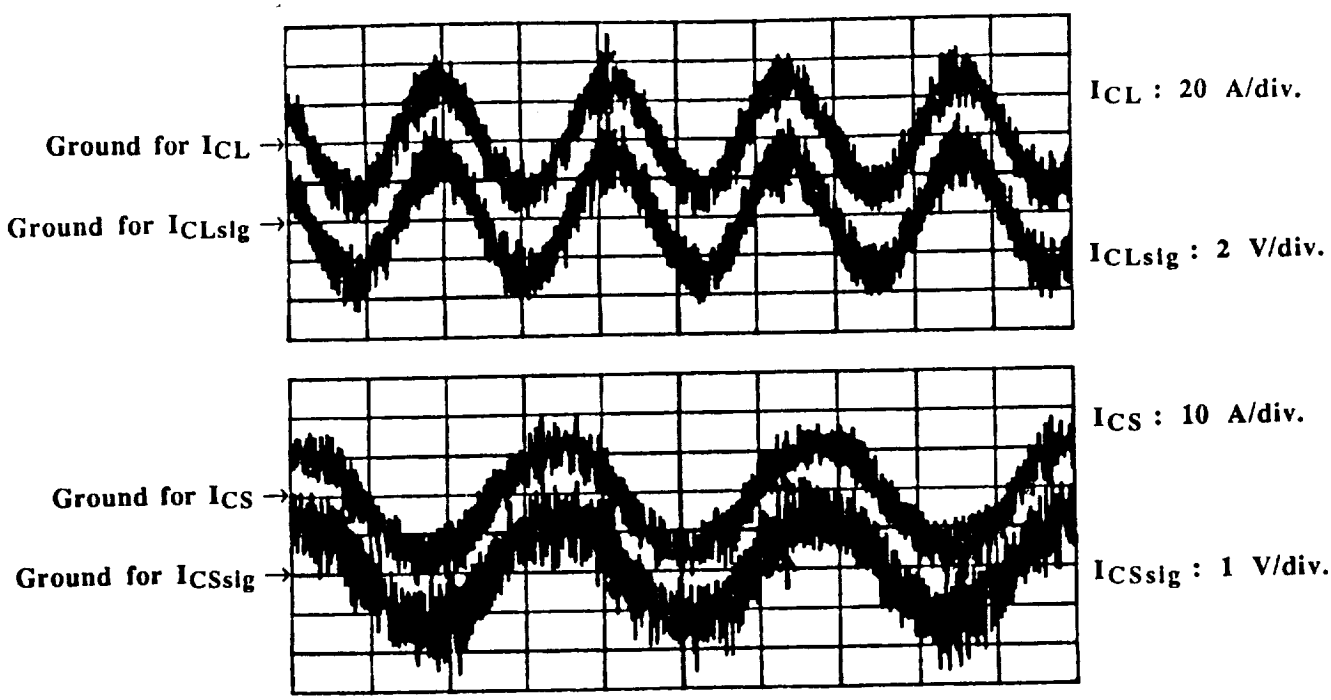


Fig. 5.6. Source and Load Current Scaling Between the Real Values and Control Signals. From the Top Respectively; Phase C Load Line Current: $I_{CL}$ : 20 A/div. Phase C Load Line Current Control Signal: $I_{CLsig}$ : 2 V/div. Phase C Source Line Current: $I_{CS}$ : 10 A/div. Phase C Source Line Current Control Signal: $I_{CSsig}$ : 1 V/div. Time/div: 5 msec.

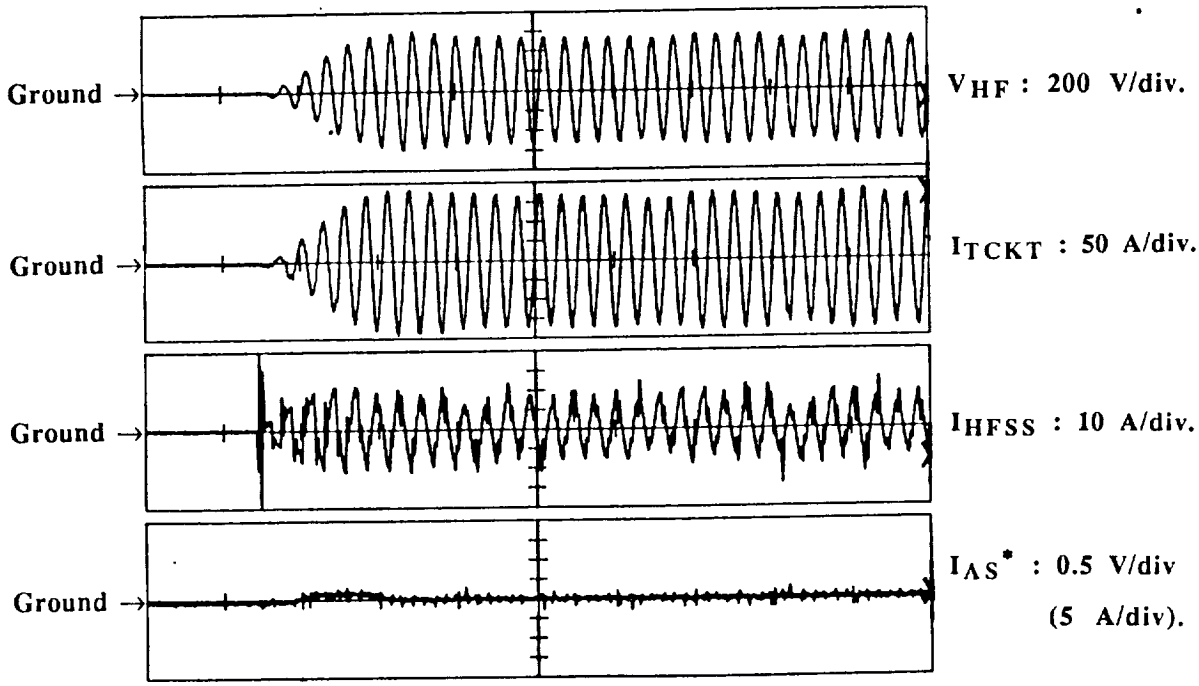


Fig. 5.7. Link Voltage Build-up and Regulation when Load Side PDM Converter is not in Operation. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. HF Resonant Tank Circuit Current: $I_{TCKT}$ : 50 A/div. Source Side HF Link Current: $I_{HFSS}$ : 10 A/div. Phase A Source Current Reference Signal: $I_{AS}^*$ : 0.5 V/div (5 A/div). Time/div: 200 μsec.

amount of energy to keep the peak link voltage constant is very small, being the value to just compensate the operation losses of the SSPDMC and the high frequency link. Therefore, one should expect that the source side high frequency link current should have much smaller magnitudes. The variational pattern of this current and its relatively high magnitude is due to the ripple current imposed on the source side currents due to the interaction of the source and the high frequency link via the switching action of the source side PDM converter.

The last figure from the top in Fig. 5.7 shows the reference current for the source side phase-A line current. The reference current increases in magnitude during the link voltage build-up and reduces once the link voltage is established. Even though the reference current is set to almost zero, the actual source currents do not become zero due to the interaction between the source and high frequency link via the PDM converter as mentioned above.

The effect of starting the load side converter is shown in Fig. 5.8. Note that for almost the first two divisions of the time scale (2 msec) the load side PDM converter is not started. As soon as it is started, the peak link voltage drops from around 500 V to around 350 V and the resonant tank circuit current decreases from around 170 A to almost 50 A. However, source side high frequency link current does not show any dramatic change which would affect the resonant tank circuit current. As seen from the last figure from the top, the source side line current reference signal magnitude is increased after the load side converter is started. However, because of the delay in the system response and the low energy storage capacity of the resonant tank circuit, the link voltage regulation becomes poor. Figure 5.9 is a magnified view of Fig. 5.8 around the load side converter starting. It is also clear from Fig. 5.9 that after load side PDM converter operation is initiated, the peak resonant tank circuit current shows large variations, this, in turn of course, causes the link voltage variations. These variations are maximum at the time of starting, but are not so dramatic especially as time progresses as seen from Fig.5.8.

Clearly, the major cause of this problem is the sudden increase of the load side high frequency link current. This point is confirmed with Figs. 5.10 and 11. In these two figures, the start of load side converter operation is re-initiated with only a change in the measurement of high frequency link current from the previous two figures. That is, the load side high frequency link current is shown instead of source side. In this case, initiation of the start of the load side converter causes the peak link voltage and the peak resonant tank circuit current to drop to zero and then rebuild. However, when the link voltage rebuilds, peak link voltage reaches 800 V for the first 6 link cycles even though it later returns to normal level of operation. Here again, the importance of the bilateral switch

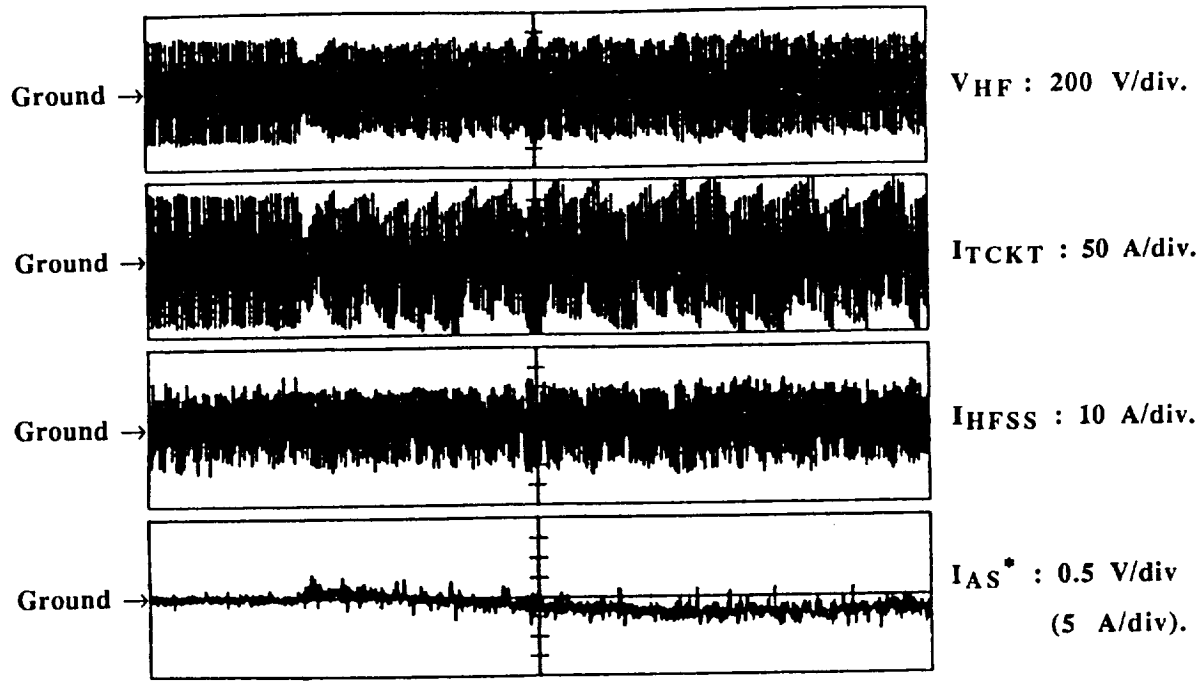


Fig. 5.8. The Effect of Starting the Load Side PDM Converter. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. HF Resonant Tank Circuit Current: $I_{TCKT}$ : 50 A/div. Source Side HF Link Current: $I_{HFSS}$ : 10 A/div. Phase A Source Current Reference Signal: $I_{AS}^*$ : 0.5 V/div (5 A/div). Time/div: 200 μsec.

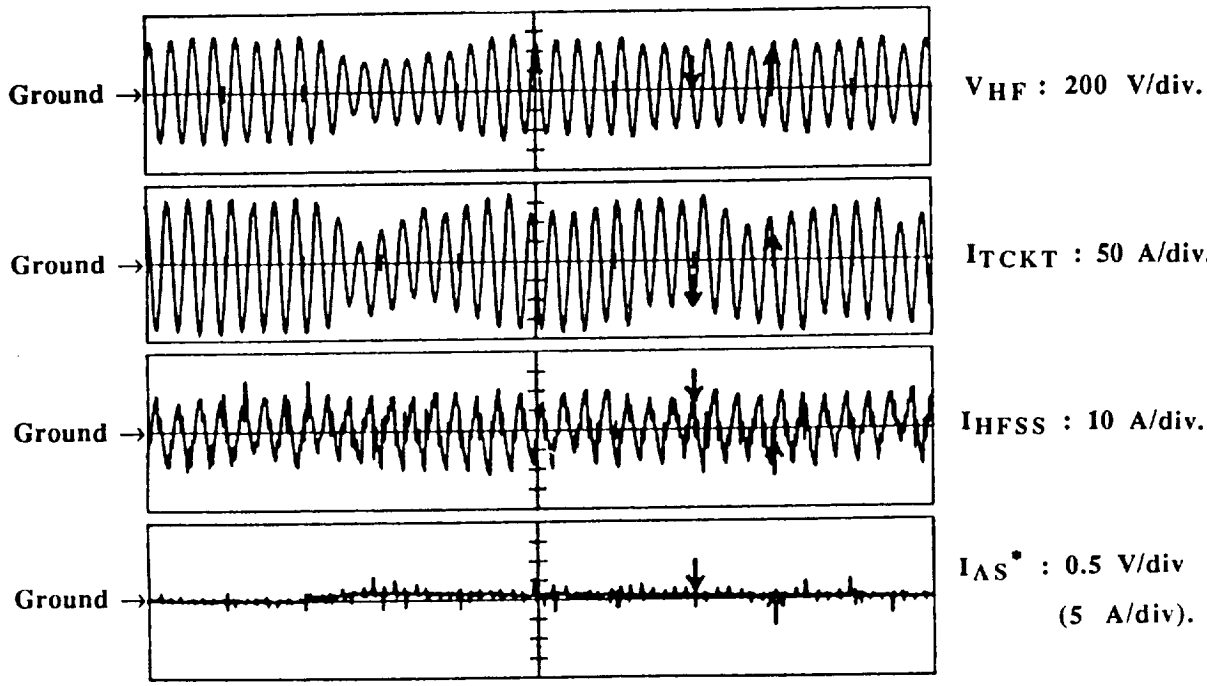


Fig. 5.9. Magnified View of Fig. 5.8 During Load Converter Starting. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. HF Resonant Tank Circuit Current: $I_{TCKT}$ : 50 A/div. Source Side HF Link Current: $I_{HFSS}$ : 10 A/div. Phase A Source Current Reference Signal: $I_{AS}^*$ : 0.5 V/div (5 A/div). Time/div: 1 msec.

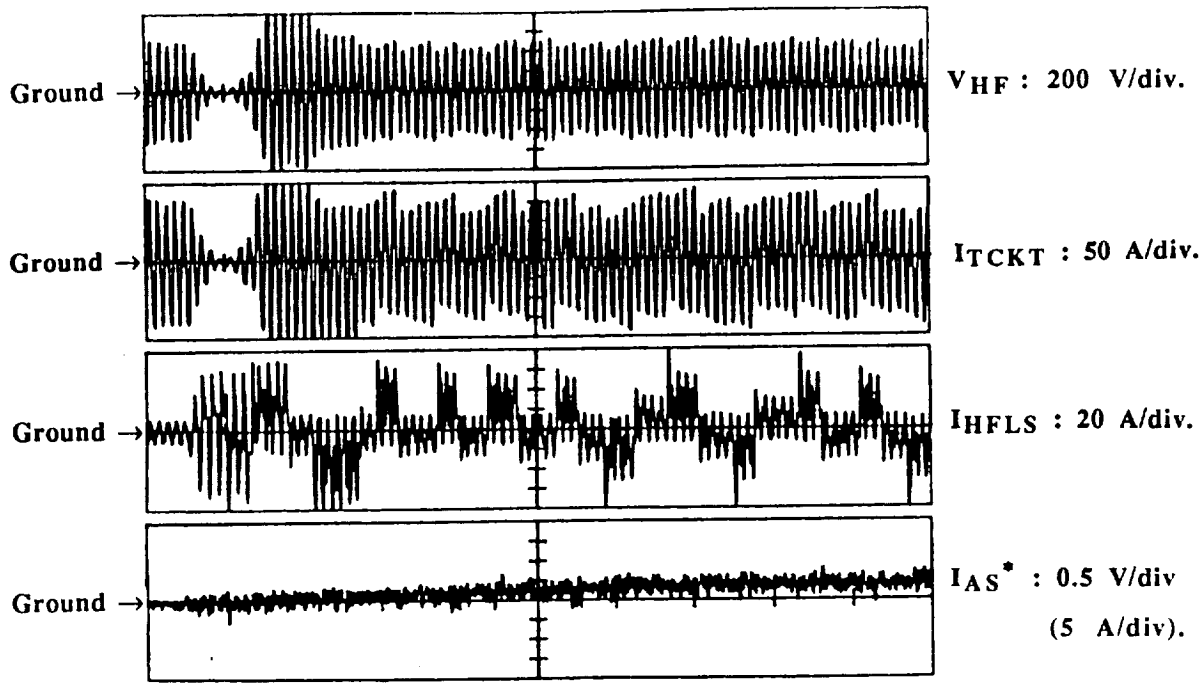


Fig. 5.10. The Effect of the Load Side Converter Operation on Peak Link Voltage Regulation. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. HF Resonant Tank Circuit Current: $I_{TCKT}$ : 50 A/div. Load Side HF Link Current: $I_{HFLS}$ : 20 A/div. Phase A Source Current Reference Signal: $I_{AS}^*$ : 0.5 V/div (5 A/div). Time/div: 500 μsec.

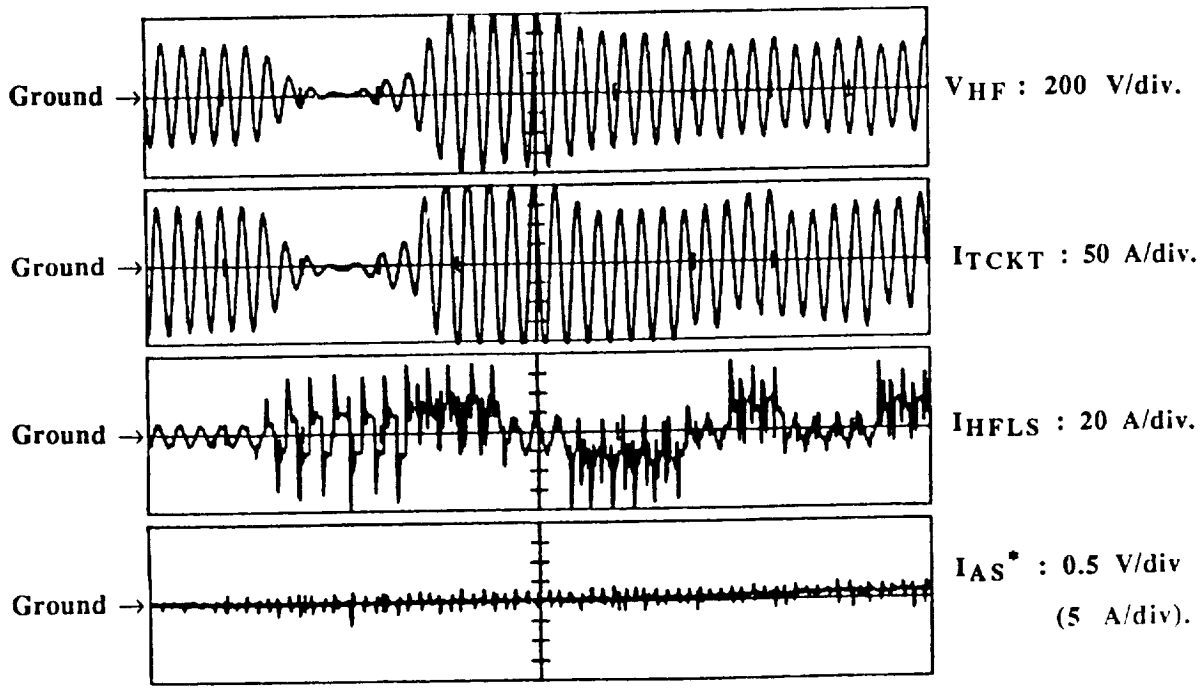


Fig. 5.11. Magnified View of Fig. 5.10 During Load Converter Starting. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. HF Resonant Tank Circuit Current: $I_{TCKT}$ : 50 A/div. Load Side HF Link Current: $I_{HFLS}$ : 20 A/div. Phase A Source Current Reference Signal: $I_{AS}^*$ : 0.5 V/div (5 A/div). Time/div: 200 μsec.

voltage stress is emphasized by requiring a 800-900 V blocking capability which is in fact more than what we anticipated in sizing the switches. It is clear from Figs. 5.10 and 11 that the magnitude and the polarity of the load side high frequency link current has very large effect on the resonant tank circuit current and relatively less effect on the high frequency link voltage. Figure 5.11 is a magnified view of the Fig. 5.10 around the starting of the load side converter.

Figure 5.12 shows a different aspect of the load side converter operation. From the top respectively, the traces show the load side Q6 device current, the resonant tank circuit current, the load side high frequency link current and the gating signal for the load side Q6 device. This figure basically reveals the relationships which exist among the load side device currents, the resonant tank circuit current and the load side high frequency link current. That is, the load side high frequency link current is determined by the three switches which are in conduction at any instant.

Figure 5.13 shows both source side and load side PDMC starts. Prior to energization, all signals are at zero level. As soon as the sourced side converter is started, the peak of the source side line currents jumps to around a 10 A level even though the peak of the reference stays around zero. As explained before, the reason for this behavior is the high frequency ripple currents on the 60 Hz source side currents due to the interaction of the source and the high frequency link via the source side converter. As seen from the trace, the peak link voltage is a little higher than 500 V and since the load side converter is not started, the load side current remains at zero. As soon as the load side converter is started, the peak load side line current increases to approximately 40 A and the peak of the source side reference current to about 7 A. This, in turn, increases the peak of the actual source line current to around 13 A because of the high frequency ripple current. Since the induction machine is driven with a field oriented controller, a constant peak value of induction machine current begins to flow beginning from very low frequency and as the speed of the induction machine increases, the frequency of the currents also increase.

### 5.3.4 Power Matching between the Source and Load

Figure 5.14 gives an idea about the power matching between the source and the load and at the same time it shows another start of the source and load side converters respectively. When the load side converter is started, the total DC power matching reference signal jumps from almost zero to a -0.8 V peak level, as noted in the second figure from the top. This signal is obtained from two signals. One portion is from the induction machine power and the overall system loss estimation signal, located as the third

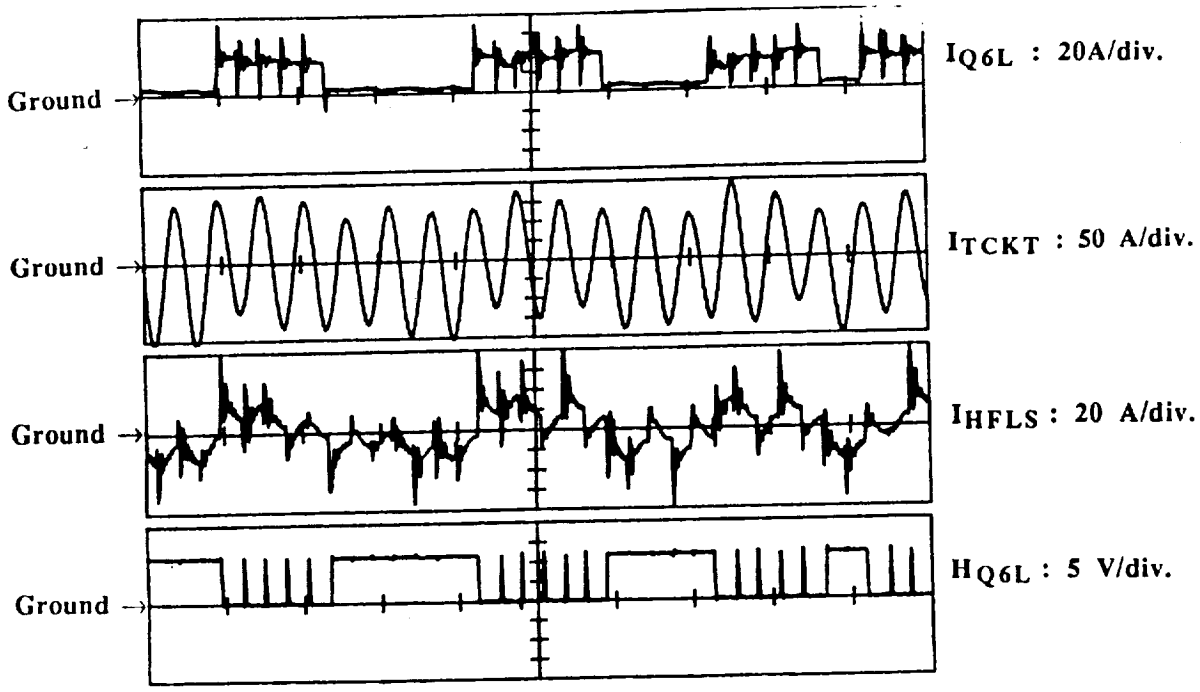


Fig. 5.12. Current Flow Relationships for the Load Side PDM Converter Operation. From the Top Respectively; $Q_{6L}$ Bilateral Device Current: $I_{Q6L}$ : 20A/div. HF Resonant Tank Circuit Current: $I_{TCKT}$ : 50 A/div. Load Side HF Link Current: $I_{HFLS}$ : 20 A/div. Gating Logic Signal for Bilateral Device Q6: $H_{Q6L}$ : 5 V/div. Time/div: 100 μsec.

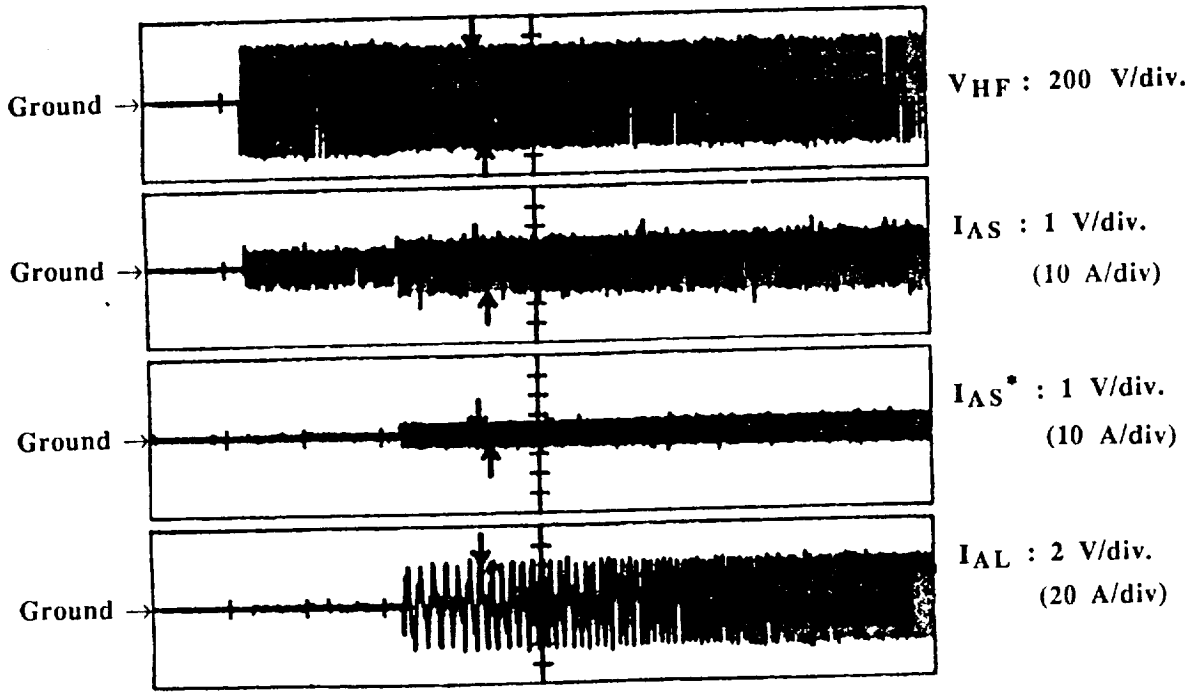


Fig. 5.13. The Effect of Starting the Source and Load Converters on Source Side Line Current. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Phase A Source Current: $I_{AS}$ : 1 V/div (10 A/div). Phase A Source Current Reference Signal: $I_{AS}^*$ : 1 V/div (10 A/div). Phase A Load (Induction Machine) Line Current: $I_{AL}$ : 2 V/div (20 A/div). Time/div: 500 msec.

figure from the top and the other is from peak link voltage PI regulator output, located as the fourth figure from the top. These two signals are summed according to independent gains to generate the resulting total DC power matching reference signal, the second figure from the top. The inverted version of this signal is used to generate 3Ø, 60 Hz source side reference current signals as described in the power matching and link voltage regulation subsection numbered as Section 5.2.3.

As is clear from Fig. 5.14, when only the source side converter is operating, the output of PI-peak link voltage regulator is operating within the linear and mostly commanding a decrease mode region for the peak link voltage. This means even a very small DC power matching reference signal is enough to meet the operating losses of the source side converter and link. As soon as the load side converter is started, the PI-peak link voltage regulator starts operating mostly commanding an increase mode region for the peak link voltage. This means most of the time the peak link voltage drops below its reference requiring more power to be delivered.

Figure 5.15 shows the source and load side converter starting in a much wider time scale. In this figure, the high frequency link voltage is replaced with the phase A source side reference current signal. As seen from the figure, source side converter starting might not be noticed from the average power matching signal, the second figure from the top or from its reflection, to the source side reference current signal, first figure from the top. However, the fourth figure from the top clearly reveals the starting of the source converter.

Step changes only occur when load side converter is started along with an immediate power requirement due to the induction machine start. Since the induction machine is commanded to operate at full flux, 40% of its rated torque, the first step jump in the required power is due to the induction machine power demand. This step jump is followed by a continuous increase in the amplitudes of DC power matching signals as well as source side Phase A reference signal as the machine speed increases until the induction machine reaches the 40% rated torque operating condition commanded by the field oriented controller.

Figure 5.16 shows a magnified view of Fig. 5.15. In this case the 60 Hz phase-A reference current signal starts with an amplitude of almost 4 A when the induction machine is started via the load side converter.

### 5.3.5 Source and Load Waveforms

Under the same operating conditions described earlier for the induction machine, Fig. 5.17 shows high frequency link voltage, 60 Hz source side line current, line to line

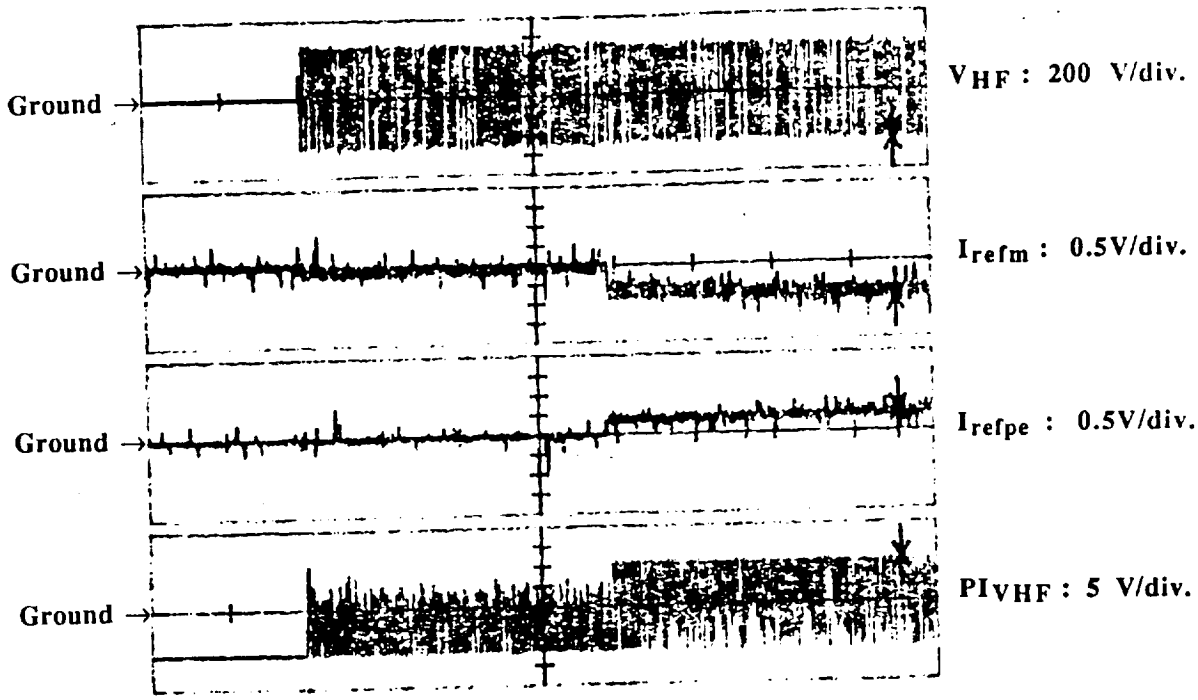


Fig. 5.14. Power Matching Signal Generation and Another View of Source and Load Converter Startup. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Total Power Matching DC Reference Signal: $I_{refm}$ : 0.5 V/div. Load And Loss Estimation Power Matching DC Reference Signal Component: $I_{refpe}$ : 0.5V/div. HF Peak Link Voltage PI Controller Output: $PI_{VHF}$ : 5 V/div. Time/div: 500 msec.

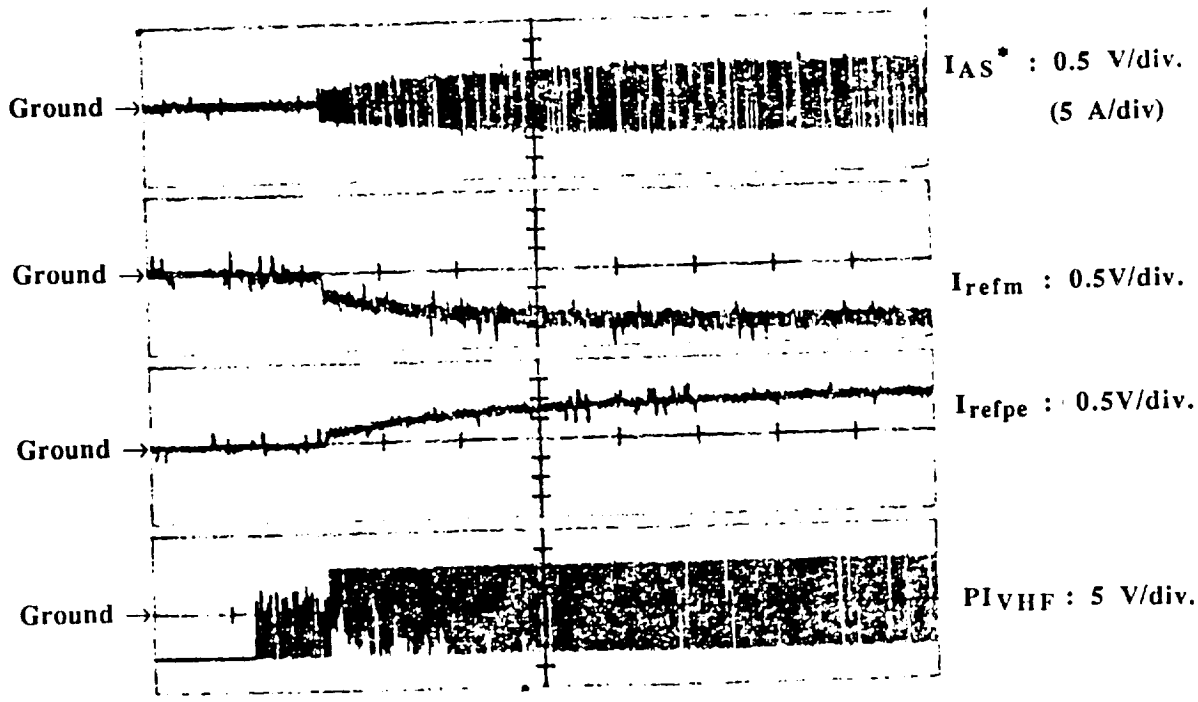


Fig. 5.15. Reflection of DC Power Matching Reference Signal to the 60Hz Source Line Current Reference Signal. From the Top Respectively; Phase A Source Current Reference Signal: $I_{AS}^*$ : 0.5 V/div (5 A/div). Total Power Matching DC Reference Signal: $I_{refm}$ : 0.5V/div. Load And Loss Estimation Power Matching DC Reference Signal Component: $I_{refpe}$ : 0.5V/div. HF Peak Link Voltage PI Controller Output: $PI_{VHF}$ : 5 V/div. Time/div: 5 sec.

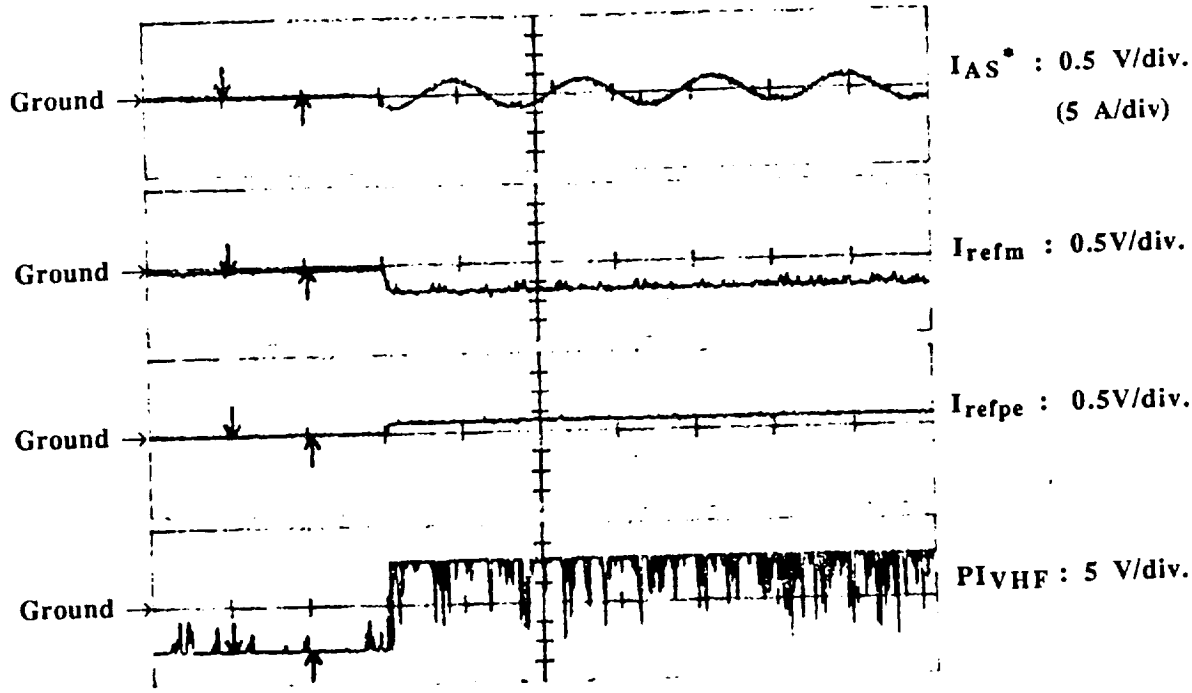


Fig. 5.16. Magnified View of Fig. 5.15. From the Top Respectively; Phase A Source Current Reference Signal: $I_{AS}^*$ : 0.5 V/div (5 A/div). Total Power Matching DC Reference Signal: $I_{refm}$ : 0.5V/div. Load And Loss Estimation Power Matching DC Reference Signal Component: $I_{refpe}$ : 0.5V/div. HF Peak Link Voltage PI Controller Output: $PI_{VHF}$ : 5 V/div. Time/div: 10 msec.

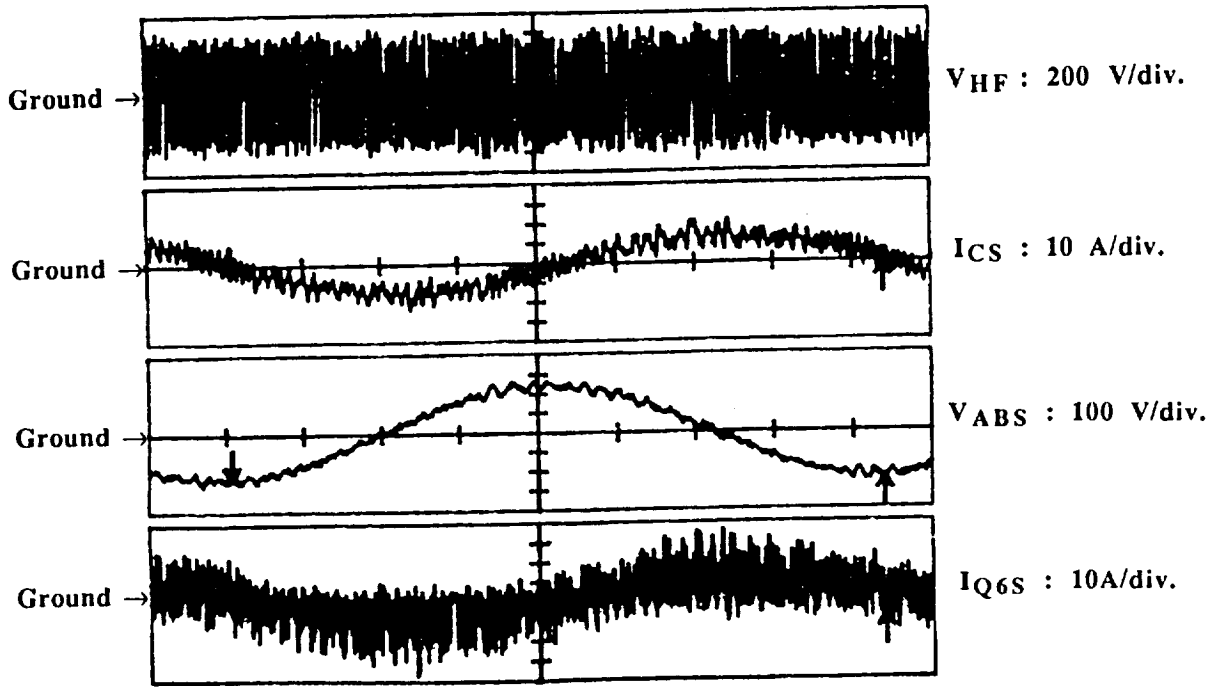


Fig. 5.17. Source Voltage and Current Waveforms in Operation. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Phase C Source Current: $I_{CS}$ : 10 A/div. Phase AB Line to Line Source Voltage: $V_{ABS}$ : 100 V/div. $Q_{6S}$ Bilateral Device Current: $I_{Q6S}$ : 10A/div. Time/div: 2 msec.

voltage, and bilateral switch current from the top to the bottom respectively. The bilateral switch current is shown as the last trace from the top. Since this current carries pieces of the source side line current, the second figure from the top, it shows the switch current stress even though it is not too precise. It is apparent that the device current stress does not exceed the 30-35 A range for source side line current magnitudes close to 20 A.

The harmonic spectrum of the source side line current shown in the second figure from the top in Fig. 5.17 is recorded in two different frequency ranges. These spectra are presented in Figs. 5.18 and 19. Figure 5.18 shows 0-2 kHz range which explicitly shows the 60 Hz fundamental component of the current and its amplitude in rms. Figure 5.19 shows the 0-50 kHz range which basically shows the harmonics present within this frequency range. In Figs. 5.18 and 19 1 mV rms corresponds to 0.5 A rms and 1 mV to 0.5 A. As can be seen from these two figures, in the 0-2 kHz range there are virtually no harmonics present. Some harmonics exist between the 3 and 9 kHz ranges but are not too significant in amplitude. The measurement of the source side line current whose harmonic spectrum is given is the same with the source line filter inductor current.

Since the high frequency ripple current imposed on the source side line currents introduces a very negligible amount of harmonics in the source voltages, their harmonic spectra are not presented here. This feature can be noticed by comparing the source side line current with the source side line to line voltage in Fig. 5.17.

Figure 5.20 shows the counterpart of the Fig. 5.17 by representing the load side waveforms instead of the source side in steady state under the same operating conditions specified before. That is, Fig. 5.20 shows the high frequency link voltage, 90 Hz load side (induction machine) line current, line to line voltage, and bilateral switch current from the top to the bottom respectively. The bilateral switch current indicates that the device current stress does not exceed 60-65 A range for load side line current magnitudes close to 30 A.

The harmonic spectrum of the induction machine current shown in the second figure from the top in Fig. 5.20 is recorded in two different frequency ranges. These spectra are presented in Figs. 5.21 and 22. Figure 5.21 shows 0-2 kHz range which explicitly shows the 90 Hz fundamental component of the current and its amplitude in rms. Figure 5.22 shows the 0-50 kHz range which basically shows harmonics present. In Figs. 5.21 and 22 1 mV rms corresponds to 2 Arms and 1 mV to 2 A. As seen from these two figures, in both ranges of frequency there are virtually no harmonics for the induction machine current. The harmonic spectrum of the load side line current is even better than the harmonic spectrum of the source side line current. The reason for this fact is the good current regulation capability of the field oriented controller. In the case of source side, the

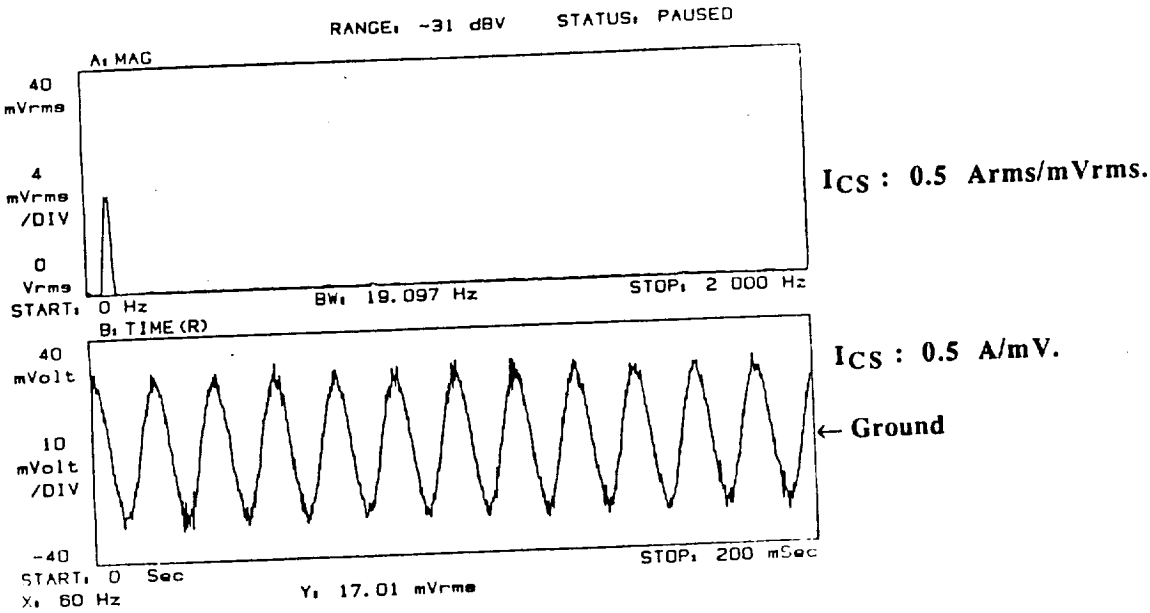


Fig. 5.18. Phase C Source Line Current (Shown in Fig. 5.17, $I_{CS}$) Harmonic Spectrum Over 0-2kHz Range. $I_{CS}$ : 0.5 Arms/mVrms & 0.5 A/mV.

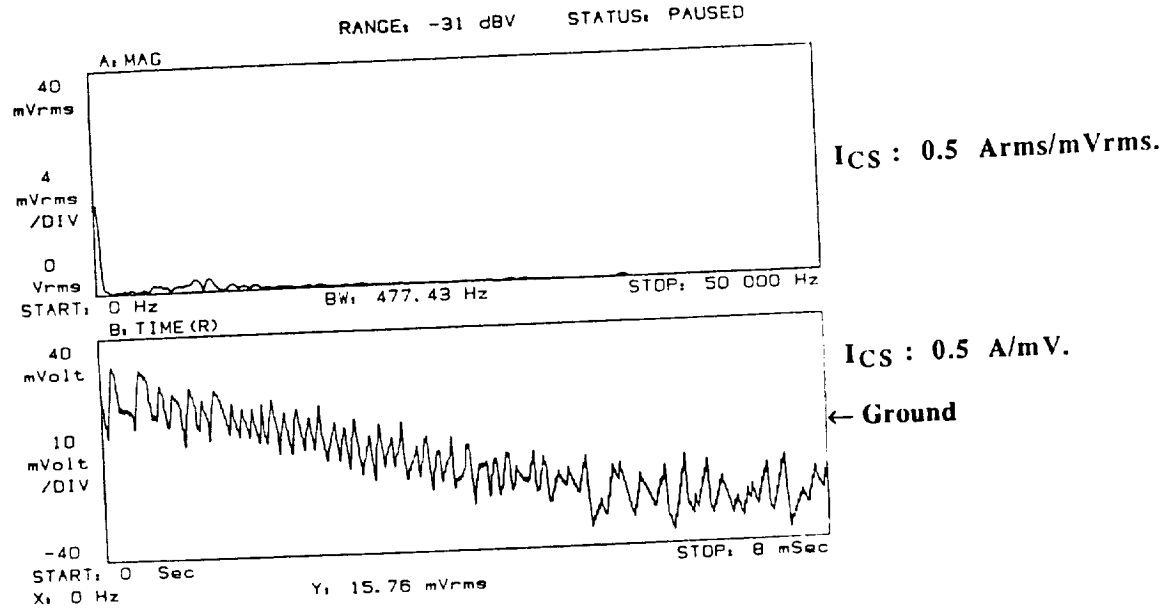


Fig. 5.19. Phase C Source Line Current (Shown in Fig. 5.17, $I_{CS}$) Harmonic Spectrum Over 0-50kHz Range. $I_{CS}$ : 0.5 Arms/mVrms & 0.5 A/mV.

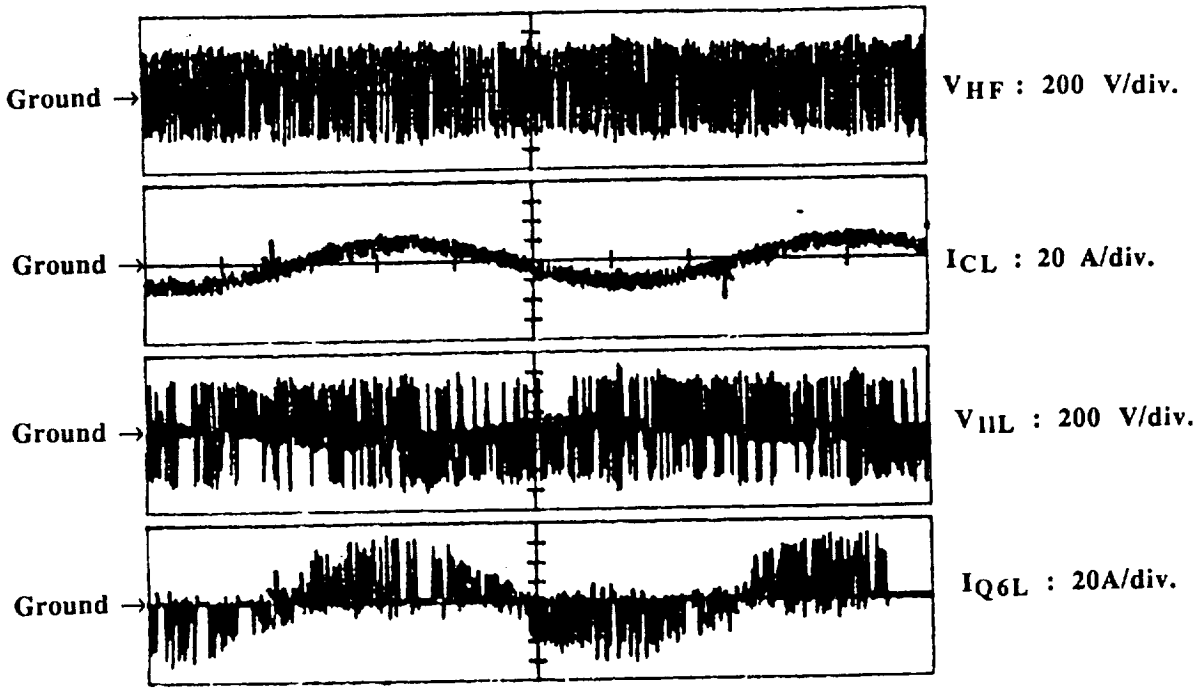


Fig. 5.20. Load (Induction Machine) Voltage and Current Waveforms in Operation. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Phase C Load Current: $I_{CL}$ : 20 A/div. Line to Line Load Voltage: $V_{llL}$ : 200 V/div. $Q_{6L}$ Bilateral Device Current: $I_{Q6L}$ : 20A/div. Time/div: 2 msec.

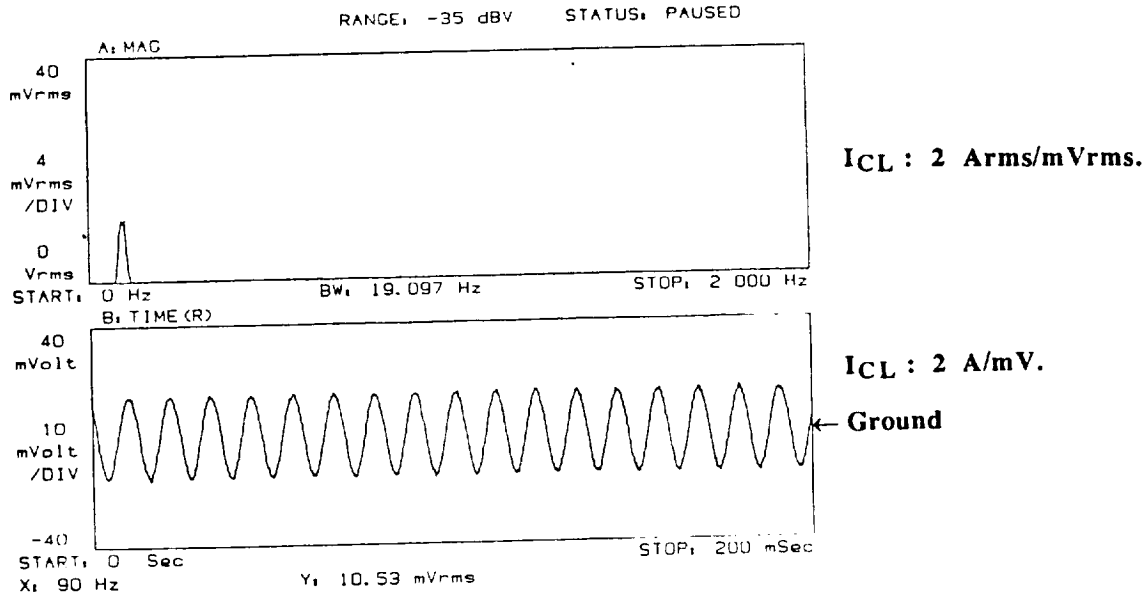


Fig. 5.21. Phase C Load (Induction Machine) Line Current (Shown in Fig. 5.20, $I_{CL}$) Harmonic Spectrum Over 0-2kHz Range. $I_{CL}$ : 2 Arms/mVrms & 2 A/mV.

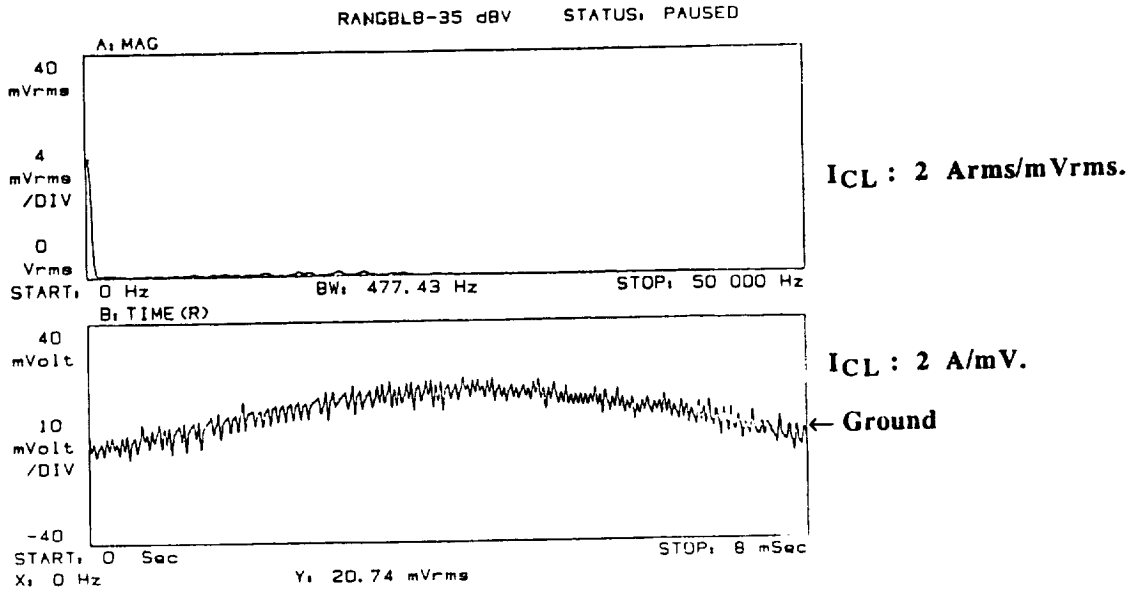


Fig. 5.22. Phase C Load (Induction Machine) Line Current (Shown in Fig. 5.20, $I_{CL}$) Harmonic Spectrum Over 0-50kHz Range. $I_{CL}$ : 2 Arms/mVrms & 2 A/mV.

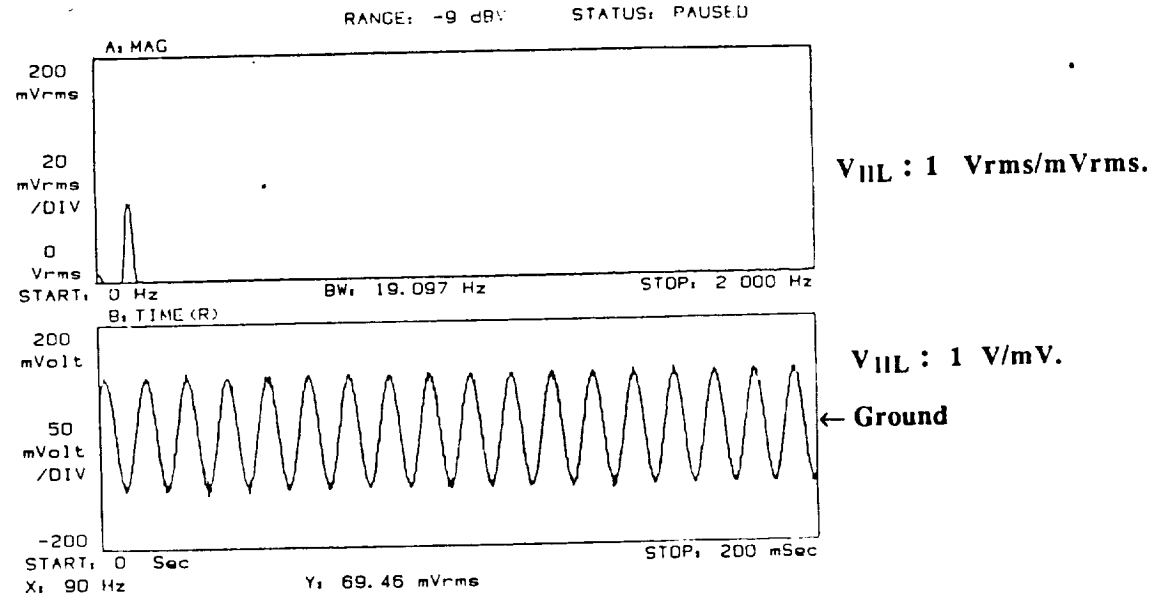


Fig. 5.23. Line to Line Load(Induction Machine) Voltage (Shown in Fig. 5.20, $V_{IIL}$) Harmonic Spectrum Over 0-2kHz Range. $V_{IIL}$ : 1 Vrms/mVrms & 1 V/mV.

amplitudes of the reference currents might not be constant due to the need for power matching process. Whenever there is a need for power matching, the amplitudes of these currents are changed on an instantaneous basis yielding to some extent, harmonic distortion even though it is not too significant.

As opposed to the source side, the load side (induction machine) line to line voltage harmonic spectrum has high harmonic content near the resonant frequency and relatively less harmonic content near the switching frequency. Figures 5.23 and 24 again show the spectrum for two different frequency ranges. The first trace shows the 0-2 kHz range where there are almost no harmonics except within 0-15 Hz range where there is around 10% of the fundamental component. The second figure shows the 0-50 kHz range which covers the large harmonic content near resonant frequency and relatively less harmonic content near the switching frequency. Even though the amplitudes of the harmonics which exist around the resonant frequency look larger than the fundamental component, their effect on the induction machine operation is relatively small because the impedances that they introduce at high frequencies are proportionally high. A 1 mV rms value in Figs. 5.23 and 25 corresponds to 1 V rms of the physical variable. Since the induction machine is operated at constant and rated flux a constant V/f ratio is expected. Figure 5.23 confirms this fact by giving us a 0.771 ratio (69.46 V rms/90 Hz) which is very close to the rated 0.766 ratio (230 V rms/300 Hz). The second figure from the top in Fig. 5.24 shows how this fundamental component at 90 Hz is synthesized from 20 kHz (to be exact 18.25 kHz) high frequency link voltage half cycles.

### 5.3.6 Bilateral Device Stresses with Zero Voltage Switching

Figures 5.25 through 5.34 are meant to show the voltage and current stresses of the bilateral switches during the operation of PDM converters under the same operating conditions previously discussed. The bilateral device Q6 in the load side converter, designated as $Q6_L$, has been selected for this purpose. Figure 5.25 shows high frequency link voltage, 90 Hz load side (induction machine) line current, bilateral device voltage and bilateral device current from the top respectively. The device voltage and current conventions are shown in Fig. 5.2.

Since the device stresses could change depending on the level of the current, Figs. 5.26 through 5.28 shows these stresses for three different current levels. These three figures are basically the magnified views of Fig. 5.25 for three different current levels. The top two traces in these three figures show the high frequency link voltage and the device voltage stress and the bottom two traces show the load side line current and the

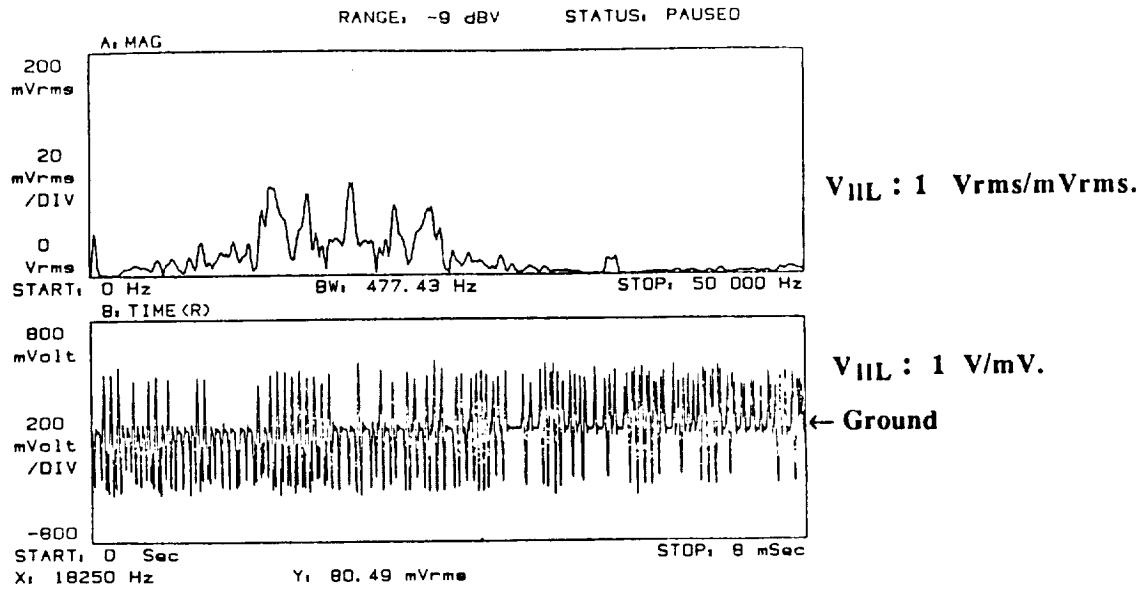


Fig. 5.24. Line to Line Load(Induction Machine) Voltage (Shown in Fig. 5.20, $V_{llL}$) Harmonic Spectrum Over 0-50kHz Range. $V_{llL}$ : 1 Vrms/mVrms & 1 V/mV.

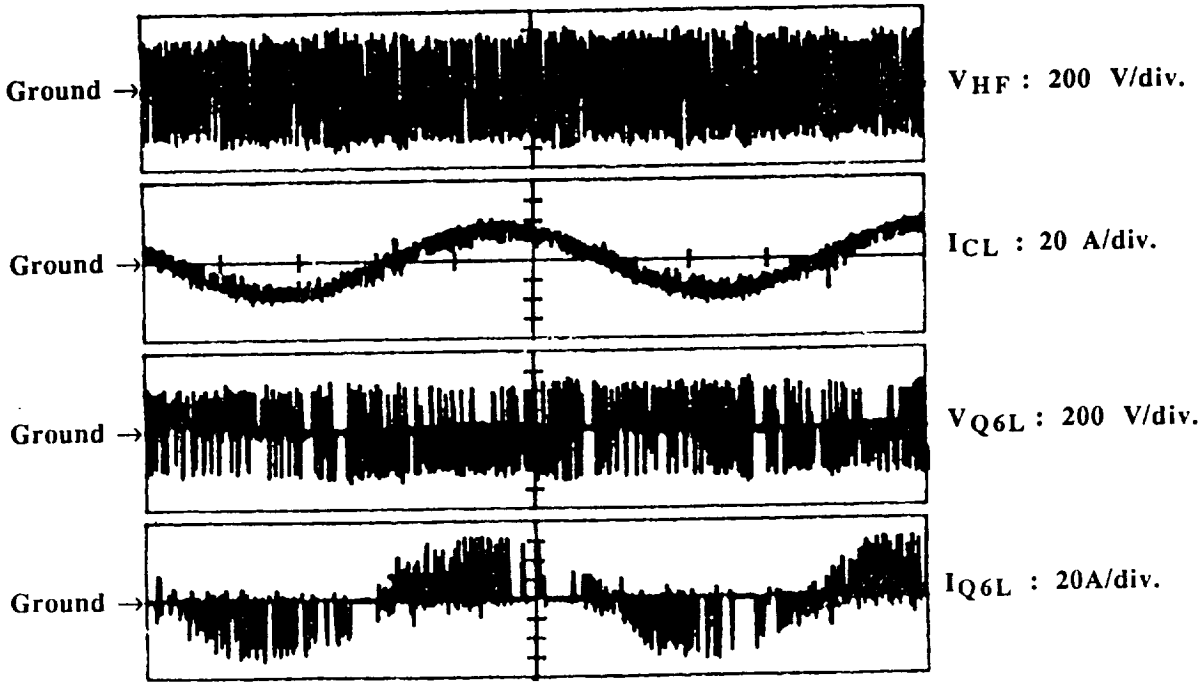


Fig. 5.25. Bilateral Device Voltage And Current Stresses in Operation. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Phase C Load Current: $I_{CL}$ : 20 A/div. $Q_{6L}$ Bilateral Device Voltage: $V_{Q6L}$ : 200 V/div. $Q_{6L}$ Bilateral Device Current: $I_{Q6L}$ : 20A/div. Time/div: 2 msec.

device current stress. As seen from the figures, the spikes in the device currents at the turn-on instants are not dramatic. In Fig. 5.26, when the device carries the pieces of the load line currents of about 40 A peak, it has no more than a 65 A spike at the turn-on instants. In Fig. 5.27, the peak of the spikes actually reduces due to low operating current levels and in Fig. 5.28, a similar observation as in Fig. 5.26 is obtained except that the direction of the device current is negative. As for the bilateral device voltage stresses, the half cycle pieces of the high frequency link voltage is reflected across the bilateral device during turn-offs and the voltage spikes at the turn-off instants do not even reach to 100 V levels in Fig. 5.26 and 28 and they can not be noticed in Fig. 5.27.

Figure 5.29 shows the turn-on and off of bilateral switch $Q6_L$ during the operation of the induction machine. The first trace from the top shows the bilateral device voltage, the second trace shows the collector-emitter voltage of the IGBT inside the bilateral device. The reason that exact rectified half cycles of high frequency link voltage do not appear in this figure is that surge suppressors were placed across the collector-emitter of the IGBT to suppress the excessive voltages and spikes. The third trace from the top shows the gating signal of the device and the fourth trace shows the bilateral device current excluding the snubber capacitor current. Thus, Fig. 5.29 gives an indication of how many half cycles of high frequency link might a bi-directional switch be required to carry in succession. In one case for instance, this device stays in conduction for 20 half cycles of high frequency link. The reader should refer to Chapter 3 for more discussion of this phenomenon.

Figure 5.30 shows the turn-on and off from a different perspective. This figure has been included to illustrate the difference between the bilateral device current which does not include the snubber capacitor current and the device which includes this current. In this figure, the first trace from the top shows the bilateral device voltage. A ringing with small amplitude imposed on this waveform is due to the snubber capacitor voltage discharge and stray inductance effect of the bilateral device during turn-on. The second trace from the top shows the gating signal for the device. The last two traces show the bilateral device currents. The third trace from the top does not include the snubber capacitor current, whereas the fourth trace includes this current. When these two currents are compared it can be seen that the device current which does not include the snubber capacitor current has a much higher peak value for the spike at the turn-on instant. For this particular case, while the peak of the spike for this current reaches 80 A, the peak of the spike for the other device stays at 60 A for a normal load line current operation of around 40 A peak. These spikes at the turn-on instants are again due to the discharge and resetting process of the snubber capacitor voltages. Since the device current stress is related to the current which does not

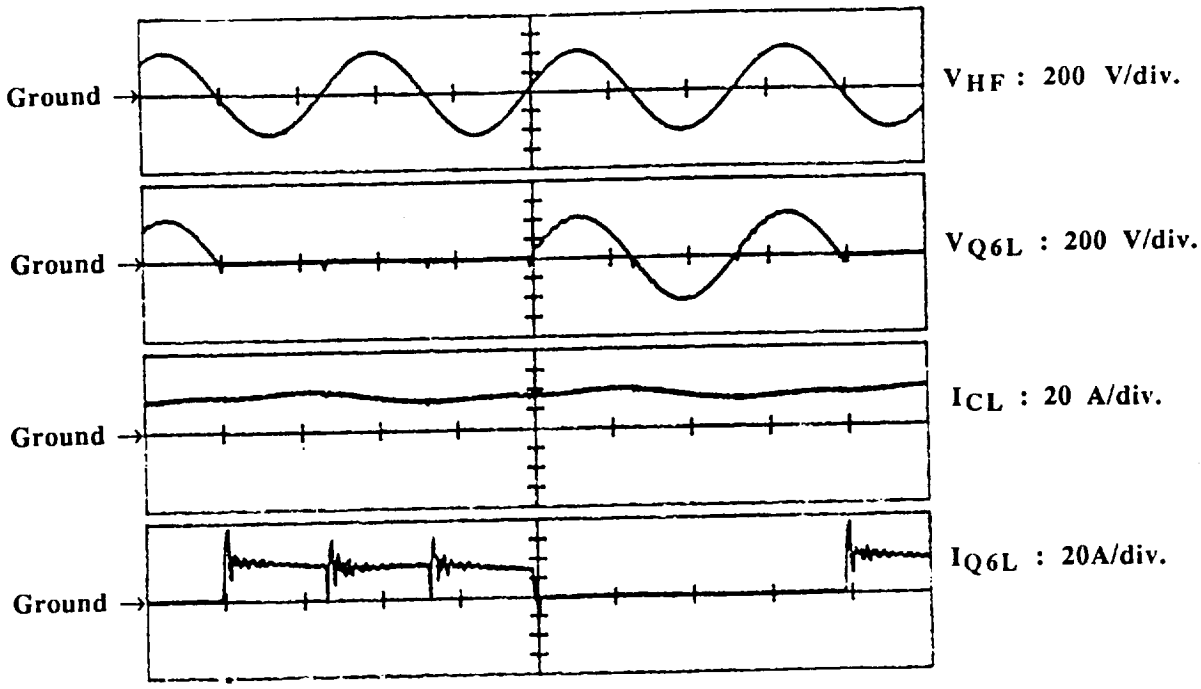


Fig. 5.26. Bilateral Device Voltage And Current Stresses Around Positive Maximum Device Current. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. $Q_{6L}$ Bilateral Device Voltage: $V_{Q6L}$ : 200 V/div. Phase C Load Current: $I_{CL}$ : 20 A/div. $Q_{6L}$ Bilateral Device Current: $I_{Q6L}$ : 20A/div. Time/div: 20 µsec.

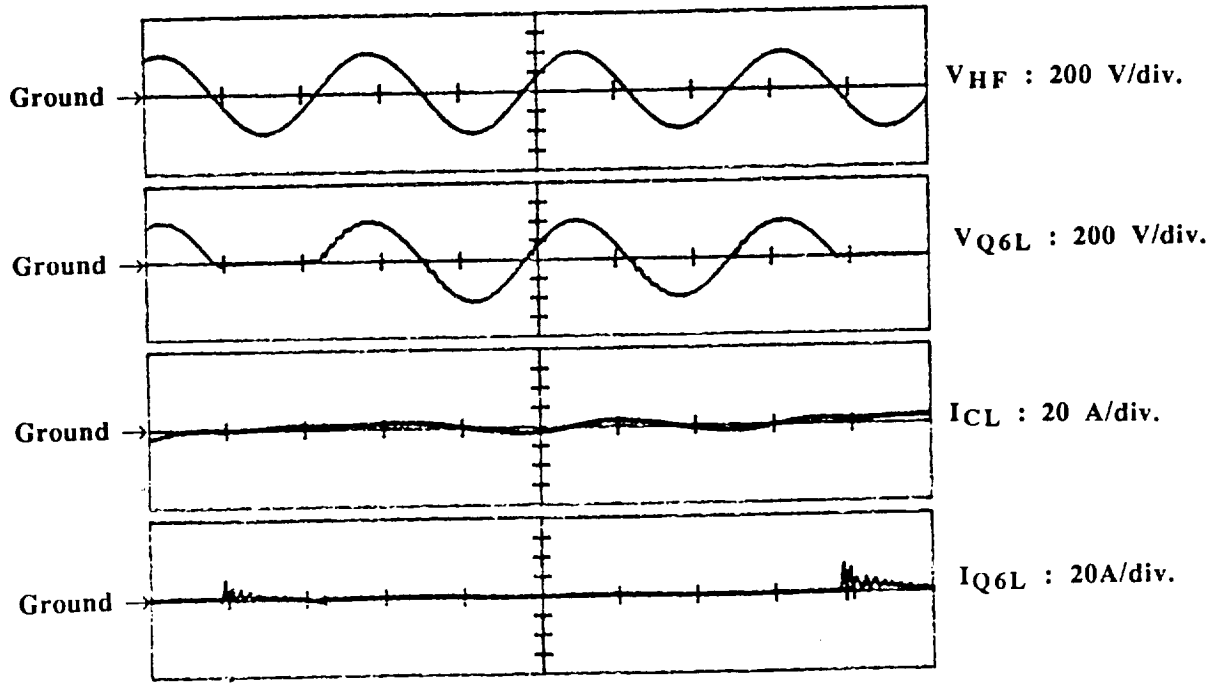


Fig. 5.27. Bilateral Device Voltage And Current Stresses Around Zero Device Current. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. $Q_{6L}$ Bilateral Device Voltage: $V_{Q6L}$ : 200 V/div. Phase C Load Current: $I_{CL}$ : 20 A/div. $Q_{6L}$ Bilateral Device Current: $I_{Q6L}$ : 20A/div. Time/div: 20 µsec.

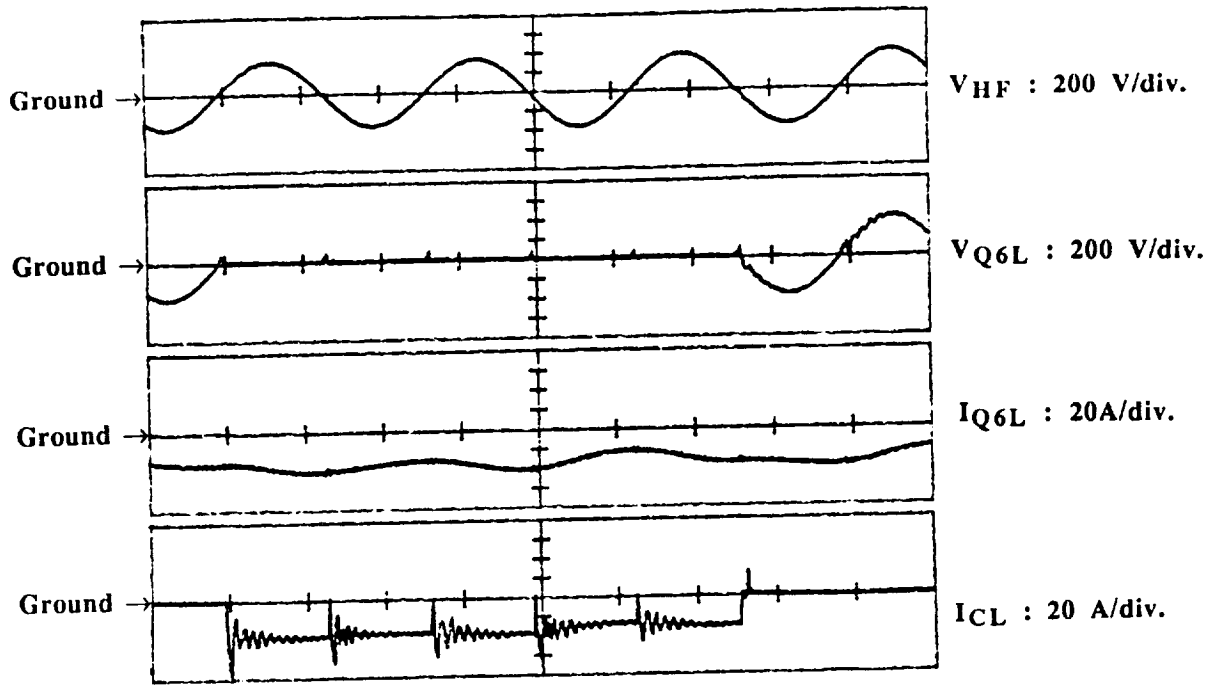


Fig. 5.28. Bilateral Device Voltage And Current Stresses Around Negative Maximum Device Current. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. $Q_{6L}$ Bilateral Device Voltage: $V_{Q6L}$ : 200 V/div. Phase C Load Current: $I_{CL}$ : 20 A/div. $Q_{6L}$ Bilateral Device Current: $I_{Q6L}$ : 20A/div. Time/div: 20 µsec.

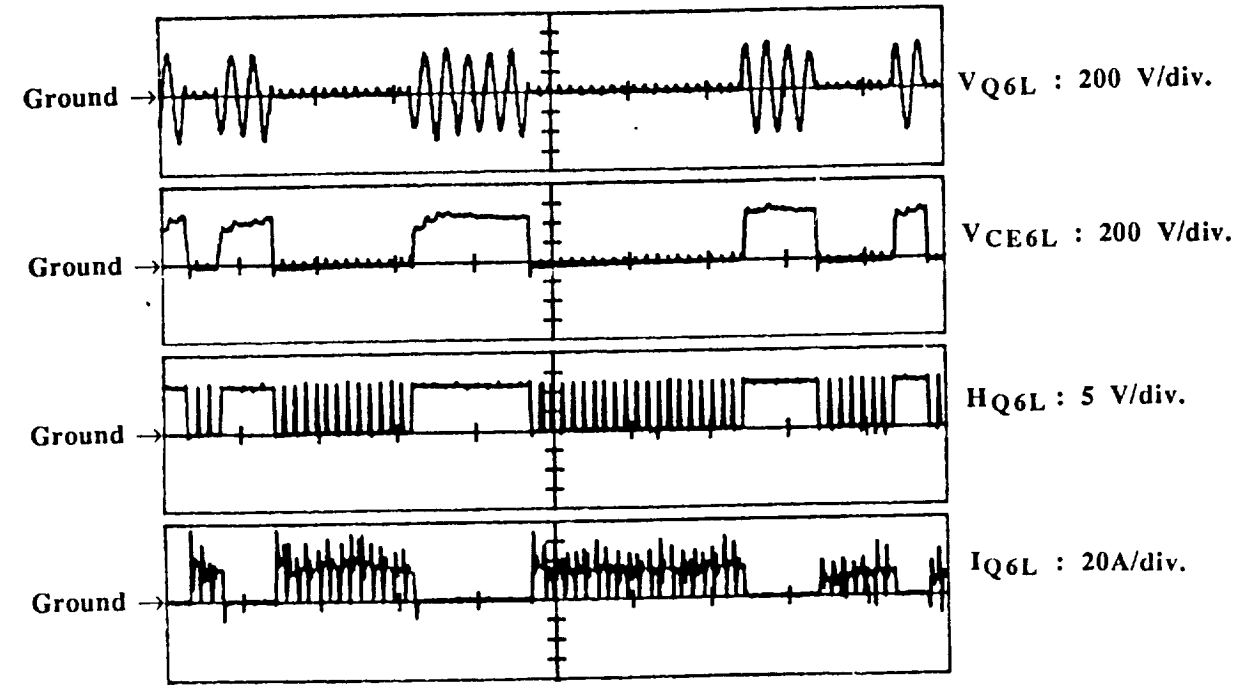


Fig. 5.29. Unilateral Device (IGBT) Safe Operating Area Observation Waveforms. (For more Information See Section 3.2.4) From the Top Respectively; $Q_{6L}$ Bilateral Device Voltage: $V_{Q6L}$ : 200 V/div. Unilateral Device Collector Emitter Voltage : $V_{CE6L}$ : 200 V/div. Gating Logic Signal for Bilateral Device $Q_{6L}$: $H_{Q6L}$ : 5 V/div. $Q_{6L}$ Bilateral Device Current: $I_{Q6L}$ : 20A/div. Time/div: 200 µsec.

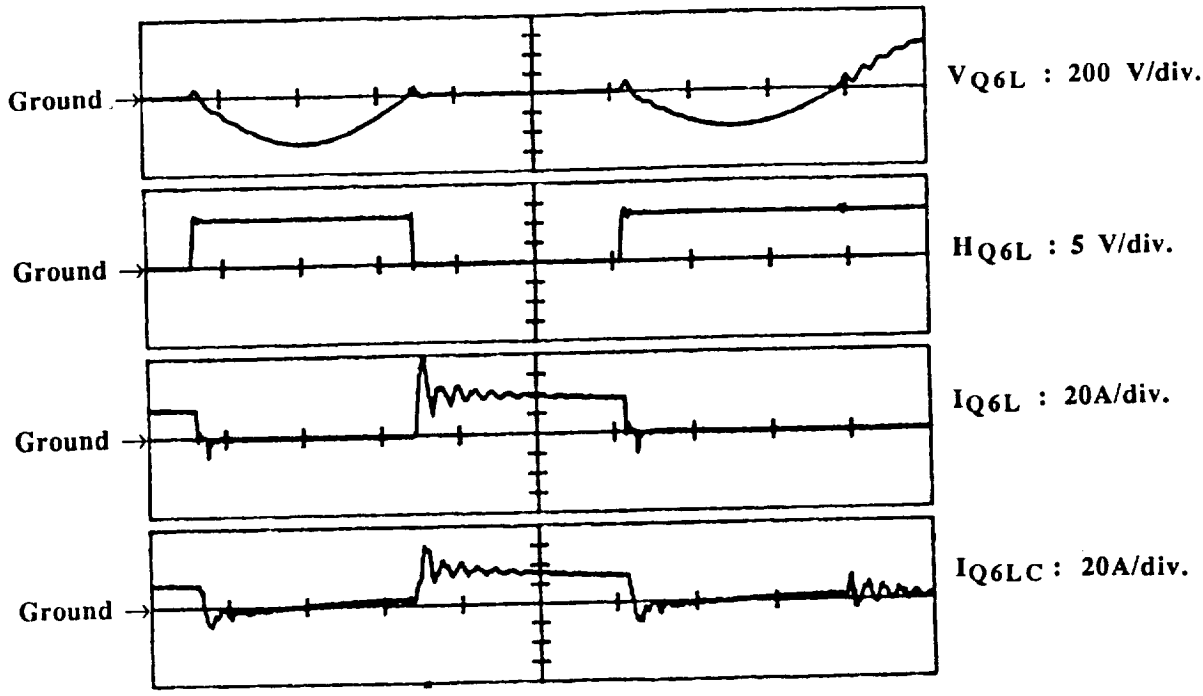


Fig. 5.30. Turn On and Off of Bilateral Device at Zero Crossings of HF Link Voltage. From the Top Respectively; $Q_{6L}$ Bilateral Device Voltage: $V_{Q6L}$ : 200 V/div. Gating Logic Signal for Bilateral Device $Q_{6L}$: $H_{Q6L}$ : 5 V/div. $Q_{6L}$ Bilateral Device Current: $I_{Q6L}$ : 20A/div. Bilateral Device Current Including the Snubber Capacitor Current: $I_{Q6LC}$ : 20A/div. Time/div: 10 µsec.

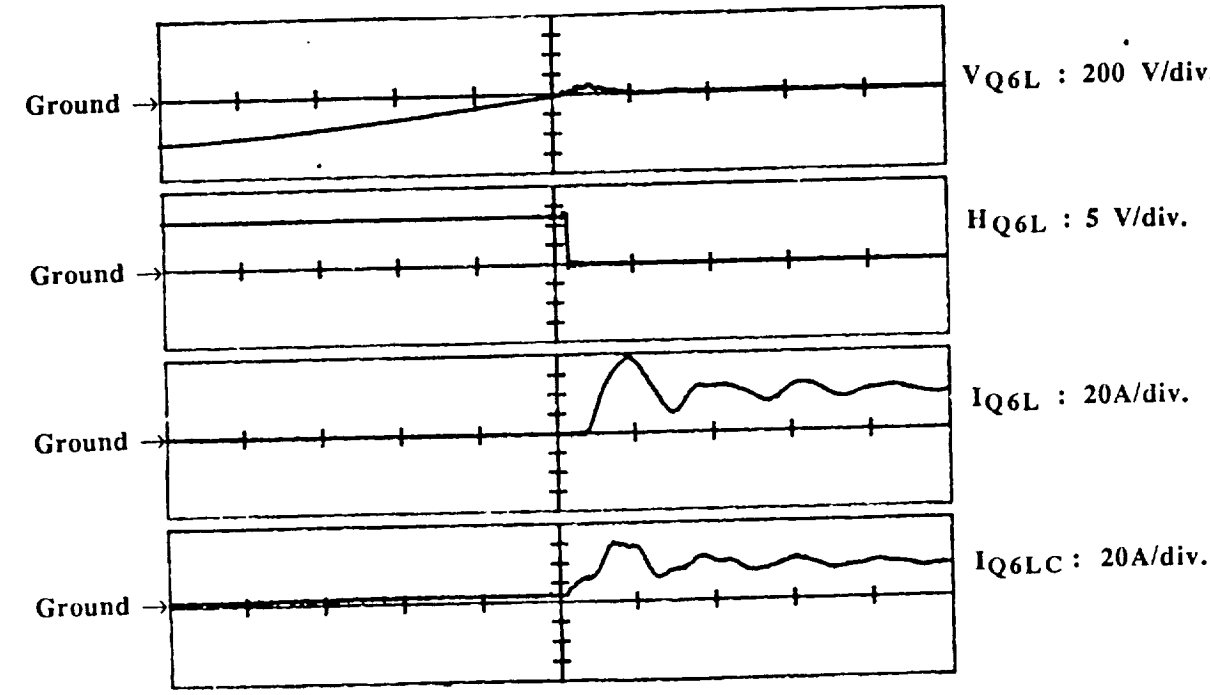


Fig. 5.31. Magnified View of Turn On of Bilateral Device. From the Top Respectively; $Q_{6L}$ Bilateral Device Voltage: $V_{Q6L}$ : 200 V/div. Gating Logic Signal for Bilateral Device $Q_{6L}$: $H_{Q6L}$ : 5 V/div. $Q_{6L}$ Bilateral Device Current: $I_{Q6L}$ : 20A/div. Bilateral Device Current Including the Snubber Capacitor Current: $I_{Q6LC}$ : 20A/div. Time/div: 2 µsec.

include snubber capacitor current, a 80 A spike peak should be assumed for device current stress in this particular case.

It is useful to now consider the turn-on and turn-off events individually from a much closer perspective through magnified views of Fig. 5.30. For this purpose, Fig. 5.31 shows the turn-on of the bilateral device. When the turn-on command is given to device $Q6_L$, the device current which does not include the snubber capacitor current does not rise immediately but begins to rise around 0.4 μsec later. This result is a typical turn-on time delay for this IGBT. On the other hand, the current which includes the capacitor current begins to rise even before the turn-on command is given. This is due to the fact that the turn-off process of the complementary switch, $Q3_L$, which is in the same branch with $Q6_L$ has already begun. This early rise in the snubber capacitor current raises the snubber capacitor voltage to around 100 V for this particular case as seen in the first trace from the top. As soon as the device starts to turn-on, snubber capacitor voltage starts to discharge through this device and the bilateral device voltage (snubber capacitor voltage) drops to its forward voltage drop levels. This discharge of the snubber capacitor voltage through the device turning on causes current spikes as mentioned earlier. The ringing seen in the current waveforms after their peak at turn-on are due to the resonance between the snubber capacitor and the stray inductance of the bilateral switch configuration. Overall, Fig. 5.31 reveals a typical turn-on time which is 0.5 μsec for the IGBT used in the bilateral device configuration.

Figure 5.32 illustrates a magnified view of the turn-off process of bilateral device. Once the turn-off command is given to $Q6_L$, the device current which does not include snubber capacitor current does not start to drop until approximately 0.5 μsec passes and then drops to zero almost instantaneously (less than 0.1 μsec) as can be seen in the third trace from the top. The device current which includes the snubber capacitor current, fourth trace from the top, begins to drop linearly almost 0.25 μsec after the turn-off command is given. Since the load side current can be assumed constant within a 2 μsec range, when the both current levels drops below the load side current level with the complementary device still not turned on, the remainder of the load current raises the device (snubber capacitor) voltage to around 100 V in a positive direction as seen in first trace from the top. Since this device is kept off for the incoming half cycle (with turned-on complementary device), the high frequency link voltage is reflected across this device.

It can be observed that when the bilateral device voltage is positive with incoming high frequency link voltage half cycle as in Fig. 5.33, a spike in the device current does not occur at turn-off but if the device voltage is negative, then a negative spike occurs as shown in Fig. 5.32. The reason for this phenomenon is that the positively charged snubber

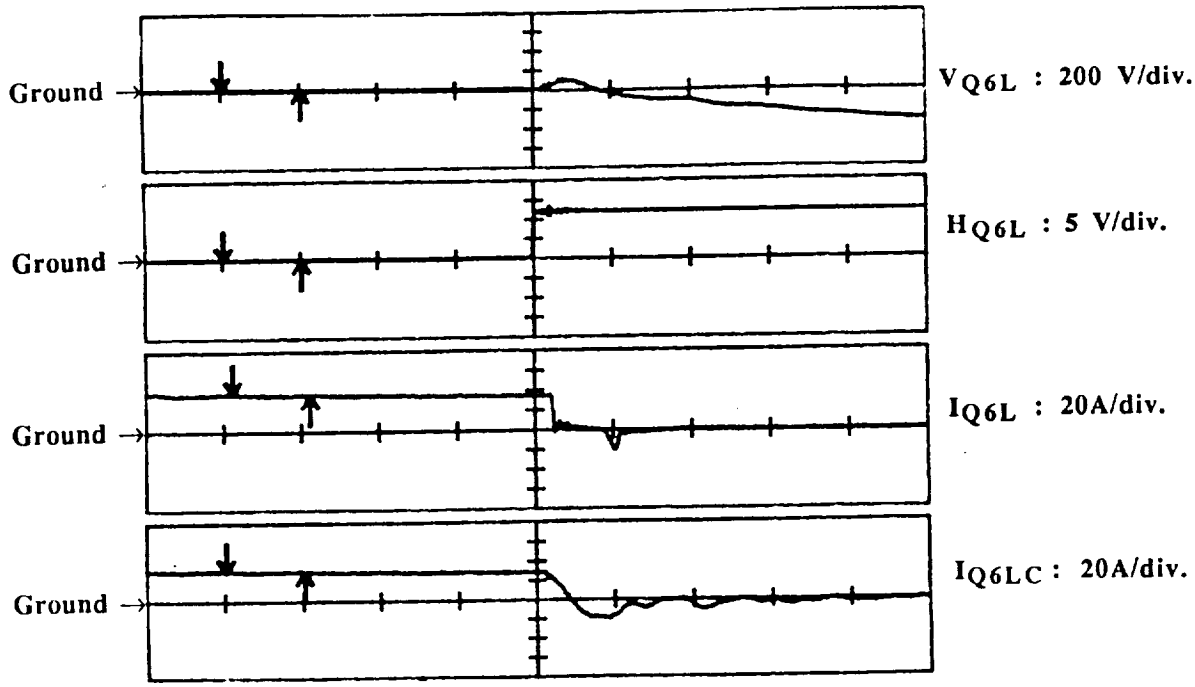


Fig. 5.32. Magnified View of Turn Off of Bilateral Device. From the Top Respectively; $Q_{6L}$ Bilateral Device Voltage: $V_{Q6L}$ : 200 V/div. Gating Logic Signal for Bilateral Device $Q_{6L}$: $H_{Q6L}$ : 5 V/div. $Q_{6L}$ Bilateral Device Current: $I_{Q6L}$ : 20A/div. Bilateral Device Current Including the Snubber Capacitor Current: $I_{Q6LC}$ : 20A/div. Time/div: 2 µsec.

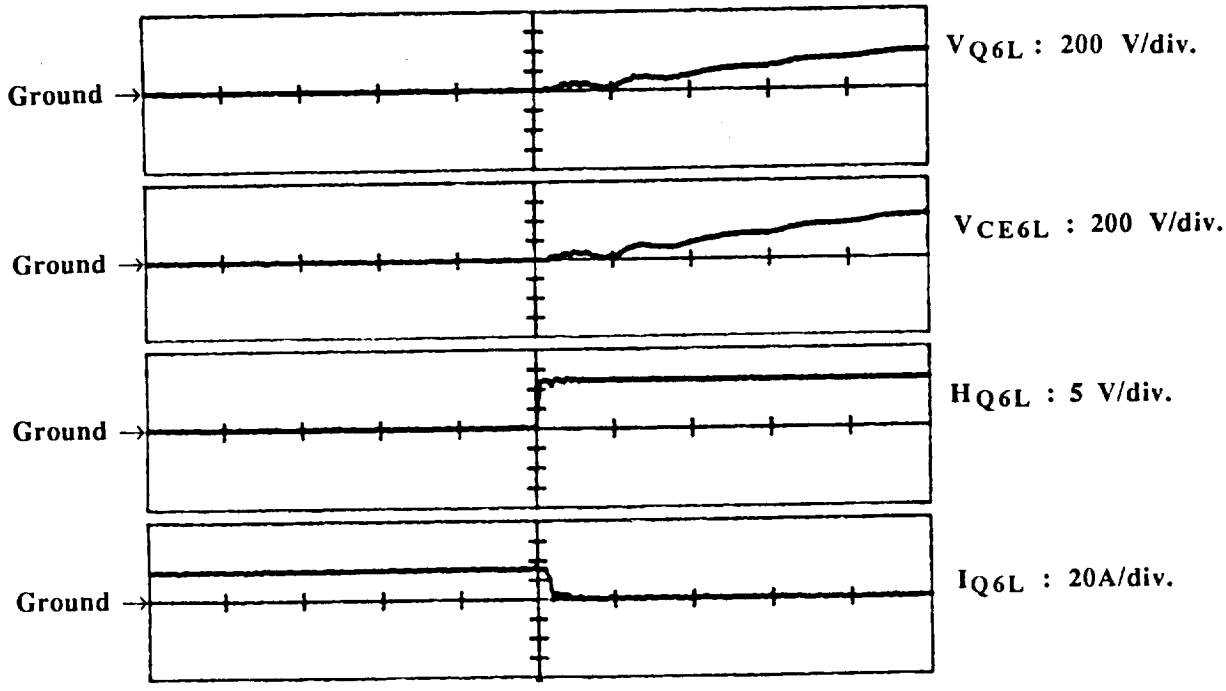


Fig. 5.33. Another Magnified View of Turn Off of Bilateral Device. From the Top Respectively; $Q_{6L}$ Bilateral Device Voltage: $V_{Q6L}$ : 200 V/div. Unilateral Device Collector Emitter Voltage : $V_{CE6L}$ : 200 V/div. Gating Logic Signal for Bilateral Device $Q_{6L}$: $H_{Q6L}$ : 5 V/div. $Q_{6L}$ Bilateral Device Current : $I_{Q6L}$ : 20A/div. Time/div: 2 µsec.

capacitor voltage does not have to discharge for positive link voltages but must discharge for negative link voltages.

Figure 5.34 shows a complete picture of the complementary operation of the two switches in the same branch of the PDM converter bridge. The device currents in these figures include the effect of the snubber capacitor currents. This figure clearly shows the relationship between the instant the turn-off command is given to one device, Q6L, and the delay of the turn-on command to its complement, Q3L. It can be noted from the figure that the turn-on command is given almost 0.4 μsec after the turn-off command is given. Current sharing between the two devices is clearly shown in this picture. The summation of these two currents yields the load side low frequency current which is almost constant within the time region shown in the picture.

### 5.3.7 Current Regulation of Induction Machine

Pictured in Figs. 5.35 and 36 is start and stop of the induction machine controlled by an Indirect Field Orientation Controller for the same operating conditions as described earlier. In particular, the controller commands the induction machine to operate at 100% rated flux and 40% rated torque in the torque regulation mode. Therefore, depending on the position of the rotor, constant amplitude 3Ø reference currents are generated. In Fig. 5.35, the start command is shown in the first trace from the top. The phase A reference current generated by the FOC is shown in the second trace from the top. As can be seen from the figure, the amplitude of this current is a constant value of about 35 A. Machine operation begins at low frequencies and as the speed of the machine increases, the command frequency is also increased until the desired torque point is reached. The third figure from the top shows the line to line induction machine voltage synthesized from high frequency link half cycles. For rated, constant flux operation, the V/f ratio should be kept constant, the line to line induction machine voltage synthesized from high frequency link half cycles should have low rms values for low frequency operation. Because the peak link voltage is essentially constant at 511 V, it is necessary to select both polarities of the link voltage to synthesize low rms value voltages for low frequency operation. Hence, the frequency and rms value of the line to line machine voltage is not immediately apparent from this picture. As the machine frequency reaches its rated frequency these quantities becomes more clear. The last trace from the top shows the actual induction machine current. A comparison of the reference and real currents shows good agreement. The real current indicates that there is around 20 A peak to peak ripple current imposed on the low frequency current.

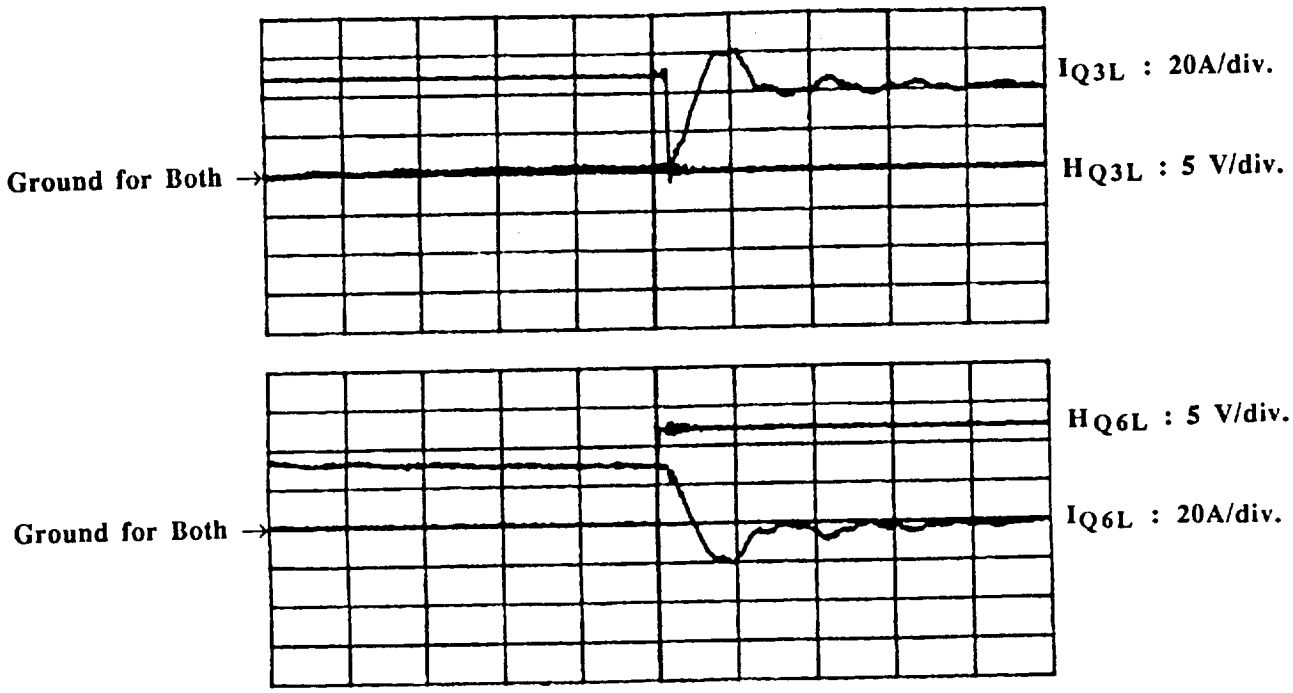


Fig. 5.34. Turn On and Off of Complementary Operating Switches. Top Two Figures; Gating Logic Signal for Bilateral Device $Q_{3L}$: $H_{Q3L}$ : 5 V/div. $Q_{3L}$ Bilateral Device Current : $I_{Q3L}$ : 20A/div. Bottom Two Figures; Gating Logic Signal for Bilateral Device $Q_{6L}$: $H_{Q6L}$ : 5 V/div. $Q_{6L}$ Bilateral Device Current: $I_{Q6L}$ : 20A/div. Time/div: 2 μsec.

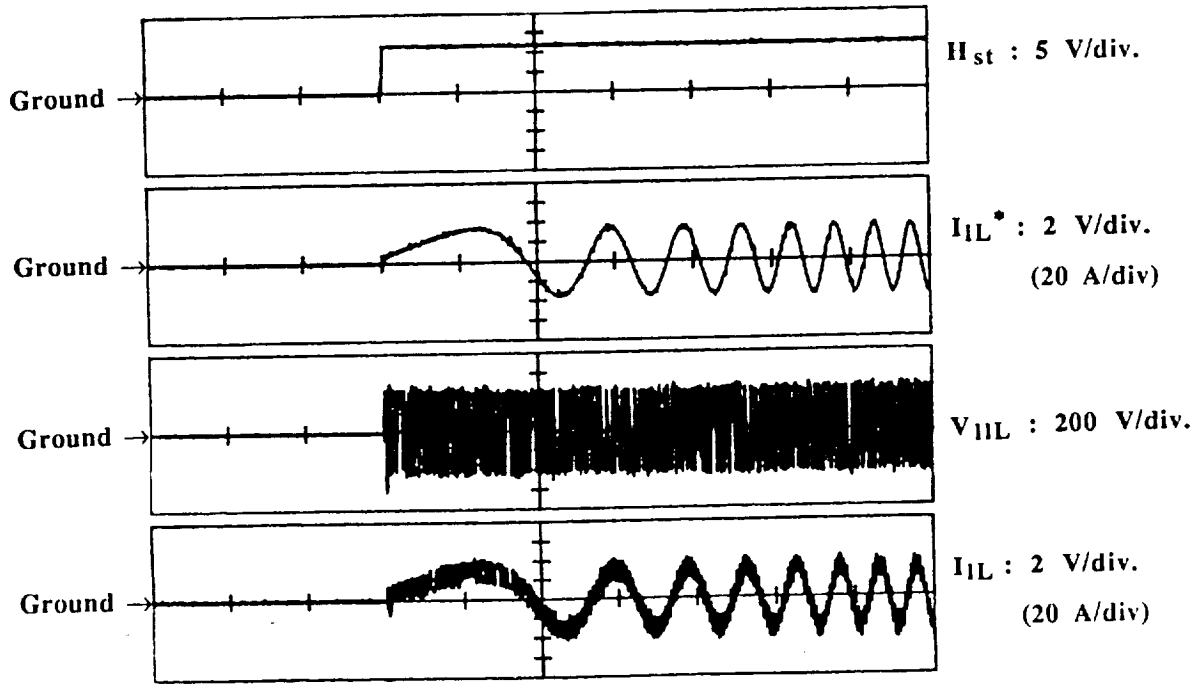


Fig. 5.35. Start of Field Oriented Controlled Induction Machine via PDM Converter. From the Top Respectively; Start Command: $H_{st}$ : 5 V/div. Induction Machine (Load) Line Current Command Reference: $I_{lL}^*$ : 2 V/div (20 A/div). Induction Machine Line to Line Voltage: $V_{llL}$ : 200 V/div. Induction Machine Line Current: $I_{lL}$ : 2 V/div (20 A/div). Time/div: 200 msec.

Current braking of the induction machine is shown in Fig. 5.36. As soon as the stop command is given, in the first trace from the top, the reference currents are set to zero. The process of setting the Phase A reference current to zero is shown in the second trace from the top. The motor currents immediately follow their reference and the induction machine is demagnetized rapidly. Only the ripple currents remain which imposes some voltage spikes on the line to line voltages. The line to line induction machine voltage is shown in the third trace from the top and the phase A measured current is shown in the last trace from the top.

### 5.3.7 Operation of the Induction Machine at Desired Load Point

Figure 5.37 shows the waveforms of steady state operation of the induction machine at 100% rated flux, 40% rated torque and 90 Hz operating frequency. The first trace from the top shows the line to line induction machine voltage. The harmonic spectrum of this waveform over two different frequency ranges is given in Figs. 5.38 and 39. A detailed discussion about the harmonic content of this waveform can be found in Section 5.2. The reference and real induction machine line currents for phase-A are shown with last two traces respectively. At this particular operating point, the reference current has an amplitude of essentially 35 A. This value actually can be calculated by taking the square root of the sum of the squared flux and torque component current commands. As given in Section 5.2, the rated flux and torque component currents for this induction machine are 30.22 A peak and 33.20 A peak respectively. Therefore, phase-A induction machine line current peak is calculated as

$$I_{AS} = \sqrt{(100\% \times I_{dsrated})^2 + (40\% \times I_{qsrated})^2} = \sqrt{(30.22)^2 + (0.40 \times 33.20)^2} = 33.01 \text{ A peak}$$

The harmonic spectrum of the measured induction machine current waveform over two different frequency ranges is given in Figs. 5.36 and 37. A detailed discussion about the harmonic content of this waveform can again be found in Section 5.2.

## 5.4 Four Quadrant Operation of Induction Machine

### 5.4.1 Response of the Induction Machine to Torque Reversal Commands

Figure 5.38 shows the response of the system to a step change in the torque command. The load for the induction machine is a DC-Dynamometer demanding or

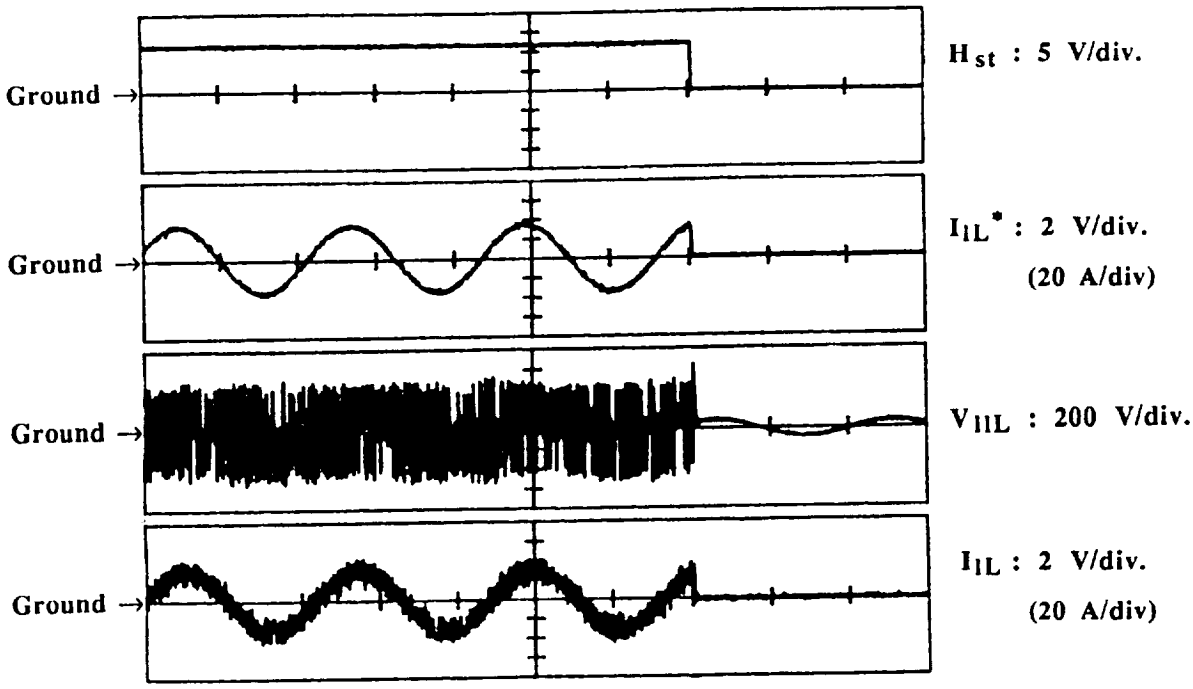


Fig. 5.36. Stop of Field Oriented Controlled Induction Machine via PDM Converter. From the Top Respectively; Stop Command: $H_{st}$ : 5 V/div. Induction Machine (Load) Line Current Command Reference: $I_{lL}^*$ : 2 V/div (20 A/div). Induction Machine Line to Line Voltage: $V_{llL}$ : 200 V/div. Induction Machine Line Current: $I_{lL}$ : 2 V/div (20 A/div). Time/div: 5 msec.

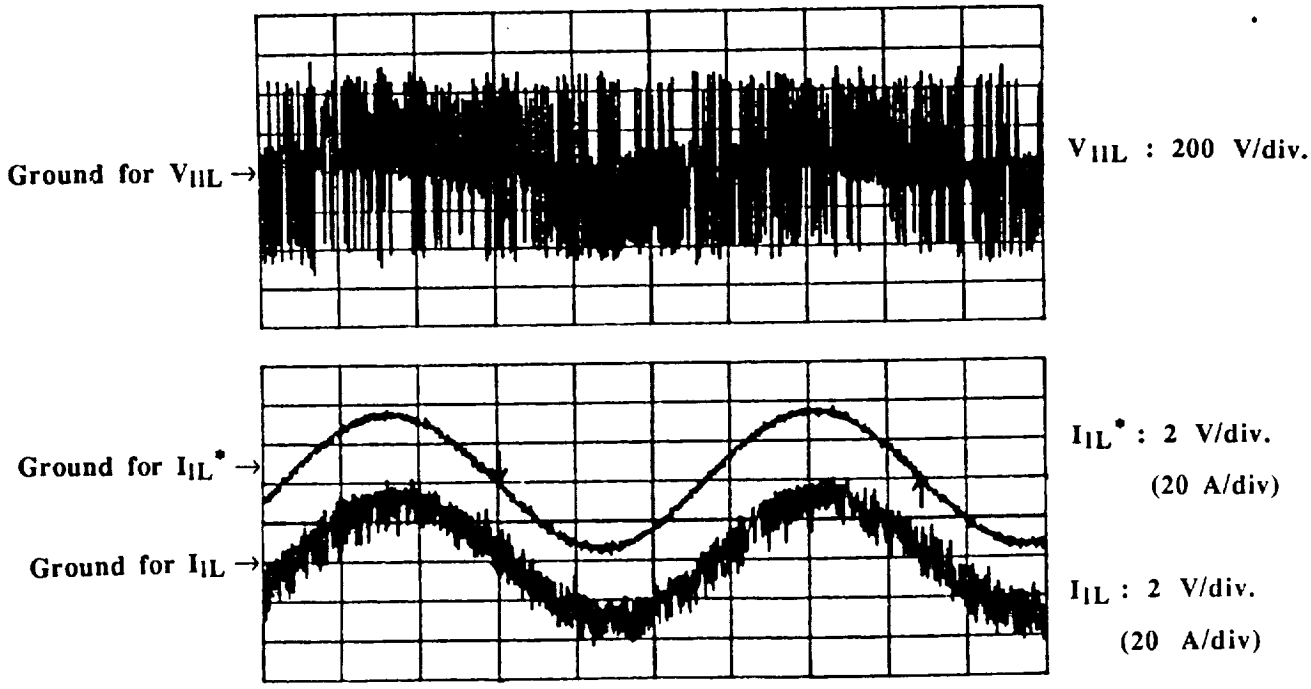


Fig. 5.37. Current Regulation of Induction Machine at 90Hz Operation. From the Top Respectively; Induction Machine (Load) Line to Line Voltage: $V_{llL}$ : 200 V/div. Induction Machine Line Current Command Reference: $I_{lL}^*$ : 2 V/div (20 A/div). Induction Machine Line Current: $I_{lL}$ : 2 V/div (20 A/div). Time/div: 2 msec.

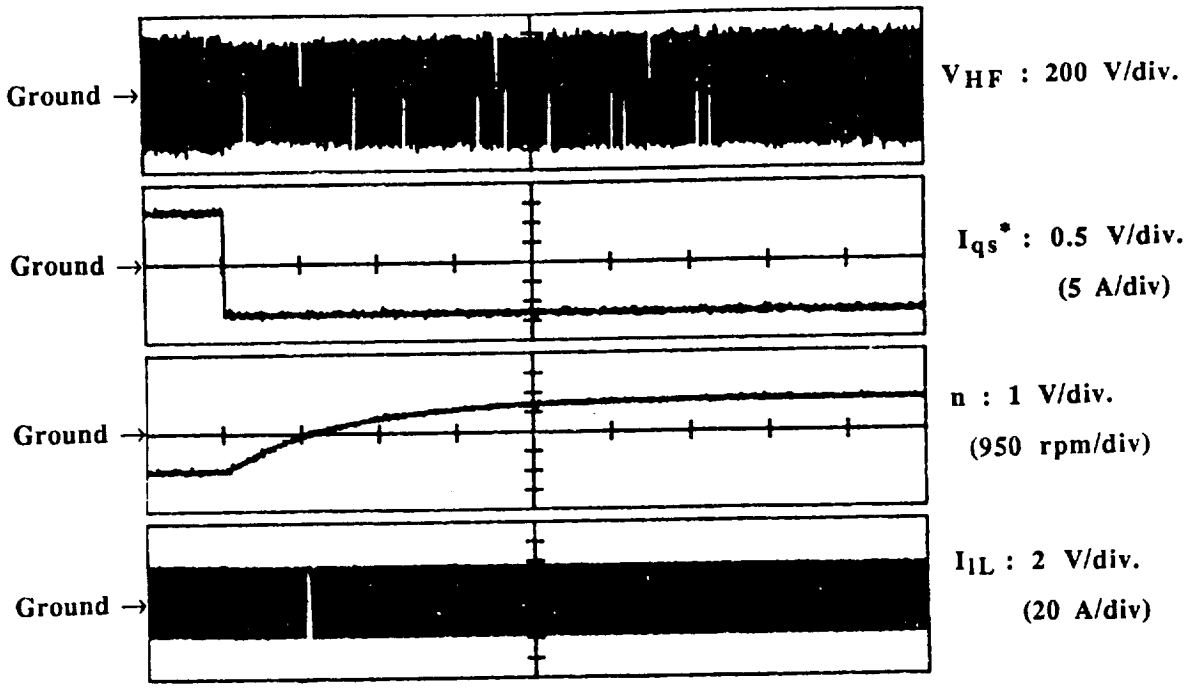


Fig. 5.38. Torque Reversal of Induction Machine Under Torque Regulation Mode. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Torque Component Current Command: $I_{qs}^*$ : 0.5 V/div (5 A/div). Speed of the Induction Machine: n : 1 V/div (950 rpm/div). Induction Machine Line Current: $I_{lL}$ : 2 V/div (20 A/div). Time/div: 5 sec.

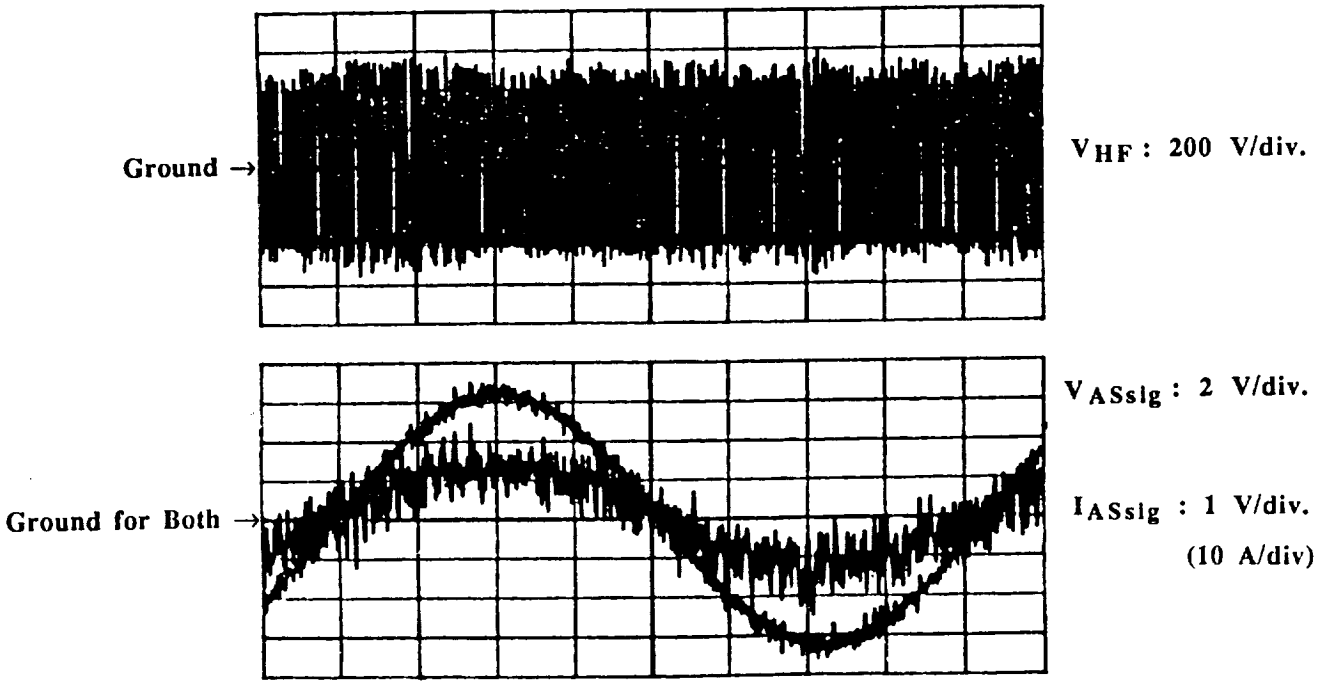


Fig. 5.39. Unity Power Factor (+1) Operation of the Source while the Induction Machine is in Motoring Mode of Operation. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Phase A Line to Neutral Source Voltage Signal: $V_{ASsig}$ : 2 V/div. Phase A Source Line Current Signal: $I_{ASsig}$ : 1 V/div (10 A/div). Time/div: 2 msec.

supplying 40% torque from the induction machine. The speed command of the DC motor is set at 90 Hz. The first trace from the top shows the high frequency link voltage, the second shows the torque command of the induction machine. The third trace from the top shows the speed and the fourth shows the line current of the induction machine. Initially, the speed of the machine is operating at around 1800 rpm CCW.

As soon as the polarity of the torque command is reversed, the peak link voltage reduces slightly because the machine begins to regenerate. The speed of the induction machine reduces, changes its direction and increases in the other direction until it reaches the desired torque operating point in the reverse direction. This causes the induction machine to change its speed from around 1800 rpm CCW to around 1800 rpm CW.

In order to evaluate what is happening to the source side quantities before and after the torque reversal, Figs. 5.39 and 5.40 are presented. Figure 5.39 illustrates unity power factor operation of the source while the machine is operating at 1800 rpm CCW at 40% torque and rated flux. This figure is taken before the torque reversal takes place. Figure 5.40 shows the transient behavior of the source side line current after the torque reversal command is given. Since the induction machine goes into the regenerative mode, the required power from the source side reduces. Although the amplitude of the source side line current reduces to very low values as shown in Fig. 5.40, the source does not go into regenerative operation because the power generated by the induction machine during its regenerative operation is spent on meeting the losses of the system.

### 5.4.2 Speed Reversal Under No Load and Four Quadrant Operation

Figure 5.41 shows a speed reversal under no load in the speed regulation mode. In this case the torque command is self adjusted by the speed controller to operate at the desired speed. The second trace from the top shows the torque command and the third trace shows the speed of the induction machine. Before the speed reversal command is given, the induction machine operates at around 1800 rpm CW with a small negative torque command to meet only the losses of the induction machine and the DC-Dynamometer coupled to the induction machine. This motoring mode of operation can be denoted as the first quadrant of operation with positive torque (negative torque command in the figure) and positive speed. When the speed reversal command is given, the torque command jumps from its small negative value to its positive limit which is set for 40% of rated torque. With the torque polarity changed, the speed stays in the same direction until it eventually reduces and changes its direction. Hence, the second quadrant of operation is entered corresponding to a regenerative mode with negative torque (positive torque command in the

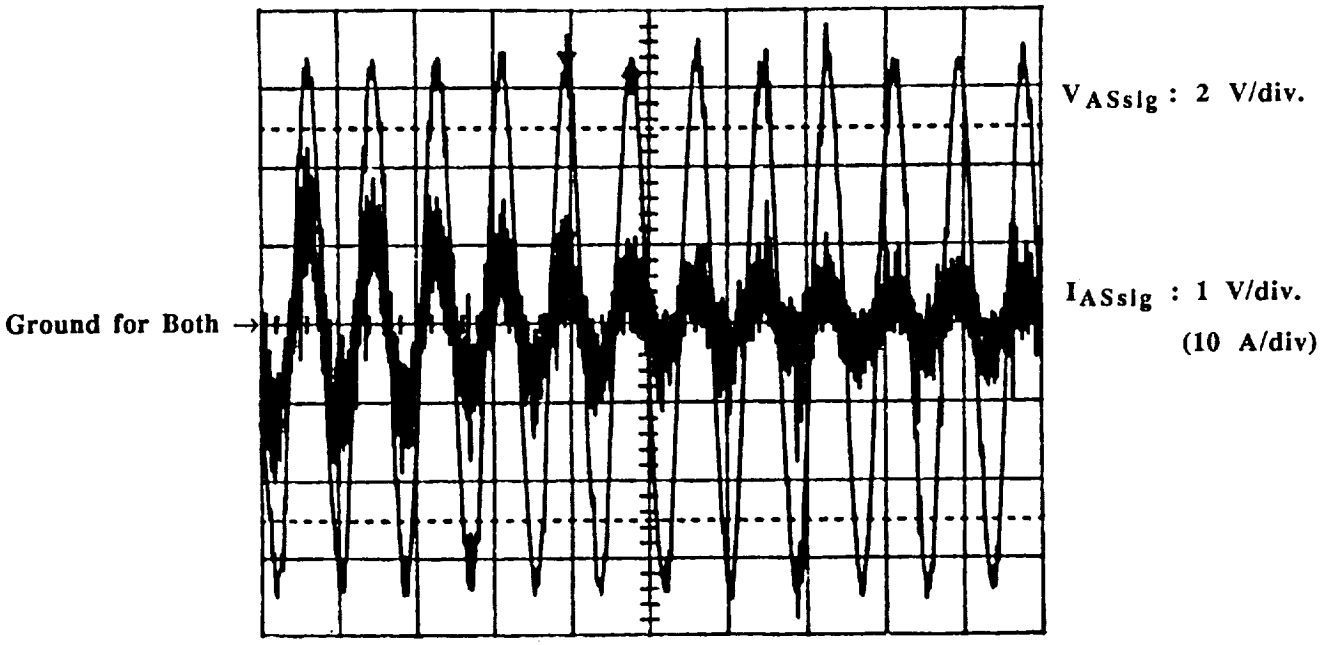


Fig. 5.40. Unity Power Factor (+1) Operation of the Source while the Induction Machine is in Regenerating Mode of Operation. NOTE: Since Regenerated Power is Low and is Dissipated as Losses, Source is Operating Still With +1 Unity Power Factor. From the Top Respectively; Phase A Line to Neutral Source Voltage Signal: $V_{ASsig}$ : 2 V/div. Phase A Source Line Current Signal: $I_{ASsig}$ : 1 V/div (10 A/div). Time/div: 20 msec.

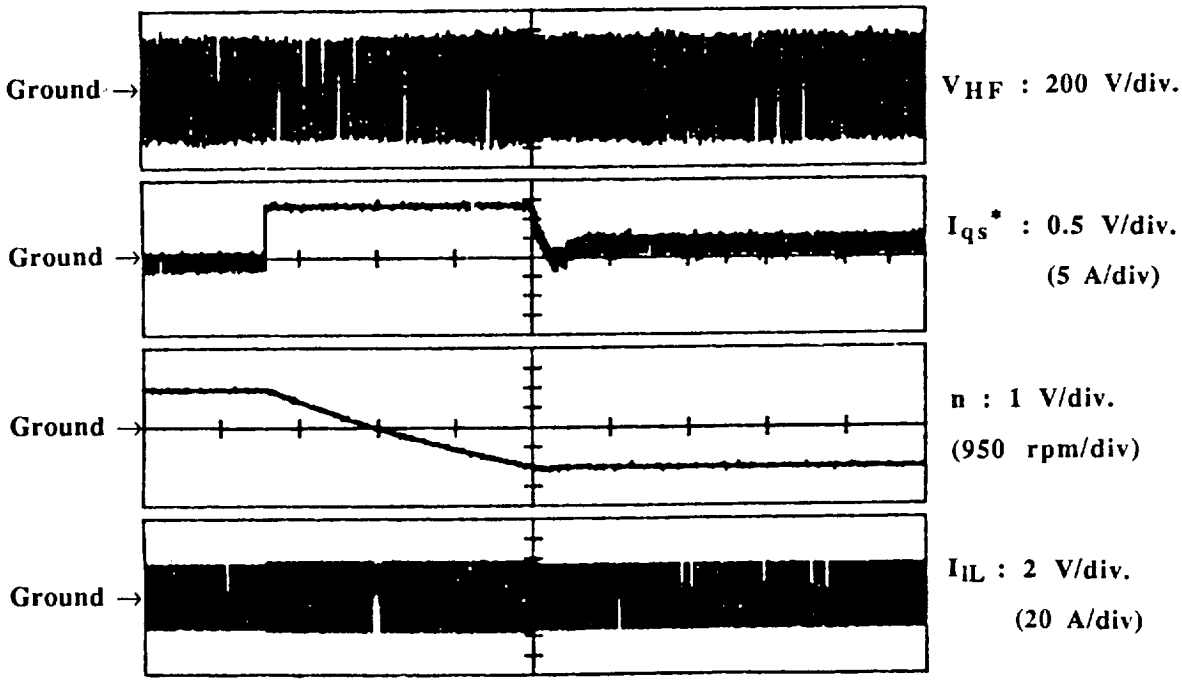


Fig. 5.41. Speed Reversal of Induction Machine Under No Load and in Speed Regulation Mode. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Torque Component Current Command: $I_{qs}^*$ : 0.5 V/div (5 A/div). Speed of the Induction Machine: n : 1 V/div (950 rpm/div). Induction Machine Line Current: $I_{IL}$ : 2 V/div (20 A/div). Time/div: 5 sec.

figure) and positive speed. As soon as the speed changes its direction, a second motoring mode is entered, the third quadrant of operation involving negative torque (positive torque command in the figure) and negative speed. When the speed reaches its final destination which is basically the negative of the initial speed, 1800 rpm CCW, the PI controller reduces the torque command from its positive limit to a small positive value after an overshoot to meet only the losses and the inertia since the DC machine is essentially unloaded. During the overshoot period, the torque command assumes a small negative value, and in doing so, enters the fourth quadrant of operation in regeneration mode involving positive torque (negative torque command in the figure) and negative speed. The first trace from the top in Fig. 5.41 shows the link voltage and the last trace shows the induction machine phase-A line current. The time scale in Fig. 5.41 does not allow viewing the phase reversal of the induction machine line current. To view phase reversal, a magnified view of this figure around zero speed is given as Fig. 5.42.

Figure 5.43 and 5.44 shows the speed reversal under no load this time from 1800 rpm CCW to 1800 rpm CW. Similar reasoning and four quadrant coverage applies also to this case.

### 5.4.3 Speed Reversal Under Load

Figures 5.45 is given to show speed reversal under load in speed regulation mode. The load torque is set to the 40% of the induction machine rated torque. That is why the torque command values before and after the speed reversal command is given exactly corresponds to 40% rated torque operation in either direction. Figure 5.45 shows the speed reversal under specified load torque from 1800 rpm CW to 1800 rpm CCW. Figure 5.38 shows the reverse procedure.

### 5.4.4 Response of the Induction Machine to Load Torque Changes in Speed Regulation Mode

This test was carried out by applying or removing a 20% load torque on the induction machine in speed regulation mode. Figure 5.46 shows a typical load torque application. The second trace from the top represents the torque command of the induction machine. Before the load torque is applied, the machine is operated under no load. As soon as the load torque is applied, a counteracting torque command is developed to regulate the speed at the desired value. As seen in the third figure from the top, almost no speed change can be noted in that speed scale shown. Similarly, Fig. 5.47 shows the same

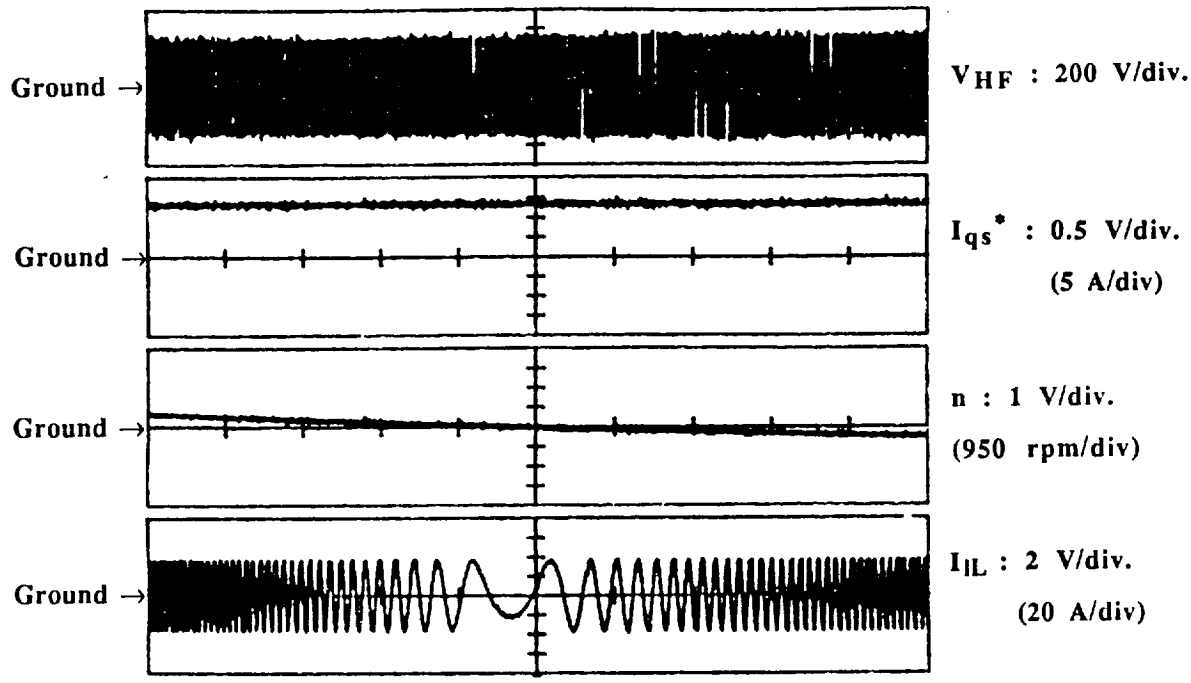


Fig. 5.42. Magnified View of Speed Reversal of Induction Machine (Fig. 5.41) Around Zero Speed. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Torque Component Current Command: $I_{qs}^*$ : 0.5 V/div (5 A/div). Speed of the Induction Machine: n : 1 V/div (950 rpm/div). Induction Machine Line Current: $I_{IL}$ : 2 V/div (20 A/div). Time/div: 500 msec.

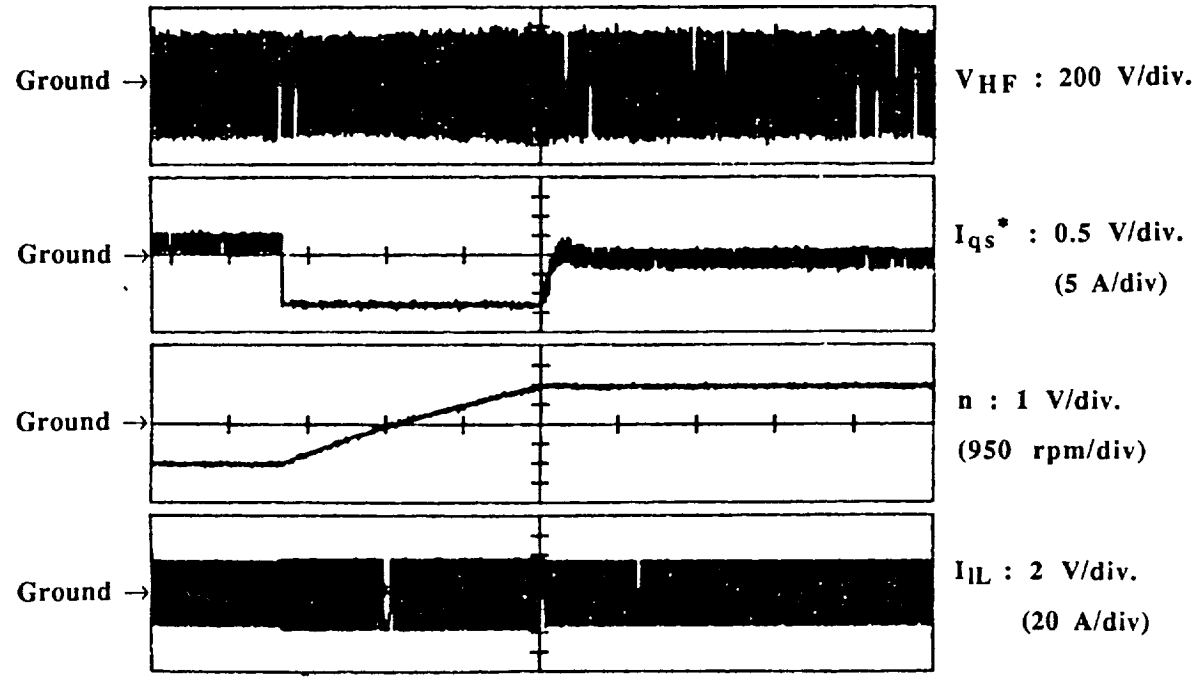


Fig. 5.43. Speed Reversal of Induction Machine Under No Load and in Speed Regulation Mode. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Torque Component Current Command: $I_{qs}^*$ : 0.5 V/div (5 A/div). Speed of the Induction Machine: n : 1 V/div (950 rpm/div). Induction Machine Line Current: $I_{IL}$ : 2 V/div (20 A/div). Time/div: 5 sec.

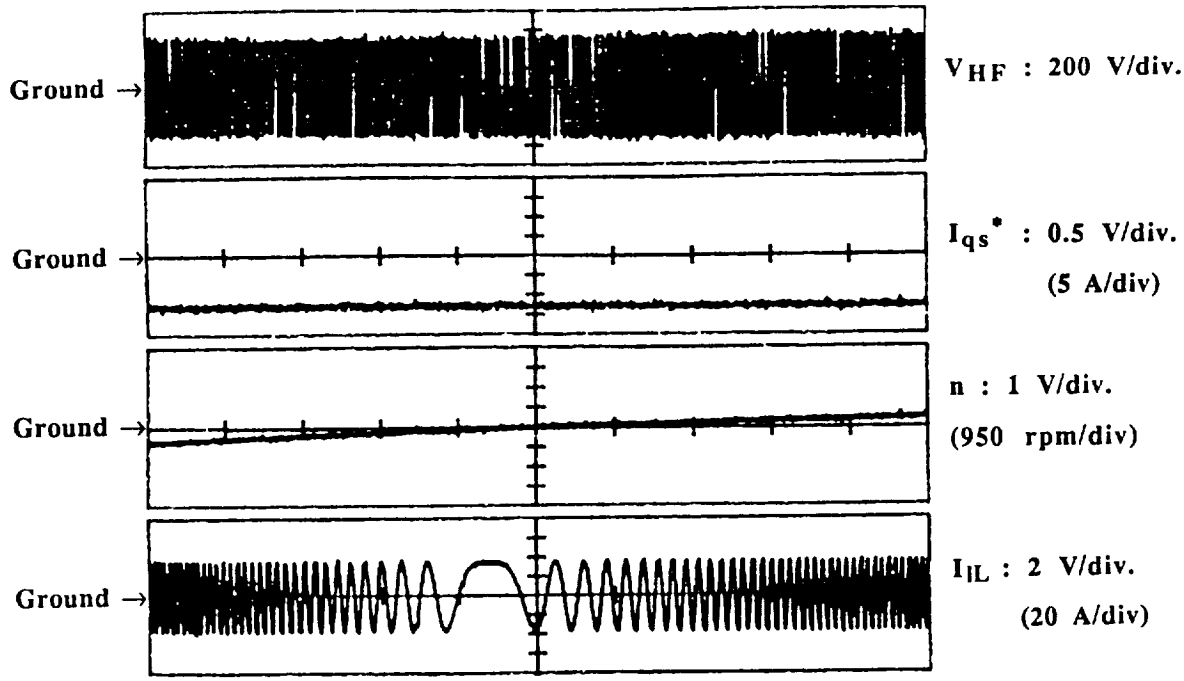


Fig. 5.44. Magnified View of Speed Reversal of Induction Machine (Fig. 5.43) Around Zero Speed. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Torque Component Current Command: $I_{qs}^*$ : 0.5 V/div (5 A/div). Speed of the Induction Machine: n : 1 V/div (950 rpm/div). Induction Machine Line Current: $I_{IL}$ : 2 V/div (20 A/div). Time/div: 500 msec.

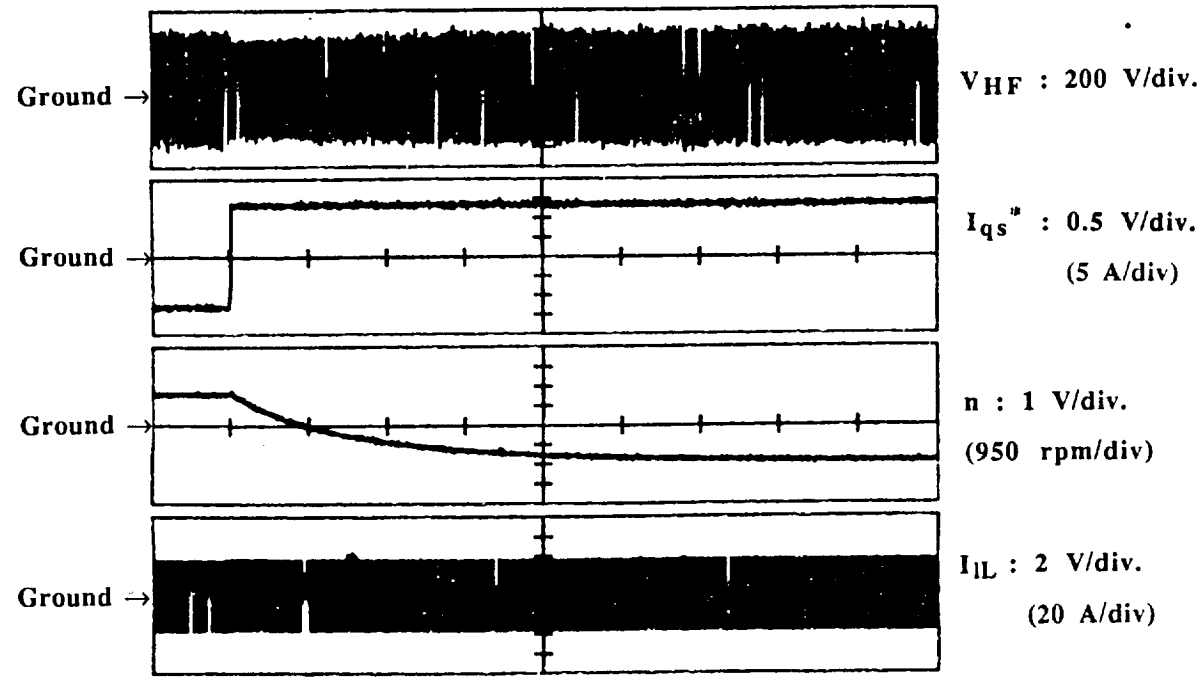


Fig. 5.45. Speed Reversal of Induction Machine Under Load and in Speed Regulation Mode. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Torque Component Current Command: $I_{qs}^*$ : 0.5 V/div (5 A/div). Speed of the Induction Machine: n : 1 V/div (950 rpm/div). Induction Machine Line Current: $I_{IL}$ : 2 V/div (20 A/div). Time/div: 5 sec.

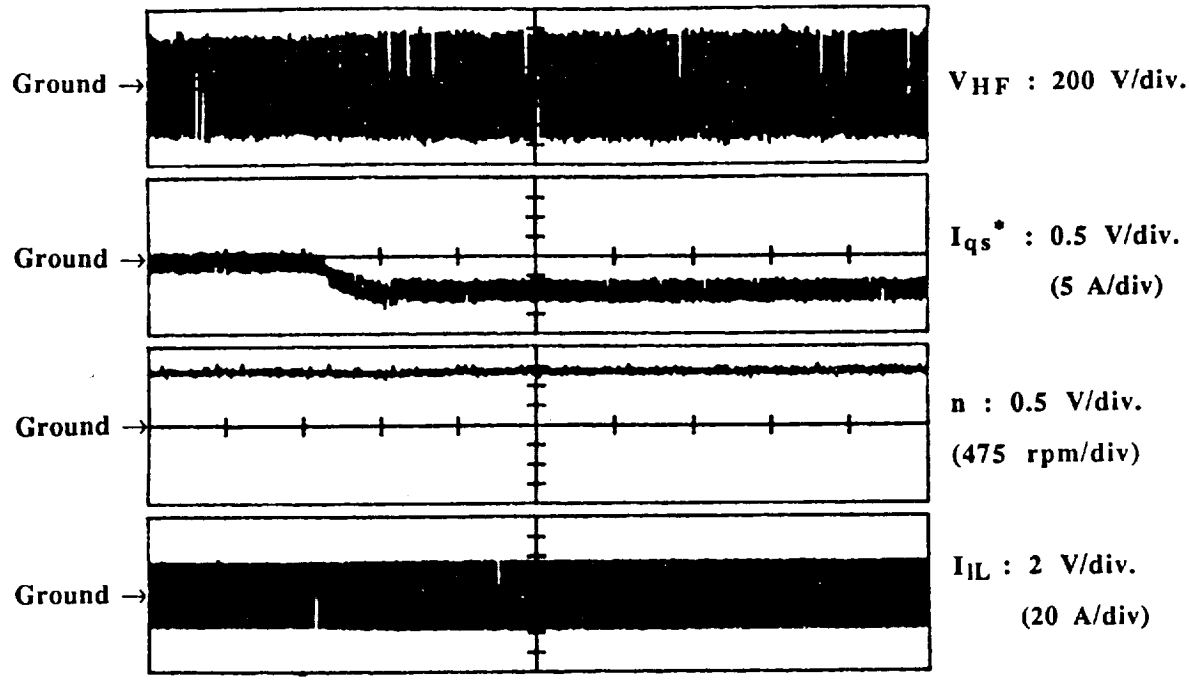


Fig. 5.46. Application of Load Torque in Speed Regulation Mode. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Torque Component Current Command: $I_{qs}^*$ : 0.5 V/div (5 A/div). Speed of the Induction Machine: n : 0.5 V/div (475 rpm/div). Induction Machine Line Current: $I_{IL}$ : 2 V/div (20 A/div). Time/div: 2 sec.

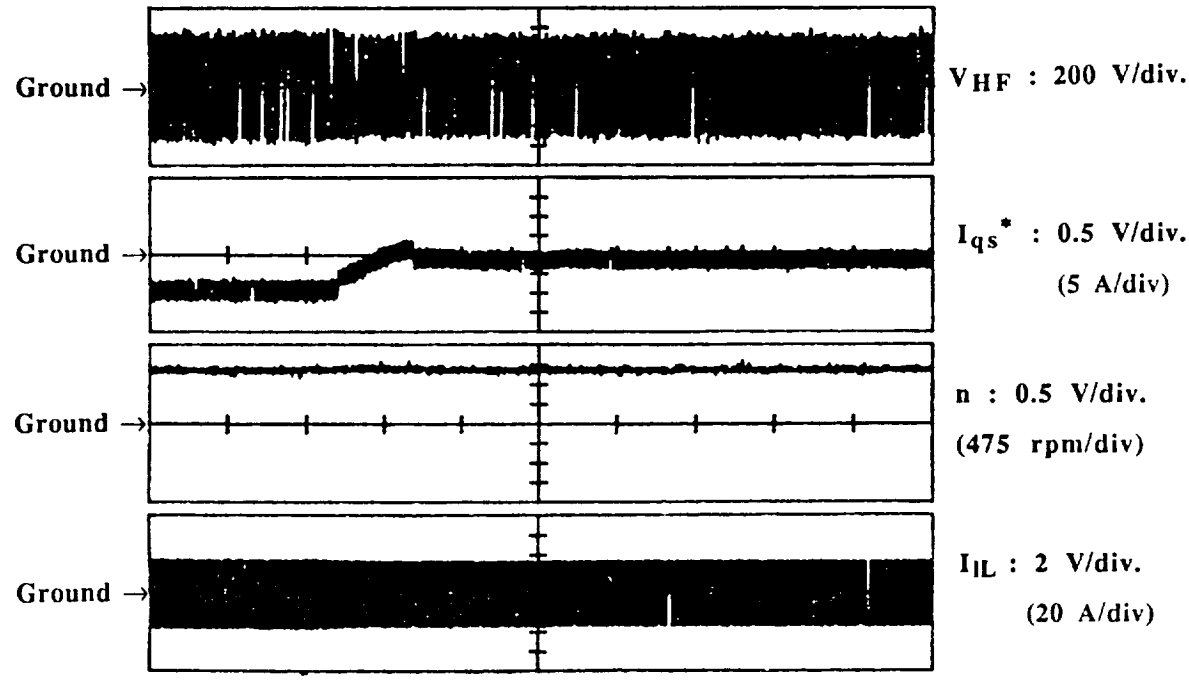


Fig. 5.47. Removal of Load Torque in Speed Regulation Mode. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Torque Component Current Command: $I_{qs}^*$ : 0.5 V/div (5 A/div). Speed of the Induction Machine: n : 0.5 V/div (475 rpm/div). Induction Machine Line Current: $I_{IL}$ : 2 V/div (20 A/div). Time/div: 2 sec.

amount of load torque removal, again causing no noticeable speed change. Hence, it appears that speed regulation of the induction machine is very satisfactory.

## 5.5 Power Level Comparison of Old and New Systems

### 5.5.1 Power Transfer Capacity of the Old System

A paper published about the design and performance of a high frequency link induction motor drive operating at unity power factor [4] has been included as Chapter 4 in this report. The experimental part of the work published in this paper was conducted with the first generation, low power level converter system. The power components used for the Load Side 3Ø-PDM Converter are given in Table 5.3 of Ref. [5] and for the Source Side 3Ø-PDM Converter in Table 6.1 of Ref. [3]. A more detailed discussion about the use of these power components and the problems encountered in their usage can be found in Chapter 3, Sections 3.2, 3 and 4 of this report.

It is useful to estimate the power delivery capacity of the system discussed in Chapter 4. Figures 4.11 and 12 indicate that the line to neutral source voltage is around 80 V zero to peak and source line current is around 7 A zero to peak. These values correspond to 57 V and 5 A rms. Operation at unity power factor implies that the source is supplying 3x57x5=855 W at this particular operating point. Because of the reasons explained in Section 3.2.1 of this report, reaching a 20 A peak device current with the utilization of the MJ10016 power darlington devices and the available general purpose base drive units is a very optimistic estimation. Hence, a maximum 20 A peak device current corresponds to a maximum 14 A rms source/load line current. Therefore, the maximum power supply level that can be achieved with 57 V rms line to neutral source voltage becomes 3x57Vx14 A=2394 W. It is possible to increase the power delivery level of the source by increasing the source voltage further without increasing the maximum peak current. However, as the level of the source voltage is increased the minimum peak link voltage value is increased. This, in turn, increases the device voltage stress. The power delivery capacity from the high frequency link supplying the induction machine can also be calculated. Again, by returning to Figs. 4.11 and 12 it can be roughly stated that the peak link voltage is varies roughly between 300 and 330 V. Hence, on average the peak link voltage is around 315 V. Substituting this peak link voltage value into Eq. 3.1.2, a maximum low frequency side induction machine voltage of around 200 V peak line to line is obtained or 141 V rms line to line. Again a maximum of 20 A peak device or 14 A rms induction machine line current can be assumed. Assuming 0.75 power factor for the induction machine, the maximum

deliverable power to the induction machine becomes $\sqrt{3}$x(141 V)x(14 A)x0.75=2564 W. The maximum power that can be delivered from the source was determined to be 2394 W. If the converter and link losses are subtracted from this amount, the maximum deliverable power to the induction machine reduces to around 1750 W.

### 5.5.2 Power Transfer Capacity of the New System

The operating condition of the system given in Figure 5.48 corresponds to the operating conditions specified in the second paragraph of Section 5.3.1. This figure reveals a 250 V peak or 177 V rms line to line source voltage and roughly 13 A peak or 9 A rms source line current operation. This implies an active power delivery of $\sqrt{3}$x(177 V)x(9 A)=2759 W at unity power factor operation as can be seen from the figure. This value is already more than three times the previous system. As designed, the system can be pushed to 50 A peak device current levels, although the excessive peak link voltage variation prevents this power level increase for the time being because of the low energy storage capacity of the link tank circuit. In other words, as the power level is increased, the existing energy storage capacity of the link tank circuit begins to become insufficient to handle the difference between the instantaneous and average power within the response time of the PI-link voltage regulator. It is obvious that the gap between the instantaneous and average power increases in proportion to the increasing power delivery level. Therefore, additional energy storage capacity is required for increased power level operations.

In the old low power rated system, two link tank circuits whose capacitor values are 3μF and inductor values are 22.5μH were used operating at 315 V peak link voltage. The energy storage capacity of the old system in this case becomes

$$2x(\tfrac{1}{2})xC_Tx{V_T}^2 = 2x(\tfrac{1}{2})x(3x10^{-6})x(315)^2 = 0.2976 \text{ joules.}$$

Because only one of the tank circuits was used in the new system due to the low current rating of one of the link tank circuit inductor, the same energy storage capacity under 510 V peak link voltage operation for the new system in this case becomes

$$1x(\tfrac{1}{2})xC_Tx{V_T}^2 = 1x(\tfrac{1}{2})x(3x10^{-6})x(510)^2 = 0.3901 \text{ joules.}$$

Even though the energy storage capacity of the new system is not increased more than 35% compared to the old system, the demonstrated operating power level has been increased more than 220% as from 855 W to 2759 W. The increase in the operating power

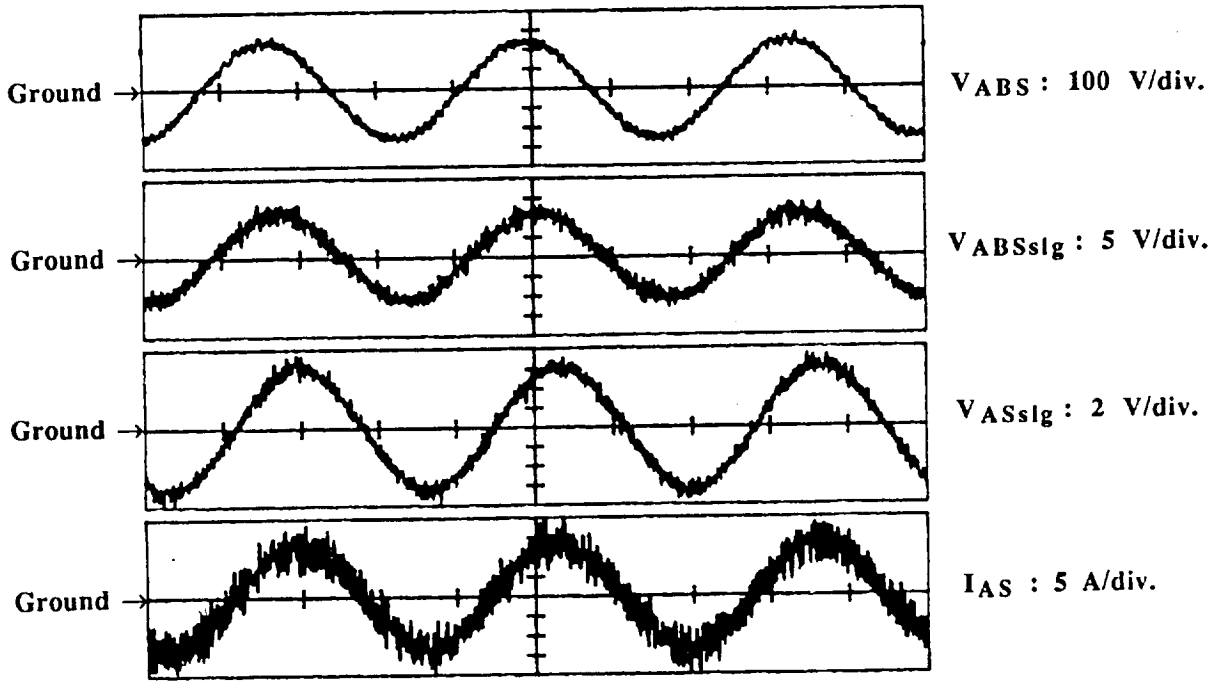


Fig. 5.48. Voltage and Current Waveforms for the Estimation of Power Drawn from the Source at Unity Power Factor. From the Top Respectively; Phase AB Line to Line Source Voltage: $V_{ABS}$ : 100 V/div. Phase AB Line to Line Source Voltage Signal: $V_{ABSsig}$ : 5 V/div. Phase A Line to Neutral Source Voltage Signal: $V_{ASsig}$ : 2 V/div. Phase A Source Current: $I_{AS}$ : 5 A/div. Time/div: 5 msec.

level with very little increase in the energy storage capacity clearly results in the substantial peak link voltage variations. Hence, more energy storage capacity is required to increase the operating power level.

Once the peak device current is pushed to 60-70 A including the high frequency ripple, a 50 A peak or 35.35 A rms source side line current can be reached. The maximum power delivery capacity of the source for the new system at unity power factor operation would then become $\sqrt{3}$x(177 V)x(35.35 A)=10.838 kW.

The power delivery capacity of the load side PDM converter can be calculated in a similar manner. By substituting a peak link voltage of 510 V into Equation 3.1.2, the maximum line to line peak induction machine voltage is found to be 324 V corresponding to 230 V line to line rms induction machine voltage. Assuming 35.35 A rms induction machine line current and 0.75 power factor leads to a maximum of $\sqrt{3}$x(230 V)x(35.35 A)x0.75=10.561 kW power delivery to the induction machine.

## 5.6 Conclusions

This chapter has summarized the performance of the 10 hp dynamometer system, built for high speed testing. The system is unique in that it not only uses an induction machine rather than a DC machine but also uses a resonant link as the frequency converter. At present, the voltage and current are limited by the speed limitations of the DC load machine (4000 RPM) and also by the design of the resonant link inductor and capacitor. To remove that latter difficulty a new air-core litz wire tank circuit inductor has been designed having a current capacity consistent with the overall rating of the converter (7.5 kW). A brief discussion of the test results with the new link inductor are given in Chapter 6.

## 5.7 References

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3. S. K. Sul, and T. A. Lipo, "Design and Test of Bidirectional Speed and Torque Control of Induction Machines Operating from High Frequency Link Converter", NASA Report, Contract No.NGA 3-786, April, 1988.

4. S.K. Sul and T.A. Lipo, "Design and Performance of a High Frequency Link Induction Motor Drive Operating At Unity Power Factor", Conf. Record of IEEE IAS Annual Meeting, 1988, pp. 308-313
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# Chapter 6

# Power Level Test of Second Generation Converter with Added Energy Storage Elements

## 6.1 Introduction

This chapter briefly describes the power level test of second generation converter driving the induction machine both in motoring and generating modes of operations with added energy storage elements to the HF link to overcome difficulties with the link voltage variation problem at high power levels. The importance of the source voltage level to achieve a better current regulation for the source side PDM converter is also briefly discussed. The power levels achieved in the motoring mode of operation shows that the proposed power levels in generating mode of operation (operation as an AC Dynamometer) can also be easily achieved if there were no mechanical speed limitation to drive the induction machine at the proposed power level.

## 6.2 Changes In the Power and Measurement Circuits

The first major change done in the power circuit is the addition of new resonant tank circuits. Two new air-core litz wire tank circuit inductors have been constructed for this purpose. Each of these new inductors has approximately 22.5 μH inductance and 200 A peak current capacity. Two new 3.0 μF, 1000 V and 161 A peak HF capacitors together with new inductors have been paralleled with the old resonant tank circuit to produce a new increased energy storage capacity for the resonant tank circuit. This modification has almost tripled the energy storage capacity of the resonant tank circuit of the second generation converter from what it is before (reported in Chapter 5). This change leads to a final definition of the link tank circuit inductor and capacitor which is given in Table 6.1. These values can be compared to the previous values given in Table 5.3.a. It is worthwhile to mention here that HF Link losses increase with the addition of the new tank circuit elements. As can be recalled from Chapter 5, when there is only one resonant tank circuit as defined in Table 5.3.a a small amount of energy was sufficient to build a 500 V peak link voltage with 178 V rms line to line source voltage while only the source side PDM converter was in operation(See Fig. 5.7.). With the addition of new tank circuit elements

| Component | Circuit Symbol | Key Specifications and Comments |
|---|---|---|
| Tank Circuit Inductor | LT | 7.5 μH, 550 A peak (One 22.5μH, 150 A peak and two 22.5 μH, 200 A peak air-core litz wire inductors in parallel) All the three inductors needs cooling especially when operated at 550 V peak. |
| Tank Circuit Capacitor | CT | 9.0 μF, 1000 V peak, 480 A peak (Nine 1.0μF GE97F8522FC in parallel) |
| Equivalent Tank Circuit Impedance | $Z_T=\sqrt{L_T/C_T}$ | 0.9129Ω |
| Source Side Voltage Sensors | $V_{SAB}$ & $V_{SBC}$ | 1000 V rms, DC - 100 kHz, 10000: 2000 ratio part #: LEM LV 100/SP5, R1=13 KΩ 212 V peak input yields 16.3 mA peak input, 81.5 mA peak output and 10.18 V control signal with 125 Ω terminator resistor. |

Table 6.1. Changed Component Values in the Power and Measurement Circuit of the Second Generation Three Phase to Three Phase Power Conversion System.

and increased HF link losses, it is experimentally determined that more than 2 kW power delivery from the source to the link is necessary to build up the same 500 V peak link voltage. This is, of course, the inevitable drawback of increasing the energy storage capacity of the resonant tank circuit.

Figure 6.1 basically portrays the HF link losses after the addition of the new resonant tank circuit elements. Since this figure is taken without the load side converter in operation, the power delivered from the source mainly reflects the HF link losses. A very small amount of these losses are produced by the SSPDM converter since the amplitude of the current is relatively small. As will be pointed out in the following paragraph along with a detailed discussion, the new value of the line to line source voltage is selected to be 153 V rms. The second figure from the top in Fig. 6.1 verifies this fact. The rms value of the source current, last figure from the top in Fig. 6.1, is determined with a harmonic spectrum analyzer to be 7.25 A. Unity fundamental power factor operation of the source is also clear

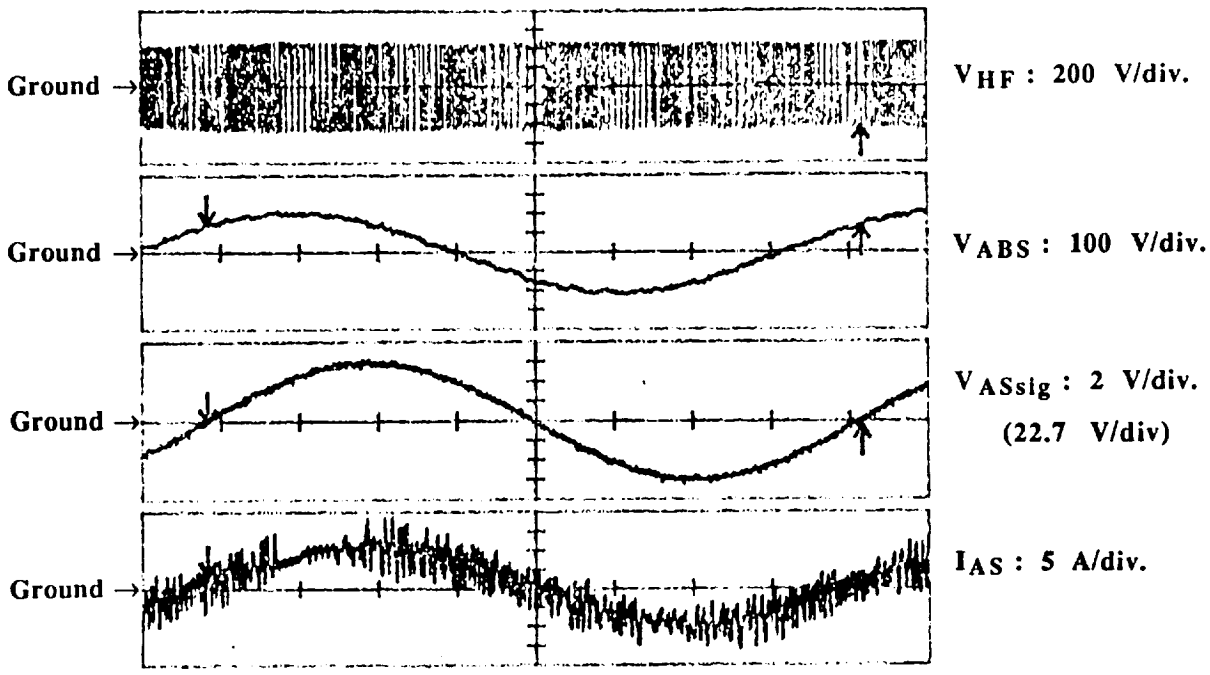


Fig. 6.1. Estimation of High Frequency Link Losses with Only Source Side PDM Converter in Operation. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Phase AB Line to Line Source Voltage: $V_{ABS}$ : 100 V/div. Phase A Line to Neutral Source Voltage Control Signal: $V_{ASsig}$ : 2 V/div (22.7 V/div). Phase A Source Line Current: $I_{AS}$ : 5 A/div. Time/div: 2 msec.

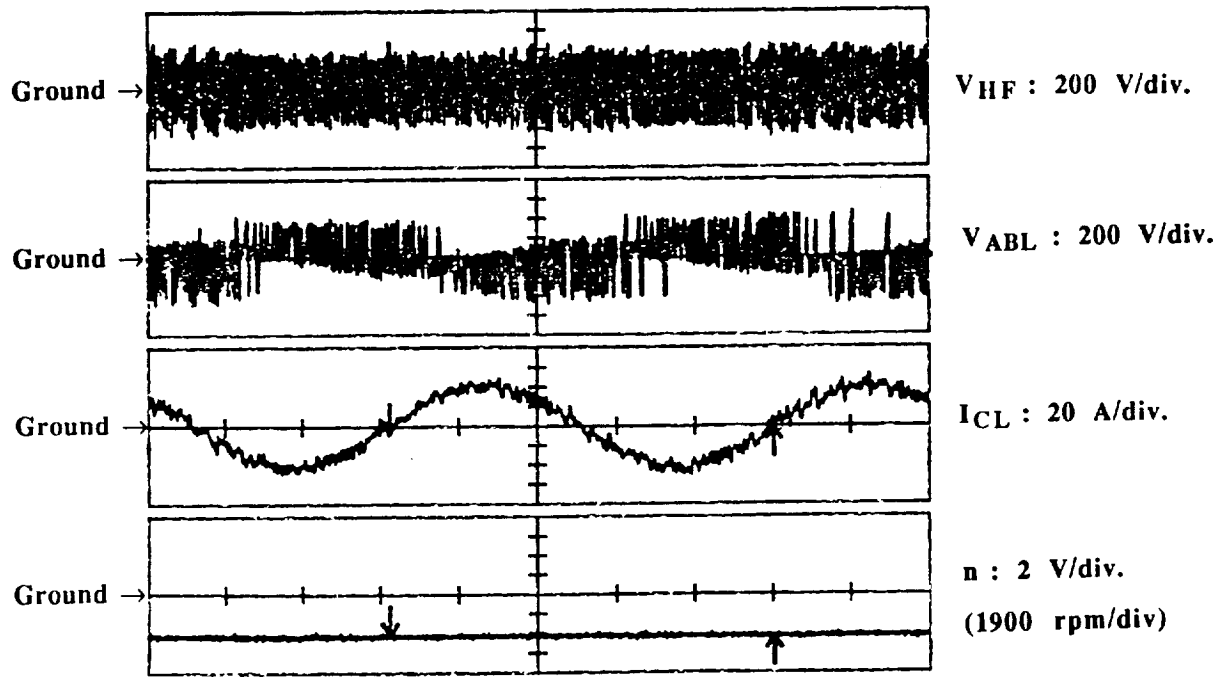


Fig. 6.2. Induction Machine in Motoring Mode of Operation at 200 Hz with Full Flux and Torque Command Applied. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Phase AB Line to Line Load (Induction Machine) Voltage: $V_{ABL}$ : 200 V/div. Phase C Load (Induction Machine) Current: $I_{CL}$ : 20 A/div. Speed of the Induction Machine: n : 2 V/div (1900 rpm/div). Time/div: 1 msec.

when the third and the last figures from the top are compared in Fig. 6.1. Therefore, the power delivered from the source for this operation becomes $\sqrt{3} * 153$ V $* 7.25$ A $= 1.921$ kW. The conduction losses of the SSPDM converter for this level of current are very small, around 140 W. This fact can be verified from Section 3.2.3 "The Conduction Losses in the PDM Converters". Switching losses are quite negligible compared to the conduction losses. Therefore, the rest of the losses, approximately 1.75 kW are spent as HF link losses in the resonant tank circuit elements for an average peak link voltage operation of around 480 V as can be verified from the first figure from the top in Fig. 6.1. As pointed out earlier, in order to push the link peak voltage to higher values such as 500-520 V, the reference current amplitude and delivered power from the source should be increased resulting in more HF link losses.

The second major change to the circuit is to modify the 60 Hz source voltage level. In particular, the source line to line voltage level had been increased and set to 208 V rms to remove the dependence of the system on a three phase auto transformer on the utility side and to reduce the conduction losses of the source side PDM converter for the same power transfer level. Unfortunately, this choice led to a poor and insufficient current regulation for the source side converter operating from 500-550 V peak link voltage. It is observed that this current regulation is good when the line to neutral source voltage is around its zero but poor around its peak. In particular, the current regulation was simply insufficient when the system is operated in regenerative mode of operation. Since the current regulation is primarily based on the peak link voltage value, the level of the source voltage can and should not exceed a certain value for a selected peak link voltage. In other words, the average peak link voltage value over any half cycle of the HF link should always be greater than any instantaneous line to line source voltage value to drive the current in the direction that the regulator commands.

It is useful to make a calculation for the above mentioned case. The average peak link voltage over any half cycle of the HF link by Equation 3.1.2 becomes

254.65 V for 400 V peak link voltage
318.30 V for 500 V peak link voltage
350.14 V for 550 V peak link voltage
381.97 V for 600 V peak link voltage

with the peak link voltage variations taken into consideration. Since peak line to line source voltage is 294.15 V for 208 V rms, the current regulation would not function at all for peak link voltages under 462.06 V and would function very poorly for voltages greater than but

close to 462.06 V. According to another theory where the link voltage is symbolically divided to two and midpoint is assumed to be at the same potential with the neutral of the source, the same limitations on the current regulation can be calculated in terms of line to neutral values.[1, 2, 3] According to this assumption, the average peak line to neutral link voltage over any half cycle of the HF link becomes

127.32 V for 400 V peak line to line link voltage
159.15 V for 500 V peak line to line link voltage
175.07 V for 550 V peak line to line link voltage
190.98 V for 600 V peak line to line link voltage

with peak link voltage variations taken into consideration. Since peak line to neutral source voltage is 169.83 V for 208 V rms line to line, the current regulation would not function properly for peak link voltages under 533.54 V and would function very poorly for peak link voltages greater than but close to 533.54 V.

In Reference [4], as the effect of source voltage to the link voltage regulation is discussed. Half the value of average peak link voltage over any half cycle of the HF link for the source voltage is recommended as an optimal source voltage for a better regulation. For the worst case, which is calculated according to the line to neutral quantities above, the optimal value of peak of the line to neutral source voltage should become 125 V for 250 V line to neutral link voltage peak or 500 V line to line link voltage peak. This 125 V line to neutral source voltage peak corresponds to 88.39 V line to neutral rms and 153.09 V line to line rms. In order to obtain better current regulation, the source voltage was set to this recommended value, approximately 153 V line to line rms, and the remainder of the experimental work is carried out with this source voltage. As a reminder, the tests reported in Chapter 5 were carried out with a 178 V line to line source voltage.

As pointed out earlier, reducing the line to line source voltage results in increasing the source current amplitude and the conduction losses for the source side PDM converter for the same power transfer. In addition, source voltage reduction reduces the power delivery capacity of the source for a given source current limit. For example, if 50 A source current amplitude is considered to be the limit, then the power delivery capacity of the source at unity power factor operation becomes $\sqrt{3} * 153\ V * (50/\sqrt{2})\ A = 9.369\ kW$. For power deliveries greater than this value, it is necessary to increase the amplitude of the source current by not endangering the safe operating area limits of the devices used in the converters specified in Table 5.3.a.

The third major change is done in the measurement circuit. To increase the accuracy of the measurement of source line to line voltages, the resistors used at the input of the LEM voltage sensors were changed from 50 kΩ to 12 kΩ. This change along with its other characteristics is shown in Table 6.1. Measured source voltage signals were readjusted to obtain 6 V line to neutral source voltage peak signal for 150 V rms line to line operating source voltage. If desired, this new source voltage scaling between the real values and the control signal quantities can be seen from Fig. 6.7. All other power matching signals in the control circuit were readjusted according to these new quantities.

## 6.3 Test Results Concerning the Power Level Test of Second Generation Converter with Added Energy Storage Elements

In this section, firstly the test results related to the motoring mode of operation of induction machine for the power range limited by the speed limit of the DC dynamometer (4000 rpm) will be presented. Secondly, the results related to the generating mode of operation of induction machine for the same speed will be shown. It is worthwhile to mention here that the DC machine must be overloaded for short periods of time to obtain these test results in both modes of operation so that we are at the limit of our loading capability in our laboratory. Thirdly, the speed reversals and four quadrant operation of induction machine will be shortly reviewed after the most recent changes. Fourthly and lastly, the induction machine decoupled from the DC machine test results at no load where the rated speed can be reached will be presented.

### 6.3.1 Test of the Induction Machine in Motoring Mode at Maximum Available Power

In this test, induction machine is driven in the motoring mode with a field oriented controller at rated torque and flux via the second generation three phase to three phase PDM converter and it is loaded with the DC dynamometer to the speed range of 4000 rpm. Since the rated speed of induction machine is 6000 rpm this operating point corresponds to 2/3 rated power operation in motoring mode for induction machine. However, this power range is quite close to the rated power defined for generating mode of operation for induction machine because of input, output and efficiency definitions in different modes.

Figure 6.2 reveals this operation for the induction machine by showing the line to line voltage and line current of induction machine at approximately 200 Hz and speed of

about 4000 rpm. The harmonic spectrum of these voltage and current waveforms can now be examined to determine exactly their fundamental components and harmonic spectrums.

Figure 6.3 shows the harmonic spectrum of the line current of induction machine over the frequency range of 0 to 2 kHz. The top trace clearly shows a 29.34 A rms fundamental component of line current at 200 Hz. Since the induction machine nameplate ratings are 32 A rms and 300 Hz, this operating point provides 2/3 rated power operation in motoring mode with only a small error in the predicted flux and torque components of the current. As can be observed from the figure, the current has a very clean harmonic spectrum over this frequency range. Figure 6.4 is meant to show the same harmonic spectrum over the frequency range of 0 to 50 kHz. Since the measurement steps of the spectrum analyzer is 125 Hz for this frequency range and the fundamental component of the current is at 200 Hz, the information concerned with the fundamental component reflected in Fig. 6.4 should be disregarded.

Figure 6.5 shows the harmonic spectrum of the line to line voltage of the induction machine over the frequency range of 0 to 2 kHz. With a 142.9 V rms line to line voltage at 200 Hz, an approximate constant flux operation of the induction machine is verified. The V/f ratio for this operating point is 142.9 V/200 Hz = 0.7145 V/Hz versus rated V/f ratio with 230 V/300 Hz = 0.7667 V/Hz. The reason that the V/Hz at 200 Hz operating point is slightly smaller than the rated value is because of the low peak link voltage amplitude. This feature can be verified from Fig. 6.2. The reason for the low peak link voltage amplitude is primarily due to the high link losses resulting from the addition of new resonant tank circuit elements and secondarily the reduced line to line source voltage level. It is possible to push the link voltage higher to 500-550 V peak range at the expense of quite high link losses. This, however, is not preferred. Figure 6.6 shows the harmonic spectrum of the line to line induction machine voltage over the frequency range of 0 to 50 kHz. The 200 Hz fundamental component information can be disregarded for the same reason mentioned in the previous paragraph.

The source side voltage and current waveforms for unity power factor operation of the source under the same operating conditions can be observed from Fig. 6.7. If source line to line voltage is carefully examined in this figure, approximately 153 V rms operation will be noticed. The same figure also provides an indication about the source voltage scaling as discussed in the last paragraph of Section 6.2. It is now useful to examine the harmonic spectrum of the source side current waveform and to determine a closer estimate of the source line current rms value before making a calculation for the power delivered from the source to the converter. Figure 6.8 shows the harmonic spectrum of the source line current over a 0 to 2 kHz range. This harmonic spectrum belongs to the source current

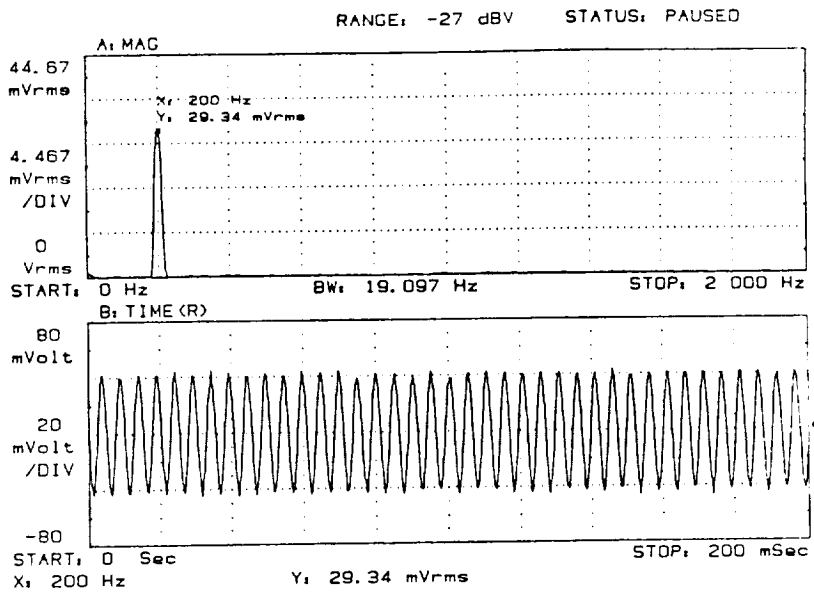


Fig. 6.3. Phase C Load (Induction Machine) Line Current (Shown in Fig. 6.2, $I_{CL}$) Harmonic Spectrum Over 0-2 kHz Range. $I_{CL}$ : 1 A rms/mV rms & 1 A/mV.

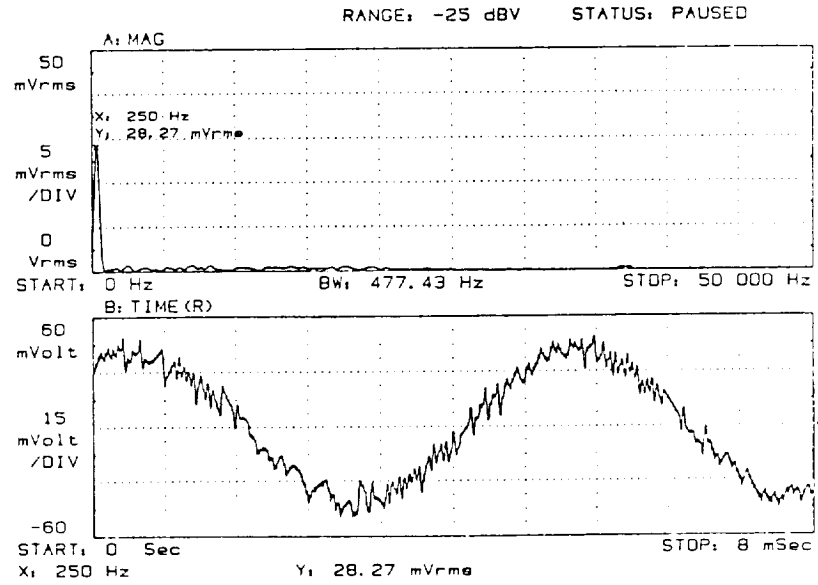


Fig. 6.4. Phase C Load (Induction Machine) Line Current (Shown in Fig. 6.2, $I_{CL}$) Harmonic Spectrum Over 0-50 kHz Range. $I_{CL}$ : 1 A rms/mV rms & 1 A/mV.

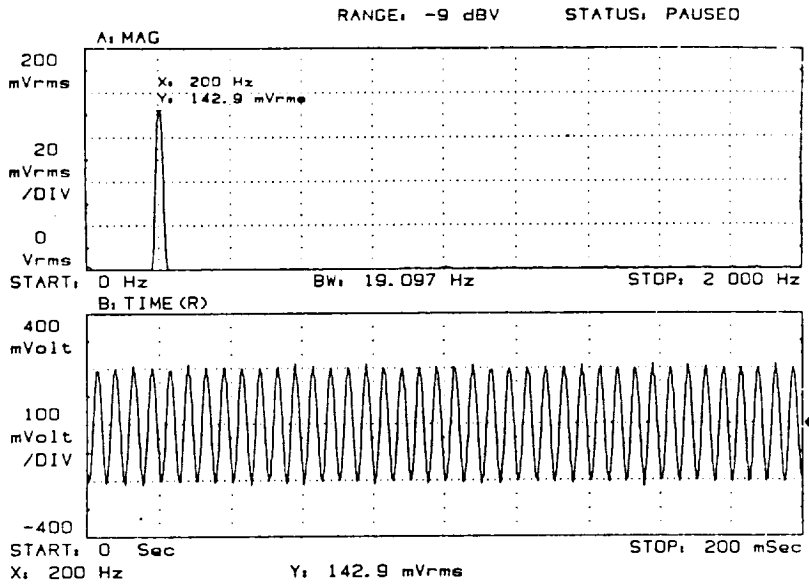


Fig. 6.5. Phase AB Line to Line Load (Induction Machine) Voltage (Shown in Fig. 6.2, $V_{ABL}$) Harmonic Spectrum Over 0-2 kHz Range. $V_{ABL}$ : 1 V rms/mV rms & 1 V/mV.

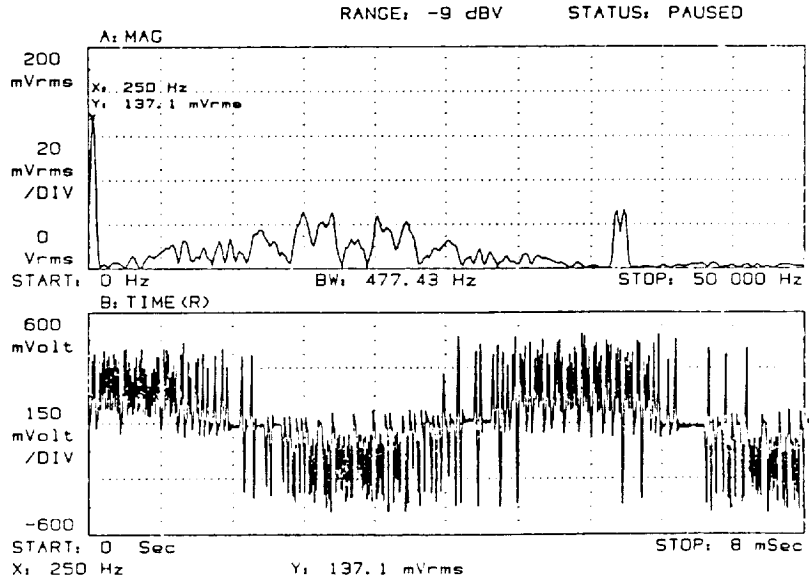


Fig. 6.6. Phase AB Line to Line Load (Induction Machine) Voltage (Shown in Fig. 6.2, $V_{ABL}$) Harmonic Spectrum Over 0-50 kHz Range. $V_{ABL}$ : 1 V rms/mV rms & 1 V/mV.

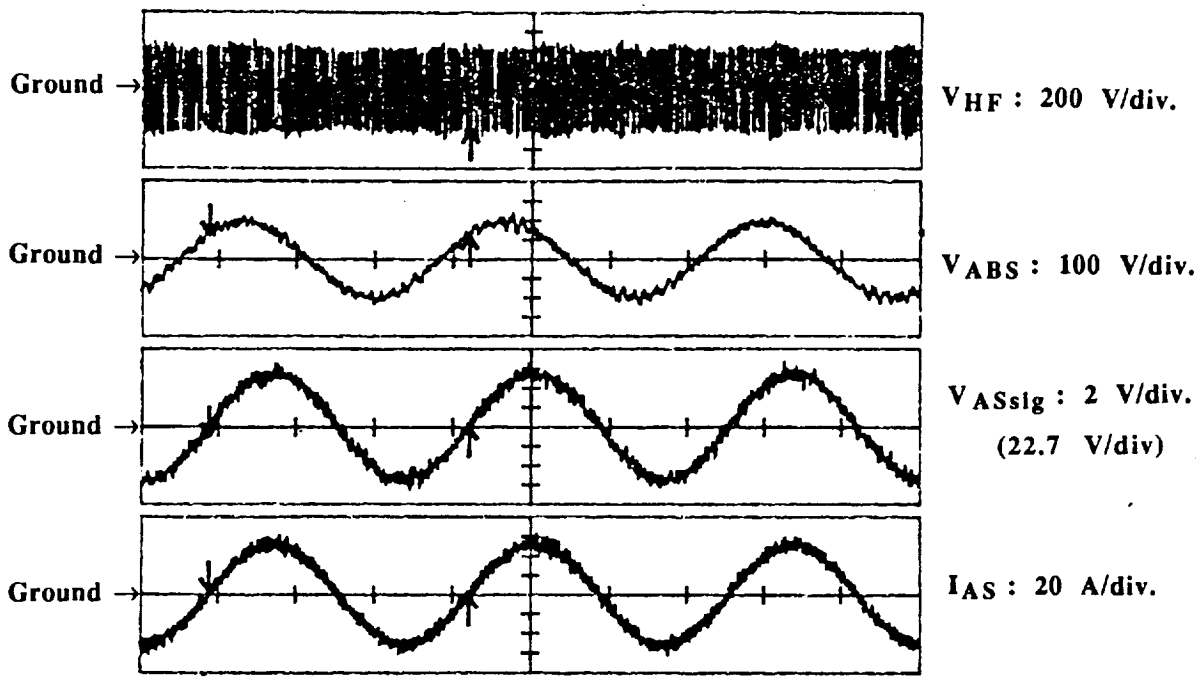


Fig. 6.7. Waveforms Pertaining to the Unity Power Factor Operation of the Source while Induction Machine is in Motoring Mode Of Operation at 200 Hz with Full Flux and Torque Command Applied. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Phase AB Line to Line Source Voltage: $V_{ABS}$ : 100 V/div. Phase A Line to Neutral Source Voltage Control Signal: $V_{ASsig}$ : 2 V/div (22.7 V/div). Phase A Source Line Current: $I_{AS}$ : 20 A/div. Time/div: 5 msec.

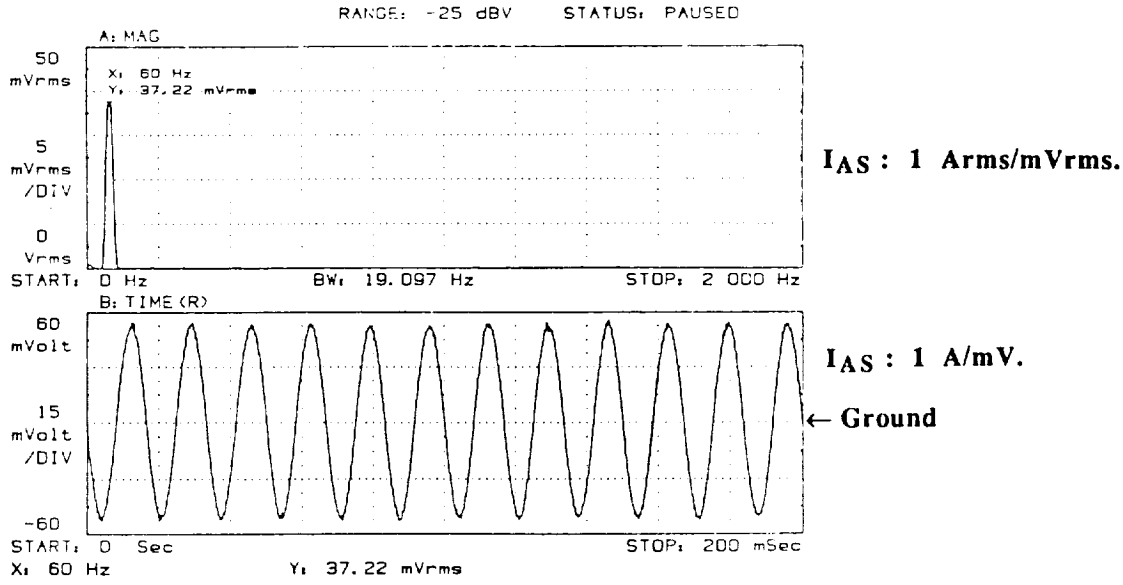


Fig. 6.8. Phase A Source (60 Hz Utility) Line Current (Shown in Fig. 6.7, $I_{AS}$) Harmonic Spectrum Over 0-2 kHz Range. $I_{AS}$ : 1 Arms/mVrms & 1 A/mV.

waveform shown in the fourth figure from the top in Fig. 6.7. The top trace in Fig. 6.7 reveals a 37.22 A rms fundamental current component at 60 Hz with a quite clean harmonic spectrum. Figure 6.9 shows the same harmonic spectrum over the frequency range of 0 to 50 kHz. Since the measurement steps of spectrum analyzer is 125 Hz for this frequency range, it does not show the fundamental component at 60 Hz and the information about the fundamental component can be disregarded in Fig. 6.9.

The power delivered from the source to the converter can now be easily calculated since all of the source side rms voltage and current quantities are determined along with a unity power factor operation. In other words, $\sqrt{3} * 153\ V * 37.22\ A * 1.0 = 9.86\ kW$ is delivered from the source to the converter. This amount of power is equivalent to 13.22 hp. In the load tests conducted to determine the equivalent circuit parameters of the induction machine at 60 Hz, 46 V rms line to line voltage and rated torque, 1.92 kW is drawn from the utility. The power drawn from the machine at this frequency and rated torque with constant V/f ratio is equivalent to the one fifth of the power which will be drawn at 300 Hz, 230 V rms and rated torque. Therefore, the rated power in motoring mode of operation is five times of that of 1.92 kW. In other words 9.6 kW. In order to determine the two thirds of the power in motoring mode of operation, we can approximately take 6.4 kW as the two thirds of 9.6 kW. If we assume that induction machine is drawing 6.4 kW while the source is delivering 9.86 kW, the difference between the two which is 3.46 kW should be dissipated as link losses in the resonant tank circuit elements and conduction and switching losses in the PDM converters. As we discussed at the end of the first paragraph of section 6.2, the HF link losses can be approximately taken to be 1.75 kW leaving 1.71 kW of 3.46 kW for the conduction and switching losses of the PDM converters.

When 10 hp induction machine is operated as its usual dyno load in the generating mode of operation, it is required to deliver 10 hp (7.46 kW) from its electrical terminals at its rated power operation. It is clear that this requirement will be no problem for the modified PDM converter because it handles already 9.86 kW input and 6.4 kW output power transfer levels.

Good current regulation for the source side is verified from Fig. 6.10 when the induction machine is operated in the motoring mode of operation under the same conditions specified before (200 Hz, rated flux, rated torque, 2/3 of rated power.) Unity fundamental power factor operation of the source is also observed with this figure.

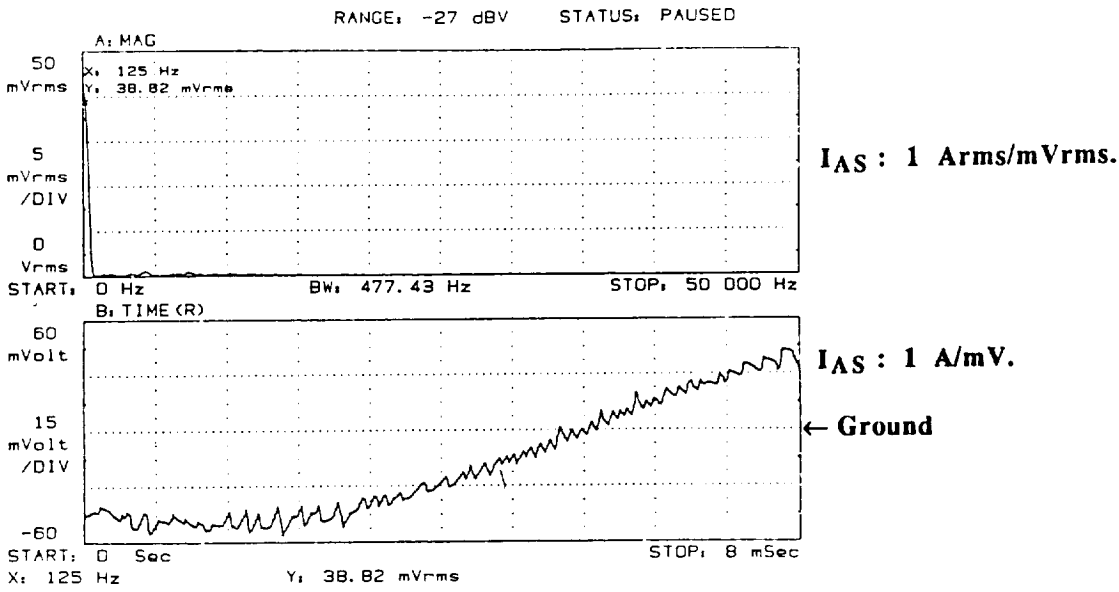


Fig. 6.9. Phase A Source (60 Hz Utility) Line Current (Shown in Fig. 6.7, $I_{AS}$) Harmonic Spectrum Over 0-50 kHz Range. $I_{AS}$ : 1 Arms/mVrms & 1 A/mV.

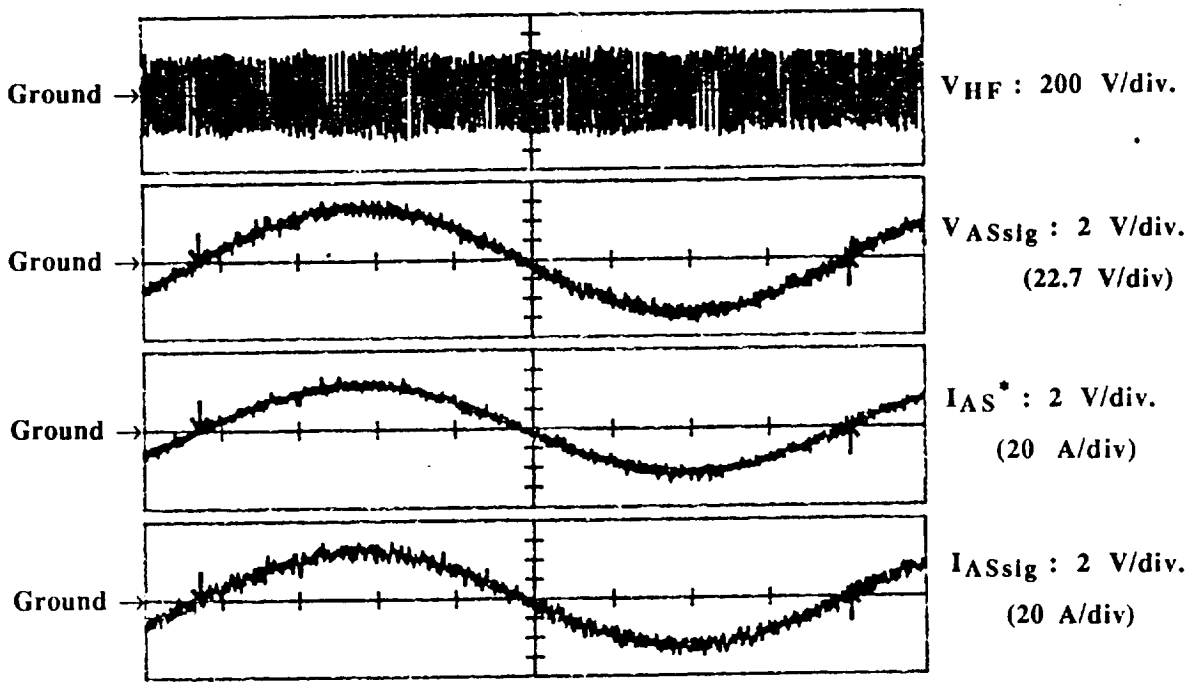


Fig. 6.10. Current Regulation and Unity Power Factor Operation of the Source When Induction Machine is in Motoring Mode Of Operation at 200 Hz with Full Flux and Torque Command Applied. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Phase A Line to Neutral Source Voltage Control Signal: $V_{ASsig}$ : 2 V/div (22.7 V/div). Phase A Source Line Current Reference Signal: $I_{AS}^*$ : 2 V/div (20 A/div). Phase A Source Line Current Measured Signal: $I_{ASsig}$ : 2 V/div (20 A/div).Time/div: 2 msec.

### 6.3.2 Test of the Induction Machine in Generating Mode at Maximum Available Power

In this test, the induction machine is operated in generating mode. The same DC machine which is used as a DC dynamometer for the previous test used to drive the induction machine in this test at 4000 rpm. This time the induction machine is used as an AC Dynamometer to load the DC machine. A field oriented controlled induction machine utilizing a three phase to three phase second generation converter is given full torque and flux commands. This operation results in overloading of the DC machine to almost twice its rated current. When the DC machine is loaded its speed drops as expected, yet by reducing the field of the DC machine the speed is readjusted to the 4000 rpm. Since the purpose of the test is to show that the converter is able to handle the requirements of regenerating the power back to the source to the power limit allowed by the mechanical speed limitation of the DC machine, the overloading of the DC machine for short period of times which will enable to get the necessary tests records had to be tolerated.

Figure 6.11 corresponds to the generating mode of operation of induction machine and shows the line to line voltage and line current of the induction machine at around 200 Hz and speed of induction machine at around 4000 rpm. The harmonic spectrum of the line current of induction machine over the range of 0-2 kHz in Fig. 6.12 reveals that the rms value of the fundamental component of this current which is also the third figure from the top in Fig. 6.11 is 37.28 A. Since the harmonic spectrum of this current over the 0-50 kHz range looks similar to that of Fig. 6.4 it is not shown here. Similarly, the harmonic spectrum of line to line voltage of induction machine over 0-2 kHz range is given in Fig. 6.13 where it reveals a 166.4 V rms fundamental component at 200 Hz. The V/f ratio of this operating point is 166.4 V/200 Hz = 0.832 as compared to the rated 230 V/300 Hz = 0.7667 which approximately reflects the constant flux operation of the induction machine. The reason that the V/f ratio of the operating point is a little higher than the rated value is the higher average peak link voltage value. Again 0-50 kHz range harmonic spectra of the voltage is skipped due to its similarity to that of Fig. 6.6.

Excellent current regulation of induction machine at this operating point is shown in Fig.6.14. In this case the reference current signal is shown as the third figure from the top and the actual current signal in the last figure from the top.

The utility grid side waveforms during this mode of operation is given in Fig. 6.15. The second figure from the top clearly reflects an approximate 153 V rms line to line source voltage operation. The third figure from the top which is the line to neutral phase A source voltage signal and fourth figure from the top which is phase A line current signal reveals clearly regenerative unity power factor operation of the source. The line current harmonic

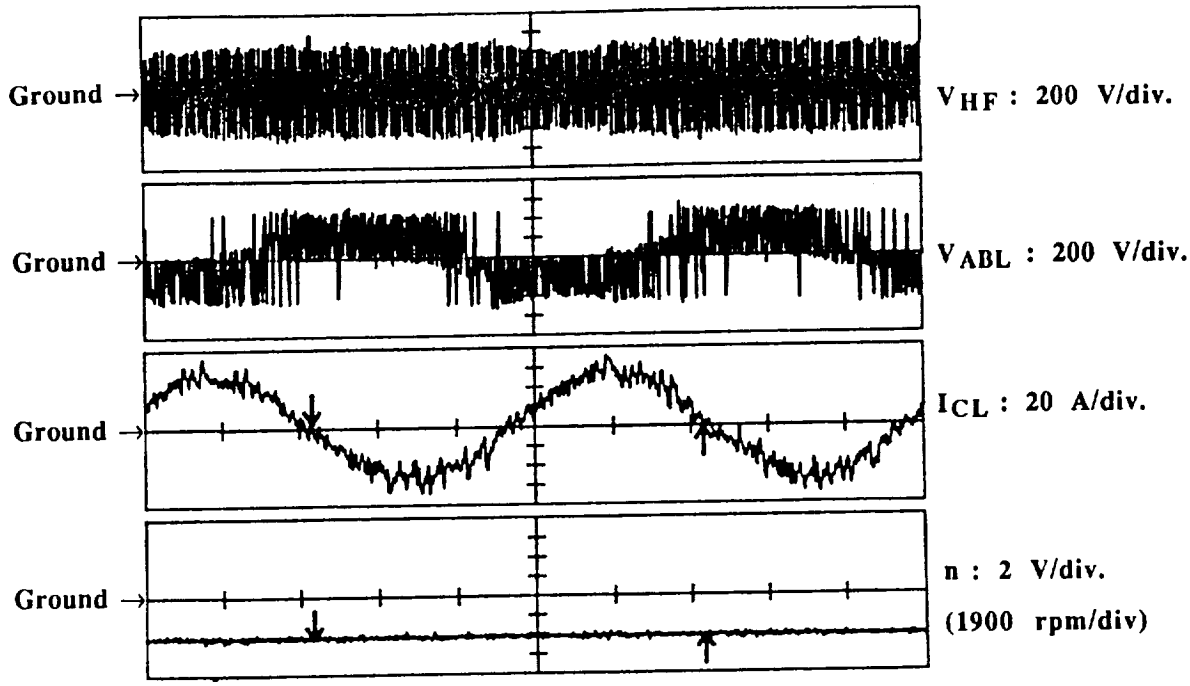


Fig. 6.11. Induction Machine in Generating Mode of Operation at 200 Hz with Full Flux and Torque Command Applied. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Phase AB Line to Line Load (Induction Machine) Voltage: $V_{ABL}$ : 200 V/div. Phase C Load (Induction Machine) Current: $I_{CL}$ : 20 A/div. Speed of the Induction Machine: n : 2 V/div (1900 rpm/div). Time/div: 1 msec.

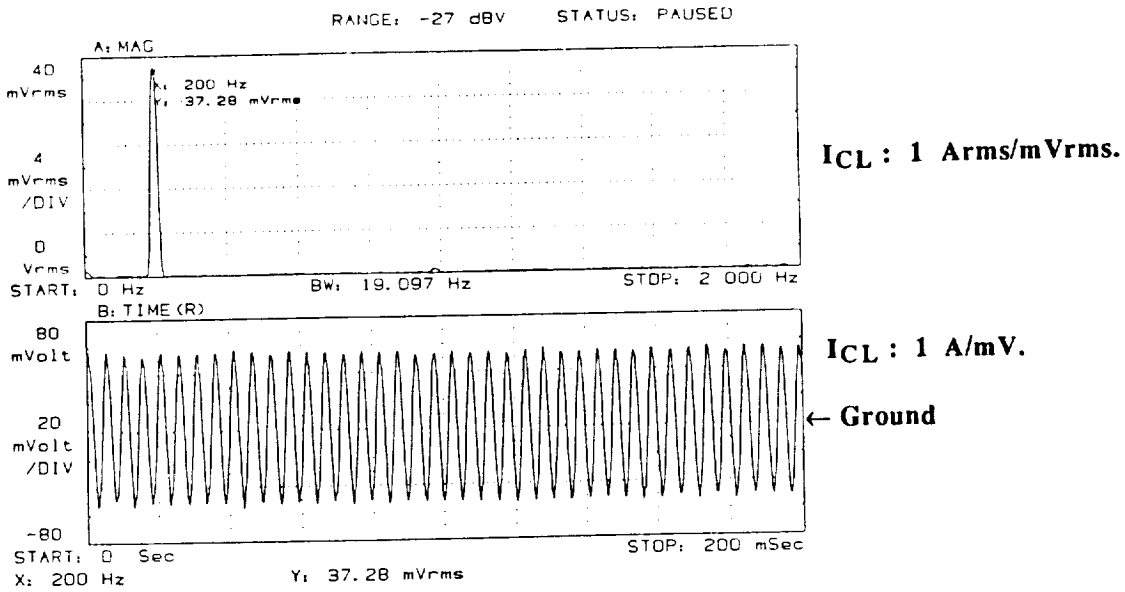


Fig. 6.12. Phase C Load (Induction Machine) Line Current (Shown in Fig. 6.11, $I_{CL}$) Harmonic Spectrum Over 0-2 kHz Range. $I_{CL}$ : 1 Arms/mVrms & 1 A/mV.

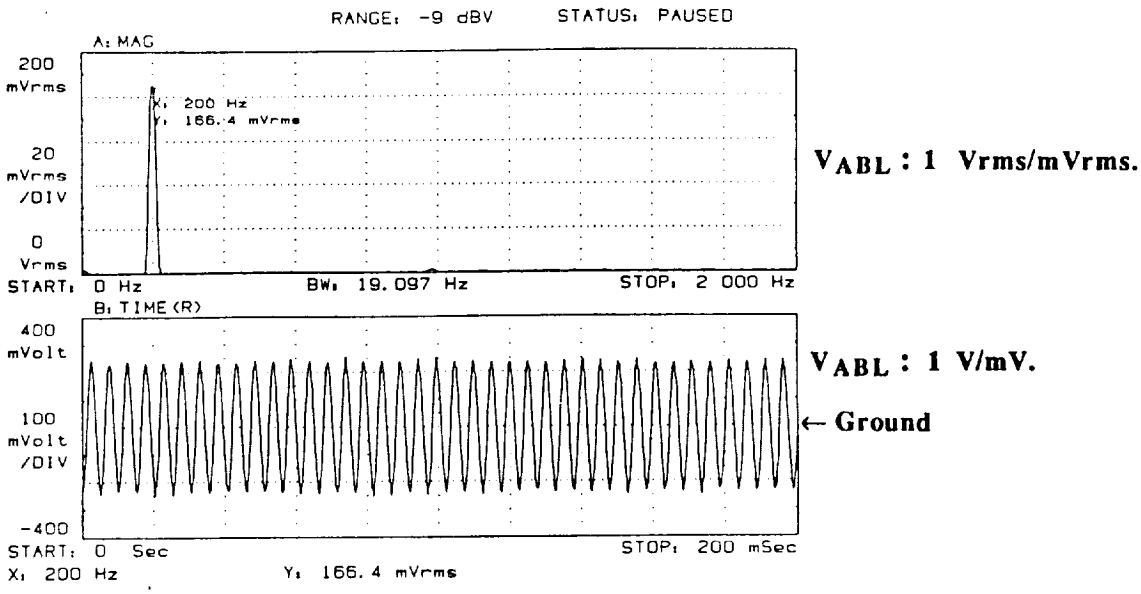


Fig. 6.13. Phase AB Line to Line Load (Induction Machine) Voltage (Shown in Fig. 6.11, $V_{ABL}$) Harmonic Spectrum Over 0-2 kHz Range. $V_{ABL}$ : 1 Vrms/mVrms & 1 V/mV.

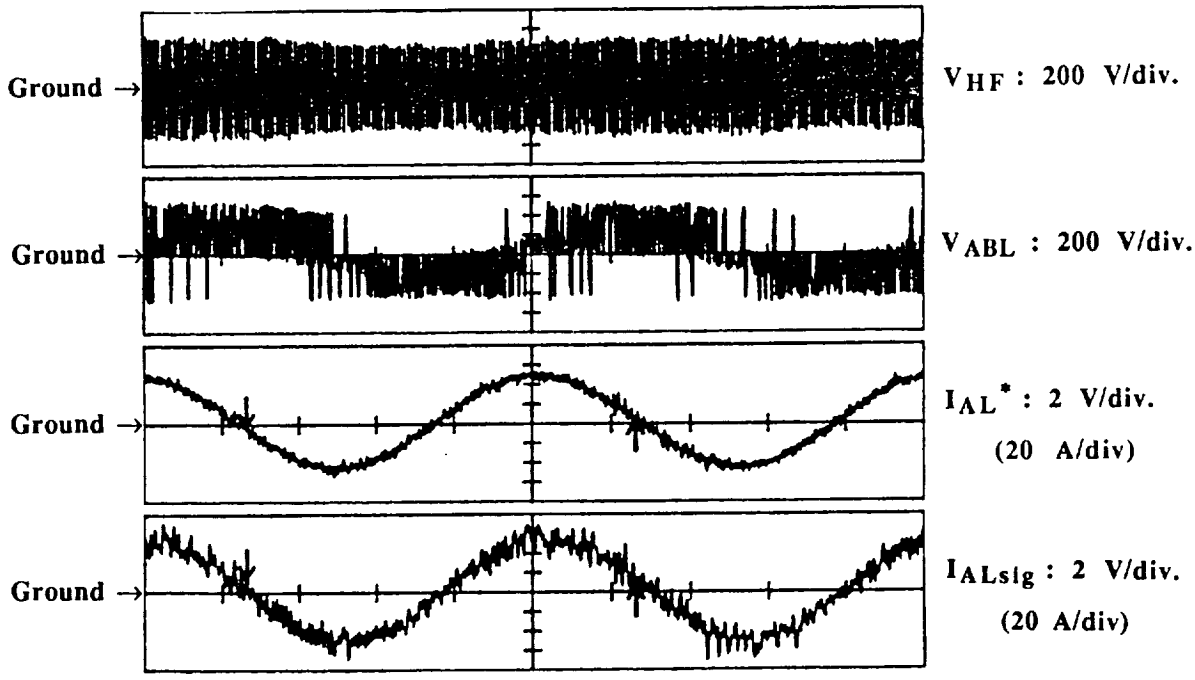


Fig. 6.14. Current Regulation of Induction Machine in Generating Mode of Operation at 200 Hz with Full Flux and Torque Command Applied. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Phase AB Line to Line Load (Induction Machine) Voltage: $V_{ABL}$ : 200 V/div. Phase C Load (Induction Machine) Reference Current Signal: $I_{CL}^*$ : 2 V/div (20 A/div). Phase C Load (Induction Machine) Measured Current Signal: $I_{CLsig}$ : 2 V/div (20 A/div). Time/div: 1 msec.

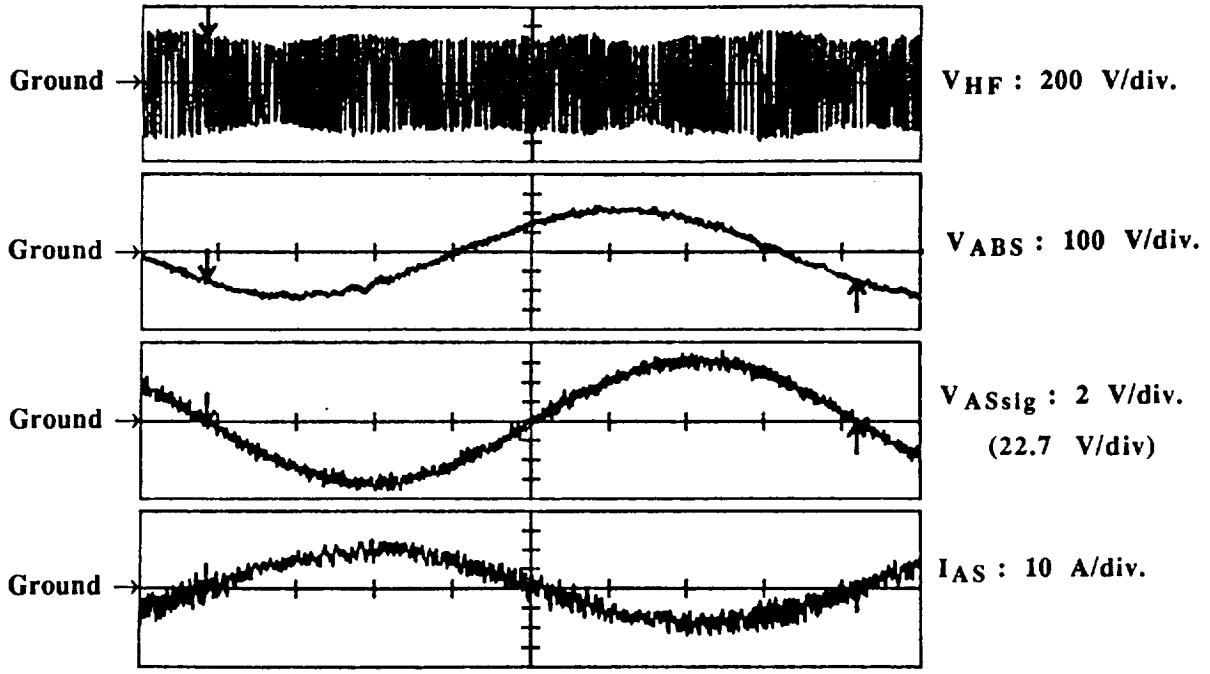


Fig. 6.15. Waveforms Pertaining to the Unity Power Factor Operation of the Source while Induction Machine is Operating in Generating Mode of Operation at 200 Hz with Full Flux and Torque Command Applied. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Phase AB Line to Line Source Voltage: $V_{ABS}$ : 100 V/div. Phase A Line to Neutral Source Voltage Control Signal: $V_{ASsig}$ : 2 V/div (22.7 V/div). Phase A Source Line Current: $I_{AS}$ : 10 A/div. Time/div: 2 msec.

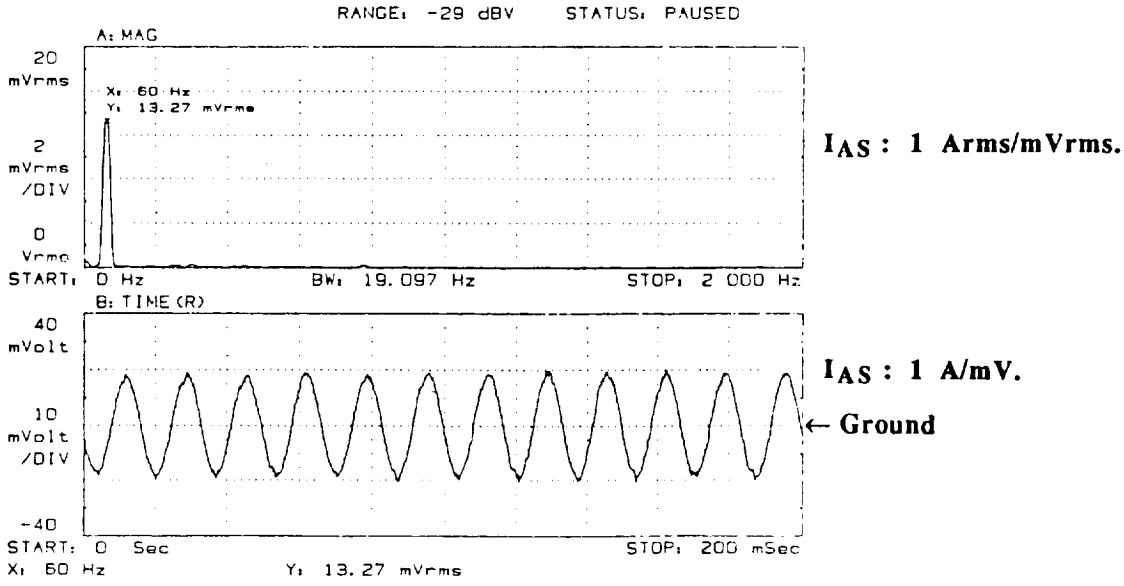


Fig. 6.16. Phase A Source (60 Hz Utility) Line Current (Shown in Fig. 6.15, $I_{AS}$) Harmonic Spectrum Over 0-2 kHz Range. $I_{AS}$ : 1 Arms/mVrms & 1 A/mV.

spectrum over 0-2 kHz range is given in Fig. 6.16. This trace indicates a 13.27 A rms fundamental component at 60 Hz. Determination of these quantities provides a means to evaluate the power delivered to the source during this mode of operation. In particular, $\sqrt{3}$ * 153 V * 13.27 A * 1.0 = 3.516 kW. If we add an approximate 3.0-3.5 kW HF link, converter conduction and switching losses to this power as estimated in the last paragraphs of section 6.3.1, approximately 6.5-7.0 kW is being delivered from the induction machine to the converter. Even though the induction machine is operating at 2/3 of its rated frequency, full torque and full flux commands in its generating mode, it is already delivering a power which is very close to 10 hp (7.46 kW).

Figure 6.17 shows the nice current regulation of the source where the reference current signal is shown in third figure from the top and actual current signal in fourth figure from the top.

As mentioned earlier, the modified converter has been shown to be able to absorb 9.86 kW and deliver around 6.4 kW for the motoring mode of operation of induction machine. Therefore, the induction machine can be driven as an AC dynamo to deliver 9.86 kW to the converter where the converter would absorb this power and deliver the remaining to the utility at regenerative unity power factor. Hence, operation of the induction machine as an AC dynamo to its rated frequency with full torque and flux commands will be possible if a mechanical speed limitation of the test machine driving the induction machine is not present.

### 6.3.3 Speed Reversals and Four Quadrant Operation of Induction Machine after New Resonant Tank Circuit and Operating Source Voltage

Figure 6.18 is presented to demonstrate speed reversals under no load where full torque command is applied when the speed reversal is desired. This figure shows 200 Hz and 4000 rpm operation of induction machine and both directions of speed reversals. This figure can be compared to Figs. 5.41 and 5.43 and to assess the improvement in the applied torque command and achieved operational speed or frequency. Figure 6.19 is intended to show the same speed reversal under load. This figure can similarly be compared to Figs. 5.38 and 5.45.

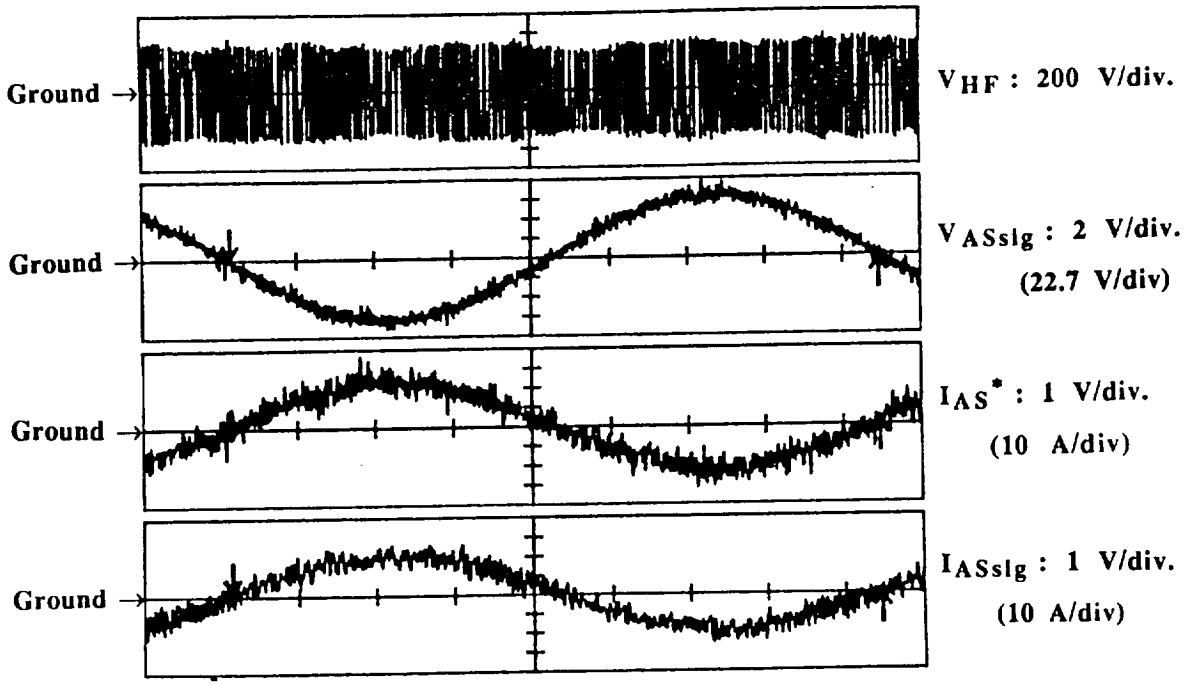


Fig. 6.17. Current Regulation and Unity Power Factor Operation of the Source When Induction Machine is in Generating Mode Of Operation at 200 Hz with Full Flux and Torque Command Applied. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Phase A Line to Neutral Source Voltage Control Signal: $V_{ASsig}$ : 2 V/div (22.7 V/div). Phase A Source Line Current Reference Signal: $I_{AS}^*$ : 1 V/div (10 A/div). Phase A Source Line Current Measured Signal: $I_{ASsig}$ : 1 V/div (10 A/div).Time/div: 2 msec.

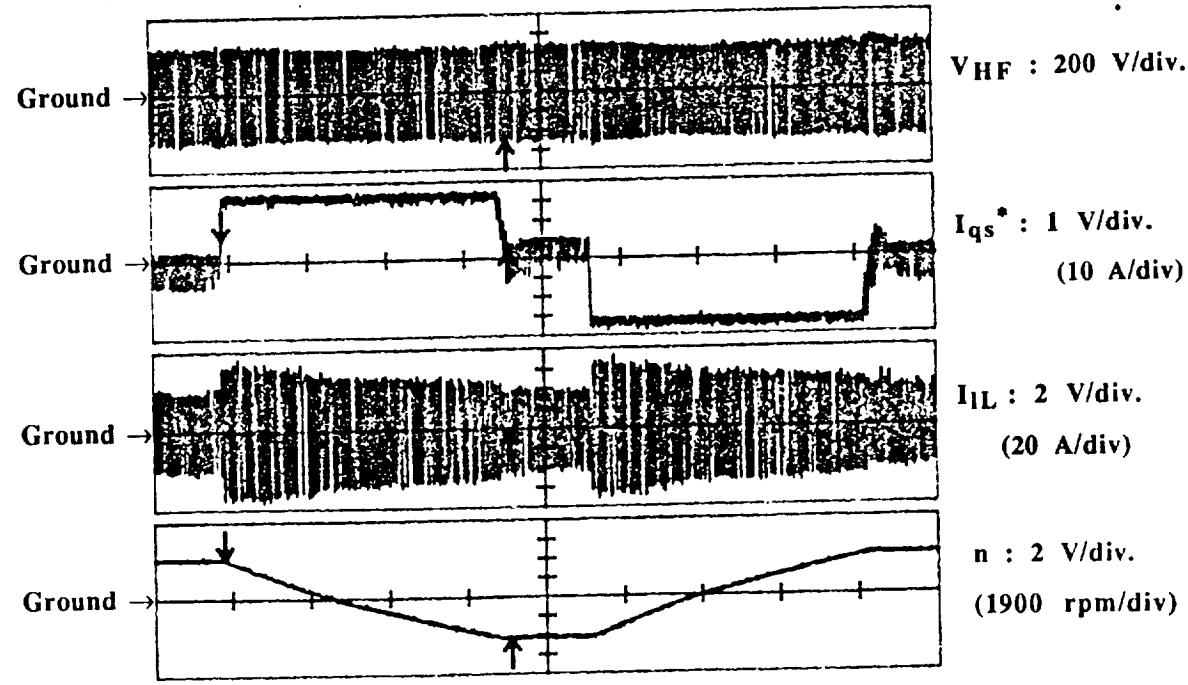


Fig. 6.18. Speed Reversal of Induction Machine Under No Load and in Speed Regulation Mode with Full Flux and Torque Command Applied During the Speed Reversal Transient. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Torque Component Current Command: $I_{qs}^*$ : 1 V/div (10 A/div). Induction Machine Phase C Line Current: $I_{CL}$ : 2 V/div (20 A/div). Speed of the Induction Machine: n : 2 V/div (1900 rpm/div). Time/div: 5 sec.

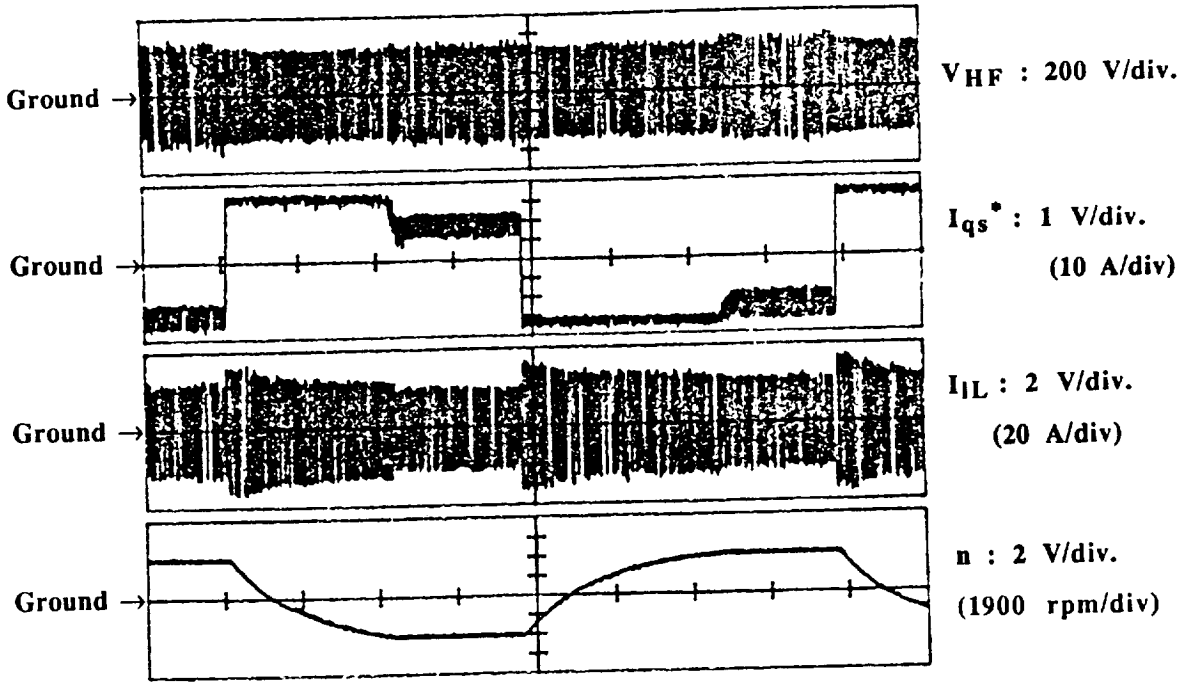


Fig. 6.19. Speed Reversal of Induction Machine Under LOAD and in Speed Regulation Mode with Full Flux and Torque Command Applied During the Speed Reversal Transient. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Torque Component Current Command: $I_{qs}^*$ : 1 V/div (10 A/div). Induction Machine Phase C Line Current: $I_{CL}$ : 2 V/div (20 A/div). Speed of the Induction Machine: n : 2 V/div (1900 rpm/div). Time/div: 10 sec.

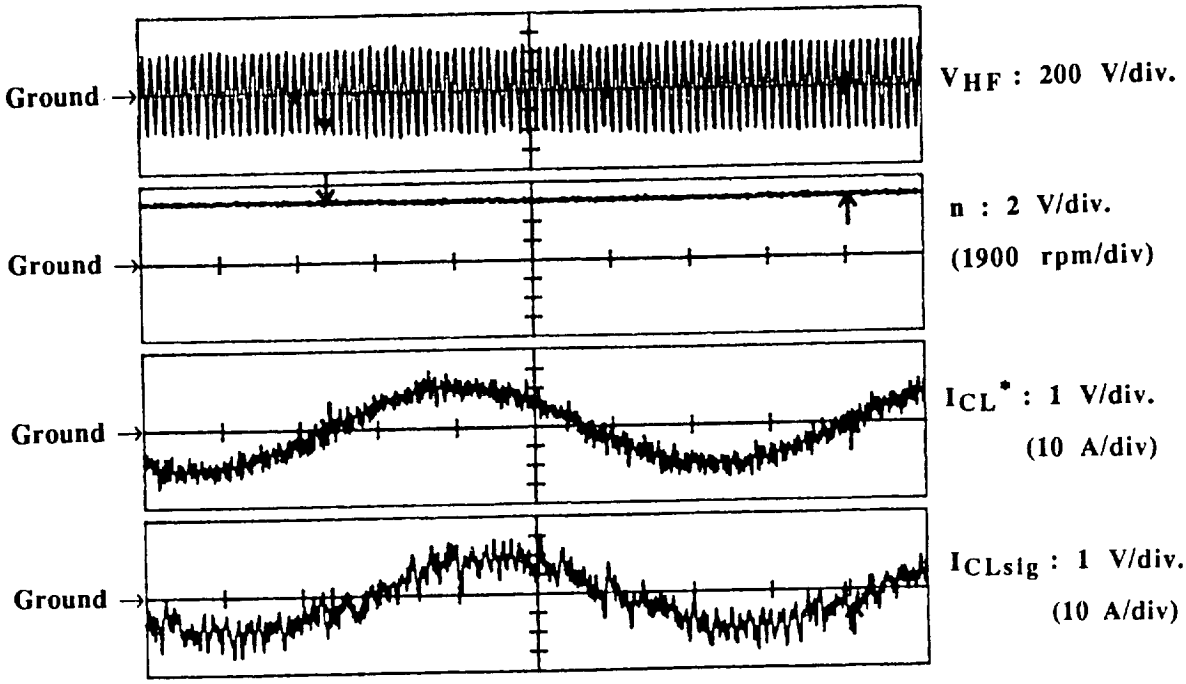


Fig. 6.20. No Load Operation of Induction Machine at 300 Hz, 6000 rpm with 2/3 Rated Flux Applied in Speed Regulation Mode. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Speed of the Induction Machine: n : 2 V/div (1900 rpm/div). Phase C Load Line Current Reference Signal: $I_{CL}^*$ : 1 V/div (10 A/div). Phase C Load Line Current Measured Signal: $I_{CLsig}$ : 1 V/div (10 A/div). Time/div: 500 μsec.

### 6.3.4 Test of the Induction Machine at Higher Frequencies by Decoupling it from the DC Machine

To demonstrate that current regulation can be achieved through the second generation converter for the rated frequency of induction machine and even at higher frequencies in field weakening region, the induction machine was decoupled from the DC machine to overcome the speed limitation problem at the expense of being able to test only at no load. Figures 6.20 through 6.24 are presented for this purpose. Fig. 6.20 shows 300 Hz and 6000 rpm operation in speed regulation mode with 2/3 rated flux applied. Careful observation of current regulation for this operation reveals some phase delay between the reference and real current. Fig 6.21 shows another view of this current regulation. The reason for the phase delay between the reference and real current is because of increased operating frequency and poor performance of the Direct ON-OFF current regulator at higher frequencies. When induction machine is operated at 300 Hz, 6000 rpm with rated flux rather than the 2/3, the load side current regulation starts to become poor and insufficient due to increased back emf. In this case, higher value of high frequency peak link voltage is required at the expense of increased link losses as pointed out earlier. Fig. 6.22 shows this type of poor current regulation for rated flux operation case. As seen from the figure, much worse phase delays are introduced due to the poor and insufficient current regulation.

Fig. 6.23 shows a higher frequency of operation with 2/3 rated flux applied. This time the frequency is 450 Hz and speed of the machine is 9000 rpm. Again an insufficient current regulation with a large phase delay is observed. Fig 6.24 shows another view of this current regulation. By weakening the field further or increasing peak link voltage this problem can be overcome. Besides, utilization of a mode controller introduced in Reference [4] would be required for the frequencies higher than 400-500 Hz to have a better performance out of the current regulator.

## 6.4 Conclusion

It has been shown in this chapter that the second generation three phase to three phase converter based on a parallel resonant 20 kHz HF link is capable of absorbing powers in the range of 9.86 kW (normal dyno loading mode) and delivering power in the range of 6.4 kW (regenerative mode delivering power to the source). Therefore, as required in the specification, this system successfully implements a high speed 10 hp

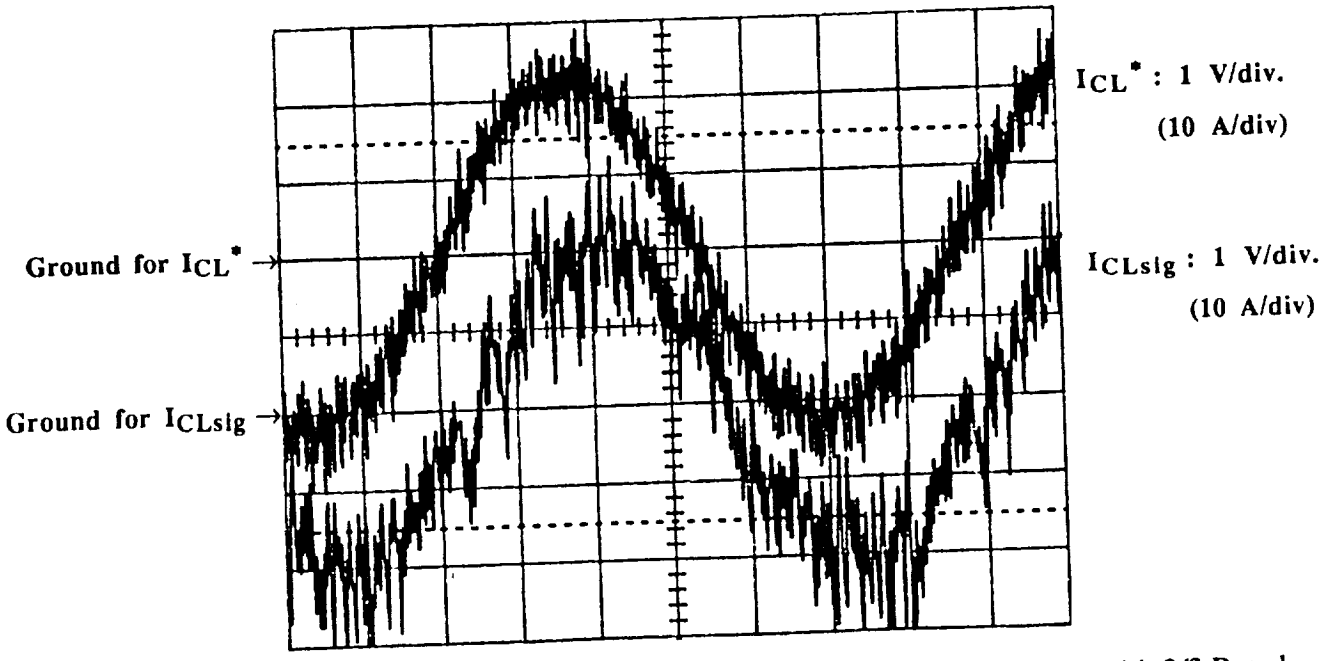


Fig. 6.21. Current Regulation of Induction Machine at 300 Hz, 6000 rpm with 2/3 Rated Flux Applied. Top Trace: Phase C Load Line Current Reference Signal: $I_{CL}^*$ : 1 V/div (10 A/div). Phase C Load Line Current Measured Signal: $I_{CLsig}$ : 1 V/div (10 A/div). Time/div: 500 µsec.

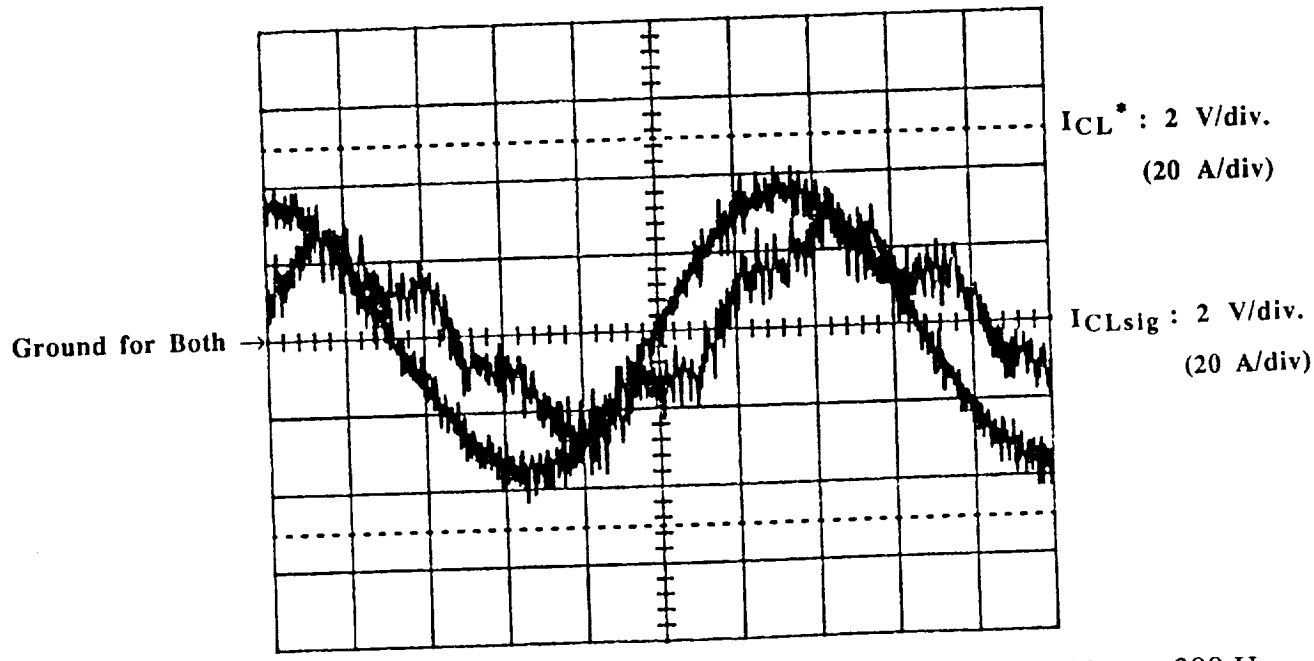


Fig. 6.22. Poor and Insufficient Current Regulation of Induction Machine at 300 Hz, 6000 rpm with Full Rated Flux Applied. Top Trace: Phase C Load Line Current Reference Signal: $I_{CL}^*$ : 2 V/div (20 A/div). Phase C Load Line Current Measured Signal: $I_{CLsig}$ : 2 V/div (20 A/div). Time/div: 500 µsec.

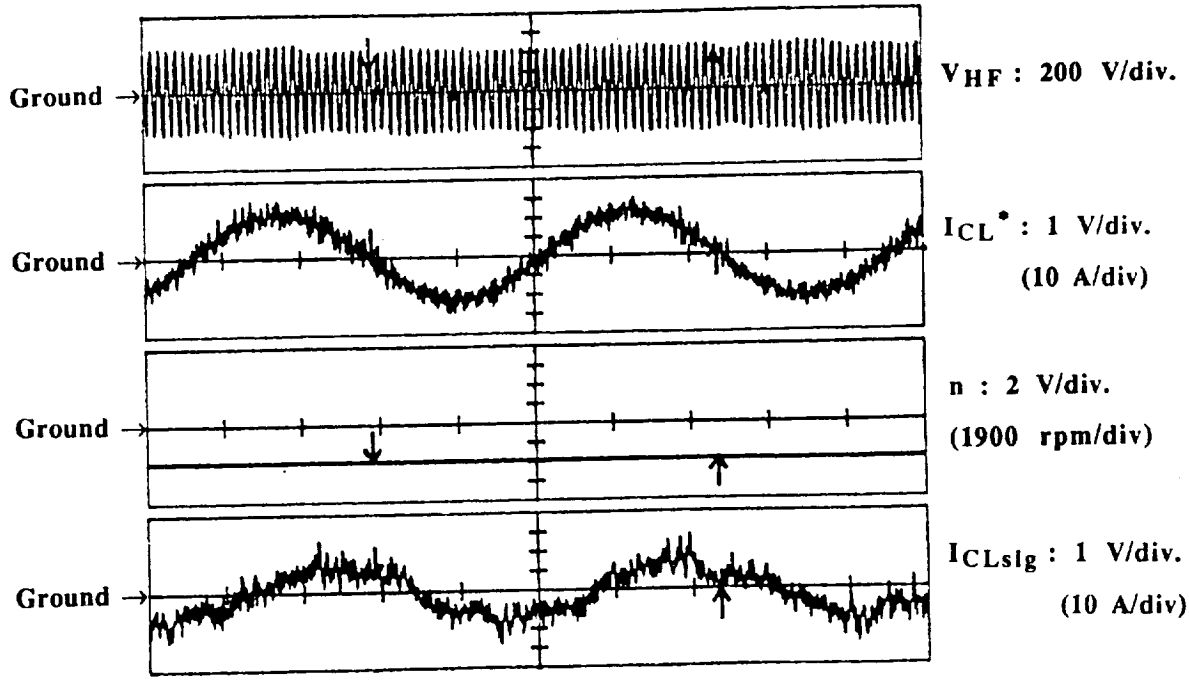


Fig. 6.23. No Load Operation of Induction Machine at 450 Hz, 9000 rpm with 2/3 Rated Flux Applied in Speed Regulation Mode. From the Top Respectively; HF Link Voltage: $V_{HF}$ : 200 V/div. Phase C Load Line Current Reference Signal: $I_{CL}^*$ : 1 V/div (10 A/div). Speed of the Induction Machine: n : 5 V/div (4750 rpm/div). Phase C Load Line Current Measured Signal: $I_{CLsig}$ : 1 V/div (10 A/div). Time/div: 500 µsec.

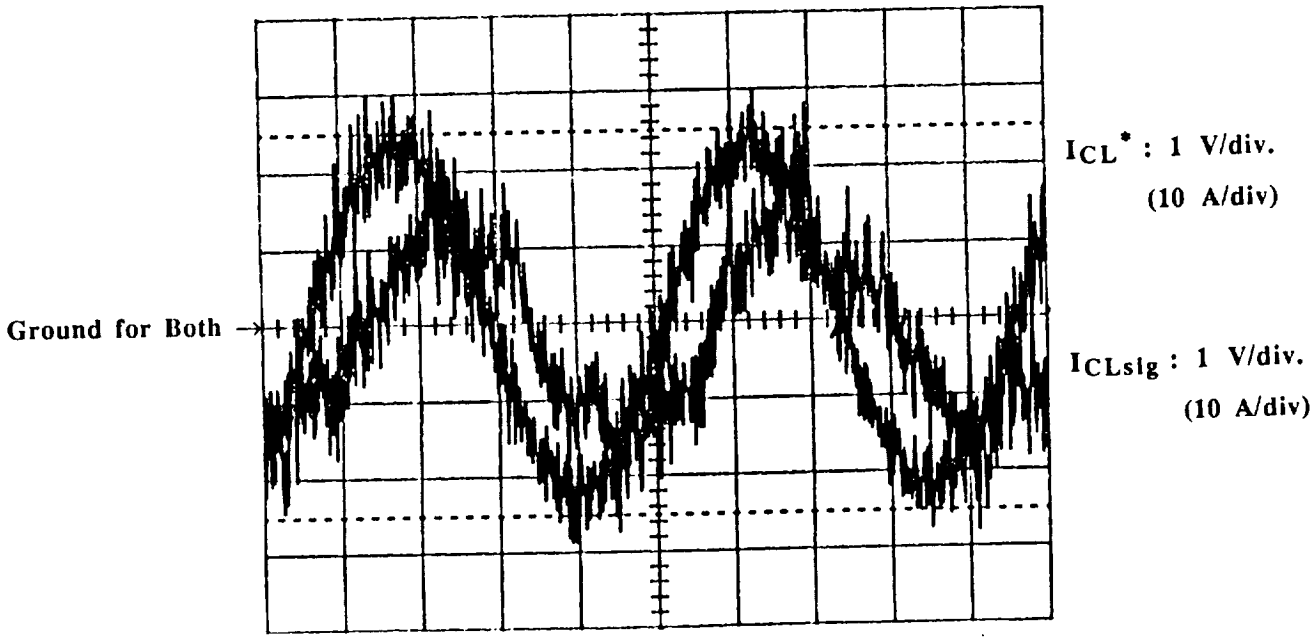


Fig. 6.24. Poor and Insufficient Current Regulation of Induction Machine at 450 Hz, 9000 rpm with 2/3 Rated Flux Applied. Top Trace: Phase C Load Line Current Reference Signal: $I_{CL}^*$ : 1 V/div (10 A/div). Phase C Load Line Current Measured Signal: $I_{CLsig}$ : 1 V/div (10 A/div). Time/div: 500 µsec.

induction machine operating as an AC dynamometer for operation at its rated power and frequency range.

## 6.5 References

1. T.A. Lipo and P. Sood," Study of the Generator/Motor Operation of Induction Machines in a High Frequency Link Space Power Systems", NASA Report, Contract No. NAG3-631, Sept. 1986.
2. P. Sood and T.A. Lipo,"Power Conversion Distribution System Using a Resonant High Frequency AC Link", Conf. Record of IEEE IAS Annual Meeting, Oct.1986, pp 533-541
3. P. Sood, T.A. Lipo and I. Hansen,"A Versatile Power Converter for High Frequency Link Systems", In Conf. Rec. 1987 Applied Power Electronics Conference, March 2-6, 1987, San Diego CA.
4. T.A. Lipo and S.K. Sul, "Design and Test of a Bidirectional Speed and Torque Control of Induction Machines Operating From High Frequency Link Converter", NASA Report, Contract No. NAG3-786, April 1988

# Chapter 7
# Conclusions and Suggestions for Future Work

## 7.1 Conclusions

This report has detailed steps taken in the design of a 10 hp high speed AC dynamometer utilizing a static power conversion employing a high frequency AC link. Test results of second generation MCTs, considered as the switch elements for the second generation power converter to be used for the dyno, showed that the MCTs are still in the stage of development and they have still problems with their turn-on and off characteristics. A new MCT gate drive chip tested along with the second generation devices was also shown to have some defects, specifically it was unable to supply a reliable gate drive in agreement with the gating logic signal. Utilization of these devices in zero voltage switching applications was shown to have some drawbacks because of high turn-on voltage requirements. Due to their unreliability in switching and high turn-on voltage requirement in zero voltage switching applications, the MCTs were not preferred to be used as switching devices in the construction of the second generation three phase to three phase power converter which was designed to be used for the 10 hp AC squirrel cage dynamometer.

Review of the design and test of the first generation three phase to three phase power converter and field oriented controlled induction machine drive system based upon PDM converters and 20 kHz parallel resonant HF AC link has shown that this system is not capable of handling the proposed power level required to drive a 10 hp induction machine as an AC dynamometer. Therefore, the need for the construction of the second generation converter became imperative. The "Insulated Gate Bipolar Transistors" (IGBT) type device was chosen as the most convenient switching devices for this new converter. To increase the operational reliability of the overall system and to gain from the building time and cost of the system, a bilateral switch realized with a one gate controlled switch imbedded in a diode bridge is preferred for the new converter at the expense of increased conduction losses and reduced system efficiency.

The experimental results have shown the need for an increased energy storage capacity for the parallel resonant HF AC link tank circuit to reach the proposed power level transfer. Specifically, it was determined that the low energy storage capacity of the resonant tank circuit causes difficulties in the regulation of the peak link voltage for increased power level transfer. To overcome this difficulty, new resonant tank circuit

inductors had to be constructed. Studies have shown that the air-core litz wire inductors have better quality factor than their moly permalloy powder core litz wire counterparts for the same value and ratings. Hence, air-core litz wire resonant tank circuit inductors were chosen as the preferred technology. On the other hand, the increased energy storage capacity of the resonant tank circuit introduces increased the HF link losses by degrading the overall converter efficiency. This is, of course, the drawback of any link with an increased energy storage capacity.

Three phase 60 Hz source voltage level was increased to 208 V rms to reduce the conduction losses of the source side PDM converter and to get rid of the dependence of the system to a 3Ø auto transformer at the input. This led to a poor and insufficient current regulation of the source for selected peak link voltage level. Later, an optimal value for the source voltage was selected and good current regulation for the source was achieved.

Finally, the second generation three phase to three phase power converter and induction machine drive system constructed and tested in the University of Wisconsin-Madison WEMPEC Laboratory based upon PDM converter and 20 kHz parallel resonant HF AC link technology. The system was shown to be capable of driving the induction machine as an AC dynamometer up to the specified power range of 10 hp (7.46 kW) and speed range of 18,000 rpm. The same system also offers the induction machine full 4-quadrant operation either in speed or torque regulation modes of operation with good and fast dynamic response and low harmonic distortion. The demagnetization of the induction machine is also very easily possible within only a few cycles of HF link in case of faulty situations with this system.

## 7.2 Suggestions for Future Work

### Design and Test of Completely Isolated Three Phase to Three Phase Induction Motor/Induction Generator System via Parallel Resonant High Frequency AC Link

As known, the experimental breadboard consists of a three phase to three phase power converter and induction machine drive system based upon a PDM converter utilizing 20 kHz parallel resonant HF AC link technology. The overall system is capable of driving the induction machine of the system as an AC dynamometer up to the power range of 10 hp (7.46 kW) and speed range of 18,000 rpm. When the induction machine is operated as an AC dynamometer, the power generated by induction machine is simply delivered back to the 60 Hz source at unity power factor via this converter. However, in

the real system the generated power can be used to drive another induction machine. In particular, in the case of a system where two induction machines are utilized at both sides of the converter in which one of them is operated in generating and the other is in the motoring mode of operation, the real power control between the two machine via a parallel resonant HF AC link is a challenging problem which should be studied to get a general insight about the application of high frequency link systems to isolated systems.

Proposed as the major effort for the rest of the year of 1991 is the operation of a complete "power system" comprised of two induction machines which are interconnected via parallel resonant HF AC link and the associated switching PDM converters. One machine will be driven by a prime-mover and operated as an induction generator. The other induction machine will be used as the load of the high frequency link by operating as a motor. The two machines may be operated with completely different frequency and voltages. However, the real power of the generator will be controlled so as to maintain the proper link voltage and match the power between the input and output. The simple block diagram of the proposed system is shown in Fig. 7.1. The overall configuration can be analyzed by means computer simulations and the results will be verified with hardware on a prototype system.

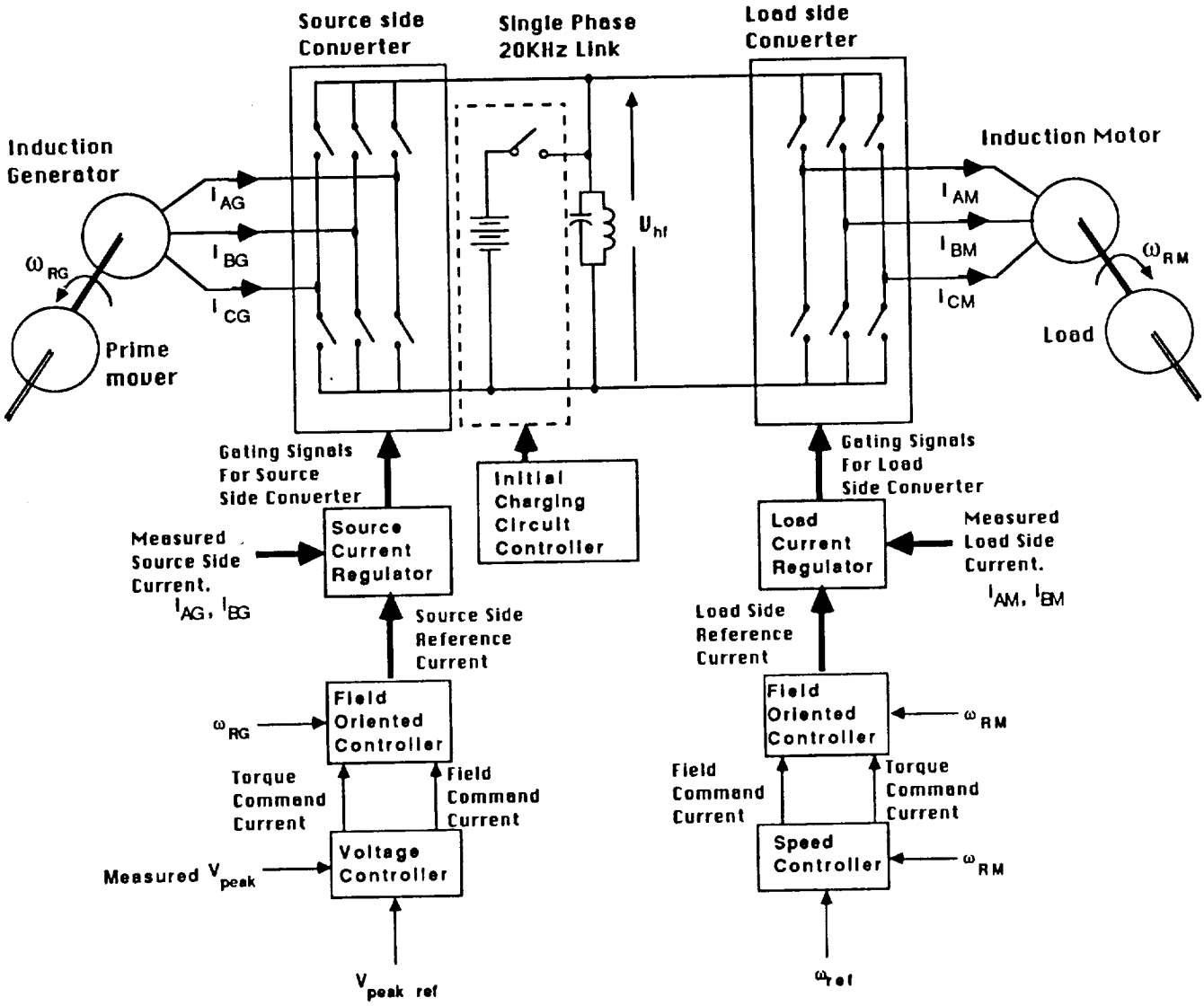


Fig. 7.1. Power Circuit and System Control Block Diagram of Completely Isolated 3Ø to 3Ø Power Conversion System Based Upon PDM Converter and Parallel Resonant HF ac Link Technology.