Combinatorial FSK Modulation for Power-Efficient High-Rate Communications

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more than 98 % of the inherent capacity.

From the equations cited in Schneider[4], a general expression can be formed which describes the symbol error rate performance of noncoherent CFSK in AWGN:

(NOTE: For M ≥ 3, this expression is valid only as an asymptotic form for large R.)

$$P_e(M) = \frac{M}{D} \sum_{r=2}^{D} (-1)^r \binom{D}{r} Q_2(\alpha,\beta,r) \exp\left[-R\left(1-\frac{1}{r}\right)\right]$$

where $D = N - M + 1$, $\quad R = \frac{E_b}{N_0} = \left(\frac{k}{M}\right)\left(\frac{E_s}{N_0}\right)$

$$k = \log_2\binom{N}{M} \text{ bits per symbol}$$

$$Q_2(\alpha,\beta,r) = \begin{cases} \dfrac{1 + r\,Q(\alpha,\beta) - Q(\beta,\alpha)}{r+1} & \text{for } M = 2 \\ 1 & \text{otherwise} \end{cases}$$

$$\alpha = \sqrt{\frac{2Rr}{r+1}}, \quad \beta = \frac{\alpha}{r}$$

$$Q(\alpha,\beta) = \text{Marcum's Q function}$$

Marcum's Q function is an integral which describes the cumulative density function (CDF) of a Rician variable, as it pertains to the envelope of a sinusoid plus narrowband AWGN[6]. No closed form solution exists for this integral; however, a simple recursive procedure for evaluating it is given by Parl[7].

The probability P_b of committing one or more bit errors is related to P_e by $P_b = 1 - (1 - P_e)^{1/k}$. Evaluating P_b for N=9 and 1≤ M ≤ 8 yields the bit error rate (BER) performance curves shown in Figure 1. As is evident with other higher-order modulation schemes, increasing signal dimensionality implies an associated increase in Eb/No to maintain a fixed BER. Note that dividing the available transmit energy equally over a large number of tones (M ≈ N) results in substantially degraded power and spectral efficiency.

The spectral efficiency of CFSK is given by:

$$\frac{R}{W} = \frac{(\text{ bits per symbol }) \cdot (\text{ symbols per second })}{\text{bandwidth in Hertz}}$$

$$= \frac{k \cdot (1/T_{symbol})}{(N/T_{symbol})} = \frac{k}{N} = \frac{\log_2\binom{N}{M}}{N}$$

The highest possible R/W value for a given N is obtained when M = Int (N/2). The following table demonstrates that N and M must grow rapidly to support CFSK spectral efficiencies above 0.85 bits / sec / Hz. Since modulator and demodulator complexity are tied to N and M, this value is also a rough limit on practically attainable R/W for CFSK.

Desired R / W	N	M	Actual R / W
0.5000	2	1	0.5000
0.5500	4	2	0.6462
0.6000	4	2	0.6462
0.6500	5	2	0.6644
0.7000	6	3	0.7203
0.7500	8	4	0.7662
0.8000	1 1	5	0.8047
0.8500	1 6	8	0.8532
0.9000	2 8	1 4	0.9021
0.9500	6 8	3 4	0.9504

Figure 2 depicts the spectral efficiency of CFSK as a function of Eb/No and N for several fixed values of M. Interestingly, the peak R/W values are all attained at an Eb/No ≈ 11.2 dB, essentially independent of M. The ability to trade off spectral efficiency, power efficiency and modem hardware complexity through the choice of N and M values is an important property of CFSK.

EXAMPLE: Compare the following CFSK schemes (both are required to operate with a 1.0E-5 BER) :

$$\binom{5}{3} = 10 \qquad k = 3.3 \qquad \frac{R}{W} = 0.664 \qquad \frac{E_b}{N_0} \approx 13.1 \text{ dB}$$

$$\binom{10}{3} = 120 \qquad k = 6.9 \qquad \frac{R}{W} = 0.691 \qquad \frac{E_b}{N_0} \approx 10.1 \text{ dB}$$

Doubling N has more than doubled k AND provided a 3 dB Eb/No reduction, without sacrificing BER performance and actually increasing R/W slightly. The second CFSK format is clearly favorable for a high data

rate system, provided the bandwidth utilization and modest hardware complexity increases are acceptable.

Sklar[8] compares the bandwidth and power efficiencies of noncoherent single-tone N-ary FSK, coherent N-ary PSK and coherent N-ary QAM modulation. Traditional N-ary FSK spectral efficiency rapidly drops below 0.5 for N>4, whereas coherent PSK and QAM provide high R/W at the expense of higher Eb/No. As the following table shows, CFSK provides useful R/W improvement over traditional FSK, operates with comparable Eb/No values, and does not require coherent processing to obtain it.

	R/W	Eb/No in dB
Noncoherent FSK	< 0.5	6 to 12
Noncoherent CFSK	**< 0.85**	**8 to 15**
Coherent ≤ 64 PSK *	1 to 6	9 to 27
Coherent ≤ 256 QAM *	4 to 8	15 to 30

* assuming ideal Nyquist filtering

Modulator Implementation

A CFSK modulator design concept is shown in Figure 3. Input source data is processed by a SYMBOL MAP function to yield binary codes at the transmit symbol rate. Each code points to a block of SAMPLE MEMORY locations containing quantized sample values for the chosen symbol. The least significant sample memory address bits are created by a COUNTER reset to zero at the symbol rate and incremented at the sample rate. The D/A converter (DAC) creates an analog CFSK symbol stream waveform based on the sequence of retrieved sample values. Spectral aliases at the DAC output are removed by an ANTI-ALIAS lowpass FILTER.

Digital processing in the CFSK modulator is very similar to that found in a numerically controlled oscillator (NCO) or direct digital synthesizer (DDS). Thorough discussions of DDS theory and applications can be found in[10-11]. Very large scale integrated (VLSI) circuit based DDS devices are currently available with sample rates up to 1 Gsample/sec; some devices include digital modulation capabilities.

The modulator output IF frequency can be flexibly selected within the constraint of a given sample rate. Sample memory content can be readily altered to generate the signalling tones at different frequencies. This property could be used for transmitter center frequency tuning in a frequency division multiple access (FDMA) network of users employing CFSK modulation.

Attempting to create tones with rapidly changing frequencies (e.g. for spread spectrum frequency hop systems) by using phase-locked loop (PLL) synthesizers or hybrid PLL / DDS schemes can yield large amounts of undesired spurious signal content. The specific mechanisms which give rise to this and the extent to which they degrade FSK communication system performance are reported by Alexovich and Gagliardi[12]. By using a sample rate equal to an integer multiple of the symbol rate, the DDS-like modulator can perform phase continuous symbol-to-symbol switching. Modulator output signal quality depends mainly on spectral purity of the DAC and an appropriate upconversion frequency plan devoid of mixer spurious product responses.

Amplifying a CFSK signal resident at microwave frequencies with a traveling-wave tube amplifier (TWTA) will create undesirable distortion products unless some degree of backoff is used. Precompensation of the modulator symbol samples may improve this situation somewhat. If possible, the use of a solid-state power amplifier (SSPA) may also be beneficial. A third possibility would be to construct several parallel DAC / RF upconverter / amplifier paths, each being utilized to process a subset of the M tones in any given CFSK symbol. The DDS-like digital processing could easily be extended to support a parallel path structure; the main concern is the attendant analog / RF hardware growth, particularly for large values of M.

Demodulator Implementation

A CFSK demodulator design concept is shown in Figure 4. Tracing the main signal processing path, the input CFSK analog signal (assumed to be imposed on an IF carrier) is downconverted to baseband by a mixer and a local oscillator (LO). The LO signal is formed by a DDS, a DAC, and an ANTI-ALIAS lowpass FILTER. The lowpass portion of the mixer output is then quantized by an A/D converter (ADC) to create signal samples. The samples are analyzed by a real-time Discrete Fourier Transform (DFT) processor to extract spectral content from each of the N signalling tone spectral regions in parallel. Signal strength in each DFT bin is then measured by a bank of DETECTORS, whose outputs are used to COMPUTE TEST STATISTICS. Finally, the M LARGEST statistic VALUES are identified, and a MAP function is used to translate the associated DFT bin numbers INTO recovered SYMBOL DATA.

Closed-loop SYMBOL SYNChronization can be achieved by advancing or retarding the sample clock in accordance with a maximum-likelihood (ML) symbol time displacement estimate. These symbols can also be used in the FREQUENCY ACQUISITION process, which combines LO stepping with examinations of the detected DFT bin outputs for proper content (averaged over several symbol times to remove noise effects in a low SNR environment). Once frequency acquisition occurs, TRACKING information is easily obtained from an ML estimator whose inputs are the detected DFT bins adjacent to the outer spectral edge tones of the CFSK signal. Similar strategies and accompanying performance analyses for traditional noncoherent single-tone N-ary FSK signalling are presented in Chadwick and Springett[13].

The conventional view of noncoherent FSK receiver structure espouses the use of square-law energy detection. In signalling schemes such as CFSK, however (where the number of equiprobable equal-energy symbols is much larger than the number of signalling tones used), VonDerEmbse et.al.[14] show that linear-law amplitude detectors are highly superior in performance.

Pipelined DFT realization with dedicated hardware is the DSP implementation of choice for a high-speed CFSK demodulator. Small transform size ($N \leq 64$) high-speed DFTs are commonplace in radar signal processors; VLSI devices for such applications have recently become available[15-16].

Practical DFT processors can also be implemented with acousto-optic (AO) Bragg cells, charge-coupled devices (CCD's) and surface acoustic wave (SAW) devices. Each of these is being considered for potential use in satellite on-board FDMA block demultiplexing[5]. CFSK demodulation with any of these alternative signal channelizer technologies may also be attractive, particularly if N is large.

Signal Simulation

A memory pattern comprised of time and amplitude quantized CFSK { N=4, M=2 } signal samples was reconstructed as an analog waveform by a commercial arbitrary waveform synthesizer (AWS) unit. One psuedo-random walk through each of the 6 unique symbol time waveforms is shown at the top of Figure 5.

Continuously repeating this symbol sequence results in the spectral content shown at the bottom of Figure 5. According to the general noncoherent FSK theory, adjacent signalling tones must be separated spectrally by at least the reciprocal of the symbol time[9]. A value twice as large was used here to allow clear observation of the modulation content impressed on the tone frequencies. Note the well-confined spectral occupancy; this is a direct consequence of the type of signalling being performed, not the result of an explicitly imposed filtering operation.

System-Level Issues

Size, weight, power and thermal management constraints imply that a spacecraft resident CFSK modem would have to be constructed with a high degree of monolithic integration. All of the digital processing functions shaded in Figures 3 and 4 are totally amenable to VLSI realization, perhaps as a single device. High-speed commercial ADC and DAC's are currently available in hybrid packages. The simple remaining circuitry could easily be incorporated into a single hybrid package. Thus, space qualified CFSK modulator and demodulator designs appear to be achievable with current technology.

FSK signalling may be contemplated for use in an environment where time-varying channel conditions must be adaptively responded to. In such cases, Hingorani and Chesler[17] suggest measuring the statistics of the quantities which form the decision variable, and processing them in a ML-like sense to yield a reliable estimate of the bit error rate. This approach provides on-line performance monitoring without test pattern transmissions. Extending this technique to work with CFSK signals may be useful.

Areas for Further Study

Three main issues associated with the use of CFSK modulation appear to warrant simulation studies. Combining CFSK with error corrective coding (ECC) would further enhance efficient use of available spacecraft power for a given data capacity and BER. The acquisition and tracking algorithms proposed for single-tone FSK communications[13] should be validated for CFSK use. Assessing the BER degradation effects of CFSK signal amplification by a TWTA and the potential of utilizing precompensation techniques would be a beneficial effort.

Conclusion

The CFSK modulation scheme presented in this paper has been shown to be viable for use in modern high data rate digital communications systems, including those which employ satellites. This viability is due in large part to the advances in signal processing technology achieved over the past quarter century. The large variety of potential CFSK schemes gives the system engineer considerable latitude in selecting a desired balance of power efficiency, spectral efficiency and modem hardware complexity.

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References

NOTE: Vendor application notes are cited to provide relevant examples of state-of-the-art processing techniques and/or capabilities, not as specific vendor or product endorsements.

[1] D. Slepian, "Permutation Modulation" , *Proc. IEEE,* vol. 53, pp.228-236, March 1965.

[2] E. Brookner, "Nonorthogonal Coding", *IEEE Trans. Communication Technology,* vol. COM-13, No.4, pp.550-552, December 1965.

[3] E. Brookner, "The Performance of FSK Permutation Modulations in Fading Channels and Their Comparison Based on a General Method for the Comparison of M-ary Modulations", *IEEE Trans. Communication Technology,* vol. COM-17, No. 6, pp.616-640, December 1969.

[4] H. L. Schneider, "Data Transmission with FSK Permutation Modulation", *Bell Syst. Tech. J.,* vol. 47, pp.1131-1138, July-August 1968.

[5] J. L. Harrold, J. M. Budinger and G. H. Stevens, "On-Board Switching and Processing", *Proc. IEEE,* vol. 78, No. 7, pp.1206-1212, July 1990.

[6] A. D. Whalen, "Detection of Signals in Noise", Academic Press Inc., 1971, pp.103-108.

[7] S. Parl, "A New Method of Calculating the Generalized Q Function", *IEEE Trans. Inform. Theory,* vol. IT-26, pp.121-124, January 1980.

[8] B. Sklar, "Digital Communications Fundamentals and Applications", Prentice Hall, 1988, pp.393-399.

[9] B. Sklar, "Digital Communications Fundamentals and Applications", Prentice Hall, 1988, pp.150-154.

[10] R.J.Zavrel Jr. and G. Edwards (Editors), Application Notes in "The DDS Handbook", pp.1-20, second edition, July 1990. Published by Stanford Telecommunications, Inc., Santa Clara, CA.

[11] R.H. Hosking, "Direct Digital Frequency Synthesis", 1973 *IEEE Intercon* Technical Papers, 6 pages.

[12] J. Alexovich and R.M. Gagliardi, "Effect of PLL Frequency Synthesizer in FSK Frequency-Hopped Communications", *IEEE Trans. Comm.,* vol. COM-37, No. 3, pp.268-276, March 1989.

[13] H. D. Chadwick and J.C. Springett, "The Design of a Low Data Rate MFSK Communication System", *IEEE Trans. Communication Technology,* vol. COM-18, No. 6, pp.740-750, December 1970.

[14] U.A. von der Embse, R.A. Scholtz and C.L. Weber, "Signal Design for Totally Phase-Incoherent Communications", *IEEE Trans. Comm.,* vol. COM-23, No. 2, pp.213-221, February 1975.

[15] Application Note: "Implementing Fast Fourier Transform Systems with the L64280/81 Chip Set", LSI Logic Digital Signal Processing (DSP) Databook, June 1990, pp.258-268.

[16] Applications Handbook: "UT69532 IQMAC (In-phase Quadrature Multiplier / ACcumulator)", United Technologies Microelectronics Center, 1989, 48 pages.

[17] G. D. Hingorani and D.A. Chesler, "A Performance Monitoring Scheme for FSK Transmission over Fading Channels", *IEEE Trans. Communication Technology,* vol. COM-16, No. 3, pp.388-392, June 1968.
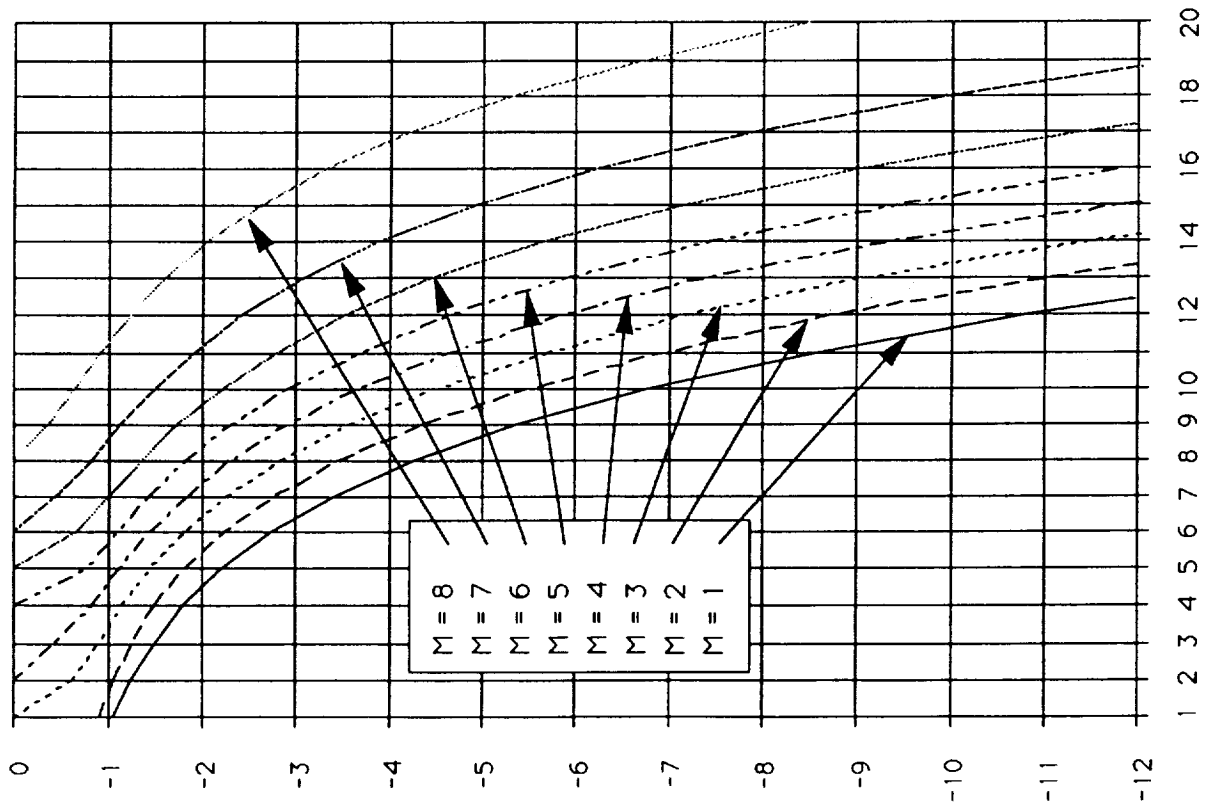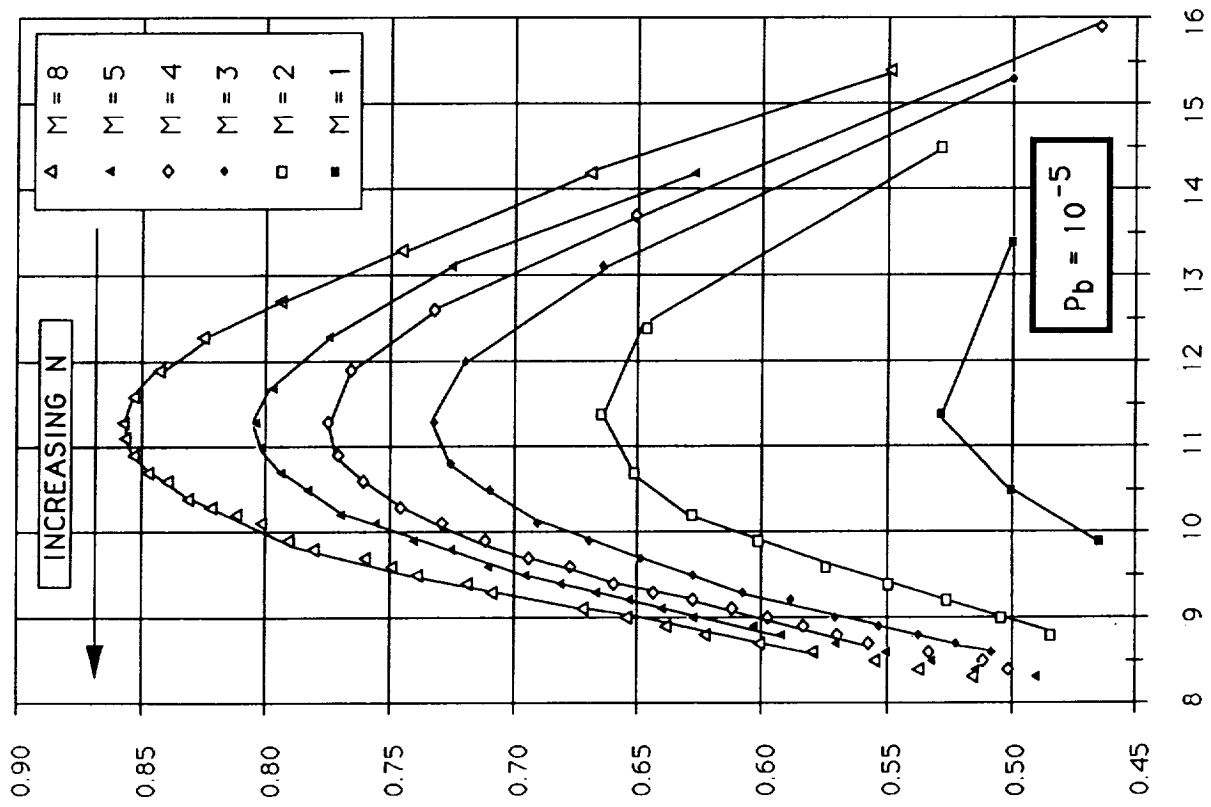
FIGURE 2 R/W (bits/sec/Hz) vs Eb/No (dB)

$P_b = 10^{-5}$

M = 8	▷
M = 5	◀
M = 4	◇
M = 3	◆
M = 2	□
M = 1	■

INCREASING N

FIGURE 1 log10 (Pb) vs Eb/No (dB) for N = 9

M = 8
M = 7
M = 6
M = 5
M = 4
M = 3
M = 2
M = 1

SAMPLE MEMORY

INPUT DATA → SYMBOL MAP → COUNTER → Symbol # 1 Samples / Symbol # 2 Samples / ⋮ / Symbol # S Samples → D / A CONVERT → ANTI-ALIAS FILTER → ANALOG OUTPUT

SYMBOL CLOCK ←

SAMPLE CLOCK

$$S = \frac{N}{M}$$
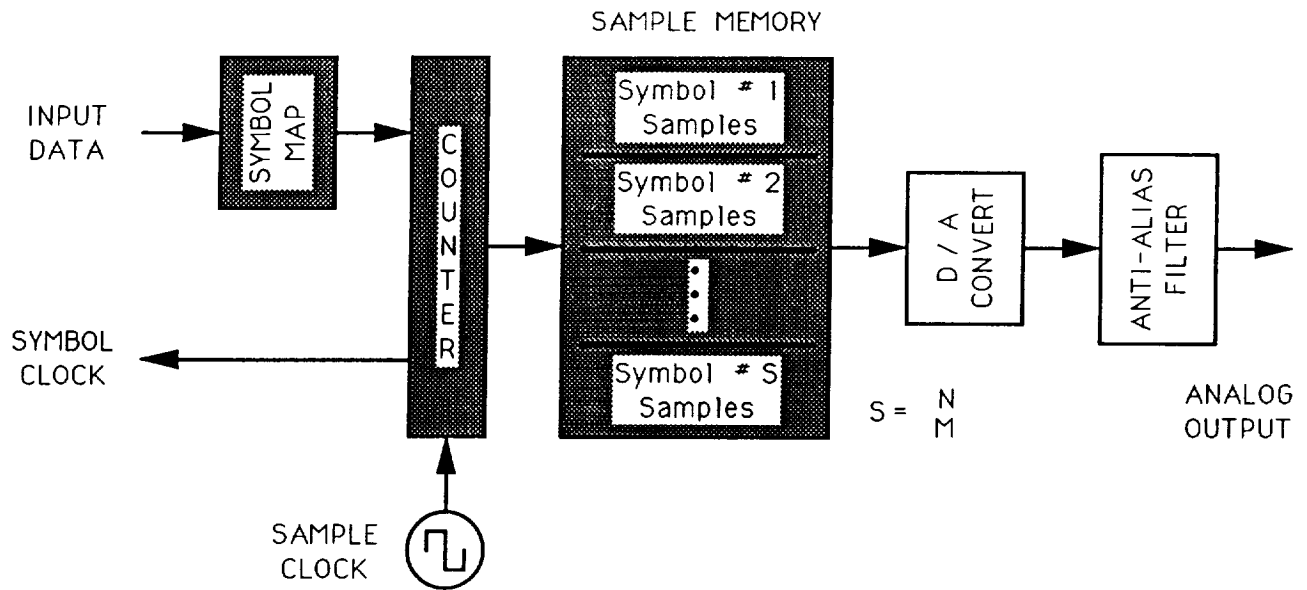
FIGURE 3   CFSK MODULATOR DESIGN CONCEPT

DIGITAL PROCESSING FUNCTIONS

SAMPLE CLOCK

SYMBOL SYNC

ANALOG INPUT → ⊗ → ADC → DFT → DETECTORS → COMPUTE TEST STATS → FIND M LARGEST → MAP INTO SYMBOL DATA → OUTPUT DATA

ANTI-ALIAS FILTER

REFERENCE OSCILLATOR

DAC ← DDS ← FREQUENCY ACQUISITION & TRACKING
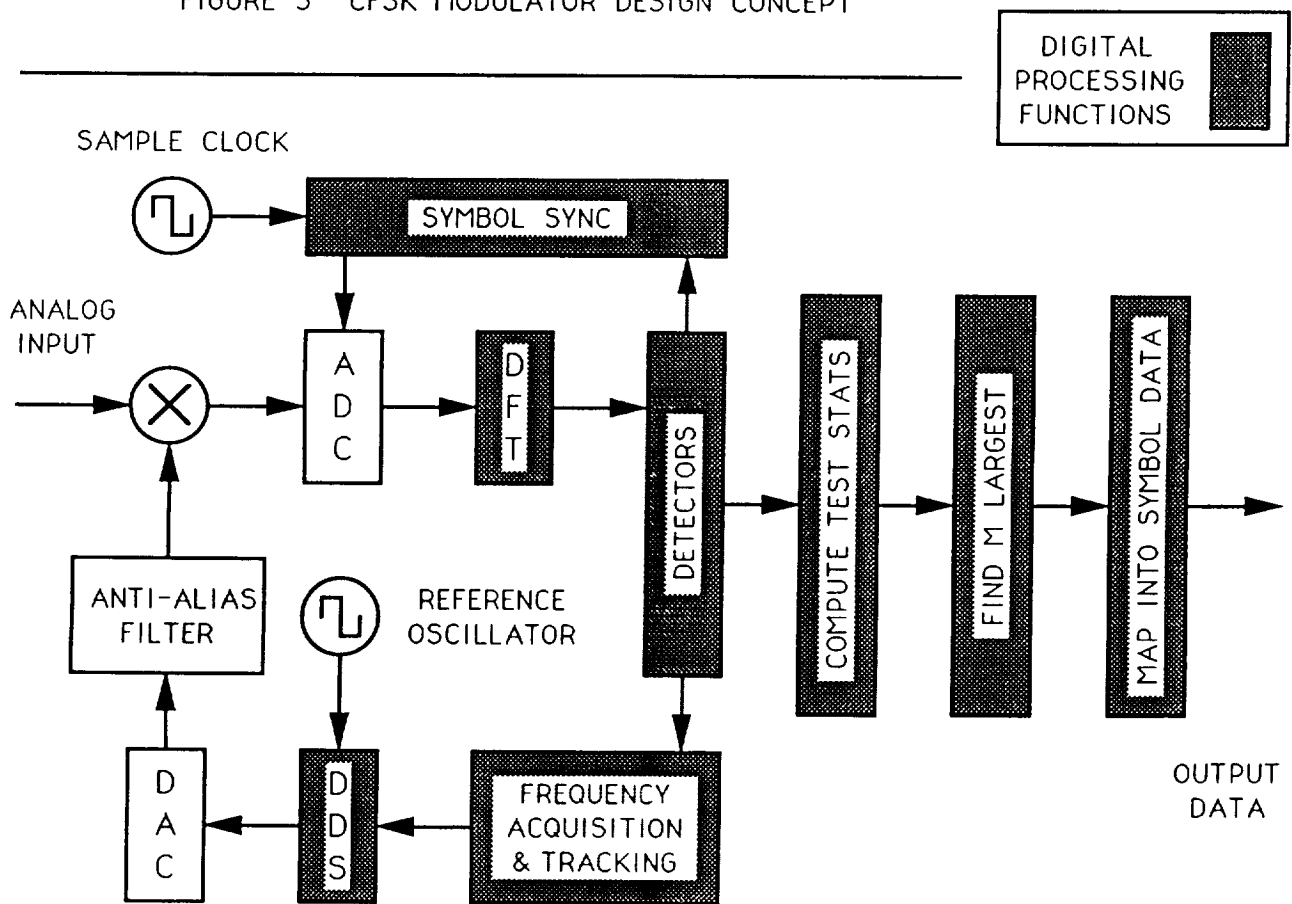
FIGURE 4   CFSK DEMODULATOR DESIGN CONCEPT

+1.97E+000

−1.97E+000
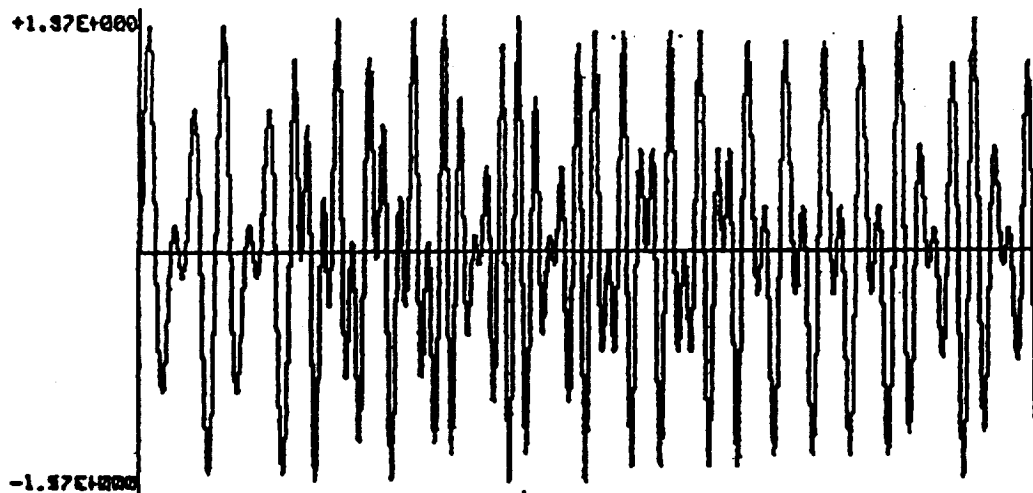
TIME DOMAIN (one instance of each symbol)

REF −2.0 dBm #ATTEN 30 dB

PEAK
LOG
6
dB/

WA SB
SC FC
CORR

CENTER 0 Hz   SPAN 4.000 MHz
  #RES BW 10 kHz   #VBW 30 kHz   #SWP 600 msec
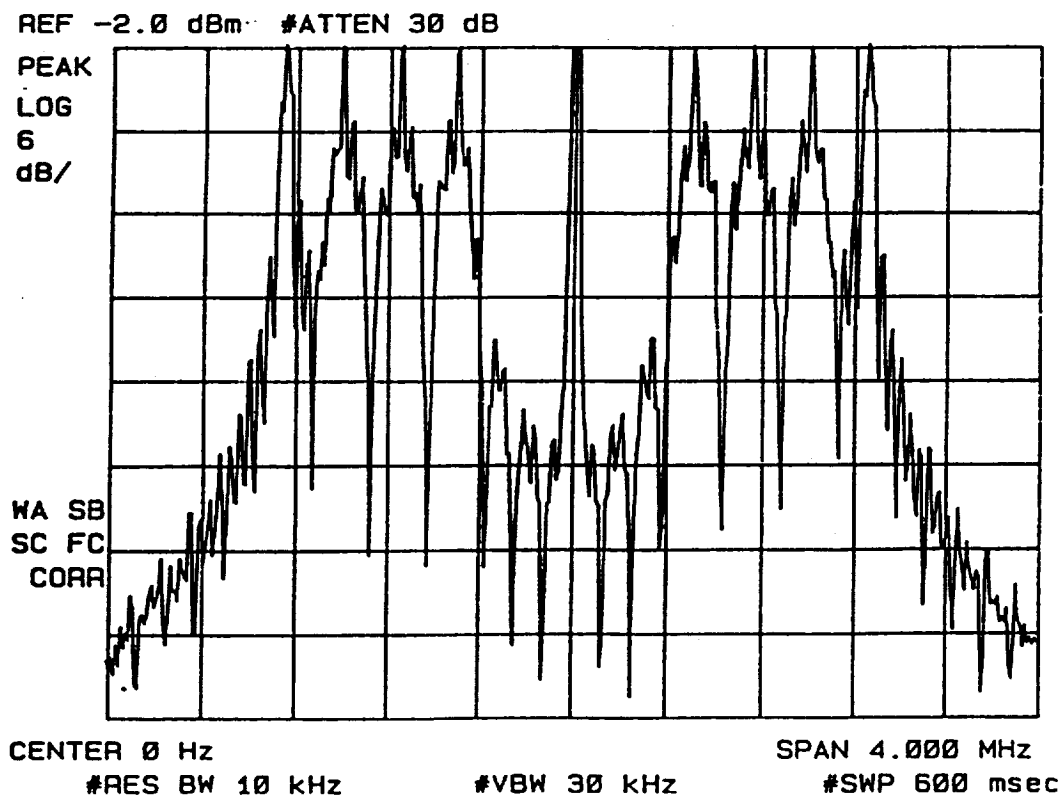
FREQUENCY DOMAIN (Symbol Rate = 0.5 * Tone Spacing)

FIGURE 5   AWS Simulation of $\begin{pmatrix} 4 \\ 2 \end{pmatrix}$ CFSK Modulation

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REPORT DOCUMENTATION PAGE

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
		Technical Memorandum

4. TITLE AND SUBTITLE

Combinatorial FSK Modulation for Power-Efficient
High-Rate Communications

5. FUNDING NUMBERS

WU - 650 - 60 - 21

6. AUTHOR(S)

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

National Aeronautics and Space Administration
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8. PERFORMING ORGANIZATION REPORT NUMBER

E - 6490

9. SPONSORING/MONITORING AGENCY NAMES(S) AND ADDRESS(ES)

National Aeronautics and Space Administration
Washington, D.C. 20546 - 0001

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

NASA TM - 105188
AIAA - 91 - 3532

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Unclassified - Unlimited
Subject Category 32

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

Deep-space and satellite communications systems must be capable of conveying high-rate data accurately with low transmitter power, often through dispersive channels. This paper investigates a class of noncoherent Combinatorial Frequency Shift Keying (CFSK) modulation schemes which address these needs. The bit error rate performance of this class of modulation formats is analyzed and compared to the more traditional modulation types. Candidate modulator, demodulator and digital signal processing (DSP) hardware structures are examined in detail. We conclude by discussing system-level issues and identifying areas for further study.

14. SUBJECT TERMS

Satellite communication; Satellite transmission; Modulation; Coding; Communication satellites; Frequency shift keying

15. NUMBER OF PAGES

10

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	