NASA Contractor Report-187555

Advanced Information Processing System for Advanced Launch System: Hardware Technology Survey and Projections

Richard Cole

THE CHARLES STARK DRAPER LABORATORY, INC.
CAMBRIDGE, MA 02139

Contract NAS1-18565
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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

This report is organized in four sections: Introduction, Technology Projection, Conclusion, and an Appendix. The introduction defines the task purpose and approach. The technology projection provides detailed information on technological capabilities which are relevant to AIPS/ALS. The next section summarizes the results of this effort. Appendix A provides a rationale and justification for technology projections by quoting appropriate research and development activity and market projections and also provides an extensive bibliography. The impact of the advanced technology on the AIPS building blocks in terms of performance, reliability and physical characteristics is an integral part of the architecture synthesis task and is discussed in the AIPS for ALS Architecture Synthesis report [Ref.1].

1.1 Purpose

The major goals of this effort are as follows: examine technology insertion options to optimize AIPS performance in the Advanced Launch System (ALS) environment, examine the AIPS concepts to ensure that valuable new technologies are not excluded from the AIPS/ALS implementations, examine advanced microprocessors applicable to AIPS/ALS, examine radiation hardening technologies applicable to AIPS/ALS, reach conclusions on AIPS hardware building blocks implementation technologies, and reach conclusions on appropriate architectural improvements. The hardware building blocks are the Fault Tolerant Processors, the Input/Output and InterComputer Networks and interfaces between the processors and the networks, viz., Input/Output Sequencers (IOS) and the InterComputer Interface Sequencers (ICIS).

In order to examine technology insertion options to optimize AIPS performance in the Advanced Launch System (ALS) environment an informal minimization problem is created: Minimize AIPS/ALS Technology Insertion Option Cost subject to the following constraints: insertion options are feasible implementations of the AIPS/ALS architecture and the options include the main relevant new technologies.

We want to examine the AIPS concepts to ensure that valuable new technologies are not excluded from AIPS/ALS implementations by first identifying the technologies which will benefit computer systems that are similar to AIPS except that they do not have AIPS advanced fault tolerance features. Once this is accomplished the architecture synthesis can attempt to insert these technologies into AIPS/ALS.

Advanced microprocessors will be examined in order to select one for use in the AIPS/ALS. The determination of most appropriate will include consideration of throughput, reliability, and cost.

Radiation hardening technologies applicable in the AIPS/ALS are those which reduce the occurrence of radiation related problems within AIPS/ALS during its mission.

Reaching conclusions on building block implementation technologies will be done during the AIPS/ALS architecture synthesis as part of the technology insertion optimization. The technology projection will identify the approximate, cost effective, capabilities which a computer design should have at the AIPS/ALS preliminary design review. Then the architecture synthesis will explore the implications of achieving these capabilities in AIPS/ALS and identify the implications for FTP, IOS,ICIS, and Network Node technology insertions.

AIPS architectural improvements will be considered during the architecture synthesis phase. Changes will be considered as required to make a cost effective implementation that uses the technologies recommended in the technology projection.

Figure 1 shows the purpose of the task reported here in the context of the overall AIPS for ALS design methodology.

This task generates a technology projection in order to predict what "state of the art" and "implementation refining" technologies will be available. The prediction is used to improve the candidate architectures in order to make the ultimate implementation more cost effective. The technology projection accomplishes its purpose by fulfilling the following subsidiary purposes : survey to establish what is available now and project to identify state of the art technology at the technology freeze date. The freeze date used for this study is the ALS preliminary design review in mid-1992. Where appropriate, technologies usable in an implementation refinement slightly later than 1992 will be considered.

The technology projections from this task will be used with the AIPS building block knowledgebase, architecture knowledgebase, AIPS/ALS avionics requirements, and performability analysis to guide the synthesis of candidate avionics architectures. The building block knowledgebase provides information about the existing AIPS building blocks. The architecture knowledgebase provides architectural constraints and fault tolerance theory. The AIPS/ALS avionics requirements are used to configure the building blocks specifically for ALS. The performability analysis is used to model the candidate architectures and compare the expected performance and reliability with the ALS requirements.

1.2. Approach

There are three general choices for technology insertion, as depicted in Figure 2, which are kept in mind during the technology projection and architecture synthesis in order to produce a more cost effective insertion. The three approaches for implementing

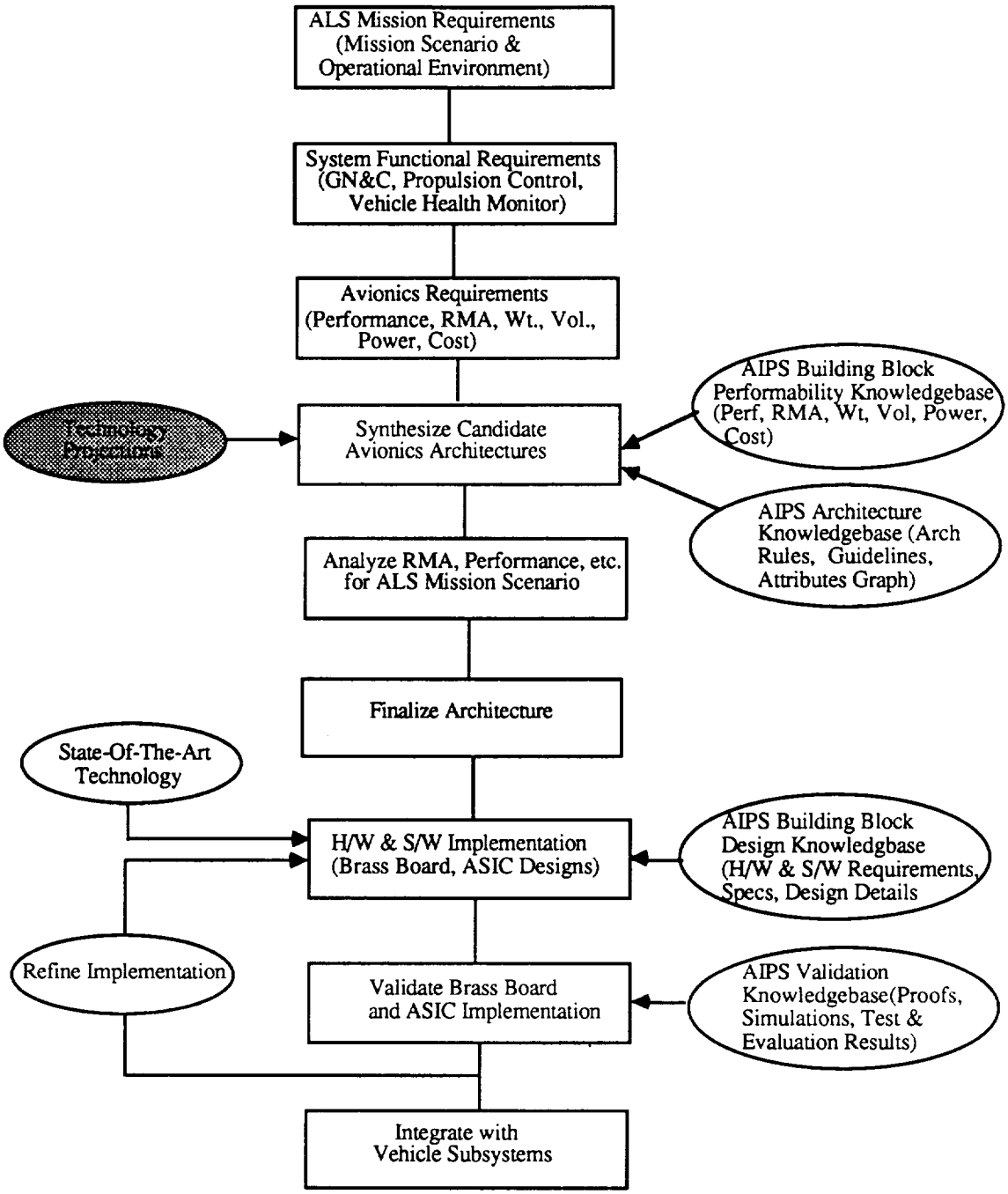

Figure 1. Technology Projection in Context of AIPS/ALS Design for Validation Methodology

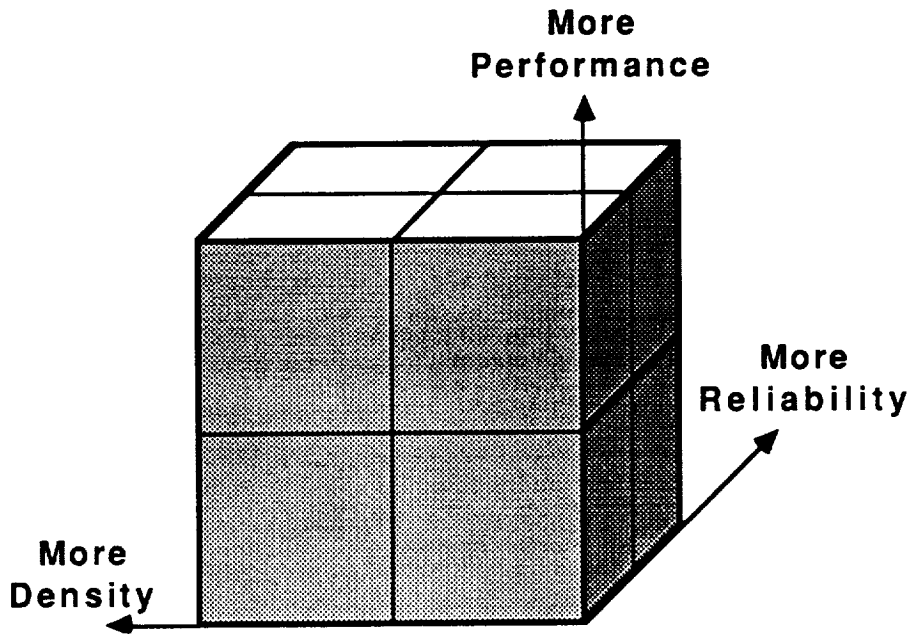

Figure 2. Different Insertion Options for Lowering Cost

cost effective systems are to: increase density, increase performance, and increase reliability. The recommended options are described in the architecture synthesis report.

The technology projection begins with the intuitive selection of five technology areas that are likely to be important for AIPS/ALS. The five areas are VLSI circuits, microprocessors, multi-chip module packaging, optical interconnections, and radiation hardening against transient effects. Each area is broken down more finely during the literature survey. After the technology survey, projections that enable architecture synthesis will be made.

In order to minimize the effects of bias and gain better survey coverage, an information space concept has been created to guide the technology survey. The space is displayed graphically in Figure 3. The concept has three dimensions: sources, technology areas, and time. The sources are government, industry, and academia. The technology areas are VLSI, microprocessors, multi-chip modules, optical interconnection, and radiation hardening against transient effects. The time periods are now and near the technology freeze date.

2.0 TECHNOLOGY SURVEY AND PROJECTIONS

The technology projection provides information on new technology capabilities which are relevant to AIPS/ALS. The technology projection is accomplished by sampling the information space and interpolating or extrapolating where necessary. Technology

survey can be categorized by sources, technology, and time period. The sources are industry, government, and academia. The technologies are very large scale integrated circuits (VLSI), microprocessors, multi-chip modules (MCM), optical interconnections, and radiation hardening against transient upsets. The time periods are now and the technology freeze date. The freeze date and the AIPS/ALS preliminary design review date are in 1992. The projections for each of the five technology areas are provided in the next five subsections. The detailed sources of the survey and the rationale and justification for projections are given in the appendix.

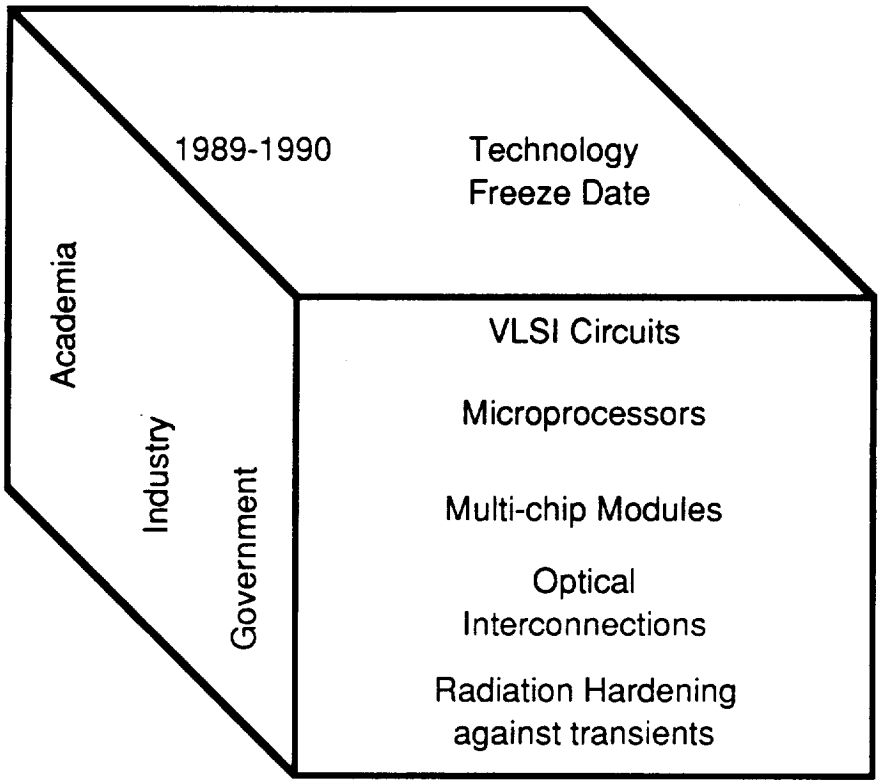

Figure 3. Literature Survey Information Space

2.1 VLSI Technology

VLSI technology contains much of the new capability that is relevant to the AIPS/ALS technology insertion. In 1992, there will be a greater variety of semiconductor device families. There are four logic technologies which are and will remain a force in the 1989-1993 marketplace as shown in Figure 4. These are Complementary Metal Oxide Semiconductor (CMOS) logic, Emitter Coupled Logic (ECL), Gallium Arsenide Enhancement / Depletion Mode Field Effect Transistor (E/D MESFET) logic, and Bipolar-CMOS (BiCMOS) logic. Other less mature families exist. One of these, Heterojunction Bipolar Transistors (HBT), may become a force in the 1992 market place.

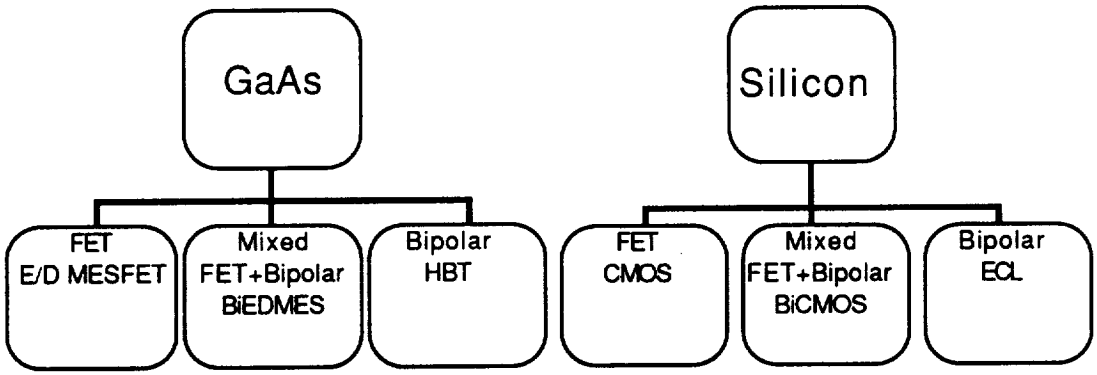

Figure 4. Relevant 1992 VLSI Circuit Logic Families

The development of these families will occur as part of three trends. The first trend is toward systems with higher clock rates. The second is toward systems with higher functional density. The third is toward achieving more cost effective systems through increased use of application specific integrated circuits (ASIC).

Higher clock rates are related to increased power dissipation. It is probable that AIPS/ALS will be cooled, in part, conductively. Therefore, technologies which pursue higher clock rates and lower power dissipation, together, are more likely to be useful in AIPS/ALS. Two technological strategies which do this have been identified. The first strategy is mixing device technologies on a single VLSI circuit. This tends to preserve each family's benefits while limiting their detriments. An example of this approach is the mixing of CMOS and Bipolar technologies to construct BiCMOS devices. The second strategy decreases device feature sizes while lowering VLSI supply voltages. This tends to decrease device RC time constants while decreasing device power dissipation. An additional reason to decrease supply voltages is to avoid electric field strengths which will destroy the finer feature devices. Numerous CMOS VLSI circuits have been implemented which have ~0.5 micron feature sizes and use 3.3 volt supplies.

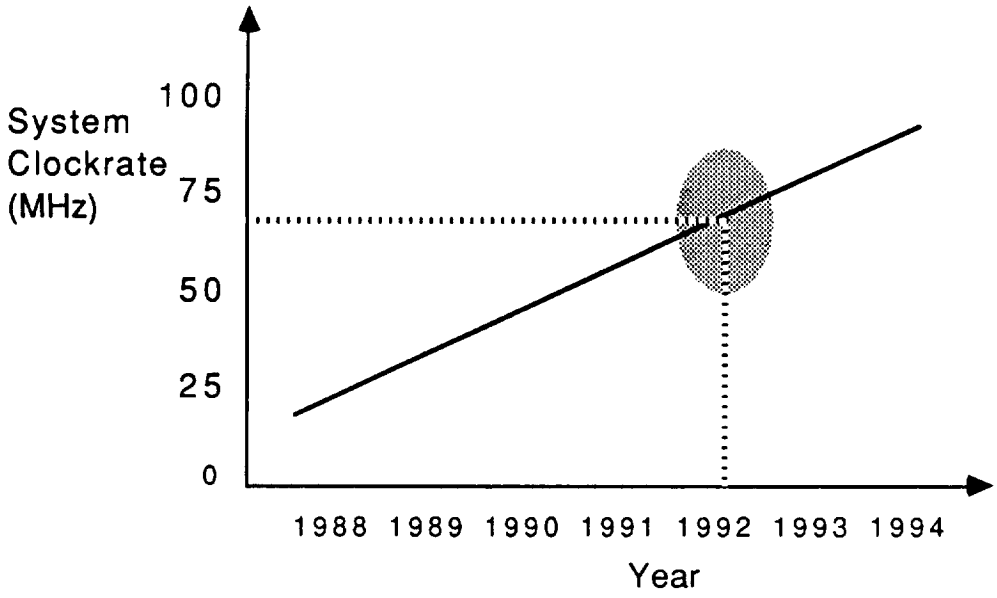

Figure 5. Projected System Clock Rate

Figure 5 shows the projected clock rate for the next several years. The projected clock rate for a cost effective AIPS system with a 1992 PDR is between 50 and 80 MegaHertz.

The second trend is toward higher functional density. One way to accomplish this is by achieving higher device density. This is done, primarily, by using devices with smaller feature sizes. Some of the factors associated with producing such devices are better clean rooms, finer line lithography equipment, better substrates, and lower supply voltages. The DoD VHSIC program has been completed. During its last phase, important research was performed in the area of high speed VLSI circuits having 0.5 micron feature sizes. This and other facts indicate that high speed VLSI with 0.3-0.5 micron feature sizes will be available in the 1992 market place.

The projected device density for custom designed VLSI is presented in Figure 6. This means a four times density increase is being produced by a device shrink from 1.0 micron to 0.5 micron feature sizes. This also means that a one megabit, 1990, maximum SRAM density implies a four megabit, 1992, maximum SRAM density. This is confirmed by SRAMs displayed at past ISSCC (International Solid State Circuits Conference).

The third trend is toward a system design environment which supports the cost effective design of systems that make extensive use of ASICs. The availability of tools for behavioral modeling, logic synthesis, interconnect modeling, and improved automatic routing will make such designs significantly more cost effective than in the recent past. Therefore, the AIPS/ALS technology insertion is likely to benefit from more intensive use of ASICs than previous AIPS systems.

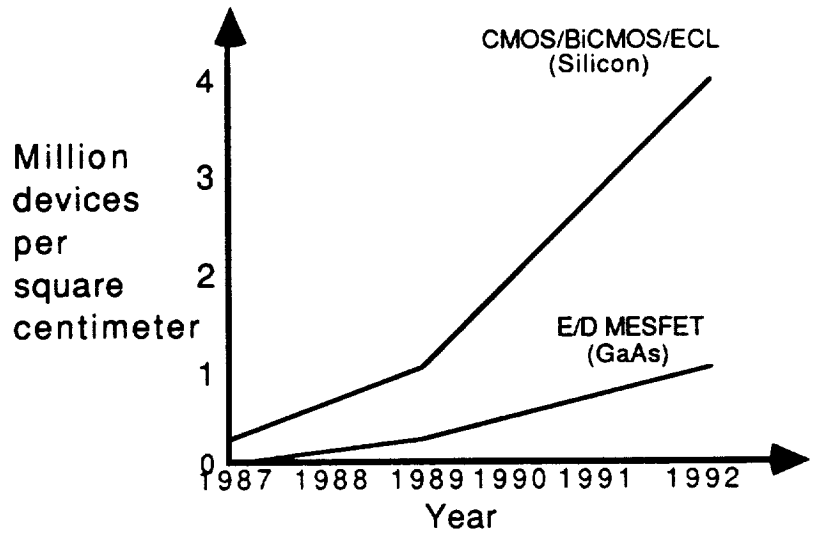

Figure 6. Device Densities for Relevant Device Technologies

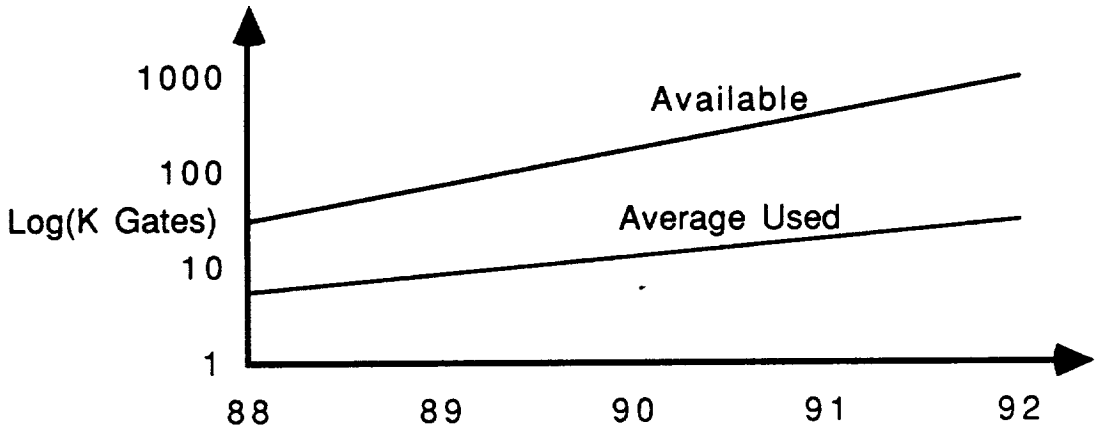

Figure 7. Cost Effective Custom and Semi-Custom Logic Density

Figure 7 highlights the distinction between the available logic density in ASIC products and the average used logic density in ASIC designs. The average used logic density is related to the most cost effective logic density for a given design environment capability. In the AIPS/ALS time frame, many will find 10-50K standard cell and gate array designs more cost effective than off-the-shelf MSI and LSI circuit approaches.

Now, the implications for an AIPS/ALS system design at a 1992 PDR are summarized by describing the system's processor, memory, and support VLSI in the light of the previous conclusions.

The AIPS/ALS will use a 50-80 MHz, 32-bit, RISC processor. This processor will use the higher device density to integrate integer, floating point, cache control, and 64 kbytes of fast memory onto a single chip. The processor VLSI circuit will use a 3.3 volt supply, ~0.5 micron minimum feature size, and either CMOS or mixed CMOS / Bipolar technology. This achieves high functional integration with around 5 Watts of dissipated power.

The off-processor memory hierarchy associated with the processor architecture will be assembled out of a small number of VLSI support chips and will provide 100-200 megabytes per second of low latency bandwidth designed for embedded computing. The on-processor cache will have under ten nanosecond access time. The one megabyte main SRAM memory will be composed of eight, less than 50 nanosecond, 3.3 volt, four megabit, CMOS/SOI SRAMs.

The support logic will include under 30K standard cell designs in CMOS, BiCMOS or GaAs. The GaAs will be used where its lower speed-power product can benefit.

2.2. Microprocessor Technology

A technology projection has been performed as part of the AIPS/ALS design process in order to identify the most cost effective technology insertion. As part of this, the performance characteristics of the most cost effective processor implementation at the time of the AIPS/ALS preliminary design review (PDR) have been projected. The full technology projection is presented in [Ref. 1] and the processor performance is discussed, briefly, below.

In order to project 1992 processor performance characteristics we consider a sample of current processors with respect to different performance benchmarks. Then we extrapolate the 1992 processor characteristics by considering vendor plans along with relevant advanced technology demonstrations.

First, we consider current processor performance with respect to the version 1.1 Dhrystone benchmark. The Dhrystone is a popular small integer benchmark. It does not use floating point, I/O, or operating system calls. Compiler optimization improve scores, significantly. The benchmark program fits into most instruction caches. In general, the Dhrystone is a useful measure of integer performance. The Dhrystone performance of various existing and future microprocessors is shown in Figure 8.

The first conclusion that we draw is that at the same clock rate, the CISC (Complex Instruction Set Computers) machines have less integer processing capability than RISC (Reduced Instruction Set Computer). For example, a MIPS R3000 @25MHz performs 5-10 times better than a Motorola 68020 @25MHz. The next conclusion we draw is that integer processing capability in 1992 will be 2-3 times greater than the R3000 (@25MHz)

capability. Two entries support this. First, the prototype processor reported at the 1990 ISSCC (i.e. International Solid State Circuits Conference) runs at twice the clock rate and has 2 times the score. Second, the R6000 runs at 3 times the clock rate and has 2.5 times the score. Verbal and written plans for 60-80 MHz processors for pre-1992 marketing have been voiced by many vendors . There is active competition between the SPARC, AMD 29000, Motorola 88000, and MIPS R3000 architectures which has resulted in versions of each in ever higher clock rates. Versions with 40 MHz clock rates will exist in 1990.

Dhrystone (Version 1.1) capability at ALS PDR is projected to be 50 to 80K Dhrystones per sec.

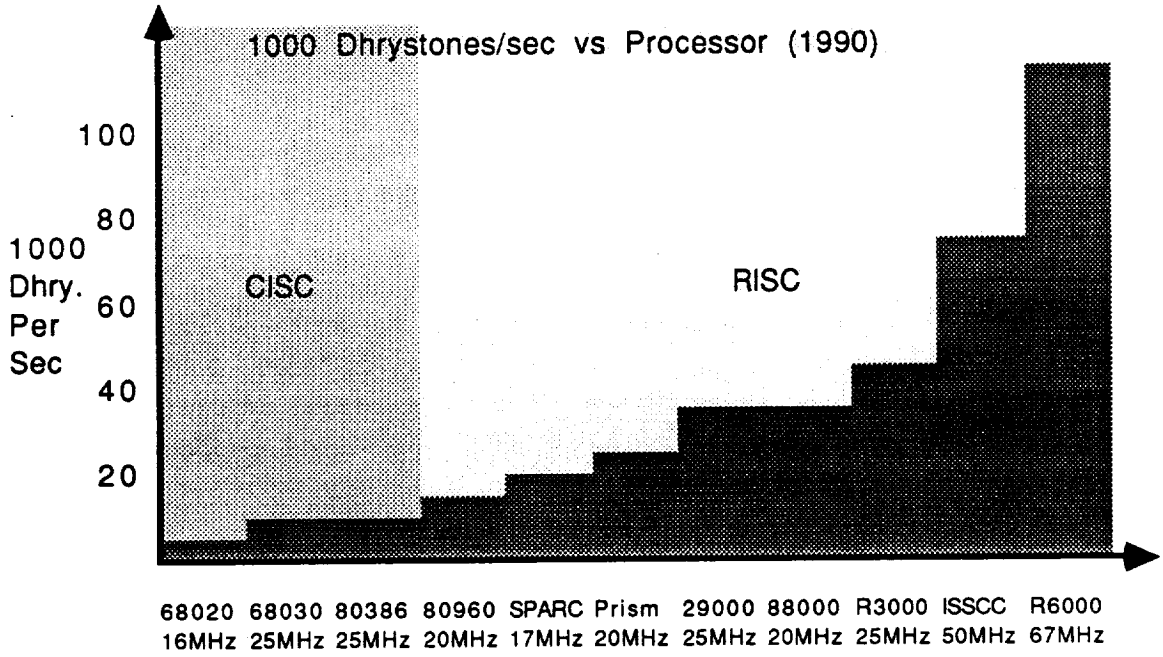

Figure 8. 1990 Dhrystone (Version 1.1) Processor Benchmarks

The Whetstone benchmark is a mix of floating point, integer, function call, array indexing, conditional jumps, and transcendental functions. Based on performance benchmark results reported in references 16-21 of Appendix A.2.2, one can conclude that compiler optimizations have little effect on the benchmark score. Whetstone memory access patterns allow performance improvement to be obtained by good cache design. The Whetstone performance of various existing and future microprocessors is shown in Figure 9.

The CISC machines have less Whetstone processing capability than the RISC machines. At the same clock rate, the 68020 has 6-15% of the RISC capability. The Whetstone capability at PDR is projected to be 15 to 25 Double Precision Mega-Whetstones per second.

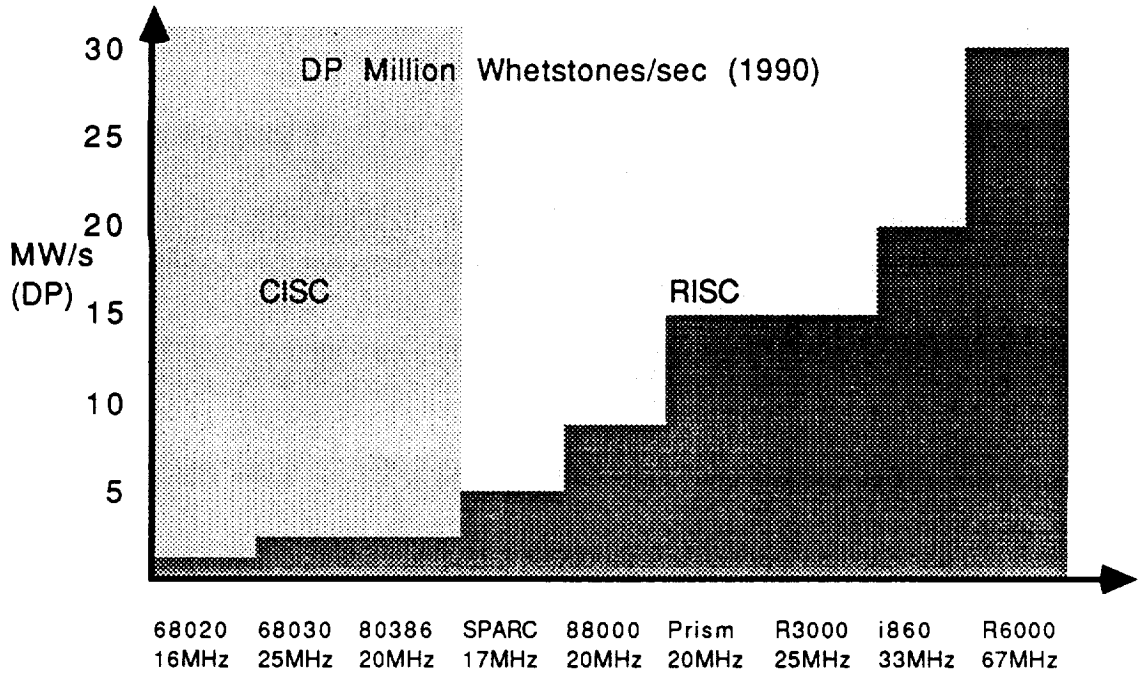

Figure 9. 1990 DP Whetstone Processor Benchmarks

In November 1988, the Systems Performance Evaluation Cooperative (SPEC) was organized in order to standardize benchmarking and increase available unbiased computer benchmarking information. The 1.0 SPEC benchmark suite is a CPU-intensive set of 10 benchmark programs. The benchmark measure for each program is performance relative to a Vax 11/780 (i.e. Vax/Sys performance). The SPEC ratio is a geometric mean of the individual benchmarks. The SPEC performance for selected existing and future microprocessors is shown in Figure 10.

At the same clock rate, different RISC architectures tend to perform about the same. The SPARC has a little less capability. The R3000 can be significantly improved with a custom floating point unit (FPU). The power dissipation of the ECL R6000 prevents its use in embedded systems but processors available by 1992 will achieve this clock rate and performance.

Now, briefly, we consider the individual benchmarks. Gcc is mainly a CPU integer-intensive benchmark. Espresso is a CPU bound integer intensive benchmark. Spice 2g6 is a CPU-bound, primarily, floating point benchmark using single precision, double precision, and complex operations. Doduc is a scalar floating point benchmark. NASKER (NASA Ames Kernel) is a double precision floating point intensive benchmark containing seven subsidiary programs. LI (LISP Interpreter) solves the 8 queens problem. Eqntott is an integer intensive benchmark that does sorting. Matrix300 and Tomcatv are vectorizable double precision floating point benchmarks. Fpppp is a double precision floating point benchmark.

By 1992, the SPEC ratio for the selected processor is projected to be 25 to 40 as indicated in Figure 11.

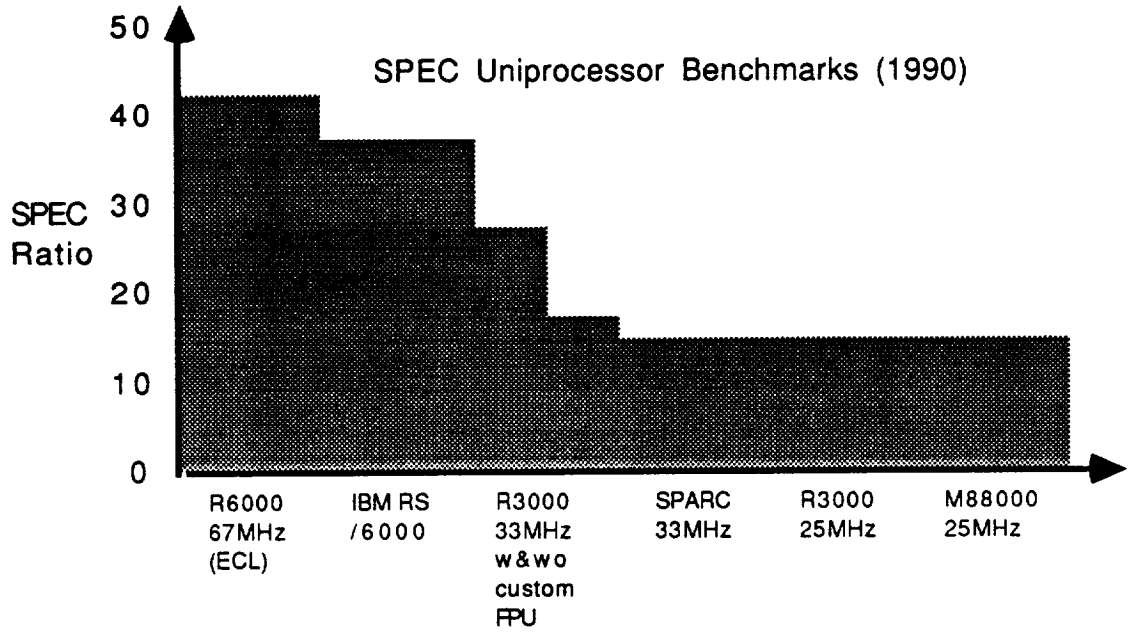

Figure 10. 1990 CPU-Intensive SPEC Ratio Mean Benchmarks

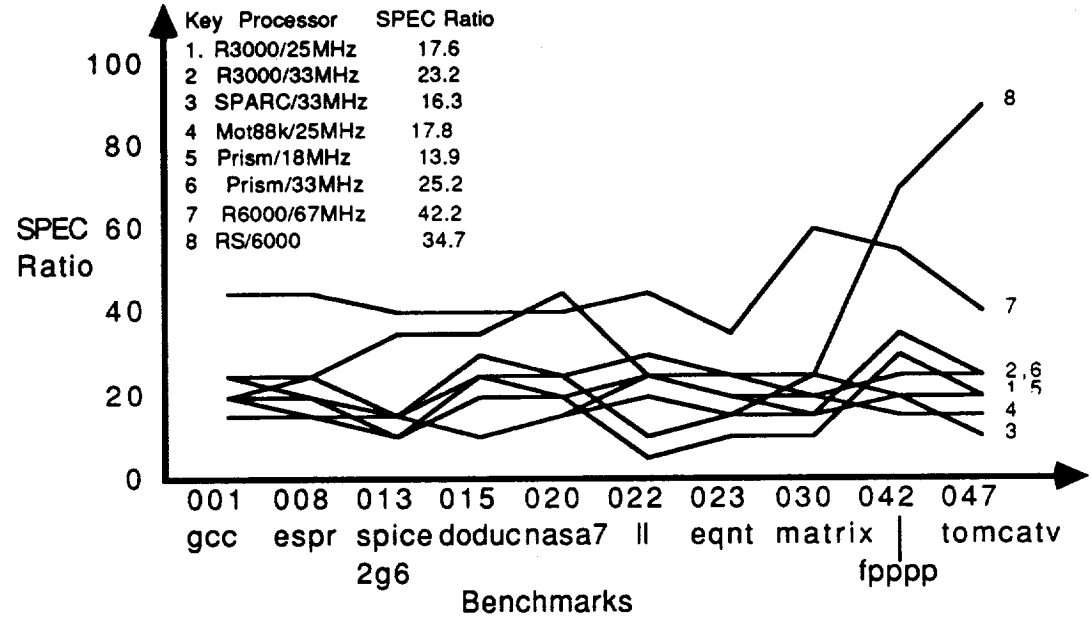

Figure 11. 1990 CPU-Intensive SPEC Ratio Benchmarks

Figure 12 graphs processor performance versus year. In the lower left, we see various CISC processors (1,2,3,4,5,6,7,8,19). The new 68040 and 80486 processors

(12,13) will have faster descendents (23). Slightly above the lower left is the current grouping of RISC processors (9,10,20,24,26,28). Higher performance versions have followed (11,29). More will follow (22,25,18,27). Militarized versions with similar performance will become available within a year and before the AIPS/ALS technology freeze date.

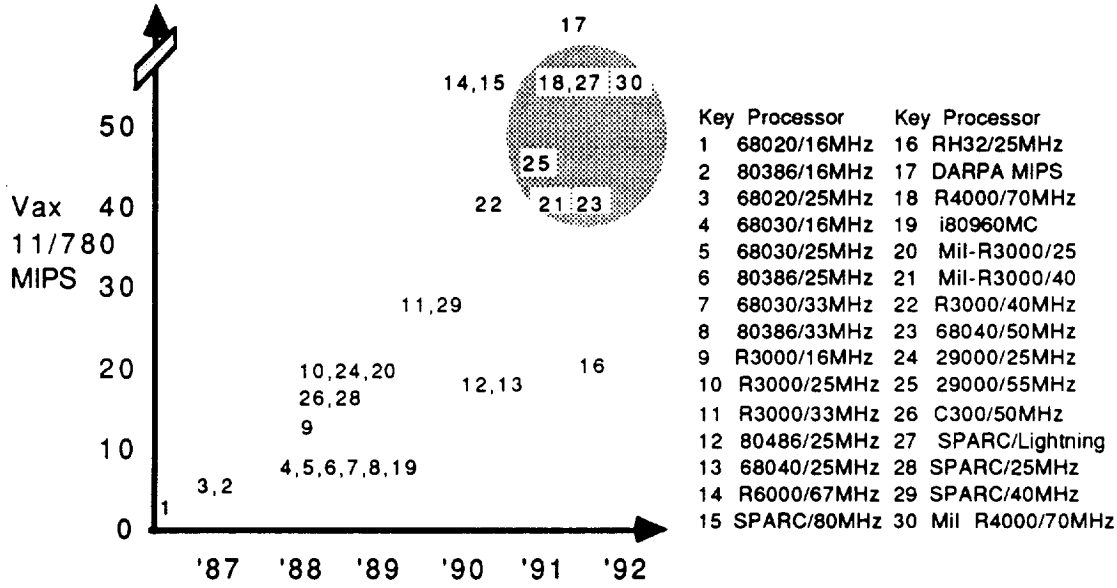

Figure 12. 1987-1992 Processor Performance Projection

The microprocessor performance projection conclusions are summarized in Table 1. These are the throughput ranges for various benchmarks and implementation technology of the processor for the AIPS/ALS technology insertion. The actual throughput will depend on the specific instruction mix of the ALS applications programs, the size of cache memory, the programming language and compiler, the selected clock rate (power dissipation requirements) and so on. These factors are taken into account in the AIPS Design and Validation Knowledgebase report [Ref. 2] and the AIPS ALS Architecture Synthesis report [Ref. 1].

Processor Performance	
Dhrystones/sec (Version 1.1)	50-80
DP M Whetstones/sec	15-25
Spec Ratio	25-40
Vax 11/780 MIPS	35-50
Processor Technology	
Clock Rate	40-80 MHz
Power Supply	3.3 Volt Power Supply
Semiconductor Process	CMOS/BiCMOS
Device Feature Size	0.5 micron

Table 1. Processor Performance and Technology Characteristics.

2.3. Multi-Chip Module Technology

The trend toward higher functional density and performance includes packaging technology. A great deal of research and development work has been and is being done to solve problems created by higher frequency VLSI circuits.

There are two primary problems which MCM packaging can mitigate. First, interconnection delay tends to dominate propagation delay. Therefore, in many cases, making faster devices will make little performance difference. Second, switching devices faster into the same capacitive load dissipates more power. The largest capacitive and resistive loads tend to be the longest interconnection runs.

The significance of interconnection delay relative to gate delay will tend to increase as clock frequency increases and device feature sizes decrease. Interconnections can be categorized as on-VLSI, off-VLSI and on-MCM, and off-MCM. The change in the percentage of interconnection delay with respect to changes in feature size is shown in Figure 13. For 0.5 micron device sizes, interconnect delay may approach 80% of total propagation delay. This on-VLSI interconnect delay ratio of four-to-one will be much better than off-VLSI ratios.

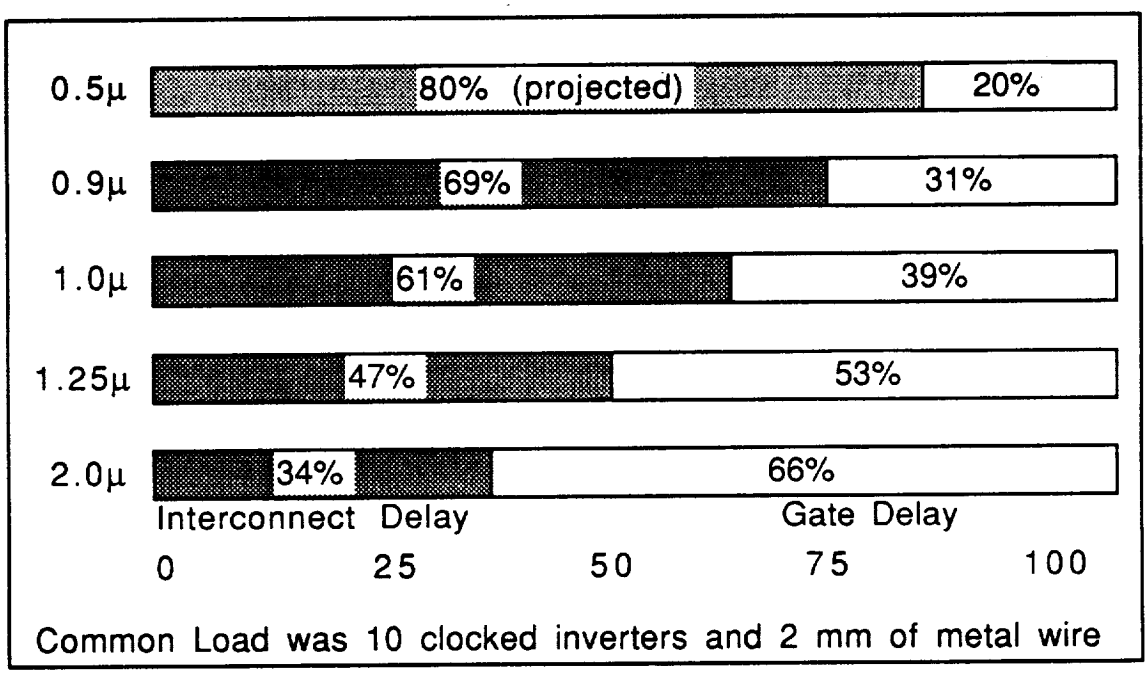

Figure 13. VLSI Circuit Delays As a Function of Feature Size for CMOS Process

Table 2, taken from the 1988 Future Advanced Control Technology Study on VHSIC/GaAs, further demonstrates the significance of interconnection delays. It displays propagation delays for three 1986 semiconductor technologies. The ratio of on-chip memory access to gate delay is between 3 and 20. The ratio of off-package to gate delay is

between 50 and 800. The table suggests that using MCMs can decrease propagation delay by 50 to 80 percent.

Characteristic	1μ E/D MESFET	2μ ECL	1.25μ CMOS
Gate Delay	50-150ps	150-250ps	500-750ps
On-chip memory access	0.5-2ns	2-3ns	10-20ns
Off-chip/on-package access	4-6ns	6-10ns	20-30ns
Off package access	10-40ns	20-60ns	40-80ns

Table 2. 1986 Delays in MESFET, ECL, and CMOS Systems

A 1989 data point, shown in Table 3, further emphasizes the significance of interconnect delays for high performance systems that do not use MCMs. A four inch wire run at 80 picosecond per millimeter in a 75 MHz clock rate system for Direct Coupled FET Logic (DCFL) has an interconnection delay that is over half of a clock cycle.

Logic	Macro	Gate(ps)	ps/mm of wire
DCFL	Inverter	140	80
	D Flip-Flop	500	80
	2:1 Mux	320	80

Table 3. Interconnect Delay For Direct Coupled FET Logic

The 1989 delay, without MCM technology, can be juxtaposed to a 1988 result with MCM technology. In the 1988 Government Microcircuits Conference papers, the Honeywell Sensors and Signal Processing Laboratory reports the MCM, thin film multilayer (TFML), interconnect characteristics as shown in Table 4. Specifically, the propagation delay for the TFML technology is about 10 times less than the wire trace on the printed circuit board example above.

Conductor Thickness	5um
Linewidth	25um
Line Pitch	75-125um
Dielectric Thickness	15-25um
Via Diameter	25-35um
Propagation Delay	62ps/cm
Characteristic Impedance	50 ohm
Resistance	1.26 ohm/cm
Capacitance	1.2pf/cm
Inductance	3.1nH/cm
Max. Backward Crosstalk	-40db

Table 4. Typical TFML Interconnect Characteristics

The second problem which MCM technology can mitigate is the tendency to increase power dissipation with faster switching speed. For example, CMOS power dissipation is proportional to load capacitance, switching frequency, and supply voltage squared. Most of the power is dissipated by devices driving external lines. The capacitance of these lines stays constant as the VLSI device feature sizes and capacitances shrink. In this case, higher switching speed means higher power dissipation. However, if the capacitances associated with the external lines can be decreased then the power dissipation might not increase with switching speed.

Table 4 shows 1.2 pf/cm capacitance and 1.26 ohm/cm resistance associated with the Honeywell, TFML interconnections. A separate estimate of 80% capacitance decrease per pin due to MCM packaging also indicates that higher switching speed with lower external capacitance and resistance can be achieved using MCM packaging. Thus power dissipation at higher switching frequencies can be decreased by using MCM.

Many MCM implementations have been reported. This evidence is used to support the above and to demonstrate that the benefits will be available, as well as be cost effective, by the technology freeze date.

2.4. Optical Interconnection Technology

Optical interconnections have performance, packaging, and electromagnetic properties which will allow decreased cost, increased safety, simpler designs, and increased data integrity.

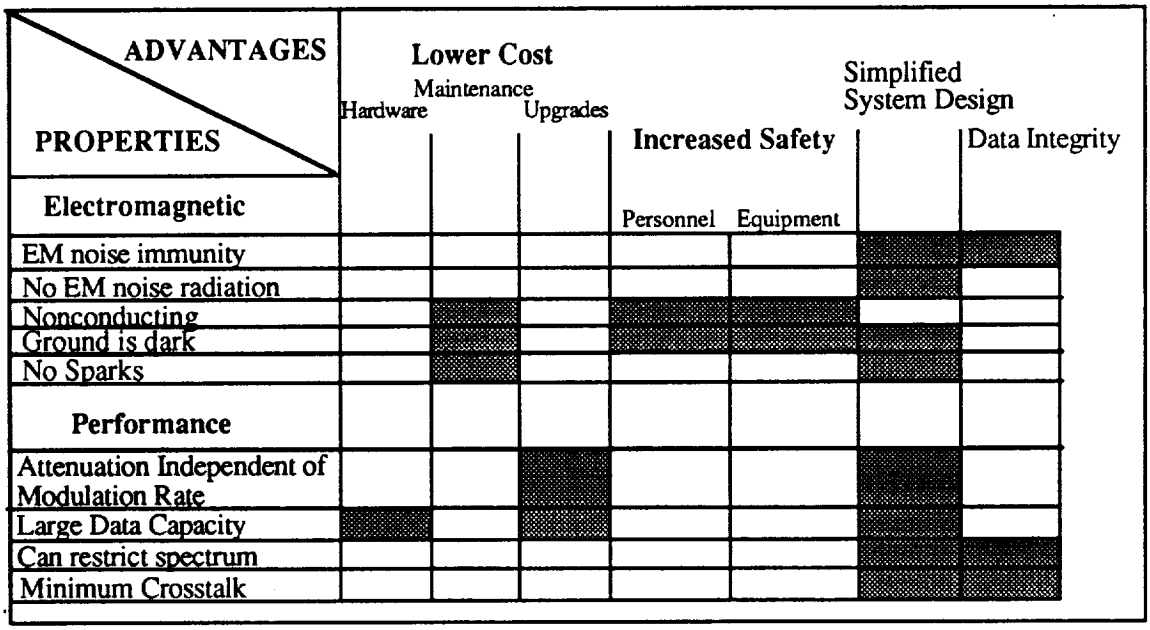

Figure 14. Why use optical interconnections?

Figure 14 shows the effect of various attributes of fiber optics on system design. A performance comparison of optical fiber and copper wire interconnections follows. There are four performance properties that tend to make optical fiber interconnections the preferred alternative. Signal attenuation is independent of modulation rate for an optical signal. This tends to make performance upgrades simpler. Also, it tends to imply that system and test equipment design is simpler. Optical fibers have very large data rate capacity. This tends to decrease total hardware cost, make system upgrades easier, and simplify system design. Since optical fibers can use a restricted portion of the frequency spectrum they are less noisy which tends to simplify system design and improve system reliability. Optical interconnections have less crosstalk than copper wires. This, also, simplifies system design and improves system reliability.

Optical interconnections are relatively immune to adverse effects of stray electromagnetic fields. So, the system design can be simpler, the bit error rates lower, and the reliability higher. That optical fibers do not generate electromagnetic fields simplifies system design, decreases power dissipation, and improves reliability. Finally, the fact that fibers are insulators and there are no "short circuits" creating sparks which makes maintenance easier, increases safety and again simplifies design.

AIPS/ALS has three possible uses for optical interconnections. These are the point to point links in the FTP data exchange mechanism, the intercomputer network, and the input/output networks. The most likely candidate for a high performance intercomputer network is, by far, the Fiber Data Distributed Interface (FDDI) or a similar high speed fiber optic interface. The availability of hardware using this standard in the AIPS/ALS time period is displayed in Figure 15.

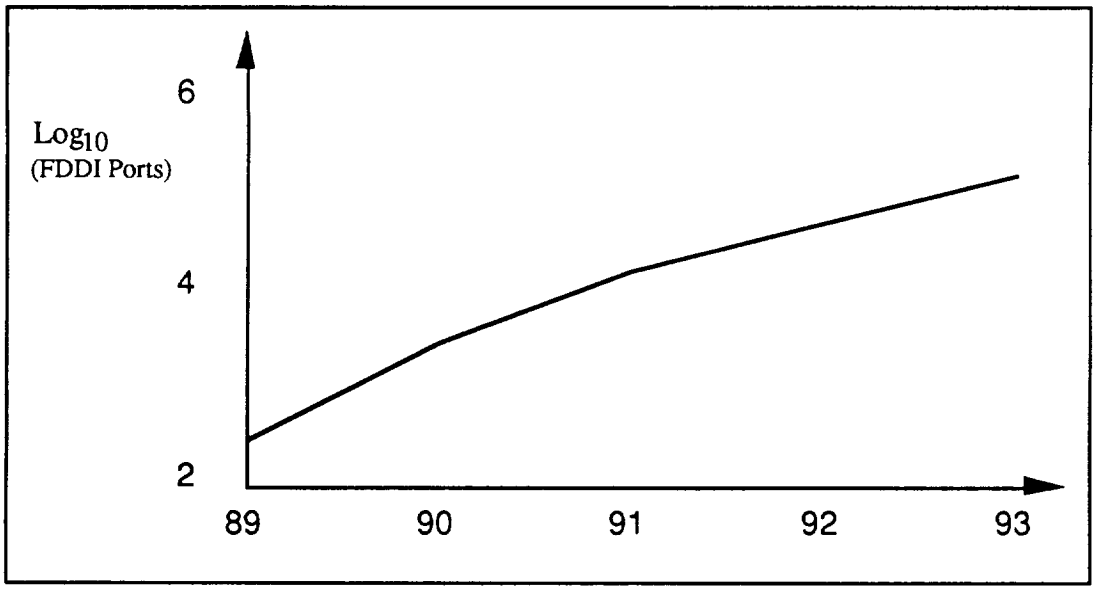

Figure 15. FDDI Projected Sales for 1989-1993 Period

The figure shows the projected sales in $\log_{10}$ (ports) units. The approximate sales quantities: 300, 3000, 22000, and 200000 units are associated with 1989, 1990, 1991, and 1993, respectively. This projection is supported by a great deal of evidence. FDDI chip set products have begun their second generation. The third will occur before 1992. The FDDI standard has been accepted by the computer and telecommunications industry. Many companies have FDDI products and projects already underway. Figure 16 shows the projections for the number of FDDI ports in personal computers for the 1989-1992 time period.

Activity by workstation and PC vendors in 1989 and 1990 tends to supports this.

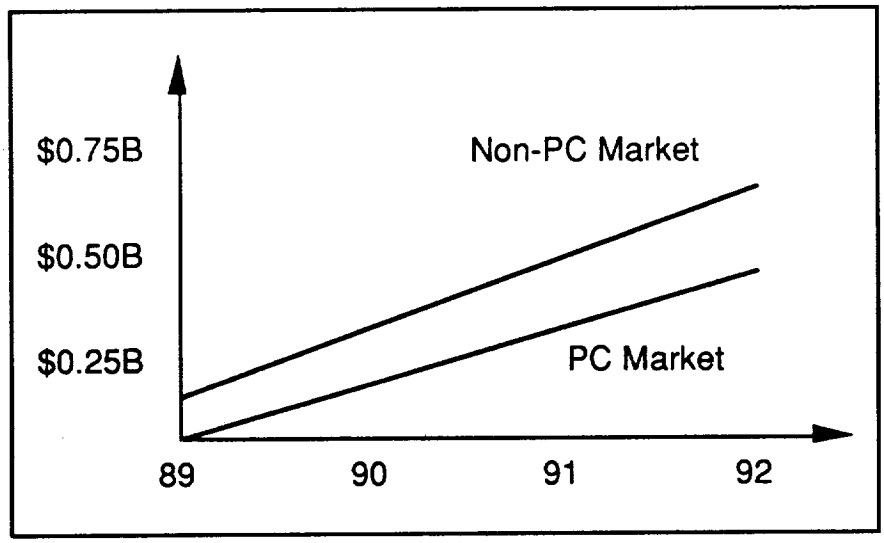

Figure 16. FDDI Sales in PC and Non-PC Product for 1989-1992

Underlying component evidence supporting the general large growth of fiber optics and FDDI in particular is the projection of GaAs optoelectronic integrated circuit sales shown in Figure 17. Not only do these support the 100 MB/S FDDI prediction but they imply that faster data rates will be available by 1992.

Several vendors are addressing optoelectronic functions which transmit and receive data at over 1 gigabit per second data rates. These include Gazelle Microcircuits, Gigabit Logic, and Vitesse semiconductor. A recent cooperative effort between Advance Micro Devices, maker of the first FDDI chip set, and Vitesse suggests an attempt to use Vitesse's gigabit per second transmission capability for the next generation FDDI. The Gazelle Microcircuits "hotrod" chipset is "FDDI compatible" and is expected to function at over a gigabit per second in 1990.

With respect to optical interconnections, AIPS/ALS can expect to have 100 megabit per second optical links and 100-1000 megabit per second point to point links in the FTP data exchange mechanism, IC network and I/O networks.

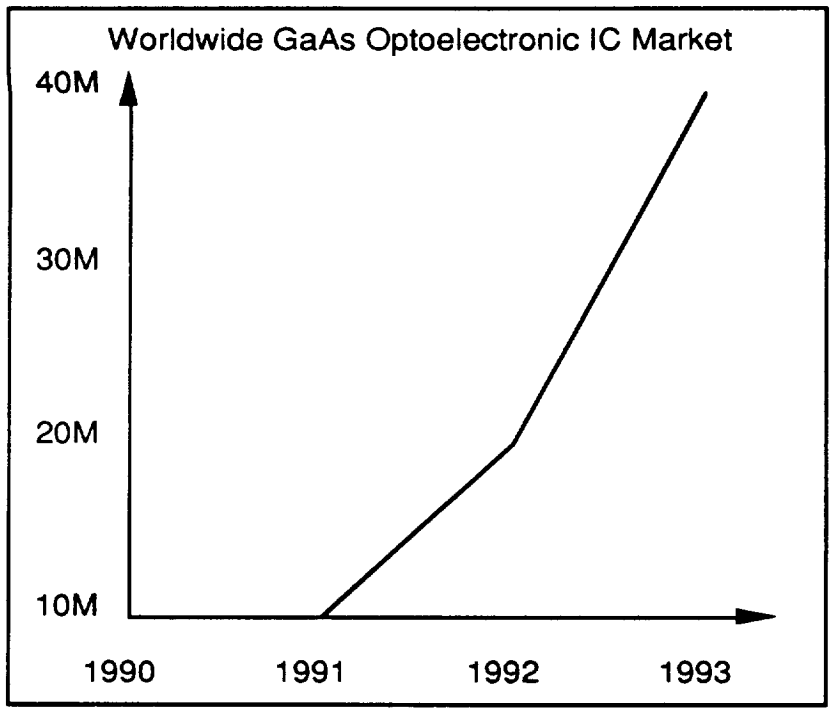

Figure 17. Projected GaAs Optoelectronic IC Sales for 1990-93

2.5. Radiation Hardened Electronics Technology

The AIPS/ALS system will enter a low earth orbit during its mission. The environmental conditions will include exposure to higher levels of radiation. The purpose of this section is to survey the radiation hardening technology which is relevant to AIPS/ALS.

The characteristics of the upper atmosphere are described in the 1987 Defense Nuclear Agency Study "Basic Mechanisms of Radiation Effects in Electronic Materials and Devices" (HDL-TR-2129). In general, the space environment consists of a low-level, constant flux of energetic charged particles including electrons, protons, alpha particles, and heavier ions. Characteristics of low earth orbit space radiation environment are listed in Table 5.

Ionization dose rate (< 1 rad/s)
Magnetospheric particles
Cosmic rays (Electrons, protons, alphas, heavier ions)

Table 5. Characteristics of Low Earth Orbit Space Radiation Environment

There are several interaction mechanisms listed in Table 6, relating radiation and a solid. These interactions result in either ionization which generates electron/hole pairs or damage due to atoms displaced from their normal lattice sites. Since displacement damage is caused by total dose, it is not relevant to AIPS/ALS. Ionization currents can be caused globally by radiation pulses or locally by energetic charged particles (i.e. single event upsets). These are the interaction mechanisms against which AIPS/ALS needs to be "hardened". It should be noted here that the AIPS architecture can tolerate transients caused by SEUs in the same manner that it can tolerate other transients. The problem is isolated to the affected fault containment region such as a processor channel or a node, the affected modules are configured out of the system and then reinstated on a trial basis by bringing their internal state in congruence with the other redundant members of the group. However, this takes a certain amount of time (from a few milliseconds to tens of milliseconds, depending on which module is affected) and if the radiation environment is severe enough, it can overwhelm the architecture's ability to recycle the affected hardware. Therefore, if an appropriate technology can be found that can reduce the transients caused by radiation without incurring greater cost or losing performance, then it would be of some value to AIPS/ALS.

Photoelectric Effect
Compton Scattering
Pair Production
Rutherford Scattering
Nuclear Interactions

Table 6. Radiation Interactions with Solid Material

Table 7 summarizes recent VLSI capability from the radiation tolerance viewpoint. The dose rate and single event upset resistance of AIPS/ALS will be achieved by having these qualities in the AIPS/ALS VLSI circuits and architecture. The approximate magnitude of the radiation threat to AIPS/ALS can be put in perspective by estimating the number of SEUs occurring during the ALS mission. For a five day mission, with VLSI circuits having SEU error rates of 10^{-7} errors per bit-day, and 4 megawords of 32 bit memory, one would expect approximately 64 errors. The technology that can withstand these errors is discussed below. For missions lasting just one or few orbits, the radiation hazard will obviously be much smaller.

10^{7}-10^{8} rad total dose
10^{10}-10^{11} rad transient upset
10^{-7} errors/bit-day for single event upset
10^{15} n/cm^{2} neutron displacement damage

Table 7. GaAs and Hard Silicon Radiation Characteristics (1987)

Research and development of VLSI which is less affected by radiation pulses is proceeding in several places. The foremost is SAT 081 which is an umbrella organization whose purpose is to coordinate radiation hardening research for the DoD. Another place is the DARPA which is studying these effects in GaAs VLSI. Finally, industry is pursuing radiation tolerant VLSI circuits.

Research and development for silicon based VLSI has focused on three processes: bulk silicon, silicon-on-saphire (SOS), and silicon-on-insulator (SOI).

The bulk silicon work has reached a state where the radiation dose rate is at SDI level 1, approximately, and cannot be improved, greatly. This is clearly adequate for 1.0 micron VLSI circuits. However, dose rate sensitivity will increase with decreasing feature size and 1992 VLSI circuit feature sizes will be near 0.5 microns. Nevertheless, the bulk silicon process may be useful and cost effective for AIPS/ALS.

The silicon-on-saphire work has potential and capability, however, it is relatively costly. Bulk silicon and silicon-on-insulator technologies seem more likely candidates for AIPS/ALS.

Silicon-on-insulator technology has the greatest potential for high density, dose rate resistant, submicron, VLSI circuits. This is because the SOI process allows greater isolation of devices from outside electric fields. The greater isolation is being used to increase device densities as well as increase dose rate resistance. The combination of these two guarantees this technology will develop rapidly. Specifically, with respect to higher device density, fabrication efforts for 16 megabit CMOS SRAMs which use SOI process steps are being made. Also, all monolithic, 3-dimensional, VLSI circuits use SOI techniques. Currently, 1 and 4 megabit, high dose rate resistant, CMOS/SOI, SRAMs are being pursued at Texas Instruments. Results generated for bulk silicon and SOS are being adapted to SOI.

Research and development for GaAs based VLSI is being targeted at developing better GaAs substrates. SOI gains its benefits from providing greater device insulation on the semiconducting silicon substrate. GaAs is a semi-insulating substrate which, therefore, already has the potential for very high device densities as well as very high dose rate resistance. However, current GaAs VLSI is less dense than Silicon due to technological immaturity with respect to low cost, large diameter, low defect density, GaAs substrates. Larger, lower cost, four inch wafers are now appearing.

In general, radiation pulse effects in GaAs VLSI circuits are comparable to those in the harder Silicon technologies. Bulk silicon, Silicon-on-Insulator and GaAs technologies will be useful and available to AIPS/ALS.

Single event upsets (SEU) are the newest, major radiation caused effects. The basic physical mechanisms and their implications for 0.5 micron VLSI circuits are still being refined. Nevertheless, SEU research was reported in IEEE Transactions on Nuclear Science, the Government Microcircuits Application Conference Proceedings, and NASA Technical Support Packages during the 1988-1989 period. Application notes explaining product SEU performance are more available now than before. Understanding this work allows better prediction of 1992 SEU resistant VLSI circuit characteristics.

Recent experimental research, partially sponsored by the Naval Research Laboratories (NRL), indicates a cooperative interaction between radiation pulse and energetic charged particle ionization mechanisms. This suggests that SEU rate estimates which are not performed in an enhanced dose rate environment will have underestimated the real system SEU rate.

More recent work reported in an October 1989 Fujitsu memory application note by M. S. Iqbal presents 1989 commercial memory technology SEU considerations. In general, SEU effects increase with higher device density and higher speeds. There are two techniques for adjusting memory cells in order to control these effects in MOS SRAMs. One increases power dissipation and the other decreases speed. A third technique for limiting SEU effects is to include error detection and correction circuitry on the memory chip. This tends to limit the access speed of the memories and does not correct multibit errors. The evaluation of 5 volt, 250 nanosecond access time, CMOS SRAM indicates FIT rates of 200-500. In 1992, smaller feature sizes and faster access speeds will tend to make these worse.

A January 1989 empirical study of single event upset susceptibility trends is available in a NASA/JPL Technical Support Package by that name. The main prediction is a ranking of existing logic families by SEU resistance as shown in Table 8.

CD4000 Series CMOS (Most Resistant)
Other CMOS Logic (LS,HC,HCT,SC)
Standard Power Bipolar (54XXX)
Other Bipolar Logic (Low Power, FAST, Schottky)
Low Power Schottky Bipolar (54LSXXX)
Advanced LS Bipolar (54ALSXXX) (Least Resistant)

Table 8. SEU Hardness Ranking by Logic Family

A theoretical SEU model has been developed in recent work done at NASA/JPL and the California Institute of Technology by Zoutendyk et al. The model can be used to design high density VLSI circuits with low SEU susceptibility. The measurement of the five model parameters is described and a sample SEU rate calculation is performed. In general, two mechanisms for SEU are identified. The first mechanism is a charged particle intersecting a charge collecting junction. This deposits charge into a device which may

change the device state. The second mechanism is a particle which misses a junction and generates charge which diffuses through the substrate. For high enough charge, device density, and circuit SEU sensitivity, multiple bit flips may result. The SEU trend associated with previously mentioned VLSI circuit trends is clearly toward more multiple bit flips.

SEU sensitivity is being addressed in three ways at once. First, the radiation pulse effects are being controlled by material research like SOI. This eliminates the increased SEU sensitivity due to the interaction effect. Second, since SEU sensitivity is largely determined by circuit geometry and electrical configuration, these configurations are being adjusted by VLSI vendors in the light of new knowledge. Two examples of this are the Harris radiation hardened, standard cell library and memory cell research reported as part of the DARPA GaAs program. Third, the increased occurrence of multiple bit flips is addressed by architectural features already in the AIPS advanced fault tolerant design.

In summary, the trend toward decreasing radiation resistance associated with VLSI circuit trends must be offset by technology insertion of improved materials, circuit design, and architecture. Better dose-rate and SEU modeling will allow improved VLSI circuit characterization so that the radiation hardness can be better verified.

3.0 CONCLUSIONS

This report has reviewed the options for the relevant technologies which will be inserted into the AIPS/ALS avionics suite. As such, it is integral to one step in the AIPS/ALS design for validation methodology, namely, the synthesis of candidate architectures. This section presents some remarks to summarize the data described in the body of the document.

The technologies which were reviewed are very large scale integration (VLSI) circuits, microprocessors, multi-chip modules (MCM), optical interconnections, and radiation hardened electronics. The scheduled date for the ALS preliminary design review, mid-1992, was used as a freeze date for technology projections, although options which may undergo refinement after that date were also considered. To achieve a balanced perspective, research trends in government agencies, academic institutions, and commercial organizations were all surveyed.

It is clear that advances in VLSI technology will continue to dominate the capabilities of avionic systems such as ALS. By 1992, the current four foundation semiconductor families (CMOS, ECL, GaAS E/D MESFET, and BiCMOS) will likely be joined by other maturing technologies. Higher clock rates, increased functional densities, and more frequent use of Application-Specific Integrated Circuits (ASICs) are the three primary trends which will drive the evolution of all VLSI circuits.

Since faster switching times generally result in increased power dissipation, high clock rates must be coupled with strategies to curtail this effect. These strategies are expected to include mixed-technology (e.g., BiCMOS and ECL) single dies, lower supply voltages, and reduced feature sizes. Increased functional density will also require reduced feature size devices. This will be realized through improved fabrication processes. ASIC insertion, on the other hand, will become cost effective for AIPS/ALS due to the rapid maturation of modelling and synthesis tools.

Based upon the technology projections, the VLSI devices which are anticipated for the AIPS/ALS will have 0.3-0.5 minimum feature sizes, have a supply source of ~3.3v, and operate at speeds in the 50-80 MHz range. The semiconductor family is likely to be CMOs or mixed CMOS/BiCMOS. Support logic will be packaged as ~30K equivalent gate arrays and standard cells.

The current state-of-the-art of microprocessors - the primary computing element of the AIPS architecture - was extrapolated to determine the architecture, features, and performance of devices likely to be inserted into the ALS configuration. Performance sampling of existing architectures showed that Reduced Instruction Set Computer (RISC) devices are clearly superior to conventional Complex Instruction Set Computer (CISC) devices for integer arithmetic and are marginally superior for floating-point calculations. Floating-point coprocessing units, however, can greatly improve RISC performance. Across the RISC class, various implementations perform equally well, making the selection of a particular design dependent upon other factors. Using clock rates as the sole factor for processing speed, the 50-80 MHz device which is anticipated is likely to be capable of 50-80K Dhrystones per second and 15-25M DP Whetstones per second. This corresponds to a 25-40 SPEC ratio and 35-50 VAX MIPS. Of course, performance in an embedded system is largely dependent upon a number of factors, including memory cache size, programming language and compiler, and exact instruction mix.

Since device interconnection delay can account for a large percentage of signal propagation delay and signal trace capacitive loading is the leading cause of device power dissipation, it would be judicious to address these problems with an appropriate packaging technology. Multi-chip module (MCM) appears to be one expedient approach. For example, thin film multi-layer connections have been shown to dramatically improve both signal propagation delay (one-tenth of wire trace pcb) and line capacitive loading (two-tenths of wire of wire trace pcb). Other favorable reports of emerging MCM implementations indicate that it can provide an effective packaging technology for AIPS/ALS microelectronics.

A corrolary issue to packaging is module interconnections. Optical interconnections, in the form of fiber links, offer properties which make them a favorable alternative to copper wire. These properties include high data capacity, low noise generation, signal attenuation independent of modulation rate, and relative immunity to EMI

corruption. These tend to simplify system design, decrease total cost, and improve reliability. The AIPS architecture, distributed and redundant in nature, can readily utilize such a communication medium. Vendor trends indicate that this will be a mature technology by the 1992 freeze date.

The AIPS/ALS microelectronics suite must be hardened to suitable immunity against the low earth orbit space radiation environment. This includes immunity to radiation dose rate and single event upsets (SEUs). Dose rate can be addressed with appropriately insulated device substrates. Silicon-on-insulator technology has the greatest potential for high density, dose rate resistant, submicron, VLSI circuits. GaAs, with its natural tendency to radiation immunity, offers another viable approach. Bulk silicon and silicon-on-saphire are other less attractive technology approaches. Experimental research on SUEs is still ongoing, with several solutions being examined, but it is important to recall that the AIPS architecture can tolerate transients such as SEUs just as it tolerates all other transient faults.

By reviewing the principal technologies which will be required by the AIPS/ALS configuration, credible projections of their state in the 1992 timeframe have been made. This information can now be merged with the AIPS Building Block Performability Knowledgebase and the AIPS Architecture Knowledgebase to properly synthesize candidate architectures for the avionics suite. This is one of the many rigorous steps in the design for validation methodology embraced by the AIPS/ALS program.

4.0 REFERENCES

1. Lala, J.H., et al "Advanced Information Processing System for Advanced Launch System Architecture Synthesis", NASA Contractor Report - 187554, September 1991.

2. Harper, R.H., L.S. Alger, and J.H. Lala, "Advanced Information Processing System Design and Validation Knowledgebase", NASA Contractor Report - 187544, September 1991.

APPENDIX A

TECHNOLOGY SURVEY SOURCES AND BIBLIOGRAPHY

The conclusions reached in the body of the report are derived by relating many data samples. These samples come from the five technology areas, different sources, some immature technologies, and some technologies which lead those that AIPS/ALS will use. In this way bias in the projections has been reduced.

In this appendix, we present the data samples upon which the report's conclusions rest. The sources are government publications, IEEE publications, trade magazines, conference proceedings, draft standards, and personal communications. The appendix is organized in five sections: one section for each technology area. Within each section, the first subsection has a very brief summary of the context and/or major conclusions of each reference. The second subsection lists the references for that technology area.

A.1.1 VLSI Discussion

1. Anadigics Inc. has signed up Thomson CSF as its exclusive second source in Europe for GaAs standard products and custom products that have data sheets available. Thomson will also act as a foundry in Europe for Anadigics.
2. Gate level design is on its way out as more designers of advanced systems use hardware description languages (HDLs) to define their designs and a combination of handwork and logic synthesis to convert those descriptions into implementations. Release 2.0 of SilcSyn from Silc Technologies takes design to a new level, by combining high-level design with architectural and gate-level synthesis.
3. Hampshire Instruments has made two agreements for technology to augment its X-ray lithography system: one with Lawrence Livermore and the other with Sandia. Hampshire started shipping X-ray steppers last month. The company received a $5.4M contract from DARPA to support commercial development of X-ray lithography.
4. Both Phillips Signetics and National Semiconductor will announce Furturebus interface chip sets within a few weeks.
5. Goaded by increasing hardware densities and shortened production schedules, engineers are fast abandoning gate-level design. A combination of hardware description language design and logic synthesis is preferred. HDL/Synthesis is going to get its biggest test and boost from users this year when Mentor Graphics ships its new release 8.0 which includes VHDL based design architect and the Quicksim II mixed level simulator.
6. Astec (BSR) Ltd., the number two producer of power supplies worldwide, is entering the merchant semiconductor business with power integreted circuits. Already in the marketplace are Unitrode, Motorola, Texas Instruments, Cherry Semiconductor and others.

7. The CAD Framework Initiative successfully completed a dry run last week of the multivendor design automation tool interchange it plans to showcase at next month's Design Automation Conference. The demonstration was significant because it embraced more tools and participants than expected. This encourages industry efforts to define and implement a common frame-work for exchanging data from different EDA tools across a multivendor environment. Some of the parties involved were Appollo, Sun, MCC, HP, Mentor Graphics, Genrad, and Computervision.
8. The report recommends that certain automatic test equipment requirements be placed on VHSIC based system modules. New and emerging technologies must not cause a proliferation of test methodologies and equipment.
9. The VHSIC phase 2 technology requires the following: feature size = 0.5 micron, functional throughput rate =10^{13} gate-Hz/cm^2, on chip clock rate = 100 MHz, failure rate 0.006%/1000 hours, and $5x10^4$ rads(Si).
10. The VHDL was initiated to establish a common DoD language with which all the elements of the system process may communicate. A VHDL technology insertion program is being pursued which involves institutions including GE, Gould, APL, RTI, Honeywell, LRS Research, Unisys, National Semiconductor, Stanford, USC, Dartmouth, and Rensselaer Polytechnique Institute. A list of companies developing design tools which directly support the VHDL includes Vantage Analysis, View Logic Systems, CAD Language Systems, Intermetrics, Endot, and VISTA Technologies. VHDL was adopted as IEEE Standard 1076 in 1987.
11. The study reports a new failure rate prediction model for VLSI devices. Also, revised failure rate prediction models have been developed for hybrid microcircuits.
12. The product guide contains information on IDT's R3000 and its support chips, CMOS SRAMs, BiCMOS ECL SRAMs, and other products.
13. The Zycad VHDL product information is a detailed example of 1990 VHDL Environment capabilities. A demonstration of the Zycad product was performed at Draper during late 1989. The VHDL product works with the Zycad gate level simulator and a logic synthesis tool.
14. Cypress Semiconductor has produced a product for the cost sensitive embedded systems market. It runs at 25 MHz and delivers 18 MIPS. A prototyping board is available from Flame Computer Corporation.
15. The presentation includes a discussion of high temperature electronics. The materials considered include silicon, and GaAs. GaAs has better high temperature performance and Silicon has greater technological maturity.
16. Integrated circuit power supply controllers which simplify the design and lower the parts count of switching power supplies are available. A list of supplying companies is included.
17. The main topics of the 1988 GOMAC were memory, radiation effects in electronics, signal processing, VHSIC technology, design automation, VHSIC applications, MIMIC, reliability, digital system applications, packaging, discontinued parts, systems, and testability.

18. The paper surveys trends in memory hierarchies. Changing levels of integration in semiconductors are changing the tradeoffs in CPU design and cache placement. Technology in 1988 did not allow large enough cache to be integrated onto processor chips. The authors project that within two years, on-chip caches will be in the range of 4-16 kbytes and will be standard for high performance microprocessors.
19. There are two fundamental obstacles delaying the insertion of high performance submicron CMOS into avionics and space applications. First, CMOS processes need to be developed which do not suffer from short channel effects. Second, systems must accomodate the 2.5-3.0V supplies which these devices require. The paper reports an example of how to overcome the obstacles.
20. The opportunities to minimize VLSI technology risks are discussed in the context of how they were handled on this program. The cost driver on the Copperhead program was to find a way to eliminate entire cards of components.
21. The difficulties with ECL gate arrays have been the extravagant liquid cooling systems required to manage the 20-30 watts of power dissipation per chip. The process dissipates 300 micro Watts per gate and has 300 picosecond average gate delays. Average chip power of the 12800 equivalent gate array ranges from 6-8 watts. The packing density is equivalent to 1.5 micron CMOS.
22. This tool provides a bridge between the system design environment and the ASIC design environment. The tool allows system designers to consider more design configurations prior to the development of ASIC designs.
23. The paper describes the architecture and design of a high performance all gallium arsenide 32-bit, single board computer. The architecture is the DARPA core MIPS and claims 100 Vax MIPS.
24. A new generation of tools is being developed to help designers manage increased design complexity brought about by higher density ASIC designs. Their goal is to dramatically decrease design time and ensure correctness and reliability by automating major portions of the implementation process including design for testability. The paper describes the benefits of these tools with example using a synthesis system from Silc Technologies, Inc.
25. The framework for effective VHSIC technology insertion has been supplied by the design of VHDL and its adoption as an IEEE standard. The implementation of the methodology which includes defining VHDL Data Item Descriptions, promoting abstract modeling in VHDL, requiring adequate simulatable VHDL descriptions in procurement contracts, and developing and disseminating library of VHDL component models are all in progress (1988).
26. This paper reports the use of VHDL to solve a system modelling problem. The authors are at Zycad Corporation.
27. In response to the increasing importance of VHDL to system designs, Honeywell developed a rapid design process which utilizes VHDL behavioral modeling and automated logic synthesis.
28. Methods of GaAs MESFET modelling are described.

29. The paper reports on the evaluation of the device electrical performance over temperature, electrostatic discharge (ESD) sensitivity tests, step stress testing, accelerated life testing, and identification of failure mechanisms. The work was conducted by RADC and Honeywell.
30. The paper describes the new Qualified Manufacturers Line concept which was developed at RADC. The QML route provides for an integrated manufacturing process from device design through final test which is predicated on the fact that quality and reliability can be designed into the product or that an ounce of prevention is worth a pound of cure. QML will significantly lower the cost of aquiring military and space qualified VLSI circuits that were associated with QPL.
31. Although VHSIC was created to advance semiconductor technologies and to expedite the introduction of advanced products and processes into new systems, it has brought with it the primary tool for resolving the problem of obsolescent components. By using VHDL system descriptions easier repartitioning, redesigning, and updating of implementations can be achieved.
32. The on-chip power distribution problem for highly scaled technologies is investigated. Metal migration and line resistance problems as well as ways to optimize multilayer metal technology for low resistance, low current density, and maximum wirability are also investigated. Fundamental lower limits and the limiting factors of the power line current density and the voltage drop are studied. Trade offs between interconnect wirability and power distribution space are examined. Power routing schemes are examined. For current MOS VLSI technology, one or two additional thick layers should solve most of the power distribution problems.
33. This is a Qualified Manufacturers Line (QML) draft standard. The foundation of the QML is to focus on the quality of the manufacturing environment instead of the quality of the product. The manufacturer acquires a manufacturing line or technology flow certification and qualification. Ongoing monitoring techniques maintain the QML status.
34. The primary new technologies for testing VLSI circuits involve scan path designs. It appears that because of their superior ability to simplify testing of sequential circuits, scan design methods should be the rule for complex chips. The recent IEEE/JTAG boundary scan standard and the appearance of standard cells which support boundary scan architectures indicate that more complex VLSI circuits can be designed to be testable.
35. The first issue of the "Triquint Quarterly" talks about GaAs standard cell design, packaging, design classes, and Class S wafers. In general it indicates that GaAs VLSI circuits are reaching the commercial market as well as the military market.
36. TI announced a product line of BiCMOS Bus Interface Functions. A claim is made that these devices may afford a 25% total system power savings when compared to a system using advanced bipolar devices for bus interface functions. Devices are available processed to the military temperature range as well as processed to MIL-STD-883C , Class B. TI is presently pursuing DESC SMD approval on all these functions.

37. The information provides parameters on Q24000 series ECL Bipolar product: Equivalent gates= 2160-30000, Average cell utilization= 95%, Maximum I/O frequency= 210 MHz, Internal gate delay(typical with 2 loads, 2mm of metal) is 0.5ns, typical power dissipation= 1.8-11.0W, and availability in the third quarter of 1990.
38. The Radstone VMEbus product information provide some data on 1989 militarized board and system level technology. The processors are 68020, 68030, 80286, and 80386 @ 16 megahertz. Their militarized VMEbus bandwidth is claimed to be a sustained 40 megabytes per second.
39. The National Semiconductor 256kx1 BiCMOS SRAM has the following features: 15ns or 18ns speed grades over the commercial temperature range, less than 1.1W power dissipation @ 50MHz, a soft error rate less than 100 FIT, over 2000V ESD protection, and uses the one micron BiCMOS III process technology. Militarized products are available.
40. The Mayo Graphical Integrated Computer Aided Design (MagiCAD) tool set was develop by the Mayo Clinic as part of the DARPA GaAs program to support MMIC and Digital GaAs VLSI circuit development. The Science Applications International Corporation (SAIC) is providing documentation and beta test site support under contract to NOSC. The tools focus on support for the development of systems based on GaAs. Tool set has been used on several of the GaAs Technology Insertion Program projects.
41. The Ga22v10 GaAs logic device is a TTL compatible GaAs pld. Its military version has a t_{pd}=12ns and a maximum frequency of 71 MHz. It propagation delay across the military range is essentially flat (a characteristic of GaAs devices which is not true of ECL or CMOS which slow down). Volume price is around $30. A second device, the Ga23SV8, is a 105 MHz TTL compatible state machine, militarized.
42. The National Semiconductor design automation tools support EDIF, VHDL, UNIX, and X-window standards.
43. The National Semiconductor confidential projection of their ASIC characteristics support AIPS/ALS predictions although there are noteworthy differences. Also, information on there current 0.8 micron technology gate array and standard cell product is here. Their M^2CMOS III technology has 0.8 micron feature sizes, runs at 150 MHz, has 252000 gates, and allows embedded ram.
44. Detailed information on National Semiconductor ASIC technology.
45. The paper compares various lithography technologies from the industrial point of view. Conventional optical lithography will remain the major candidate for half-micron technology. Beyond half micron, either excimer laser lithography, electron beam lithography or X-ray lithography will replace the conventional optical lithograpy.
46. The article describes the adaptation of RISC architecture implementations to support embedded applications. By removing nonessential hardware from the implementations, designers are creating a new selection of scalable chips that lower

cost without altering performance. Chips sets by LSI Logic and IDT are described for the SPARC and MIPS architectures, respectively.

47. Leading edge designs are based on submicron processes and have hundreds of thousands of gates. Improvements in CMOS and BiCMOS are making these the technologies of choice for 70-100 Mhz clock rate systems. The adoption of BiCMOS technology by silicon foundries may be the most important advancement in recent years. GaAs fabrication has recently moved from three to four inch wafers. Vitesse Semiconductor expects to produce GaAs products with 100K gates by the end of 1990 with more than 90% utilization. One source reports that at frequencies above 80MHz, the difference in power dissipation between CMOS and BIPOLAR is small. The 5 volt power standard will likely be lower to about 3 volts.
48. The 1990 Custom Integrated Circuits Conference (CICC) will emphase system level ASIC design. High level synthesis, partitioning, behavioral simulation, and timing driven layout. Analog and digital mixed signal tools and processes will be presented. A key theme is the implementation of a system by a chip set.
49. VLSI circuit processes and tools are now including capabilities for using a third interconnection layer on VLSI circuits.
50. The information discusses Zicad's VHDL product and their gate level hardware simulation accelerators (16k-4000k gate capacity). They call their design concept virtual prototyping.
51. In 1989, Cypress has RISC, PROM, PLD, Logic, and SRAM product families. The RISC family chip set has MP, CMU, MMU, Cache RAM, FPC, FPU, and FPP chips. The densest SRAM is 256kx1.
52. The SUSIE^{TM} logic simulator supports simulation of GigaBit Logic GaAs integrated circuits. The circuit models were developed as a joint venture between Aldec and GigaBit Logic.
53. The Xilinx XC4000 field programmable gate array product will be released in mid-1990. The technology will be sub-micron CMOS. Gate densities will be up to 20K gates. Performance will be improved by 50% over their XC3000 product. These can be used in systems with clock rates approaching 50 MHz.
54. Japanese semiconductor manufacturers are investing heavily in Sea-of-Gates architecture Gate Arrays with triple level metal. A Texas Instruments spokesman commented that the market for 50k products is taking off. This is being stimulated by the inclusion of embedded RAM with the logic gates.
55. The article contains a discussion of digital ICs, analog ICs, CAD, test and measurement, computers, communications, power, and packaging advancements. Cypress semiconductor produced the first cache controller and memory management unit to combine all of the intelligence and tag memories needed to implement the Sun Microsystem reference MMU architecture for its SPARC architecute. It runs at 33 MHz. Mixed mode VLSI circuits and VHDL CAD tools be came available in 1989.
56. This article focuses on Japanese X-ray laser work. Wavelengths between 2 and 5 nanometers have been generated. The work was done at the Tokyo based Institute of Physical and Chemical Research (RIKEN).

57. Any function that requires blocking voltages in excess of 50 volts and/or mandates current flows in excess of 2 amperes and/or dissipates more than 2 watts is a candidate for an intelligent or smart power solution. Intelligent power implies a tight coupling between the control/sensing portion of the system and the output power section. Intelligent power ASICs are a high growth VLSI circuit area. CAD tool development is lagging process development.
58. The AT&T FE050A, FE100A, and FE150A power module product provides 82% efficiency, parallel operation with load sharing, 0.5 inch profile, internal EMI filter, complete input/output filtering, input/output isolation, remote sensing, remote on/off, short circuit protection, and output overvoltage clamp at 6.6 volts. Two power architectures supported by this component are redundant and distributed architectures.
59. This is a particularly valuable source. It summarizes VHSIC and GaAs technologies through 1987 and includes a projection. The bibliography is extensive including 531 references. The performance of these technologies at high switching speeds in high temperature and high radiation environments is examined. The research activity in commercial, academic, and military environments is examined. Materials, processing, device, circuit, packaging, interconnect, electro-optical capability, computer architecutre, design tools, testing, manufacturability, and reliability results are discussed. A research roadmap is presented. In general, VHSIC and GaAs technologies will contribute to systems like AIPS/ALS in a significant way.
60. The article describes a scanned laser lithography system by Ateq company with 0.5 micron resolution. This meets Sematech's phase II performance requirements. Production deliveries of the system are scheduled for the fourth quarter of 1990.
61. The preliminary information describes the IDT 79R3000 CPU, 7RS301 development board, 79R3020 write buffer, 7RS101 CPU module, and 71586 Cache SRAM. The information includes power dissipation, speed, functionality, and more.
62. Spire Corporation has received awards from the Naval Weapons support Center for development of GaAs complementary heterojunction bipolar technology (HBT).
63. AT&T and Hampshire Instruments are collaborating in three areas of x-ray lithography development. These are x-ray optics, reticle technology, and x-ray resists.
64. Sandia National Laboratiories is transfering its injection seeding laser technology to Hampshire Instruments to improve the efficiency and throughput of the latter's X-ray lithography system.
65. This two volume set updates the survey of GaAs technology described in reference 59. For example, AT&T has a GaAs pilot line for their HFET device technology where their contract, approach, accomplishments, and contract plan for 1989-1990 are presented. Also, Booz Allen & Hamilton have done a systems analysis of the military payoff of the digital GaAs insertion projects. Insertion contractors include E-Systems, Martin Marietta, Texas Instruments, Grumman, McDonnell Douglas, Honeywell, Kor Electronics, ITT Avionics, and Sanders Associates.
66. Bipolar Integrated Technologies has unveiled its P201 ECL process. P201 can integrate 150k gates on an air cooled chip. P201's predecessor process produced

ECL SPARC and ECL MIPS architectures for 50-100 MHz clock rates. The new process produces more than twice the speed and density at the same power. Chips made with the process will be available in early 1991.

67. The paper describes the architecture and design of an all gallium arsenide (GaAs), 32 bit, single board computer. The computer is part of the DARPA GaAs Program and has a design goal of a 200 MHz clockrate.
68. Performance offers 3.3 volt center ground SRAMs, 1750A processors, and a MIPS R3000 processor with support chips. Performance has three CMOS processes having 0.8, 0.7, and 0.4 micron effective channel lengths.
69. The 1989 Motorola MECL Device Data book presents one example of the 1988-1989 state of the art in ECL components.
70. The 1989 GigaBit Logic GaAs IC Data Book and designer's guide presents performance, reliability, functionality, and packaging information on their high performance GaAs circuits. Their main product families are logic, memory, analog/instrumentation, communications, prototyping, and standard cell ASICs. They describe foundry services, testing methods, quality assurance, and thermal management for their ICs.
71. The Cypress 1989 data book provides information on 1988-1989 CMOS/BiCMOS state or the art information. They have SPARC processor and support chips. These are an integer unit, floating point unit, cache controller and memory management unit.
72. The Micron Technology data book presents 1988-1989 state of the art CMOS data. Advance information on a 1 megabit SRAM is presented.
73. The Xilinx Programmable Gate Array data book presents 1989 state of the art FPGA data.
74. Advanced ASICs require adequate tool support. Significant improvements in key design tools are becoming available. Products to be announced at the CICC will be ECL logic synthesis from Synopsis and a new Mentor Graphics Quicksim with delay modeling equations from ASIC vendors. Proprietary tool sets are giving way to cooperation with EDA vendors and many ASIC vendors are implementing frameworks that support both third party and proprietary tools.
75. The 1990 Design Automation Conference showed an increased interest in timing issues like interconnect delays.
76. Some of the next generation ASIC plans announced at the CICC included gate arrays with densities over 400k gates. Feature sizes are around 0.8 micron (drawn) or 0.6 micron (effective) and product arrival times are in 1991.
77. The McDonnell Douglas engineering group is pursuing processing within the RADC CMOS RH32 program and the DARPA GaAs program. The information discusses that work.
78. The capabilities of processing ASICS with a few hundred thousand gate densities places a heavy burden on the ASIC design environment. This design automation technology trend discussion includes architectural synthesis, logic synthesis, and VHDL mixed level simulation tools discussions.
79. This information discusses SilcSyn's architecture synthesis product.

80. The product information describes LSI Logic's ASICS, radiation hardened ASICS, and MIPS microprocessors ICs.
81. This product information describes Triquint Semiconductors GaAs Custom IC Foundry Products and Services.
82. The Vitesse GaAs VLSI circuit data book details their gate array, standard cell, telecommunication, memory, and microprocessor products. Additional packaging, application notes, quality assurance, and reliability information is provided.
83. The Texas Intruments BiCMOS Interface Logic data book discusses why these products can decrease system power by up to 25% over bipolar devices. The functions are pin for pin compatible with existing industry standard functions.
84. The Mentor Graphic design environment is described here.
85. The book presents a collection of IEEE articles on GaAs technology properties, devices and IC implementations, computer design concepts, system examples, and a microprocessor design example.
86. The article describes TI and IBM work in high density memories. IBM expects to produce 16Mbit DRAMs on 8 inch wafers in the third quarter of '91. Market research predicts 1million 16 Mbit DRAMs shipped by late 1991 and 20 million shipped in 1992. Note that 16Mbit DRAMs are similar to 4Mbit SRAMs in many relevant ways. So, this suggests that 4Mbit SRAMs will be available in 1992.
87. This facsimile describes a plan by Texas Instruments to make a GaAs MIPS microprocessor for the AIPS/ALS program. The chip currently operates at 150 MHz and has a floating point unit support chip. This is the group that is participating in the DARPA GaAs program.
88. The article discusses distributed power architectures and what advantages and technologies are making them more popular.
89. The article discusses the increasing competitiveness of BiCMOS technology with respect to CMOS and ECL. The advantages of BiCMOS over CMOS and ECL are discussed.
90. The article discusses how the high density and high drive of BiCMOS give the technology a competitive advantage for many applications.
91. Texas Instruments projects their standard cell library feature sizes through 1991.
92. Several articles present from different points of view why RISC architectures will have a competitive advantage over CISC architectures over the next few years.
93. This articles discusses ASIC costs. One graphic indicates that for designs with 10k-100k complexity standard cell designs are slightly less costly than gate array designs. Cost per gate (NRE amortized over quantity) for 10k-100k quantity is under 1 cent.
94. The buyers guide presents ASIC companies, products, and characteristics.
95. This article discusses the competition between high performance ASIC technologies.
96. This article discusses the different ASIC niches which ASIC technologies have created. Companies, services offered, and other product differentiating characteristics are described.

97. The article describes a memory density projection ending in a 64 Mbit DRAM in 1995. Evidence toward 8 inch wafers, 3.3 volt power supplies, and 0.5 micron 4 Mbit SRAMs by 1992 is presented.
98. The article presents the difference between process capability and design utilization from 1988 thru 1992.
99. The article discusses IBM's program in Xray lithography.
100. This article compares 1990-1991 SRAM memory processes for nine vendors.
101. The article summaries what will be discussed at the 1989 Wescon conference. Particular emphasis is placed on rapidly developing ECL technology for systems with clock rates over 50 MHz.
102-104 These articles report improvements in our understanding of single event upsets. They have corresponding technical support packages which discuss the information in greater depth.
105. BiCMOS is being used with ECL and with CMOS to develop ASIC processes which have a wide variety of characteristics.
106. The 1989 International Electron Devices Meeting is previewed in this article.
107. This month's update on federally supported photonics research available for transfer to the private sector includes a new process for growing low defect density GaAs crystals. The process was developed at the Lawrence Berkeley Laboratory.
108. The viewgraph presentation is a presentation of work done for the DARPA GaAs program as well as a projection of future TI GaAs goals.

A.1.2 VLSI Bibliography

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A.2.1 Microprocessor Discussion

1. Commercial developments must be more effectively leveraged by NASA. Four major recommendations are 1) Ensure adequate funding levels and stable funding profiles, 2) create a spacecraft computer technology applications activity, 3) facilitate insertion of new technology at all program stages, 4) clarify and consolidate required space qualification procedures. Computers with 2-3 years of development maturity will still have to be selected 4-5 years before flight even if the above recommendations are implemented.
2. The Radstone VMEbus product information provides some data on 1989 militarized board and system level technology. The processors are 68020, 68030, 80286, and 80386 @ 16 megahertz. Their militarized VMEbus bandwidth is claimed to be a sustained 40 megabytes per second.
3. This is a detailed presentation on the MIPS architecture.
4. This is LSI product information which shows the current level of integration for their MIPS architecture implementation.
5. The McDonnell Douglas view graph presentation is an expanded presentation of their DARPA GaAs Core MIPS microprocessor presentation.
6. The Texas Instrument view graph presentation is an expanded presentation of their DARPA GaAs Core MIPS microprocessor presentation.
7. The 1989 Performance Semiconductor data book contains information about their MIPS R3000 implementation.
8. This is the 1989 Cypress Semiconductor data book which contains information about their SPARC implementation.
9. Volume 1 of the DARPA Digital GaAs Review contains the GaAs 200 MHz Core MIPS Microprocessor projects. One is being pursued by Texas Instruments and the other is being pursued by McDonnell-Douglas.
10. This is a discussion of the state of research and development of memory hierarchies. Efficient memory hierarchies are particularly necessary in RISCs.
11. The paper discusses a radiation hardened R3000 implementation being pursued as part of the RADC RH32 program.
12. This paper is a GaAs microprocessor system. It indicates some of the effects of very high clock rates on RISC system design.
13. The paper discusses the design of a GaAs microprocessor system and indicates some of the effect that high clock rates have on such designs.
14. The paper discusses the Harris Semiconductor RTX2000 RISC controller for embedded real time applications.
15. The Texas Instruments presentation considers RISC vs CISC performance, processor selection consideration, manufacuting sources for processors, and then presents their own MIPS based architecture.

16-21 These are papers related to benchmarks and benchmarking.

22. This describes LSI Logic SPARC L64801 products.
23. This is information on the Systems Performance Evaluation Cooperative (SPEC).

24. These are the Release 1.0 SPEC Benchmark Suite results. Processors considered are Prism 18.2 MHz, R2000 12.5 MHz, R2000 16.7 MHz, MC68030 16.7 MHz, MC68030 33 MHz, PA-RISC 15 MHz, R3000 25 MHz, MC88100 20 MHz, and the CYC7C601 25MHz SPARC.
25. The three day seminar contains presentations by Sun Microsystems, Motorola, MIPS/IDT, Advanced Micro Devices, Intel, VLSI Technology, and Intergraph Corporation.
26. The AMD memory design handbook shows that the problems related to RISC processor memory hierarchies are well understood. Higher levels of integration and chips set RISC architectures are lowering the cost of RISC hierarchical memory design.
27. The article discusses the innovations presented at the 1990 International Solid State Circuits Conference. Integration levels were higher. Feature sizes were smaller. Bus structures were wider. In particular, A Very Long Instruction Word microprocessor by Phillip-Signetics demonstrated higher performance achieved through greater parallelism. Hewlett Packard showed a 90 MHz, 3.3 volt, CMOS implementation of its RISC Precision Architecture. IBM implemented its 370 architecture in a five chip set. Another trend is that microprocessors are being adapted to the system more than in the past. Solborne Computer and Matsushita Electric have codeveloped a SPARC implementation which uses a 0.8 micron process to integrate CPU, FPU, instruction cache, data cache, MMU and bus controller onto one chip.
28. This is a projection by John Hennessy of the future directions for RISC processors.
29. This is a program on "RISC : Recent Developments In Processor Design". There are three presentations titled "Microprocessor Development and Implementation", "RISC Architectures", and "Real RISC Machines". The following topics are considered: present state of development and implementation, forecast of the microprocessor market, basic approach and performance, a look at RISC architecture compiler principles, comparison of RISC vs. CISC, compiler technology need to achieve single cycle execution, an assessment of the RISC future, why RISC is the architecture of choice, a comparison of RISC chips, and an analysis of the current level of 10-30 MIPS RISC microprocessors.

30+31 These are presentations made at the 1989 and 1988 Government Computing Meeting. The meeting attempts to bring together all government agencies at one time to discuss all hardware and software under development or proposed development by the government.

32. The Chairman of Intel Corporation sent a letter to Colonel William Stackhouse (Chairman of Govt. Computing Meeting) regarding the leveraging of commercial microprocessor technology. Part of the letter is presented below.

"Since you serve both as Chairman of the Government Computing Meeting and as a key advisor to the Air Force in areas of high technology, I wanted to extend an offer to you.

Intel Corporation, a leader in semiconductor development for the last twenty years, is well known for being in the forefront of computer technology since the original development of the DRAM chip and, more recently, the 386 family.

In keeping with the state-of-the-art, Intel recently developed the 80960 chip, which is a 32-bit architecture, incorporating fault tolerance and floating point capabilities targeted for the avionics market place. Since Intel already produced this chip and has it available for the market, we are proud of its capabilities and are willing to offer to the United States Government the 80960 instruction set architecture (ISA) to become the 32-bit ISA standard.

We are willing to provide the 80960 ISA data to the Government with limited rights for the purpose of developing a military standard based upon our ISA. In addition, we would assist you in understanding this ISA, and we understand the importance of a smooth technology insertion.

In offering this ISA to the Government, we are further willing for the Government to use this ISA for any Government end use. Intel would still maintain the commercial end use market and would be willing to provide a royalty free license for the ISA to any contractor for Government end use.

In total, we believe this offers the Government a state of the art solution for the next generation 32-bit ISA standard, and at the same time promotes Intel's name and recognition in the commercial market."

33. The CEO and Chairman of MIPS Computer Systems sent a letter to Colonel William Stackhouse regarding the leveraging of commercial microprocessor technology. Part of the letter is presented below.

"MIPS Computer Systems is a leading supplier of RISC technology to the commercial market. We believe it would be beneficial for the United States Government to take advantage of the significant gains constantly being made in computer performance through RISC technology by incorporating it in a variety of military programs. To that end, we have committed to work closely with several committees that have efforts to choose a 32-bit Instruction Set Architecture (ISA) standard.

Now, we would like to extend our commitment to you in your role as Chairman of the Government Computing Meeting and your role regarding high leverage technology within the Air Force. For background, we wish to reference the offers MIPS Computer Systems has made to the Joint Integrated Avionics Working Group (letter dated 18 August, 1988 from Robert C. Miller to Captain Strauss, Wright Paqtterson AFB) and to the SAE (letter dated 14 October 1988 from Jacob F. Vigil to Mr. Gerard Tyra, Chairman SAE AS-

5 32-Bit ISA Committee). Specifically, we propose to offer to the government through your offices similar rights to that which has been offered within the SAE as follows:

MIPS Computer Systems is pleased to offer the MIPS R2000/R3000 ISA for consideration as the 32-bit ISA standard. If this ISA is chosen as the base line ISA, then MIPS will give the United States Government the right to develop a MIL-STD-XXXX ISA which is based on the MIPS R2000/R3000 ISA. The United States Government will have exclusive data rights to the MIL-STD-XXXX ISA and any corporation will have the right to build products executing the MIL-STD-XXXX ISA and distribute such products for use by the United States Government and its agencies or contractors and their subcontractors for purposes which are vital to the national defense and security, which will advance the national interests in space or in connection with Foreign Military Sales Agreements. Such rights will be gtranted by MIPS to the United States Government by a royalty free license at the time the MIPS R2000/R3000 ISA is sanctioned as the base line ISA for development of the 32 bit ISA standard designated as MIL-STD-XXXX ISA by the United States Government.

We believe that adoption of the MIPS RISC architecture would provide the United States Government and its agencies with access to a key technology necessary to achieving a competitive edge. MIPS is anxious to cooperate fully to aid in the evaluation and incorporation of a standard based on the MIPS RISC technology. Please let us know how we may be of further help."

34. Electronic Trend Publications published "RISC Impact on the Computer Industry". Architectural changes will increase performance over 60 MIPs in the AIPS/ALS time period. Technology changes to ECL and GaAs will significantly increase clock rates and performance.
35. These are three application notes describing details about working with the Clipper architecture.
36. This discusses some of Digital Equipment Corporation's new RISC products. They combine the R3000 and the Intel 80860.
37. AT&T and Pyramid technologies are producing a multiprocessing product based on the MIPS architecture.
38. This is a discussion of the importance of clock frequency in RISC performance.
39. A SPARC product claiming 80 MIPs and called the Lightning chip will be developed by Hyundai Electronics, LSI Logic, and Metaflow Technologies. Also, LSI Logic is releasing a "SPARC kit" family with the claim that it is the first complete SPARC chip set.
40. This describes the R3000 Processor interface.
41. Pyramid Technology and AT&T have agreed to produce a MIPS Architecture based RISC product.
42. Sun has reached an agreement with a new GaAs vendor and received the first of its own GaAs SPARC chips from GigaBit Logic. SPEC corporation will develop a three

chip version of SPARC on a NASA contract issued under the SBIR program. The 200 MHz implementation will feature separate integer unit, floating point unit, and interprocessor communication unit.

43. This article discusses problems encountered in RISC based designs. Efficient memory design is the key to fixing most of them.
44. This is the announcement of the ECL MIPS R6000 processor.
45. Intergraph partners with Samsumg Semiconductor to produce the Clipper Architecture.
46. A 33MHz implementation of the SPARC architecture by Cypress Semiconductor/Ross Technologies was announced.
47. The article reports on the 2nd Annual Microprocessor Forum. Solbourne computer has produced a 64 bit SPARC architecture.
48. IDT has optimized its MIPS architecture for embedded systems. Its called the 79R3001.
49. The article describes HP and Sun RISC chips.
50. This reports on a 1990 state of the art floating point math chip. The chips were built by BIT using their P111 ECL process.

51+52 These are examples of existing real time software for the MIPS architecture.

53. The article describes competition within the RISC processor and product market. It evaluates SPARC, MIPS, and the 88000 as the strongest market competitors. Also, the article warns that there are too many RISC architectures for all of them to survive.
54. The article discusses the 80960CA implementation and claims that the CA has 30 Vax MIPS performance. Whether the CA meets the criteria of low cost, low chip counts, and low power consumption is not clear. The clock rate is 33 MHz.
55. The facsimile from Jan Wine discusses the cost advantages of GaAs, GaAs processor demonstrations, GaAs processor Ada software, and benchmarking. Estimates of 20 DAIS MIPS for the McDonnell Douglas RH32 processor being done for RADC and >60 DAIS MIPS for the 200 MHz DARPA GaAs Core MIPS architecture. Information is also provided on the cache approach taken for the GaAs machine.
56. The articles discusses SPEC's purposes and membership. SPEC is a non-profit organization founded to develop a common set of performance benchmarks.
57. The newsletter indicates that Systems and Processes Engineering Corporation will develop a gallium arsenide SPARC microprocessor and compatible coprocessors. Initial samples will be available in late 1990.
58. The R3000 memory bandwidth is 160 Megabytes per second at 20 MHz. The 80960 memory bandwidth is 53.3 Megabytes per second at 20 MHz. The memory bandwidth ratio is 3. The R3000 has 18 MIPs at 20 MHz. The 80960kb has 7.5 MIPS at 20 MHz. The performance ratio is 2.5. The 80960CA has a faster processor but the memory bandwidth is still around 50-60 Megabytes per second. This is likely to limit the performance that can be obtained from the CA.

59-61. These describe the Acorn RISC architecture.

62. The product information describes the 80960mc implementation. It has 6 MIPS sustained performance.

63. The product information describes the 80960kb implementation. It has 7.5 MIPS sustained performance.
64. The paper discusses the 80960 architecture.
65. This describes the Clipper microprocesssor in detail.
66. This describes the Clipper architecture in detail.
67. The Intergraph comparison shows the chip integration levels of the Sun SPARC, AMD 29000, and MIPs architectures during 1987, 1988, and 1986, respectively, were lower than Clipper and Motorola. Higher levels of integration in the form of chip sets are now available for all these architectures. Also shown is a code density evaluation which describes Intergraph's Clipper and Motorola's 88000 as Ultra-high, MIPS as high, and SPARC and AMD as low.
68. The IDT product information gives details on its R3000 related chip set. Versions run at 16.7 MHz, 25 MHz, and 33 MHz.
69. The article shows that optimization of existing RISC architectures for embedded environments is both possible and under way. There is a trend to make the RISC functions available as macro cells for use in very high density (i.e. a few hundred K gates) ASICs.
70. This details IDT's support for the MIPS R3000 architecture. IDT offers R3000, R3010, R3020 CPU, FPU, and write buffer VLSI circuits.
71. This is a specification involving the 80960 P12 processors.
72. A collection of articles discussing RISC architectures. The MIPS, Clipper, SPARC, AM29000, Motorola 88000, HP Performance, Intel 80860, VLSI Technology Acorn, Intel 80960, and the Inmos Transputer are discussed. A discussion of the SPECmark benchmarks is presented. A discussion of the importance of high performance memory systems is presented.
73. The article describes, briefly, the 68040.
74. The article describes, briefly, the 68040 and includes a block diagram.
75. The article describes, briefly, the 68040.
76. The article discusses the applicability of RISC architectures to real time systems. Evidence that context switching on RISC architectures can be faster than on CISC architectures is presented. LSI Logic plans to make both their SPARC and MIPS processors available as standard macrocells within their ASIC libraries. The processor may be broken up into its constituent functions (i.e. CPU, FPU, MMU,...).
77. The directory of RISC processors contains 18 companies. The range of clock frequencies is from 12 MHz to 80 MHz. The power dissipations range from under 1 Watt to 21 Watts. Other characteristics which are presented are interrupt latency, on-chip cache, on-chip mmu, on-chip FPU, package availability, and development support.
78. This is a discussion of choosing the right RISC architecture for embedded computing applications by one of the manufacturers of the MIPS architecture. Much of the discussion is about caching.
79. The article discusses hardware and software tradeoffs in RISC architectures.

80. This is a discussion of ECL and CMOS RISC implementations. Current generation ECL processors dissipate too much power for AIPS/ALS. Also, their memory hierarchies are more complicated indicating a slight immaturity in the technology. The R6000 dissipates about 9 times the power of the R3000 and has about 3 times the performance. It requires 7 ns cache access times as opposed to 20 ns access times for the R3000. The above is 1989-1990 technology. By 1992, 50-100 MHz processors which are usable in AIPS/ALS are likely.
81. The MIPS RC6280 is based on the ECL R6000 implementation. The implementation was made by Bipolar Integrated Technologies using their P111 process. The applicability of the next generation process (i.e. P201) or of a CMOS architecture of equivalent clock rate (i.e. HP 90 MHz CMOS Precision Architecture) makes this information relevant.
82. An independent assessment of the Intel 80960KB and the R3000 architectures was performed by the Atlantic Research Corporation. The complete set of Common Avionics Processor 32-bit Ada benchmark programs was hand coded into the assembly languages of the two machines. Additional results have been obtained for Ada compiled benchmarks for both machines. Hand compilation rules were provided by WRDC and ARC. The CAP-32 Ada benchmark suite is available on the Joint Integrated Avionics Working Group (JIAWG) Bulletin Board System (BBS). The R3000 architecture performance is about 2-3 times better. The R3000 Ada compiler is better.
83. The article compares the R3000 to other RISC architectures. SPARC has a systems viewpoint, much applications software, good C and Fortran compilers. SPARC has lower performance at a given clock rate than others, no support for unaligned data, and lower VLSI integration at this time. Motorola 88000 has a customer base, reasonable chip architecture, and systems expertise. However, the available software is worse, the on-chip floating point function has slower scalar performance, and double precision performance is poor. AMD 29000 has a controller market share. But, little software integration, no native tools, lack of byte/halfward operations, and the only addressing mode is direct address in register. This tends to produce a large increase in the number of fetched instructions. More details of the above nature are provided which become more reliable as they are cross referenced against other sources.
84. The article describes Bipolar Integrated Technologies ECL SPARC implementation. It is a chip set implementation which runs at 80 MHz and offers 65 MIPs. The power dissipation is too high for AIPS/ALS. However, their P201 process described elsewhere indicates the possibility of a 65 MIPS processor by a 1992 PDR. Also, an 80MHz CMOS architecture (see ISSCC HP 90 MHz CMOS implementation) will deliver about the same performance and is likely to be available by 1992.
85. The article describes the newly released 68040. It claims 21 MIPS and 3.5 DP MFLOPS,and 25 MHz clock rate. It executes 68030 code without modification. A Harvard cache architecture is used. The aggregate cache-processor bandwidth is 200 Mbytes per second.

86. This is a discussion of the Intel 80486 implementation. Its on chip primary cache is inadequate to take full advantage of the chip's performance capabilities and in addition the necessary secondary cache is reported to be difficult to interface.
87. This article is evidence of a trend toward adapting RISC workstation architectures to work in embedded, real time, systems. Ross Technology, a subsidiary of Cypress Semiconductor, has made a cheaper 25 MHz, 18 MIPs SPARC implementation for embedded systems.
88. The description and specification of the M/2000 are presented. This is an R3000/R3010 based system with 64KByte data and instruction caches, 25 MHz clock frequency, and various benchmark results are reported.
89. The Systems Performance Evaluation Cooperative (SPEC) extended its benchmarking standard by adding a "SPECthroughput" measure for evaluating multiprocessor performance as well as more benchmarking results using their "SPECmark" measure. A discussion of the meaning of "SPECmark" and "SPECthruput" is provided. Results for HP, Solbourne, Motorola, DEC, Stardent, Silicon Graphics, MIPS RC6280 (ECL), IBM RS/6000, and Sun implementations are presented. More information is available from SPEC.
90. This discussion of compilers for the MIPS architecture describes its Ada compiler as validated through version 1.9 and as having a front end derived from the Verdix VADs product. Face-to-face discussions with MIPS representatives show an ongoing commitment to Ada. These include plans to validate for future versions and exploration of acquiring a front end which has a lower code expansion coefficient.
91. The MIPS R4000 target specification is confidential. However, the information in this report is consistent with the specification. Conversations with engineers at Performance Semiconductor prior to receipt of the target specification have provided independent corroboration of the data in the specification. Discussions with engineers at Texas Instruments provides additional information from more recent revisions of the specification.
92. The Motorola 68040 microprocessor was announced, officially. It runs at 25 MHz. It claims 20 MIPs performance and 3.5 double precision MFLOPS. Future speeds up to 33 MHz and 50 MHz are planned. It was reported that there has been a lot of erosion in the 68K workstation market share in favor of alternative RISC architectures.
93. This describes the 80960KB hardware. A sustained performance of 7.5 VAX 11/780 MIPS is claimed.
94. This is a comprehensive reference for the R3000/R3010 RISC computer. This functional description applies to all R3000/R3010 implementations including the Integrated Device Technology, LSI Logic, MIPS Computer Systems, and Performance Semiconductor ones.
95. This is a description of the MIPS floating point coprocessor interface including operation, instruction set, exceptions, pinout, timing, and physical characteristics.

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A.3.1 Multi-Chip Module Discussion

1. Electrical interconnect technology beyond the integrated circuit die level tends to limit the performance of very high speed logic. There is an increase in problems related to signal skew, cross talk, spurious reflections, circuit layout, and power dissipation. The solution to this includes higher density integrated circuits and substrates, low dielectric constant material, controlled impedance transmission lines, and internal bypass capacitors. This solution will be called the multi-chip module solution. Another possible approach is to use optical interconnections between integrated circuits on a board. This approach is too immature for use in AIPS/ALS.

   The faster the devices in a given technology are the more critical it is to consider the effect of interconnects. The promise of VHSIC and GaAs VLSI circuits cannot be realized if there are significant losses when interconnecting devices and modules together. Even in CMOS technology, off-chip delays are high enough compared with device speeds to be of serious concern at the system level.

   The area of research that perhaps holds the greatest promise in impacting system performance is that of system packaging In silicon VLSI, it is not unusual to find over 75% of the surface being taken for interconnection. Much research effort has been expended in decreasing device dimensions and decreasing switching speeds. However, these do not reflect proportionally in system speeds because of the losses due to interconnections.

2. The article describes a high speed, high density, wafer scale packaging technology for the implementation of GaAs systems. An example is presented where 23 GaAs dies for a GaAs RISC processor were interconnected on a wafer substrate.

3. Lawrence Livermore is conducting a "Laser Pantography Project" in order to develop Hybrid Wafer Scale Integration for Supercomputing. They are currently packaging a MIPS RISC. Wafers with ten memory chips have been made and tested.

4. A significant gap between integrated circuit technology and packaging and interconnect technology has opened up: a gap in performance, cost, and reliability. However, the two technologies are converging and many of the advanced packaging technologies being developed at MCC are exploiting the materials and process understanding that has been gained in the semiconductor development arena. We can expect, during the 1990s, that a 10 million gate machine will be assembled from 100 chips of 100,000 gates/chip on a single substrate, have a 3 nanosecond cycle time, and cost $1000 less the cost of the chips. MCC feels a copper/polyimide technology will be the best technology to achieve this goal.

5. The packaging session reflects trends in packaging. There is one paper on high density interconnection of chips in multichip modules and it describes a maskless overlay process using copper-polyimide. Kohl et. al. of General Electric Corporate R&D describe their GE HDI program. The approach claims significant advantages : entire chip area is available for interconnect lines; interconnect lines have a <2 mil pitch; via connections to chip pads are direct and of low inductance relative to wire bonds or TAB contacts; computer control leads to high reproduceability; convenient single bare chip testing at speed is feasible; chips of any size and technology can be packed together; and heat dissipation is optimum.

6. A package performance bottleneck is developing because of the inability to densely wire single chip modules together on the printed wiring board. An array processor, constructed by means of various high performance packaging techniques, demonstrates that multichip modules of even modest size can give dramatic improvements in the packaging figure of merit. A comparison of packaging approaches for a 100 chip, 50 MHz, 4.36 million gate implementation of an array processor system is described. Packaging characteristics included density, i/os, interconnections, package performance, and a gates-cm^2/pJ figure of merit.

7. Texas Instruments began a multichip module packaging program, during the VHSIC program, in 1985. Interamics fabricated two size packages : 196 i/o and 308 i/o. The units have distributed power and ground planes and provision for decoupling capacitors. Chip-to-chip interconnection is incorporated in a multilayer tape automated bonding (TAB) system which is customized for each chip combination and will fit a standard i/o pattern in the package. The interconnection materials used were thick film ceramic and a copper polyimide structure.

   The Lawrence Livermore Laser Pantography project has built chip-to-wafer interconnections with up to 1600 gold thin film wires around a 1 centimeter chip. In addition, LLL has built 4 layer interconnect structures using laser planarization and fabrication and testing of thin film transmission lines for wafer scale interconnect using laser pantography.

8. Improvement in circuit density and performance, in both chips and in chip-to-chip interconnections on substrates and printed circuit boards, is continuing to drive advancements in tape-automated bonding (TAB). With VLSI and ASIC devices requiring more than 500 leads on finer pin pitches and running clock frequencies in excess of 50 MHz, semiconductor manufacturers have begun to demand TAB tapes that can handle fast rise times without signal degradation and can minimize any crosstalk between adjacent pins carrying high-speed signals.

9. AT&T Microelectronics has introduced a hybrid circuit fabrication process that matches the source impedance of ICs with the impedance of the traces on the substrate, thus

producing high density circuits capable of handling 600 MHz signals. AT&T calls the process "Polyhic".

10. Several large computer and aerospace houses have had internal multichip module businesses for the last 20 years. Most RISC workstation manufacturers are planning modules for their high speed CPU implementations.

11. The thesis presents an electrical characterization of multilevel aluminum interconnects on a MCM silicon substrate.

12. This article presents some of the activity at the 1990 Nepcon West packaging conference. While there are several approaches to packing multichips on high density substrates, the copper polyimide interconnect method is the most favored for multichip modules. That method uses spin on glass or polyimide techniques to fabricate multilayer thin films for high density, multilayer systems.

    Many believe that the next level of performance in systems will not be achieved without advances in multichip packaging and interconnects, areas that until now have often been ignored. The DEC Vax 9000 and NEC SX-3 computers have been packaged using MCM technology.

    Scientists have begun to explore optical interconnect techniques to overcome the limitations of electrical interconnects. A group from UCSD will present a paper on the subject.

13. The transmission characteristics of wafer scale interconnection lines, which are modeled by weakly coupled slightly lassy transmission lines were investigated.

14. This describes Draper Laboratories research progress in Wafer Scale and Multichip Module packaging.

15. The information describes AT&T's thick-film hybrids, ceramic multilayer boards, thin-film hybrids, and POLYHICs. Properties of thin film and multilayer thin film (POLYHIC) processes are presented.

16. The report describes high speed logic packaging considerations. This is background information for understanding MCM capabilities.

17. Propagation mechanism in interconnection lines on silicon substrates is more complex than in lines deposited on insulating substrates (like GaAs). Theoretical and experimental results show that the resistivity of the silicon substrate plays an important part on the delay and rise times of the signal at the output of the line. It can reach an important value on W.S.I. circuits where lengths up to 10 cm are expected. This

phenomenon limits the upper frequency of the clock in digital applications and induces an important decrease in circuits performances.

18. By 1995 there will be a rapid swing from packaged I.C.'s surface mounted to printed wiring boards to multi-chip modules. These modules will drop rapidly in price from several thousand dollars today to about $200 by 1995 [about AIPS/ALS production time]. The author describes the status of MCC's packaging technologies program.

19. The paper presents the logical and physical design for a physically compact, high-performance computer in which the advantages of an emerging packaging technology are exploited. The machine organization is a message passing, multicomputer. A 1 inch by 2 inch substrate can carry twelve 1 cm^2 dies.

    A machine organization has been proposed and analyzed to exploit polyimide substrate, solder bumping, and button contact packaging techniques for constructing physically compact, high performance computers.

20. A new packaging technology, ideal for CMOS multichip modules is described. Thin film metal and polymer dielectric are used to fabricate 5 metal layer structures with 25 micron wide traces and 11 micron thick dielectric layers. Features on the top pad layer can be fabricated to match the chip pads allowing for orthogonal wire bonding with no fan out. In a microstrip configuration, the typical capacitance is 3.5pF/inch with a time about 54% of the speed of light in vacuum (This corresponds to a polyimide dielectric constant of 3.4). Multi-chip modules have been fabricated for applications ranging from 2 to 25 IC's, plus associated capacitors and resistors.

    With these features, the interconnect related propagation delay due to the capacitive loading or, time of flight, is in most cases less than switching time of the driver gates (normally 1 nsec). Low inductance power and ground planes are used throughout the module with on-board decoupling capacitors. Wire bonds on a 6 mil substrate pitch can be made routinely. The 6 mil pitch consists of a 4 mil pad and a 2 mil spacing between pads. With this pitch and short conductor lengths, bonding parasitics less than 1.2nH are possible. Simultaneous switching noise is drastically reduced over conventional single chip packaging methods. With low interconnect capacitance, the AC power dissipation is low as well.

    A table comparing the R, L, C, G of Printed Wiring Board and MCM is provided.

21. The key process steps: patterning, conductor deposition, reactive ion etching, dielectric deposition, via filling process, and chip to substrate bonding, utilized in the fabrication of high performance thin film multichip modules were discussed. The integration of the developed process steps for the fabrication of a 128 chip memory module which served as a demonstration vehicle was described. The importance of repair techniques

for yield enhancement was addressed, and solutions for defect repairs were proposed. Thin film multichip packaging technology offers high density interconnection capability and design flexibility. To make this technology economically viable, a number of issues still need to be resolved.

22. The paper compares interconnect and substrate technologies with a focus on the density and performance aspects.

23. The paper discusses ground and power plane design parameters of CMOS VLSI multilayer packages. Simulations of the noise generated on the i486 processor package ground plane due to simultaneously switching signal lines driving a system load are presented.

24. Multichip modules are developing in one way to house differing functions and in another way to house memories. Several different Japanese firms, discussed in the article, have MCM packaging capability.

25. DARPA is soliciting industry proposals for the creation of a major US merchant foundry for multichip modules, a technology that many consider to be the next technology in semiconductor packaging for high speed systems. The foundry should be capable of turning out at least 100 digital multichip modules a month, each with overall clock frequencies over 100 MHz. DARPA recently set up its own microelectronics packaging program and has been talking with industry for some time about the direction and intensity of multichip module research.

26. MCC has been awarded a $1.27M contract by DARPA to develop a rapid prototyping tool for multichip modules. The funding is for the first phase of a three phase, three year program that MCC expects will produce a prototype of a programmable Laser Customization Tool.

27. The article describes DEC's MCM packaging of the Vax 9000 series machine. Copper/polyimide is used and offers more than twice the performance of a single chip packaging approach. Other details are provided.

28. A hybrid wafer scale integration technology utilizing laser pantography thin film interconnections is being applied to packaging a RISC architecture multiprocessor system, based on commercially available chips for use in military and space applications.

29. To meet JIAWG's strenuous avionics processing requirements within a SEM-E module's space, several companies are developing unique multichip packaging techniques.

A.3.2 Multi-Chip Module Bibliography

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A.4.1 Optical Interconnect Discussion

1. GaAs's direct bandgap implies optoelectronic properties. These allow the creation of small scale monolithic optoelectronic circuits (MOEIC). An example of a MOEIC is an integrated pin diode, a FET, and a laser diode. High speed fiber optic communications applications (>1 Gigabit per second) are making use of GaAs components. Optical computing, in 1987, is beginning to see R&D activity.

2. Most optoelectronics technology is now at the device (quantum well, laser, lightwave guide, etc.) level. Fabrication of GaAs optical and integrated opto-electronics is being done at Fujitsu, Honeywell, Hitachi, Mitsubishi, NEC, and others. Current markets are emerging for fiber optic communications links. Digital/optical GaAs ICs are critical to driving fiber optics at high speeds.

3. Special funding for technology development should be applied to optical electronics. In particular, the development of optical interconnects, monolithic opto-electronic integrated circuits, optical memory, and optical processing/computing.

4. This paper discusses the possible uses of optical interconnections for VLSI Systems. Interconnections can be applied functions which are 1) physically dispersed, 2) on the same backplane, 3) on the same module, 4) on the same MCM, and 5) on the same VLSI circuit. An overview of electrooptic technology as it pertains to interconnects is provided.

5. The paper describes a high performance packetized data transmitter-receiver device. The implementation is summarized in a table. The device coding scheme is to provide DC balance (i.e. the same number of ones and zeros are in the serial bit stream).

6. GaAs circuits and optoelectronic devices are likely to be found in future computer networks. The first applications will be built around optical connections for data communications. Results with MESFET ICs, laser and integrated receivers are described. A Gb/s link has been demonstrated with two MESFET ICs and one laser array.

   OEIC link activity at IBM is described. GaAs quantum well lasers are used. GaAs MESFET ICs are used. Silicon carriers for chips, optics, and transmission lines are used. Mulimode fibers with low reflection coupling and low mode selective loss connections are used. A transmitter laser array is described. A receiver photodiode array is described. A summary of the used MESFET IC technology is given. The receiver and transmitter 3 mm by 3 mm chips are discussed.

7. The paper outlines fundamental fiber optic benefits and technology. The technology provides much greater communication capacity, electro-magnetic interference

immunity, no ground loop problems, small size, lightweight, and requires no line power. The fiber is fused silica glass with a core surrounded by cladding and comes in multimode and single mode versions. Multimode is used in LANs with distances less than 2 km and bandwidth requirements less than 100 MHz. A table of fiber specifications is provided.

8. This paper addresses the connections made between the optical fibers and the data transmitting and receiving equipment along with intermediate connections in the transmission path. A duplex fiber optic connector is described as an example of a high performance data link implementation.

9. Spending on optical fiber and related components for military interconnections will explode in the early 1990s from $225.1 million in fiscal year 1989 to $441.7 million in fiscal 1994, according to Frost and Sullivan Inc.. Next generation aircraft have fiber optics designed into their sensors, data communications, on-board computers and flight-control systems. Space saving multifiber connectors are a major component in these aircraft including some rack and panel connectors designed to accommodate up to 40 contacts.

10. The role of optics in the near future is limited to interconnects. Processor-to-Processor interconnects can be implemented with optical fibers replacing the electronic data busses. Board-to-Board interconnects have been under study for over a decade and are now close to being implemented. There are power consumption and speed reasons to go to chip-to-chip interconnects but implementation in operating computers is still in the future.

11. The paper contains a detailed comparison between optical and electrical interconnects with the emphasis on advantages and drawbacks of optical link utilization. Attenuation, crosstalk, sensitivity, and fanout, and maximum bit rate are considered. The implementation of optical interconnects into a high performance multichip module was studied. Since polyimide materials are used as the dielectrics for the thin film interconnects various combinations of polyimides are being explored to establish their suitability as optical links. These materials are compatible with processes involved in manufacturing of high performance multichip packages. Typical losses measured for these waveguides were of 3 dB/cm level. Fluorinated polyimides are under investigation due to their lower attenuation.

12. Many new military programs for data communications on mobile platforms require the use of fiber optic systems. The advantages of fiber optic systems include EMI immunity, reduced weight, and increased bandwidth. The components operate over the full military temperature range. One product is the 200 Mb/s hybrid optical data link by AT&T called the ODL 200H. The packaging of this product is discussed. Initial reliability data indicates that the ODL 200H can successfully survive the harsh

military environmental requirements for which it was designed. Information gained from the development of this package is currently being used in a follow on program to develop a surface mount, 0.12 inch high version of the military data link.

13. The book contains fiber optics and GaAs IC information that is applicable to data link design.

14. The article discusses the National Semiconductor FDDI 5 chip-set. The set includes three BiCMOS devices: a physical layer controller, a clock recovery device, and a clock distribution device. A CMOS chip for controlling frames sent between the media and host system and a basic media access controller are the other two chips. NS is using quad packs to cut foot-print size.

15. The interconnection of electronic system modules, boards, and chips will become increasingly difficult using conventional electrical techniques as the required speed and complexity increase. A monolithically integrated optoelectronic interconnect technique based on a metalorganic vapor-phase technique in conjunction with conventional GaAs ion-implanted technology capable of operating up to frequencies as high as 1.8 GHz has been developed. This technology forms the basis for higher level integration involving integrated 8:1 multiplexer-transmitters and 1:8 demultiplexer-receivers for data rates up to 3 Gb/sec.

    Integrated optoelectronic technology based on the metalorganic vapor-phase epitaxial technology in conjunction with direct implanted GaAs IC technology is maturing rapidly. Possible near term applications of this technology include high speed data links between remote systems.

16. The new FDDI standard is being used for 100 Mb/s data rates. However, faster rates are desired. Vitesse Semiconductor, which makes fast GaAs ICs, and Advance Micro Devices, which made the first FDDI chip set, are collaborating on a 1 Gb/s FDDI compatible chip set.

17. IBM made a major concession to intervendor connectivity. In general, FDDI standards are evolving rapidly. IEEE committee 802.5 deals with token ring issues. IEEE 802.1 deals with LAN bridging issues. The IBM proposal will make it easier for suppliers of FDDI gear to develop products that will address the needs of both token ring and Ethernet LANs.

18. The congressional Office of Technology Assessment places most of the blame on structural rather than technical differences between commercial supply and military demand. The conclusions and an analysis of the structural differences appear in a newly published second volume of "Holding the edge" Maintaining the defense

technology base.". The application of these conclusions to fiber optics is analyzed in a 13 page case history in the new volume.

19. The book includes descriptions of Vitesse telecommunication products. These include multiplexors and demultiplexors.

20. The article describes a DARPA funding of Gazelle Microcircuits high speed digital communications circuits which operate at 1 Gb/s and above.

21. A graphic projection GaAs microwave, digital/linear, and optoelectronic ICs is presented. A table showing successful GaAs insertions into military systems is presented.

22. The article discusses the National Semiconductor FDDI chip set.

23. The article discusses how to design FDDI applications.

24. The article describes the next generation of FDDI chip sets that is coming. They are more highly integrated and have lower cost.

25. The article projects the growth in FDDI use. Within two years, FDDI will be established as the dominant high end LAN for the 1990s is a claim that is made.

26. The NASA facility uses high speed fiber links to create a large network. FDDI links are the high performance, back bone links.

27. This discusses working with the ANSI/CBEMA X3T9.5 committee's FDDI standard. In particular, it discusses testing.

28. The paper describes the 250 Mb/s militarized optical transmitter-receiver device.

29. The article discusses the advantages of fiber optic communications.

30. The article discusses near term research and potential applications.

31. The article describes the current state of the monolithic optoelectronic integrated circuit art. These circuits will provide the low cost functionality needed to support fiberoptic network applications.

32. The article describes some recent detector and receiver research results and the applications.

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A.5.1 Radiation Hardened Electronic Discussion

1-2. GaAs has a superior total dose performance when compared to silicon due to the absence of radiation sensitive dielectric layers.

VHSIC Phase 1 technologies and the radiation hardness goals are shown. The means of enhancing the hardness by materials/processing technology are summarized. Circuit design techniques and issues are shown.

3. The paper compares the radiation hardness of GaAs and silicon. With respect to neutron, total dose, dose rate, and single particle phenomena, comparative tables are presented for various GaAs and Silicon logic families. GaAs ICs are relatively neutron hard. GaAs is relatively total dose hard. Transient upset thresholds of GaAs ICs vary widely, corresponding approximately with harder silicon bipolar devices. SEU sensitivity of GaAs cannot be accurately established (1983).

4-15. These papers discuss radiation hardening results presented at the GOMAC 1988 conference.

The qualified manufacturing line and statistical process control concepts are discussed with respect to how it affects ASICs going into radiation hardened systems. Harris Semiconductor has developed a library of radiation hardened standard cells and what special design techniques were made to insure consistent rad-hard ASIC circuits.

The paper discusses a planned move to a radiation hardened substrate from a relatively inexpensive non-hardened one.

A power MOSFET by Harris Semiconductor which is rad-hard is described.

In this paper, an investigation of parameters which affect the throughput of a 1.2 micron radiation insensitive CMOS process lead to the derivation of simple equations for rise and fall time delays.

The response of resistive load SRAMs in a dose rate environment is described. The relative dominance of local and distributed dose rate effects in these circuits is presented. Methods for prediction of the interaction of the two mechanisms (i.e. local and distributed) with a minimum of design information and experimental data, are presented. Issues of the applicability of resistive load circuits in dose rate environments are discussed.

The RH32 project at RADC will finish a radiation hardened 32-bit MIPS architecture RISC by 1992. The paper briefly discusses a Unisys effort which is related to the RH32 project.

A radiation hardened VHSIC 5V 10K Gate Array has been fabricated for space applications by Westinghouse. This has been accomplished by the substitution of only two of the base silicon masks and without increasing process complexity or chip area. This enables the fabrication of radiation hardened gate arrays using already existing logic designs and interconnect personalizations.

The SAT-081 program is developing technology that will be available to all U.S. Government sponsored programs. Results to date have attained level I hardness and demonstrate the potential to reach level II. The circuits used to demonstrate the above will be available in 100s quantities within a few months (1988).

16-20. These articles present the radiation hardening results for GaAs Digital ICs as presented at the DARPA DSO 1989 Digital IC Conference.

The Electronics Research Laboratory has irradiated some of the devices produced by other program participants. A test chip in association with JPL is being sent to MOSIS. The objectives are to assess neutron hardness of GaAs devices and to enhance the accuracy and timeliness of the GaAs reliability data.

The radiation hardened SEU tolerant microcomputer chip effort has four objectives : develop SEU tolerant CPU architecture, use GaAs for high speed and rad-hardness, develop high speed GaAs VLSI design baseline, and demonstrate rad-hard SEU tolerant circuit. Their effort is scheduled to finish in FY92.

JPL is validating GaAs IC fabrication by statistical assessment of their electrical process and device parameters.

The Martin Marietta On-Board Space Processor program seeks to develop GaAs VLSI suitable for space. The desired qualities are low power, SEU, and reliability. Their program will end in FY 1991.

21. The article discusses how Qualified Manufacturing Lines handle the qualification of radiation hardened components for Space.

22. The two volume set is a comprehensive 1983 study of radiation effects in optoelectronic devices including light emmitting diodes, laser diodes, optical fibers, photodetectors, and multicomponent devices. A section on system consideration with respect to these effects is included.

23. This reports radiation hardening within the VHSIC program.

24. The article discusses Class S screening prior to the QML program.

25. The article explains how limited experimental information can be used to make conservative design estimates with respect to SEU in CMOS.

26. The report reviews primary physical processes underlying the response of electronic materials and devices to radiation as well as the relationship of the processes to the modes of circuit degradation and failure.

27. The presentation summarizes results and plans for SAT-081 related programs.

28. The report summarizes existing SEU data.

29. Within the 1989 GOMAC papers are the following relevant papers:

    "A High Performance 'Non-Upsetable' 64K Rad-Hard Simox SRAM"
    "GaAs Quality, Material Assessment, and Reliability Evaluation"
    "Reliability of a VLSI Rad-Hard CMOS Technology"
    "GaAs IC Failure Rate Models"
    "VHSIC Phase-1 Radiation Hardening Program: Extension to Space Levels"
    "The Title III SOS Program"
    "64kx1 and 8kx8 Rad Hard SEU Immune Static RAMs"

30. The paper presents a mathematical model which yields estimates of the upper and lower bounds on the rates of SEU's in logic circuits.

31. This experimental study presents SEU empirical modeling examples. In general, the data support the adoption of a simplified worst case model in which the cross section for SEU by an ion above a threshold energy equals the area of the memory cell.

32. The paper discusses the response of an enhancement mode MOSFET to a cosmic ray ion that passes perpendicularly through its gate oxide layer.

33. The paper presents experimental measurements on lateral spreading of ion track induced charge in integrated circuits. The results will improve the quality of IC design with respect to single event upsets.

34. Discusses the susceptibility of memory devices to single bit upsets. In addition, the soft error rate is estimated as a function of design and parametric variations.

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16. Abstract

The major goals of this effort are as follows: examine technology insertion options to optimize Advanced Information Processing System (AIPS) performance in the Advanced Launch System (ALS) environment, examine the AIPS concepts to ensure that valuable new technologies are not excluded from the AIPS/ALS implementations, examine advanced microprocessors applicable to AIPS/ALS, examine radiation hardening technologies applicable to AIPS/ALS, reach conclusions on AIPS hardware building blocks implementation technologies, and reach conclusions on appropriate architectural improvements. The hardware building blocks are the Fault-Tolerant Processors, the Input/Output and InterComputer Networks and interfaces between the processors and the networks, viz., Input/Output Sequencers (IOS) and the InterComputer Interface Sequencers (ICIS).

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