Architecture for Survivable System Processing (ASSP)

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SUMMARY:

The ASSP Program is a multi-phase effort to implement DOD and commercially developed high-tech hardware, software and architectures for reliable space avionics and ground based systems. System configuration options provide processing capabilities to address Time Dependent Processing (TDP), Object Dependent Processing (ODP) and Mission Dependent Processing (MDP) requirements through Open System Architecture (OSA) alternatives that allow for the enhancements, incorporation and capitalization of a broad range of development assets. High technology developments of hardware, software, networking models address technology challenges of long processor life times, fault tolerance, reliability, throughput, memories, radiation hardening, size, weight, power (SWAP) and security.

Hardware and software design, development and implementations focus on the interconnectivity/interoperability of an open system architecture and is being developed to apply new technology into practical OSA components. To insure for widely acceptable architecture capable of interfacing with various commercial/military components, this Program provides for regular interactions with Standardization Working groups (eg) the International Standards Organization (ISO), American National Standards Institute (ANSI), Society of Automotive Engineers (SAE), and Institute of Electrical and Electronic Engineer (IEEE). Selection of a viable open architecture is based on the widely accepted standards that implement the ISO/OSI Reference Model.

DEVELOPMENT:

The ASSP Program provides research and development tasks to implement heterogeneous processing nodes of various configurations into the OSA network. Each node resides on a single circuit card with onboard scalar, vector processing components. (See Figure 1).

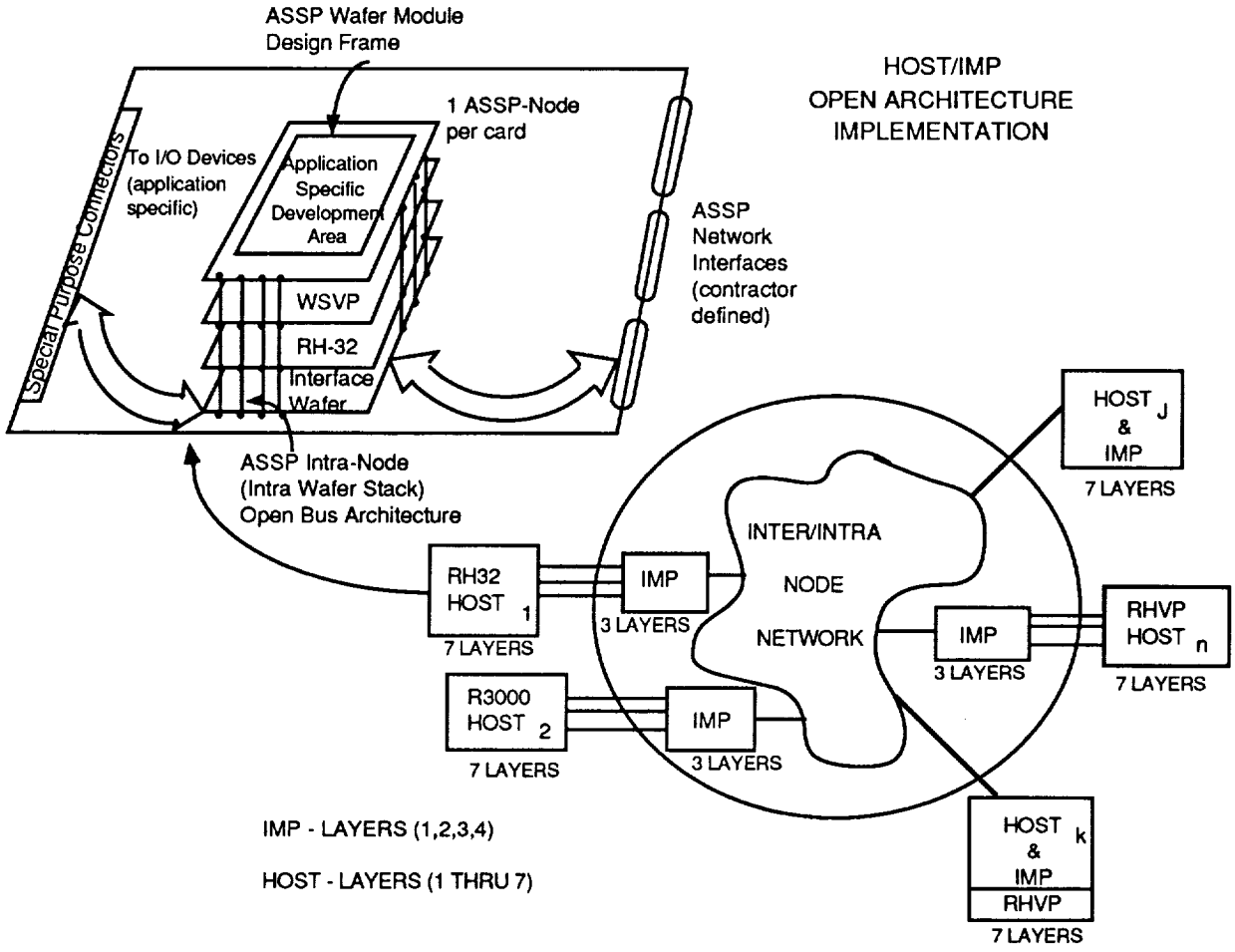

FIGURE 1

Simulation and demonstrations will be accomplished to incorporate processing components (i.e. 3D Computer, AOSP LAN, large memories, associated co-processor) into the expandable open architecture. As such, key features include standard bus hardware/protocols, support for tightly coupled and/or loosely coupled multiprocessing, and object oriented operating system primitives. The ASSP will build on the successes of the Advanced Onboard Signal Processor (AOSP) program by furthering system reliability through shrinking node size, improving reliability at each level of the architecture through incorporation of fault tolerance techniques, and exploiting the latest advances in fault tolerant, secure operating systems design. As hardware development technology provides more capable and innovative components, such as radiation hardened, WSI, HDI, Photonics, Wafer Stacking and application specific integrated circuits (ASIC), they will be implemented into the ASSP phase two effort. Integration along with developments of form fit factors to support physical space budgets will be demonstrated as an Advanced Development Model (ADM).

The major thrust of this program will address the key technical challenges for:

a. Open system architectures for rapid insertion of commercial/military technology
b. Interoperability/Interchangeability of heterogeneous processing nodes
c. Architectural incorporation of stacked hybrid wafer integration
d. Fault tolerant, real-time ADA Run-time systems for distributed heterogeneous processors

The ASSP program also includes implementation of industry and/or military hardware/software in accordance with standards that conform to the International Standards Organization, Open System Interconnection (ISO/OSI) Reference model (ISO 7498). To meet these objectives, advanced state of the art language and modeling designs/developments will be made to adequately represent each of the ISO/OSI levels, their interactions, and additions. (See Figure 2).

ISO/OSI REFERENCE MODEL

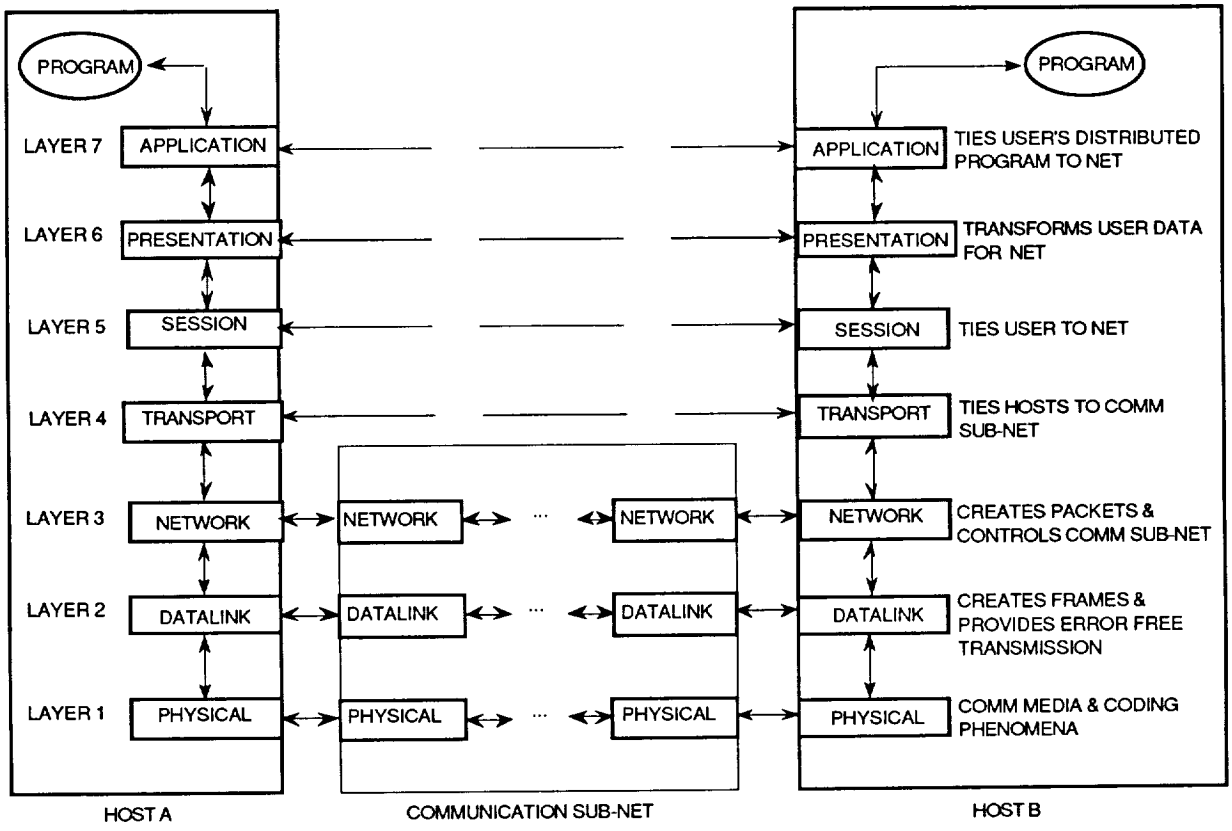

FIGURE 2

The Reference model will provide specifications for networks, backplanes, interfaces, and busses to support open systems. Model simulations will be developed and tested to ensure conformance with objectives that provides commonality, high performance, availability, and fault tolerance.

Implementation of current high technology components in this effort such as the WSVP, RH32, RHVP, WSI-HDI, Radiation Hardened Memories as well as commercial components like MIPS R3000 and Intel i860 processors in an "open architecture" processor network will be seriously considered for integration and demonstrations.

The two phased program is a five year effort with the first phase being two years duration. During this first phase, intensive studies of commercial and military hardware/software systems and components will be made to assess applicability for integration into the OSA. The design of an architecture adhering to accepted standards and responsive to space based applications will then be performed. The selected design will consider Intra-Nodal multiprocessing networks (Sub-net, or within a node or single board), Inter-Nodal Multi-processor networks (array of processors loosely or tightly coupled) and Inter-Satellite networks (Super-net, loosely coupled, communications may be micro-wave). (See Figure 3).

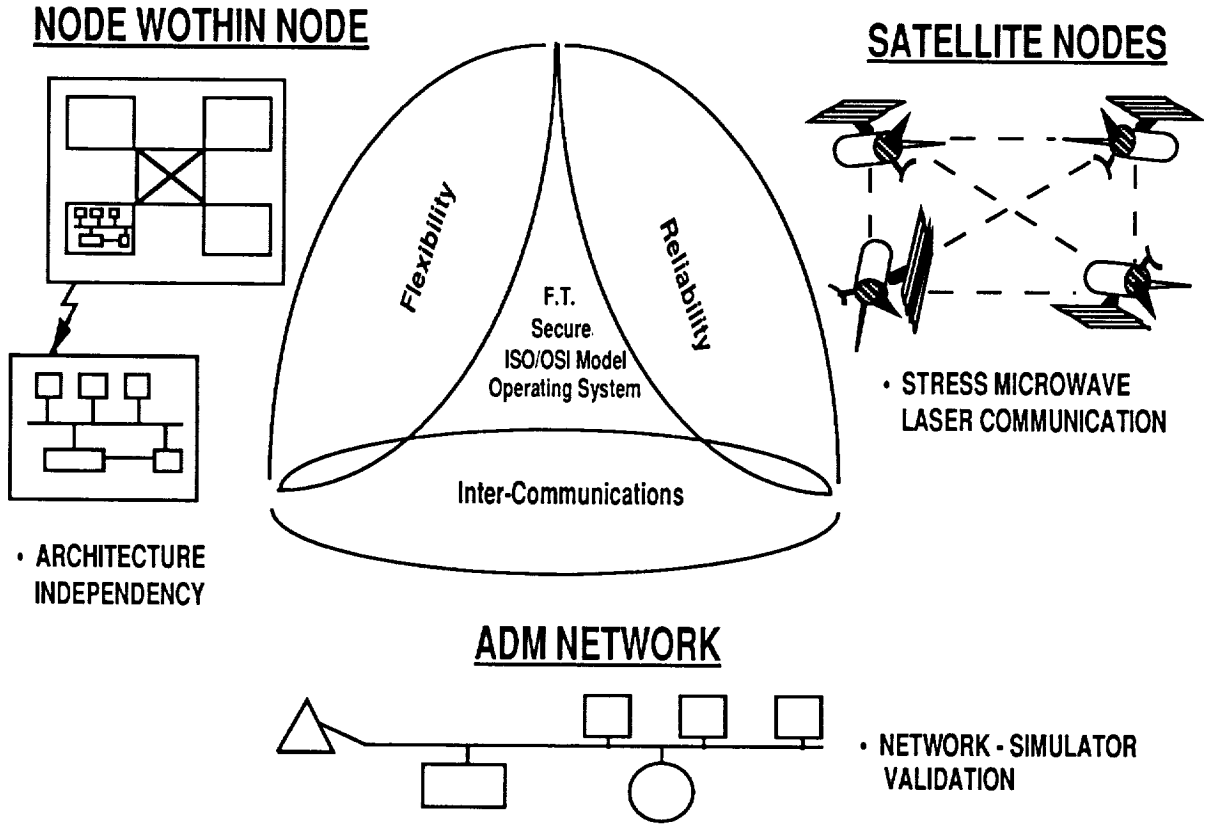

FIGURE 3

During the study and evaluation period, research in network simulators and tools will also be accomplished. New developments will be undertaken to support requirements where deficiencies occur. A final simulator configuration will then be selected and developed that will represent the Inter-Nodal Multi-Processor Network (INMPN) and also be the baseline design to support further development of the simulators for the Subnet and Supernet configurations. The INMPN simulator will be

used to prove the breadboard design concept of the OSA selected prior to the Preliminary Design Review (PDR).

The Phase I activities develop technology to control the open system via operating software that conform to layered protocols that implement the ISO/OSI model. Investigation of capabilities and potential applications of POSIX, SAFENET, NOS/GOS, and GOSIP will be accomplished, as well as hardware components such as Wafer Scale Vector Processors, military and commercial RISC/CISC processors. These components will be "retro-fitted" into the OSA via bus interface units (BIU's) to prove feasibility and acceptability of heterogeneous processors to operate as an integrated system.

Successful completion of Phase I will provide an operational application demonstration with a breadboard model of open system design exercising the heterogeneity of hosts. Capabilities will include graceful degradation, error recovery, dynamic routing and high performance capabilities with minimal latencies. The breadboard model along with respective simulations will provide the basis for implementation validation and design verification. Specifications, simulators, software development platform, and the baseline Open System Architecture will then be transitioned to Phase II.

Phase II is a three year program which basically reduces into hardware design the results obtained from Phase I. However, because of the updating of standards and to take advantage of new technology the Phase I architectural design will be refined to maximize responsiveness to the user community.

The Industrial/Commercial community has already widely accepted the standardization processes being offered by the ISO, ANSI, IEE etc. Therefore, Phase II will take advantage of this cooperation and inturn incorporate commercial breakthroughs in processor, communications and network technologies. Radiation hardened components, high technology processors such as the 3D computer, Gallium Arsenide developments, Photonics and Opto-Electronics technologies will be incorporated into the Open Systems where applicable to further advance the state of the art in network processing OSA. Components will be integrated without BIU's as the standardization regimens will dictate requirements to meet interoperability/interchangeability criteria.

To insure the proper application of developed standards (the ASSP program will NOT develop standards) associated contractors and the Technical Advisory Group (TAG) will work very closely with Standardization Working Groups of the various standardization communities. The TAG will be composed of government only experts in the fields of networking, fault-tolerance, security, reliability-maintainability, signal-data processing, memories, software and packaging. The TAG will insure that proper design and architectural plans are acceptable and representative of the government's interest. That the Architecture selected is widely acceptable by the military, industrial, commercial complex and where ever possible insure that potential standards specifically attributable to space based applications are considered by the Standardization committees.

Successful completion of Phase II will provide an Advanced Development Model (ADM) that will demonstrate interoperability/interchangeability along with the

above iterated assets in an Open Systems Architecture Network. This will provide the acceptable standard multiprocessor interconnects, high performance backplanes, switch networks, and network operating system.

The ASSP directly responds to an AIR FORCE, SDIO deficiency in providing an architecture that can support and upgrade processing systems without major redesigns, and procurements. This program also provides capabilities to launch processing networks that are versatile, offer various levels of complexity and are capable of rapid upgrades in mission profiles, hardware, and operating systems. The capability to incorporate commercial hardware breakthroughs along with their respective software support in a very short time frame and with a minimum of redesign/retooling is most beneficial and advantageous to the military-commercial community.