LABORATORY MEASUREMENTS OF ON-BOARD SUBSYSTEMS

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SUMMARY

Good progress has been achieved on the Test Bed for On-Board Subsystems for future satellites. The Test Bed is for subsystems developed under previous INTELSAT R&D contracts. Four test setups have been configured in the INTELSAT Technical Laboratories:

1. TDMA On-Board Modem (MODEM, MELCO);
2. MultiCarrier Demultiplexer Demodulator (MCDD, TELESPAZIO/ALCATEL);
3. IBS/IDR BaseBand Processor (BBP, NEC); and
4. Baseband Switch Matrix (BSM, NEC).

The first three series of tests are completed and the tests on the BSM are in progress. Descriptions of test setups and major test results are included in this poster presentation; the format of the poster is outlined below. A companion paper discusses the systems benefits and constraints, and summarizes the status of these on-board technologies [Ref. 1].

TITLE PAGE

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*               MODEM           *            * -            MCDD             -
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+                             + :                  :  BBP        :          :
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+          BSM                +++++++++++++++++++++++++++++++++++++++++++++++++++
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*This paper was presented in Session 4: Concurrent Poster Presentations and Demonstrations. Row and column numbers explain the poster layout.
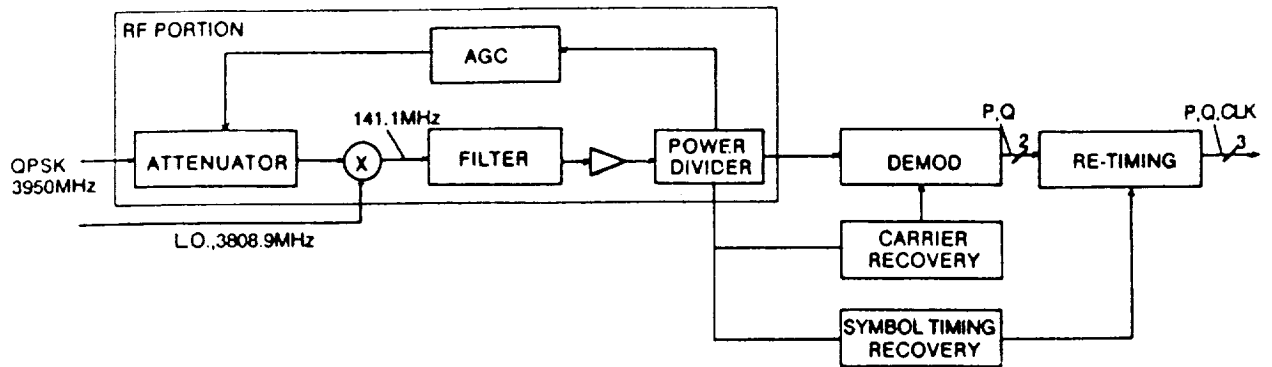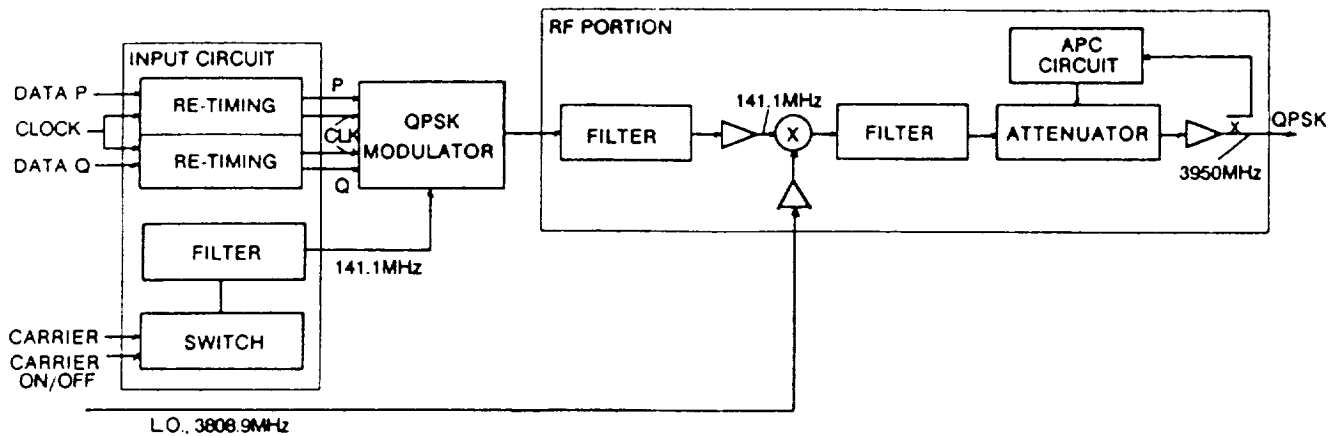
FIGURE 1 (A)   ON-BOARD DEMODULATOR

FIGURE 1 (B)   ON-BOARD MODULATOR

THE CODE GENERATOR PRODUCES
THE P, Q, CLOCK AND GATE SIGNALS (IN BURST MODE).

THE CODE ERROR DETECTOR ACCEPTS THE P, Q, AND CLOCK SIGNALS
AND THE STATUS AND APERTURE SIGNALS FROM THE CODE GENERATOR
AND MAKES BER, UNIQUE WORD MISSING DETECTION (UWMD) TESTS ETC.

THE ADAPTER IS AN INTERFACE BETWEEN THE CODE GENERATOR,
CODE ERROR DETECTOR AND THE EARTH STATION (E/S) MODEM.

ATTENUATOR 1 IS USED TO ADJUST THE INPUT SIGNAL LEVEL
TO THE UPCONVERTER, WHICH IS ABOUT -20 DBM.

SWITCH 1 CONTROLS THE SIGNAL CONNECTION FOR SIGNAL MONITORING
AND E_b/N_o CALIBRATION DURING THE MEASUREMENT PROCESS.

ROW 1, COLUMN 1

THE BURST 3950-MHz RF SIGNAL IS FED TO THE RF PORTION WHICH INCLUDES
THE DOWNCONVERTER, THE IF ROLL-OFF FILTER AND THE AGC CIRCUIT.

THE DEMODULATION CIRCUIT IS A COHERENT DETECTOR.

THE CARRIER RECOVERY CIRCUIT CONSISTS OF A TIMES-FOUR MULTIPLIER,
A TANK-LIMITER WITH AFC (AUTOMATIC FREQUENCY CONTROL)
AND A DIVIDE-BY-FOUR CIRCUIT.

THE SYMBOL-TIMING-RECOVERY CIRCUIT CONSISTS OF THE IF SQUARING CIRCUIT
AND TANK-LIMITERS.

IN THE MODULATOR, THE P AND Q STREAMS AND THEIR CLOCK OF 60.416 MHz
(DATA RATE IS 120.832 MBIT/S) ARE RECEIVED BY THE RETIMING CIRCUIT.
P AND Q STREAMS ARE SYNCHRONIZED BY THE CLOCK.

THIS SWITCH IS CONTROLLED BY THE CARRIER ON-OFF SIGNAL
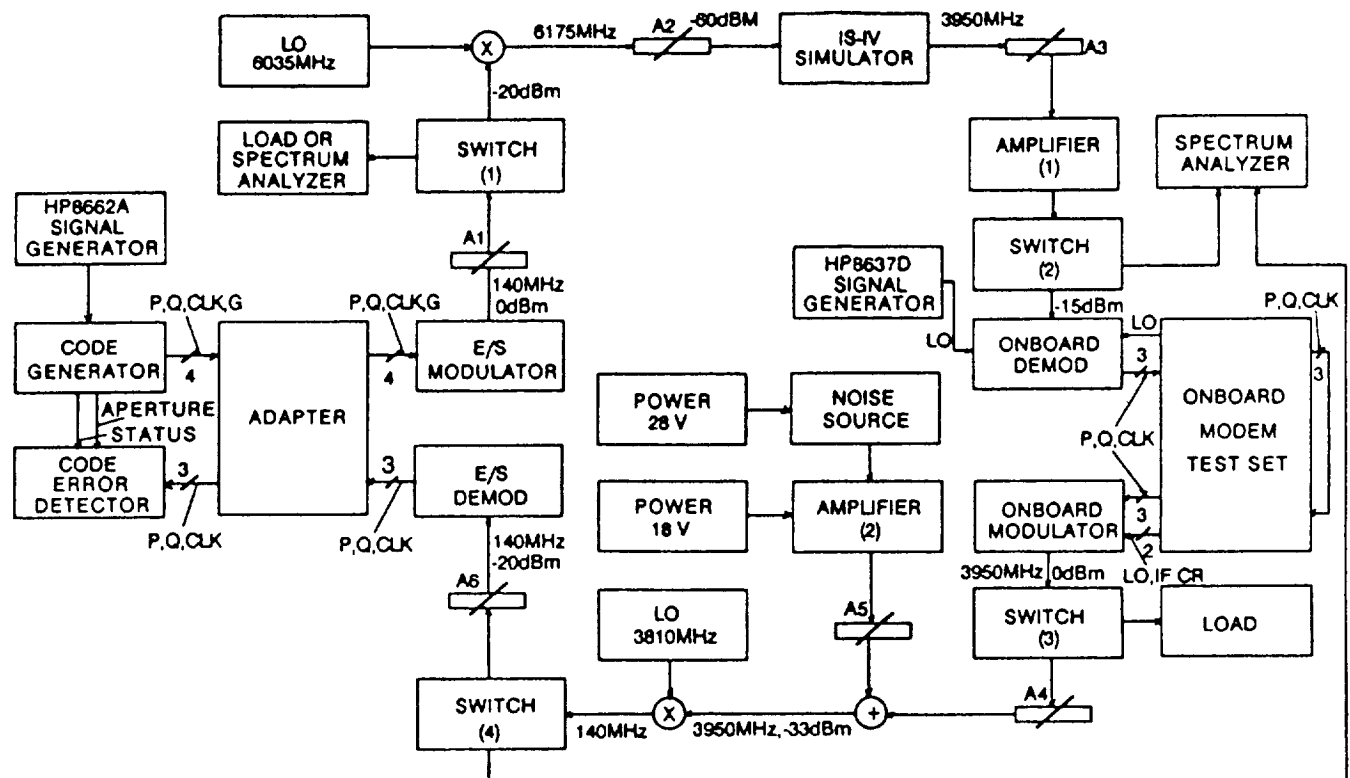FROM THE TEST SET AND IT CONTROLS THE OUTPUT OF THE MODULATOR.

FIGURE 2   BER TEST SETUP

ROW 1, COLUMN 2

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THE EQUIPMENT FROM THE CODE GENERATOR TO THE UPCONVERTER SIMULATES THE FUNCTION OF THE E/S TRANSMITTER IN WHICH THE QPSK-MODULATED 6-GHz SIGNAL IS PRODUCED.

THE LOW NOISE AMPLIFIER (LNA) IS IN THE INTELSAT-IVA TRANSPONDER SIMULATOR. ATTENUATOR 2 IS USED TO CONTROL THE SIGNAL LEVEL TO THE LNA AMPLIFIER AND TO CALIBRATE THE UPLINK E_b/N_o.

A DOWNCONVERTER WITH LO FREQUENCY OF 2225 MHz IS ALSO IN THE INTELSAT-IVA TRANSPONDER SIMULATOR.

SWITCH 2 IS USED TO CONTROL THE SIGNAL CONNECTION FOR SIGNAL LEVEL AND SPECTRUM MEASUREMENT OR MONITORING IN THE TEST PROCESS; THIS IS DONE WITHOUT CHANGING THE PHYSICAL CONNECTION IN ORDER TO IMPROVE THE MEASUREMENT ACCURACY AND FACILITATE OPERATION.

THE DEMODULATED P AND Q SIGNALS AND RECOVERED CLOCK FROM THE ON-BOARD DEMODULATOR PASS THROUGH THE BUFFER AND CONDITIONING CIRCUITS IN THE MODEM TEST SET.

SWITCH 3 IS FOR DOWNLINK E_b/N_o CALIBRATION AND SIGNAL MONITORING. THE VARIABLE ATTENUATOR 5 IS USED TO CONTROL THE NOISE LEVEL TO REACH THE REQUIRED DOWNLINK E_b/N_o. SWITCH 4 IS USED FOR DOWNLINK E_b/N_o CALIBRATION AND SPECTRUM MONITORING WITHOUT CHANGING THE PHYSICAL CONNECTION.

IN THE BER TEST, THE MEASURED PERFORMANCE IS THE SUMMATION OF THE UPLINK AND DOWNLINK BERs. IF THE UPLINK (OR DOWNLINK) E_b/N_o IS VERY HIGH, FOR INSTANCE OVER 40 dB, THE MEASURED RESULT WILL MAINLY INDICATE THE PERFORMANCE OF THE DOWNLINK (OR UPLINK RESPECTIVELY).

THE E_b/N_o CALIBRATIONS ARE DIFFERENT FOR THE UPLINK AND THE DOWNLINK. FOR THE UPLINK, THE NOISE IS MAINLY THE THERMAL CONTRIBUTION FROM THE LNA IN THE INTELSAT-IVA TRANSPONDER SIMULATOR. THE SPECTRUM ANALYZER IS USED TO MEASURE THE SIGNAL LEVEL (UNMODULATED CARRIER) AND THE NOISE POWER DENSITY (IN dBm/Hz).

FOR THE DOWNLINK, AN INDEPENDENT NOISE SOURCE IS USED. THE SPECTRUM ANALYZER MEASURES THE UNMODULATED CARRIER LEVEL UNDER VERY WEAK NOISE CONDITIONS, AND THE NOISE SPECTRAL POWER DENSITY WITHOUT THE SIGNAL. IN THE ENTIRE CALIBRATION PROCESS THE SIGNAL CONNECTION IS CONTROLLED BY SWITCHES WITHOUT CHANGING ANY PHYSICAL CONNECTION, SO THE CALIBRATION ERROR IS REDUCED SIGNIFICANTLY.

ROW 1, COLUMN 3

THE DEMULTIPLEXER SEPARATES THE CHANNELS USING A PER-CHANNEL, ANALYTIC SIGNAL APPROACH.

THE DEMODULATOR IS A SINGLE-CHANNEL DEMODULATOR THAT RECOVERS THE TRANSMITTED BIT STREAM AND OUTPUTS IT TO A BASEBAND SWITCH MATRIX. THE BIT RATE OF THIS MCDD CANNOT BE VARIED AND ONLY ONE CHANNEL CAN BE PROCESSED AT ANY ONE TIME. THE INPUT FDMA SIGNAL HAS A 10-MHz BANDWIDTH AND CONSISTS OF 3 CHANNELS AT 4.4 MBIT/S TRANSMISSION RATE, OR 12 CHANNELS AT 1.1 MBIT/S TRANSMISSION RATE; IT IS SAMPLED AT A RATE OF ABOUT 20 MHz.

AN ANALOG INPUT INTERFACE IS PROVIDED THAT IS ABLE TO ACCEPT THE SIGNAL AT INTERMEDIATE FREQUENCY (140 MHz), TO PERFORM THE ANTI-ALIASING FILTERING AND THE DOWN-CONVERSION TO BASEBAND, SO THAT THE FINAL ANALOG-TO-DIGITAL CONVERSION IS DONE AT NYQUIST RATE.

AT THE OUTPUT OF THE MCDD, A DIGITAL-TO-ANALOG CONVERTER IS USED FOR THE PURPOSE OF TESTING, AND ALLOWS AN OSCILLOSCOPE TO BE USED TO OBSERVE SIGNAL CONSTELLATIONS AND OTHER SIGNIFICANT PARAMETERS.

THE FDMA SIGNAL GENERATOR CONSISTS OF A BANK (THREE IN THIS CASE) OF MODULATORS WHICH HAVE THE SAME CONFIGURATIONS BUT THEIR CARRIER FREQUENCIES CAN BE SELECTED INDEPENDENTLY WITHIN CERTAIN RANGES.

THE HP3326A SYNTHESIZER PROVIDES THE REQUIRED CLOCK SIGNAL TO THE HP3762A DATA GENERATOR WHICH PRODUCES THE DATA SEQUENCE AND CLOCK.

THE ALCATEL SYNTHESIZER PROVIDES THE SOURCE FREQUENCY TO THE FDMA SIGNAL GENERATOR. IT CAN PRODUCE A MAXIMUM OF 3 MODULATED CARRIERS SIMULTANEOUSLY. THE HP3708A NOISE TEST SET IS USED TO INTRODUCE GAUSSIAN NOISE IN THE CHANNEL UNDER TEST.

A0 IS THE OUTPUT ATTENUATOR INSIDE THE FDMA SIGNAL GENERATOR. ATTENUATORS A1 AND A2 ARE USED TO ADJUST THE SIGNAL LEVEL TO MEET THE REQUIREMENTS OF THE HP3708A NOISE TEST SET AND THE MCDD. THE HP8566B IS FOR SPECTRUM MONITORING AND ANALYSIS.
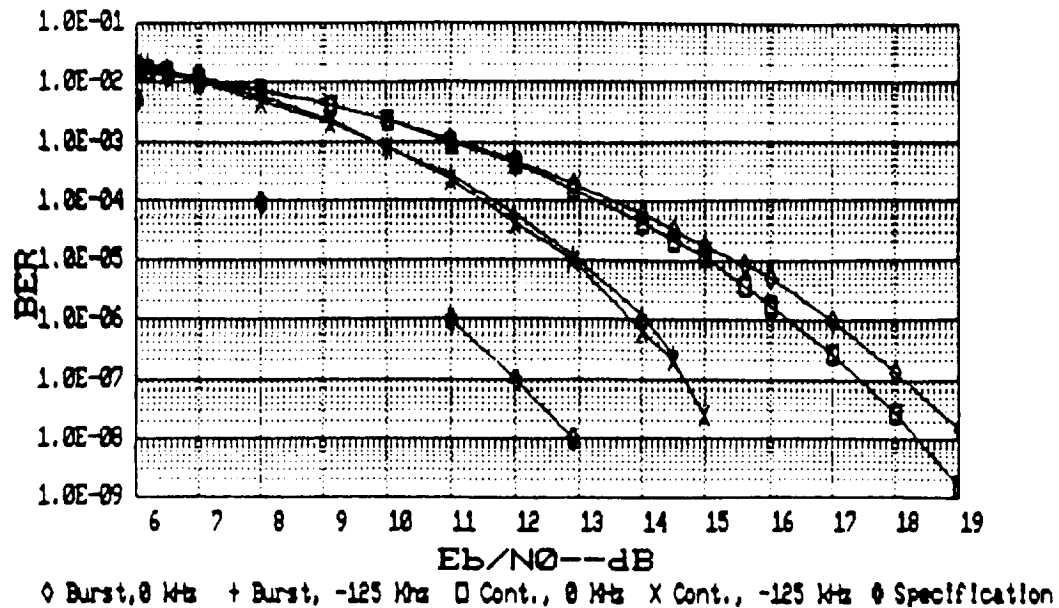
ROW 1, COLUMN 4

FIGURE 3   UPLINK BER FOR MODEM

THE UPLINK BER IS AN INDICATION OF THE ON-BOARD DEMODULATOR PERFORMANCE. THE BER VERSUS E_b/N_o FOR THE BURST MODE AND CONTINUOUS MODE ARE SIMILAR. THE UPLINK E_b/N_o NEEDS TO INCREASE BY 2.1 TO 4.7 DB IN ORDER TO GET THE SAME BER AS DEFINED IN THE SPECIFICATION. THE DEGRADATION REDUCES TO 0.7 TO 1.6 DB WHEN THE LO FREQUENCY OFFSET IS AT ABOUT -125 KHZ OR THE CARRIER FREQUENCY OFFSET IS +125 KHZ.
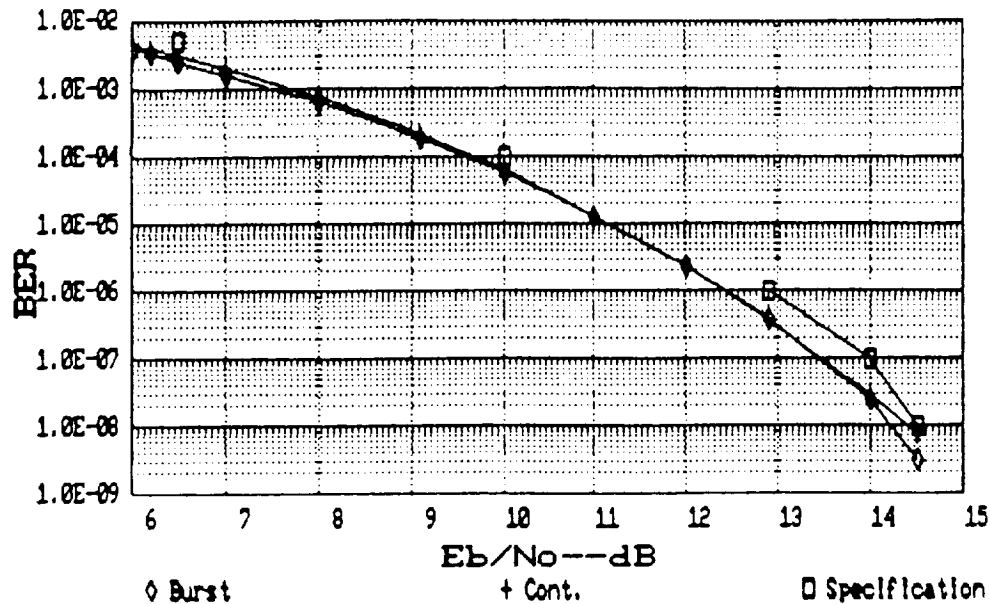
ROW 2, COLUMN 1

FIGURE 4   DOWNLINK BER FOR MODEM

THE DOWNLINK BER REFLECTS THE ON-BOARD MODULATOR AND THE E/S
DEMODULATOR PERFORMANCE. THE BER VERSUS E_b/N_o FOR THE BURST MODE
AND THE CONTINUOUS MODE ARE VERY SIMILAR. FOR THE BURST MODE,
THE MEASURED BER VERSUS E_b/N_o IS BETTER THAN THE SPECIFICATIONS,
BY ABOUT 0.3 TO 0.6 DB FOR THE ON-BOARD MODEM
AND BETTER BY ABOUT 1.1 TO 2.0 DB FOR THE E/S MODEM.

DURING TESTS OF AMPLITUDE VARIATIONS, THE SWITCH ON THE CODE GENERATOR
WAS USED TO SELECT THE OPERATION MODE AND MEASURE THE CARRIER LEVEL
WITH THE SPECTRUM ANALYZER. IN THE FIXED MODE (NO MODULATION) BOTH P
AND Q CHANNELS CAN BE SET WITH SWITCHES FOR A CONSTANT 0 OR 1, WHICH
PRODUCES AN AMPLITUDE VARIATION OF 0 DB. IN THE CONTINUOUS MODE A
PSEUDO-RANDOM SEQUENCE IS SELECTED TO MODULATE A CONTINUOUS CARRIER.
THE PEAK-TO-PEAK AMPLITUDE VARIATION IN THIS CASE IS 0.6 DB,
SO THE MODEM MEETS THE SPECIFICATION OF ±0.5 DB AMPLITUDE VARIATION.

CARRIER ON/OFF ISOLATION WAS MEASURED AS 55 DB
AND EXCEEDS THE SPECIFIED 50 DB.

THE SPECIFICATION OF PROBABILITY OF UNIQUE WORD MISSED DETECTION (UWMD)
IS BETTER THAN 1×10^{-8} WHEN THE E_b/N_o IS EQUAL TO 7 DB.
THE TEST RESULT SHOWS THAT ABOUT 2 DB E_b/N_o INCREASE IS NEEDED
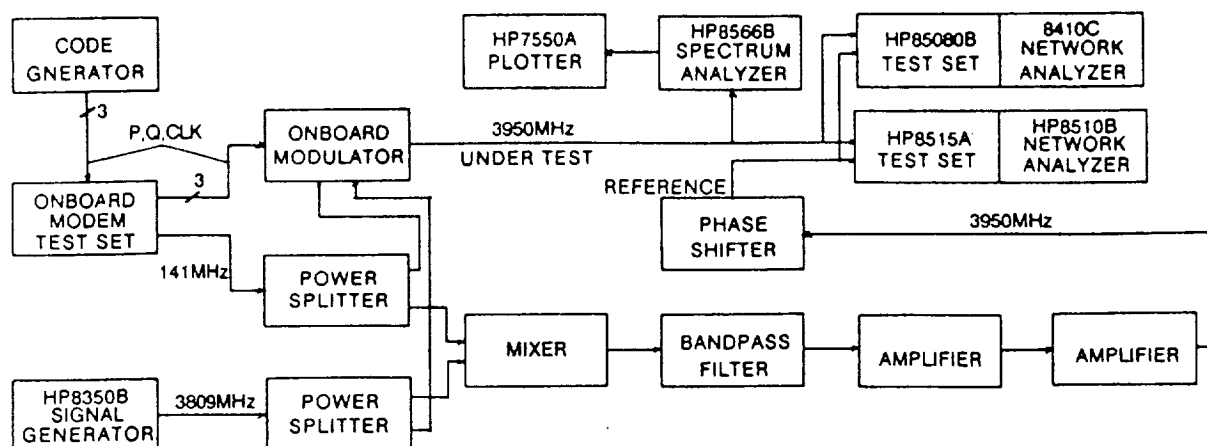TO MEET THAT UWMD PROBABILITY.

ROW 2, COLUMN 2

FIGURE 5   TEST SETUP FOR CARRIER PHASE SHIFT
            AND AMPLITUDE VARIATION

THE HP8510B NETWORK ANALYZER IS USED FOR PHASE SHIFT MEASUREMENTS BY
COMPARING THE MODULATED CARRIER WITH THE REFERENCE CARRIER.

SINCE THE PURPOSE IS TO MEASURE THE RELATIVE PHASE DIFFERENCES AMONG
THE 00, 01, 11, 10 PHASES, THE ACCURACY OF THE ABSOLUTE VALUE IS NOT
VERY IMPORTANT.

WITHIN THE ON-BOARD MODULATOR, THE P AND Q DATA MODULATE THE IF CARRIER
OF 141 MHz FIRST, THEN THE IF CARRIER IS UPCONVERTED TO 3950 MHz. THIS
MODULATED SIGNAL IS SENT TO THE NETWORK ANALYZER FOR PHASE SHIFT
MEASUREMENTS.

THE REFERENCE SIGNAL HAS THE SAME RF FREQUENCY AND IS PHASE COHERENT TO
THE MODULATED CARRIER (UNDER TEST) OF THE ON-BOARD MODULATOR.

THE OUTPUT OF THE MIXER HAS THREE PRODUCTS AT VERY CLOSE LEVELS AT 3950
MHz (SUMMATION), 3809 MHz (LO) AND 3668 MHz (DIFFERENCE) RESPECTIVELY.
THE FREQUENCY OF THE DESIRED PRODUCT IS 3950 MHz AND THE FILTER SELECTS
THE DESIRED ONE.

THE PHASE SHIFTER IN THE REFERENCE CHANNEL IS USED TO COMPENSATE THE
STATIC PHASE DIFFERENCE BETWEEN THE TWO CHANNELS.

TEST RESULTS ARE 0.0, 90.7, 180.2, 269.4 DEGREES FOR THE FOUR PHASE
STATES AND MEET THE SPECIFICATIONS (0, 90, 180, 270, ±2 DEGREES).
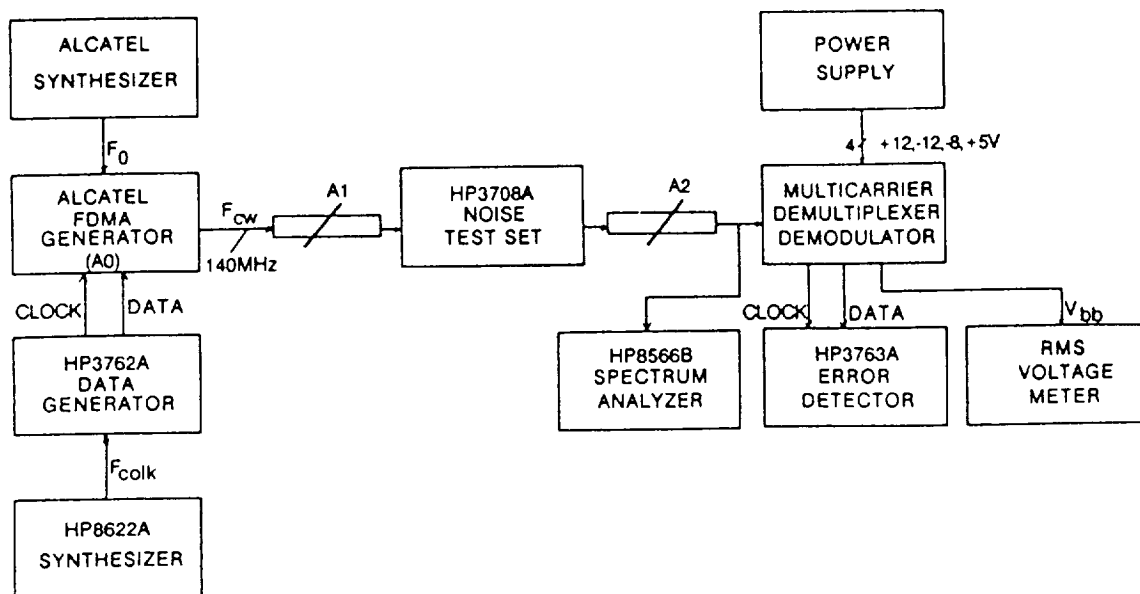
ROW 2, COLUMN 3

FIGURE 6   BER TEST BED FOR MCDD
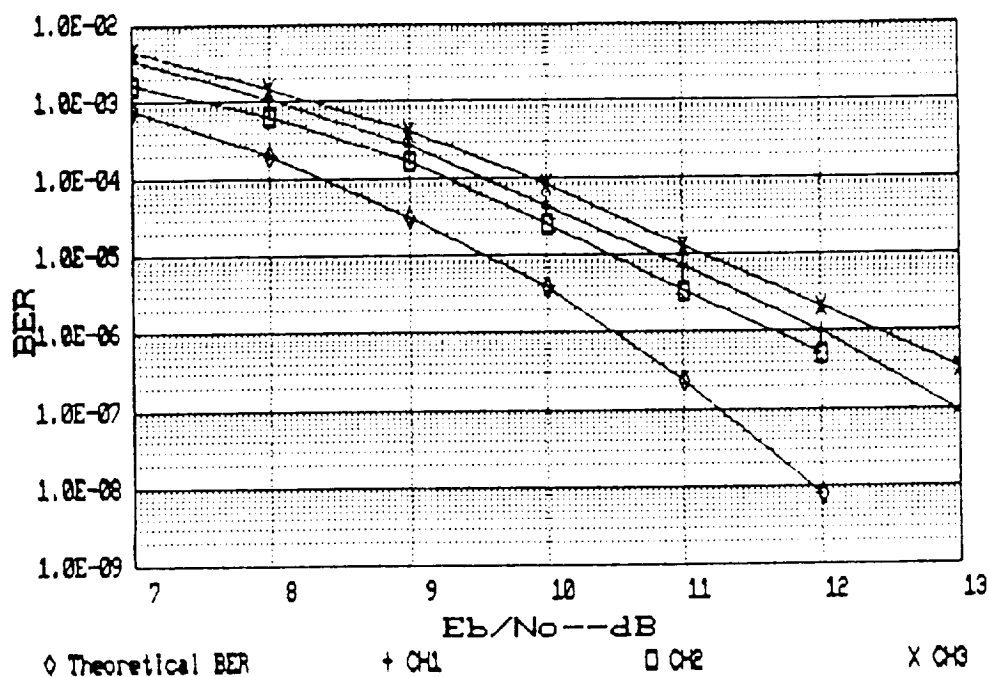

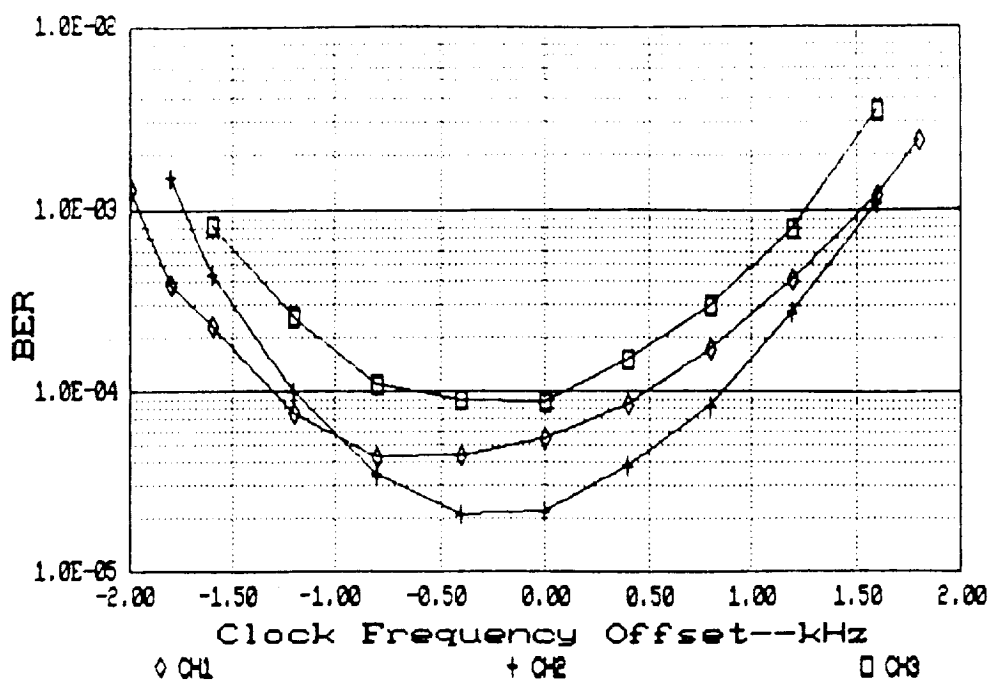FIGURE 7   BER FOR MCDD AT 4.4 MBIT/S

ROW 1, COLUMN 5

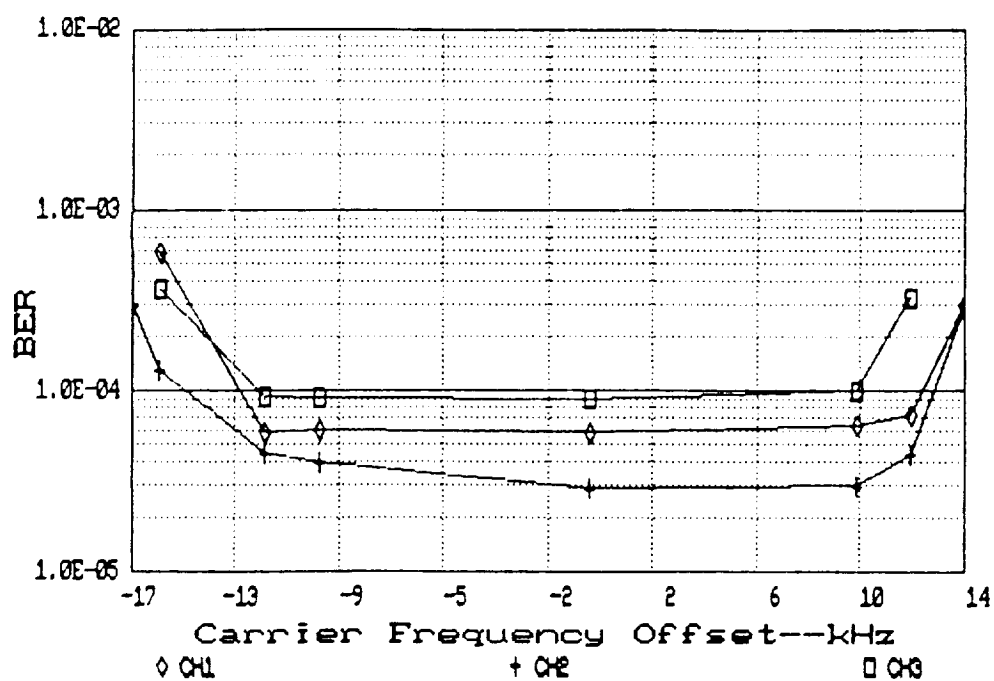FIGURE 8   BER FOR MCDD VERSUS CLOCK FREQUENCY OFFSET

FIGURE 9   BER FOR MCDD VERSUS CARRIER FREQUENCY OFFSET
ROW 2, COLUMN 4

TWO ADJACENT CHANNELS (UPPER AND LOWER) ARE THE INTERFERING CHANNELS.
TWO ADDITIONAL ALCATEL SYNTHESIZERS (1 AND 3) ARE USED TO PROVIDE TWO
SOURCE SIGNALS TO THE FDMA SIGNAL GENERATOR FOR THE UPPER AND LOWER
CHANNELS. ANOTHER HP3326A, HP3762A AND DIVIDER ARE USED TO PROVIDE THE
INTERFERING DATA SIGNALS AND CLOCKS TO MODULATE THE UPPER AND LOWER
CHANNEL CARRIERS. MEASUREMENTS ARE ONLY PERFORMED FOR THE CENTER
CHANNEL.

THE DEGRADATION DUE TO THE ACI INTERFERENCE IS NO MORE THAN 0.2 DB LOSS
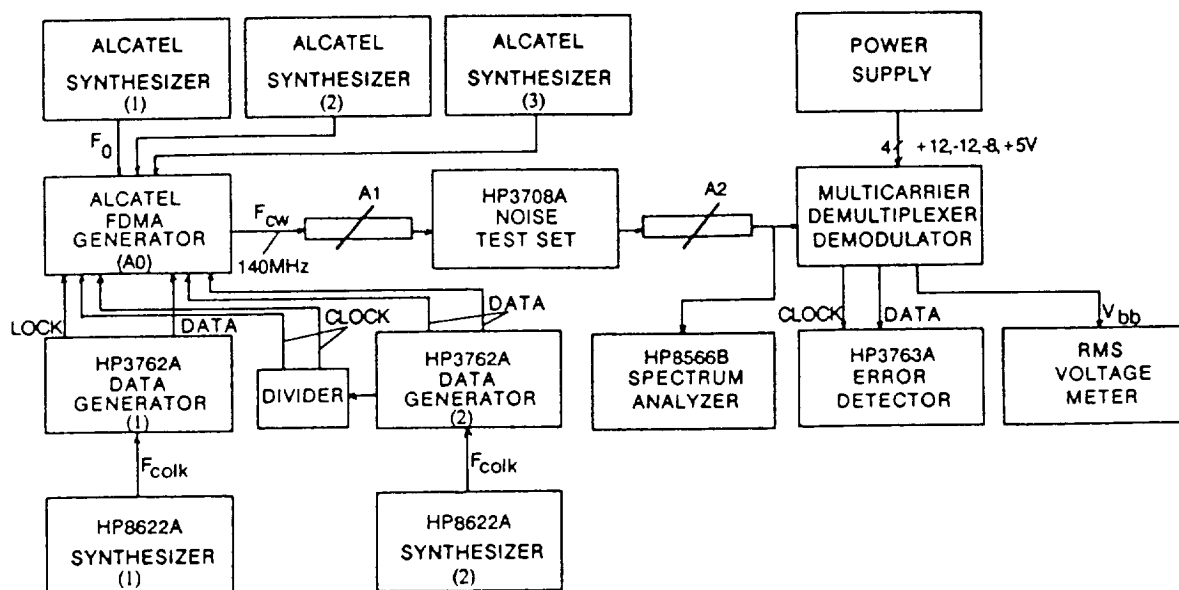FOR THE 4.4 MBIT/S DATA RATE CASE.

FIGURE 10   SETUP FOR THE ADJACENT CHANNEL INTERFERENCE TEST

ROW 2, COLUMN 5

THE PROOF-OF-CONCEPT HARDWARE FOR THE BBP CONSISTS OF 12 PRINTED WIRED
BOARDS: ONE TDM/TDMA CONVERTER, ONE TDMA/TDM CONVERTER, ONE FDMA
BUFFER, FIVE FOR THE SWITCH CIRCUITS, FOUR FOR THE CONTROL UNIT.

THE PRINCIPAL FUNCTIONS OF THE BBP CONSIST OF DATA RATE CHANGING;
TRAFFIC ROUTING AT BYTE LEVEL, INCLUDING MULTIPLEX (TDM-DOWN), MULTI-
CAST AND DISTRIBUTION ETC.; TDM/TDMA CONVERSION; AND DIAGNOSIS.

THE SWITCH CIRCUIT PERFORMS DATA RATE CHANGES AND ALL SWITCHING
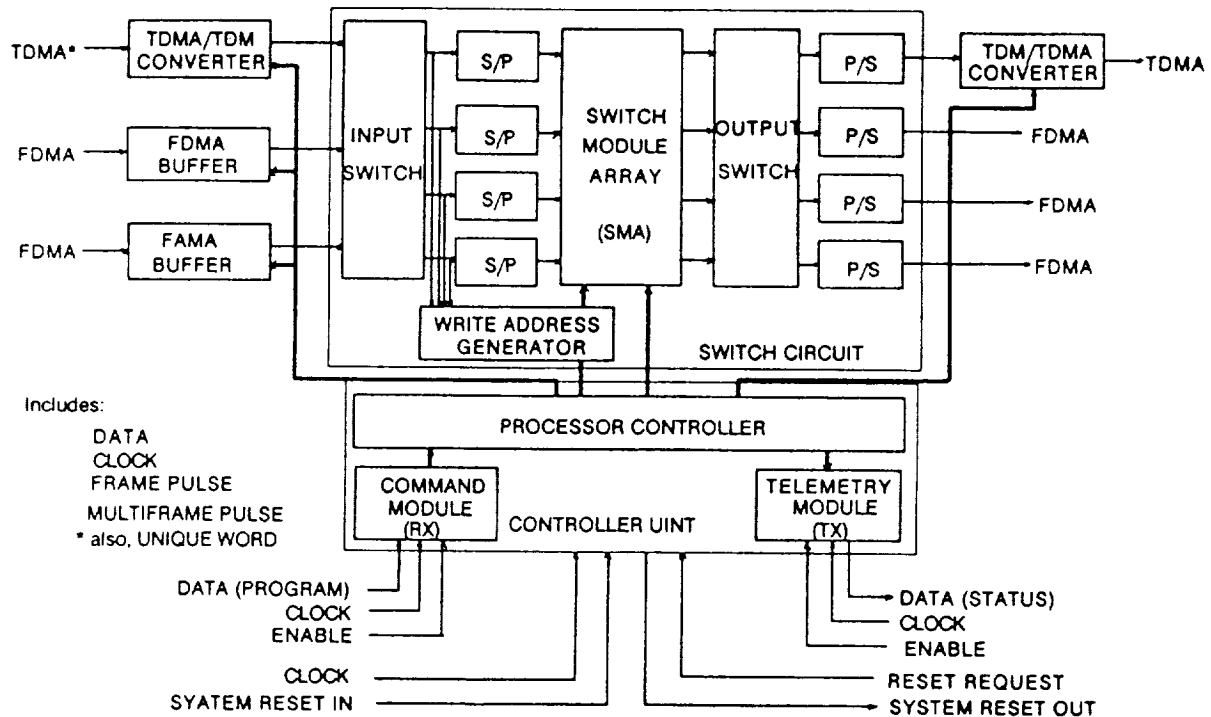FUNCTIONS.

FIGURE 11   BLOCK DIAGRAM FOR BASEBAND PROCESSOR (BBP)

THE BBP HARDWARE IS THE DEVICE UNDER TEST.   THE TEST SET GENERATES THE
INPUT SIGNALS FOR THE BBP AND RECEIVES THE OUTPUT SIGNALS FROM THE BBP.
THE DATA RATES OF THREE PN DATA ARE 8192, 2048 AND 68.3 KBIT/S
RESPECTIVELY.

THE TIMING SIGNAL GENERATOR (A) GENERATES THE MASTER CLOCK OF 16.384
MHz AND SYSTEM RESET SIGNAL AND OUTPUTS THEM TO THE BBP HARDWARE;
(B) GENERATES THREE CLOCKS (8192 kHz, 2048 kHz AND 68.3 kHz) AND SENDS
THEM TO THE PN DATA GENERATORS VIA THE MUX; (C) GENERATES SIX KINDS OF
FRAME AND MULTI-FRAME PULSES (PERIOD: 250 US, 2 MS, 7.5 MS, 16 MS AND
480 MS) WHOSE PULSE DURATIONS ARE 244 NS; AND (D) OUTPUTS THESE CLOCKS
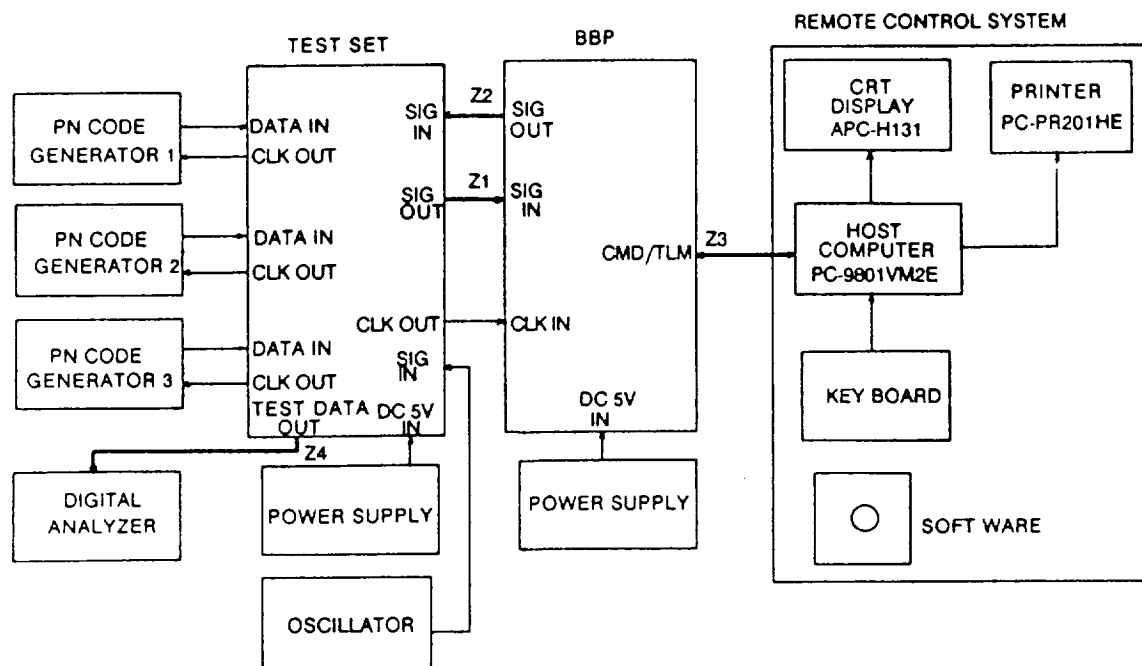AND PULSES TO THE MULTIPLEXER IN THE TEST SET.

FIGURE 12   TEST SETUP FOR THE BBP TESTS

THE MULTIPLEXER GENERATES THREE INPUT DATA STREAMS: TDMA DATA, 1920 KBIT/S TDM DATA AND 64 KBIT/S TDM DATA. THE MUX GENERATES THE UNIQUE WORD SIGNAL FOR EACH INPUT DATA STREAM. THE UNIQUE WORD SIGNALS INCLUDE PREAMBLE DATA AND REFERENCE BURST DATA IN TDMA DATA, MULTI-FRAME DATA INSERTED IN BYTES 0, 16, 32 AND 48 IN TDM DATA.

ANOTHER VERY IMPORTANT FUNCTION OF THE MULTIPLEXER IS INSERTING 8-BIT TEST DATA TO A CHANNEL IN AN INPUT LINE. THE 8-BIT DATA CAN BE ARBITRARILY SELECTED BY SETTING THE "8-BIT TEST DATA" SWITCHES ON THE FRONT PANEL OF THE TEST SET. THE LINE AND THE CHANNEL CAN BE SELECTED BY SETTING THE OUT LINE SEL AND OUT CHANNEL SEL DIGITAL SWITCHES ON THE FRONT PANEL OF THE TEST SET RESPECTIVELY. THE MULTIPLEXER INSERTS THE RECEIVED PN DATA INTO EVERY CHANNEL IN EACH OUTPUT LINES, EXCEPT THE CHANNEL INTO WHICH 8-BIT TEST PATTERN DATA ARE INSERTED.

THE DEMULTIPLEXER RECEIVES THE OUTPUT SIGNALS FROM THE BBP HARDWARE, AND SELECTS ONE FROM 4 OUTPUT LINES AND A CHANNEL IN THE SELECTED LINE TO DISPLAY. THE SELECTION IS PERFORMED BY SETTING THE IN LINE SEL AND IN CHANNEL SEL SWITCHES IN THE FRONT PANEL OF THE TEST SET RESPECTIVELY. THE DEMULTIPLEXER DISPLAYS THE SELECTED 8-BIT DATA BY "IN 8-BIT TEST DATA" LED DISPLAY ON THE FRONT PANEL OF THE TEST SET.

THE OTHER FUNCTION OF THE DEMULTIPLEXER IN THE TEST SET IS PERFORMING THE ERROR DETECTION FOR THE SELECTED 8-BIT DATA. THIS IS PERFORMED BY COMPARING THE 8-BIT OUTPUT DATA DETERMINED BY SETTING THE "8-BIT TEST DATA" SWITCH WITH THE 8-BIT INPUT DATA MONITORED ON THE LED DISPLAY. WHEN AN ERROR IS DETECTED, THE "ERROR" LED DISPLAY ON THE FRONT PANEL OF THE TEST SET TURNS ON AND AN ERROR PULSE IS GENERATED AND OUTPUT FROM THE "ERR PLS OUT" BNC CONNECTOR ON THE REAR PANEL OF THE TEST SET.

THE DEMULTIPLEXER ALSO PERFORMS THE SERIAL / PARALLEL CONVERSION OF THE SELECTED OUTPUT LINE DATA AND OUTPUTS THE PARALLEL DATA FROM THE Z4 (TEST DATA OUT) CONNECTOR ON THE REAR PANEL OF THE TEST SET.

THE REMOTE CONTROL OPERATION SYSTEM SIMULATES THE CONTROL FUNCTIONS OF THE CONTROL EARTH STATION IN A SATELLITE COMMUNICATION NETWORK. ITS MAIN FUNCTION ARE COMMAND SETTING, TELEMETRY DATA DISPLAY, AND TRANSMISSION/ RECEPTION CONTROLS.

IBS/IDR BBP TESTS INCLUDE:
    COMMUNICATION BETWEEN HOST COMPUTER AND THE BBP;
        (COMMAND AND TELEMETRY);
    DATA LOAD-UP AND READ-OUT;
    HARDWARE REDUNDANCY SWITCHING (CONTROL STATUS);
    SWITCHING FUNCTIONS:
        MULTI-CAST, TDM-DOWN, DISTRIBUTION, DATA RATE CHANGE;
    DIAGNOSTIC FUNCTIONS:
        COLUMN CONTROL MEMORY DIAGNOSIS
        AND SWITCHING MODULE MEMORY DIAGNOSIS.

THE IBS/IDR BBP PERFORMANCE MEETS THE FUNCTIONAL SPECIFICATIONS.

THE BASEBAND SWITCH MATRIX IS A 16x16 MATRIX WHICH CONSISTS OF 4 CHIPS REALIZED IN GaAs LSI TECHNOLOGY. THE CHIPS DEVELOPED UNDER CONTRACT INTEL-321 HAVE 16 INPUT CHANNELS AND 4 OUTPUT CHANNELS.

LOW POWER CONSUMPTION (7.78 W) IS ACHIEVED THROUGH THE CONSTRUCTION OF BUFFERED FET LOGIC WITH DEPLETION-TYPE FETs.

THE CHIPS ARE VERY SMALL AND HAVE LOW MASS. THE MASS OF THE DEMONSTRATION UNIT IS 1.25 KG AND IT HAS A SIZE OF 24x18x1.7 cm^3.

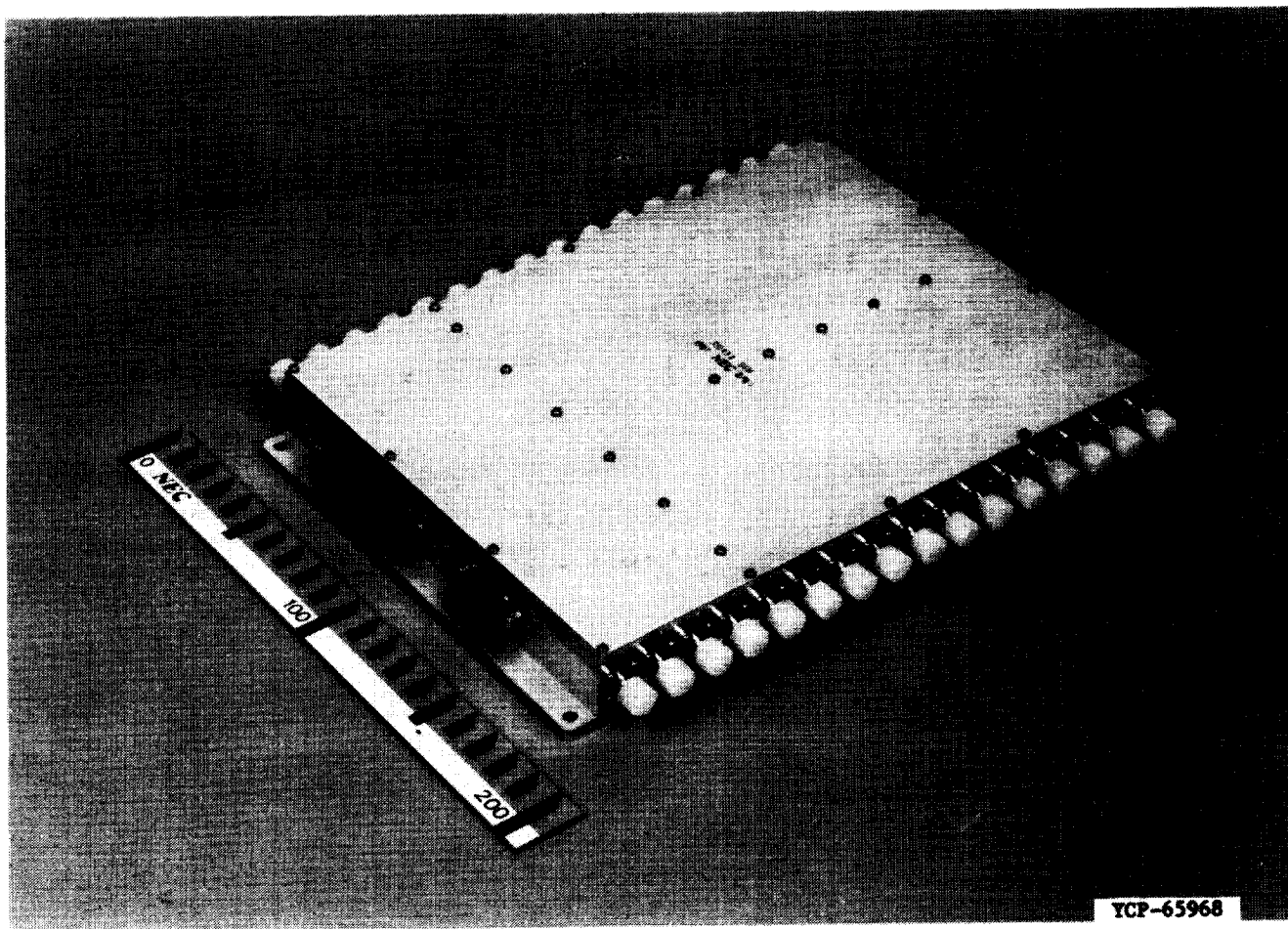EACH CHANNEL RUNS AT A 60-MHz CLOCK RATE; USED IN PAIRS, THEY SUPPORT 120-MBIT/S DATA RATE.

YCP-65968

FIGURE 13   PHOTOGRAPH OF BASEBAND SWITCH MATRIX

BSM TESTS   ROW 3, COLUMN 1   ++++

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THE BSM CHIP CONSISTS OF 4 FOUR-BIT REGISTER-1S, 4 FOUR-BIT REGISTER-2S, 4-TO-16 DECODERS AND 64 DIGITAL SWITCHES. REGISTER-1 STORES THE SWITCH ADDRESS COMING FROM THE DCU, AND LOADS REGISTER-2 UPON A DCU LATCH PULSE.

REGISTER-2 FEEDS THE 4-TO-16 DECODER WHICH SELECTS ONE SWITCH IN THE 16-GATE COLUMN. EACH SWITCH CONSISTS OF AN AND GATE MADE WITH DEPLETION-TYPE FET. THE AND GATES ARE ARRANGED ON THE CROSS POINTS OF THE MATRIX AND THE SIXTEEN AND-GATE OUTPUTS ARE INTERCONNECTED BY WIRED-OR TO THE OUTPUT LINE.

IN DYNAMIC OPERATION, THE DISTRIBUTION CONTROL UNIT (DCU) CAN UPDATE THE CONFIGURATION OF THE MATRIX UP TO 50 TIMES IN THE 2 MS FRAME. THROUGH THE TT&C INTERFACE, TRAFFIC FLOW PATTERNS ARE STORED IN THE OFF-LINE MEMORY OF THE DCU. AT THE BEGINNING OF THE MASTER FRAME PULSE (8129x2 MS = 16 SEC), THE NEW PATTERN (MAXIMUM 50 CONFIGURATIONS) IS PLACED IN SERVICE IN THE ON-LINE MEMORY OF THE DCU.

BSM TESTS   ROW 4, COLUMN 1   ++++
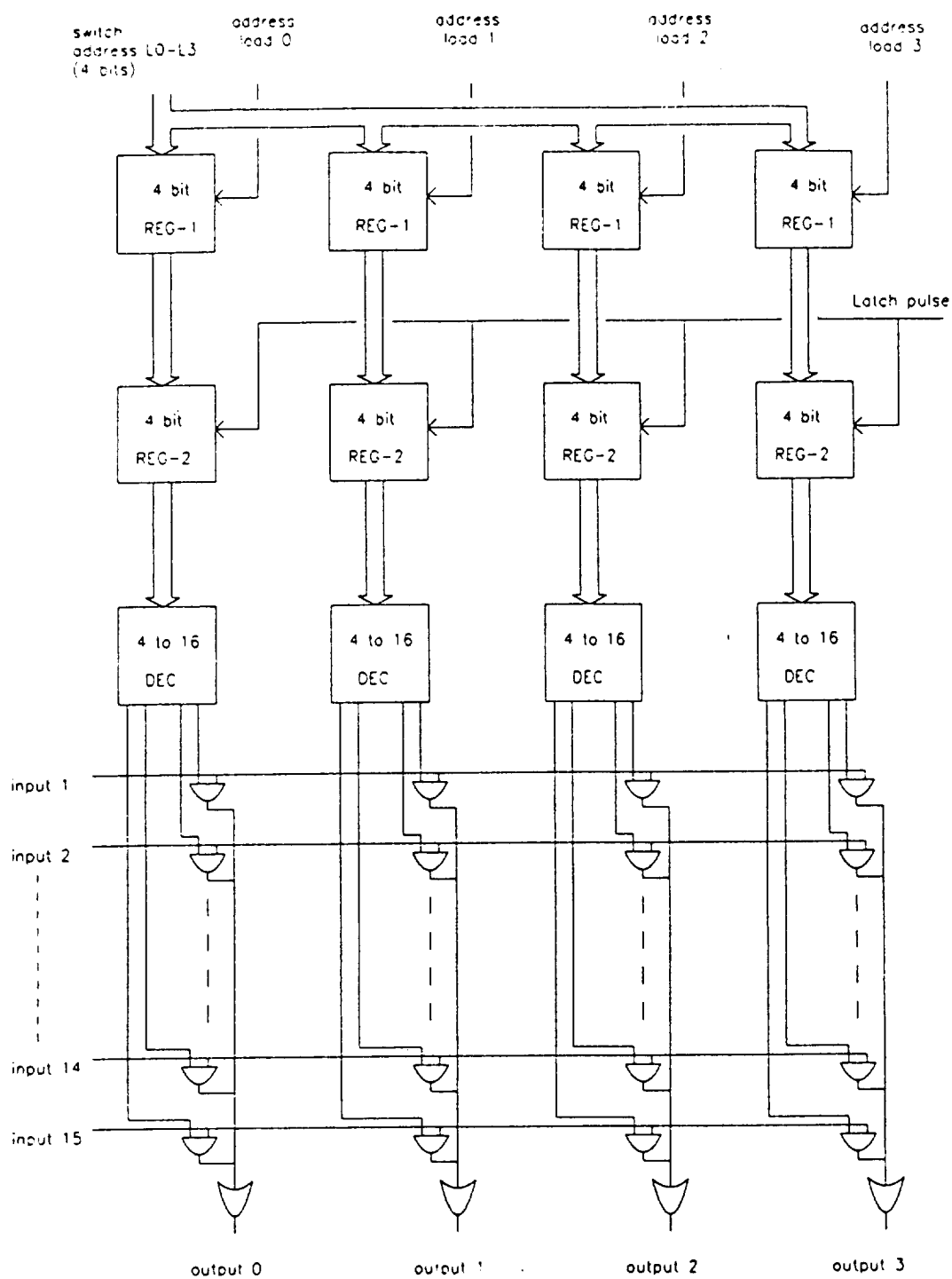
FIGURE 14   GaAs LSI BSM Chip Block Diagram

BSM TESTS   ROW 4, COLUMN 2   ++++

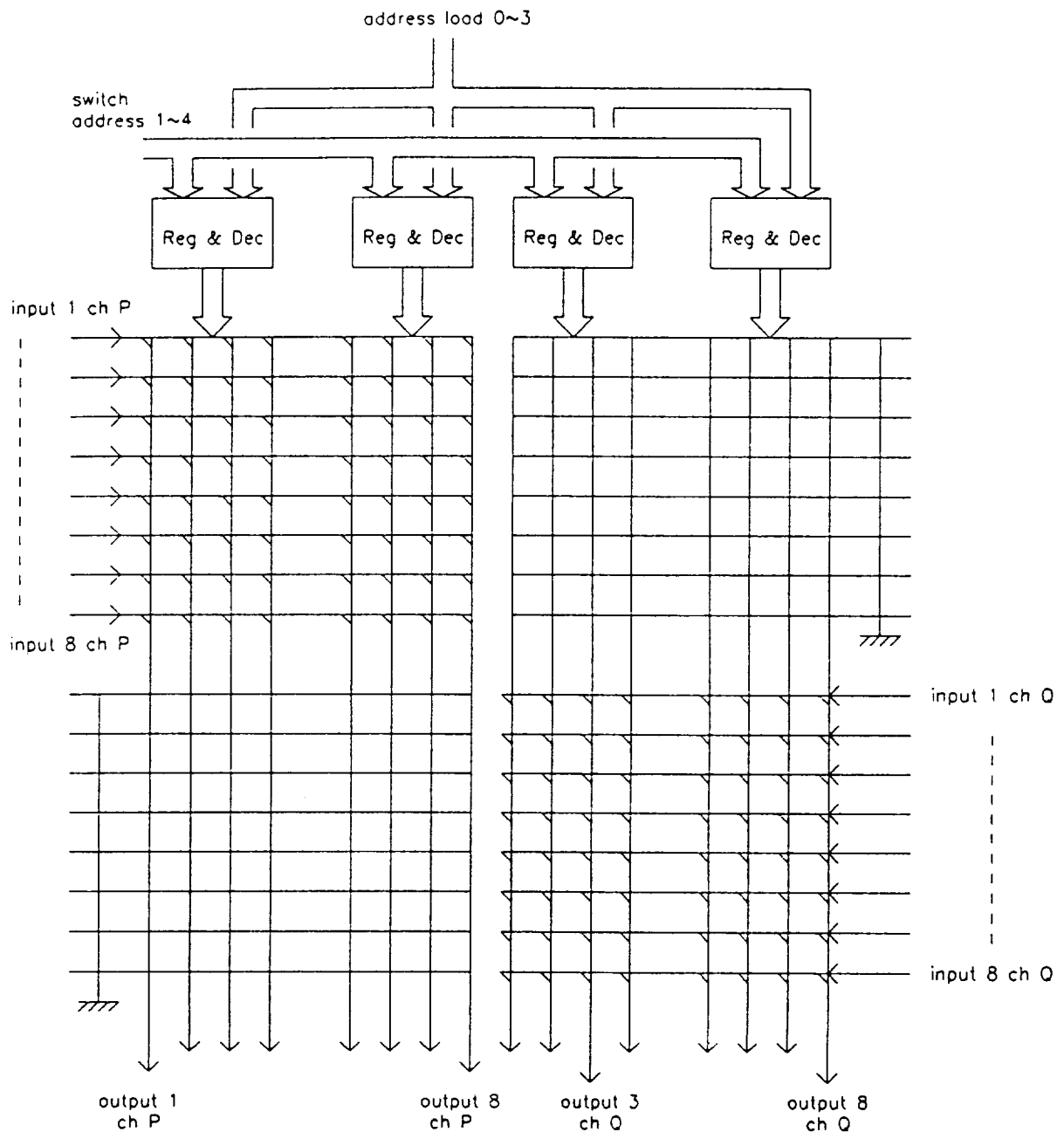FIGURE 15   BSM TEST IMPLEMENTATION: TWO 8 x 8 MATRICES

IN THE TEST CONFIGURATION, THE BSM SIMULTANEOUSLY CONNECTS DYNAMICALLY
AND STATICALLY TWO SETS OF 8 INPUT PORTS TO 8 OUTPUT PORTS FOR P AND Q
CHANNELS, UNDER THE CONTROL OF THE DISTRIBUTION CONTROL UNIT.
[THIS IMPLEMENTATION USES HALF THE SURFACES OF THE CHIPS.]

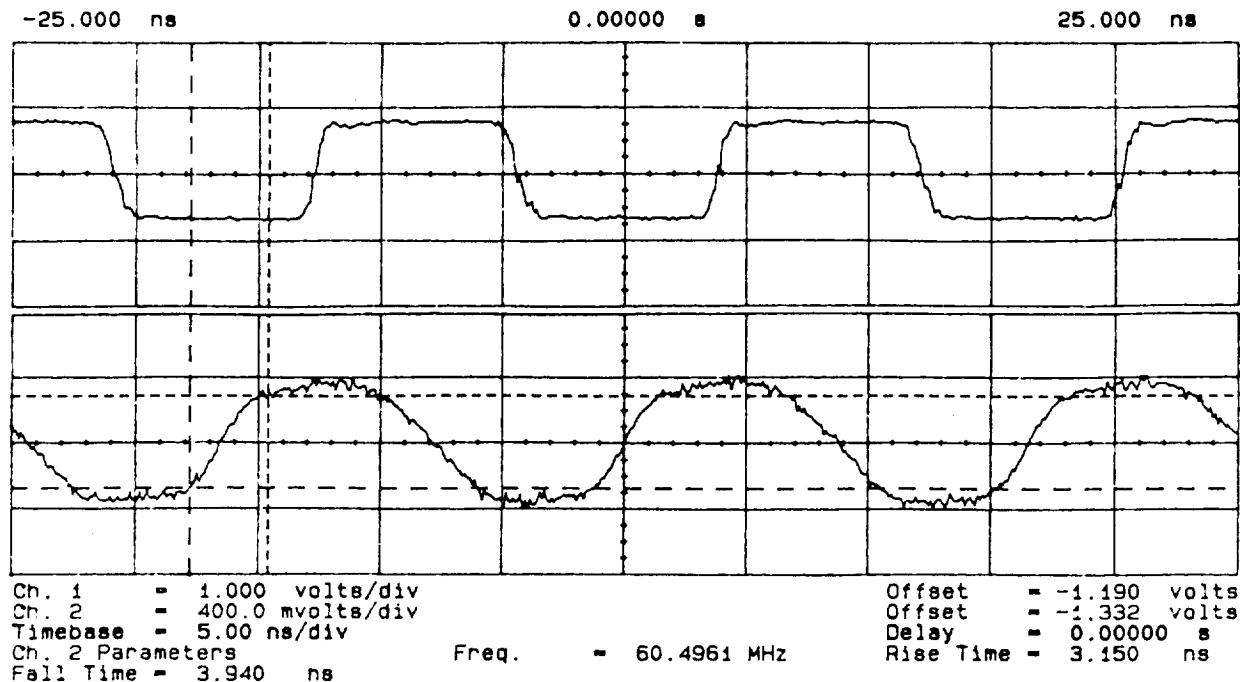BSM TESTS   ROW 3, COLUMN 2   ++++

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Ch. 1      =  1.000  volts/div              Offset   = -1.190  volts
Ch. 2      =  400.0 mvolts/div              Offset   = -1.332  volts
Timebase   =  5.00 ns/div                   Delay    =  0.00000  s
Ch. 2 Parameters            Freq.   =  60.4961 MHz   Rise Time = 3.150  ns
Fall Time  =  3.940  ns
```

FIGURE 16   INPUT AND OUTPUT WAVEFORMS

THE OUTPUT AND INPUT LEVELS ARE ECL COMPATIBLE.
ALL THE SWITCHES FUNCTION AS REQUIRED.

WITH A RANDOM SEQUENCE (LENGTH = 2^{15} - 1) AS INPUT AND AN ERROR DETECTOR AS A MONITOR, A TEST HAS CONFIRMED THAT THE WORKING SPEED IS THE 60-MHz CLOCK RATE, AS REQUIRED IN QPSK 120-MBIT/S TDMA SYSTEMS. SOME SWITCHES WORK UP TO 90 MSYMBOL/S.

WHEN THE BSM OPERATES AT 60 MHz, SOME PRECAUTIONS IN THE RISE TIME AND THE FALL TIME MEASUREMENTS ARE REQUIRED. TO AVOID LINE REFLECTIONS, WE ADDED AN ECL GATE WHICH TERMINATES ON A 50-OHM RESISTOR.

BSM TESTS   ROW 4, COLUMN 3   ++++
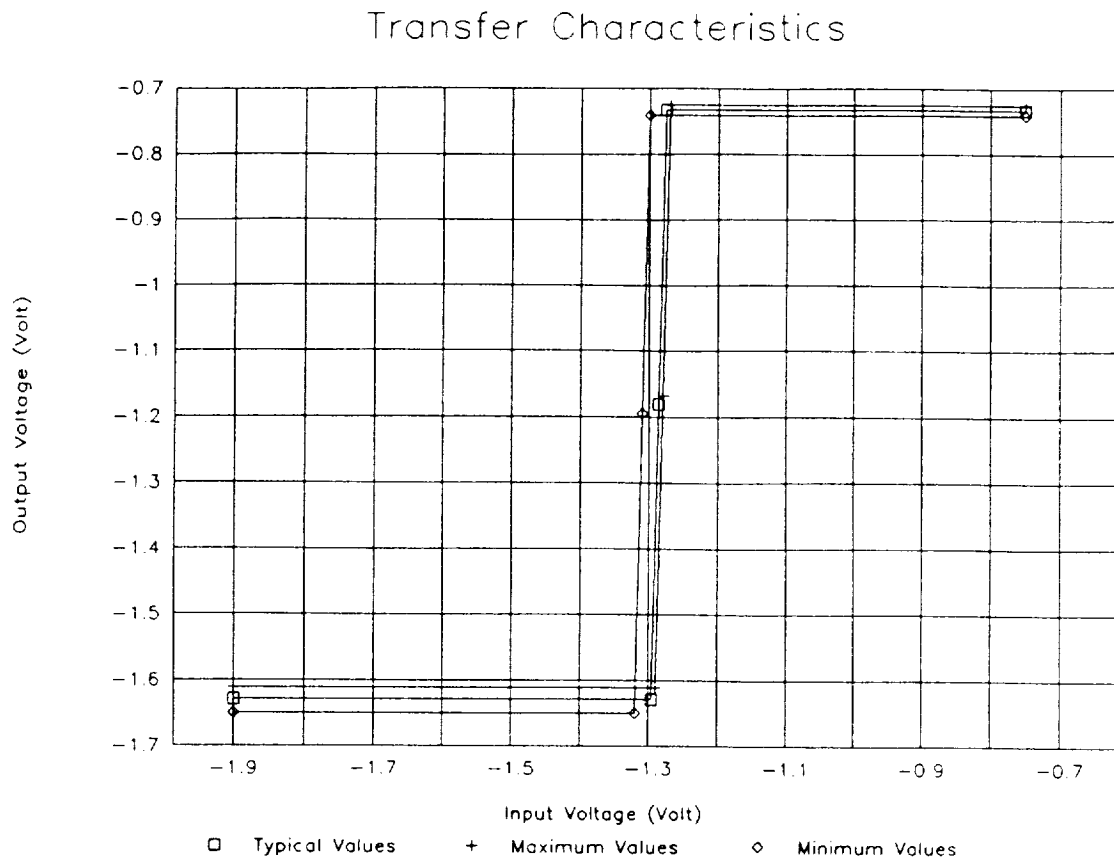
Transfer Characteristics

FIGURE 17   BSM: V_{out} VERSUS V_{in}

THE FIGURE SHOWS A COMPOSITE OF OBSERVED INPUT / OUTPUT CHARACTERISTICS FOR MANY BSM GATES.

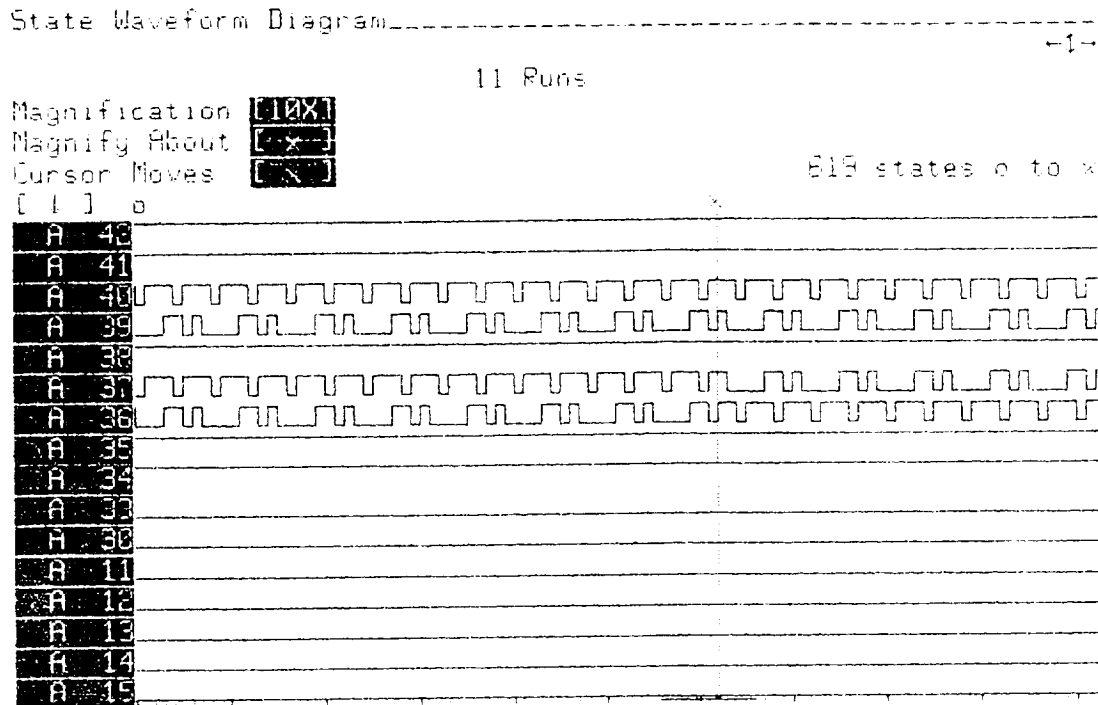THE INPUT / OUTPUT TRANSFER CHARACTERISTICS FOR ALL GATES ARE ACCEPTABLE.

BSM TESTS   ROW 4, COLUMN 4   ++++

State Waveform Diagram_____
                                                                    ←1→
                              11 Runs

Magnification [10X]
Magnify About [_x_]
Cursor Moves   [_x_]   619 states o to x
[|] o

| A 43 |
| A 41 |
| A 40 |
| A 39 | Inputs
| A 38 |
| A 37 | Outputs
| A 36 |
| A 35 |
| A 34 |
| A 33 |
| A 30 |
| A 11 |
| A 12 |
| A 13 |
| A 14 |
| A 15 |

FIGURE 18   DYNAMIC TEST OF THE BSM

THE FIGURE ILLUSTRATES THAT THE DATA STREAMS ARE SWAPPED
FROM P CHANNEL 1 TO P CHANNEL 8.

THIS DYNAMIC TEST SHOWED THAT THERE ARE NO BIT LOSSES
DURING THE SWITCHING OPERATION.

REFERENCE

1.   P.P. NUSPL AND G. DONG, "ON-BOARD PROCESSING FOR
     TELECOMMUNICATIONS SATELLITES", TO BE PRESENTED AT SECOND NASA
     SPACE COMMUNICATIONS TECHNOLOGY CONFERENCE, ONBOARD SWITCHING AND
     PROCESSING, CLEVELAND, NOVEMBER 1991.

BSM TESTS   ROW 4, COLUMN 5   ++++