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ON-BOARD PROCESSING FOR TELECOMMUNICATIONS SATELLITES

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SUMMARY

In this decade, communications satellite systems will probably face dramatic challenges from alternative transmission means. To balance and overcome such competition, and to prepare for new requirements, INTELSAT has developed several on-board processing techniques, including Satellite-Switched TDMA (SS-TDMA), Satellite-Switched FDMA (SS-FDMA), several Modulators / Demodulators (Modem), a Multicarrier Multiplexer and Demodulator (MCDD), an IBS / IDR BaseBand Processor (BBP), etc. Some proof-of-concept hardware and software were developed, and tested recently in the INTELSAT Technical Laboratories. This paper presents these techniques and shows some test results.

INTRODUCTION

Communications satellites will probably face dramatic competition with alternative (terrestrial/undersea) transmission means. More sophisticated and flexible user-oriented satellite system architectures are being studied and developed to minimize the overall system cost (space and ground segment), and to meet the requirements for low-cost, smaller earth terminals to directly access satellites at low-to-moderate data rates. Reconfigurability and adaptability to different traffic scenarios are also important. Shorter terrestrial tails are needed in many services. Such requirements result in putting as many features as possible into the satellite payloads, and implementing some suitable access / modulation / coding schemes to improve link budgets.

On-Board Processing (OBP) systems, in the form of significant conditioning of traffic signals, are appropriate solutions to these problems, since OBP increases the flexibility of resource utilization and improves link performance [Ref. 1]. OBP offers alternatives to the approach of merely increasing the transmitted power and G/T of receivers. Under its R&D Programs, INTELSAT has developed several on-board processing techniques, including SS-TDMA (operational, and an advanced form), SS-FDMA, Modems, MCDD, IBS/IDR BBP and other items. [IBS is the International Business Service and IDR stands for Intermediate Data Rate, INTELSAT's range of public switched telephony services.] SS-TDMA and IBS/IDR BBP improve the connectivity and flexibility of these services; the Modems and MCDD improve the link performance. Some of these are good for both performance and connectivity improvements. There are some which are simpler and low-risk technologies, and can be specified in the near future. For others, there are some technical problems and system issues which should be resolved before the technologies can be used on-board. Some of

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these are suitable for use with transparent transponders but most are in the regenerative class.

Proof-of-concept hardware and software were developed under contracts, and tested recently in the INTELSAT Technical Laboratories. This paper describes these techniques and shows some test results.

OBP FOR TRANSPARENT PAYLOADS

OBP with transparent payloads mainly includes SS-TDMA, where 4-GHz signals with 72-MHz bandwidths are routed from beam to beam, and SS-FDMA, where smaller channels are formed, routed and reformatted. Since regeneration is avoided, these systems are simple and have less risk for on-board application in the near future. The benefits are better performance and higher connectivity.

Satellite-Switched TDMA

In Satellite-Switched TDMA (SS-TDMA), the uplink signals from the satellite receiving beams are demultiplexed in typically 80-MHz bands at RF and sent to the SS-TDMA Switch Matrix which maps the input signals to output beams dynamically. Since the HPA handles only one signal, capacity can be used more efficiently than in multicarrier FDMA.

The Microwave Switch Matrix (MSM) of the INTELSAT VI communication subsystem is an example of SS-TDMA applications [Ref. 2]. This MSM is capable of routing individual bursts of traffic between various satellite beam inputs and outputs. There are actually three functional units associated with the operation of the MSM: the microwave switches, the distribution control unit (DCU), and the timing source. The basic interconnections among the three units are shown in Figure 1.

The MSM payload on INTELSAT VI satellites is a solid state unit which takes advantage of MIC fabrication technology. This MSM has 10 input lines and 6 output lines. The 10 input lines are preceded by a ring-redundancy network which is made up of coaxial R switches. With central symmetry and flexible routing of the input ports through the network, there is minimal signal leakage. Only 6 of the 10 input lines to the matrix are active at any time. The matrix uses a bi-planar coupled crossbar configuration to achieve maximum interconnectivity. The MSM Switching Junction is shown in Figure 2. The input and the output planes are connected through quarter-wave 10-dB directional couplers and PIN diode attenuators. The directional couplers, while increasing the matrix insertion loss, reduce the VSWR and provide good isolation between interconnection points. The PIN diode attenuators act as the RF switching elements. The input preamplifiers, with 16 dB gain, are used to overcome the additional insertion loss caused by the directional couplers. The DCU provides dynamic controls for the MSM. Switch configuration information, called burst time plans, can be up-linked and stored in three DCU memories. The Timing Source provides all the timing signals for the DCU and the switch matrix.

An Advanced Satellite Switching Center has also been developed under R&D contract with NEC (Japan), some years ago [Ref. 3]. It has the same three functional units: MSM array, DCU and Timing Source. A major improvement consists of a redundant design with two 6 x 4 planes passively combined, and replicated again, to achieve an 8 x 8 matrix which has no single-point failure mode. The most significant innovation is the use of dual-gate FET switch modules, which in fact provide very stable and consistent gains (instead of losses). The MSM topology uses directional couplers with optimal ratios to achieve the

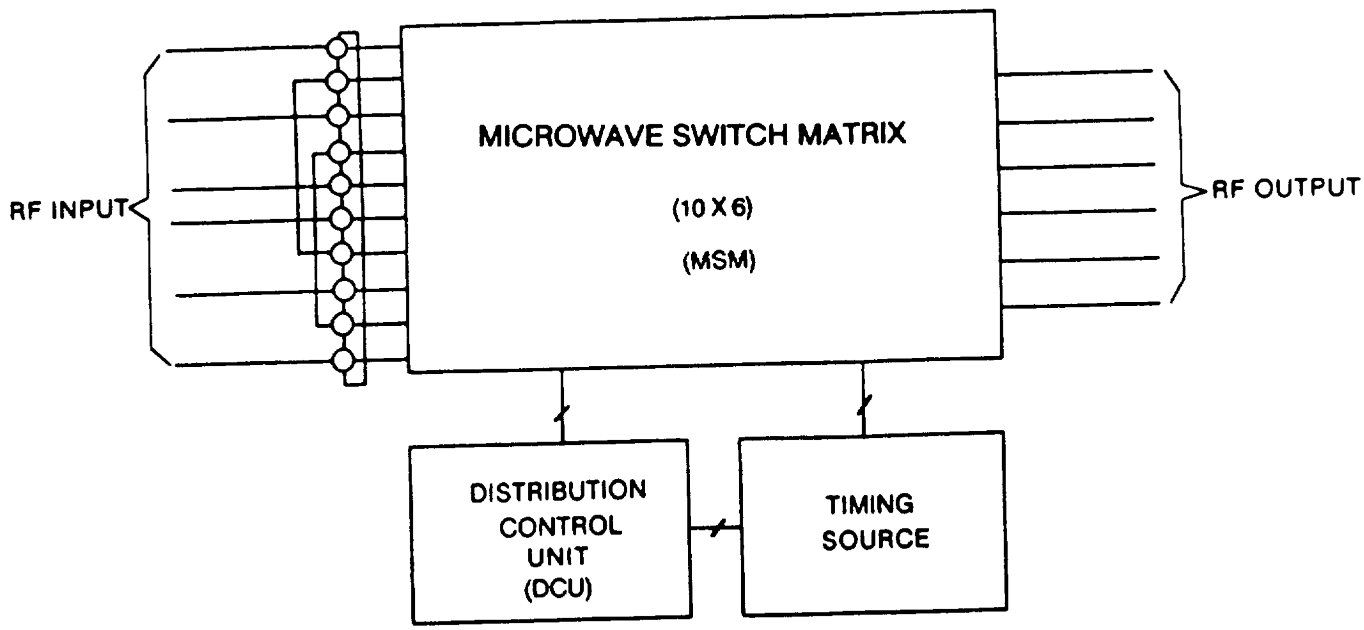

Figure 1 Interconnections among MSM, DCU and Timing Source

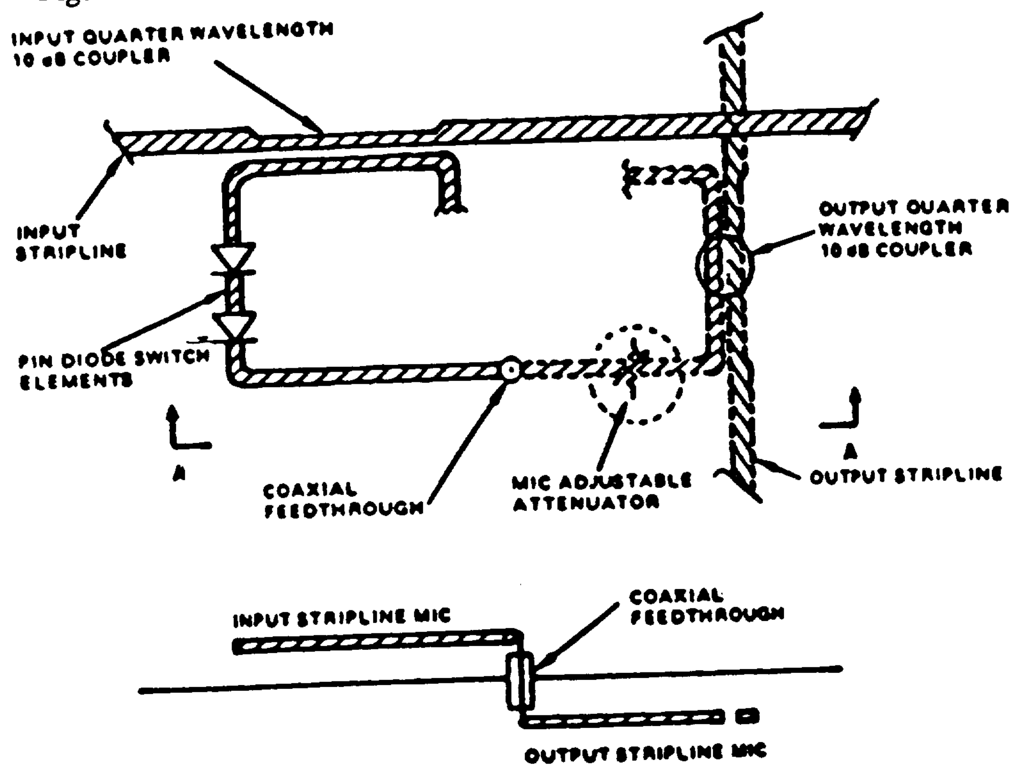

Figure 2 MSM Switching Function Detail

lowest insertion loss.

In a more recent advancement, on-board non-interfering diagnostics have been added, so that appropriate operations and status of the array can be made known to the ground control station. Details have been reported previously [Ref. 4].

Satellite-Switched FDMA

SS-FDMA is an alternative means in the frequency domain to enhance connectivity for FDMA services. In the existing transponder structure, the input demultiplexing and output multiplexing are performed on the transponder channels, i.e., the transponder bandwidths are taken as the elementary minimum bandwidths. With the SS-FDMA concept, the signals in a transponder bandwidth are further demultiplexed into a number of narrower subbands, some of which are multiplexed before the on-board HPA's in a "one-HPA-for-many-duplexed-channels" scheme.

An SS-FDMA package consists of demultiplexers, a static switch array, and multiplexers. A demultiplexer can be a bank of filters with variable bandwiths and variable center frequencies (VBVCF). A switch array consists of the single-pole-multiple-throw (SPMT) switches and crossbar switch matrices; it maps the inputs from the demultiplexer to its outputs. To have a reasonable number of HPAs, a frequency multiplexer combines several subchannels.

Under R&D contract to KDD (Japan), INTELSAT has developed an SS-FDMA technology demonstrator in the form of a VBVCF diplexer (2-channel multiplexer) which utilizes lithium tantalate ($LiTaO_3$) SAW filter technologies and Gallium Arsenide (GaAs) switch technologies [Ref. 5]. Figure 3 shows the layout of this unit. Its main parameters and characteristics are listed in Table 1.

With SS-FDMA processing, the connectivity between the input and output ports is achieved for the narrower subbands in the FDMA services. With this feature, the uplink FDMA signals of mixed high- and low-power densities can be separated before going into the HPA. The performance for the low-power density carriers is improved and the HPA power is used efficiently, with less backoff.

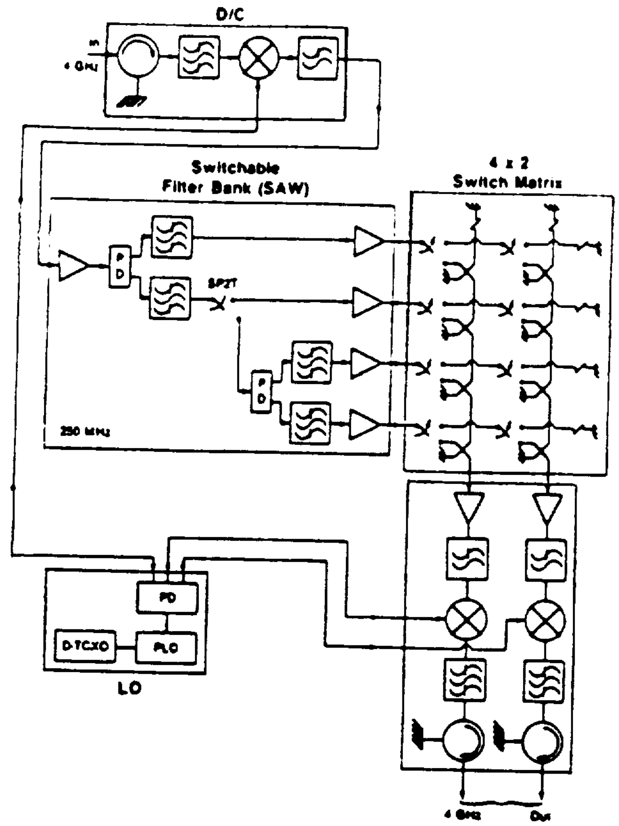

Figure 3 INTELSAT SS-FDMA Demonstrator

OBP FOR REGENERATIVE PAYLOADS

On-Board Processing for regenerative payloads includes demodulation, baseband switching, and remodulation. On-board demodulation / modulation improve the link performance and isolate the downlink from the uplink. Baseband switching provides better connectivity and a high degree of flexibility. Demodulation for the IDR and TDMA services and the MCDD for IBS and IDR services are discussed below.

In transparent transponders, the uplink noise and interference in the receiver is amplified and retransmitted in the downlink. At the E/S receiver the total noise is the summation of the downlink noise and interference, and the retransmitted uplink noise. The system BER performance is determined by the total $E_b/N_o)_t$.

$$\frac{1}{\left.\frac{E_b}{N_o}\right)_t} = \frac{1}{\left.\frac{E_b}{N_o}\right)_{up}} + \frac{1}{\left.\frac{E_b}{N_o}\right)_{dn}} \qquad Eq.\ 1$$

For the given BER performance, say $1\text{x}10^{-6}$, the relation between the uplink $E_b/N_o)_{up}$, and downlink $E_b/N_o)_{dn}$ is shown in Figure 4. The curve without regeneration varies slowly with both $E_b/N_o)_{up}$ and $E_b/N_o)_{dn}$, and for a large range the total noise is sensitive to both uplink noise and downlink noise, in this non-regenerative case.

In regenerative systems, the uplink data is demodulated on-board the satellite and modulated on the downlink carrier. From the standpoint of BER performance analysis, all regenerative links may be regarded as a pair of Binary-Symmetric-Channels (BSCs) in cascade. Figure 5 (A) illustrates this schematically, where P_{bu} and P_{bd} denote the information-BERs of the uplink and downlink BSCs, respectively. It is relatively easy to show that the cascaded BSCs reduce to an equivalent BSC (see Figure 5 (B)) whose information-BER P_b is given by:

$$\begin{aligned} P_b &= (1-P_{bu})P_{bd} + P_{bu}(1-P_{bd}) \qquad Eq.\ 2 \\ &= P_{bu} + P_{bd} - 2P_{bu}P_{bd} \end{aligned}$$

For most practical cases, both P_{bu} and P_{bd} are much less than 1, and $2P_{bu}P_{bd}$ is much less than P_{bu} or P_{bd}, and the above equation is well approximated by Equation 3:

$$P_b = P_{bu} + P_{bd} \qquad Eq.\ 3$$

The total BER is a summation of uplink BER and the downlink BER. For the given BER of $1\text{x}10^{-6}$, the relation between the $E_b/N_o)_{up}$ and $E_b/N_o)_{dn}$ is also shown with regeneration in Figure 4 for comparison. It is clear from the figure that the curve is very steep with changes of $E_b/N_o)_{up}$ and $E_b/N_o)_{dn}$. The curve is mainly determined by $E_b/N_o)_{up}$ (uplink limited) or $E_b/N_o)_{dn}$ (downlink limited). Only in a very small range is the system BER determined by $E_b/N_o)_{up}$ and $E_b/N_o)_{dn}$ together, but this is the best operating range. OBP allows operation with reduced $E_b/N_o)_{dn}$ and much lower $E_b/N_o)_{up}$.

TDMA Modem

Under an R&D contract to MELCO (Japan), INTELSAT has developed an On-Board Modem for TDMA operation at 120 Mbit/s [Ref. 6], and it was tested recently in the INTELSAT Technical Labs. The On-Board Modem contains a Demodulator and Modulator for burst-mode QPSK 60 Msymbol/s signals.

The Demodulator diagram is shown in Figure 6 (A). The demodulation circuit is a coherent detector. The carrier recovery circuit consists of a times-four multiplier, a tank-limiter with AFC (Automatic Frequency Control) and a divided-by-four circuit. The symbol-timing-recovery (STR) circuit consists of the IF squaring circuit and tank-limiters. The burst 3950 MHz RF signal is fed to the RF channel which includes the downconverter, the IF roll-off filter and the AGC circuit. The RF chain converts the RF signal frequency from 3950 MHz to an IF of 141.1 MHz. The output IF signal is divided into two parts; one is fed to the demodulation circuit and the other is fed to the multiplier in the STR circuit. The frequency multiplier generates times-four and times-two signals, and parallel filters extract the components of the carrier and symbol timing

Table 1 Performance of Diplexer

PARAMETERS		CHARACTERISTICS
1-dB Bandwidth	B1	≥ 35 MHz
Center Frequencies	f1	232 MHz
	f2	268 MHz
Guard Band	BG1	≤ 1 MHz
Transition Bandwidth (1 to 30 dB)	F1	≤ 1 MHz
1-dB Bandwidth	B2	≥ 17 MHz
Center Frequencies	f3	259 MHz
	f4	277 MHz
Guard Band	BG2	≤ 1 MHz
Transition Bandwidth (1 to 30 dB)	F2	≤ 1 MHz
Minimum Insertion Loss		1.5 dB
Insertion Loss Variation (Channel to Channel)		≤ 0.7 dB
Out-of-Band Attenuation		> 30 dB
Group Delay Variation		< 10% of Minimum Group Delay
Amplitude Ripple		1 dB p-p
Phase Ripple		≤ 6 ° p-p
Input VSWR		≤ 1.3
Output VSWR		≤ 1.3

signals. The frequency variation of the IF signal is tracked by an AFC circuit in the carrier recovery circuit. The recovered carrier is used as a reference frequency signal for coherent detection in the demodulator. Demodulated P and Q signals go to the regeneration circuit where each of them is converted to a digital signal.

The Modulator is shown in Figure 6 (B). The P and Q streams and their clock of 60.416 MHz (data rate is 120.832 Mbit/s) are received by the retiming circuit. P and Q streams are synchronized by the Clock. The P and Q bit streams from the retiming circuit go to the QPSK modulator. The carrier signal of 141.1 MHz comes from the Test Set through a switch and bandpass filter. This switch is

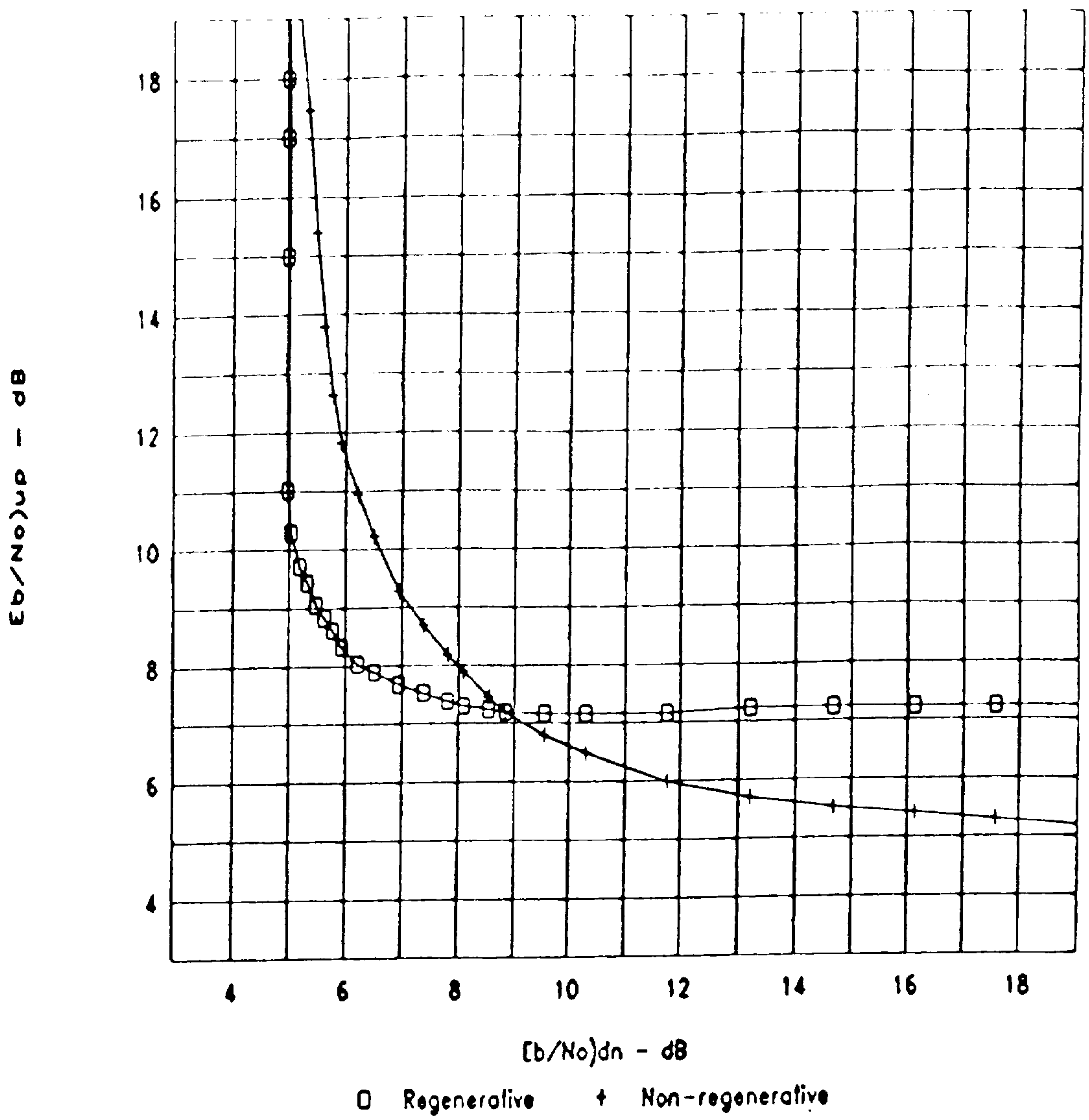

Figure 4 Uplink to Downlink Relationship
(No OB Modem, BER = 10^{-6}, calculated)

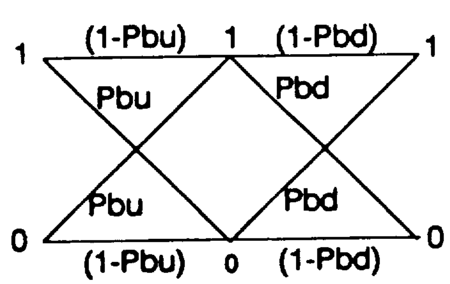

Figure 5 (A) Uplink BSC and Downlink BSC in Cascade

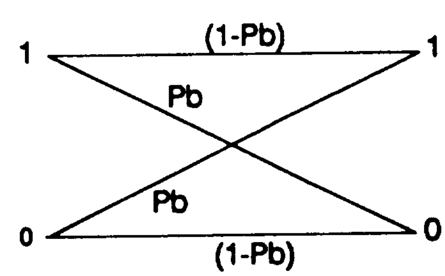

Figure 5 (B) Equivalent BSC of Regenerative Link

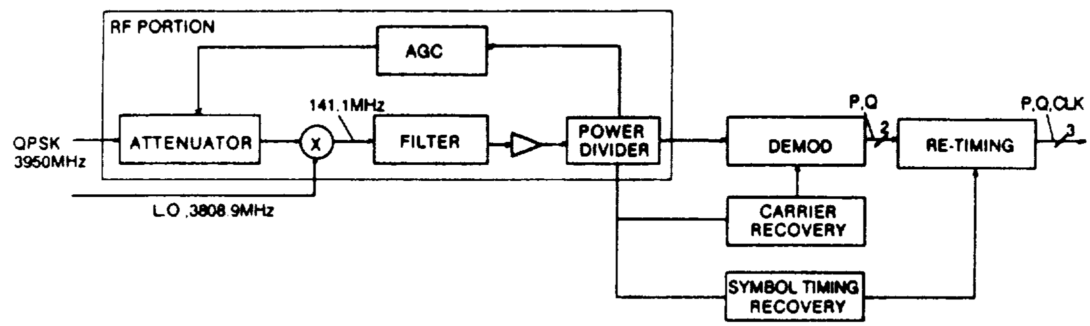

Figure 6 (A) On-Board Demodulator

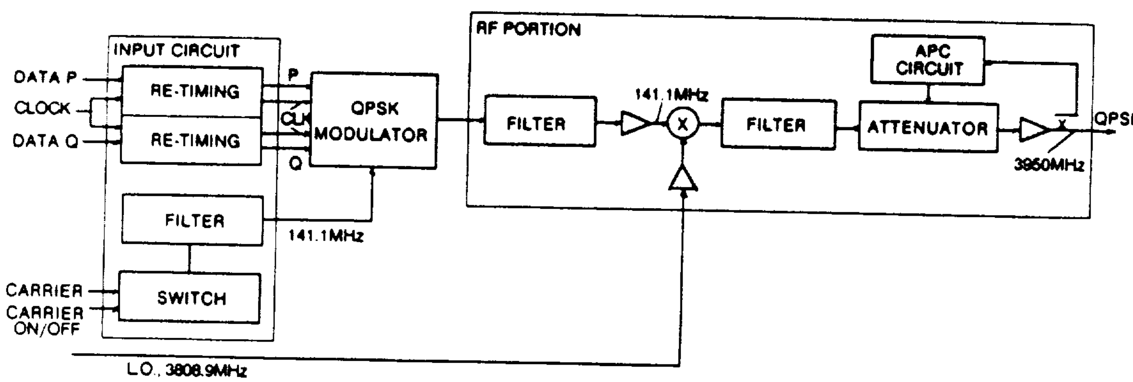

Figure 6 (B) On-Board Modulator

controlled by the carrier on-off signal from the Test Set and it controls the output of the modulator. The modulated signal from the QPSK modulator passes through the IF filter, amplifier and upconverter in which it is converted into an RF signal at 3950 MHz. The LO signal of the Converter which comes from the Test Set is 3808.9 MHz. The RF signal is filtered, amplified and output.

The main items of the TDMA Modem performance were also tested recently at INTELSAT H.Q. and included: Bit Error Ratio (BER) versus E_b/N_o, BER versus carrier frequency offset, BER versus Local Oscillator (LO) frequency offset, BER versus clock frequency offset, BER versus input signal level variation, carrier phase and amplitude variations and on/off isolation. The E_b/N_o relationship between uplink and downlink for the On-Board Modem for the given BER was also determined.

Figure 7 shows the uplink BER versus E_b/N_o curves of the test results. The specification BER curve is also printed in the figure for performance comparison. The uplink BER performance indicates mainly the On-Board Demodulator performance. The BER versus E_b/N_o results in burst mode and continuous mode are similar. Compared to its specifications the E_b/N_o needs to increase 2.1 to 4.7 dB. The degradation reduces to the range 0.7 to 1.6 dB when the LO frequency offset is at about -125 kHz or the carrier frequency offset is +125 kHz.

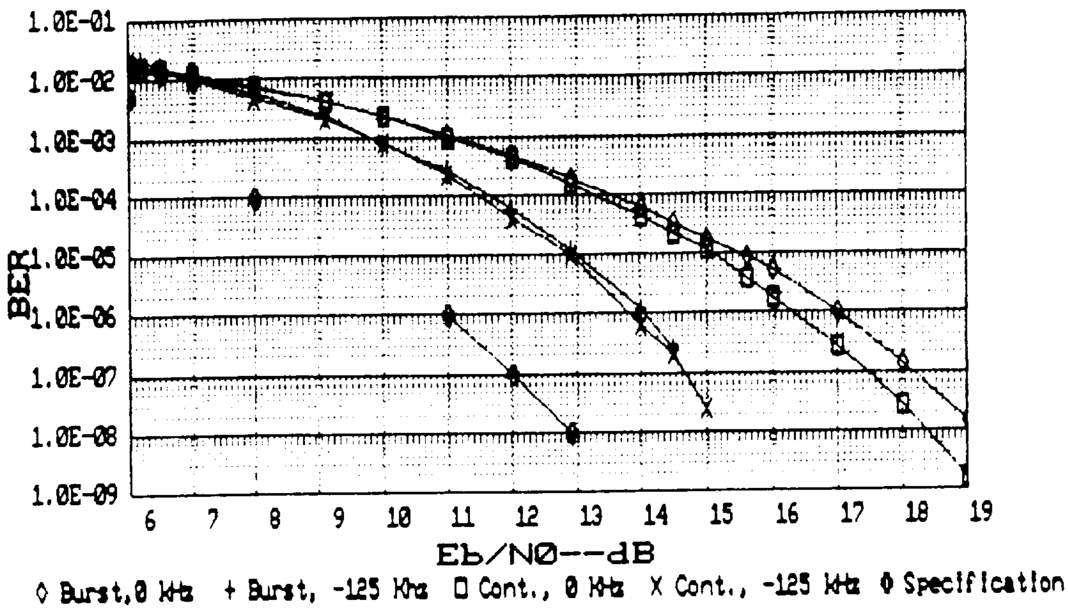

Figure 7 Uplink MODEM BER vs E_b/N_o

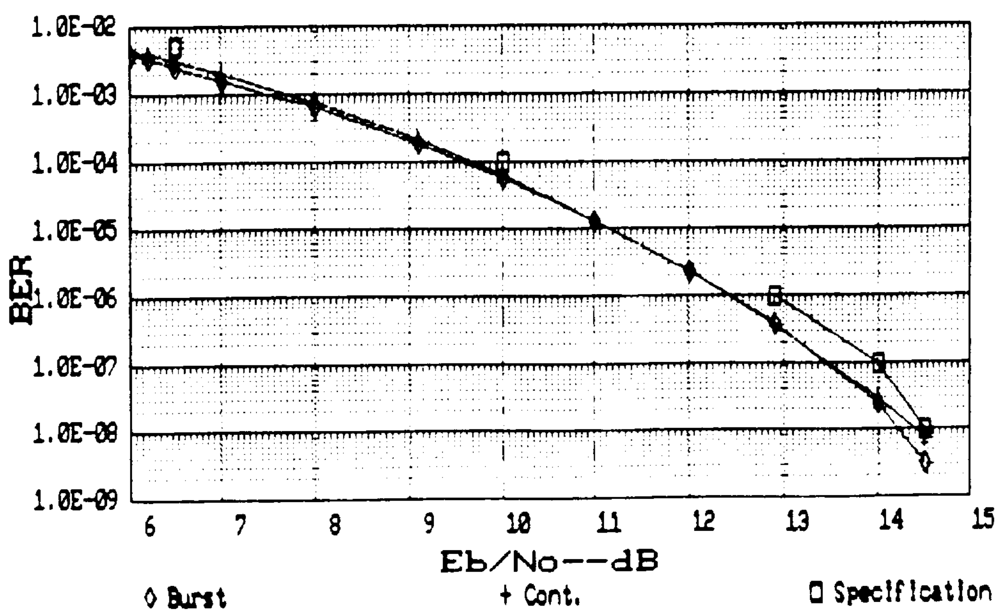

Figure 8 Downlink MODEM BER vs E_b/N_o

Figure 8 shows the downlink BER versus E_b/N_o curves, and the specification BER curves are also shown for comparison. The downlink BER indicates mainly the On-Board Modulator and the E/S Demodulator performance. The BER versus E_b/N_o for burst-mode and continuous mode are very similar. The BER versus E_b/N_o as measured is better than the specifications, for the burst mode about 0.3 to 0.6 dB better than the On-Board Modem specification.

The relationship between the uplink and downlink E_b/N_o was tested for the given BER and the results are shown in Figure 9. Although there is degradation, the relationship

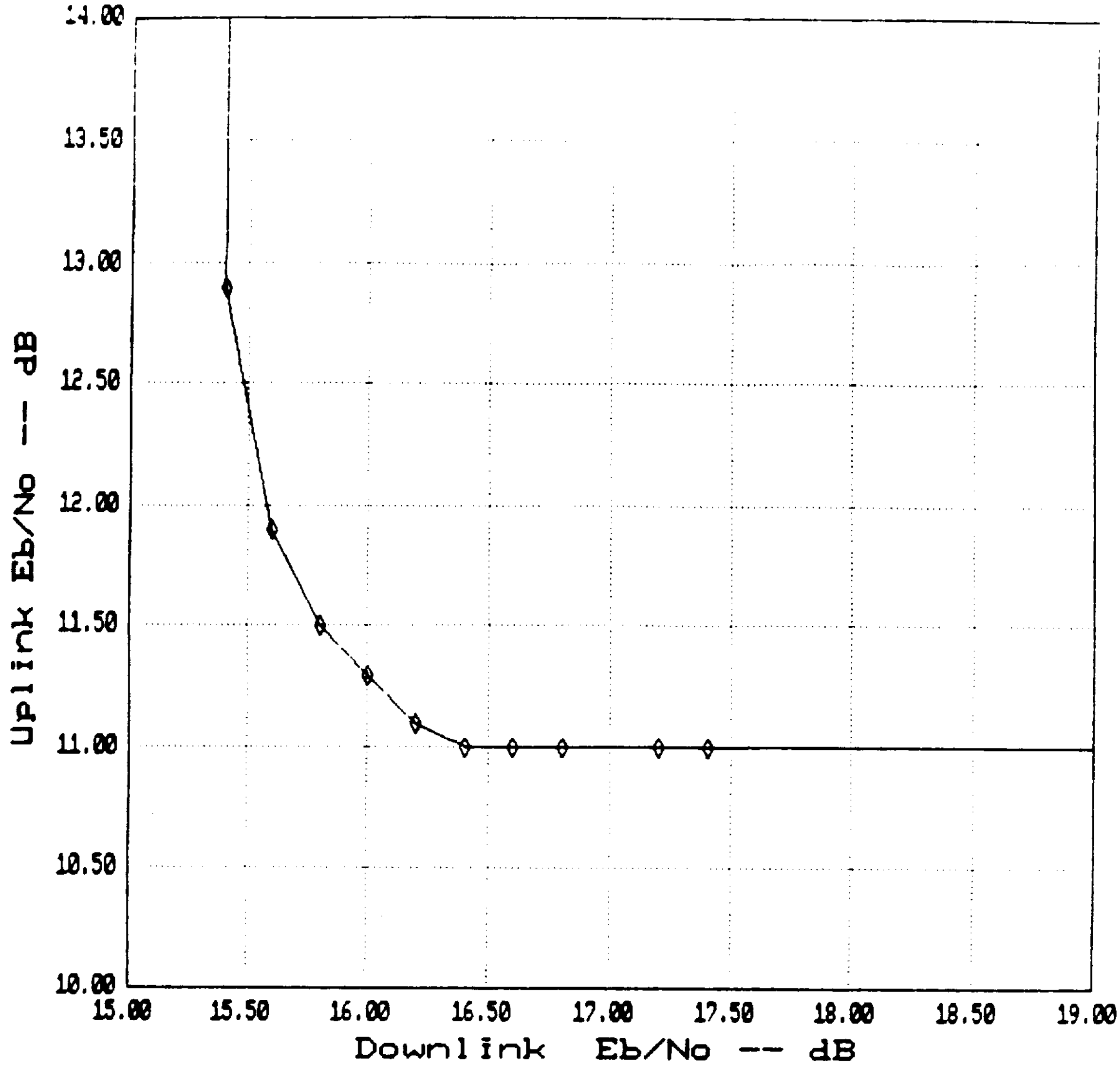

Figure 9 Uplink and Downlink Relationships
(with OB Modem, BER = 10^{-5}, measured)

is very close to that in Figure 4, i.e., the uplink and downlink are well isolated from each other.

MultiCarrier Demultiplexer and Demodulator

Under R&D contract to TELESPAZIO / ALCATEL (Italy/France), INTELSAT has sponsored a proof-of-concept unit of a MultiCarrier Demultiplexer Demodulator (MCDD) [Ref. 7]. The general structure of a MCDD consists of two main blocks: the demultiplexer and the demodulator. The demultiplexer separates the channels and down-converts them to baseband. The demodulator is a single-channel demodulator that recovers the transmitted bit stream and outputs it to a baseband switch matrix. The bit rate of this MCDD can not be varied and only one channel

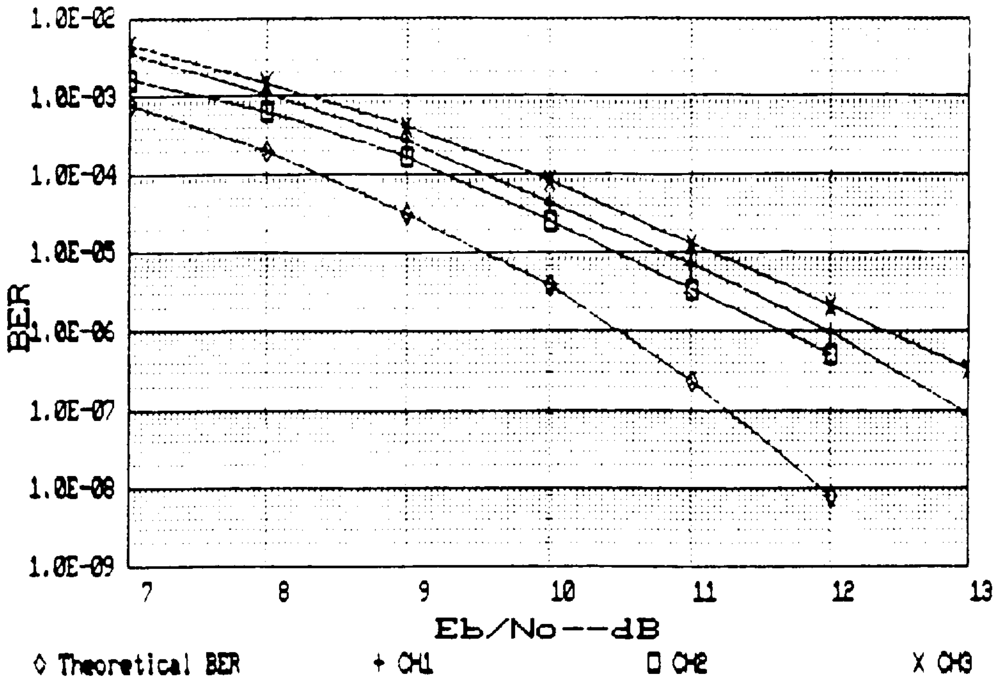

Figure 10 MCDD BER vs E_b/N_o

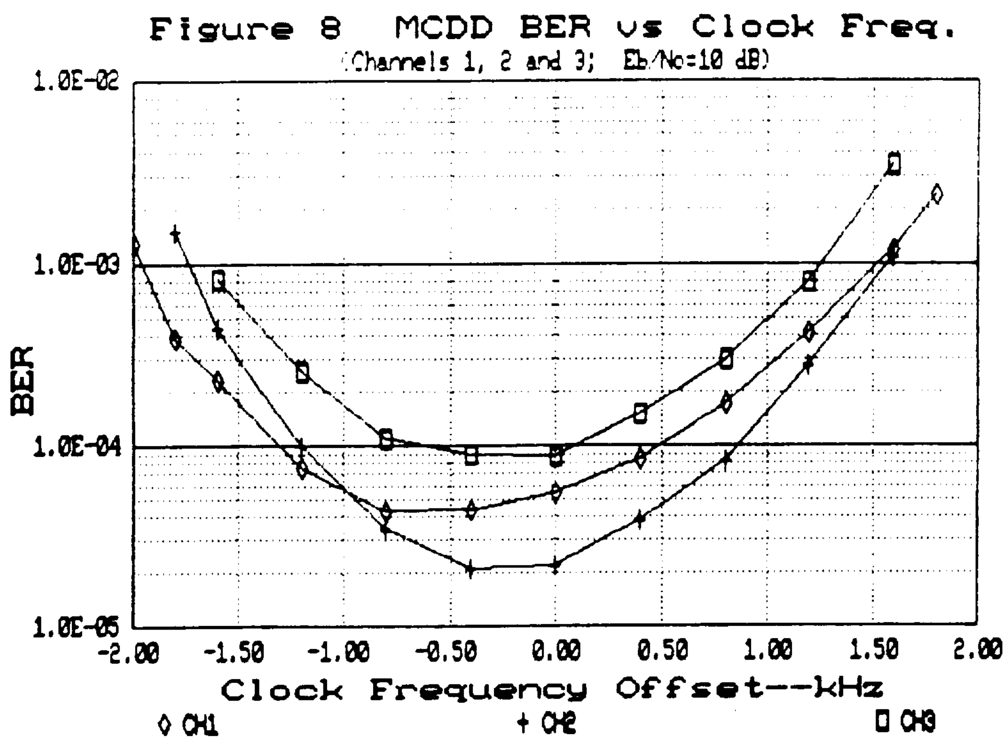

Figure 11 MCDD BER vs Clock Frequency Offset

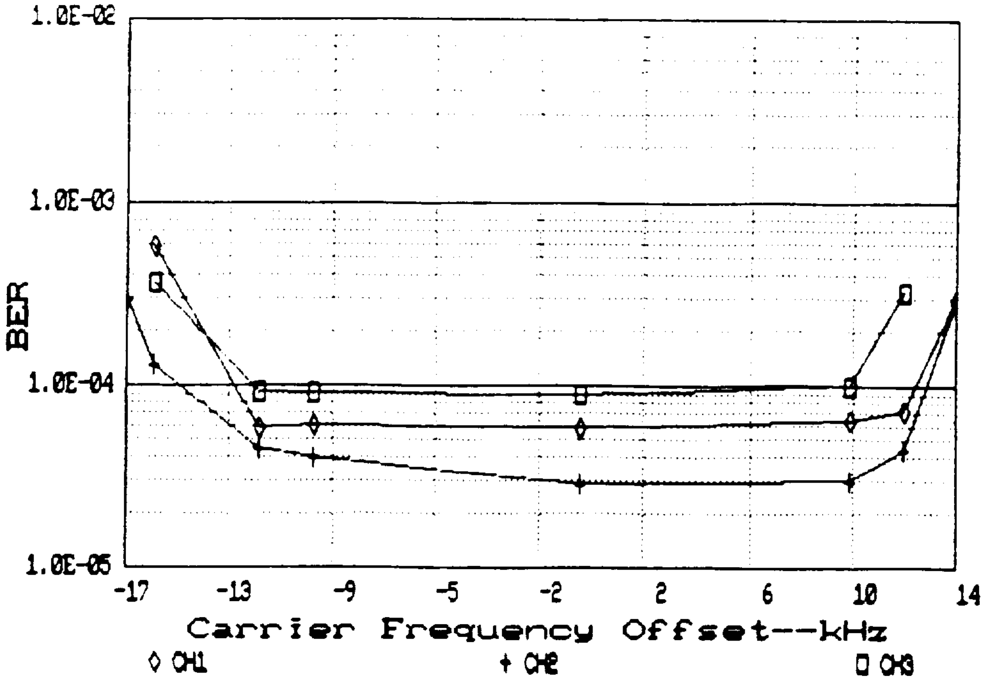

Figure 12 MCDD BER vs Carrier Frequency Offset

can be processed at any one time. The FDMA signal with a 10-MHz bandwidth, occupied by 3 channels at 4.4 Mbit/s transmission rate, or by 12 channels at 1.1 Mbit/s transmission rate, is sampled at a rate of about 20 MHz and fed into the demultiplexer, which uses a per-channel, "analytic signal" approach. The MCDD contains not only the digital portion of the system but also the analog front end. At the input of the MCDD, an Analog Input Interface is provided that is able to accept the signal at intermediate frequency (140 MHz), to perform the anti-alias filtering and the down-conversion to baseband, so that the final analog-to-digital conversion is done at the Nyquist rate. At the output of the MCDD a Digital-to-Analog Converter is used for the purpose of testing, and allows an oscilloscope to be used to observe scattering diagrams and other significant parameters.

The MCDD tests were performed at INTELSAT, for 6 channels, 3 at 4.4 Mbit/s data rate and 3 at 1.1 Mbit/s data rate, and consisted of: BER versus E_b/N_o, and BER sensitivities to clock frequency offset, carrier frequency offset, baseband signal amplitude variation, and adjacent channel interference (ACI). Figures 10, 11, and 12 show the performance of BER versus E_b/N_o, clock frequency offset, and carrier frequency offset for the 4.4 Mbit/s data rate.

In the Adjacent Channel Interference test, two adjacent channels (upper and lower) are the interfering channels. Measurements are only performed for the center channel. The other two channels are used for producing interference and the MCDD does not demodulate them. The degradation due to the ACI interference is no more than 0.2 dB loss for the 4.4 Mbit/s data rate case.

The BER versus E_b/N_o results are acceptable. However, bit synchronization needs to be improved in the case where E_b/N_o is equal to or less than 8 dB.

BaseBand Processor

Under R&D contract to NEC (Japan), INTELSAT developed POC hardware and software for a BaseBand Processor (BBP) for INTELSAT IBS services and for the lower rates in the IDR services [Ref. 8]. The hardware consists of 12 printed wired boards: one TDM/TDMA Converter, one TDMA/TDM Converter, one FDMA Buffer, five for Switch Circuits, and four for the Control Unit; the block diagram is shown in Figure 13. The TDMA/TDM Converter converts the input data format of TDMA to that of TDM. The FDMA Buffers 1 and 2 convert the input data rate to that required in the Switch Module Array (SMA). Switch Circuits perform data rate changes and all switching functions. The TDM/TDMA Converter converts the output data format of TDM to that of TDMA. The Control Unit provides various kinds of clocks, timing signals and read address data for the other subsystems.

The principal functions of the BBP consist of data rate changing; traffic routing at byte level, including Multiplex (TDM-Down), Multi-cast and Distribution, etc.; TDM/TDMA and TDMA/TDM conversions; and Diagnosis.

IBS/IDR BBP tests include communications between the Host Computer and the BBP (Command and Telemetry), data uploading and verification, hardware control (status, switching), switching functions (multi-cast, TDM-down, distribution, data rate changes), and diagnosis function (Column Control Diagnosis and Switching Module Diagnosis). The IBS/IDR BBP performance meets the specifications.

CONCLUSION

OBP systems in several forms are likely to be very significant payload items, and INTELSAT has sponsored their development in the 1980s. The system benefits and constraints are becoming clearer as a result of such work: connectivity, improved link budgets and flexibility are the main objectives; payload constraints include mass, power consumption and reliability with redundancy and diagnostics.

Recent tests at INTELSAT have verified the correct functioning of the On-Board Modem, the FET MSM, the MCDD and the BBP. The Modem and FET MSM are ready for specification development, whereas the MCDD and BBP need to be further developed as engineering models and further tests will be necessary.

A companion poster paper [Ref. 9] shows some more details of the measurements of these OBP subsystems.

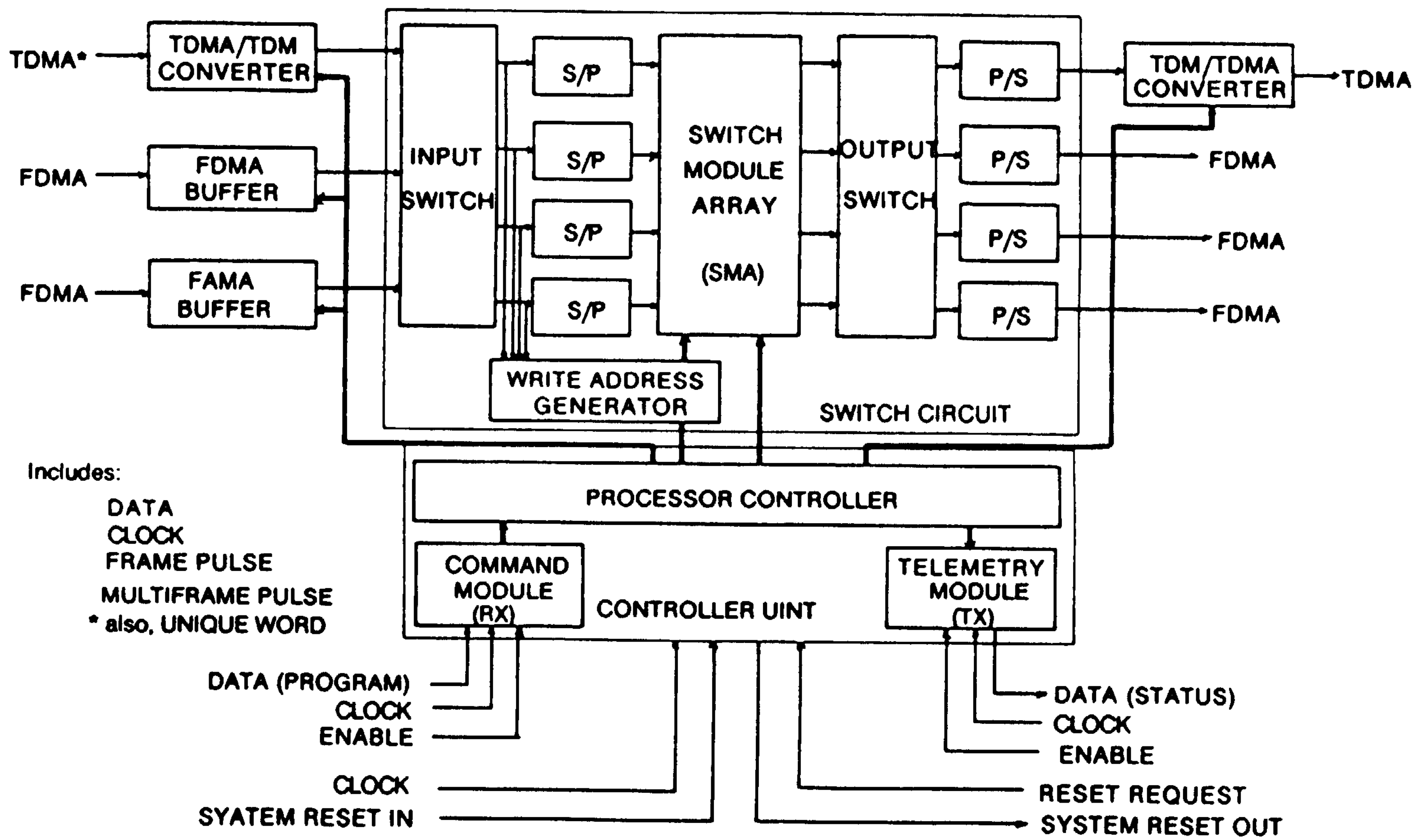

Figure 13 IBS / IDR BaseBand Processor (BBP)

REFERENCES

1. P. Nuspl, R. Peters, T. Abdel-Nabi and N. Mathews, "On-board Processing for Communications Satellites: Systems and Benefits", INTERNATIONAL JOURNAL OF SATELLITE COMMUNICATIONS, Vol. 5, No. 2, pp. 65-76, Wiley-Interscience, April-June 1987.

2. J. Lunsford, J. Phiel, R. Bedford and S. Tamboli, "SSTDMA System Design", to be published in Special Issue on SS-TDMA, COMSAT TECHNICAL REVIEW, COMSAT Labs, Clarksburg, MD, 1991.

3. Y. Takimoto, S. Kitazume and N. Komiyama, "Satellite Switching Center with Diagnostics for SS-TDMA System", Conference Record, GLOBECOM'86, Houston, Vol. 3, paper 47.1, December 1986.

4. K. Betaharon, S. Kitazume, Y. Takimoto, and N. Komiyama, "Advanced Satellite Switching Center with On-Board Diagnostics", Proc. ICDSC-7, Munich, May 1986.

5. P.V. de Santis, "Non-Regenerative Satellite Switched FDMA (SS/FDMA) Payload Technologies", INTERNATIONAL JOURNAL OF SATELLITE COMMUNICATIONS, Vol. 5, No. 2, pp. 171-182, Wiley-Interscience, April-June 1987.

6. T. Ishizu, Y. Kazekami, H. Sawada and K. Kinuhata, "A Design Approach for On-Board Modems", Conference Record, ICC'86, Toronto, Vol. 3, pp. 1814 - 1820, June 1986.

7. E. Saggese and G. Chiassarini, "SAW and Digital Technologies in Multicarrier Demodulators", INTERNATIONAL JOURNAL OF SATELLITE COMMUNICATIONS, Vol. 7, No. 4, pp. 295-306, Wiley-Interscience, November 1989.

8. T. Kumagai, Y. Takeshima, S. Senba, Y. Ohgushi and P.P. Nuspl, "On-Board Processor for INTELSAT Business Services", Proc. ICDSC-8, Guadeloupe, April 1989.

9. P.P. Nuspl, G. Dong and H.C. Seran, "Laboratory Measurements of On-Board Subsystems", poster paper at Second NASA Space Communications Technology Conference, Onboard Switching and Processing, Cleveland, November 1991.

ADDITIONAL BIBLIOGRAPHY
(chronological)

Y. Kazekami, H. Sawada, K. Kinuhata and P. Nuspl, "Hardware Implementation of On-Board Modem", Conference Record, GLOBECOM'85, New Orleans, December 1985.

P. Nuspl, R. Peters and T. Abdel-Nabi, "On-Board Processing for Communications Satellite Systems: Systems and Benefits", Proc. ICDSC-7, Munich, May 1986.

K. Betaharon, K. Kinuhata, P. Nuspl, and R. Peters, "On-Board Processing for Communications Satellite Systems: Technologies and Implementation", Proc. ICDSC-7, Munich, May 1986.

K. Betaharon, K. Kinuhata, P. Nuspl, and R. Peters, "On-board Processing for Communications Satellite Systems: Technologies and Implementations", INTERNATIONAL JOURNAL OF SATELLITE COMMUNICATIONS, Vol. 5, No. 2, pp. 139-146, Wiley-Interscience, April-June 1987.

F. Ananasso and P. de Santis, "On-Board Technologies for User-Oriented SS-FDMA Satellite Systems", Proc. ICC'87, pp. 8.2.1-8.2.5, Seattle, June 1987.

N. Mathews, "Performance Evaluation of Regenerative Digital Satellite Links with FEC Codecs", SATELLITE INTEGRATED COMMUNICATIONS NETWORKS, North-Holland, 1988.

P. de Santis, "Reconfigurable On-Board Connectivity for INTELSAT Thin Route Services", Proc. ICDSC-8, Guadeloupe, April 1989.

Legend:

ICC - International Conference on Communications (IEEE)
ICDSC - International Conference on Digital Satellite Communications