A B-ISDN-COMPATIBLE MODEM/CODEC*

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ABSTRACT

Coded modulation techniques for development of a B-ISDN-compatible modem/codec are investigated. The selected baseband processor system must support transmission of 155.52 Mbit/s of data over an INTELSAT 72-MHz transponder. Performance objectives and fundamental system parameters, including channel symbol rate, code rate, and the modulation scheme, are determined. From several candidate codes, a concatenated coding system, consisting of a coded octal phase shift keying modulation as the inner code and a high-rate Reed-Solomon as the outer code, is selected, and its bit error rate performance is analyzed by computer simulation. The hardware implementation of the decoder for the selected code is also described.

INTRODUCTION

Current INTELSAT V/V-A time-division multiple access (TDMA) links use quadrature phase shift keying (QPSK) modulation with a transmission rate of 60 Msymbol/s. The INTELSAT V/V-A system has a transponder frequency spacing of 80 MHz and a usable bandwidth of 72 MHz per transponder. With forward error correction (FEC) coding of rate 7/8, the bandwidth efficiency of the QPSK TDMA system is about 1.31 bit/s/Hz of the allocated bandwidth.

A recently developed coded octal PSK (COPSK) modem with a transmission rate of 60 Msymbol/s supports an information rate of 140 Mbit/s. This modem has been field tested to demonstrate restoration of the TAT-8 fiber optic cable by satellite. The implemented 140-Mbit/s modem/codec consists of a 16-state trellis code of rate 7/9 and an OPSK modem (ref. 1). The bandwidth efficiency of the 140-Mbit/s COPSK system is 1.57 bit/s/Hz of the allocated bandwidth, which is an improvement of 33 percent over the QPSK TDMA system.

The synchronous optical network (SONET) is a family of interfaces primarily for use in optical networks. The SONET standard is designed to specify how optical signals would be transported between a number of different vendors' equipment and networks. This standard, along with several other specifications, provides an interface to broadband integrated services digital networks (B-ISDNs). A B-ISDN provides broadband services such as broadcast TV, high-definition TV, and transmission of database files at a high data rate. The standard line bit rate of OC-3 (optical carrier level 3) in the SONET hierarchy is 155.52 Mbit/s, which equals the standard bit rate for B-ISDN.

Given the high reliability of satellites, it is advantageous for network operators to have available economical, B-ISDN-compatible links via the INTELSAT system using only one 72-MHz transponder. Such satellite links can interconnect B-ISDN networks and provide early introduction of this service. Satellites also offer worldwide connectivity and, if B-ISDN is to prosper in many areas of the world, then satellite support is

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necessary. Satellites can also act as a "safety valve" in optical fiber networks. Note that, in the case of fiber failure or network congestion, traffic can be routed through a satellite channel on a demand-assigned basis.

This paper investigates the design, performance, and implementation of a B-ISDN-compatible modem/codec. System performance objectives and parameters are briefly reviewed, and OPSK is selected as the modulation format because of its constant envelope and the high power efficiency achievable when combined with an appropriate code. Coded modulation techniques, including Ungerboeck codes and Imai-Hirakawa codes, are then briefly reviewed. The selected code is an Imai-Hirakawa code, with block/convolutional component codes concatenated with a high-rate Reed-Solomon (RS) code in order to achieve high integrity. The hardware implementation and bit error rate (BER) performance of the proposed code over an additive white Gaussian noise (AWGN) channel and a typical INTELSAT V nonlinear channel are presented, and the flexibility of the decoder for transmission of 140 Mbit/s is examined in detail.

SYSTEM PARAMETERS AND PERFORMANCE OBJECTIVES

For a given information bit rate, fundamental parameters for a coded modulation system include the channel symbol rate, the code rate (R), the modulation scheme, and the expected error performance. A transmission symbol rate of 60 Msymbol/s is preferred because the QSPK TDMA system is operating at this rate, and hence the available subsystems, such as transmit and receive filters and equalizers, can also be used in the B-ISDN system, thus reducing the overall unit cost. Also, high-level modulation schemes are sensitive to phase noise. The main sources of phase noise are the group delay distortion of pulse-shaping and satellite-multiplexing filters, AM/AM and AM/PM nonlinearities, residual phase modulation in high-power amplifiers (HPAs), and carrier phase noise. Group delay distortion of filters can be almost perfectly equalized when the channel symbol rate is 60 Msymbol/s or less; however, an equalizer for higher channel symbol rates might not perform as well.

International standards for the error performance of B-ISDNs are not yet available. However, it is expected that a BER of approximately 10^{-10} for 90 percent of the available time will be adapted by the CCITT for broadband service.

Extensive link analysis, laboratory hardware measurements, and field trials have indicated that the INTELSAT V transponders are primarily interference limited, not thermal noise limited, when supporting very high data rate services (ref. 2). Bandwidth efficient coded modulation schemes, suitable for high-speed implementation, do not afford sufficient power efficiency for correcting all the errors caused by the link interferences. The BER vs E_b/N_o performance curves exhibit unresolvable errors at bit error rates of 10^{-7} and less. Therefore, a concatenated coding system, consisting of a power- and bandwidth-efficient inner code and a high-rate RS outer code was considered for achieving the required BER performance of 10^{-10}. Performance objectives and system parameters for the B-ISDN codec/modem are summarized in Table 1.

CANDIDATE MODULATION SCHEMES

The transmission of 155.52 Mbit/s over INTELSAT V transponders requires a bandwidth efficiency of about 1.94 bit/s/Hz, or an improvement of 48 percent over the QPSK TDMA system. Because the required bandwidth efficiency cannot be achieved by QPSK modulation, higher level modulation schemes such as OPSK or 16-ary signal constellations must be considered.

Candidate modulation schemes for the B-ISDN channel include OPSK, 16-ary PSK, and 16-ary quadrature amplitude modulation (QAM).

OPSK modulation, together with a suitable code, can achieve good power and bandwidth efficiency over the satellite channels. Sixteen-ary PSK is also a bandwidth-efficient modulation scheme; however, it has not yet been implemented for high-speed applications. The performance of 16-ary PSK modulation is very sensitive to phase noise, and its demodulator requires fine resolution for distinguishing between the 16 points closely packed on the circumference of a circle. Moreover, the complexity of the synchronization circuits for symbol timing and carrier and clock recovery is greater than that for the OPSK demodulator.

Table 1. B-ISDN-Compatible Codec/Modem Performance Objectives and System Parameters

Nominal Information Rate	155.52 Mbit/s
Nominal Channel Symbol Rate	60 Msymbol/s
Nominal Code Rate	≈ 5/6
Mode of Operation	Continuous
Satellite Transponder	INTELSAT V, V-A, or VI
Usable Transponder Bandwidth	72 MHz
Allocated Bandwidth	80 MHz
Coverages	Hemispheric, Zonal
BER Goals:	
IF Loopback	Better than 10^{-10} at E_b/N_0 = 11 dB
Typical Nonlinear Channel	Better than 10^{-10} at E_b/N_0 = 14 dB
Energy Dispersal	Scrambling, in accordance with CCIR Rec. 359-3

Sixteen-ary QAM is a power- and bandwidth-efficient modulation scheme, but is most suitable for linear channels. For the present application, the earth station HPAs, and particularly the satellite traveling wave tube amplifiers (TWTAs), must operate in the nonlinear region near their saturation point. Therefore, the BER performance of the 16-ary QAM is not expected to meet the system specifications.

Based on the above factors, OPSK appears to be the only viable candidate modulation method. Therefore, coded OPSK modulation techniques are examined in the next section.

COPSK MODULATION TECHNIQUES AND THE SELECTED CODES

The area of power- and bandwidth-efficient coded modulation techniques has been of great research interest for several years. In addition to the class of coded continuous-phase frequency shift keying (CPFSK) modulation schemes, research in this area has focused in two closely related areas now known as Ungerboeck codes and Imai-Hirakawa codes. CPFSK modulation schemes, which include the class of multi-*h* codes, are not suitable for the present application because of their low power efficiency and the unmanageable complexity of the modem and codec hardware implementation operating at the required speed.

UNGERBOECK CODES

In 1982, Ungerboeck (ref. 3) introduced the concept of "set partitioning" and applied this idea to constructing bandwidth-efficient trellis codes. A properly designed trellis code can provide significant coding gain over an uncoded modulation system. Coding gains of about 4 to 5 dB can readily be achieved with a low- to moderate-complexity decoder, at the expense of a more complicated modem.

The hardware implementation complexity of the decoder for Ungerboeck codes depends on the number of encoder states and the code rate, $R = k/n$. The code rate must be selected to minimize the complexity of branch metric computations.

IMAI-HIRAKAWA CODES

The multilevel coding method proposed in 1977 by Imai and Hirakawa (ref. 4) is convenient for high-speed implementation and, for a selected modulation signal space, allows a wide range for the code rate.

In a multilevel/phase signal space, the Euclidian distances between a particular signal point and the remaining points in the signal set are not equal. Since the distance between adjacent signal points is much smaller than the maximum distance between elements in the signal space, more code redundancy must be allocated for encoding the adjacent points. Similarly, the information bits that distinguish between signal points which are far from each other can be encoded by a high-rate code or remain uncoded.

The structure of the class of codes known as the Imai-Hirakawa codes is based on the above concept, and they are generated by several encoders of various rates, as indicated in Figure 1. Low-rate codes are used for encoding the adjacent symbols, and high-rate codes are selected for encoding signal points located a large

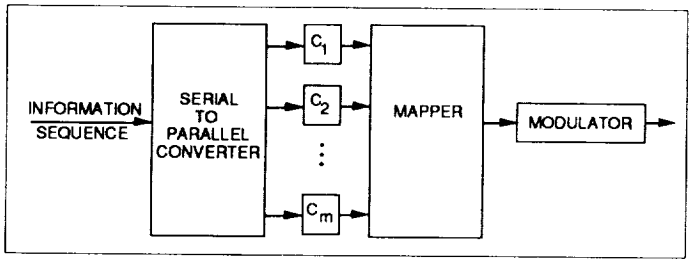

Figure 1. A Coded Modulation System Using Imai-Hirakawa Codes

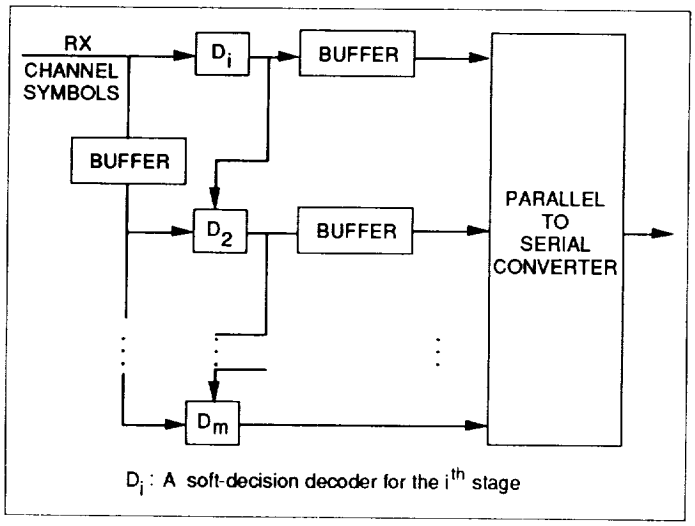

Figure 2. Multistage Decoding Procedure for Imai-Hirakawa Codes

distance from each other. For a signal space with 2^m elements, $C_i = (n, k_i, d_i)$, $1 \le i \le m$, constitutes the set of m component block codes with a common code length n, where $R_i = k_i/n$ defines the code rate and d_i denotes the minimum Hamming distance for the ith code. Both block codes and convolutional codes can be used as the component codes.

Generalized versions of the Imai-Hirakawa codes have been designed by Ginzburg (ref. 5) and Sayegh (ref. 6). In particular, Sayegh described the efficient multistage decoding procedure of Figure 2, in which the most error-prone information bits are estimated first, using *a posteriori* probabilities based on the received channel symbols and the code structure. These estimates are then used in later decoding stages to estimate the successively less error-prone information bits.

Power- and bandwidth-efficient Imai-Hirakawa codes can be readily constructed by using the available optimum block/convolutional codes as the component codes. More importantly, available high-speed decoders can be used in the multistage decoding procedure.

Among several candidate coded OPSK modulation schemes, a block/convolutional Imai-Hirakawa code of rate 13/15, affording an asymptotic coding gain of 3.58 dB over uncoded QPSK, was selected as the inner code (ref. 7). While other coded QPSK modulation schemes potentially might yield a higher power/bandwidth efficiency, this particular code was chosen mainly because of its simplicity of hardware implementation.

The encoder for the block/convolutional code of rate 13/15 consists of three component encoders whose outputs are arranged in a 3-row by 15-column array. The first row of the array is a block of 15 consecutive encoded bits, generated at the output of a punctured convolutional encoder of rate 2/3 and constraint length 7. The second component code is a single-parity check code of length 15 and rate 14/15, and the third row of the array is a block of 15 uncoded information bits, which is a codeword in the universal (15, 15, 1) code of rate 1. The 3 bits in each column of the array specify one of the points in the OPSK signal space.

After analyzing the burst error statistics of the inner code, an 8-symbol error correcting (255,239) RS outer code was found suitable for achieving the required BER performance. The overall rate of this concatenated coding system is approximately 13/16 and requires a channel symbol rate of 64 MHz for supporting 155.22-Mbit/s data and synchronization overhead bits.

The required channel symbol rate can be reduced to 62.4 MHz by using a (15, 15, 1) universal code instead of the (15, 14, 2) parity check code in the second encoding stage. In this case, the inner code operates at 58.5 MHz. Finally, a 140-Mbit/s codec can be realized if the inner code of rate 13/15 is concatenated with a (195, 175) 10-error-correcting shortened Reed-Solomon code requiring a channel symbol rate of 60 MHz.

PERFORMANCE ANALYSIS

The BER performance of the considered concatenated coding system was evaluated by first examining the performance of the inner code, without the RS outer code, under various link conditions. Then, the performance of the concatenated coding system was evaluated under worst-case link conditions.

The BER performance of the OPSK coded modulation of rate 13/15 for transmission of 155.52 Mbit/s was evaluated by computer simulation. The received channel symbols were first quantized by a 64-level quantizer, and then compressed to 3 bits by a nonlinear mapping. Over an AWGN channel and at a BER of 10^{-5}, the BER performance of this quantization scheme is within 0.2 dB of the performance of the coded system using unquantized channel symbols.

BER performance results over an AWGN channel and over a typical INTELSAT V nonlinear channel are shown in Figure 3. The system environment and performance parameters considered in the computer simulations are summarized in Table 2. For the AWGN channel, a coding gain of 1.2 dB over uncoded QPSK is observed at a BER of 10^{-5}. An effective coding gain of about 2.5 dB is expected at a BER of 10^{-8}, which can be obtained by extrapolating the BER performance curve of Figure 3. The 1.08-dB discrepancy between the asymptotic coding gain for this code (3.58 dB) and the effective coding gain of 2.5 dB is due to the adversary path multiplicity in the k = 7 punctured convolutional code of rate 2/3, suboptimum multistage decoding (instead of maximum-likelihood decoding), and 3-bit soft-decision quantization (instead of an infinite number of quantization levels).

At a BER of 10^{-4}, the performance of the single nonlinear satellite channel degrades by about 1.5 dB relative to the performance of the AWGN channel, due to link nonlinearities and intersymbol interference. The BER performance degrades by an additional 1 dB with one entry of co-channel interference (CCI) at a power level of -18.5 dB with respect to the desired channel. The two 60-Msymbol/s adjacent channels located at +80 and -80 MHz relative to the center frequency of the desired channel degrade the BER performance by an additional 0.3 dB.

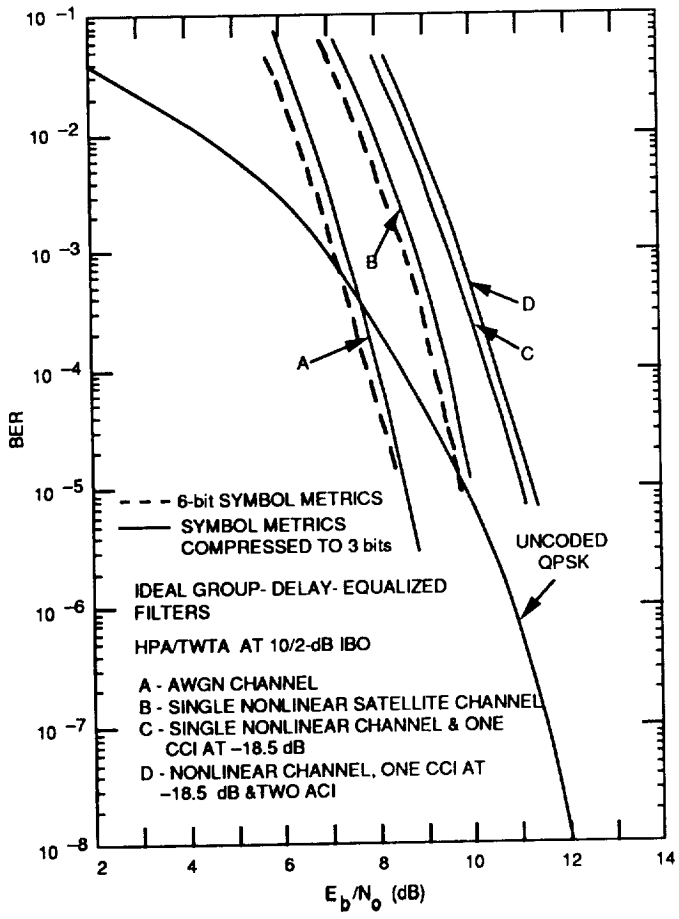

Figure 3. Ber Performance of the Rate 13/15 Code Over the Nonlinear Satellite Channel

The BER performance results shown in Figure 3 are obtained by assuming that the group delay distortion of the modem filters and satellite multiplexing filters is ideally equalized. In a real channel, phase noise caused by the carrier oscillator, link nonlinearities, and group delay distortion of filters degrades system performance. At a BER of 10^{-4}, degradations due to unequalized group delay distortion can be as much as 0.8 dB.

The BER performance of the concatenated coding system was also evaluated by computer simulation. The results obtained are shown in Figure 4 for the nonlinear channel with two ACI and one CCI at -18.5 dB. The dashed curves show the BER performance of the inner code, without the RS outer coding. The performance of the concatenated coding system with channel symbol rates of 64 Msymbol/s and

Table 2. Summary of System Variables and Assumptions Used in the Computer Simulations

Number of Samples per Symbol	16
HPA Input Backoff	10 dB
Satellite TWTA Input Backoff	2 dB
CCI Level	–18.5 dB
Separation Between Adjacent Channels	80 MHz
Rolloff Factor for Square-Root Nyquist Modem Filters	40%
Ideally Group Delay Equalized Filters	
Perfect Symbol Phase and Symbol Timing	

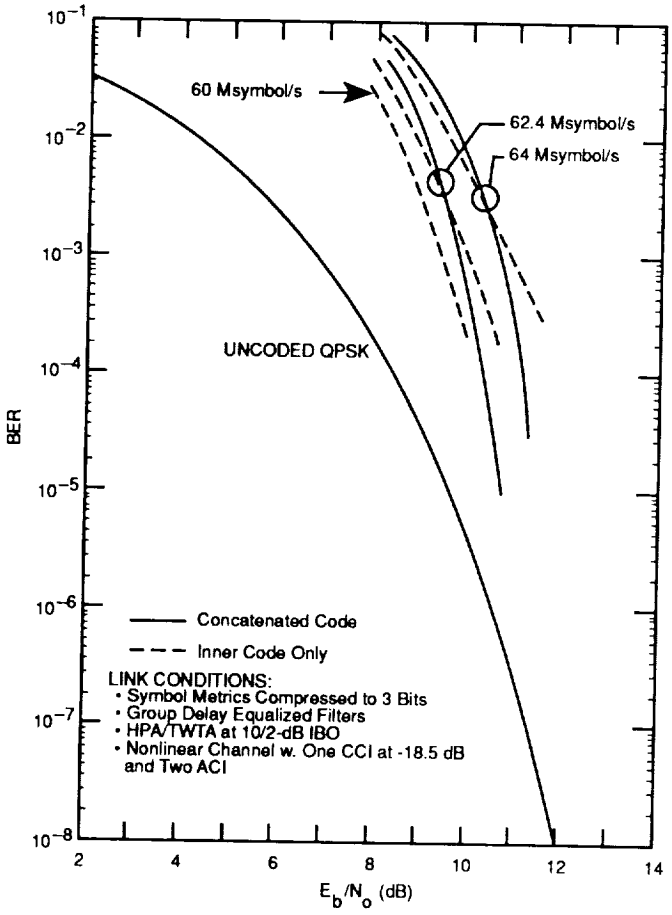

Figure 4. BER Performance of the Concatenated Coding System Over the INTELSAT V Transponders

62.4 Msymbol/s, corresponding to the inner codes with and without parity check coding in the second stage, are depicted as solid curves. Because of its lower channel symbol rate, the 62.4-Msymbol/s system outperforms the 64-Msymbol/s system by about 1 dB. The 62.4-Msymbol/s system is expected to achieve a BER of 10^{-10} at less than 12 dB, which allows sufficient margin for modem implementation loss and the transmission link.

SYNCHRONIZATION

To achieve synchronization and OPSK phase ambiguity resolution, the system employs an innovative digital technique which synchronizes and controls the decoder while simultaneously providing an on-line BER measurement at the codec output. The synchronization method is unique in that the overhead data are periodically inserted into the encoder during transmit data processing. When transmitting data at 155.52 Mbit/s, the overhead data are added at a rate of 1 percent in the form of a single 40-bit data packet inserted into the multistage encoder once after every 100 information blocks have been processed. The encoded overhead packet is largely recognizable at the input to the decoder because the unique word information is transmitted through the uncoded stage of the multistage encoder while the other two stages encode zeros during the overhead packet. This results in a stream of consecutive OPSK symbols that can take on one of two BPSK points in the OPSK signal space. The unique word detection circuit is able to detect the unique word regardless of the phase state the modem is locked in, and, combined with the hard decision data output from the modem, the synchronization circuit effects a digital phase rotation of the data which removes any phase rotation before decoding takes place.

The innovative synchronization scheme offers several advantages over conventional synchronization approaches including elimination of the need for large asynchronous buffers for overhead insertion/removal, insertion of the overhead packet directly into the encoder (overhead packet is directly linked to the structure of the code), removal of the need for a preamble sequence to resolve modem phase ambiguity, elimination of another step in phase-locked loop circuitry, and the side benefit of providing a real-time BER monitoring capability since the overhead data are passed through the decoder before being removed from the data stream.

A number of alarms and operational features from relative CCITT recommendations were incorporated into the proof-of-concept hardware model, which renders the codec design suitable for manufacturing and field deployment. Included among the operational enhancements is the ability of the system to detect an incoming alarm indication signal (AIS) from upstream equipment, the ability to generate an AIS signal when a fatal error in the coded modulation system is present, on-line BER monitoring capability, high BER alarm, standard coded mark inverse (CMI) high speed interface compatibility and plesiochronous/Doppler buffering for operation with satellites in inclined orbits up to 3°. The most prominent maintenance features include the development of universal test equipment that is compatible with all boards and subsystems within the system, baseband loopback capability, clock and data activity detectors and indicators, power supply indicators, and ample test points.

HARDWARE IMPLEMENTATION

Detailed design and construction of the multistage inner coding system has been completed, and hardware design, construction, and test of the RS outer codec is under way and will be completed in 1991.

To implement the concatenated multistage inner code and the RS outer code, the concatenated coding system uses five circuit boards housed in a common chassis with backplane intercommunications. The circuit boards employ an efficient mixture of high-speed emitter-coupled logic (ECL), intermediate speed complementary metal-oxide semiconductor (CMOS) and transistor-transistor logic (TTL) circuitry, and analog phase-locked loop components. The first circuit board implements the high-speed data interfaces to the system, the phase-locked loop timing circuits, and the serial-to-parallel data conversion function. The CMOS/TTL design of the second board executes the outer code RS encoding, decoding, interleaving, and block code synchronization functions. Parallel use of off-the-shelf RS codec chips supports the system's high data rate throughput. A combination of the parallel RS coding devices and auxiliary codeword memory serves to implement the depth of four interleaving that is necessary for the RS code to effectively combat the system's burst errors. An efficient combination of programmable gate array devices and discrete logic and memory comprise the rest of the second board design. The third board uses programmable and discrete CMOS logic to implement the transmit functions for the inner coding system, including multistage encoding, data scrambling, unique word insertion, data frame construction, and interface to the OPSK modulator. The fourth and fifth boards are responsible for the inner code receive-side processing. In particular, the fourth board operates at a symbol rate of 58.5 Msymbol/s and uses high-speed ECL circuitry to perform OPSK phase ambiguity resolution, inner decoder synchronization, Viterbi metric calculation, parity decoding, universal decoding, and overall decoder timing and control. The fifth board uses a parallel array of commercially available Viterbi codec chips with a mixture of CMOS discrete and programmable logic to implement the Viterbi decoding portion of the multistage decoder, the data alignment function, and the Doppler buffering.

The OPSK modulator accepts 3-bit symbols from the encoder and creates one of the eight phase states in the OPSK signal space. The OPSK demodulator receives the incoming IF signal, makes gain adjustments to the signal path, removes the modulation to recover the carrier, generates symbol timing, and demodulates the data into soft decision quadrature baseband streams. In the past, COMSAT Laboratories developed a 180-Mbit/s OPSK modem for use in its 140-Mbit/s rate-7/9 COPSK system (ref. 2). The basic structure for this design was incorporated into the modem design for this project, with enhancements for additional alarms and operational features.

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